User's Manual

RA4W1 Group

User's Manual: Hardware

32-bit MCU
Renesas Advanced (RA) Family
Renesas RA4 - Efficiency Series

Renesas Electronics
www.renesas.com

Rev.1.00 Mar 2020

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32位MCURenesasAdvanced(RA)
系列RenesasRA4效率系列

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General Precautions

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

一般注意事项

1.防止静电放电(ESD)强电场暴露于CMOS器件时，会导致栅极氧化物的破坏，并最终导致

降级设备操作。必须采取措施，尽可能地阻止静电的产生，并在产生时迅速消散。环境控制必须充分。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量工具，包括工作台和地板都必须接地。操作员还必须使用腕带接地。不得赤手触摸半导体器件。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。

2.通电时的处理通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，并且在供电时寄存器设置和引脚的状态是不确定的。在将复位信号施加到外部复位管脚的成品中，从通电到复位过程完成，管脚的状态不能得到保证。类似地，通过片内上电复位功能复位的产品中的引脚状态从通电到达到指定复位电平的时间都无法保证。

3.关机状态下的信号输入不要在设备关机状态下输入信号或IO上拉电源。输入此类信号或IO上拉电源导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件劣化。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。

4.未使用引脚的处理按照手册中未使用引脚处理中的说明处理未使用引脚。CMOS产品的输入引脚一般处于高阻状态。在未使用的引脚处于开路状态的情况下，在LSI附近会感应出额外的电磁噪声，相关的直通电流会在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。

5.时钟信号应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序执行过程中切换时钟信号时，请等待目标时钟信号稳定。在复位期间使用外部谐振器或外部振荡器生成时钟信号时，请确保仅在时钟信号完全稳定后才释放复位线。此外，当在程序执行过程中切换到由外部谐振器或外部振荡器产生的时钟信号时，请等待目标时钟信号稳定。

6.输入引脚的电压施加波形由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入由于噪声等原因停留在VIL(Max.)和VIH(Min.)之间的区域内，器件可能会发生故障。当输入电平固定时，以及输入电平通过VIL(Max.)和VIH(Min.)之间的区域时，请注意防止抖动噪声进入设备。

7.禁止访问保留地址
禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些地址，因为不能保证LSI的正确操作。

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Preface

1. About this Document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using the Renesas Microcontroller. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

3. Renesas Publications

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Component	Document type	Description
Microcontrollers	Datasheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	Datasheet	Functional descriptions and specific performance data for software modules
	User's Manual: Software	API reference and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manual and quick start guide for developing embedded software applications with Development Kit (DK), Starter Kit (SK), Promotion Kit (PK), Target Board Kit (TB), Product Examples (PE), and Application Examples (AE)
	User's Manual: Software	
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

Preface

1. 关于本文档

本手册一般由产品概述、CPU说明、系统控制功能、外围功能、电气特性和使用说明组成。本手册描述了微控制器(MCU)超集的产品规格。根据您的产品，某些引脚、寄存器或功能可能不存在。保留存储不可用寄存器的地址空间。

2. Audience

本手册是为使用瑞萨微控制器设计和编程应用程序的系统设计人员编写的。要求用户具备电路、逻辑电路和MCU的基本知识。

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Component	文件类型	Description
Microcontrollers	Datasheet	MCU的特性、概述和电气特性
	User's Manual: Hardware	MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述
	应用笔记	技术说明、电路板设计指南和软件迁移信息
	技术更新(TU)	限制、勘误等产品规格的初步报告
Software	Datasheet	软件模块的功能描述和具体性能数据
	User's Manual: Software	API参考和编程信息
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例
工具和套件，Solutions	用户手册：开发工具	使用开发套件(DK)、入门套件(SK)、促销套件(PK)、目标板套件(TB)、产品示例(PE)和应用示例(AE)开发嵌入式软件应用程序的用户手册和快速入门指南
	User's Manual: Software	
	快速入门指南	
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x, based on C/C++ formatting.
1234	Decimal number. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
ICU.NMICR.NMIMD	Periods separate a function module symbol (ICU), register symbol (NMICR), and bit field symbol (NMIMD)
ICU.NMICR	A period separates a function module symbol (ICU) and register symbol (NMICR)
NMICR.NMIMD	A period separates a register symbol (NMICR) and bit field symbol (NMIMD)
NFCLKSEL[1:0]	In a register bit name, the bit range enclosed in square brackets indicates the number of bits in the field at this location. In this example, NFCLKSEL[1:0] represents a 2-bit field at the specified location in the NMI Pin Interrupt Control Register (NMICR).

6. Unit Prefix

The following unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Prefix	Description
b	Bit
B	Byte. This unit prefix is generally used for memory specification of the MCU and address space.
k	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings:

Term	Description
NC	Not connected pin. NC means the pin is not connected to the MCU.
Hi-Z	High impedance

4. 编号符号

本手册通篇使用以下编号符号：

Example	Description
011b	二进制数。例如，数字3的二进制等价物是011b。
1Fh	十六进制数。例如，数字31的十六进制等值表示为1Fh。在某些情况下，根据CC++格式，显示带有前缀0x的十六进制数。
1234	十进制数。十进制数字通常不带后缀。

5. 排版符号

本手册通篇使用以下印刷符号：

Example	Description
ICU.NMICR.NMIMD	句点分隔功能模块符号(ICU)、寄存器符号(NMICR)和位域符号(NMIMD)
ICU.NMICR	句点分隔功能模块符号(ICU)和寄存器符号(NMICR)
NMICR.NMIMD	句点分隔寄存器符号(NMICR)和位域符号(NMIMD)
NFCLKSEL[1:0]	在寄存器位名称中，方括号中的位范围表示该位置的字段中的位数。在本例中，NFCLKSEL[1:0]表示NMI引脚中断控制寄存器(NMICR)中指定位置的2位字段。

6. 单位前缀

以下单位前缀有时会产生误导。这些单位前缀在本手册中进行了描述，含义如下：

Prefix	Description
b	Bit
B	字节。该单元前缀一般用于MCU的内存规范和地址空间。
k	1000=103。k也用于表示1024(210)，但在本手册中，此单位前缀用于表示1000(103)。
K	1024=210。在本手册中，该单位前缀用于表示1024(210)而不是1000(103)。

7. 特别条款

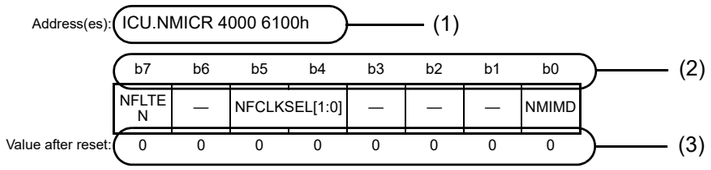
以下术语具有特殊含义：

Term	Description
NC	未连接引脚。NC表示该引脚未连接到MCU。
Hi-Z	高阻抗

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

X.X.X NMI Pin Interrupt Control Register (NMICR)



(4) (5) (6)

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disable the digital filter 1: Enable the digital filter.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. ICU.NMICR 4000 6100h means NMI Pin Interrupt Control Register (NMICR) of Interrupt Controller Unit (ICU) is assigned to address 4000 6100h.

(2) Bit number

This number indicates the bit number. These bits are shown in order from b31 to b0 for a 32-bit register, from b15 to b0 for a 16-bit register, and from b7 to b0 for an 8-bit register.

(3) Value after reset

This symbol or number indicates the value of each bit after a reset. The value is shown in binary unless specified otherwise.
0: Indicates that the value is 0 after a reset.
1: Indicates that the value is 1 after a reset.
x: Indicates that the value is undefined after a reset.

(4) Bit symbol

Bit symbol indicates the short name of the bit field. Reserved bit is expressed with a —.

(5) Bit name

Bit name indicates the full name of the bit field.

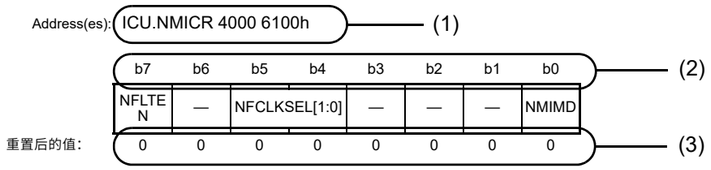
(6) R/W

The R/W column indicates access type: whether the bit field is read or write.
R/W: The bit field is read and write.
R/(W): The bit field is read and write. But writing to this bit field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit field is read-only. Writing to this bit field has no effect.
W: The bit field is write-only. The read value is undefined.

8. 注册说明

每个寄存器描述都包括一个显示位分配的寄存器图和一个描述每个位内容的寄存器位表。这些表中使用的符号示例将在以下部分中描述。以下是寄存器描述和相关位字段定义的示例。

X.X.X NMI引脚中断控制寄存器(NMICR)



(4) (5) (6)

Bit	Symbol	位名称	Description	R/W
b0	NMIMD	NMI检测集	0：下降沿1： 上升沿。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟 Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	NFLTEN	NMI数字滤波器启用	0：禁用数字滤波器1：启 用数字滤波器。	R/W

(1) 功能模块符号、寄存器符号、地址分配

一般表示该寄存器的功能模块符号、寄存器符号、地址分配。ICU.NMICR40006100h表示中断控制器单元(ICU)的NMI引脚中断控制寄存器(NMICR)分配到地址40006100h。

(2) 位号

该数字表示位数。对于32位寄存器，这些位按照从b31到b0的顺序显示，对于16位寄存器，这些位从b15到b0，对于8位寄存器，按照从b7到b0的顺序显示。

(3) 重置后的值

该符号或数字表示复位后每个位的值。除非另有说明，否则该值以二进制显示。0：表示复位后值为0。
1：表示复位后值为1。x：表示复位后该值未定义。

(4) 位符号

位符号表示位域的简称。保留位用—表示。

(5) 位名称

位名表示位域的全称。

(6) R/W

RW列表示访问类型：位域是读还是写。
RW：位域可读写。
R(W)：位域可读写。但是写入这个位域有一些限制。有关限制的详细信息，请参见各个寄存器的说明或注释。R：位域是只读的。写入该位域无效。

W：位域是只写的。读取值未定义。

9. Abbreviations

Abbreviations used in this manual are shown in the following table:

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ECC	Elliptic Curve Cryptography
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating-Point Unit
GSM	Global System for Mobile communications
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter

9. Abbreviations

本手册中使用的缩写如下表所示：

Abbreviation	Description
AES	高级加密标准
AHB	先进的高性能总线
AHB-AP	AHB访问端口
APB	先进的外围总线
ARC	Alleged RC
ATB	高级跟踪总线
BCD	二进制编码的十进制
BSDL	边界扫描描述语言
DES	数据加密标准
DSA	数字签名算法
ECC	椭圆曲线密码学
ETB	嵌入式跟踪缓冲区
ETM	嵌入式跟踪宏单元
FLL	锁频环
FPU	Floating-Point Unit
GSM	全球移动通信系统
HMI	人机接口
IrDA	红外数据协会
LSB	最低有效位
MSB	最高有效位
NVIC	嵌套向量中断控制器
PC	程序计数器
PFS	端口功能选择
PLL	锁相环
POR	Power-On Reset
PWM	脉冲宽度调制
RSA	Rivest Shamir Adleman
SHA	安全哈希算法
S/H	采样和保持
SP	堆栈指针
SWD	串口线调试
SW-DP	串行线调试端口
TRNG	真随机数发生器
UART	通用异步收发器

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Contents

Contents

High efficiency 48-MHz Arm® Cortex®-M4 core, 512-KB code flash memory, 96-KB SRAM, Segment LCD Controller, Capacitive Touch Sensing Unit, Bluetooth Low Energy, USB 2.0 Full-Speed, 14-Bit A/D Converter, 12-Bit D/A Converter, security and safety features.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 48 MHz
- Support for 4-GB address space
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: ITM, DWT, FPB, TPIU, and ETB
- CoreSight™ debug port: JTAG-DP and SW-DP

■ Memory
- 512-KB code flash memory
- 8-KB data flash memory (100,000 erase/write cycles)
- 96-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity
- Bluetooth Low Energy
  - Bluetooth 5.0 core specification compliant BLE transceiver and link layer
  - Supporting LE 1M, 2M and Coded PHY, and LE Advertising extension
  - Dedicated AES-CCM (128-bit blocks) encryption circuit
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 4
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- Controller Area Network (CAN) module

■ Analog
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) ×2 (for ACMPLP)
- Low Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 1
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit (GPT32) × 4
- General PWM Timer 16-bit (GPT16) × 3
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and Battery Backup support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 4
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/256
- GHASH
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Segment LCD Controller (SLCDC)
  - Up to 9 segments × 4 commons
  - Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 3.6 V)
  (1 to 8 MHz when VCC = 1.8 to 2.4 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 3.6 V)
  (24, 32, 48 MHz when VCC = 1.8 to 3.6 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 35 input/output pins
  - Up to 3 CMOS input
  - Up to 32 CMOS input/output
    - Up to 4 input/output 5 V tolerant
    - Up to 1 high current (20 mA)

■ Operating Voltage
- VCC: 1.8 to 3.6 V

■ Operating Temperature and Packages
- Ta = –40°C to +85°C
  - 56-pin QFN (7 mm × 7 mm, 0.4 mm pitch)

高效48-MHzArm®Cortex®-M4内核、512-KB代码闪存、96-KBSRAM、段LCD控制器、
电容式触摸感应单元、低功耗蓝牙、USB2.0全速、14位AD转换器、12位DA转换器、安全和安全功能。

Features

■带浮点单元(FPU)的ArmCortex-M4内核带DSP指令集的Armv7E-M架构最大工作频率：48MHz支持4GB地址空间具有8个区域的Arm内存保护单元(ArmMPU)调试和跟踪：ITM、DWT、FPB、TPIU和ETBCoreSight 调试端口：JTAG-DP和SW-DP

■ Memory
512KB代码闪存 8KB数据闪存（100 000次擦除写入周期） 96KBSRAM 闪存(FCACHE) 内存保护单元 内存镜像功能(MMF) 128位唯一ID

■ Connectivity
低功耗蓝牙
符合蓝牙5.0核心规范的BLE收发器和链路层支持LE1M、2M和编码PHY，以及LE广告扩展专用AES-CCM（128位块）加密电路USB2.0全速(USBFS)模块片上收发器兼容带USB电池充电规范1.2 串行通信接口(SCI)×4UART简单IIC简单SPI 串行外设接口(SPI)×2 I2C总线接口(IIC)×2 控制器局域网(CAN)模块

■ Analog
14位AD转换器(ADC14) 12位DA转换器(DAC12) 8位DA转换器(DAC8)×2（用于ACMPLP） 低功耗模拟比较器(ACMPLP)×2 运算放大器(OPAMP)×1 温度传感器(TSN)

■ Timers
通用PWM定时器32位(GPT32)×4 通用PWM定时器16位(GPT16)×3 异步通用定时器(AGT)×2 看门狗定时器(WDT)

■ Safety
SRAM中的纠错码(ECC) SRAM奇偶校验错误检查 闪存区域保护 ADC自诊断功能 时钟频率精度测量电路(CAC) 循环冗余校验(CRC)计算器 数据操作电路(DOC) 端口GPT(POEG)的输出使能 独立看门狗定时器(IWDT) GPIO回读电平检测 寄存器写保护 主振荡器停止检测 非法内存访问

■系统和电源管理 低功耗模式 支持日历和备用电池的实时时钟(RTC) 事件链接控制器(ELC) DMA控制器(DMAC)×4 数据传输控制器(DTC) 按键中断功能(KINT) 上电复位 具有电压设置的低电压检测(LVD)

■安全和加密 AES128256 GHASH 真随机数生成器(TRNG)

■人机界面(HMI) 段式LCD控制器(SLCDC)
最多9段×4个公共端电容式触摸传感单元(CTSU)

■多个时钟源
主时钟振荡器(MOSC)
(VCC=2.4至3.6V时为1至20MHz)(VCC=1.8至2.4V时为1至8MHz) 副时钟振荡器(SOSC)(32.768kHz) 高速片上振荡器(HOCO)

（VCC=2.4至3.6V时为24、32、48、64MHz） (VCC=1.8至3.6V时为24、32、48MHz） 中速片上振荡器(MOCO)(8MHz) 低速高速片上振荡器(LOCO)(32.768kHz) IWDT专用片上振荡器(15kHz) HOCO MOCOLOCO的时钟微调功能 时钟输出支持

■通用IO端口 最多35个输入输出引脚
最多3个CMOS输入最多32个CMOS输入输出最多4个输入输出5V耐受最多1个高电流(20mA)

■工作电压 VCC：1.8至3.6V

■工作温度和封装 Ta= 40°C至+85°C

- 56-pin QFN (7 mm × 7 mm, 0.4 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a low-power and high-performance Arm Cortex®-M4 32-bit core running up to 48 MHz, with the following features:

- 512-KB code flash memory
- 96-KB SRAM
- Bluetooth Low Energy (BLE)
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M4 core: - Revision: r0p1-01rel0 - Armv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU): - Armv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB of code flash memory. See section 43, Flash Memory.
Data flash memory	8 KB of data flash memory. See section 43, Flash Memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the desired application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF).
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). An area in SRAM0 provides error correction capability using ECC. See section 42, SRAM.

1. Overview

MCU集成了多个系列软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外设，以促进设计可扩展性和基于平台的高效产品开发。

该系列中的MCU采用了运行频率高达48MHz的低功耗高性能ArmCortex®-M432位内核，具有以下特性：

- 512-KB代码闪存
- 96-KB SRAM
- 低功耗蓝牙(BLE)
- 段式LCD控制器(SLCDC)
- 电容式触控感应单元(CTSU)
- USB2.0全速模块(USBFS)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- 安全功能。

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M4内核	最大工作频率：高达48MHz ArmCortex-M4内核：修订版：r0p1-01rel0Armv7E-M架构配置文件符合ANSIIEEEStd754-2008的单精度浮点单元。 Arm内存保护单元（ArmMPU）： Armv7受保护的内存系统架构8个保护区域 SysTick计时器： 由SYSTICCLK(LOCO)或ICLK驱动。

Table 1.2 Memory

Feature	功能说明
代码闪存	最大512KB的代码闪存。请参阅第43节，闪存。
数据闪存	8KB数据闪存。请参阅第43节，闪存。
Option-setting memory	选项设置存储器确定复位后MCU的状态。见第7节，Option-Setting Memory.
内存镜像功能(MMF)	内存镜像功能(MMF)可配置为将代码闪存中所需的应用程序映像加载地址镜像到23位未使用的内存空间（内存镜像空间地址）中的应用程序映像链接地址。您的应用程序代码已开发并链接到从该MMF目标地址运行。应用程序代码不需要知道它存储在代码闪存中的加载位置。请参阅第5节，内存镜像功能(MMF)。
SRAM	具有奇偶校验位或纠错码(ECC)的片上高速SRAM。一个地区在SRAM0使用ECC提供纠错能力。参见第42节，SRAM。

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/USB boot mode. See section 3, Operating Modes.
Resets	14 resets: • RES pin reset • Power-on reset • VBATT-selected voltage power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD).
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Bluetooth-dedicated clock oscillator • Bluetooth-dedicated low-speed on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU).
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT).
Low Power Mode	Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery powered area includes RTC, SOSC, LOCO, wakeup control, backup memory, VBATT_R low voltage detection, and switch between VCC and VBATT. During normal operation, the battery powered area is powered by the main power supply, which is the VCC pin. When a VCC voltage fall is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 12, Battery Backup Function.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection.

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种工作模式： 单芯片模式 SCIU SB启动模式。请参阅第3节，操 作模式。
Resets	14次复位： RES引脚复位 上电复位 VBATT 选择的电压上电复位 独立看门狗定时器复 位 看门狗定时器复位 电压监视器0复位 电压 监视器1复位 SRAM奇偶校验错误复位 SRA MECC错误复位 总线主控MPU错误复位 总 线从属MPU错误复位 堆栈指针错误复位 软 件复位。请参阅第6节，重置。
低电压检测(LVD)	低电压检测(LVD)监控输入到VCC引脚的电压电平，并且可以使用软件程序选择检测电平。 请参见第8节，低电压检测(LVD)。
Clocks	主时钟振荡器(MOSC) 子时钟振荡器(SOSC) 高速片 上振荡器(HOCO) 中速片上振荡器(MOCO) 低速片上 振荡器(LOCO) PLL频率合成器 IWDT专用片上振荡器 蓝牙专用时钟振荡器 蓝牙专用低速片上振荡器 时钟 输出支持。请参见第9节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在用作测量基准的时钟（测量基准时钟）生成的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据是否脉冲数在允许范围内。当测量完成或测量参考时钟在时间内产生的脉冲数不在允许范围内时，将产生中断请求。请参见第10节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到NVICDTC模块和DMAC模块。ICU还控制NMI中断。参见第14节，中断控制器单元(ICU)。
按键中断功能(KINT)	通过设置按键返回模式寄存器(KRM)并向按键中断输入引脚输入上升沿或下降沿，可以生成按键中断。请参见第21节，按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗，例如通过设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参见第11节，低功耗模式。
电池备份功能	提供电池备份功能，由电池部分供电。电池供电区域包括RTC、SOSC、LOCO、唤醒控制、备份内存、VBATT_R低电压检测以及VCC和VBATT之间的切换。在正常工作期间，电池供电区域由主电源供电，即VCC引脚。当检测到VCC电压下降时，电源切换到专用电池备用电源引脚VBATT引脚。当电压再次上升时，电源从VBATT引脚切换到VCC引脚。请参阅第12节，电池备份功能。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。请参见第13节，寄存器写保护。

Table 1.3 System (2 of 2)

Feature	Functional description
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 26, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 27, Independent Watchdog Timer (IWDT).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC).
DMA Controller (DMAC)	A 4-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC).

Table 1.3 系统(2之2)

Feature	功能说明
内存保护单元(MPU)	提供四个内存保护单元(MPU)和一个CPU堆栈指针监控功能用于内存保护。请参阅第16节，内存保护单元(MPU)。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，下溢可能会产生不可屏蔽的中断或中断。可以设置刷新允许周期来刷新计数器，作为系统失控检测的条件。请参见第26节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。它可用于复位MCU或为定时器下溢产生不可屏蔽的中断中断。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以在复位、下溢、刷新错误或寄存器中的计数值刷新时自动触发。请参见第27节，独立看门狗定时器(IWDT)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的中断请求作为事件信号，将它们连接到不同的模块，实现模块之间的直接交互，无需CPU干预。请参阅第19节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅第18节，数据传输控制器(DTC)。
DMA Controller (DMAC)	提供了一个4通道DMA控制器(DMAC)模块，用于在没有CPU的情况下传输数据。 当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。请参见第17节，DMA控制器(DMAC)。

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 4 channels and a 16-bit timer with 3 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG).
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 24, Asynchronous General Purpose Timer (AGT).
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 25, Realtime Clock (RTC).

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 and SCI1 have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 29, Serial Communications Interface (SCI).
I²C bus interface (IIC)	The 2-channel I2C bus interface (IIC) conforms with and provides a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions. See section 30, I²C Bus Interface (IIC).
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 32, Serial Peripheral Interface (SPI).
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 31, Controller Area Network (CAN) Module.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports revision 1.2 of the Battery Charging Specification. See section 28, USB 2.0 Full-Speed Module (USBFS).

Table 1.6 Timers

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个4通道的32位定时器和一个3通道的16位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参见第23节，通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	使用PortOutputEnableforGPT(POEG)功能将通用PWM定时器(GPT)输出引脚置于输出禁用状态。请参阅第22节，GPT(POEG)的端口输出启用。
异步通用 Timer (AGT)	异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参见第24节，异步通用定时器(AGT)。
实时时钟(RTC)	实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，由寄存器设置控制。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。 二进制计数模式可用于公历（西方）以外的日历。 请参见第25节，实时时钟(RTC)。

Table 1.7 通信接口（2个中的1个）

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)可配置为五个异步和同步串行接口： 异步接口（UART和异步通信接口适配器(ACIA)） 8位时钟同步接口 简单IIC（仅限主机） 简单SPI 智能卡接口。智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCI0和SCI1具有FIFO缓冲器以实现连续和全双工通信，并且可以使用片内波特率发生器独立配置数据传输速度。参见第29节，串行通信接口(SCI)。
I2C总线接口(IIC)	2通道I2C总线接口(IIC)符合并提供NXPI2C（内部集成电路）总线接口功能的子集。请参阅第30节，I2C总线接口(IIC)。
串行外设接口(SPI)	两个独立的串行外围接口(SPI)通道能够与多个处理器和外围设备进行高速、全双工同步串行通信。请参阅第32节，串行外设接口(SPI)。
控制器局域网(CAN)模块	控制器局域网(CAN)模块提供了在电磁噪声应用中使用基于消息的协议在多个从机和主机之间接收和传输数据的功能。CAN模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。请参阅第31节，控制器局域网(CAN)模块。
USB2.0全速(USBFS)模块	USB2.0全速(USBFS)模块可以作为主机控制器或设备控制器运行。该模块支持通用串行总线规范2.0中定义的全速和低速（仅适用于主机控制器）传输。该模块有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，最多可提供10个管道。可以根据用于通信的外围设备或根据用户系统为管道1到9分配任何端点编号。MCU支持电池充电规范1.2版。请参阅第28节，USB2.0 Full-Speed Module (USBFS).

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
Bluetooth low energy(BLE)	• On-chip RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification • Bit rates: 1 Mbps, 2 Mbps, 500 kbps, and 125 kbps • LE Advertising extension support • Includes an RF transceiver power supply (selectable as a DC-to-DC converter or linear regulator) • On-chip matching circuit to help reduce the number of external parts • Transmission power: +4 dBm support

Table 1.8 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 8 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 34, 14-Bit A/D Converter (ADC14).
12-bit D/A Converter (DAC12)	The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 35, 12-Bit D/A Converter (DAC12).
8-bit D/A Converter (DAC8) for ACMPLP	The 8-bit D/A Converter (DAC8) converts data and does not include an output amplifier. The DAC8 is used only as the reference voltage for ACMPLP. See section 39, 8-Bit D/A Converter (DAC8).
Temperature Sensor (TSN)	The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 36, Temperature Sensor (TSN).
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from an input to the CMPREFi(i = 0,1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting the high-speed mode decreases the response delay time, but increases current consumption. Setting the low-speed mode increases the response delay time, but decreases current consumption. See section 38, Low Power Analog Comparator (ACMPLP).
Operational Amplifier (OPAMP)	The Operational Amplifier (OPAMP) can be used to amplify small analog input voltages and output the amplified voltages. A differential operational amplifier unit with two input pins and one output pin are provided. See section 37, Operational Amplifier (OPAMP).

Table 1.9 Human machine interfaces

Feature	Functional description
Segment LCD Controller (SLCDC)	The SLCDC provides the following functions: • Waveform A or B selectable • The LCD driver voltage generator uses an external resistance division method • Automatic output of segment and common signals based on automatic display data register read • The LCD can be made to blink. See section 44, Segment LCD Controller (SLCDC).
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode. See section 40, Capacitive Touch Sensing Unit (CTSU).

Table 1.7 通信接口（2个中的2个）

Feature	功能说明
低功耗蓝牙（BLE）	符合蓝牙5.0低功耗规范的片上RF收发器和链路层 比特率：1Mbps、2Mbps、500kbps和125kbps LE广告扩展支持 包括一个RF收发器电源（可选择作为DC-to-DC转换器或线性稳压器） 片上匹配电路有助于减少外部部件的数量 传输功率：支持+4dBm

Table 1.8 Analog

Feature	功能说明
14-bit A/D Converter (ADC14)	提供了一个14位逐次逼近模数转换器。最多可选择8个模拟输入通道。可选择温度传感器输出和内部参考电压进行转换。AD转换精度可从12位和14位转换中选择，从而可以在生成数字值时优化速度和分辨率之间的折衷。请参阅第34节，14位AD转换器(ADC14)。
12-bit D/A Converter (DAC12)	12位DA转换器(DAC12)转换数据并包括一个输出放大器。请参阅第35节，12位DA转换器(DAC12)。
用于ACMPLP的8位DA转换器(DAC8)	8位DA转换器(DAC8)转换数据，不包括输出放大器。DAC8仅用作ACMPLP的参考电压。请参阅第39节，8位DA转换器(DAC8)。
温度传感器(TSN)	片上温度传感器确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压呈线性关系。输出电压被提供给ADC14进行转换，并且可以被最终应用进一步使用。请参见第36节，温度传感器(TSN)。
低功耗模拟比较器(ACMPLP)	低功耗模拟比较器(ACMPLP)比较参考输入电压和模拟输入电压。比较结果可以通过软件读取，也可以对外输出。参考电压可以从CMPREFi(i=0 1)引脚的输入、内部8位DA转换器输出或MCU内部生成的内部参考电压(Vref)中选择。可以在开始操作之前设置ACMPLP响应速度。设置高速模式会减少响应延迟时间，但会增加电流消耗。设置低速模式会增加响应延迟时间，但会降低电流消耗。请参见第38节，低功耗模拟比较器(ACMPLP)。
运算放大器(OPAMP)	运算放大器(OPAMP)可用于放大小的模拟输入电压并输出放大后的电压。提供了一种具有两个输入引脚和一个输出引脚的差分运算放大器单元。请参阅第37节，运算放大器(OPAMP)。

Table 1.9 人机界面

Feature	功能说明
段式LCD控制器(SLCDC)	SLCDC提供以下功能： 波形A或B可选 LCD驱动电压发生器使用外部电阻分压方法 根据自动显示数据寄存器读取自动输出段和公共信号 可以使LCD闪烁。请参见第44节，段式LCD控制器(SLCDC)。
电容式触控感应单元(CTSU)	电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围，因此手指不会直接接触电极。请参阅第40节，电容式触摸传感单元(CTSU)。

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 33, Cyclic Redundancy Check (CRC) Calculator.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 41, Data Operation Circuit (DOC).

Table 1.11 Security

Feature	Functional description
Secure Crypto Engine 5 (SCE5)	• Security algorithm: - Symmetric algorithm: AES • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: GHASH.

Table 1.10 数据处理

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅第33节，循环冗余校验(CRC)计算器。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。见第41节，数据运算电路（DOC）。

Table 1.11 Security

Feature	功能说明
安全加密引擎5(SCE5)	• Security algorithm: 对称算法：AES 其他支持功能： TRNG（真随机数生成器）哈希值生成：GHASH。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group may have a subset of the features.

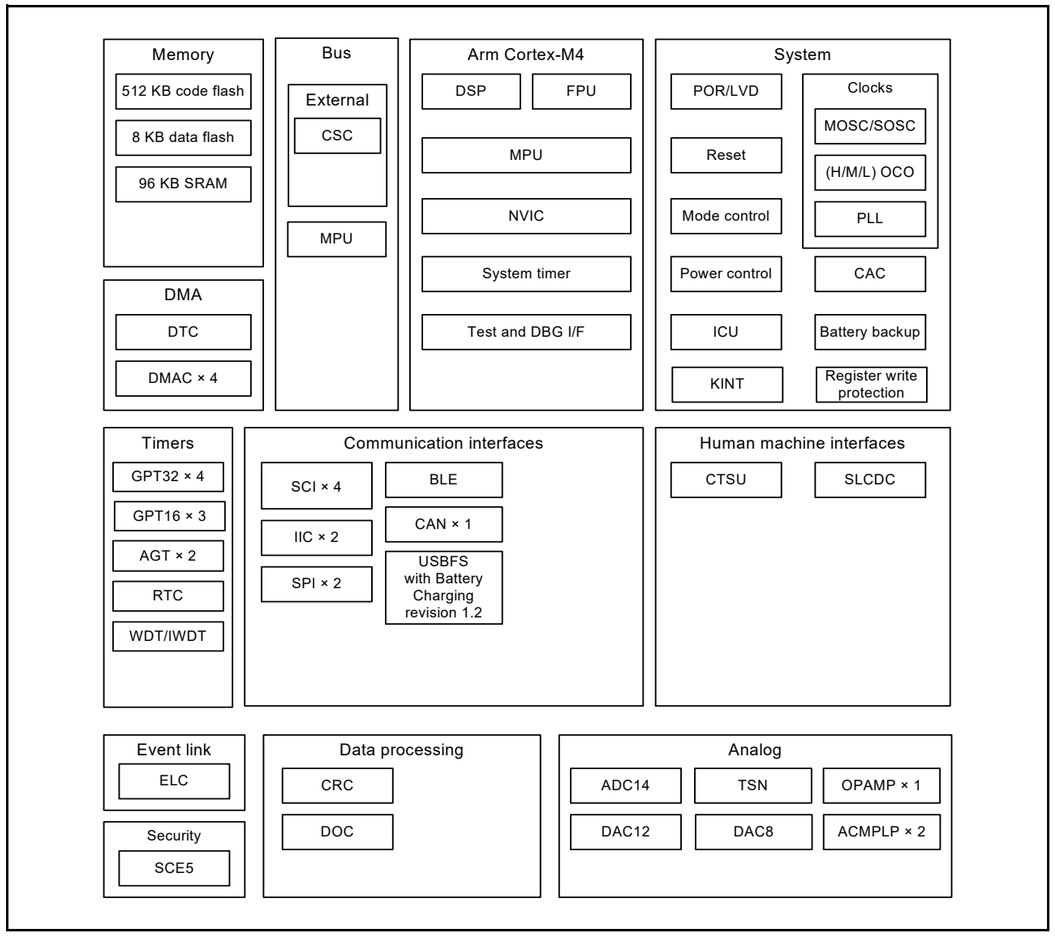


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows how to read the product part number information, including memory capacity, and package type. Table 1.13 shows a product list.

1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备可能具有功能的子集。

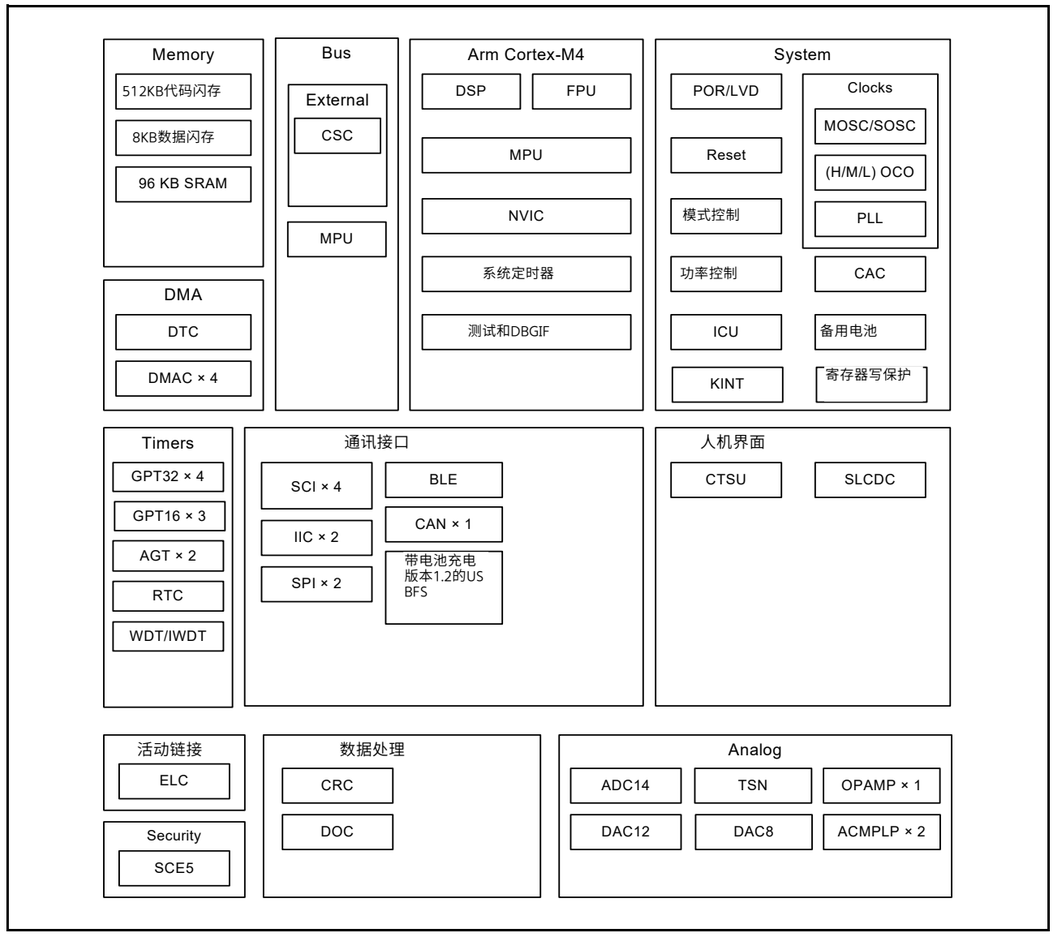


Figure 1.1 框图

1.3 零件编号

图1.2显示了如何读取产品型号信息，包括内存容量和封装类型。表1.13显示了一个产品列表。

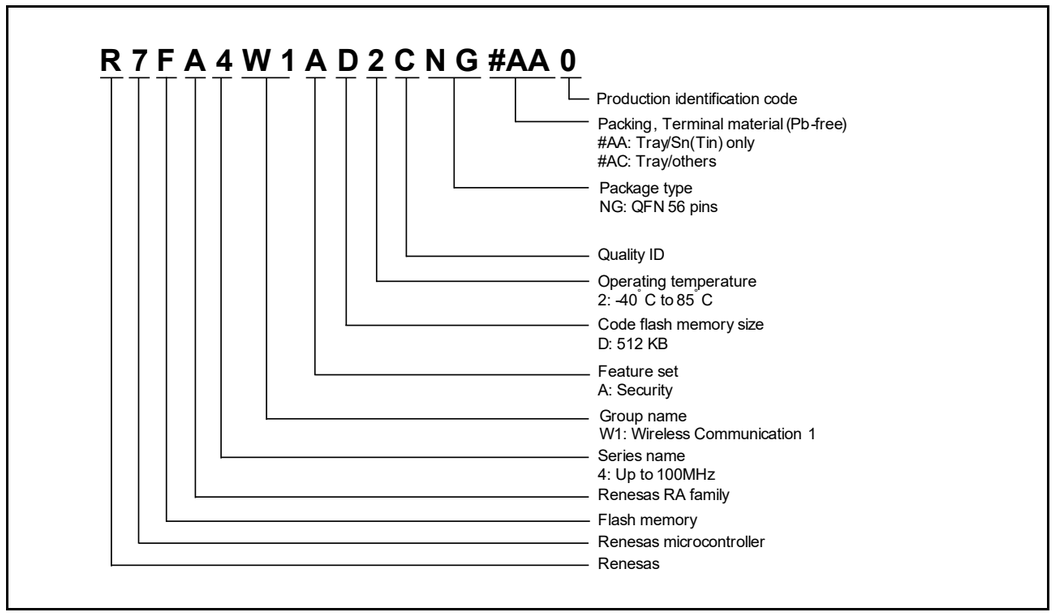


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Code flash	Data flash	SRAM	Operating temperature
R7FA4W1AD2CNG	R7FA4W1AD2CNG#AA0	512 KB	8 KB	96 KB	-40 to +85°C

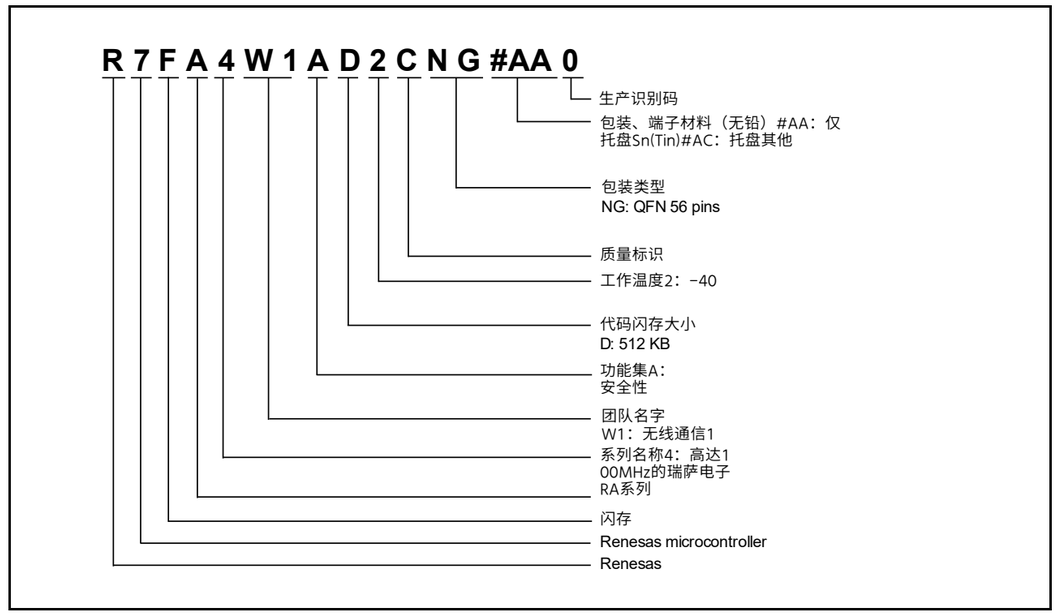


Figure 1.2 零件编号方案

Table 1.12 产品列表

产品部件号	可订购部件号	代码闪存	数据闪存	SRAM	工作温度
R7FA4W1AD2CNG	R7FA4W1AD2CNG#AA0	512 KB	8 KB	96 KB	-40 to +85°C

1.4 Function Comparison

Table 1.13 Function comparison

Part numbers		R7FA4W1AD2CNG
Pin count		56
Package		QFN
Code flash memory		512 KB
Data flash memory		8 KB
SRAM		96 KB
	Parity	80 KB
	ECC	16 KB
System	CPU clock	48 MHz
	Backup registers	512 bytes
	ICU	Yes
	KINT	8
Event control	ELC	Yes
DMA	DTC	Yes
	DMAC	4
Timers	GPT32	4
	GPT16	3
	AGT	2
	RTC	Yes
	WDT/IWDT	Yes
Communication	SCI	6
	IIC	2
	SPI	2
	CAN	1
	USBFS	Yes
	BLE	An RF transceiver and link layer compliant with Bluetooth 5.0 low energy specification
Analog	ADC14	8
	DAC12	1
	DAC8	2
	ACMPLP	2
	OPAMP	1
	TSN	Yes
HMI	SLCDC	4 com × 9 seg
	CTSU	11
Data processing	CRC	Yes
	DOC	Yes
Security		SCE5

1.4 功能比较

Table 1.13 功能对比

零件号		R7FA4W1AD2CNG
针数		56
Package		QFN
代码闪存		512 KB
数据闪存		8 KB
SRAM		96 KB
	Parity	80 KB
	ECC	16 KB
System	中央处理器时钟	48 MHz
	备份寄存器	512 bytes
	ICU	Yes
	KINT	8
事件控制	ELC	Yes
DMA	DTC	Yes
	DMAC	4
Timers	GPT32	4
	GPT16	3
	AGT	2
	RTC	Yes
	WDT/IWDT	Yes
Communication	SCI	6
	IIC	2
	SPI	2
	CAN	1
	USBFS	Yes
	BLE	符合蓝牙5.0低功耗规范的射频收发器和链路层
Analog	ADC14	8
	DAC12	1
	DAC8	2
	ACMPLP	2
	OPAMP	1
	TSN	Yes
HMI	SLCDC	4com×9seg
	CTSU	11
数据处理	CRC	Yes
	DOC	Yes
Security		SCE5

1.5 Pin Functions

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT_RF	Output	Bluetooth-dedicated clock output pin for output of a 1-, 2-, or 4-MHz signal
	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. Connect a 32-MHz oscillator to these pins.
	XTAL2_RF	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11, IRQ14, IRQ15	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip debug	TMS	I/O	On-chip emulator pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	SWDIO	I/O	Serial Wire debug Data Input/Output pin
	SWCLK	Input	Serial Wire Clock pin
	SWO	Output	Serial Wire trace Output pin
Battery backup	VBATWIO0	I/O	Output wakeup signal for the VBATT wakeup control function. External event input for the VBATT wakeup control function.
GPT	GTETRGA, GTETRGB	Input	External trigger input pin
	GTIO0A to GTIOA5A,GTIO8A, GTIO0B to GTIOA5B,GTIO8B	I/O	Input capture, Output capture, or PWM output pin
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable
	AGTIO0, AGTIO1	I/O	External event input and pulse output
	AGTO0, AGTO1	Output	Pulse output
	AGTOB0	Output	Output compare match B output

1.5 引脚功能

Function	Signal	I/O	Description
电源	VCC	Input	电源引脚。将其连接到系统电源。通过一个0.1μF电容将此引脚连接到VSS。电容应靠近引脚放置。
	VCL	Input	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。
	VSS	Input	接地引脚。将其连接到系统电源(0V)。
	VBATT	Input	备用电源引脚
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。
	EXTAL	Input	
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	CLKOUT_RF	Output	蓝牙专用时钟输出引脚，用于输出1、2或4MHz信号
	XTAL1_RF	Input	用于连接蓝牙专用时钟振荡器的引脚。连接32 MHz振荡器连接到这些引脚。
	XTAL2_RF	Output	
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放时的操作模式转换期间，这些引脚上的信号电平不得更改。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11, IRQ14, IRQ15	Input	可屏蔽中断请求引脚
KINT	KR00 to KR07	Input	通过向按键中断输入引脚输入下降沿可以产生按键中断
On-chip debug	TMS	I/O	片上仿真器引脚
	TDI	Input	
	TCK	Input	
	TDO	Output	
	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
	SWO	Output	串行线迹线输出引脚
备用电池	VBATWIO0	I/O	VBATT唤醒控制功能的输出唤醒信号。 VBATT唤醒控制功能的外部事件输入。
GPT	GTETRGA, GTETRGB	Input	外部触发输入引脚
	GTIO0A to GTIOA5A,GTIO8A, GTIO0B to GTIOA5B,GTIO8B	I/O	输入捕捉、输出捕捉或PWM输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEE0, AGTEE1	Input	外部事件输入使能
	AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出
	AGTO0, AGTO1	Output	脉冲输出
	AGTOB0	Output	输出比较匹配B输出

Function	Signal	I/O	Description
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0, RTCIC2	Input	Time capture event input pins
SCI	SCK0,SCK1,SCK4, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD4, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD4, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS4_RTS4, CTS9_RTS9	I/O	Input/Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL4, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA4, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK4, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO4, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI4, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
	SS0, SS1,SS4,SS9	Input	Slave-select input pins (simple SPI), active-low
IIC	SCL0 to SCL1	I/O	Input/output pins for clock
	SDA0 to SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1, SSLA2, SSLA3, SSLB1, SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB transceiver. Apply the same voltage as VCC_USB.
	VCC_USB	I/O	Input: Power supply pin for USB transceiver.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	External overcurrent detection signals should be connected to these pins.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
ADC14	AN004 to AN006, AN009, AN010, AN017, AN019, AN020	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
DAC12	DA0	Output	Output pins for the analog signals to be processed by the D/A converter

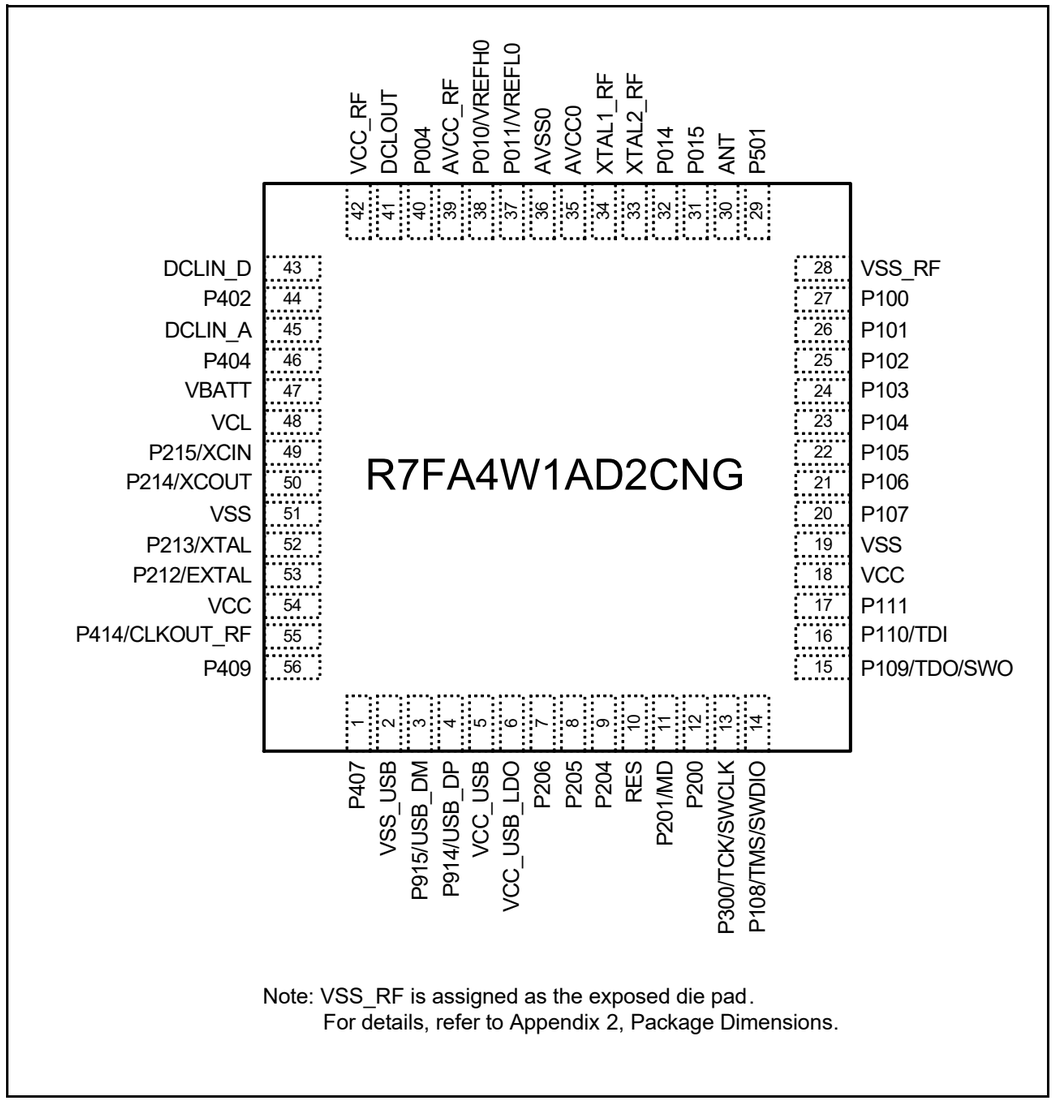
Function	Signal	I/O	Description
RTC	RTCOUT	Output	1Hz64Hz时钟的输出引脚
	RTCIC0, RTCIC2	Input	时间捕捉事件输入引脚
SCI	SCK0,SCK1,SCK4, SCK9	I/O	时钟输入输出引脚（时钟同步模式）
	RXD0, RXD1, RXD4, RXD9	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXD0, TXD1, TXD4, TXD9	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTS0_RTS0, CTS1_RTS1, CTS4_RTS4, CTS9_RTS9	I/O	Input用于控制发送和接收开始的输出引脚（异步模式时钟同步模式），低电平有效
	SCL0, SCL1, SCL4, SCL9	I/O	IIC时钟的输入输出引脚（简单IIC）
	SDA0, SDA1, SDA4, SDA9	I/O	IIC数据的输入输出引脚（简单IIC）
	SCK0, SCK1, SCK4, SCK9	I/O	时钟的输入输出引脚（简单SPI）
	MISO0, MISO1, MISO4, MISO9	I/O	用于从机传输数据的输入输出引脚（简单SPI）
	MOSI0, MOSI1, MOSI4, MOSI9	I/O	用于数据主传输的输入输出引脚（简单SPI）
	SS0, SS1,SS4,SS9	Input	从机选择输入引脚（简单SPI），低电平有效
IIC	SCL0 to SCL1	I/O	时钟输入输出引脚
	SDA0 to SDA1	I/O	数据输入输出引脚
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	输入或输出从主机输出的数据
	MISOA, MISOB	I/O	从机输入或输出数据输出
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1, SSLA2, SSLA3, SSLB1, SSLB3	Output	从机选择的输出引脚
CAN	CRX0	Input	接收数据
	CTX0	Output	传输数据
USBFS	VSS_USB	Input	接地引脚
	VCC_USB_LDO	Input	USB收发器的电源引脚。施加与VCC_USB相同的电压。
	VCC_USB	I/O	输入：USB收发器的电源引脚。
	USB_DP	I/O	USB片上收发器的D+IO引脚。该引脚应连接到USB总线的D+引脚。
	USB_DM	I/O	D USB片上收发器的IO引脚。该引脚应连接到USB总线的D 引脚。
	USB_VBUS	Input	USB电缆连接监视器引脚。该引脚应连接到USB总线的VBUS。当USB模块作为设备控制器运行时，可以检测到VBUS引脚状态（连接或断开）。
	USB_VBUSEN	Output	VBUS(5V)为外部供电芯片供电使能信号
	USB_OVRCURA, USB_OVRCURB	Input	外部过流检测信号应连接到这些引脚。
模拟电源	AVCC0	Input	模拟模块电源引脚
	AVSS0	Input	模拟模块电源接地引脚
	VREFH0	Input	参考电源引脚
	VREFL0	Input	参考电源接地引脚
ADC14	AN004 to AN006, AN009, AN010, AN017, AN019, AN020	Input	AD转换器要处理的模拟信号的输入引脚
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚，低电平有效
DAC12	DA0	Output	由数模转换器处理的模拟信号的输出引脚

Function	Signal	I/O	Description
Comparator output	VCOUT	Output	Comparator output pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP2+	Input	Analog voltage input pins
	AMP2-	Input	Analog voltage input pins
	AMP2O	Output	Analog voltage output pins
CTSU	TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34	Input	Capacitive touch detection pins (touch pins)
	TSCAP	—	Secondary power supply pin for the touch driver
I/O ports	P004, P010, P011, P014, P015	I/O	General-purpose input/output pins
	P100 to P111	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300	I/O	General-purpose input/output pins
	P402, P404, P407, P409, P414	I/O	General-purpose input/output pins
	P501	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins
SLCDC	VL1, VL2, VL4	I/O	Voltage pin for driving the LCD
	COM0 to COM3	Output	Common signal output pins for the LCD controller/driver
	SEG6, SEG9, SEG11, SEG12, SEG20, SEG23, SEG49, SEG52, SEG53	Output	Segment signal output pins for the LCD controller/driver
BLE (Bluetooth Low Energy)	ANT	I/O	RF single I/O pin for the RF transceiver Set the impedance of the signal line to 50 Ω.
	DCLOUT	Output	RF transceiver power-supply output pin
	DCLIN_A	Input	RF transceiver power-supply output connection pin
	DCLIN_D	Input	RF transceiver power-supply output connection pin
	VCC_RF	Input	RF transceiver power supply pin
	AVCC_RF	Input	RF transceiver power supply pin
	VSS_RF	Input	RF transceiver ground pin

Function	Signal	I/O	Description
比较器输出	VCOUT	Output	比较器输出引脚
ACMPLP	CMPREF0, CMPREF1	Input	参考电压输入引脚
	CMPIN0, CMPIN1	Input	模拟电压输入引脚
OPAMP	AMP2+	Input	模拟电压输入引脚
	AMP2-	Input	模拟电压输入引脚
	AMP2O	Output	模拟电压输出引脚
CTSU	TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34	Input	电容式触摸检测引脚（触摸引脚）
	TSCAP	—	触摸驱动器的辅助电源引脚
I/O ports	P004, P010, P011, P014, P015	I/O	General-purpose input/output pins
	P100 to P111	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	通用输入引脚
	P300	I/O	General-purpose input/output pins
	P402, P404, P407, P409, P414	I/O	General-purpose input/output pins
	P501	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins
SLCDC	VL1, VL2, VL4	I/O	用于驱动LCD的电压引脚
	COM0 to COM3	Output	LCD控制器驱动器的公共信号输出引脚
	SEG6, SEG9, SEG11, SEG12, SEG20, SEG23, SEG49, SEG52, SEG53	Output	LCD控制器驱动器的段信号输出引脚
BLE（蓝牙低 Energy)	ANT	I/O	RF收发器的RF单IO引脚 将信号线的阻抗设置为50Ω。
	DCLOUT	Output	RF收发器电源输出引脚
	DCLIN_A	Input	RF收发器电源输出连接引脚
	DCLIN_D	Input	RF收发器电源输出连接引脚
	VCC_RF	Input	RF收发器电源引脚
	AVCC_RF	Input	RF收发器电源引脚
	VSS_RF	Input	射频收发器接地引脚

1.6 Pin Assignments

Figure 1.3 shows the pin assignments.

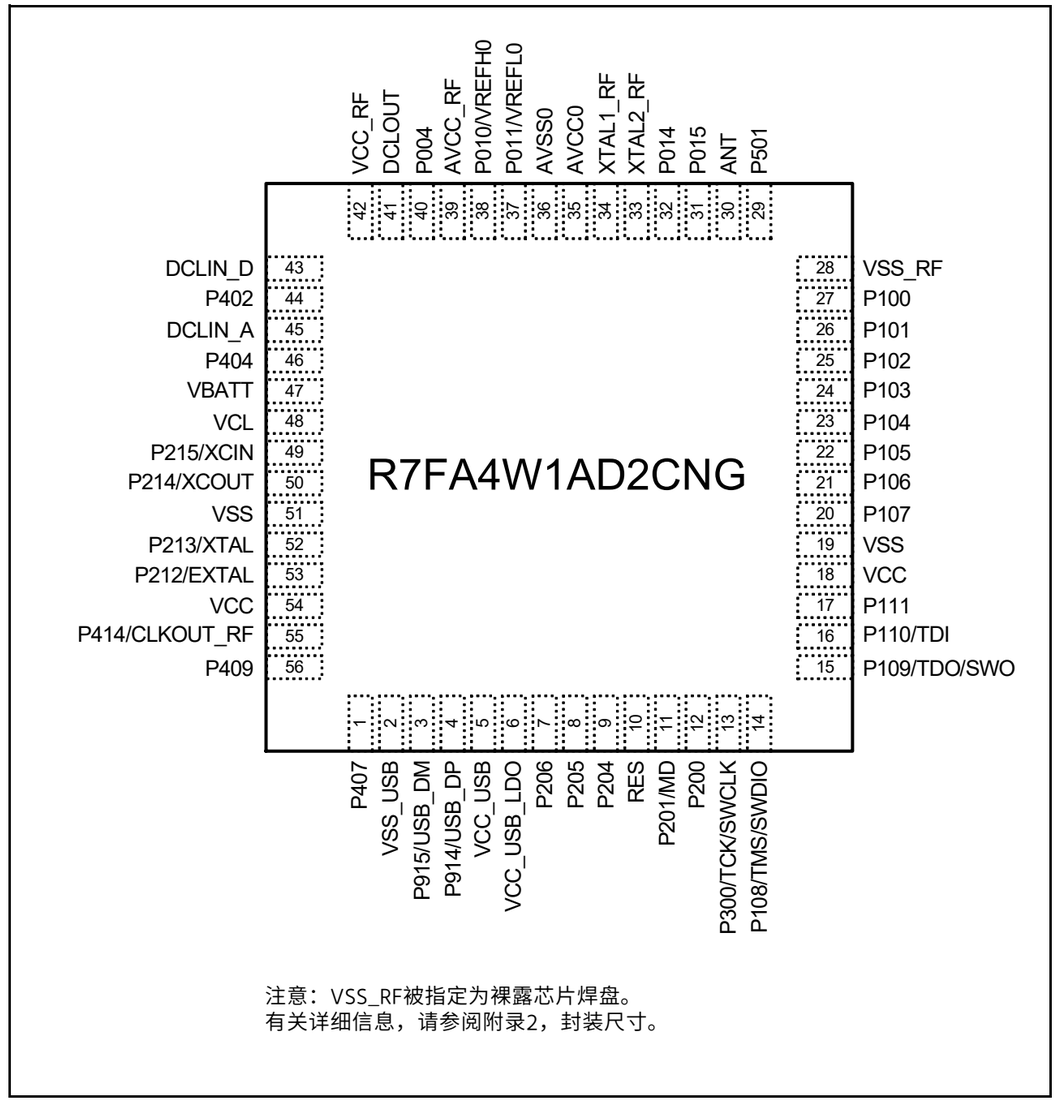


Note: VSS_RF is assigned as the exposed die pad.
For details, refer to Appendix 2, Package Dimensions.

Figure 1.3 Pin assignment for QFN 56-pin (top view)

1.6 引脚分配

图1.3显示了引脚分配。



注意：VSS_RF被指定为裸露芯片焊盘。
有关详细信息，请参阅附录2，封装尺寸。

Figure 1.3 QFN56引脚的引脚分配（顶视图）

1.7 Pin Lists

Pin number				Timers					Communication interfaces						Analogs			HMI	
QFN56	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC		USBFS, CAN	SCI	IIC	SPI	RF		ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
1			P407	AGTIO0			RTCOUT		USB_VBUS	CTS4_RTS4/SS4	SDA0	SSLB3			ADTRG0			SEG11	TS3
2	VSS_USB																		
3			P915						USB_DM										
4			P914						USB_DP										
5	VCC_USB																		
6	VCC_USB_LDO																		
7		IRQ0	P206		GTIU				USB_VBUSEN	RXD4/MISO4/SCL4	SDA1	SSLB1						SEG12	TS1
8	CLKOUT	IRQ1	P205	AGTO1	GTIV	GTIOC4A			USB_OVRCURA	TXD4/MOSI4/SDA4/CTS9_RTS9/SS9	SCL1	SSLB0						SEG20	TSCAP
9	CACREF		P204	AGTO1	GTIW	GTIOC4B			USB_OVRCURB	SCK4/SCK9	SCL0	RSPCKB						SEG23	TS0
10	RES																		
11	MD		P201																
12		NMI	P200																
13	TCK/SWCLK		P300		GTOUUP	GTIOC0A						SSLB1							
14	TMS/SWDIO		P108		GTOULO	GTIOC0B				CTS9_RTS9/SS9		SSLB0							
15	TDO/SWO/CLKOUT		P109		GTOVUP	GTIOC1A			CTX0	SCK1/TXD9/MOSI9/SDA9		MOSIB						SEG52	TS10
16	TDI	IRQ3	P110		GTOVLO	GTIOC1B			CRX0	RXD9/MISO9/SCL9		MISOB					VCOUT	SEG53	
17		IRQ4	P111			GTIOC3A				SCK9		RSPCKB							TS12
18	VCC																		
19	VSS																		
20		KR07	P107			GTIOC8A												COM3	
21		KR06	P106			GTIOC8B						SSLA3						COM2	
22		KR05/IRQ0	P105		GTETRGA	GTIOC1A						SSLA2						COM1	TS34
23		KR04/IRQ1	P104		GTETRGB	GTIOC1B				RXD0/MISO0/SCL0		SSLA1						COM0	TS13
24		KR03	P103		GTOWUP	GTIOC2A			CTX0	CTS0_RTS0/SS0		SSLA0			AN019		CMPREF1	VL4	
25		KR02	P102	AGTO0	GTOWLO	GTIOC2B			CRX0	SCK0		RSPCKA			AN020/ADTRG0		CMPIN1		
26		KR01/IRQ1	P101	AGTEE0	GTETRGB	GTIOC5A				TXD0/MOSI0/SDA0/CTS1_RTS1/SS1	SDA1	MOSIA					CMPREF0	VL2	

1.7 引脚列表

针号				Timers					通讯接口						Analogs			HMI	
QFN56	电源、系统、时钟、调试、CAC、VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC		USBFS, CAN	SCI	IIC	SPI	RF		ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
1			P407	AGTIO0			RTCOUT		USB_VBUS	CTS4_RTS4/SS4	SDA0	SSLB3			ADTRG0			SEG11	TS3
2	VSS_USB																		
3			P915						USB_DM										
4			P914						USB_DP										
5	VCC_USB																		
6	VCC_USB_LDO																		
7		IRQ0	P206		GTIU				USB_VBUSEN	RXD4/MISO4/SCL4	SDA1	SSLB1						SEG12	TS1
8	CLKOUT	IRQ1	P205	AGTO1	GTIV	GTIOC4A			USB_OVRCURA	TXD4/MOSI4/SDA4/CTS9_RTS9/SS9	SCL1	SSLB0						SEG20	TSCAP
9	CACREF		P204	AGTO1	GTIW	GTIOC4B			USB_OVRCURB	SCK4/SCK9	SCL0	RSPCKB						SEG23	TS0
10	RES																		
11	MD		P201																
12		NMI	P200																
13	TCK/SWCLK		P300		GTOUUP	GTIOC0A						SSLB1							
14	TMS/SWDIO		P108		GTOULO	GTIOC0B				CTS9_RTS9/SS9		SSLB0							
15	TDO/SWO/CLKOUT		P109		GTOVUP	GTIOC1A			CTX0	SCK1/TXD9/MOSI9/SDA9		MOSIB						SEG52	TS10
16	TDI	IRQ3	P110		GTOVLO	GTIOC1B			CRX0	RXD9/MISO9/SCL9		MISOB					VCOUT	SEG53	
17		IRQ4	P111			GTIOC3A				SCK9		RSPCKB							TS12
18	VCC																		
19	VSS																		
20		KR07	P107			GTIOC8A												COM3	
21		KR06	P106			GTIOC8B						SSLA3						COM2	
22		KR05/IRQ0	P105		GTETRGA	GTIOC1A						SSLA2						COM1	TS34
23		KR04/IRQ1	P104		GTETRGB	GTIOC1B				RXD0/MISO0/SCL0		SSLA1						COM0	TS13
24		KR03	P103		GTOWUP	GTIOC2A			CTX0	CTS0_RTS0/SS0		SSLA0			AN019		CMPREF1	VL4	
25		KR02	P102	AGTO0	GTOWLO	GTIOC2B			CRX0	SCK0		RSPCKA			AN020/ADTRG0		CMPIN1		
26		KR01/IRQ1	P101	AGTEE0	GTETRGB	GTIOC5A				TXD0/MOSI0/SDA0/CTS1_RTS1/SS1	SDA1	MOSIA					CMPREF0	VL2	

Pin number				Timers				Communication interfaces					Analogs			HMI	
QFN56	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	RF	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
27		KR00/ IRQ2	P100	AGTIO0	GTETRGA	GTIOC5B			RXD0/ MISO0/ SCL0/ SCK1	SCL1	MISOA				CMPIN0	VL1	
28												VSS_RF					
29		IRQ11	P501	AGTOB0	GTIV	GTIOC2B		USB_OVRC URA					AN017		CMPIN1	SEG49	
30												ANT					
31		IRQ7	P015										AN010				TS28
32			P014										AN009	DA0			
33												XTAL2_RF					
34												XTAL1_RF					
35	AVCC0																
36	AVSS0																
37	VREFL0	IRQ15	P011										AN006	AMP2+			TS31
38	VREFH0	IRQ14	P010										AN005	AMP2-			TS30
39												AVCC_RF					
40		IRQ3	P004										AN004	AMP2O			
41												DCLOUT					
42												VCC_RF					
43												DCLIN_D					
44	VBATWIO 0	IRQ4	P402	AGTIO0/ AGTIO1			RTCIC0	CRX0	RXD1/ MISO1/SCL1							SEG6	TS18
45												DCLIN_A					
46			P404			GTIOC3B	RTCIC2										
47	VBATT																
48	VCL																

针号		Timers						通讯接口					Analogs			HMI	
QFN56	电源，系统，时钟，调试，CAC，VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	RF	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
27		KR00/ IRQ2	P100	AGTIO0	GTETRGA	GTIOC5B			RXD0/ MISO0/ SCL0/ SCK1	SCL1	MISOA				CMPIN0	VL1	
28												VSS_RF					
29		IRQ11	P501	AGTOB0	GTIV	GTIOC2B		USB_OVRC URA					AN017		CMPIN1	SEG49	
30												ANT					
31		IRQ7	P015										AN010				TS28
32			P014										AN009	DA0			
33												XTAL2_RF					
34												XTAL1_RF					
35	AVCC0																
36	AVSS0																
37	VREFL0	IRQ15	P011										AN006	AMP2+			TS31
38	VREFH0	IRQ14	P010										AN005	AMP2-			TS30
39												AVCC_RF					
40		IRQ3	P004										AN004	AMP2O			
41												DCLOUT					
42												VCC_RF					
43												DCLIN_D					
44	VBATWIO 0	IRQ4	P402	AGTIO0/ AGTIO1			RTCIC0	CRX0	RXD1/ MISO1/SCL1							SEG6	TS18
45												DCLIN_A					
46			P404			GTIOC3B	RTCIC2										
47	VBATT																
48	VCL																

Pin number				Timers				Communication interfaces					Analogs			HMI	
QFN56	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	RF	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
49	XCIN		P215														
50	XCOUT		P214														
51	VSS																
52	XTAL	IRQ2	P213		GTETRGA	GTIOC0A			TXD1/ MOSI1/ SDA1								
53	EXTAL	IRQ3	P212	AGTEE1	GTETRGB	GTIOC0B			RXD1/ MISO1/SCL1								
54	VCC																
55		IRQ9	P414			GTIOC0B					SSLA1	CLKOUT_ RF					
56		IRQ6	P409		GTOWUP	GTIOC5A		USB_EXICE N								SEG9	

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针号				Timers				通讯接口					Analogs			HMI	
QFN56	电源，系统，时钟，调试，CAC，VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	RF	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
49	XCIN		P215														
50	XCOUT		P214														
51	VSS																
52	XTAL	IRQ2	P213		GTETRGA	GTIOC0A			TXD1/ MOSI1/ SDA1								
53	EXTAL	IRQ3	P212	AGTEE1	GTETRGB	GTIOC0B			RXD1/ MISO1/SCL1								
54	VCC																
55		IRQ9	P414			GTIOC0B					SSLA1	CLKOUT_ RF					
56		IRQ6	P409		GTOWUP	GTIOC5A		USB_EXICE N								SEG9	

2. CPU

The MCU is based on the Arm® Cortex®-M4 core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M4
  - Revision: r0p1-01rel0
  - Armv7E-M architecture profile
  - Single Precision Floating-Point Unit compliant with the ANSI/IEEE Std 754-2008.
- Memory Protection Unit (MPU)
  - Armv7 Protected Memory System Architecture
  - 8 protected regions.
- SysTick timer
  - Driven by SYSTICCLK (LOCO) or ICLK.

See reference 1. and reference 2. for details.

2.1.2 Debug

- Arm CoreSight™ ETM™-M4
  - Revision: r0p1-00rel0
  - Arm ETM Architecture version 3.5.
- CoreSight Instrumentation Trace Macrocell (ITM)
- Data Watchpoint and Trace Unit (DWT)
  - 4 comparators for watchpoints and triggers.
- Flash Patch and Breakpoint Unit (FPB)
  - Flash Patch (remap) function is unavailable, only breakpoint function is available
  - 6 instruction comparators
  - 2 literal comparators.
- CoreSight Time Stamp Generator (TSG)
  - Time stamp for ETM and ITM
  - Driven by CPU clock.
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control.
- CoreSight Debug Access Port (DAP)
  - JTAG Debug Port (JTAG-DP)
  - Serial Wire Debug Port (SW-DP).
- Cortex-M4 Trace Port Interface Unit (TPIU)
  - Serial Wire Output (SWO).
- CoreSight Embedded Trace Buffer (ETB)

2. CPU

MCU基于Arm®Cortex®-M4内核。

2.1 Overview

2.1.1 CPU

- Arm Cortex-M4
  - Revision: r0p1-01rel0
  - Armv7E-M架构简介
  - 符合ANSIIEEEStd754-2008的单精度浮点单元。
- 内存保护单元(MPU)
  - Armv7受保护的内存系统架构
  - 8个保护区。
- SysTick timer
  - 由SYSTICCLK(LOCO)或ICLK驱动。

有关详细信息，请参阅参考1.和参考2。

2.1.2 Debug

- Arm CoreSight™ ETM™-M4
  - Revision: r0p1-00rel0
  - ArmETM架构版本3.5。
- CoreSight仪表跟踪宏单元(ITM)
- 数据观察点和跟踪单元(DWT)
  - 4个用于观察点和触发器的比较器。
- 闪存补丁和断点单元(FPB)
  - FlashPatch（remap）功能不可用，只有断点功能可用
  - 6 instruction comparators
  - 2 literal comparators.
- CoreSight时间戳生成器(TSG)
  - ETM和ITM的时间戳
  - 由CPU时钟驱动。
- 调试寄存器模块(DBGREG)
  - 重置控制
  - 停止控制。
- CoreSight调试访问端口(DAP)
  - JTAG调试端口(JTAG-DP)
  - 串行线调试端口(SW-DP)。
- Cortex-M4跟踪端口接口单元(TPIU)
  - 串行线输出(SWO)。
- CoreSight嵌入式跟踪缓冲区(ETB)

- CoreSight Trace Memory Controller with ETB configuration
- Buffer size: 1 KB.

See reference 1. and 2. for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 48 MHz
- Serial Write Output (SWO) trace interface: maximum 12.5 MHz
- Joint Test Action Group (JTAG) interface: maximum 12.5 MHz
- Serial Wire Debug (SWD) interface: maximum 12.5 MHz.

Figure 2.1 shows a block diagram of the Cortex-M4 CPU.

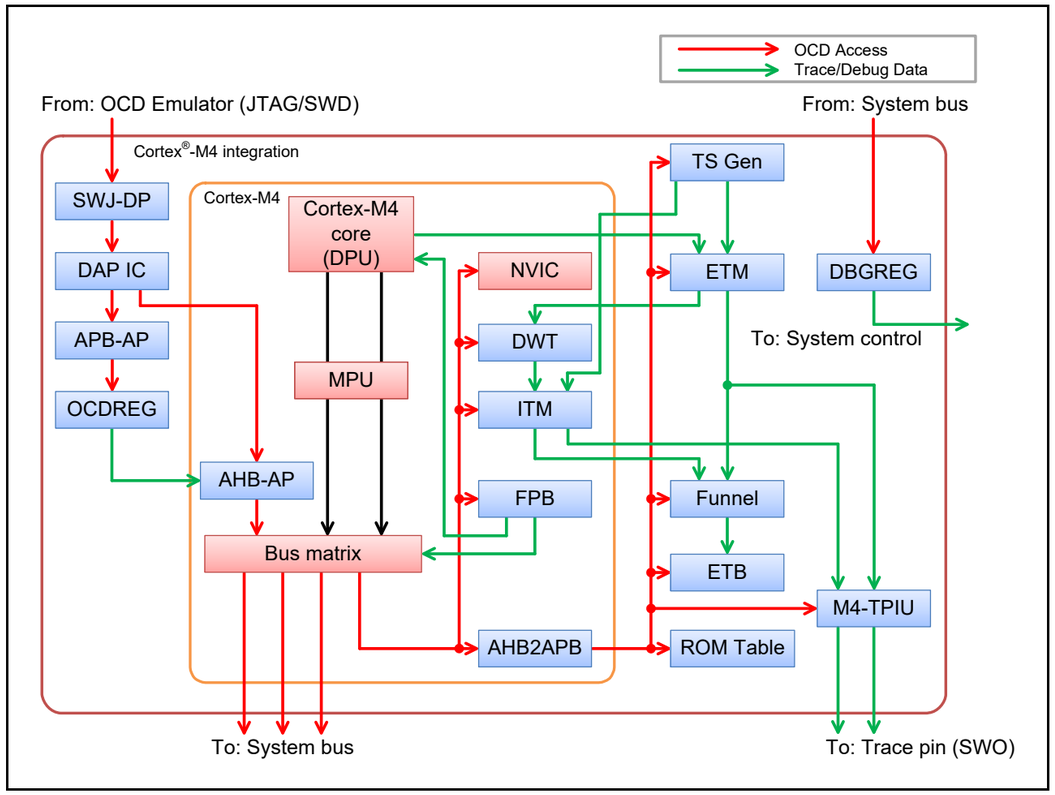


Figure 2.1 Cortex-M4 CPU block diagram

- 具有ETB配置的CoreSight跟踪内存控制器
- Buffer size: 1 KB.

有关详细信息，请参阅参考1.和2.。

2.1.3 工作频率

MCU的工作频率如下：

- CPU: maximum 48 MHz
- 串行写输出(SWO)跟踪接口：最大12.5MHz
- 联合测试行动组(JTAG)接口：最大12.5MHz
- 串行线调试(SWD)接口：最大12.5MHz。

图2.1显示了Cortex-M4CPU的框图。

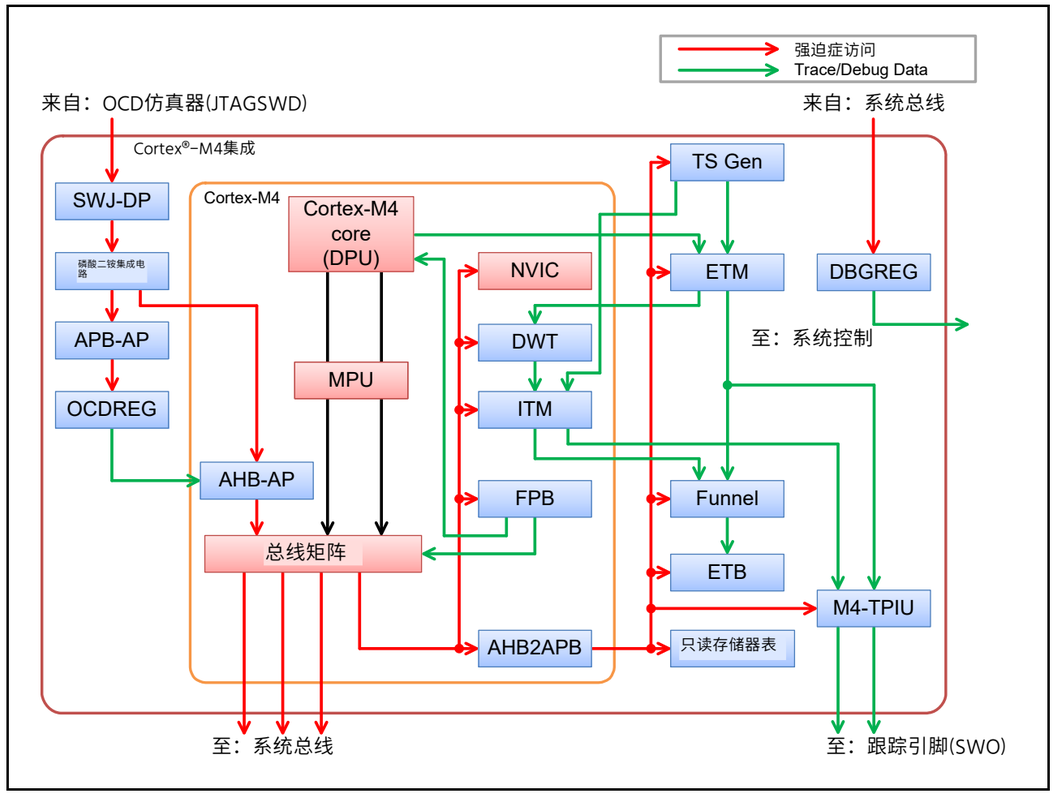


Figure 2.1 Cortex-M4CPU框图

2.2 MCU Implementation Options

Table 2.1 shows the implementation options of the MCU and is based on the configurable options in reference 2.

Table 2.1 Implementation options

Option	Description
MPU	Included, 8 protect regions
FPB	Flash Patch (remap) function is unavailable, only breakpoint function is available.
DWT	Included
ITM	Included
ETM	Included
AHB-AP	Included
HTM interface	Not included
TPIU	Included Only Serial Wire Output
WIC*1	Not included
Debug Port	SWJ-DP
FPU	Included
Number of interrupts	32
Number of priority bits	4 bits (16 levels)
Endianness	Little-endian
Time Stamp Generator	Included
ETB	Included
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 11, Low Power Modes. Note: SCB.SCR.SLEEPDEEP is ignored.
Memory features	Cacheable attribute is utilized in the MCU. See section 15, Buses for the detail.
SysTick Timer	Included SYST_CALIB = 4000 0147h Bit [31] = 0 Reference clock provided Bit [30] = 1 TERMS value is inexact Bits [29:24] = 00h Reserved Bits [23:0] = 000147h TERM: (32768 × 10 ms) - 1 / 32.768 kHz = 326.66 decimal = 327 with skew = 000147h
Event input/output	Not implemented
System reset request output	The SYSRESETREQ bit in Application Interrupt and Reset Control Register causes a CPU reset
Auxiliary fault inputs (AUXFAULT)	Not implemented

Note 1. The ICU can wake up the CPU instead of the Wakeup Interrupt Controller (WIC). For more details, see section 14, Interrupt Controller Unit (ICU).

2.3 Trace Interface

A Serial Wire Output (SWO) provides trace output. Table 2.2 shows the MCU pin for the trace function. This pin is multiplexed with other functions.

Table 2.2 Trace function pin

Name	I/O	Width	Function	When not in use
TDO/SWO	Output	1 bit	Serial wire output Multiplexed with JTAG TDO pin	Open

2.2 MCU实施选项

表2.1显示了MCU的实现选项，基于参考2中的可配置选项。

Table 2.1 实施选项

Option	Description
MPU	包括，8个保护区
FPB	FlashPatch（remap）功能不可用，只有断点功能可用。
DWT	Included
ITM	Included
ETM	Included
AHB-AP	Included
HTM interface	不包含
TPIU	Included 仅串行线输出
WIC*1	不包含
调试端口	SWJ-DP
FPU	Included
中断数	32
优先级位数	4 bits (16 levels)
Endianness	Little-endian
时间戳生成器	Included
ETB	Included
睡眠模式省电	支持睡眠模式和其他低功耗模式。有关详细信息，请参阅第11节，低电源模式。 Note: SCB.SCR.SLEEPDEEP被忽略。
记忆功能	可缓存属性在MCU中使用。 有关详细信息，请参阅第15节，总线。
SysTick Timer	Included SYST_CALIB = 4000 0147h Bit [31] = 0 提供参考时钟 Bit [30] = 1 TERMS值不准确 Bits [29:24] = 00h Reserved Bits [23:0] = 000147h TERM：(32768×10ms)132.768kHz=326.66十进制=327withskew=000147h
Event input/output	未实现
系统复位请求输出	应用程序中断和复位控制寄存器中的SYSRESETREQ位导致CPU复位
辅助故障输入(AUXFAULT)	未实现

Note 1. ICU可以唤醒CPU而不是唤醒中断控制器(WIC)。有关详细信息，请参阅第14节，中断控制器单元（ICU）。

2.3 跟踪接口

串行线输出(SWO)提供跟踪输出。表2.2显示了用于跟踪功能的MCU引脚。该引脚与其他功能复用。

Table 2.2 跟踪功能引脚

Name	I/O	Width	Function	不使用时
TDO/SWO	Output	1 bit	串行线输出 与JTAGTDO引脚复用	Open

2.4 JTAG/SWD Interface

Table 2.3 shows the JTAG/SWD pins.

Table 2.3 JTAG/SWD pins

Name	I/O	P/N	Width	Function	When not in use
TCK/SWCLK	Input	Pos.	1 bit	JTAG clock pin SWD clock pin	Pull-up
TMS/SWDIO	I/O	Neg.	1 bit	JTAG TMS pin SWD I/O pin	Pull-up
TDI	Input	Pos.	1 bit	JTAG TDI pin	Pull-up
TDO/SWO	Output	Neg.	1 bit	JTAG TDO pin Multiplexed with serial wire output	Open

2.5 Debug Mode

2.5.1 Debug Mode Definition

In single chip mode, the debugger state of the connection is defined as OCD mode, and the debugger state of the disconnection is defined as User mode. Table 2.4 shows the CPU debug modes and usage conditions.

Table 2.4 CPU debug mode and conditions

Conditions		Mode	
OCD connect	**JTAG/SWD authentication**	**Debug mode**	**Debug authentication**
Not connected	-	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	OCD mode	Enabled

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.
Note 2. Debug Authentication is defined by the ARMv7-M architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both are not permitted.

2.5.2 Debug Mode Effects

This section describes the effects of debug mode, which occur both internally and externally to the CPU.

2.5.2.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby or Snooze mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.6.5.3, MCU Control Register (MCUCTRL).

2.5.2.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR setting.

Table 2.5 Reset or interrupt and mode setting (1 of 2)

	Control in On-Chip Debug (OCD) mode	
Reset or Interrupt name	**OCD break mode**	**OCD run mode**
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting*2

2.4 JTAG/SWD Interface

表2.3显示了JTAGSWD引脚。

Table 2.3 JTAG/SWD pins

Name	I/O	P/N	Width	Function	不使用时
TCK/SWCLK	Input	Pos.	1 bit	JTAG时钟引脚 SWD时钟引脚	Pull-up
TMS/SWDIO	I/O	Neg.	1 bit	JTAG TMS pin SWD I/O pin	Pull-up
TDI	Input	Pos.	1 bit	JTAG TDI pin	Pull-up
TDO/SWO	Output	Neg.	1 bit	JTAGTDO引脚 与串行线输出复用	Open

2.5 调试模式

2.5.1 调试模式定义

在单片机模式下，连接的调试器状态定义为OCD模式，断开的调试器状态定义为用户模式。表2.4显示了CPU调试模式和使用条件。

Table 2.4 CPU调试模式和条件

Conditions		Mode	
强迫症连接	**JTAG/SWD authentication**	**调试模式**	**调试认证**
未连接	-	用户模式	Disabled
Connected	Failed	用户模式	Disabled
Connected	Passed	强迫症模式	Enabled

Note 1. OCD连接由SWJ-DP寄存器中的CDBGPWRUPREQ位输出决定。该位只能由强迫症。但是，可以通过读取DBGSTR.CDBGPWUPREQ位来确认该位的电平。
Note 2. 调试身份验证由ARMv7-M架构定义。启用意味着允许侵入式和非侵入式CPU调试。禁用意味着两者都不允许。

2.5.2 调试模式效果

本节描述调试模式的影响，它在CPU内部和外部都发生。

2.5.2.1 低功耗模式

即使CPU进入软件待机或贪睡模式，所有CoreSight调试组件都可以存储寄存器设置。但是，AHB-AP在这些低功耗模式下无法响应片上调试(OCD)访问。OCD必须等待取消低功耗模式才能访问CoreSight调试组件。要请求取消低功耗模式，OCD可以设置MCUCTRL寄存器中的DBIRQ位。有关详细信息，请参见第2.6.5.3节，MCU控制寄存器（MCUCTRL）。

2.5.2.2 Reset

在OCD模式下，一些复位取决于CPU状态和DBGSTOPCR设置。

Table 2.5 复位或中断和模式设置（1of2）

	片上调试(OCD)模式下的控制	
复位或中断名称	**强迫症休息模式**	**强迫症运行模式**
RES引脚复位	与用户模式相同	
Power-on reset	与用户模式相同	
独立看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置*2

Table 2.5 Reset or interrupt and mode setting (2 of 2)

Reset or Interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting*2
Voltage monitor 0 reset	Depends on DBGSTOPCR setting*3	
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting*3	
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting*3	
SRAM ECC error reset/interrupt	Depends on DBGSTOPCR setting*3	
MPU bus master reset/interrupt	Same as user mode	
MPU bus slave reset/interrupt	Same as user mode	
Stack pointer error reset/interrupt	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.
Note 2. The IWDT and WDT operation depends on the DBGSTOPCR setting.
Note 3. Reset or interrupt masking depends on the DBGSTOPCR setting.

2.6 Programmers Model

2.6.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD register.

Figure 2.2 shows a block diagram of the AP connection and address spaces.

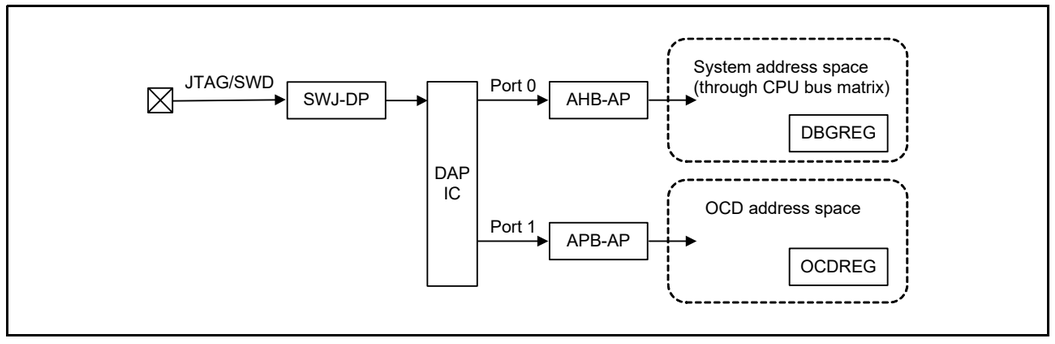


Figure 2.2 JTAG/SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access the OCD registers.

2.6.2 Cortex-M4 Peripheral Address Map

In the system address space, the Cortex-M4 core has a Private Peripheral Bus (PPB) that can only be accessed from the CPU and OCD emulator. The PPB is expanded from the Cortex-M4 original implementation for the MCU. Table 2.6 shows the address map of the MCU.

Table 2.5 复位或中断和模式设置(2of2)

复位或中断名称	片上调试(OCD)模式下的控制	
	强迫症休息模式	强迫症运行模式
看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置*2
电压监控器0复位	取决于DBGSTOPCR设置*3	
电压监视器1复位中断	取决于DBGSTOPCR设置*3	
SRAM奇偶校验错误复位中断	取决于DBGSTOPCR设置*3	
SRAM ECC error reset/interrupt	取决于DBGSTOPCR设置*3	
MPU总线主机复位中断	与用户模式相同	
MPU总线从机复位中断	与用户模式相同	
堆栈指针错误复位中断	与用户模式相同	
软件复位	与用户模式相同	

Note: 在OCD中断模式下，CPU停止。在OCD运行模式下，CPU处于OCD模式并且CPU不会停止。
Note 1. IWDT和WDT始终在此模式下停止。
Note 2. IWDT和WDT操作取决于DBGSTOPCR设置。
Note 3. 复位或中断屏蔽取决于DBGSTOPCR设置。

2.6 程序员模型

2.6.1 地址空间

MCU调试系统包括两个CoreSight访问端口(AP)：

- AHB-AP，与CPU总线矩阵相连，与系统地址空间具有相同的访问权限CPU
- APB-AP，它有一个专用的地址空间（OCD地址空间），并与OCD寄存器相连。

图2.2显示了AP连接和地址空间的框图。

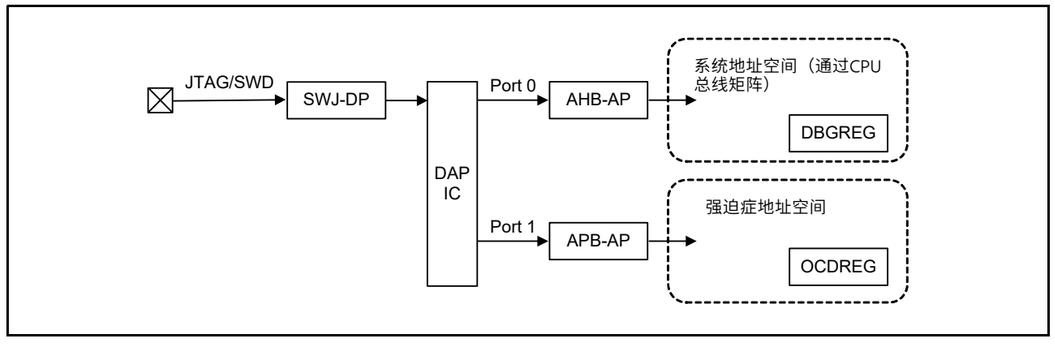


Figure 2.2 JTAGSWD认证框图

出于调试目的，有两个寄存器模块，DBGREG和OCDREG。DBGREG位于系统地址空间中，可以从OCD仿真器、CPU和MCU中的其他总线主控器访问。OCDREG位于OCD地址空间，只能从OCD工具访问。CPU和其他总线主机无法访问OCD寄存器。

2.6.2 Cortex-M4外设地址映射

在系统地址空间中，Cortex-M4内核有一个私有外设总线(PPB)，只能从CPU和强迫症模拟器。PPB从MCU的Cortex-M4原始实现扩展而来。表2.6显示了MCU的地址映射。

Table 2.6 Cortex-M4 peripheral address map

Component name	Start address	End address	Note
ITM	E000 0000h	E000 0FFFh	See reference 2.
DWT	E000 1000h	E000 1FFFh	See reference 2.
FPB	E000 2000h	E000 2FFFh	See reference 2.
SCS	E000 E000h	E000 EFFFh	See reference 2.
TPIU	E004 0000h	E004 0FFFh	See reference 2.
ETM	E004 1000h	E004 1FFFh	See reference 5.
ATB Funnel	E004 2000h	E004 2FFFh	See section 2.7 and reference 4.
ETB	E004 3000h	E004 3FFFh	See reference 6.
Time Stamp Generator	E004 4000h	E004 4FFFh	See section 2.10 and reference 4.
ROM Table	E00F F000h	E00F FFFFh	See section 2.6.3 and reference 7.

2.6.3 CoreSight ROM Table

The MCU contains one CoreSight ROM Table, which lists the Arm components.

2.6.3.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 7. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Target module
0	E00F F000h	32 bits	R	FFF0 F003h	SCS
1	E00F F004h	32 bits	R	FFF0 2003h	DWT
2	E00F F008h	32 bits	R	FFF0 3003h	FPB
3	E00F F00Ch	32 bits	R	FFF0 1003h	ITM
4	E00F F010h	32 bits	R	FFF4 1003h	TPIU
5	E00F F014h	32 bits	R	FFF4 2003h	ETM
6	E00F F018h	32 bits	R	FFF4 3003h	Funnel
7	E00F F01Ch	32 bits	R	FFF4 4003h	ETB
8	E00F F020h	32 bits	R	FFF4 5003h	TSG
9	E00F F024h	32 bits	R	0000 0000h	(End of entries)

2.6.3.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.8 shows the registers. See reference 7. for details of each register.

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	E00F FFCCh	32 bits	R	0000 0001h
PID4	E00F FFD0h	32 bits	R	0000 0004h
PID5	E00F FFD4h	32 bits	R	0000 0000h
PID6	E00F FFD8h	32 bits	R	0000 0000h

Table 2.6 Cortex-M4外设地址映射

组件名称	起始地址	结束地址	Note
ITM	E000 0000h	E000 0FFFh	参见参考文献2。
DWT	E000 1000h	E000 1FFFh	参见参考文献2。
FPB	E000 2000h	E000 2FFFh	参见参考文献2。
SCS	E000 E000h	E000 EFFFh	参见参考文献2。
TPIU	E004 0000h	E004 0FFFh	参见参考文献2。
ETM	E004 1000h	E004 1FFFh	参见参考文献5。
ATB Funnel	E004 2000h	E004 2FFFh	参见第2.7节和参考4。
ETB	E004 3000h	E004 3FFFh	参见参考文献6。
时间戳生成器	E004 4000h	E004 4FFFh	请参阅第2.10节和参考4。
只读存储器表	E00F F000h	E00F FFFFh	参见第2.6.3节和参考7。

2.6.3 CoreSightROM表

MCU包含一个CoreSightROM表，其中列出了Arm组件。

2.6.3.1 ROM条目

表2.7显示了CoreSightROM表中的ROM条目。OCD仿真器可以使用ROM条目来确定系统中实现了哪些组件。有关详细信息，请参见参考资料7。

Table 2.7 CoreSightROM表

#	Address	访问大小	R/W	Value	目标模块
0	E00F F000h	32 bits	R	FFF0 F003h	SCS
1	E00F F004h	32 bits	R	FFF0 2003h	DWT
2	E00F F008h	32 bits	R	FFF0 3003h	FPB
3	E00F F00Ch	32 bits	R	FFF0 1003h	ITM
4	E00F F010h	32 bits	R	FFF4 1003h	TPIU
5	E00F F014h	32 bits	R	FFF4 2003h	ETM
6	E00F F018h	32 bits	R	FFF4 3003h	Funnel
7	E00F F01Ch	32 bits	R	FFF4 4003h	ETB
8	E00F F020h	32 bits	R	FFF4 5003h	TSG
9	E00F F024h	32 bits	R	0000 0000h	(End of entries)

2.6.3.2 CoreSight组件寄存器

CoreSightROM表列出了ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.8显示了寄存器。有关每个寄存器的详细信息，请参见参考资料7。

Table 2.8 CoreSightROM表中的CoreSight组件寄存器(1of2)

Name	Address	访问大小	R/W	初始值
DEVTYPE	E00F FFCCh	32 bits	R	0000 0001h
PID4	E00F FFD0h	32 bits	R	0000 0004h
PID5	E00F FFD4h	32 bits	R	0000 0000h
PID6	E00F FFD8h	32 bits	R	0000 0000h

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	E00F FFDCh	32 bits	R	0000 0000h
PID0	E00F FFE0h	32 bits	R	0000 0013h
PID1	E00F FFE4h	32 bits	R	0000 0030h
PID2	E00F FFE8h	32 bits	R	0000 000Ah
PID3	E00F FFECh	32 bits	R	0000 0000h
CID0	E00F FFF0h	32 bits	R	0000 000Dh
CID1	E00F FFF4h	32 bits	R	0000 0010h
CID2	E00F FFF8h	32 bits	R	0000 0005h
CID3	E00F FFFCh	32 bits	R	0000 00B1h

2.6.4 DBGREG Module

The DBGREG register module controls the debug functionalities and is implemented as a CoreSight compliant component.

Table 2.9 shows the DBGREG registers other than the CoreSight component registers.

Table 2.9 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	4001 B000h	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W
Trace Control Register	TRACECTR	Port 0	4001 B020h	32 bits	R/W

2.6.4.1 Debug Status Register (DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0	R
b28	CDBGPWRUPREQ	Debug power-up request	0: OCD is not requesting debug power-up 1: OCD is requesting debug power-up.	R
b29	CDBGPWRUPACK	Debug power-up acknowledge	0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged.	R
b31, b30	—	Reserved	These bits are read as 0	R

Table 2.8 CoreSightROM表中的CoreSight组件寄存器(2of2)

Name	Address	访问大小	R/W	初始值
PID7	E00F FFDCh	32 bits	R	0000 0000h
PID0	E00F FFE0h	32 bits	R	0000 0013h
PID1	E00F FFE4h	32 bits	R	0000 0030h
PID2	E00F FFE8h	32 bits	R	0000 000Ah
PID3	E00F FFECh	32 bits	R	0000 0000h
CID0	E00F FFF0h	32 bits	R	0000 000Dh
CID1	E00F FFF4h	32 bits	R	0000 0010h
CID2	E00F FFF8h	32 bits	R	0000 0005h
CID3	E00F FFFCh	32 bits	R	0000 00B1h

2.6.4 DBGREG Module

DBGREG寄存器模块控制调试功能，并被实现为符合CoreSight的组件。

表2.9显示了除CoreSight组件寄存器之外的DBGREG寄存器。

Table 2.9 Non-CoreSight DBGREG registers

Name		端口	Address	访问大小	R/W
调试状态寄存器	DBGSTR	Port 0	4001 B000h	32 bits	R
调试停止控制寄存器	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W
跟踪控制寄存器	TRACECTR	Port 0	4001 B020h	32 bits	R/W

2.6.4.1 调试状态寄存器(DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b27 to b0	—	Reserved	这些位被读为0	R
b28	CDBGPWRUPREQ	调试上电请求	0：OCD不请求调试上电1：OCD请求调试上电。	R
b29	CDBGPWRUPACK	调试上电确认	0：未确认调试上电请求1：确认调试上电请求。	R
b31, b30	—	Reserved	这些位被读为0	R

2.6.4.2 Debug Stop Control Register (DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	—	DBGSTOP_LVD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	DBGSTOP_IWDT	Mask bit for IWDT reset or interrupt	0: Enable IWDT reset or interrupt 1: Mask IWDT reset or interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b1	DBGSTOP_WDT	Mask bit for WDT reset or interrupt	0: Enable WDT reset or interrupt 1: Mask WDT reset or interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DBGSTOP_LVD[1:0]	Mask bit for LVD0 reset	0: Enable LVD0 reset 1: Mask LVD0 reset.	R/W
b17		Mask bit for LVD1 reset or interrupt	0: Enable LVD1 reset or interrupt 1: Mask LVD1 reset or interrupt.	R/W
b23 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DBGSTOP_RPER	Mask bit for SRAM parity error reset or interrupt	0: Enable SRAM parity error reset or interrupt 1: Mask SRAM parity error reset or interrupt.	R/W
b25	DBGSTOP_RECCR	Mask bit for SRAM ECC error reset or interrupt	0: Enable SRAM ECC error reset or interrupt 1: Mask SRAM ECC error reset or interrupt.	R/W
b31 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The Debug Stop Control Register (DBGSTOPCR) specifies the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.6.4.3 Trace Control Register (TRACECTR)

Address(es): DBG.TRACECTR 4001 B020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ENETBFULL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b30 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	ENETBFULL	Enable bit for halt request on ETB full	0: ETB full does not cause a CPU halt 1: ETB full causes a CPU halt.	R/W

2.6.4.2 调试停止控制寄存器(DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	—	DBGSTOP_LVD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b0	DBGSTOP_IWDT	IWDT复位或中断屏蔽位	0：使能IWDT复位或中断1：当CPU处于OCD中断模式时，屏蔽IWDT复位或中断并停止WDT计数。	R/W
b1	DBGSTOP_WDT	WDT复位或中断屏蔽位	0：使能WDT复位或中断1：当CPU处于OCD中断模式时，屏蔽WDT复位或中断并停止WDT计数。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	DBGSTOP_LVD[1:0]	LVD0复位屏蔽位	0：使能LVD0复位1 ：屏蔽LVD0复位。	R/W
b17		LVD1复位或中断的屏蔽位	0：使能LVD1复位或中断1：屏蔽LVD1复位或中断。	R/W
b23 to b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	DBGSTOP_RPER	SRAM奇偶校验错误复位或中断的屏蔽位	0：使能SRAM奇偶校验错误复位或中断1：屏蔽SRAM奇偶校验错误复位或中断。	R/W
b25	DBGSTOP_RECCR	SRAMECC错误复位或中断的屏蔽位	0：使能SRAMECC错误复位或中断1：屏蔽SRAMECC错误复位或中断。	R/W
b31 to b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W

调试停止控制寄存器(DBGSTOPCR)指定OCD模式下的功能停止。当MCU不处于OCD模式时，寄存器中的所有位都被视为0。

2.6.4.3 跟踪控制寄存器(TRACECTR)

Address(es): DBG.TRACECTR 4001 B020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ENETBFULL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b30 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	ENETBFULL	ETB满时停止请求的启用位	0：ETB满不导致CPU停止1：ETB满导致CPU停止。	R/W

2.6.4.4 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture. Table 2.10 shows these registers. See reference 7. for details of each register.

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	4001 BFD0h	32 bits	R	00000004h
PID5	4001 BFD4h	32 bits	R	00000000h
PID6	4001 BFD8h	32 bits	R	00000000h
PID7	4001 BFDCh	32 bits	R	00000000h
PID0	4001 BFE0h	32 bits	R	00000005h
PID1	4001 BFE4h	32 bits	R	00000030h
PID2	4001 BFE8h	32 bits	R	0000001Ah
PID3	4001 BFECh	32 bits	R	00000000h
CID0	4001 BFF0h	32 bits	R	0000000Dh
CID1	4001 BFF4h	32 bits	R	000000F0h
CID2	4001 BFF8h	32 bits	R	00000005h
CID3	4001 BFFCh	32 bits	R	000000B1h

2.6.5 OCDREG Module

The OCDREG register module controls the On-Chip Debug (OCD) emulator functionalities and is implemented as a CoreSight-compliant component.

Table 2.11 shows the OCDREG registers other than the CoreSight component registers.

Table 2.11 Non-CoreSight OCDREG registers

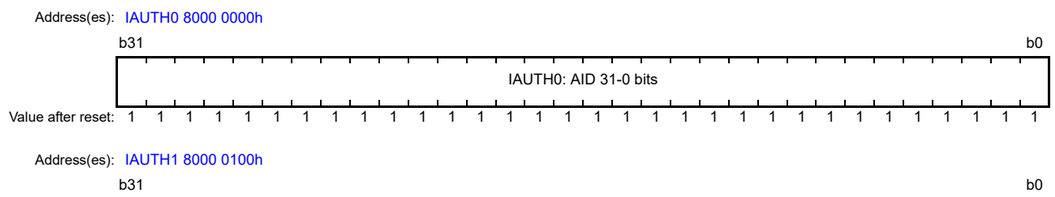
Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	8000 0000h	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	8000 0100h	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	8000 0200h	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	8000 0300h	32 bits	W
MCU Status Register	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU Control Register	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map. See section 2.6.2, Cortex-M4 Peripheral Address Map.

2.6.5.1 ID Authentication Code Register (IAUTH0 to 3)

Four authentication registers are provided for writing the 128-bit key. These registers must be written in sequential order from IAUTH0 to IAUTH3. If the set of register writes is not compliant with this order, the result is unpredictable.

Only 32-bit writes are permitted. The initial value of the registers is all 1s. This means that JTAG/SWD access is initially permitted when the ID code in the OSIS register has the initial value. See section 2.11.2, Unlock ID Code.



2.6.4.4 DBGREGCoreSight组件寄存器

DBGREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。表2.10显示了这些寄存器。有关每个寄存器的详细信息，请参见参考资料7。

Table 2.10 DBGREGCoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	4001 BFD0h	32 bits	R	00000004h
PID5	4001 BFD4h	32 bits	R	00000000h
PID6	4001 BFD8h	32 bits	R	00000000h
PID7	4001 BFDCh	32 bits	R	00000000h
PID0	4001 BFE0h	32 bits	R	00000005h
PID1	4001 BFE4h	32 bits	R	00000030h
PID2	4001 BFE8h	32 bits	R	0000001Ah
PID3	4001 BFECh	32 bits	R	00000000h
CID0	4001 BFF0h	32 bits	R	0000000Dh
CID1	4001 BFF4h	32 bits	R	000000F0h
CID2	4001 BFF8h	32 bits	R	00000005h
CID3	4001 BFFCh	32 bits	R	000000B1h

2.6.5 OCDREG Module

OCDREG寄存器模块控制片上调试(OCD)仿真器功能，并实现为CoreSight-compliant component.

表2.11显示了除CoreSight组件寄存器之外的OCDREG寄存器。

Table 2.11 Non-CoreSight OCDREG registers

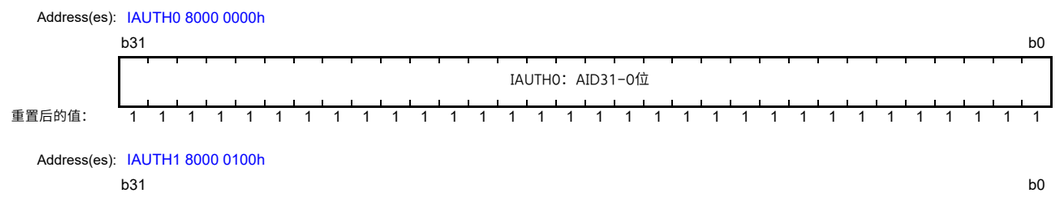
Name		端口	Address	访问大小	R/W
ID验证码寄存器0	IAUTH0	Port 1	8000 0000h	32 bits	W
ID验证码寄存器1	IAUTH1	Port 1	8000 0100h	32 bits	W
ID验证码寄存器2	IAUTH2	Port 1	8000 0200h	32 bits	W
ID验证码寄存器3	IAUTH3	Port 1	8000 0300h	32 bits	W
MCU状态寄存器	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU控制寄存器	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

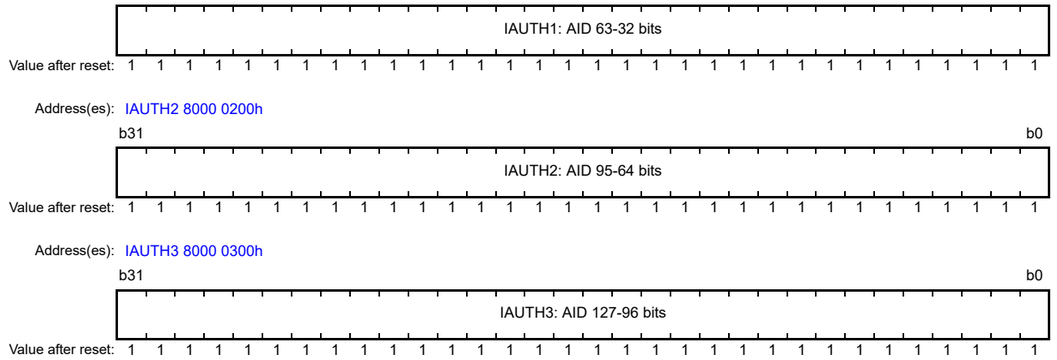
Note: OCDREG位于专用的OCD地址空间中。该地址映射独立于系统地址映射。
请参阅第2.6.2节，Cortex-M4外设地址映射。

2.6.5.1 ID验证码寄存器（IAUTH0至3）

提供了四个认证寄存器用于写入128位密钥。这些寄存器必须按IAUTH0到IAUTH3的顺序写入。如果寄存器写入的集合不符合此顺序，则结果是不可预测的。

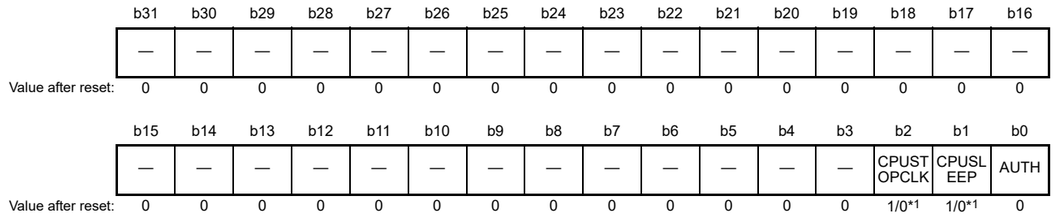
只允许32位写入。寄存器的初始值全为1。这意味着当OSIS寄存器中的ID代码具有初始值时，最初允许JTAGS WD访问。请参阅第2.11.2节，解锁ID代码。





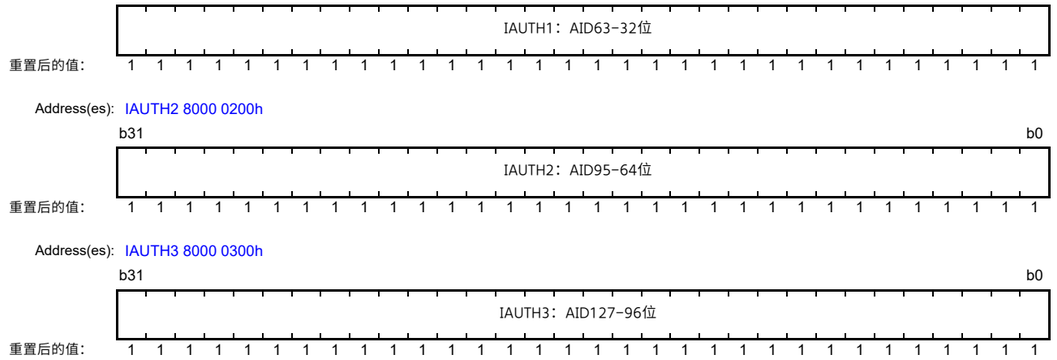
2.6.5.2 MCU Status Register (MCUSTAT)

Address(es): MCUSTAT 8000 0400h



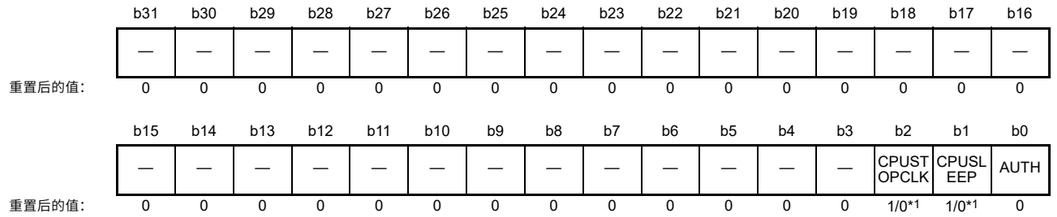
Bit	Symbol	Bit name	Description	R/W
b0	AUTH		0: Authentication failed 1: Authentication succeeded.	R
b1	CPUSLEEP		0: CPU is not in Sleep mode 1: CPU is in Sleep mode.	R
b2	CPUSTOPCLK		0: CPU clock is not stopped. This indicates that the MCU is in Normal mode or Sleep mode 1: CPU clock is stopped. This indicates that the MCU is in Snooze mode or Software Standby mode.	R
b31 to b3	—	Reserved	These bits are read as 0	R

Note 1. Depends on the MCU status.



2.6.5.2 MCU状态寄存器(MCUSTAT)

Address(es): MCUSTAT 8000 0400h



Bit	Symbol	位名称	Description	R/W
b0	AUTH		0：认证失败1：认证成功。	R
b1	CPUSLEEP		0：CPU不处于休眠模式1： CPU处于休眠模式。	R
b2	CPUSTOPCLK		0：CPU时钟不停止。这表明MCU处于正常模式或休眠模式1： CPU时钟停止。这表明MCU处于贪睡模式或软件待机模式。	R
b31 to b3	—	Reserved	这些位被读为0	R

Note 1. 取决于MCU状态。

2.6.5.3 MCU Control Register (MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EDBGRQ	External Debug Request	Writing 1 to the bit causes a CPU halt or debug monitor exception: 0: Debug event not requested 1: Debug event requested. When the EDBGRQ bit is set to 0 or the CPU is halted, the EDBCRQ bit is cleared.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DBIRQ	Debug Interrupt Request	Writing 1 to the bit wakes up the MCU from low power mode: 0: Debug interrupt not requested 1: Debug interrupt requested. The condition can be cleared by writing 0 to the DBIRQ bit.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set DBIRQ and EDBGRQ to the same value.

2.6.5.4 OCDREG CoreSight component registers

The OCDREG module provides the CoreSight component registers defined in the Arm CoreSight architecture

Table 2.12 shows these registers. See reference 7. for details of each register.

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	8000 0FD0h	32 bits	Read only	00000004h
PID5	8000 0FD4h	32 bits	Read only	00000000h
PID6	8000 0FD8h	32 bits	Read only	00000000h
PID7	8000 0FDCh	32 bits	Read only	00000000h
PID0	8000 0FE0h	32 bits	Read only	00000004h
PID1	8000 0FE4h	32 bits	Read only	00000030h
PID2	8000 0FE8h	32 bits	Read only	0000000Ah
PID3	8000 0FECh	32 bits	Read only	00000000h
CID0	8000 0FF0h	32 bits	Read only	0000000Dh
CID1	8000 0FF4h	32 bits	Read only	000000F0h
CID2	8000 0FF8h	32 bits	Read only	00000005h
CID3	8000 0FFCh	32 bits	Read only	000000B1h

2.6.5.3 MCU控制寄存器(MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EDBGRQ	外部调试 Request	向该位写入1会导致CPU停止或调试监视器异常：0：未请求调试事件1：已请求调试事件。当EDBGRQ位设置为0或CPU停止时， EDBCRQ位清零。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	DBIRQ	调试中断 Request	向该位写入1将MCU从低功耗模式唤醒：0：未请求调试中断1：请求调试中断。可以通过将0写入DBIRQ位来清除该条件。	R/W
b31 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 将DBIRQ和EDBGRQ设置为相同的值。

2.6.5.4 OCDREGCoreSight组件寄存器

OCDREG模块提供ArmCoreSight架构中定义的CoreSight组件寄存器

表2.12显示了这些寄存器。有关每个寄存器的详细信息，请参见参考资料7。

Table 2.12 OCDREGCoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	8000 0FD0h	32 bits	只读	00000004h
PID5	8000 0FD4h	32 bits	只读	00000000h
PID6	8000 0FD8h	32 bits	只读	00000000h
PID7	8000 0FDCh	32 bits	只读	00000000h
PID0	8000 0FE0h	32 bits	只读	00000004h
PID1	8000 0FE4h	32 bits	只读	00000030h
PID2	8000 0FE8h	32 bits	只读	0000000Ah
PID3	8000 0FECh	32 bits	只读	00000000h
CID0	8000 0FF0h	32 bits	只读	0000000Dh
CID1	8000 0FF4h	32 bits	只读	000000F0h
CID2	8000 0FF8h	32 bits	只读	00000005h
CID3	8000 0FFCh	32 bits	只读	000000B1h

2.7 CoreSight ATB Funnel

There is one CoreSight ATB funnel in the MCU. The funnel has two ATB slaves and one ATB master, and it selects the debug trace source from ETM and ITM to ETB. Figure 2.3 shows the CoreSight ATB connection in the MCU.

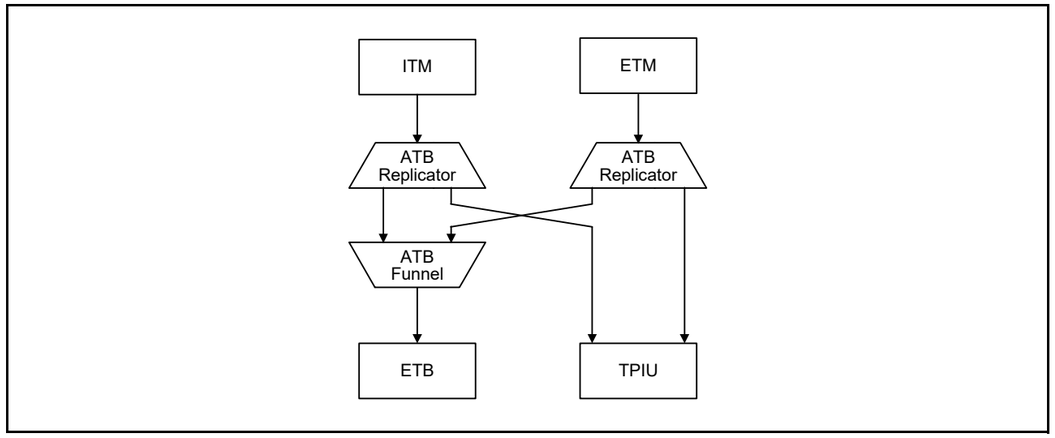


Figure 2.3 CoreSight ATB connection

Table 2.13 shows the ATB slave connection for the funnel.

Table 2.13 ATB slave connection

ATB slave number	Connected trace source
#0	ITM
#1	ETM

For details of ATB and funnel, see reference 4.

2.8 Flash Patch and Break Unit

The MCU has a flash patch and break unit. Breakpoint function is available, but flash patch (remap) function is unavailable. Therefore, do not set the REPLACE bits, [31:30], in the FP_COMPn register to 0. Bit [28] of FP_REMAP register is always set to 1. When writing to this register, write 1 in bit [28]. When reading this register, bit [28] is always read as 1. See reference 1. for details.

2.9 SysTick System Timer

The SysTick system timer provides a simple 24-bit down counter. The reference clock for the timer can be selected as the CPU clock (ICLK) or SysTick Timer clock (SYSTICCLK). See section 9, Clock Generation Circuit and reference 1.*1 for details.

Note 1. In the reference, the IMPLEMENTATION DEFINED external reference clock is SYSTICCLK (LOCO), and the processor clock is ICLK.

2.10 CoreSight Time Stamp Generator

A CoreSight Time Stamp Generator provides a CPU clock-based timestamp to ITM and ETM. The 48 LSB bits of the 64-bit counter are used for the two components. See reference 4. for details.

2.11 OCD Emulator Connection

A JTAG/SWD authentication mechanism checks access permission for debug and chip resources. To obtain full debug functionality, a pass result of the authentication mechanism is required.

Figure 2.4 shows a block diagram of the authentication mechanism.

2.7 CoreSight ATB Funnel

MCU中有一个CoreSightATB漏斗。漏斗有两个ATB从站和一个ATB主站，它选择从ETM和ITM到ETB的调试跟踪源。图2.3显示了MCU中的CoreSightATB连接。

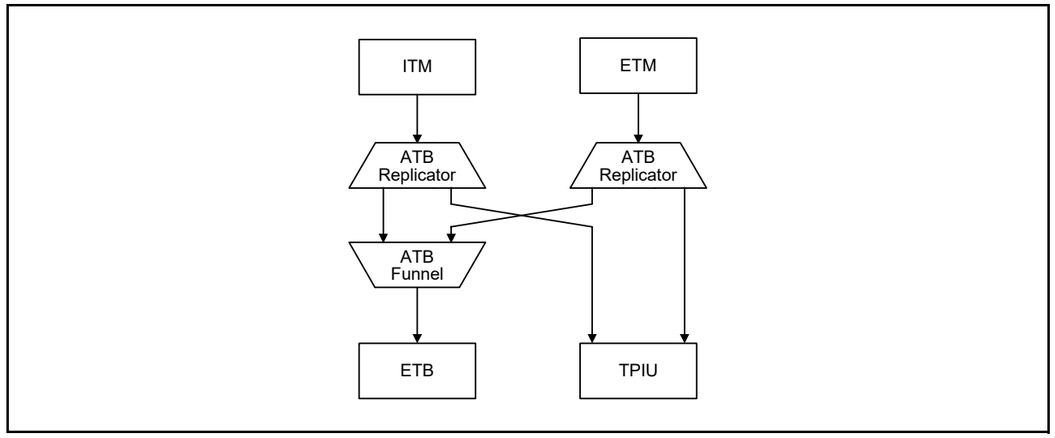


Figure 2.3 CoreSight ATB connection

表2.13显示了漏斗的ATB从属连接。

Table 2.13 ATB从机连接

ATB从机号	连接的跟踪源
#0	ITM
#1	ETM

关于ATB和漏斗的详细信息，请参见参考资料4。

2.8 闪存补丁和中断单元

MCU有一个闪存补丁和中断单元。断点功能可用，但闪存补丁（重映射）功能不可用。因此，不要将FP_COMPn寄存器中的REPLACE位[31:30]设置为0。FP_REMAP寄存器的位[28]始终设置为1。写入该寄存器时，在位[28]中写入1。读取该寄存器时，位[28]始终读取为1。有关详细信息，请参见参考文献1。

2.9 SysTick系统定时器

SysTick系统定时器提供了一个简单的24位递减计数器。定时器的参考时钟可以选择为CPU时钟(ICLK)或SysTick定时器时钟(SYSTICCLK)。请参阅第9节，时钟生成电路和参考1。*1了解详细信息。

注1.在参考中，实现定义的外部参考时钟是SYSTICCLK(LOCO)，处理器时钟是ICLK。

2.10 CoreSight时间戳生成器

CoreSight时间戳生成器为ITM和ETM提供基于CPU时钟的时间戳。64位计数器的48个LSB位用于这两个组件。详见参考文献4。

2.11 OCD模拟器连接

JTAGSWD认证机制检查调试和芯片资源的访问权限。要获得完整的调试功能，需要验证机制的通过结果。

图2.4显示了认证机制的框图。

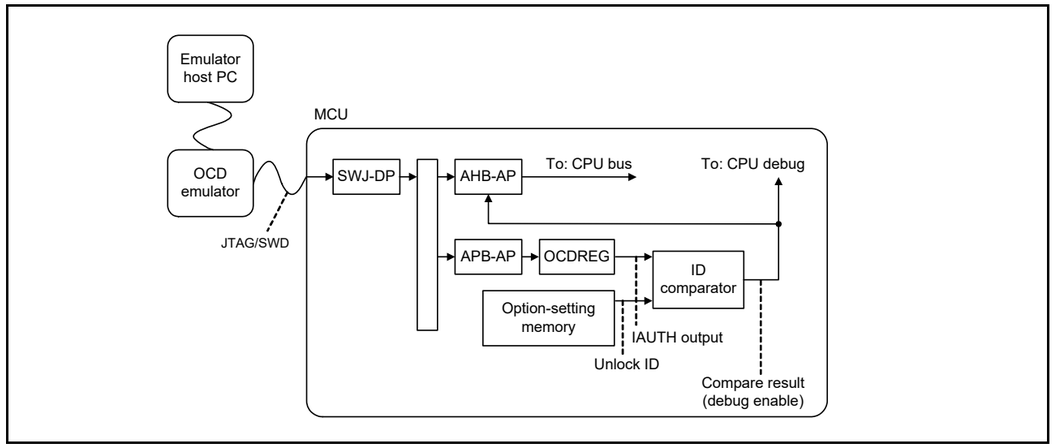


Figure 2.4 Authentication mechanism block diagram

An ID comparator is available in the MCU for authentication. The comparator compares the 128-bit IAUTH output from OCDREG and the 128-bit unlock ID code from the option-setting memory. When the two outputs are identical, the CPU debug functions and system bus access from the OCD emulator are permitted.

2.11.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 11, Low Power Modes for details.

2.11.2 Unlock ID Code

The unlock ID code is used for checking permissions for debug and access to on-chip resources. If the unlock ID code matches the 128-bit data written in the ID Authentication Registers 0 to 3, the JTAG/SWD debugger obtains access permission. Unlock ID code is written in the OCD/Serial Programmer ID Setting Register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (FFFFFFFF_FFFFFFFF_FFFFFFFF_FFFFFFFFh). See section 7, Option-Setting Memory for details.

2.11.3 Restrictions on Connecting an OCD Emulator

This section describes the restrictions on emulator access.

2.11.3.1 Starting connection while in low power mode

When starting a JTAG/SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby or Snooze mode, the OCD emulator can cause the MCU to hang.

2.11.3.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby or Snooze mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the OCD emulator in these modes. Table 2.14 shows the restrictions.

Table 2.14 Restrictions by mode (1 of 2)

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes

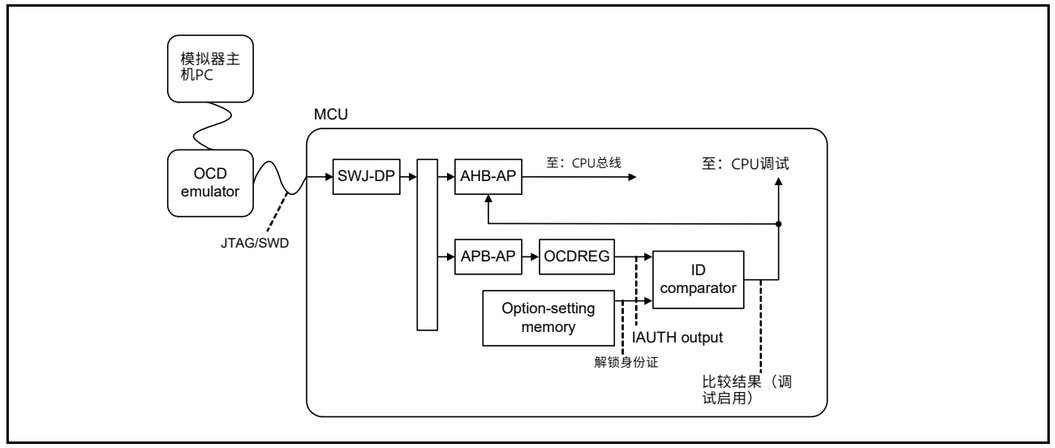


Figure 2.4 认证机制框图

MCU中有一个ID比较器用于身份验证。比较器比较来自OCDREG的128位IAUTH输出和来自选项设置存储器的128位解锁ID代码。当两个输出相同时，允许从OCD仿真器访问CPU调试功能和系统总线。

2.11.1 DBGEN

OCD模拟器获得访问权限后，OCD模拟器必须设置SystemControlOCD中的DBGEN位控制寄存器(SYOCDCR)。此外，OCD仿真器必须在断开连接之前清除DBGEN位。有关详细信息，请参见第11节，低功耗模式。

2.11.2 解锁ID码

解锁ID码用于检查调试权限和对片上资源的访问权限。如果解锁ID代码与写入ID验证寄存器0到3的128位数据匹配，则JTAGSWD调试器获得访问权限。解锁ID代码写入选项设置存储器中的OCD串行编程器ID设置寄存器(OSIS)。解锁ID码初始值为全1（FFFFFFFF_FFFFFFFF_FFFFFFFF_FFFFFFFFh）。有关详细信息，请参阅第7节，选项设置内存。

2.11.3 连接强迫症模拟器的限制

本节介绍对仿真器访问的限制。

2.11.3.1 在低功耗模式下开始连接

从OCD仿真器启动JTAGSWD连接时，MCU必须处于正常或睡眠模式。如果MCU处于软件待机或贪睡模式，OCD仿真器会导致MCU挂起。

2.11.3.2 在OCD模式下更改低功耗模式

当MCU处于OCD模式时，可以更改低功耗模式。但是，在软件待机或贪睡模式下，禁止从AHB-AP访问系统总线。在这些模式下，只能从OCD仿真器访问SWJ-DP、APB-AP和OCDREG。表2.14显示了这些限制。

Table 2.14 模式限制(1of2)

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
软件待机	No	Yes	No	Yes

Table 2.14 Restrictions by mode (2 of 2)

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Snooze	No	Yes	No	Yes

If system bus access is required in Software Standby or Snooze mode, set the MCUCTRL.DBIRQ bit in OCDREG to wake up the MCU from the low power modes. Simultaneously, using the MCUCTRL.EDBGRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.11.3.3 Modifying the unlock ID code in OSIS

After modifying the unlock ID code in OSIS, the OCD emulator must reset the MCU by asserting the RES pin or setting the SYSRESETREQ bit of the Application Interrupt and Reset Control Register in the system control block to 1. The modified unlock ID code is reflected after reset.

2.11.3.4 Connecting sequence and JTAG/SWD authentication

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, the OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required. After the negation of the reset, a 44 µs wait time is required before comparing the OSIS value at cold start.

(1) When MSB of OSIS is 0 (bit [127] = 0)

The ID code is always mismatching and connection to the OCD is prohibited.

(2) When OSIS is all 1s (default)

OCD authentication is not required and the OCD can use the AHB-AP without the authentication.

1. Connect the OCD emulator to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access the DAP Bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
4. Start accessing the CPU debug resources using the AHB-AP.

(3) When OSIS[127:126] is 10b

OCD authentication is required and the OCD must write the unlock code to the IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code matches the OSIS value, the AHB-AP is authorized to issue an AHB transaction. The authorization result can be confirmed by the AUTH bit in the MCUSTAT Register or the DbgStatus bit in the AHB-AP Control Status Word Register.
   - When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
   - When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.
6. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
7. Start accessing the CPU debug resources using the AHB-AP.

(4) When OSIS[127:126] is 11b

OCD authentication is required and the OCD must write the unlock ID code to IAUTH registers 0 to 3 in OCDREG. The

Table 2.14 模式限制(2of2)

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Snooze	No	Yes	No	Yes

如果在软件待机或贪睡模式下需要系统总线访问，设置OCDREG中的MCUCTRL.DBIRQ位以将MCU从低功耗模式唤醒。同时，使用OCDREG中的MCUCTRL.EDBGRQ位，OCD仿真器可以唤醒MCU，而无需使用CPU中断启动CPU执行。

2.11.3.3 修改OSIS中的解锁ID码

在OSIS中修改解锁ID代码后，OCD仿真器必须通过置位RES引脚或将系统控制块中的应用程序中断和复位控制寄存器的SYSRESETREQ位设置为1来复位MCU。修改后的解锁ID代码反映在重置。

2.11.3.4 连接顺序和JTAGSWD认证

由于OCD仿真器受JTAGSWD身份验证机制的保护，因此可能需要OCD将ID代码输入到身份验证寄存器中。选项设置内存中的OSIS值决定是否需要该代码。在复位否定后，在冷启动时比较OSIS值之前需要44微秒的等待时间。

(1) 当OSIS的MSB为0时（位[127]=0）

ID代码总是不匹配，并且禁止连接到OCD。

(2) 当OSIS全为1时（默认）

不需要OCD身份验证，OCD无需身份验证即可使用AHB-AP。

1. 通过JTAG或SWD接口将OCD仿真器连接到MCU。
2. 设置SWJ-DP以访问DAP总线。在设置中，OCD模拟器必须在SWJ-DP控制状态寄存器，然后等到同一寄存器中的CSDBGPWRUPACK置位。
3. 设置AHB-AP以访问系统地址空间。AHB-AP连接到DAP总线端口0。
4. 开始使用AHB-AP访问CPU调试资源。

(3) 当OSIS[127:126]为10b时

需要OCD验证，并且OCD必须在使用AHB-AP之前将解锁码写入OCDREG中的IAUTH寄存器0到3。

1. 通过JTAG或SWD接口将OCD调试器连接到MCU。
2. 设置SWJ-DP以访问DAP总线。在设置中，OCD模拟器必须在SWJ-DP中断言CDBGPWRUPREQ控制状态寄存器，然后等到同一寄存器中的CSDBGPWRUPACK被断言。
3. 设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。
4. 使用APB-AP将128位ID代码写入OCDREG中的IAUTH寄存器0到3。
5. 如果128位ID代码与OSIS值匹配，则授权AHB-AP发出AHB事务。授权结果可以通过MCUSTAT寄存器中的AUTH位或AHBAP控制状态字寄存器中的DbgStatus位来确认。
   - 当DbgStatus位为1时，128位ID码与OSIS值匹配。允许AHB转移。
   - 当DbgStatus位为0时，128位ID代码与OSIS值不匹配。不允许AHB转移。
6. 设置AHB-AP以访问系统地址空间。AHB-AP连接到DAP总线端口0。
7. 开始使用AHB-AP访问CPU调试资源。

(4) 当OSIS[127:126]为11b时

需要OCD身份验证，并且OCD必须将解锁ID代码写入OCDREG中的IAUTH寄存器0到3。这

connection sequence is the same as when OSIS[127:126] is 10b except for ALeRASE capability.

When IATUH0-3 are ALeRASE in ASCII code, the content of code flash, data flash, and the configuration area are erased at once. See section 43, Flash Memory for details.

ALeRASE sequence

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Setup SWJ-DP to access DAP bus. In the set up, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. The APB-AP is connected to DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents of code flash, data flash, and the configuration area are erased. After that, the MCU transitions to Sleep mode.

2.12 References

1. *ARM® v7-M Architecture Reference Manual* (ARM DDI 0403D).
2. *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).
3. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).
5. *ARM® CoreSight™ ETM-M4 Technical Reference Manual* (ARM DDI 0440C).
6. *ARM® CoreSight™ Trace Memory Controller Technical Reference Manual* (ARM DDI 0461B).
7. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029D).

连接顺序与OSIS[127:126]为10b时相同，但ALeRASE功能除外。

当IATUH0-3在ASCII码中为ALeRASE时，codeflash、dataflash和配置区的内容同时被擦除。有关详细信息，请参见第43节，闪存。

ALeRASE sequence

1. 通过JTAG或SWD接口将OCD调试器连接到MCU。
2. 设置SWJ-DP以访问DAP总线。在设置中，OCD模拟器必须在SWJDP中断言CDBGPWRUPREQ控制状态寄存器，然后等到同一寄存器中的CSDBGPWRUPACK被断言。
3. 设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。
4. 使用APB-AP将128位ID代码写入OCDREG中的IAUTH寄存器0到3。
5. 如果128位ID代码是ASCII代码中的ALeRASE(414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh)，则擦除代码闪存、数据闪存和配置区的内容。之后，MCU转换到休眠模式。

2.12 References

1. ARM®v7-M架构参考手册(ARMDDI0403D)。
2. ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)。
3. ARM®Cortex®-M4设备通用用户指南(ARMDUI0553A)。
4. ARM®CoreSight SoC-400技术参考手册(ARMDDI0480F)。
5. ARM®CoreSight ETM-M4技术参考手册(ARMDDI0440C)。
6. ARM®CoreSight 跟踪内存控制器技术参考手册(ARMDDI0461B)。
7. ARM®CoreSight 架构规范(ARMIHI0029D)。

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2, Details of Operating Modes. Operation starts with the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin		
MD	**Operating mode**	**On-chip flash memory**
1	Single-chip mode	Enable
0	SCI/USB boot mode	Enable

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs. When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in a dedicated area within the MCU, is used. The on-chip flash, including the code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (SCI). For details, see section 43, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.2.3 USB Boot Mode

In this mode, the on-chip flash memory programming routine (USB boot program), stored in the boot area within the MCU, is used. The on-chip flash, including the code flash memory and data flash memory, can be modified from outside the MCU by using the USB. For details, see section 43, Flash Memory. The MCU starts in USB boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Mode Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin.

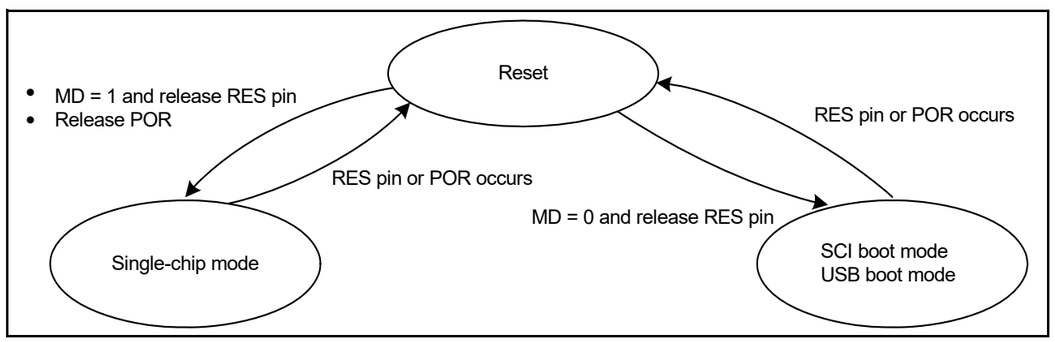


Figure 3.1 Mode-setting pin level and operating mode

3. 操作模式

3.1 Overview

表3.1显示了通过模式设置引脚选择的工作模式。有关详细信息，请参阅第3.2节，详细信息
操作模式。无论操作以何种模式开始，操作都会从启用片上闪存开始。

Table 3.1 通过模式设置引脚选择工作模式

Mode-setting pin		
MD	**操作模式**	**片上闪存**
1	Single-chip mode	Enable
0	SCIUSB启动模式	Enable

3.2 操作模式的详细信息

3.2.1 Single-Chip Mode

在单片机模式下，所有IO引脚都可用作输入或输出端口、外围功能的输入或输出，或用作中断输入。当MD引脚为高电平时释放复位时，MCU以单芯片模式启动，并启用片上闪存。

3.2.2 SCI启动模式

在这种模式下，使用存储在MCU内的专用区域中的片上闪存编程例程（SCI引导程序）。片上闪存，包括代码闪存和数据闪存，可以通过使用通用异步接收发送器(SCI)从MCU外部进行修改。有关详细信息，请参阅第43节，闪存。如果MD引脚在从复位状态释放时保持低电平，则MCU以SCI启动模式启动。

3.2.3 USB启动模式

在这种模式下，片上闪存编程例程（USB引导程序），存储在引导区域内
单片机，使用。片上闪存，包括代码闪存和数据闪存，可以从MCU外部使用USB进行修改。有关详细信息，请参阅第43节，闪存。如果MD引脚在从复位状态释放时保持低电平，则MCU在USB引导模式下启动。

3.3 操作模式转换

3.3.1 由模式设置引脚确定的操作模式转换

图3.1显示了由MD引脚的设置决定的操作模式转换。

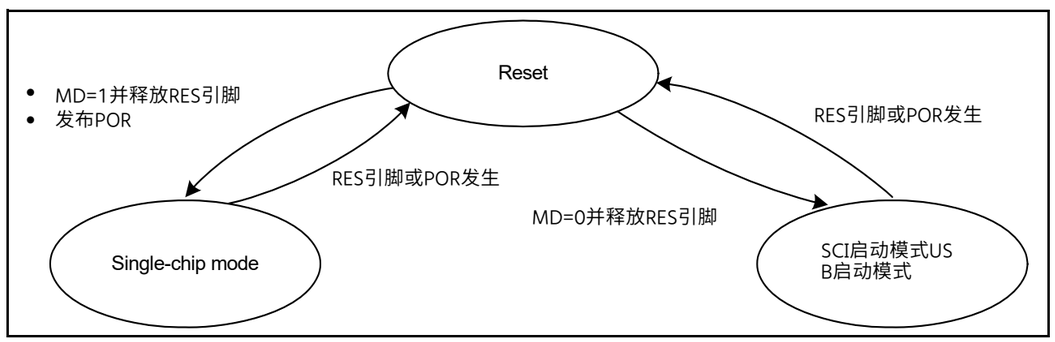
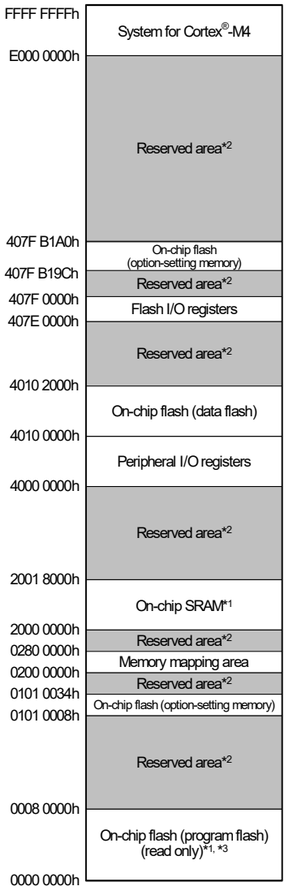


Figure 3.1 模式设置引脚电平和操作模式

4. Address Space

4.1 Overview

The MCU supports a 4-GB linear address space ranging from 0000 0000h to FFFF FFFFh that can contain both program and data. Figure 4.1 shows the memory map.



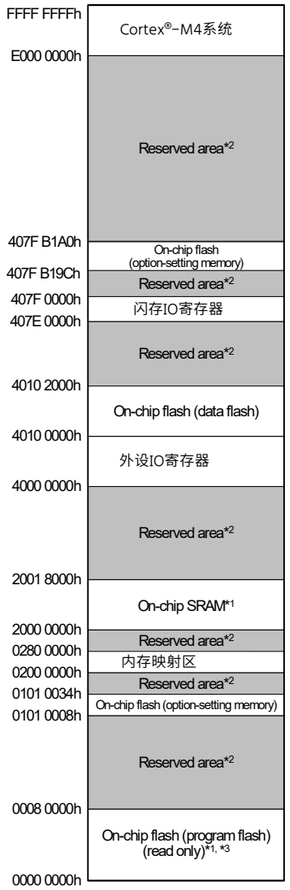
Note 1. The capacity of the flash or SRAM differs depending on the product.
Note 2. Do not access reserved areas.
Note 3. Some regions are reserved for the option-setting memory. For details on the regions, see section 7, Option-Setting Memory.

Figure 4.1 Memory map

4. 地址空间

4.1 Overview

MCU支持4-GB线性地址空间，范围从00000000h到FFFFFFFFh，可以同时包含程序和数据。图4.1显示了内存映射。



Note 1. 闪存或SRAM的容量因产品而异。
Note 2. 不要进入保留区域。
Note 3. 某些区域是为选项设置内存保留的。有关区域的详细信息，请参阅第7节，选项设置Memory.

Figure 4.1 内存映射

5. Memory Mirror Function (MMF)

5.1 Overview

The MCU provides a Memory Mirror Function (MMF). You can configure the MMF to map an application image load address in the code flash memory to the application image link address in the unused 23-bit memory mirror space addresses. Your application code must be developed and linked to run from this MMF destination address. The application code is not required to know the load location where it is stored in the code flash memory.

Table 5.1 lists the MMF specifications.

Table 5.1 MMF specifications

Parameter	Description
Memory mirror space	8 MB (0200 0000h to 027F FFFFh)
Memory mirror boundary	128 bytes

5.2 Register Descriptions

5.2.1 MemMirror Special Function Register (MMSFR)

Address(es): MMF.MMSFR 4000 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	MEMMIRADDR[15:9]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MEMMIRADDR[8:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22 to b7	MEMMIRADDR[15:0]	Memory Mirror Address	0000h to FFFFh (8 MB)	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b24	KEY[7:0]	MMSFR Key Code	These bits enable or disable rewriting of the MEMMIRADDR bits	R/W

MEMMIRADDR[15:0] bits (Memory Mirror Address)

The MEMMIRADDR bits specify bits [22:7] of the memory mirror address. They define where the start address of the memory mirror space addresses (0200 0000h) is linked to. Writing to these bits is enabled only when this register is accessed in 32-bit words and the value DBh is written to the KEY[7:0] bits.

KEY[7:0] bits (MMSFR Key Code)

The KEY[7:0] bits enable or disable rewriting of the MEMMIRADDR bits. Data written to the KEY bits is not saved. These bits are read as 0. The KEY code and MEMMIRADDR must be written to in the same cycle.

5. 内存镜像功能(MMF)

5.1 Overview

MCU提供内存镜像功能(MMF)。您可以配置MMF以将代码闪存中的应用程序映像加载地址映射到未使用的23位内存镜像空间地址中的应用程序映像链接地址。您的应用程序代码必须经过开发和链接才能从此MMF目标地址运行。应用程序代码不需要知道它存储在代码闪存中的加载位置。

表5.1列出了MMF规范。

Table 5.1 MMF specifications

Parameter	Description
内存镜像空间	8 MB (0200 0000h to 027F FFFFh)
内存镜像边界	128 bytes

5.2 注册说明

5.2.1 MemMirror特殊功能寄存器(MMSFR)

Address(es): MMF.MMSFR 4000 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	MEMMIRADDR[15:9]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MEMMIRADDR[8:0]								—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b22 to b7	MEMMIRADDR[15:0]	内存镜像地址	0000h to FFFFh (8 MB)	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b31 to b24	KEY[7:0]	MMSFR密钥代码	这些位启用或禁用重写 MEMMIRADDR bits	R/W

MEMMIRADDR[15:0]位（内存镜像地址）

MEMMIRADDR位指定内存镜像地址的位[22:7]。它们定义了内存镜像空间地址（02000000h）的起始地址链接到哪里。仅当以32位字访问该寄存器并将值DBh写入KEY[7:0]位时，才能写入这些位。

KEY[7:0]位（MMSFR密钥代码）

KEY[7:0]位启用或禁用MEMMIRADDR位的重写。不保存写入KEY位的数据。
这些位读为0。KEY代码和MEMMIRADDR必须在同一个周期内写入。

5.2.2 MemMirror Enable Register (MMEN)

Address(es): MMF.MMEN 4000 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b0	EN	Memory Mirror Function Enable	0: Disable MMF 1: Enable MMF.	R/W
b23 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b24	KEY[7:0]	MMEN Key Code	These bits enable or disable rewriting of the EN bit.	R/W

EN bit (Memory Mirror Function Enable)

Writing to the EN bit is enabled only when the MemMirror Enable Register is accessed in 32-bit words and the value DBh is written to the KEY[7:0] bits.

KEY[7:0] bits (MMEN Key Code)

The KEY[7:0] bits enable or disable rewriting of the EN bit. Data written to the KEY[7:0] bits is not saved. These bits are read as 0. The KEY code and the EN bit must be written in the same cycle.

5.3 Operation

5.3.1 MMF Operation

The MMF links the memory mirror space (0200 0000h to 027F FFFFh) to the code flash area. If MMEN.EN = 1, the CPU can access code flash using both normal addresses (starting at 0000 0000h) and memory mirror space addresses (starting at 0200 0000h). Figure 5.1 shows an overview of the MMF. The MMSFR.MEMMIRADDR bits specify where the start address of the memory mirror space addresses (0200 0000h) is linked to. Figure 5.2, Figure 5.3, and Figure 5.4 show the operation of the MMF. Figure 5.5 shows the setting procedure of the MMF.

5.2.2 MemMirror启用寄存器(MMEN)

Address(es): MMF.MMEN 4000 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b0	EN	内存镜像功能 Enable	0：禁用MMF1 ：启用MMF。	R/W
b23 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b24	KEY[7:0]	MMEN键码	这些位启用或禁用EN位的重写。	R/W

EN位（内存镜像功能使能）

仅当以32位字访问MemMirror使能寄存器并且值
DBh被写入KEY[7:0]位。

KEY[7:0]位（MMEN键码）

KEY[7:0]位启用或禁用EN位的重写。写入KEY[7:0]位的数据不保存。这些位读为0。KEY代码和EN位必须在同一个周期内写入。

5.3 Operation

5.3.1 MMF Operation

MMF将内存镜像空间（02000000h到027FFFFFh）链接到代码闪存区域。如果MMEN.EN=1，CPU可以使用普通地址（从00000000h开始）和内存镜像空间地址（从02000000h开始）访问代码闪存。图5.1显示了MMF的概述。MMSFR.MEMMIRADDR位指定内存镜像空间地址(02000000h)的起始地址链接到的位置。图5.2、图5.3和图5.4显示了MMF的操作。图5.5显示了MMF的设置过程。

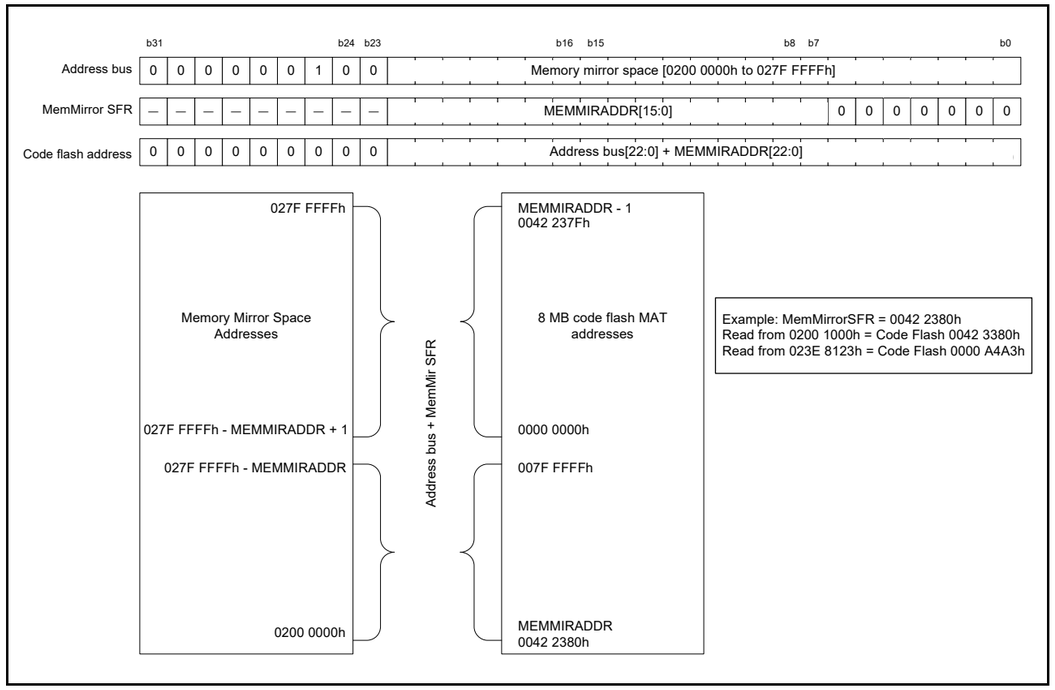
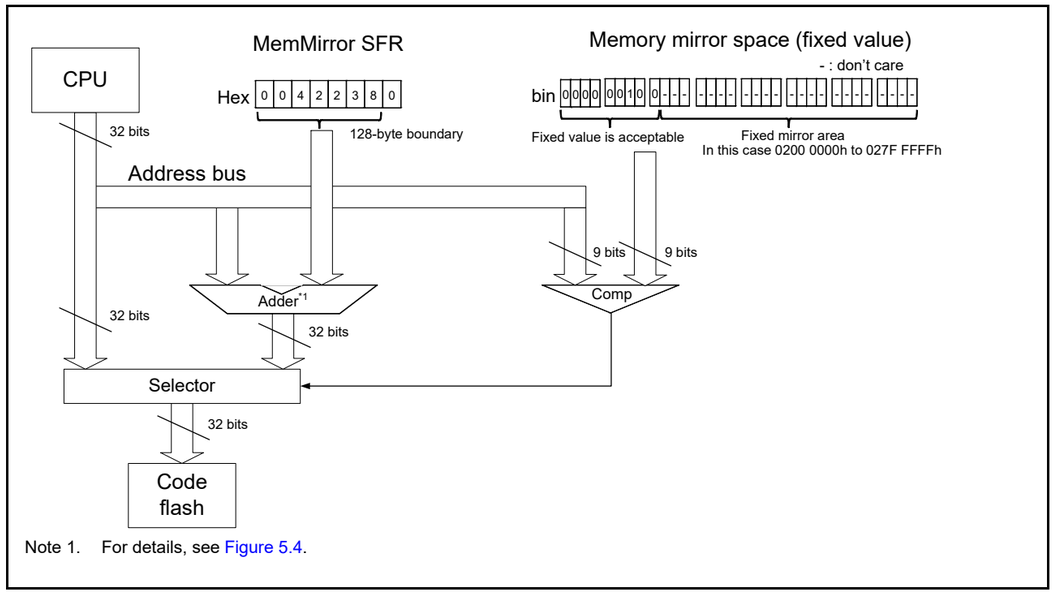


Figure 5.1 MMF operation



Note 1. For details, see Figure 5.4.

Figure 5.2 MMF block diagram

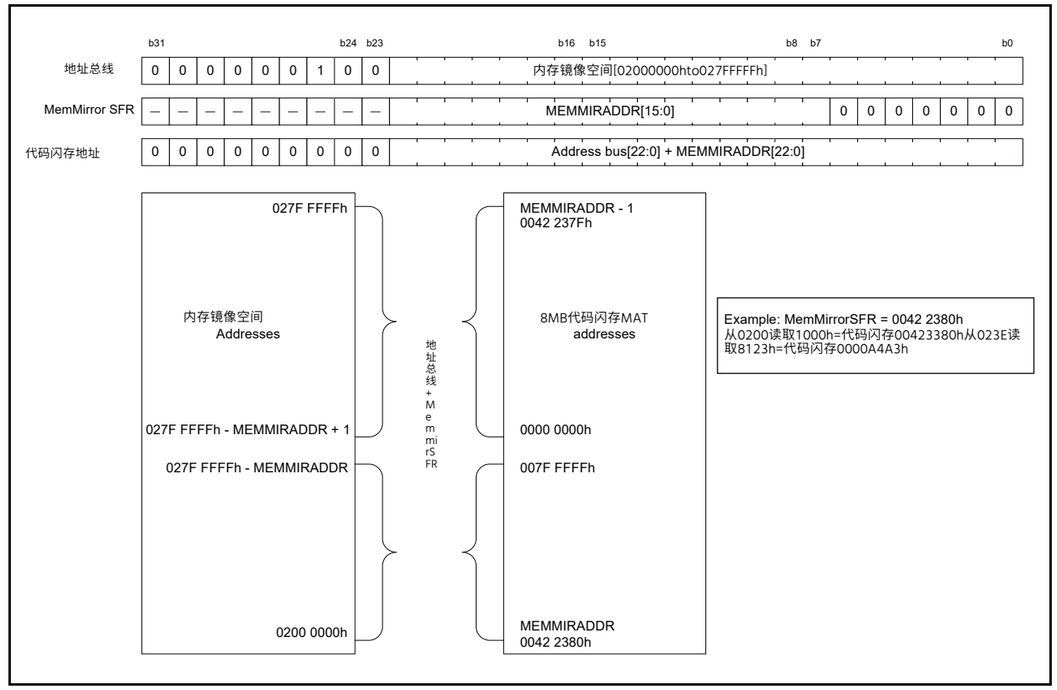
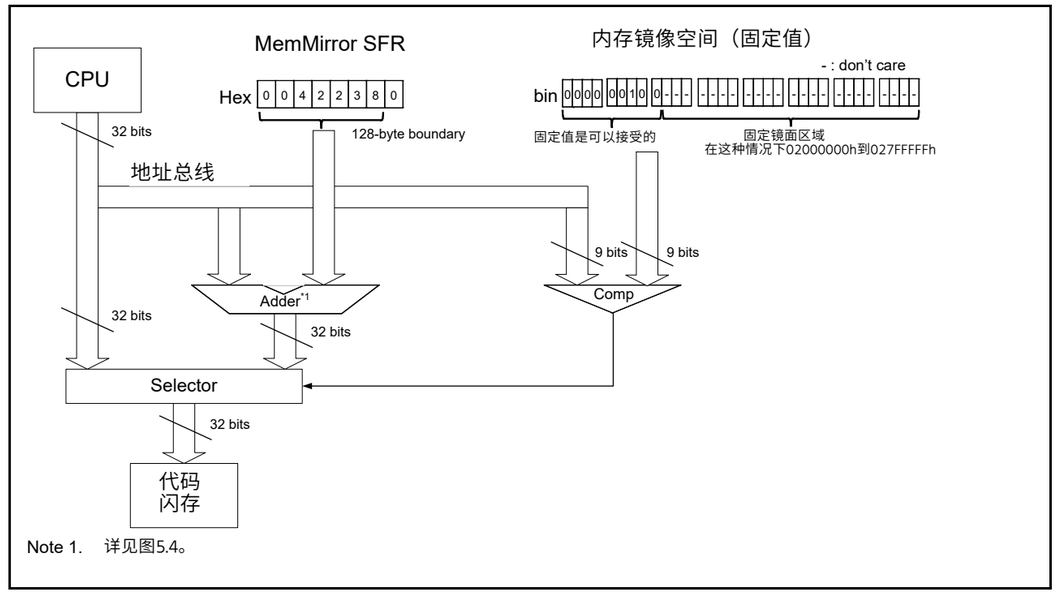


Figure 5.1 MMF operation



Note 1. 详见图5.4。

Figure 5.2 MMF框图

Figure 5.3 shows the addresses handled by each module. The Arm® MPU uses the original address of the CPU. The Security MPU and code flash memory each use an address after conversion through the Memory Mirror Function.

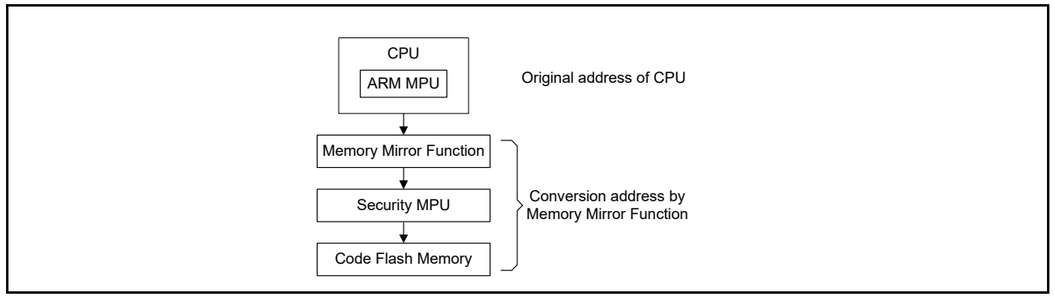


Figure 5.3 MMF address handling

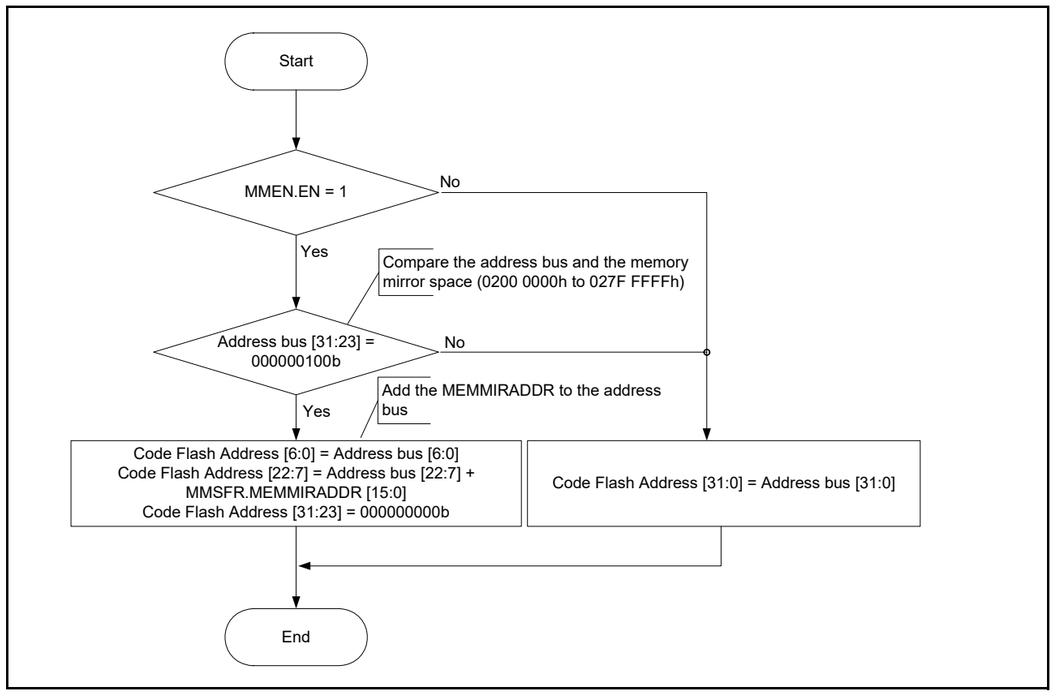


Figure 5.4 MMF operation flow

图5.3显示了每个模块处理的地址。Arm®MPU使用CPU的原始地址。这安全MPU和代码闪存各使用一个通过内存镜像功能转换后的地址。

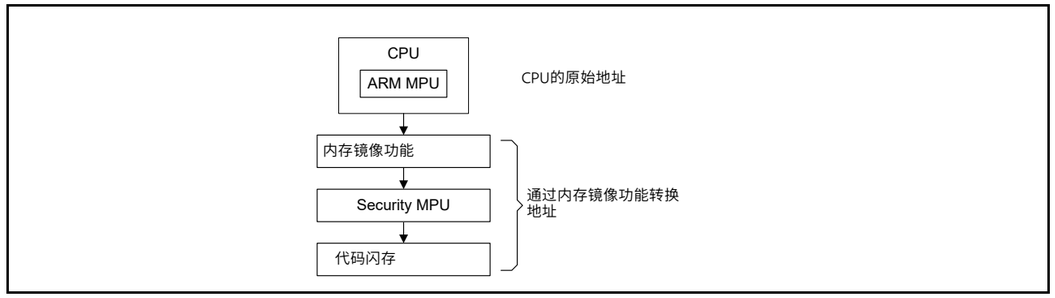


Figure 5.3 MMF地址处理

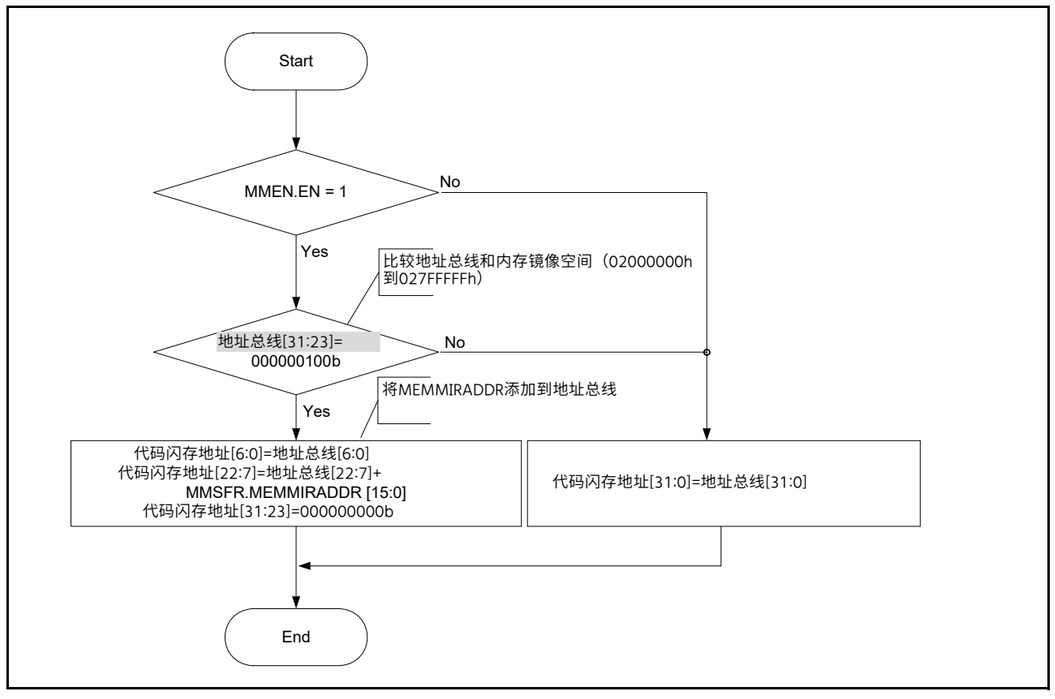


Figure 5.4 MMF操作流程

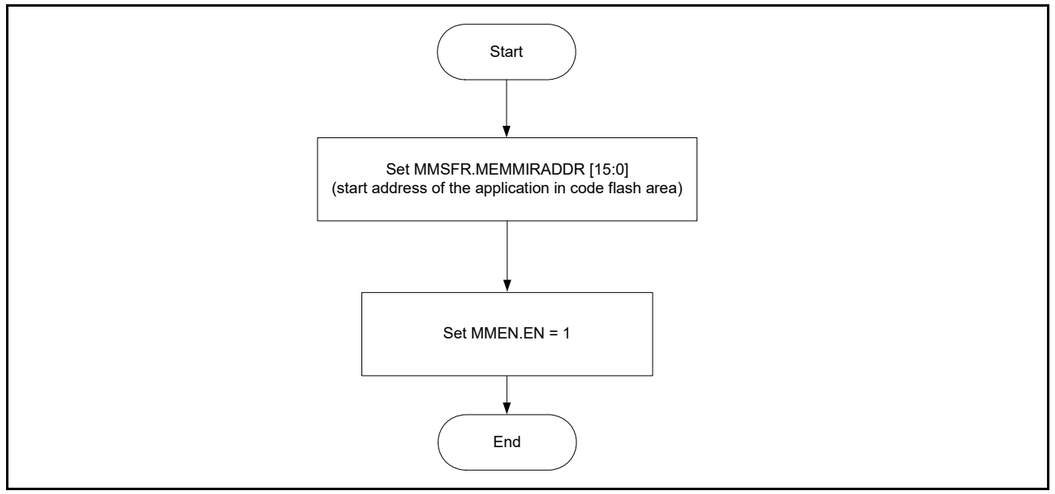


Figure 5.5 MMF setup flow

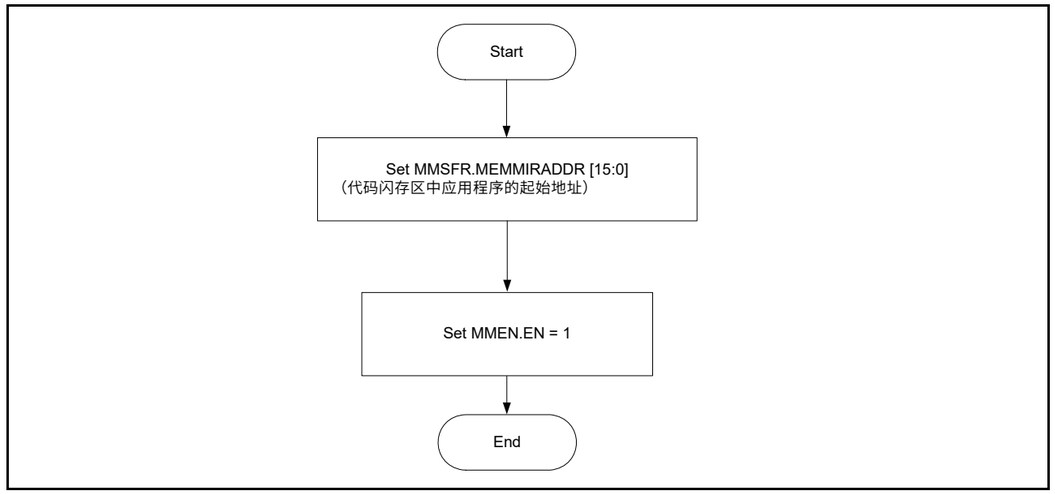


Figure 5.5 MMF设置流程

5.3.2 Setting Example

The target application code on the code flash can be accessed from the address of 0200 0000h on the memory mirror space by setting up the code flash start address in MMSFR.MEMMIRADDR and setting MMEN.EN to 1.

Figure 5.6 shows an example of how to use the MMF.

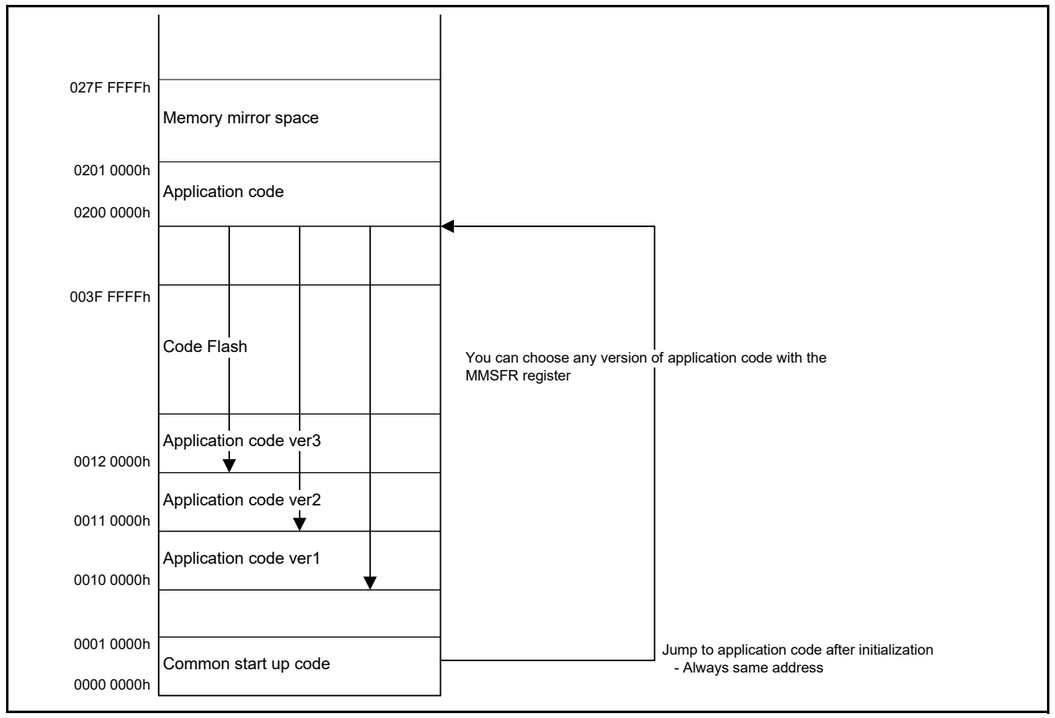


Figure 5.6 MMF setting example

Setting the MMSFR register to DB10 0000h to use the application code ver1.

Setting the MMSFR register to DB11 0000h to use the application code ver2.

Setting the MMSFR register to DB12 0000h to use the application code ver3.

5.3.2 设置示例

通过在MMSFR.MEMMIRADDR中设置代码闪存起始地址并将MMEN.EN设置为1，可以从内存镜像空间上的02000000h地址访问代码闪存上的目标应用程序代码。

图5.6显示了如何使用MMF的示例。

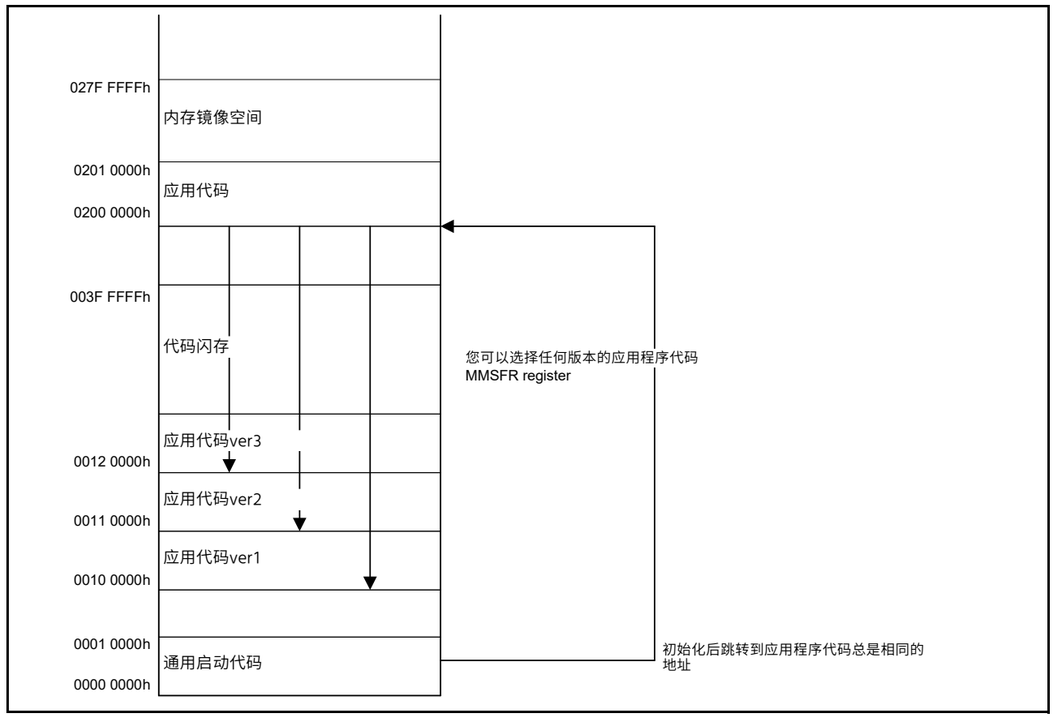


Figure 5.6 MMF设置示例

将MMSFR寄存器设置为DB100000h以使用应用程序代码ver1。

将MMSFR寄存器设置为DB110000h以使用应用程序代码ver2。

将MMSFR寄存器设置为DB120000h以使用应用程序代码ver3。

6. Resets

6.1 Overview

The MCU provides 14 resets:

- RES pin reset
- Power-on reset
- VBATT-selected voltage power-on reset
- Independent watchdog timer reset
- Watchdog timer reset
- Voltage monitor 0 reset
- Voltage monitor 1 reset
- SRAM parity error reset
- SRAM ECC error reset
- Bus master MPU error reset
- Bus slave MPU error reset
- Stack pointer error reset
- Software reset.

Table 6.1 lists the reset names and sources.

Table 6.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
VBATT selected voltage power-on reset	VCC fall (voltage detection $V_{DETBATT}$)*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog Timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
SRAM parity error reset	SRAM parity error detection
SRAM ECC error reset	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection
Bus slave MPU error reset	Bus slave MPU error detection
Stack pointer error reset	Stack pointer error detection
Software reset	Register setting (use the Arm® software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1} and $V_{DETBATT}$), see section 8, Low Voltage Detection (LVD), section 12., Battery Backup Function, and section 48, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 6.2 and Table 6.3 list the targets initialized by resets.

Table 6.2 Reset detect flags initialized by each reset source (1 of 2)

	Reset source						
Flags to be initialized	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Software reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	×	×	×	×	×	×

6. Resets

6.1 Overview

MCU提供14次复位：

- RES引脚复位
- Power-on reset
- VBATT-选择电压上电复位
- 独立看门狗定时器复位
- 看门狗定时器复位
- 电压监控器0复位
- 电压监视器1复位
- SRAM奇偶校验错误复位
- SRAMECC错误复位
- 总线主控MPU错误复位
- 总线从机MPU错误复位
- 堆栈指针错误复位
- 软件复位。

表6.1列出了复位名称和来源。

Table 6.1 重置名称和来源

重设名称	Source
RES引脚复位	输入到RES引脚的电压被驱动为低电平
Power-on reset	VCC上升（电压检测VPOR）*1
VBATT选择电压上电复位	VCC下降(电压检测VDETBATT)*1
独立看门狗定时器复位	IWDT下溢或刷新错误
看门狗定时器复位	WDT下溢或刷新错误
电压监控器0复位	VCC下降（电压检测Vdet0）*1
电压监视器1复位	VCC下降（电压检测Vdet1）*1
SRAM奇偶校验错误复位	SRAM奇偶校验错误检测
SRAMECC错误复位	SRAMECC错误检测
总线主控MPU错误复位	总线主控MPU错误检测
总线从机MPU错误复位	总线从机MPU错误检测
堆栈指针错误复位	堆栈指针错误检测
软件复位	寄存器设置（使用Arm®软件复位位AIRCR.SYSRESETREQ）

Note 1. 有关要监控的电压（VPOR、Vdet0、Vdet1和VDETBATT）的详细信息，请参见第8节，低电压检测(LVD)，第12节，电池备份功能和第48节，电气特性。

内部状态和引脚由复位初始化。表6.2和表6.3列出了由复位初始化的目标。

Table 6.2 由每个复位源初始化的复位检测标志（2个中的1个）

	重置源						
要初始化的标志	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	软件复位
上电复位检测标志(RSTSR0.PORF)	✓	×	×	×	×	×	×

Table 6.2 Reset detect flags initialized by each reset source (2 of 2)

Flags to be initialized	Reset source						
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Software reset
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	×	×	×	×	×
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	×	×	×	×
Watchdog Timer Reset Detect Flag(RSTSR1.WDTRF)	✓	✓	✓	×	×	×	×
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	×	×	×	×
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	×	×	×	×
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	×	×	×	×
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	✓	✓	✓	×	×	×	×
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	✓	✓	✓	×	×	×	×
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	×	×	×	×
Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	✓	✓	✓	×	×	×	×
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	×	✓	×	×	×	×	×

Flags to be initialized	Reset source					
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	VBATT_POR*1
Power-On Reset Detect Flag (RSTSR0.PORF)	×	×	×	×	×	×
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	×	×	×	×	×	×
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	×	×	×	×	×	×
Watchdog Timer Reset Detect Flag(RSTSR1.WDTRF)	×	×	×	×	×	×
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	×	×	×	×	×	×
Software Reset Detect Flag (RSTSR1.SWRF)	×	×	×	×	×	×
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	×	×	×	×	×	×
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	×	×	×	×	×	×
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	×	×	×	×	×	×
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	×	×	×	×	×	×
Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	×	×	×	×	×	×
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	×	×	×	×	×	×

✓: Initialized to 0

×: Not initialized

Note 1. For VBATT_POR details, see section 12, Battery Backup Function.

Table 6.3 Module-related registers initialized by each reset source (1 of 2)

Registers to be initialized		Reset source						
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Software reset
Registers related to the Watchdog Timer	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓	×	×
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	×	×
Register related to the SOSC	SOSCCR	×	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×

Table 6.2 由每个复位源初始化的复位检测标志（2个中的2个）

要初始化的标志	重置源						
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	软件复位
电压监视器0复位检测标志(RSTSR0.LVD0RF)	✓	✓	×	×	×	×	×
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	✓	✓	✓	×	×	×	×
看门狗定时器复位检测Flag(RSTSR1.WDTRF)	✓	✓	✓	×	×	×	×
电压监视器1复位检测标志(RSTSR0.LVD1RF)	✓	✓	✓	×	×	×	×
软件复位检测标志(RSTSR1.SWRF)	✓	✓	✓	×	×	×	×
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	✓	✓	✓	×	×	×	×
SRAMECC错误复位检测标志(RSTSR1.REERF)	✓	✓	✓	×	×	×	×
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	✓	✓	✓	×	×	×	×
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	✓	✓	✓	×	×	×	×
堆栈指针错误复位检测标志(RSTSR1.SPERF)	✓	✓	✓	×	×	×	×
冷启动热启动确定标志(RSTSR2.CWSF)	×	✓	×	×	×	×	×

要初始化的标志	重置源					
	SRAM奇偶校验错误复位	SRAMECC错误复位	总线主控MPU错误复位	总线从机MPU错误复位	堆栈指针错误复位	VBATT_POR*1
上电复位检测标志(RSTSR0.PORF)	×	×	×	×	×	×
电压监视器0复位检测标志(RSTSR0.LVD0RF)	×	×	×	×	×	×
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	×	×	×	×	×	×
看门狗定时器复位检测Flag(RSTSR1.WDTRF)	×	×	×	×	×	×
电压监视器1复位检测标志(RSTSR0.LVD1RF)	×	×	×	×	×	×
软件复位检测标志(RSTSR1.SWRF)	×	×	×	×	×	×
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	×	×	×	×	×	×
SRAMECC错误复位检测标志(RSTSR1.REERF)	×	×	×	×	×	×
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	×	×	×	×	×	×
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	×	×	×	×	×	×
堆栈指针错误复位检测标志(RSTSR1.SPERF)	×	×	×	×	×	×
冷启动热启动确定标志(RSTSR2.CWSF)	×	×	×	×	×	×

：初始化为0×：
未初始化注1。

有关VBATT_POR的详细信息，请参见第12节，电池备份功能。

Table 6.3 由每个复位源初始化的模块相关寄存器（2个中的1个）

待初始化的寄存器		重置源						
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	软件复位
相关的寄存器 看门狗定时器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
与电压监控功能相关的寄存器1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓	×	×
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	×	×
SOSC相关的注册	SOSCCR	×	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×

Table 6.3 Module-related registers initialized by each reset source (2 of 2)

Registers to be initialized		Reset source						
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Software reset
Register related to the LOCO	LOCOCR	×	×	×	×	×	×	×
	LOCOUTCR	×	×	×	×	×	×	×
Register related to the MOSC	MOMCR	✓	✓	✓	✓	✓	✓	✓
Register related to the realtime clock*2		×	×	×	×	×	×	×
Register related to the AGT		×	✓	✓	×	×	✓	×
Register related to the MPU		✓	✓	✓	✓	✓	✓	✓
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓	✓
Pin state (XCIN/XCOUT pin)		×	×	×	×	×	×	×
Battery backup	VBTCR1	×	✓	×	×	×	×	×
	VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTICTLR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR	×	×	×	×	×	×	×
	VBTBKRn(n = 0 to 511)	×	×	×	×	×	×	×
Registers other than the above, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓

Registers to be initialized		Reset source					
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	VBATT_POR*3
Registers related to the Watchdog Timer	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	×
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	×	×	×	×	×	×
	LVD1CR1/LVD1SR	×	×	×	×	×	×
Register related to the SOSC	SOSCCR	×	×	×	×	×	✓*1
	SOMCR	×	×	×	×	×	✓
Register related to the LOCO	LOCOCR	×	×	×	×	×	✓
	LOCOUTCR	×	×	×	×	×	✓
Register related to the MOSC	MOMCR	✓	✓	✓	✓	✓	×
Register related to the realtime clock*2		×	×	×	×	×	×
Register related to the AGT		×	×	×	×	×	×
Register related to the MPU		✓	✓	×	×	×	×
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	×
Pin state (XCIN/XCOUT pin)		×	×	×	×	×	✓
Battery backup	VBTCR1	×	×	×	×	×	×
	VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTICTLR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR	×	×	×	×	×	✓
	VBTBKRn(n = 0 to 511)	×	×	×	×	×	×
Registers other than the above, CPU, and internal state		✓	✓	✓	✓	✓	×

✓: Initialized

×: Not initialized

Note 1. For the initial value of each register, see section 9, Clock Generation Circuit.

Note 2. The RTC has a software reset. RCR1.RTCOS, RCR1.CIE, RCR2.RTCOE, RCR2.ADJ30, and RCR2.RESET are initialized by all types of resets. For details on the target bits, see section 25, Realtime Clock (RTC).

Note 3. For VBATT_POR details, see section 12, Battery Backup Function.

The RTC is not initialized by any reset source. SOSC and LOCO can be selected as the clock sources of RTC and AGT.

Table 6.3 由每个复位源初始化的模块相关寄存器（2个中的2个）

待初始化的寄存器		重置源						
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	软件复位
与LOCO相关的注册	LOCOCR	×	×	×	×	×	×	×
	LOCOUTCR	×	×	×	×	×	×	×
注册相关的MOSC	MOMCR	✓	✓	✓	✓	✓	✓	✓
与实时时钟相关的寄存器*2		×	×	×	×	×	×	×
与AGT相关的注册		×	✓	✓	×	×	✓	×
MPU相关寄存器		✓	✓	✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚）		×	×	×	×	×	×	×
备用电池	VBTCR1	×	✓	×	×	×	×	×
	VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTICTLR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR	×	×	×	×	×	×	×
	VBTBKRn(n = 0 to 511)	×	×	×	×	×	×	×
上述以外的寄存器、CPU、内部状态		✓	✓	✓	✓	✓	✓	✓

待初始化的寄存器		重置源					
		SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	总线从机MPU错误复位	堆栈指针错误复位	VBATT_POR*3
相关的寄存器看门狗定时器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	×
与电压监控功能相关的寄存器1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	×	×	×	×	×	×
	LVD1CR1/LVD1SR	×	×	×	×	×	×
SOSC相关的注册	SOSCCR	×	×	×	×	×	✓*1
	SOMCR	×	×	×	×	×	✓
与LOCO相关的注册	LOCOCR	×	×	×	×	×	✓
	LOCOUTCR	×	×	×	×	×	✓
注册相关的MOSC	MOMCR	✓	✓	✓	✓	✓	×
与实时时钟相关的寄存器*2		×	×	×	×	×	×
与AGT相关的注册		×	×	×	×	×	×
MPU相关寄存器		✓	✓	×	×	×	×
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓	×
引脚状态（XCINXCOUT引脚）		×	×	×	×	×	✓
备用电池	VBTCR1	×	×	×	×	×	×
	VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTICTLR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR	×	×	×	×	×	✓
	VBTBKRn(n = 0 to 511)	×	×	×	×	×	×
上述以外的寄存器、CPU、内部状态		✓	✓	✓	✓	✓	×

：已初始化×：
未初始化注1。

对于每个寄存器的初始值，请参见第9节，时钟生成电路。

Note 2. RTC具有软件复位功能。RCR1.RTCOS、RCR1.CIE、RCR2.RTCOE、RCR2.ADJ30和RCR2.RESET由所有类型的复位初始化。有关目标位的详细信息，请参见第25节，实时时钟(RTC)。

Note 3. 有关VBATT_POR的详细信息，请参见第12节，电池备份功能。

RTC不会被任何复位源初始化。可选择SOSC和LOCO作为RTC和AGT的时钟源。

Table 6.4 and Table 6.5 show the states of SOSC and LOCO when a reset occurs.

Table 6.4 States of SOSC when a reset occurs

		Reset source	
		VBATT_POR	**Other**
SOSC	Enable or disable	Initialized to disable	Continue with the state that was selected before the reset occurred
	Drive capability	Initialized to normal mode	Continue with the state that was selected before the reset occurred
	XCIN/XCOUT	Initialized to general-purpose input pins	Continue with the state that was selected before the reset occurred

Table 6.5 States of LOCO when a reset occurs

		Reset source	
		VBATT_POR	**Other**
LOCO	Enable or disable	Initialized to enable	Continue with the state that was selected before the reset occurred
	Oscillation accuracy	Initialized to accuracy before trimming by LOCOUTCR (accuracy: ±15%)	Continue with the accuracy that was trimmed by LOCOUTCR

When a reset is canceled, reset exception handling starts.

Table 6.6 lists the pin related to the reset function.

Table 6.6 Pin related to reset

Pin name	I/O	Function
RES	Input	Reset pin

6.2 Register Descriptions

6.2.1 Reset Status Register 0 (RSTSR0)

Address(es): SYSTEM.RSTSR0 4001 E410h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LVD1RF	LVD0RF	PORF
Value after reset:	0	0	0	0	x	x*1	x*1	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected 1: Power-on reset detected.	R(/W)*2
b1	LVD0RF	Voltage Monitor 0 Reset Detect Flag	0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected.	R(/W)*2
b2	LVD1RF	Voltage Monitor 1 Reset Detect Flag	0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected.	R(/W)*2
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

表6.4和表6.5显示了复位发生时SOSC和LOCO的状态。

Table 6.4 发生复位时SOSC的状态

		重置源	
		VBATT_POR	**Other**
SOSC	启用或禁用	初始化为禁用	继续使用重置发生之前选择的状态
	驱动能力	初始化为正常模式	继续使用重置发生之前选择的状态
	XCIN/XCOUT	初始化为通用输入引脚	继续使用重置发生之前选择的状态

Table 6.5 发生复位时的LOCO状态

		重置源	
		VBATT_POR	**Other**
LOCO	启用或禁用	初始化为启用	继续使用重置发生之前选择的状态
	振荡精度	通过LOCOUTCR微调前初始化为精度（精度：±15%）	继续使用被修剪的精度 LOCOUTCR

当复位被取消时，复位异常处理开始。

表6.6列出了与复位功能相关的引脚。

Table 6.6 复位相关引脚

引脚名称	I/O	Function
RES	Input	复位引脚

6.2 注册说明

6.2.1 复位状态寄存器0(RSTSR0)

Address(es): SYSTEM.RSTSR0 4001 E410h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LVD1RF	LVD0RF	PORF
重置后的值:	0	0	0	0	x	x*1	x*1	x*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PORF	上电复位检测标志	0：未检测到上电复位1：检测到上电复位。	R(/W)*2
b1	LVD0RF	电压监视器0复位检测标志	0：未检测到电压监控器0复位1：检测到电压监控器0复位。	R(/W)*2
b2	LVD1RF	电压监视器1复位检测标志	0：未检测到电压监控器1复位1：检测到电压监控器1复位。	R(/W)*2
b3	—	Reserved	读取值未定义。写入值应为0。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后的值取决于复位源。
Note 2. 只能写入0来清除标志。该标志必须在读取1后写入0来清除。

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to PORF.

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below Vdet0.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD0RF.

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below Vdet1.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD1RF.

6.2.2 Reset Status Register 1 (RSTSR1)

Address(es): SYSTEM.RSTSR1 4001 E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPERF	BUSMRF	BUSSRF	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	0	0	0	x*1	x*1	x*1	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected.	R(/W) *2
b1	WDTRF	Watchdog Timer Reset Detect Flag	0: Watchdog timer reset not detected 1: Watchdog timer reset detected.	R(/W) *2
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected 1: Software reset detected.	R(/W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	RPERF	SRAM Parity Error Reset Detect Flag	0: SRAM parity error reset not detected 1: SRAM parity error reset detected.	R(/W) *2
b9	REERF	SRAM ECC Error Reset Detect Flag	0: SRAM ECC error reset not detected 1: SRAM ECC error reset detected.	R(/W) *2
b10	BUSSRF	Bus Slave MPU Error Reset Detect Flag	0: Bus slave MPU error reset not detected 1: Bus slave MPU error reset detected.	R(/W) *2

PORF标志（上电复位检测标志）

PORF标志表示发生了上电复位。

[Setting condition]

- 发生上电复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从PORF读取1然后将0写入PORF。

LVD0RF标志（电压监视器0复位检测标志）

LVD0RF标志表示VCC电压低于Vdet0。

[Setting condition]

- 发生电压监视器0复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从LVD0RF读取1然后将0写入LVD0RF。

LVD1RF标志（电压监视器1复位检测标志）

LVD1RF标志表示VCC电压低于Vdet1。

[Setting condition]

- 当电压监视器1发生复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从LVD1RF读取1然后将0写入LVD1RF。

6.2.2 复位状态寄存器1(RSTSR1)

Address(es): SYSTEM.RSTSR1 4001 E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPERF	BUSMRF	BUSSRF	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
重置后的值：	0	0	0	x*1	x*1	x*1	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	IWDTRF	独立看门狗定时器复位检测标志	0：未检测到独立看门狗定时器复位1：检测到独立看门狗定时器复位。	R(/W) *2
b1	WDTRF	看门狗定时器复位检测标志	0：未检测到看门狗定时器复位1：检测到看门狗定时器复位。	R(/W) *2
b2	SWRF	软件复位检测标志	0：未检测到软件复位1：检测到软件复位。	R(/W) *2
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	RPERF	SRAM奇偶校验错误复位检测标志	0：未检测到SRAM奇偶校验错误复位1：检测到SRAM奇偶校验错误复位。	R(/W) *2
b9	REERF	SRAMECC错误复位检测标志	0：未检测到SRAMECC错误复位1：检测到SRAMECC错误复位。	R(/W) *2
b10	BUSSRF	总线从机MPU错误复位检测标志	0：未检测到总线从机MPU错误复位1：检测到总线从机MPU错误复位。	R(/W) *2

Bit	Symbol	Bit name	Description	R/W
b11	BUSMRF	Bus Master MPU Error Reset Detect Flag	0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected.	R(/W) *2
b12	SPERF	SP Error Reset Detect Flag	0: SP error reset not detected 1: SP error reset detected.	R(/W) *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurred.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurred.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurred.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that a SRAM parity error reset occurred.

[Setting condition]

- When a SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to RPERF.

REERF flag (SRAM ECC Error Reset Detect Flag)

The REERF flag indicates that a SRAM ECC error reset occurred.

[Setting condition]

- When a SRAM ECC error reset occurs.

Bit	Symbol	位名称	Description	R/W
b11	BUSMRF	总线主控MPU错误复位检测标志	0：未检测到总线主控MPU错误复位1：检测到总线主控MPU错误复位。	R(/W) *2
b12	SPERF	SP错误复位检测标志	0：未检测到SP错误复位1：检测到SP错误复位。	R(/W) *2
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后的值取决于复位源。
Note 2. 只能写入0来清除标志。该标志必须在读取1后写入0来清除。

IWDTRF标志（独立看门狗定时器复位检测标志）

IWDTRF标志指示发生了独立的看门狗定时器复位。

[Setting condition]

- 当发生独立的看门狗定时器复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从IWDTRF读取1然后将0写入IWDTRF。

WDTRF标志（看门狗定时器复位检测标志）

WDTRF标志表示发生了看门狗定时器复位。

[Setting condition]

- 当发生看门狗定时器复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从WDTRF读取1然后将0写入WDTRF。

SWRF标志（软件复位检测标志）

SWRF标志表明发生了软件复位。

[Setting condition]

- 当发生软件复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从1读取然后0写入SWRF。

RPERF标志（SRAM奇偶校验错误复位检测标志）

RPERF标志表明发生了SRAM奇偶校验错误复位。

[Setting condition]

- 当SRAM奇偶校验错误复位发生时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从RPERF读取1然后将0写入RPERF。

REERF标志（SRAMECC错误复位检测标志）

REERF标志表示发生了SRAMECC错误复位。

[Setting condition]

- 当SRAMECC错误复位发生时。

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to REERF.

BUSSRF flag (Bus Slave MPU Error Reset Detect Flag)

The BUSSRF flag indicates that a bus slave MPU error reset occurred.

[Setting condition]

- When a bus slave MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to BUSSRF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurred.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to BUSMRF.

SPERF flag (SP Error Reset Detect Flag)

The SPERF flag indicates that a stack pointer error reset occurred.

[Setting condition]

- When a stack pointer error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to SPERF.

6.2.3 Reset Status Register 2 (RSTSR2)

Address(es): SYSTEM.RSTSR2 4001 E411h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start.	R(/W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从REERF读取1然后将0写入REERF。

BUSSRF标志（总线从机MPU错误复位检测标志）

BUSSRF标志表示发生了总线从机MPU错误复位。

[Setting condition]

- 当发生总线从机MPU错误复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从1被读取然后0被写入BUSSRF。

BUSMRF标志（总线主控MPU错误复位检测标志）

BUSMRF标志指示发生了总线主控MPU错误复位。

[Setting condition]

- 当发生总线主控MPU错误复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 读取1，然后将0写入BUSMRF。

SPERF标志（SP错误复位检测标志）

SPERF标志表明发生了堆栈指针错误复位。

[Setting condition]

- 发生堆栈指针错误复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从SPERF读取1然后将0写入SPERF。

6.2.3 复位状态寄存器2(RSTSR2)

Address(es): SYSTEM.RSTSR2 4001 E411h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
重置后的值：	0	0	0	0	0	0	0	x*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	CWSF	冷暖启动确定标志	0：冷启动1： 热启动。	R(/W) *2
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后的值取决于复位源。
Note 2. 只能写入1来设置标志。

RSTSR2判断是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in Table 6.2 occurs.

6.3 Operation

6.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 48, Electrical Characteristics.

6.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. If the RES pin is in a high level state when power is supplied, a power-on reset is generated. After VCC exceeds VPOR and the specified power-on reset time elapses, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is a stabilization period for the external power supply and the MCU circuit. After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset.

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below Vdet0, the RSTSR0.LVD0RF flag is set to 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used.

After VCC exceeds Vdet0 and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling. The Vdet0 voltage detection level can be changed by the setting in the VDSEL1[2:0] bits in Option Function Select Register 1 (OFS1).

Figure 6.1 shows example of operations during a power-on reset and voltage monitor 0 reset.

CWSF标志（冷暖启动确定标志）

CWSF标志指示复位处理的类型，冷启动或热启动。CWSF标志由上电复位初始化。它不会被RES引脚产生的复位信号初始化。

[Setting condition]

- 当1由软件写入时。将0写入CWSF不会将其设置为0。

[Clearing condition]

- 发生表6.2中列出的复位时。

6.3 Operation

6.3.1 RES引脚复位

RES引脚产生此复位。当RES引脚被驱动为低电平时，所有正在进行的处理都被中止，MCU进入复位状态。要成功复位MCU，RES引脚必须在上电时指定的电源稳定时间内保持低电平。

当RES引脚从低电平驱动为高电平时，内部复位会在RES取消后等待时间(tRESWT)过去后取消。CPU然后开始复位异常处理。

有关详细信息，请参见第48节，电气特性。

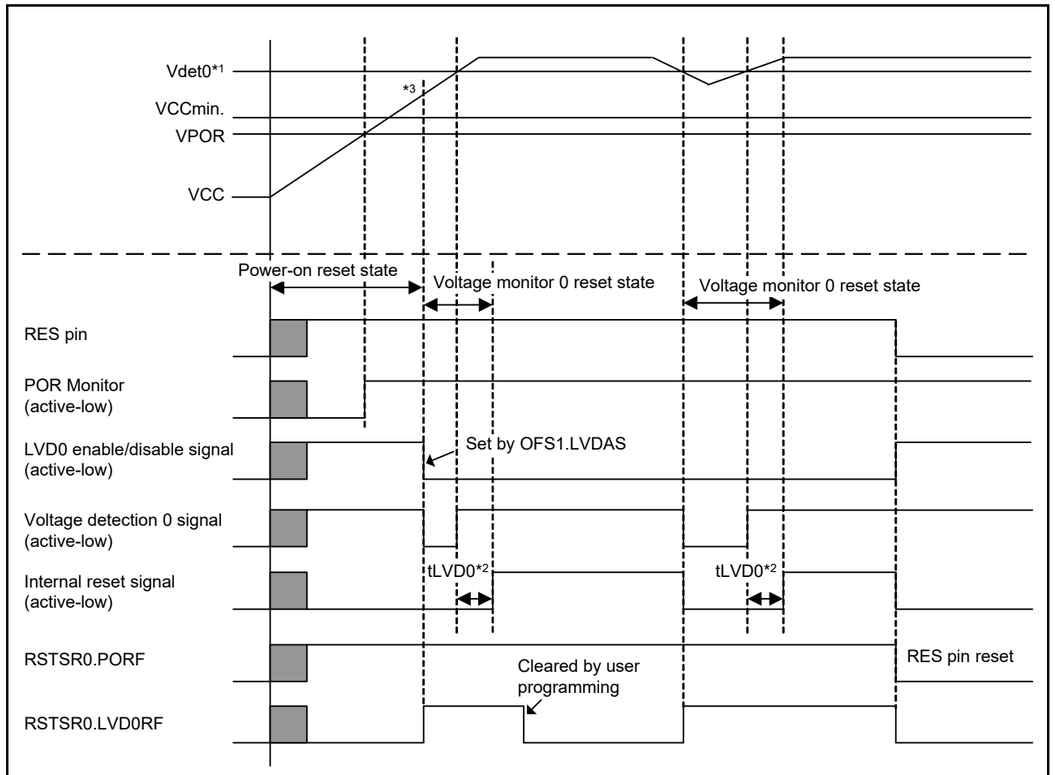
6.3.2 Power-On Reset

上电复位（POR）是由上电复位电路产生的内部复位。如果在供电时RES引脚处于高电平状态，则会产生上电复位。VCC超过VPOR并经过规定的上电复位时间后，内部复位被取消，CPU开始复位异常处理。上电复位时间是外部电源和MCU电路的稳定期。上电复位产生后，RSTSR0中的PORF标志设置为1。PORF标志由RES引脚复位初始化。

电压监控器0复位是由电压监控器电路产生的内部复位。如果选项功能选择寄存器1(OFS1)中的电压检测0电路启动(LVDAS)位为0（复位后使能电压监视器0复位）并且VCC低于Vdet0，则RSTSR0.LVD0RF标志设置为1，并且电压检测电路产生电压监视器0复位。如果要使用电压监视器0复位，则将OFS1.LVDAS位清零。

在VCC超过Vdet0并且电压监视器0复位时间(tLVD0)过去后，内部复位被取消，并且CPU启动复位异常处理。Vdet0电压检测电平可以通过在选项功能选择寄存器1(OFS1)中的VDSEL1[2:0]位。

图6.1显示了上电复位和电压监视器0复位期间的操作示例。



Note: For details on the electrical characteristics, see section 48, Electrical Characteristics.
Note 1. Vdet0 shows a voltage monitor 0 reset detection level, VPOR shows a power-on reset detection level, and VCCmin shows the minimum guaranteed voltage of MCU.
Note 2. tLVD0 shows a time for voltage monitor 0 reset.
Note 3. At power-on, VCC should have risen to the minimum guaranteed voltage before the POR reset is released.

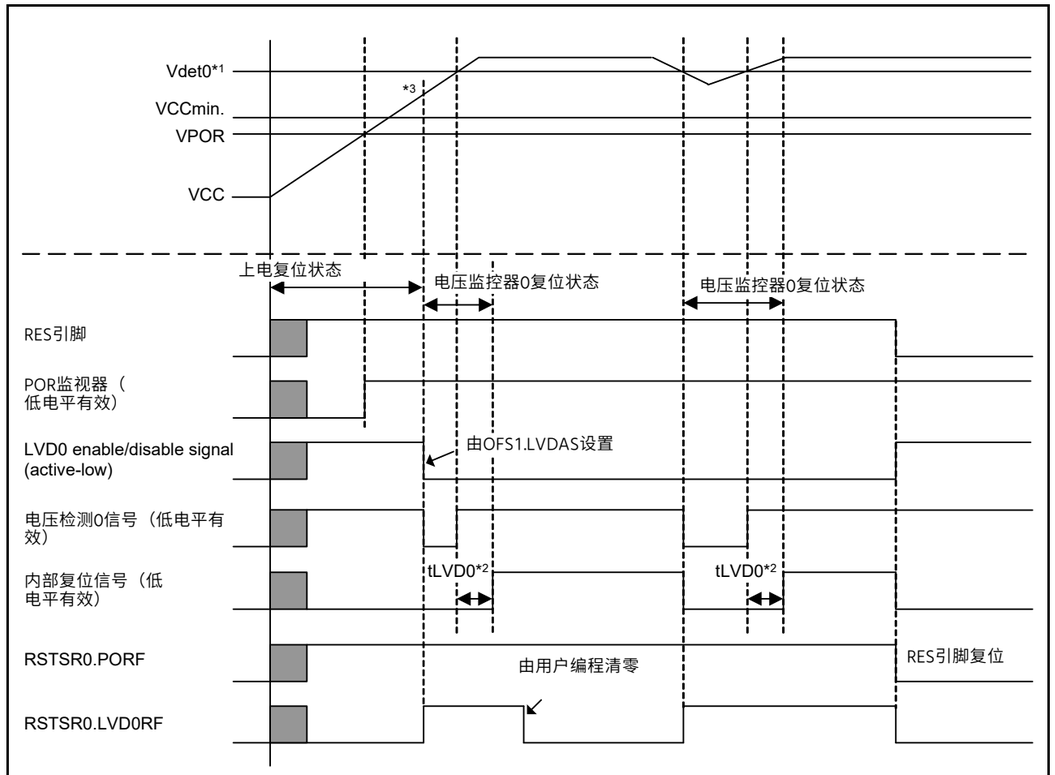
Figure 6.1 Example of operations during power-on and voltage monitor 0 resets

6.3.3 Voltage Monitor Reset

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in Option Function Select register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below Vdet0, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates a voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds Vdet0 and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (LVD1CR0.RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in the Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below Vdet1.

Similarly, timing for release from the voltage monitor 1 reset state is selectable in the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0. When the LVD1CR0.RN bit is 0 and VCC falls to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses after VCC rises above Vdet1. When the LVD1CR0.RN bit is 1 and VCC falls to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses.



Note: 有关电气特性的详细信息，请参见第48节，电气特性。
Note 1. Vdet0表示电压监视器0复位检测电平，VPOR表示上电复位检测电平，VCCmin表示MCU的最低保证电压。
Note 2. tLVD0显示电压监视器0复位的时间。
Note 3. 上电时，VCC应该在POR复位释放之前上升到最低保证电压。

Figure 6.1 上电和电压监控0复位期间的操作示例

6.3.3 电压监视器复位

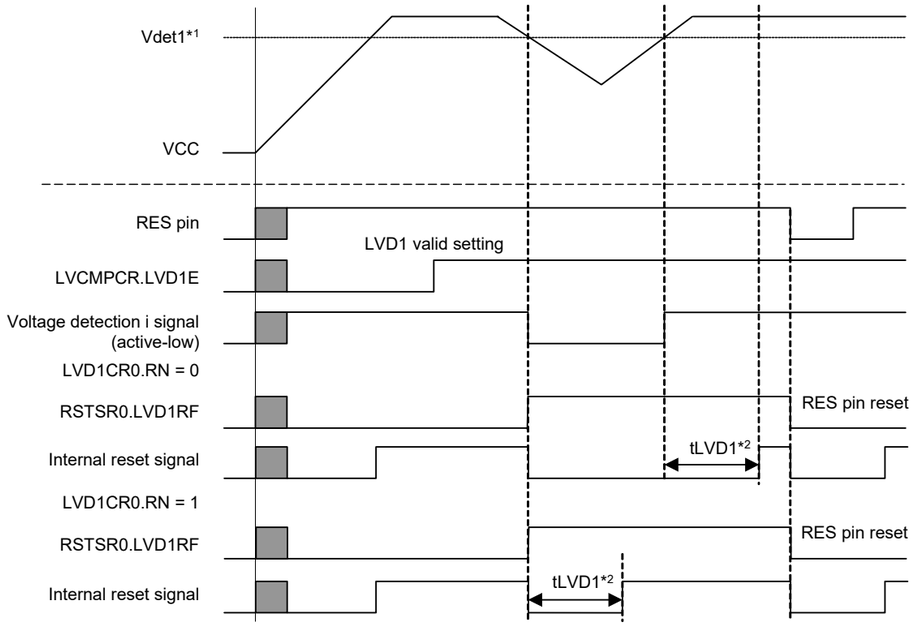
电压监控器0复位是由电压监控器电路产生的内部复位。如果电压检测0选项功能选择寄存器1(OFS1)中的电路启动(LVDAS)位为0（复位后使能电压监视器0复位）且VCC低于Vdet0，RSTSR0.LVD0RF标志变为1，电压检测电路生成电压监视器0复位。如果要使用电压监视器0复位，则将OFS1.LVDAS位清零。在VCC超过Vdet0并且电压监视器0复位时间(tLVD0)过去后，内部复位被取消，CPU开始复位异常处理。

当电压监控器1中断复位允许位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监控器1电路模式选择位(LVD1CR0.RI)设置为1（选择电压监控器1电路控制寄存器0(LVD1CR0)中的低电压检测产生复位），RSTSR0.LVD1RF标志设置为1，如果VCC下降到电压检测电路产生电压监控器1复位或低于Vdet1。

类似地，从电压监视器1复位状态释放的时序可在LVD1CR0的电压监视器1复位否定选择位(RN)中选择。当LVD1CR0.RN位为0且VCC下降到或低于Vdet1时，CPU会从内部复位状态中释放并在VCC上升到Vdet1以上后经过LVD1复位时间(tLVD1)时开始复位异常处理。当LVD1CR0.RN位为1且VCC降至或低于Vdet1时，CPU会从内部复位状态中释放，并在LVD1复位时间(tLVD1)过去后开始复位异常处理。

Detection level Vdet1 can be changed in the Voltage Detection Level Select Register (LVDLVLR).

Figure 6.2 shows example of operations during voltage monitor 1 reset. For details on the voltage monitor 1 reset, see section 8, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 48, Electrical Characteristics.
Note 1. Vdet1 indicates the detection level of voltage monitor 1 reset
Note 2. tLVD1 indicates the time for voltage monitor 1 reset

Figure 6.2 Example of operation during voltage monitor 1 reset

6.3.4 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 27, Independent Watchdog Timer (IWDT).

6.3.5 Watchdog Timer Reset

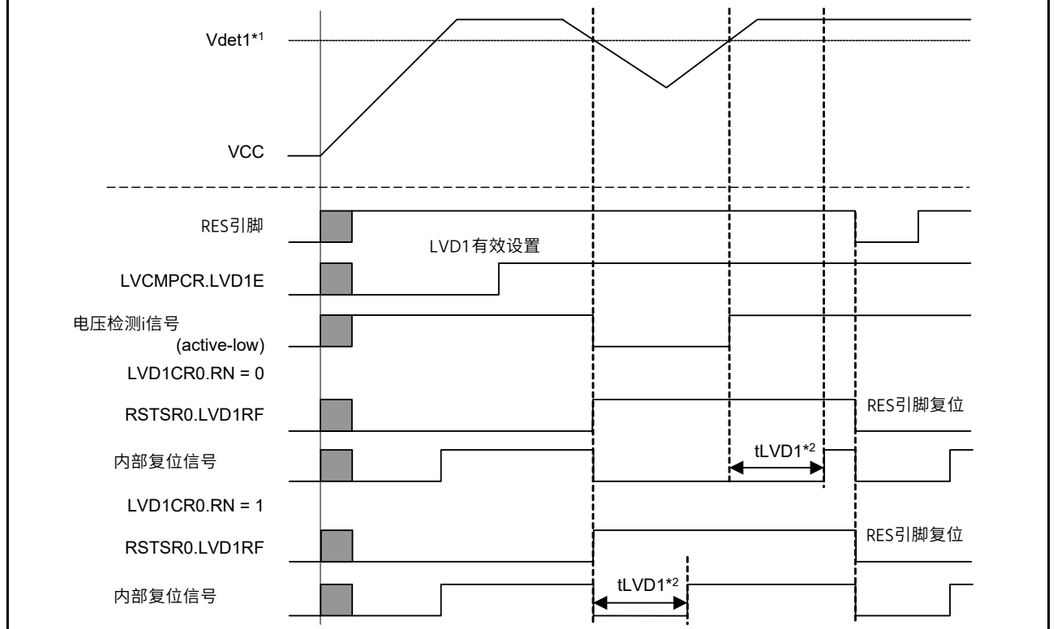
The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select Register 0 (OFS0).

When output of the watchdog timer reset is selected, the reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 26, Watchdog Timer (WDT).

检测电平Vdet1可以在电压检测电平选择寄存器(LVDLVLR)中更改。

图6.2显示了电压监视器1复位期间的操作示例。有关电压监视器1复位的详细信息，请参阅第8节，低电压检测(LVD)。



Note: 有关电气特性的详细信息，请参见第48节，电气特性。
Note 1. Vdet1表示电压监视器1复位的检测电平
Note 2. tLVD1表示电压监视器1复位的时间

Figure 6.2 电压监视器1复位时的动作示例

6.3.4 独立看门狗定时器复位

独立看门狗定时器复位是由独立看门狗定时器（IWDT）产生的内部复位。
可以在选项功能选择寄存器0(OFS0)中选择IWDT的复位输出。

Whenoutputoftheindependentwatchdogtimerresetisselected theresetisgeneratediftheIWDTunderflows orifdataiswrittenwhenrefreshoperationisdisabled.当独立看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关独立看门狗定时器复位的详细信息，请参见第27节，独立看门狗定时器(IWDT)。

6.3.5 看门狗定时器复位

看门狗定时器复位是由看门狗定时器(WDT)产生的内部复位。从复位输出
可以在WDT复位控制寄存器(WDTRCR)或选项功能选择寄存器0(OFS0)中选择WDT。

选择看门狗定时器复位的输出时，如果WDT下溢，或者在禁止刷新操作时写入数据，则产生复位。当看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关看门狗定时器复位的详细信息，请参见第26节，看门狗定时器(WDT)。

6.3.6 Software Reset

The software reset is an internal reset generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (tRESW2) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M4 Technical Reference Manual*.

6.3.7 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. The flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start). Otherwise, the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 6.3 shows an example of a cold/warm start determination operation.

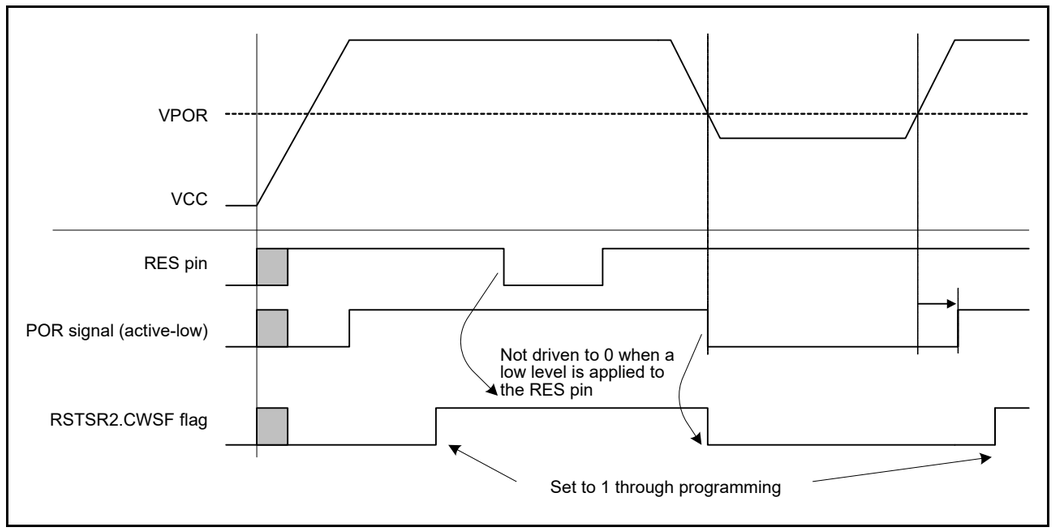


Figure 6.3 Example of a cold/warm start determination operation

6.3.8 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling. Figure 6.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after it is read as 1.

6.3.6 软件复位

软件复位是通过软件设置Arm内核的AIRCR寄存器中的SYSRESETREQ位产生的内部复位。当SYSRESETREQ位设置为1时，会产生软件复位。当软件复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关SYSRESETREQ位的详细信息，请参阅ARM®Cortex®-M4技术参考手册。

6.3.7 冷暖启动的测定

读取RSTSR2中的CWSF标志以确定复位处理的原因。该标志指示是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

发生上电复位（冷启动）时，CWSF标志设置为0。否则，该标志不设置为0。当通过软件向其写入1时，该标志设置为1。即使向其写入0，它也不会设置为0。

图6.3显示了冷暖启动确定操作的示例。

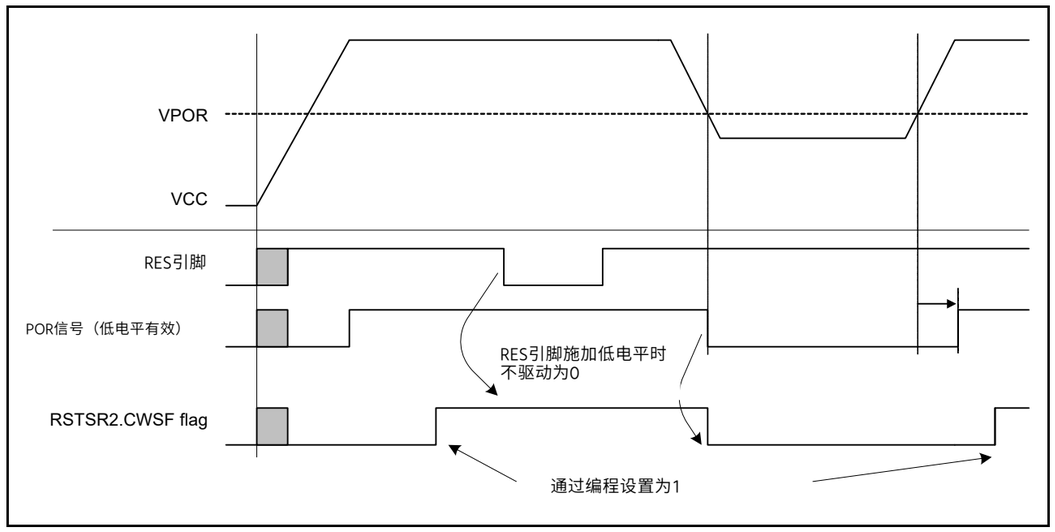
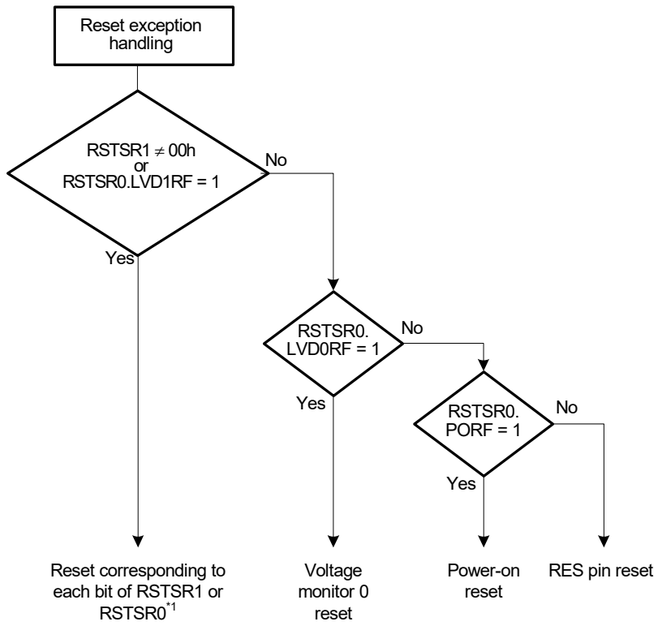


Figure 6.3 冷暖启动判定动作示例

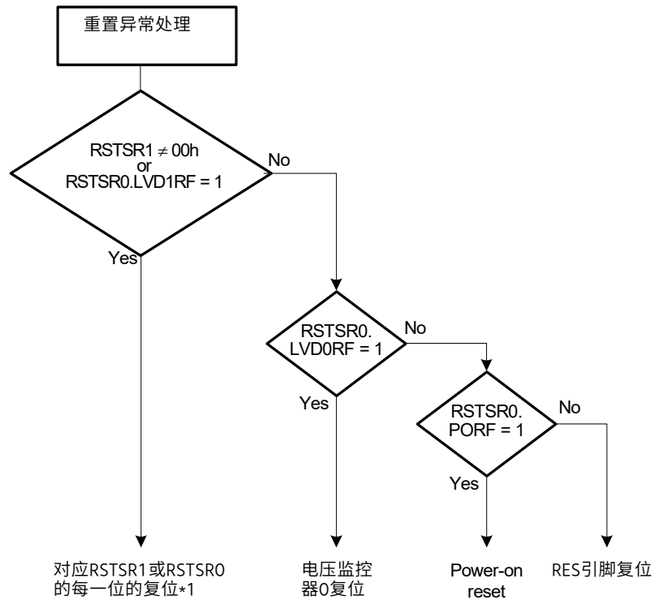
6.3.8 复位产生源的确定

读取RSTSR0和RSTSR1以确定哪个复位执行复位异常处理。图6.4显示了识别复位产生源的流程示例。复位标志读为1后必须写为0。



Note 1. If a reset associated with each bit of RSTSR1 or RSTSR0.LVD1RF occurs at the same time, all reset flags are set to 1.

Figure 6.4 Example of reset generation source determination flow



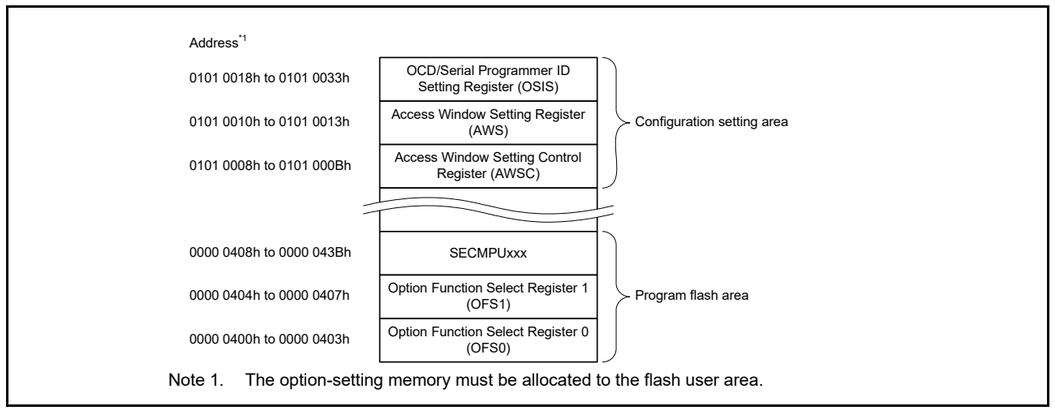
Note 1. 如果与RSTSR1或RSTSR0.LVD1RF的每一位相关的复位同时发生，则所有复位标志都设置为1。

Figure 6.4 复位产生源确定流程示例

7. Option-Setting Memory

7.1 Overview

The option-setting memory determines the state of the MCU after a reset. The option-setting memory is allocated to the configuration setting area and the program flash area of the flash memory, and the available methods of setting are different for the two areas. Figure 7.1 shows the option-setting memory area.



Note 1. The option-setting memory must be allocated to the flash user area.

Figure 7.1 Option-setting memory area

7.2 Register Descriptions

7.2.1 Option Function Select Register 0 (OFS0)

Address(es): OFS0 0000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:	The value set by the user*1															

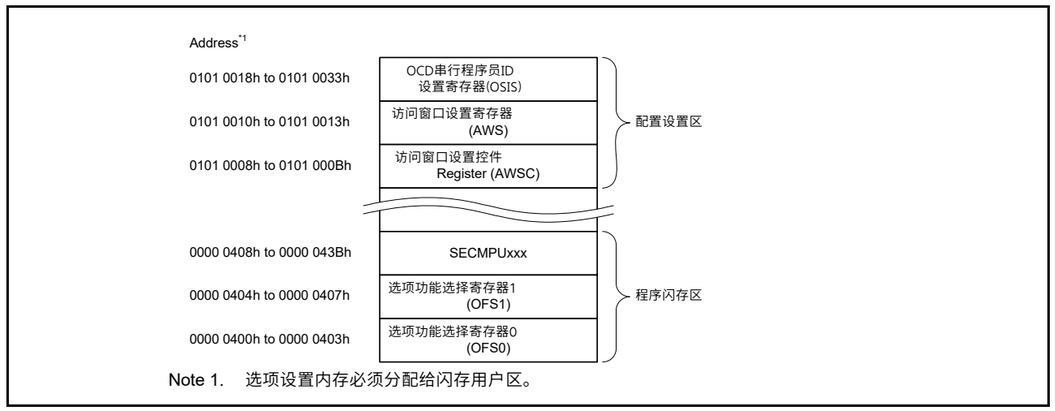
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT.	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Selects	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh).	R

7. Option-Setting Memory

7.1 Overview

选项设置存储器确定复位后MCU的状态。选项设置存储器被分配到闪存的配置设置区和程序闪存区，两个区域的可用设置方法不同。图7.1显示了选项设置存储区。



Note 1. 选项设置内存必须分配给闪存用户区。

Figure 7.1 选项设置存储区

7.2 注册说明

7.2.1 选项功能选择寄存器0(OFS0)

Address(es): OFS0 0000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
重置后的值:	用户设置的值*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
重置后的值:	用户设置的值*1															

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	读取时，该位返回写入的值。写入值应为1。	R
b1	IWDTSTRT	IWDT启动模式选择	0：复位后自动激活IWDT（自动启动模式）1：禁用IWDT。	R
b3, b2	IWDTTOPS[1:0]	IWDT超时周期选择	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh).	R

Bit	Symbol	Bit name	Description	R/W
b7 to b4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: × 1 0 0 1 0: × 1/16 0 0 1 1: × 1/32 0 1 0 0: × 1/64 1 1 1 1: × 1/128 0 1 0 1: × 1/256. Other settings are prohibited.	R
b9, b8	IWDTRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting).	R
b11, b10	IWDTRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting).	R
b12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select	0: Enable non-maskable interrupt request or interrupt request 1: Enable reset.	R
b13	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b14	IWDTSTPCTL	IWDT Stop Control	0: Continue counting 1: Stop counting when in Sleep mode, Snooze mode, or Software Standby mode.	R
b16, b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b17	WDTSTRT	WDT Start Mode Select	0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode).	R
b19, b18	WDTTOPS[1:0]	WDT Timeout Period Select	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R
b23 to b20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	b23 b20 0 0 0 1: PCLKB divided by 4 0 1 0 0: PCLKB divided by 64 1 1 1 1: PCLKB divided by 128 0 1 1 0: PCLKB divided by 512 0 1 1 1: PCLKB divided by 2048 1 0 0 0: PCLKB divided by 8192. Other settings are prohibited.	R
b25, b24	WDTRPES[1:0]	WDT Window End Position Select	b25 b24 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting).	R
b27, b26	WDTRPSS[1:0]	WDT Window Start Position Select	b27 b26 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting).	R
b28	WDTRSTIRQS	WDT Reset Interrupt Request Select	WDT Behavior Select: 0: NMI 1: Reset.	R
b29	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b30	WDTSTPCTL	WDT Stop Control	0: Continue counting 1: Stop counting when entering Sleep mode.	R
b31	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R

Bit	Symbol	位名称	Description	R/W
b7 to b4	IWDTCKS[3:0]	IWDT-Dedicated Clock 分频比 Select	b7b40000：×10010：×116 0011：×1320100：×16411 11：×11280101：×1256。 禁止其他设置。	R
b9, b8	IWDTRPES[1:0]	IWDT窗口结束位置 Select	b9b800：75%01：50%10：25%11：0%（无窗口结束位置设置）。	R
b11, b10	IWDTRPSS[1:0]	IWDT窗口起始位置 Select	b11b1000：25%01：50%10：75%11：100%（无窗口起始位置设置）。	R
b12	IWDTRSTIRQS	IWDT复位中断 请求选择	0：使能不可屏蔽中断请求或中断请求1：使能复位。	R
b13	—	Reserved	读取时，该位返回写入的值。写入值应为1。	R
b14	IWDTSTPCTL	IWDT停止控制	0：继续计数1：在休眠模式、贪睡模式或软件待机模式下停止计数。	R
b16, b15	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b17	WDTSTRT	WDT启动模式选择	0：复位后自动激活WDT（自动启动模式）1：复位后停止WDT（寄存器启动模式）。	R
b19, b18	WDTTOPS[1:0]	WDT超时周期选择	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R
b23 to b20	WDTCKS[3:0]	WDT时钟频率 分频比选择	b23b200001：PCLKB除以40100：PCLKB除以641111：PCLKB除以1280110：PCLKB除以5120111：PCLKB除以20481000：PCLKB除以8192。禁止其他设置。	R
b25, b24	WDTRPES[1:0]	WDT窗口结束位置 Select	b25b2400：75%01：50%10：25%11：0%（无窗口结束位置设置）。	R
b27, b26	WDTRPSS[1:0]	WDT窗口起始位置 Select	b27b2600：25%01：50%10：75%11：100%（无窗口起始位置设置）。	R
b28	WDTRSTIRQS	WDT复位中断请求 Select	WDT行为选择：0：NMI1：复位。	R
b29	—	Reserved	读取时，该位返回写入的值。写入值应为1。	R
b30	WDTSTPCTL	WDT停止控制	0：继续计数1：进入休眠模式时停止计数。	R
b31	—	Reserved	读取时，该位返回写入的值。写入值应为1。	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Selects)

The IWDTTOPS[1:0] bits select the timeout period, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the IWDT takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 27, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, or 1/256. Using this setting combined with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 128 to 524,288 IWDT clock cycles.

For details, see section 27, Independent Watchdog Timer (IWDT).

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting of the IWDTTOPS[1:0] bits.

For details, see section 27, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible. However, refresh is not possible outside this period.

For details, see section 27, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to an independent watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 27, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep mode, Snooze mode, or Software Standby mode.

For details, see section 27, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto start mode). When WDT is activated in auto start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, the time it takes for the down counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that the counter takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

Note 1. 空白产品中的值为FFFFFFFFh。它设置为您的应用程序写入的值。

IWDTSTRT位（IWDT启动模式选择）

IWDTSTRT位选择复位后激活IWDT的模式（停止状态或激活状态）。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位选择超时周期，即递减计数器下溢所需的时间，如IWDTCKS[3:0]位中设置的分频时钟的128、512、1024或2048个周期.刷新操作后IWDT下溢的时钟周期数由IWDTCKS[3:0]和

IWDTTOPS[1:0] bits.

有关详细信息，请参见第27节，独立看门狗定时器(IWDT)。

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于将IWDT的时钟频率分频为11、116、132、164、1128或1256的预分频器的分频比。将此设置与IWDTTOPS[1:0]位设置，IWDT计数周期可以设置为128到524 288个IWDT时钟周期。

有关详细信息，请参见第27节，独立看门狗定时器(IWDT)。

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值。否则，只有窗口起始位置的值有效。

与IWDTRPSS[1:0]中窗口的开始和结束位置的设置相关的计数器值和
IWDTRPES[1:0]位随IWDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第27节，独立看门狗定时器(IWDT)。

IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始和结束位置之间的间隔成为可以刷新的时间段。

但是，在此期间之外无法刷新。

有关详细信息，请参见第27节，独立看门狗定时器(IWDT)。

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择独立看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第27节，独立看门狗定时器(IWDT)。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位指定在进入休眠模式、贪睡模式或软件时是否停止计数
待机模式。

有关详细信息，请参见第27节，独立看门狗定时器(IWDT)。

WDTSTRT位（WDT启动模式选择）

WDTSTRT位选择WDT在复位后激活的模式（停止状态或在自动启动模式下激活）。当WDT在自动启动模式下激活时，WDT的OFS0寄存器设置有效。

WDTOPS[1:0]位（WDT超时周期选择）

WDTTOPS[1:0]位指定超时周期，即递减计数器下溢所需的时间，如WDTCKS[3:0]位中设置的分频时钟的1024、4096、8192或16384个周期.刷新操作后计数器下溢的PCLKB周期数由WDTCKS[3:0]和WDTTOPS[1:0]位的组合决定。

For details, see section 26, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler to divide the frequency of PCLKB as 1/4, 1/64, 1/128, 1/512, 1/2048, or 1/8192. Using this setting combined with the WDTTOPS[1:0] bit setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 26, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window, in the WDTRPSS[1:0] and WDTRPES[1:0] bits, vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 26, Watchdog Timer (WDT).

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible. However, refresh is not possible outside this period.

For details, see section 26, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to a watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 26, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode.

For details, see section 26, Watchdog Timer (WDT).

7.2.2 Option Function Select Register 1 (OFS1)

Address(es): OFS1 0000 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	HOCOFRQ1[2:0]			—	—	—	HOCO EN	—	—	VDSEL1[2:0]			LVDAS	—	—
	The value set by the user*1															

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset.	R

有关详细信息，请参见第26节，看门狗定时器(WDT)。

WDTCKS[3:0]位（WDT时钟分频比选择）

WDTCKS[3:0]位指定预分频器的分频比，以将PCLKB的频率分频为14、164、1128、1512、12048或18192。将此设置与WDTTOPS[1:0]位设置，WDT计数周期可设置为4096到134217728个PCLKB周期。

有关详细信息，请参见第26节，看门狗定时器(WDT)。

WDTRPES[1:0]位（WDT窗口结束位置选择）

WDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值。否则，只有窗口起始位置的值有效。

与窗口的开始和结束位置的设置相关的计数器值，在WDTRPSS[1:0]和WDTRPES[1:0]位，随WDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第26节，看门狗定时器(WDT)。

WDTRPSS[1:0]位（WDT窗口起始位置选择）

WDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始和结束位置之间的间隔成为可以刷新的时间段。但是，在此期间之外无法刷新。

有关详细信息，请参见第26节，看门狗定时器(WDT)。

WDTRSTIRQS位（WDT复位中断请求选择）

WDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第26节，看门狗定时器(WDT)。

WDTSTPCTL位（WDT停止控制）

WDTSTPCTL位指定进入休眠模式时是否停止计数。

有关详细信息，请参见第26节，看门狗定时器(WDT)。

7.2.2 选项功能选择寄存器1(OFS1)

Address(es): OFS1 0000 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	用户设置的值*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	—	HOCOFRQ1[2:0]			—	—	—	HOCO EN	—	—	VDSEL1[2:0]			LVDAS	—	—
	用户设置的值*1															

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b2	LVDAS	电压检测0电路 Start	0：启用电压监控器0复位后复位1：禁用电压监控器0复位后复位。	R

Bit	Symbol	Bit name	Description	R/W
b5 to b3	VDSEL1[2:0]	Voltage Detection 0 Level Select	b5 b3 0 0 0: Settings prohibited 0 0 1: Selects 2.82 V 0 1 0: Selects 2.51 V 0 1 1: Selects 1.90 V Other settings are prohibited.	
b7, b6	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b8	HOCOEN	HOCO Oscillation Enable	0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset.	R
b11 to b9	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b14 to b12	HOCOFRQ1[2:0]	HOCO Frequency Setting 1	b14 b12 0 0 0: 24 MHz 0 1 0: 32 MHz 1 0 0: 48 MHz 1 0 1: 64 MHz. Other settings are prohibited.	R
b31 to b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in the blank product is FFFF FFFFh. It is set to the value written by your application.

LVDAS bit (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

VDSEL1[2:0] bits (Voltage Detection 0 Level Select)

The VDSEL1[2:0] bits select the voltage detection level of the voltage detection 0 circuit.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ1 bit to an optimum value.

After a reset release, operation is in the low-voltage mode, and therefore HOCOCR.HCSTP must be set immediately to 0.

HOCOFRQ1[2:0] bits (HOCO Frequency Setting 1)

The HOCOFRQ1[2:0] bits select the HOCO frequency after a reset as 24, 32, 48, or 64 MHz.

7.2.3 MPU Registers

Table 7.1 shows the registers related to the MPU function. For details, see section 16, Memory Protection Unit (MPU).

The security MPU is disabled on erasure of flash memory. If improper data is written to the MPU register, the MCU might fail to operate. See section 16, Memory Protection Unit (MPU) to set the proper data.

Table 7.1 MPU registers (1 of 2)

Register name	Symbol	Function	Address	Size (byte)
Security MPU Program Counter Start Address Register 0	SECMPU PCS0	Specifies the security fetch region of flash or SRAM	0000 0408h	4
Security MPU Program Counter End Address Register 0	SECMPU PCE0	Specifies the security fetch region of flash or SRAM	0000 040Ch	4

Bit	Symbol	位名称	Description	R/W
b5 to b3	VDSEL1[2:0]	电压检测0电平 Select	b5b3000：禁止设置001：选择2.82V010：选择2.51V011：选择1.90V禁止其他设置。	
b7, b6	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b8	HOCOEN	HOCO振荡使能	0：复位后启用HOCO振荡1：复位后禁用HOCO振荡。	R
b11 to b9	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b14 to b12	HOCOFRQ1[2:0]	HOCO频率设定1	b14b12000：24MHz010：32MHz100：48MHz101：64MHz。禁止其他设置。	R
b31 to b15	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

Note 1. 空白产品中的值为FFFFFFFFh。它设置为您的应用程序写入的值。

LVDAS位（电压检测0电路启动）

LVDAS位选择在复位后是启用还是禁用电压监视器0复位。

VDSEL1[2:0]位（电压检测0电平选择）

VDSEL1[2:0]位选择电压检测0电路的电压检测电平。

HOCOEN位（HOCO振荡使能）

HOCOEN位选择在复位后是启用还是禁用HOCO振荡。将此位设置为0允许在CPU开始操作之前启动HOCO振荡，从而减少振荡稳定的等待时间。

Note: 当HOCOEN位设置为0时，系统时钟源不切换到HOCO。系统时钟源只能通过设置时钟源选择位(SCKSCR.CKSEL[2:0])切换到HOCO。要使用HOCO时钟，您必须将OFS1.HOCOFRQ1位设置为最佳值。

复位释放后，操作处于低电压模式，因此HOCOCR.HCSTP必须立即设置为0。

HOCOFRQ1[2:0]位（HOCO频率设置1）

HOCOFRQ1[2:0]位选择复位后的HOCO频率为24、32、48或64MHz。

7.2.3 MPU Registers

表7.1显示了与MPU功能相关的寄存器。有关详细信息，请参阅第16节，内存保护单元(MPU)。

擦除闪存时禁用安全MPU。如果不正确的数据写入MPU寄存器，MCU可能无法运行。请参阅第16节，内存保护单元(MPU)以设置正确的数据。

Table 7.1 MPU寄存器(1of2)

注册名称	Symbol	Function	Address	Size (byte)
安全MPU程序计数器启动地址寄存器0	SECMPU PCS0	指定闪存的安全提取区域或SRAM	0000 0408h	4
安全MPU程序计数器结束地址寄存器0	SECMPU PCE0	指定闪存的安全提取区域或SRAM	0000 040Ch	4

Table 7.1 MPU registers (2 of 2)

Register name	Symbol	Function	Address	Size (byte)
Security MPU Program Counter Start Address Register 1	SECMPUPCS1	Specifies the security fetch region of flash or SRAM	0000 0410h	4
Security MPU Program Counter End Address Register 1	SECMPUPCE1	Specifies the security fetch region of flash or SRAM	0000 0414h	4
Security MPU Region 0 Start Address Register	SECMPUS0	Specifies the secure program and flash data	0000 0418h	4
Security MPU Region 0 End Address Register	SECMPUE0	Specifies the secure program and flash data	0000 041Ch	4
Security MPU Region 1 Start Address Register	SECMPUS1	Specifies the secure data of SRAM	0000 0420h	4
Security MPU Region 1 End Address Register	SECMPUE1	Specifies the secure data of SRAM	0000 0424h	4
Security MPU Region 2 Start Address Register	SECMPUS2	Specifies the secure data of security functions	0000 0428h	4
Security MPU Region 2 End Address Register	SECMPUE2	Specifies the secure data of security functions	0000 042Ch	4
Security MPU Region 3 Start Address Register	SECMPUS3	Specifies the secure data of security functions	0000 0430h	4
Security MPU Region 3 End Address Register	SECMPUE3	Specifies the secure data of security functions	0000 0434h	4
Security MPU Access Control Register	SECMPUAC	Security enabled/disabled region is specified	0000 0438h	4

7.2.4 Access Window Setting Control Register (AWSC)

Address(es): AWSC 0101 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset: The value set by the user	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset: The value set by the user	—	FSPR	—	—	—	—	—	BTFLG	—	—	—	—	—	—	—	—

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b8	BTFLG	Startup Area Select Flag	This bit specifies whether the address of the startup area is exchanged for the boot swap function. 0: First 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh) are exchanged 1: First 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh) are not exchanged.	R
b13 to b9	—	Reserved	When read, these bits return the value written by the user. The write value should be 1.	R

Table 7.1 MPU寄存器（2个中的2个）

注册名称	Symbol	Function	Address	Size (byte)
安全MPU程序计数器启动地址寄存器1	SECMPUPCS1	指定闪存的安全提取区域或SRAM	0000 0410h	4
安全MPU程序计数器结束地址寄存器1	SECMPUPCE1	指定闪存的安全提取区域或SRAM	0000 0414h	4
安全MPU区域0起始地址Register	SECMPUS0	指定安全程序和闪存数据	0000 0418h	4
安全MPU区域0结束地址Register	SECMPUE0	指定安全程序和闪存数据	0000 041Ch	4
安全MPU区域1起始地址Register	SECMPUS1	指定SRAM的安全数据	0000 0420h	4
安全MPU区域1结束地址Register	SECMPUE1	指定SRAM的安全数据	0000 0424h	4
安全MPU区域2起始地址Register	SECMPUS2	指定安全功能的安全数据	0000 0428h	4
安全MPU区域2结束地址Register	SECMPUE2	指定安全功能的安全数据	0000 042Ch	4
安全MPU区域3起始地址Register	SECMPUS3	指定安全功能的安全数据	0000 0430h	4
安全MPU区域3结束地址Register	SECMPUE3	指定安全功能的安全数据	0000 0434h	4
安全MPU访问控制寄存器	SECMPUAC	指定了启用安全性的禁用区域	0000 0438h	4

7.2.4 访问窗口设置控制寄存器(AWSC)

Address(es): AWSC 0101 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：用户设置的值	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：用户设置的值	—	FSPR	—	—	—	—	—	BTFLG	—	—	—	—	—	—	—	—

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b8	BTFLG	启动区选择标志	该位指定是否为启动交换功能交换启动区域的地址。0：交换第一个8-KB区域（00000000h到00001FFFh）和第二个8-KB区域（00002000h到00003FFFh）1：第一个8-KB区域（00000000h到00001FFFh）和第二个8-KB区域（00002000h到00003FFFh)不交换。	R
b13 to b9	—	Reserved	读取时，这些位返回用户写入的值。写入值应为1。	R

Bit	Symbol	Bit name	Description	R/W
b14	FSPR	Protection of Access Window and Startup Area Select Function	This bit controls the programming of the write/erase protection for the access window, the Startup Area Select Flag (BTFLG), and the temporary boot swap control. When this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the access window (FAWE[11:0], FAWS[11:0]) and the Startup Area Select Flag (BTFLG) is invalid. 1: Executing the configuration setting command for programming the access window (FAWE[11:0], FAWS[11:0]) and the Startup Area Select Flag (BTFLG) is valid.	R
b31 to b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

7.2.5 Access Window Setting Register (AWS)

Address(es): AWS 0101 0010h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	FAWE[11:0]*1											
Value after reset:				The value set by the user											

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	FAWS[11:0]*1											
Value after reset:				The value set by the user											

Bit	Symbol	Bit name	Description	R/W
b11 to b0	FAWS[11:0]*1	Access Window Start Block Address*1	These bits specify the start block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The block address specifies the first address of the block and consists of the address bits [21:10].	R
b15 to b12	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b27 to b16	FAWE[11:0]*1	Access Window End Block Address*1	These bits specify the end block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The end block address for the access window is the next block to the acceptable programming and erasure region defined by the access window. The block address specifies the first address of the block and consists of the address bits [21:10].	R
b31 to b28	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Note 1. The write value should be 0 for FAWE[0] and FAWS[0].

Issuing the program or erase command to an area outside the access window causes a command-locked state. The access window is only valid in the program flash area. The access window provides protection in self-programming mode, serial programming mode, and on-chip debug mode. The access window can be locked by the FSPR bit.

The access window is specified in both the FAWS[11:0] and FAWE[11:0] bits. The following describes how to set the FAWS[11:0] and the FAWE[11:0] bits.

- FAWE[11:0] = FAWS[11:0]: The P/E command is allowed to execute in the full program flash area.
- FAWE[11:0] > FAWS[11:0]: The P/E command is only allowed to execute in the window from the block pointed to by the FAWS[11:0] bits to the block one lower than the block pointed to by the FAWE[11:0] bits.
- FAWE[11:0] < FAWS[11:0]: The P/E command is not allowed to execute in the program flash area.

Bit	Symbol	位名称	Description	R/W
b14	FSPR	访问窗口和启动区域选择功能的保护	该位控制访问窗口的写擦除保护、启动区域选择标志(BTFLG)和临时引导交换控制的编程。当该位设置为0时，不能更改为1。0：执行用于编程访问窗口（FAWE[11:0]、FAWS[11:0]）和启动区域选择标志（BTFLG）的配置设置命令）是无效的。1：执行访问窗口（FAWE[11:0]、FAWS[11:0]）和启动区选择标志（BTFLG）编程的配置设置命令有效。	R
b31 to b15	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

7.2.5 访问窗口设置寄存器(AWS)

Address(es): AWS 0101 0010h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	FAWE[11:0]*1											
重置后的值：				用户设置的值											

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	FAWS[11:0]*1											
重置后的值：				用户设置的值											

Bit	Symbol	位名称	Description	R/W
b11 to b0	FAWS[11:0]*1	访问窗口启动块 Address*1	这些位指定访问窗口的起始块地址。 它们不代表访问窗口的块号。访问窗口仅在程序闪存区有效。块地址指定块的首地址，由地址位[21:10]组成。	R
b15 to b12	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b27 to b16	FAWE[11:0]*1	访问窗口结束块 Address*1	这些位指定访问窗口的结束块地址。它们不代表访问窗口的块号。访问窗口仅在程序闪存区有效。访问窗口的结束块地址是访问窗口定义的可接受编程和擦除区域的下一个块。块地址指定块的首地址，由地址位[21:10]组成。	R
b31 to b28	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

注1.FAWE[0]和FAWS[0]的写入值应为0。

向访问窗口之外的区域发出编程或擦除命令会导致命令锁定状态。访问窗口仅在程序闪存区有效。访问窗口在自编程模式、串行编程模式和片上调试模式下提供保护。访问窗口可以通过FSPR位锁定。

访问窗口在FAWS[11:0]和FAWE[11:0]位中指定。下面介绍如何设置FAWS[11:0]和FAWE[11:0]位。

- FAWE[11:0]=FAWS[11:0]：允许PE命令在整个程序闪存区执行。
- FAWE[11:0]>FAWS[11:0]：PE命令只允许在窗口中从FAWS[11:0]位指向的块到比FAWS[11:0]指向的块低一级的块执行FAWE[11:0]位。
- FAWE[11:0]<FAWS[11:0]：PE命令不允许在程序闪存区执行。

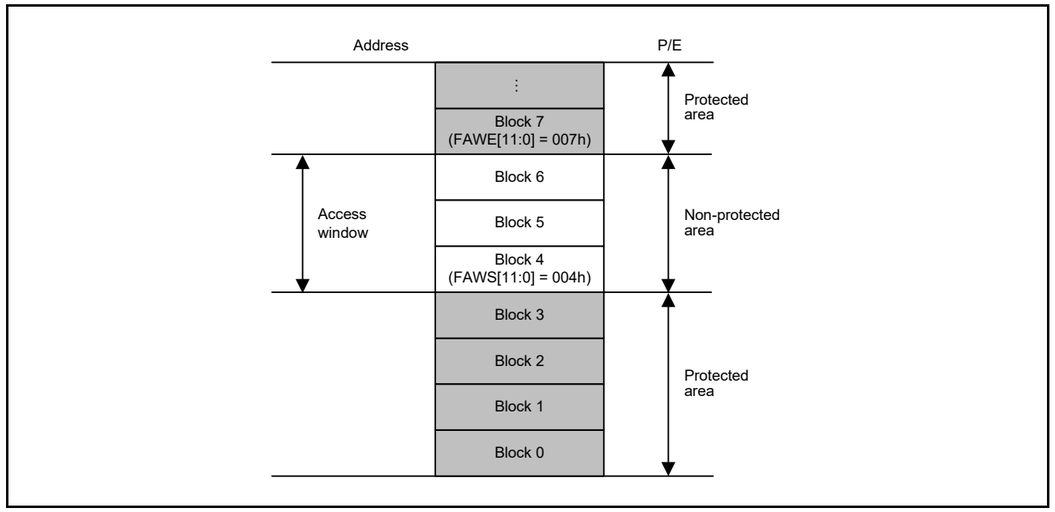


Figure 7.2 Access window overview

7.2.6 OCD/Serial Programmer ID Setting Register (OSIS)

The OSIS register stores the ID for ID code protection of the OCD/serial programmer. When connecting the OCD/serial programmer, write values so that the MCU can determine whether to permit the connection. Use this register to check whether a code transmitted from the OCD/serial programmer matches the ID code in the option-setting memory. When the ID codes match, connection of the OCD/serial programmer is permitted, if not, connection with the OCD/serial programmer is not possible. The OSIS register must be set in 32-bit words.

Address(es): OSIS 0101 0018h, OSIS 0101 0020h, OSIS 0101 0028h, OSIS 0101 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	The value set by the user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	The value set by the user															

These fields hold the ID for use in ID authentication for the OCD/serial programmer.

ID code bit [127] and bit [126] determine whether the ID code protection is enabled and the method of authentication to use with the host. Table 7.2 shows how the ID code determines the method of authentication.

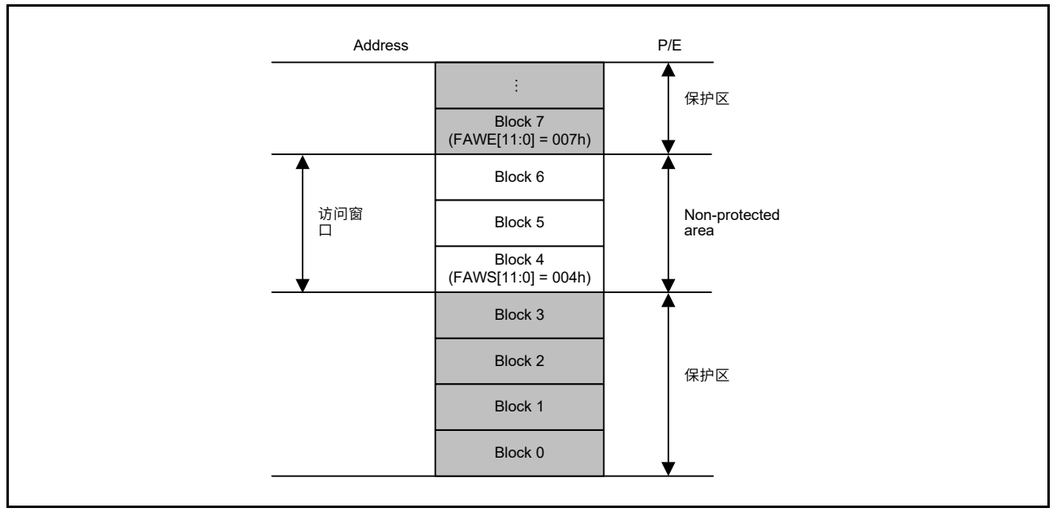


Figure 7.2 访问窗口概述

7.2.6 OCD串行编程器ID设置寄存器(OSIS)

OSIS寄存器存储用于保护OCD串行编程器的ID代码的ID。连接OCD串口编程器时，写入数值，让MCU判断是否允许连接。使用该寄存器检查从OCD串行编程器发送的代码是否与选项设置存储器中的ID代码匹配。当ID码匹配时，允许连接OCD串行编程器，如果不匹配，则不能连接OCD串行编程器。OSIS寄存器必须设置为32位字。

Address(es): OSIS 0101 0018h, OSIS 0101 0020h, OSIS 0101 0028h, OSIS 0101 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	用户设置的值															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	用户设置的值															

这些字段保存用于OCD串行编程器身份验证的ID。

ID代码位[127]和位[126]确定是否启用ID代码保护以及与主机一起使用的身份验证方法。表7.2显示了ID代码如何确定身份验证方法。

Table 7.2 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI/USB boot mode) On-chip debug mode (JTAG/SWD Boot mode)	FFh, …, FFh (all bytes are FFh)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to the programmer or on-chip debugger is permitted
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not FFh	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the content of the user flash (code and data) area, and the configuration area are erased. However, forced erasure is not executed when the FSPR bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, and the connection to the programmer or the on-chip debugger is prohibited.

7.3 Setting Option-Setting Memory

7.3.1 Allocation of Data in Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 7.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

7.3.2 Setting Data for Programming Option-Setting Memory

Allocating data according to the procedure described in section 7.3.1, Allocation of Data in Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

Use the programming command to write data to the program flash area. Use the configuration setting command to write data to the option-setting memory in the configuration setting area. In addition, use the startup area select function to safely update the boot program that includes the option-setting memory.

For details of the programming command, the configuration setting command, and the startup area select function, see section 43, Flash Memory.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, see the tool manual for details.

The MCU provides two setting procedures:

- Read the data allocated as described in section 7.3.1, Allocation of Data in Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data as allocated in section 7.3.1, Allocation of Data in Option-Setting Memory.

Table 7.2 ID码保护规范

启动时的操作模式	身份证号码	保护状态	连接到编程器或片上调试器的操作
串行编程模式（SCIUSB启动模式） 片上调试模式（JTAGSWD引导模式）	FFh … FFh（所有字节均为FFh）	保护已禁用	ID码不检查，ID码始终匹配，允许连接编程器或片上调试器
	位[127]=1，位[126]=1，16个字节中至少有一个不是FFh	启用保护	匹配ID代码=验证完成，允许连接到编程器或片上调试器。不匹配的ID代码=转换到ID代码保护等待状态。当编程器或片上调试器发送的ID码为ASCII码（414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh）中的ALeRASE时，用户闪存（代码和数据）区和配置区的内容被擦除。然而，强制擦除不执行时 FSPR位为0。
	位[127]=1和位[126]=0	启用保护	匹配ID代码=验证完成，允许连接到编程器或片上调试器。不匹配的ID代码=转换到ID代码保护等待状态。
	Bit [127] = 0	启用保护	ID码不检查，ID码总是不匹配，禁止连接编程器或片上调试器。

7.3 设置选项设置内存

7.3.1 选项设置内存中的数据分配

编程数据被分配到图7.1所示的选项设置存储器中的地址。分配的数据由闪存编程软件或片上调试器等工具使用。

Note: 编程格式因编译器而异。有关详细信息，请参阅编译器手册。

7.3.2 编程选项设置存储器的设置数据

根据第7.3.1节"在选项设置内存中分配数据"中描述的过程分配数据，并不会真正将数据写入选项设置内存。您还必须遵循本节中描述的操作之一。

(1) 通过自编程更改选项设置存储器

使用编程命令将数据写入程序闪存区域。使用配置设置命令将数据写入配置设置区的选项设置内存。此外，使用启动区域选择功能可以安全地更新包含选项设置存储器的引导程序。

有关编程命令、配置设置命令和启动区域选择功能的详细信息，请参见第43节，闪存。

(2) 通过OCD进行调试或通过闪存写入器进行编程

此过程取决于所使用的工具，详细信息请参见工具手册。

MCU提供两种设置程序：

- 从编译器生成的目标文件或MotorolaS格式文件中读取如第7.3.1节"选项设置内存中的数据分配"中所述分配的数据，并将数据写入MCU
- 使用工具的GUI界面对第7.3.1节中分配的数据进行编程，数据分配 Option-Setting Memory.

7.4 Usage Note

7.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits of reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

7.4 使用说明

7.4.1 用于编程选项设置中的保留区域和保留位的数据 Memory

当期权设置内存中的保留区域和保留位在编程范围内时，将1写入保留区域和所有保留位的所有位。如果将0写入这些位，则无法保证正常操作。

8. Low Voltage Detection (LVD)

8.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. The LVD module consists of two separate voltage level detectors, 0 and 1, which measure the voltage level input to the VCC pin. LVD voltage detection registers allow your application to configure detection of VCC changes at various voltage thresholds.

Each voltage level detector has a voltage monitor associated with it, for example voltage monitor 0, and 1. Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 8.1 lists the LVD specifications. Figure 8.1 shows a block diagram of voltage detectors 0 and 1, Figure 8.2 shows a block diagram of the voltage monitor 1 interrupt/reset circuit.

Table 8.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1
VCC monitoring	Monitored voltage	Vdet0	Vdet1
	Detected event	Voltage falls below Vdet0	Voltage rises or falls past Vdet1
	Detection voltage	Selectable from three different levels in the OFS1.VDSEL1[2:0] bits	Selectable from 10 different levels in the LVDLVLR.LVD1LVL[4:0] bits
	Monitor flag	None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than Vdet1
			LVD1SR.DET flag: Vdet1 passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt
			Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vdet1 > VCC or VCC > Vdet1
Event linking		None	Available Output of event signals on detection of Vdet1 crossings

8. 低电压检测(LVD)

8.1 Overview

低电压检测(LVD)模块监控输入到VCC引脚的电压电平，并且可以使用软件程序选择检测电平。LVD模块由两个独立的电压电平检测器0和1组成，它们测量输入到VCC引脚的电压电平。LVD电压检测寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。

每个电压电平检测器都有一个与之关联的电压监视器，例如电压监视器0和1。电压监视器寄存器用于配置LVD，以在超过阈值时触发中断、事件链接输出或复位。

表8.1列出了LVD规格。图8.1显示了电压检测器0和1的框图，图8.2显示了电压监测器1中断复位电路的框图。

Table 8.1 LVD specifications

Parameter		电压监视器0	电压监视器1
VCC monitoring	监控电压	Vdet0	Vdet1
	检测到的事件	电压低于Vdet0	电压上升或下降超过Vdet1
	检测电压	可从OFS1.VDSEL1[2:0]位的三个不同级别中选择	可从10个不同的级别中选择 LVDLVLR.LVD1LVL[4:0] bits
	监控标志	None	LVD1SR.MON标志：监控电压是高于还是低于Vdet1
			LVD1SR.DET标志：Vdet1通过检测
电压检测流程	Reset	电压监控器0复位	电压监视器1复位
		当Vdet0>VCC时复位 CPU在指定时间后重启 VCC > Vdet0	当Vdet1>VCC时复位 CPU重启时间可选：在VCC>Vdet1或Vdet1>VCC的指定时间后
	Interrupt	无中断	电压监视器1中断
			可选择不可屏蔽中断或可屏蔽中断
			当Vdet1>VCC或 VCC > Vdet1
事件链接		None	检测到Vdet1交叉时事件信号的可用输出

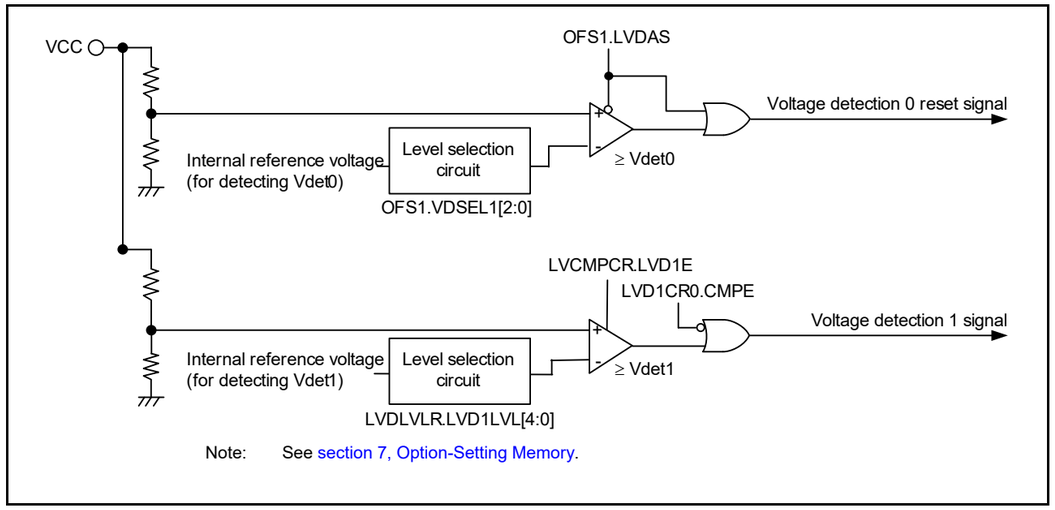


Figure 8.1 Voltage detection 0 and 1 block diagram

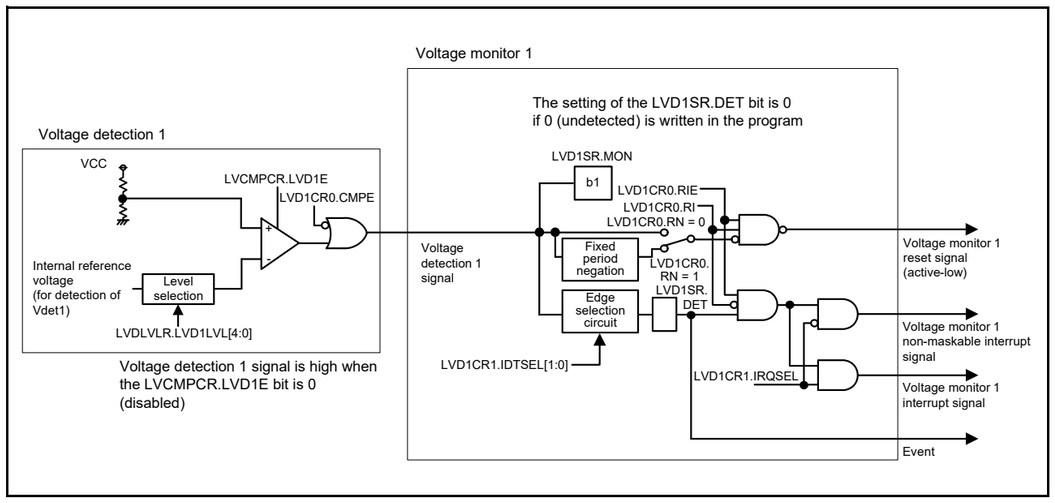


Figure 8.2 Voltage monitor 1 interrupt/reset circuit block diagram

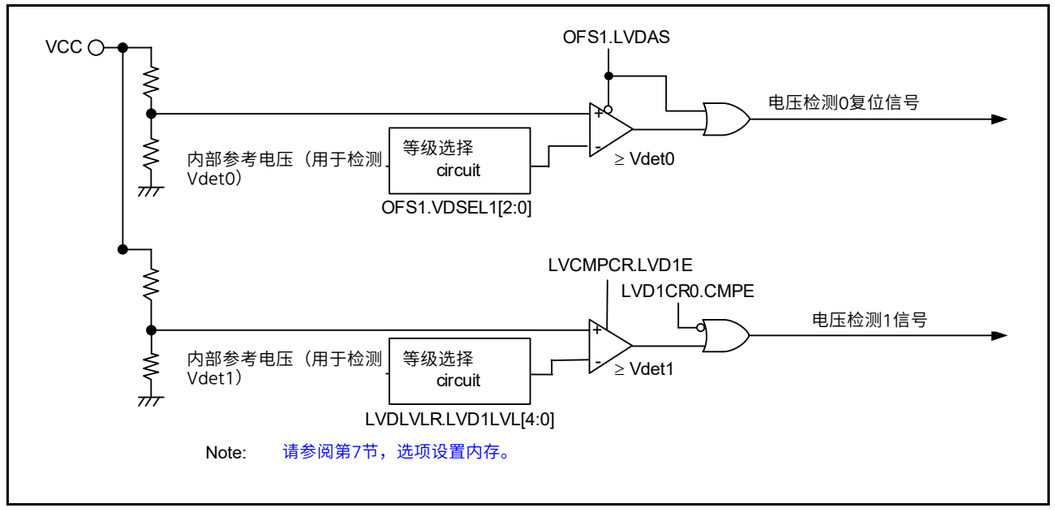


Figure 8.1 电压检测0和1框图

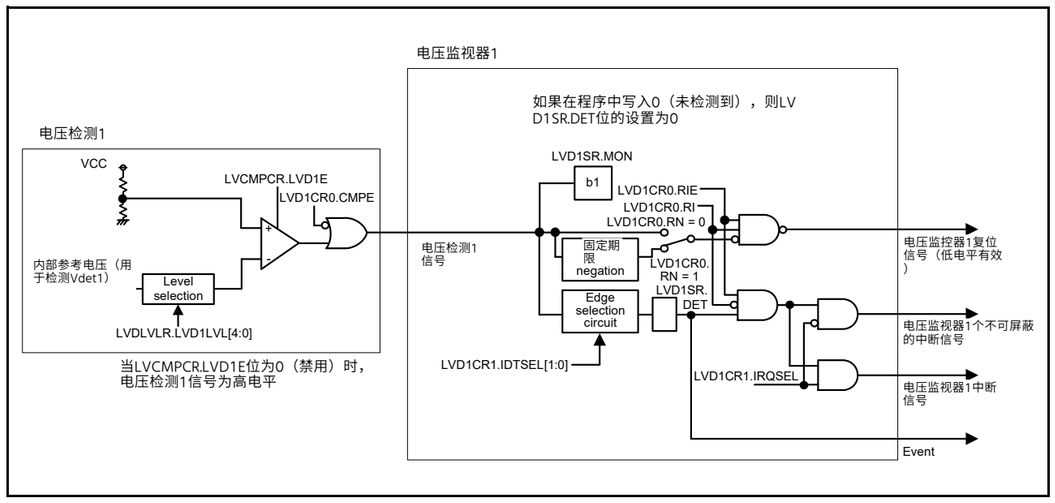


Figure 8.2 电压监视器1中断复位电路框图

8.2 Register Descriptions

8.2.1 Voltage Monitor 1 Circuit Control Register 1 (LVD1CR1)

Address(es): SYSTEM.LVD1CR1 4001 E0E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ Vdet1 (rise) is detected 0 1: When VCC < Vdet1 (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 1 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt*1.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the value of the NMIER.LVD1EN bit in the ICU from the reset state.

8.2.2 Voltage Monitor 1 Circuit Status Register (LVD1SR)

Address(es): SYSTEM.LVD1SR 4001 E0E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 1 Voltage Change Detection Flag	0: Not detected 1: Vdet1 passage detected.	R(/W) *1
b1	MON	Voltage Monitor 1 Signal Monitor Flag	0: VCC < Vdet1 1: VCC ≥ Vdet1 or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

Set the DET flag to 0 after LVD1CR0.RIE is set to 0 (disabled). LVD1CR0.RIE can be set to 1 (enabled) after 2 or more PCLKB cycles have elapsed.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

8.2 注册说明

8.2.1 电压监视器1电路控制寄存器1(LVD1CR1)

Address(es): SYSTEM.LVD1CR1 4001 E0E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b1, b0	IDTSEL[1:0]	电压监视器1中断发生条件选择	b1b000：检测到VCC Vdet1（上升）时01：检测到VCC<Vdet1（下降）时10：检测到下降和上升时11：禁止设置。	R/W
b2	IRQSEL	电压监视器1中断类型 Select	0: Non-maskable interrupt 1: Maskable interrupt*1.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
Note 1. 当启用可屏蔽中断时，不要从复位状态更改ICU中NMIER.LVD1EN位的值。

8.2.2 电压监视器1电路状态寄存器(LVD1SR)

Address(es): SYSTEM.LVD1SR 4001 E0E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	DET	电压监视器1电压变化检测标志	0：未检测到1：检测到Vdet1通过。	R(/W) *1
b1	MON	电压监视器1信号监视器标志	0：VCC<Vdet11：VCC Vdet1或MON被禁用。	R
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
Note 1. 该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器1电压变化检测标志）

当LVCMPCR.LVD1E位为1（使能电压检测1电路）且LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

在LVD1CR0.RIE设置为0（禁用）后，将DET标志设置为0。LVD1CR0.RIE可以在2或更多之后设置为1（启用）PCLKB周期已经过去。

MON标志（电压监视器1信号监视器标志）

当LVCMPCR.LVD1E位为1（使能电压检测1电路）且LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

8.2.3 Voltage Monitor Circuit Control Register (LVCMPCR)

Address(es): SYSTEM.LVCMPCR 4001 E417h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled.	R/W
b7, b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts when td(E-A) elapses after the LVD1E bit value is changed from 0 to 1.

8.2.4 Voltage Detection Level Select Register (LVDLVLR)

Address(es): SYSTEM.LVDLVLR 4001 E418h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	LVD1LVL[4:0]				
Value after reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during fall in voltage)	b4 b0 0 0 1 0 0: 3.10 V (Vdet1_4) 0 0 1 0 1: 3.00 V (Vdet1_5) 0 0 1 1 0: 2.90 V (Vdet1_6) 0 0 1 1 1: 2.79 V (Vdet1_7) 0 1 0 0 0: 2.68 V (Vdet1_8) 0 1 0 0 1: 2.58 V (Vdet1_9) 0 1 0 1 0: 2.48 V (Vdet1_A) 0 1 0 1 1: 2.20 V (Vdet1_B) 0 1 1 0 0: 1.96 V (Vdet1_C) 0 1 1 0 1: 1.86 V (Vdet1_D) Other settings are prohibited.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The contents of the LVDLVLR register can only be changed if the LVCMPCR.LVD1E bit (voltage detection 1 circuit disable) is 0.

8.2.3 电压监控电路控制寄存器(LVCMPCR)

Address(es): SYSTEM.LVCMPCR 4001 E417h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD1E	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	LVD1E	电压检测1使能	0：电压检测1电路无效1：电压检测1电路有效。	R/W
b7, b6	—	Reserved	该位读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVD1E位（电压检测1使能）

当使用电压检测1中断复位或LVD1SR.MON位时，将LVD1E位设置为1。当LVD1E位值从0变为1后经过td(E-A)时，电压检测1电路启动。

8.2.4 电压检测电平选择寄存器(LVDLVLR)

Address(es): SYSTEM.LVDLVLR 4001 E418h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	LVD1LVL[4:0]				
重置后的值	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	LVD1LVL[4:0]	电压检测1电平选择（电压下降时的标准电压）	b4b000100：3.10V(Vdet1_4)00101：3.00V(Vdet1_5)00110：2.90V(Vdet1_6)00111：2.79V(Vdet1_7)01000：2.68V(Vdet1_8)01001：2.58V(Vdet1_9)01010：2.48V(Vdet1_A)01011：2.20V(Vdet1_B)01100：1.96V(Vdet1_C))01101:1.86V(Vdet1_D)禁止其他设置。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVDLVLR寄存器的内容只有在LVCMPCR.LVD1E位（电压检测1电路禁用）为0时才能更改。

8.2.5 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0)

Address(es): SYSTEM.LVD1CR0 4001 E41Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	—	—	—	CMPE	—	RIE
Value after reset:	1	0	0	0	x	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 1 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	—	Reserved	The read value is 0. The write value should be 0.	R/W
b2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable	0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	RI	Voltage Monitor 1 Circuit Mode Select	0: Generate voltage monitor 1 interrupt on Vdet1 passage 1: Enable voltage monitor 1 reset when the voltage falls to and below Vdet1.	R/W
b7	RN	Voltage Monitor 1 Reset Negate Select	0: Negate after a stabilization time (tLVD1) when VCC > Vdet1 is detected 1: Negate after a stabilization time (tLVD1) on assertion of the LVD1 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 1 interrupt/reset. Set this bit to ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). In addition, if a transition to Software Standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) when this is the case.

8.3 VCC Input Voltage Monitor

8.3.1 Monitoring Vdet0

The comparison results from voltage monitor 0 are not available for reading.

8.3.2 Monitoring Vdet1

Table 8.2 shows the procedure to set up monitoring against Vdet1. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

Table 8.2 Procedures to set up monitoring against Vdet1 (1 of 2)

Step		Monitoring the results of comparison from voltage monitor 1
Setting the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 to enable voltage detection 1.
	4	Wait for at least td(E-A) for LVD operation stabilization after LVD is enabled.

8.2.5 电压监视器1电路控制寄存器0(LVD1CR0)

Address(es): SYSTEM.LVD1CR0 4001 E41Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	—	—	—	CMPE	—	RIE
重置后的值:	1	0	0	0	x	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RIE	电压监视器1中断复位 Enable	0：禁用1 ：启用。	R/W
b1	—	Reserved	读取值为0。写入值应为0。	R/W
b2	CMPE	电压监视器1电路 比较结果输出使能	0：禁止电压监视1电路比较结果输出1：使能电压监视1电路比较结果输出。	R/W
b3	—	Reserved	读取值未定义。写入值应为1。	
b5, b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	RI	电压监视器1电路模式 Select	0：在Vdet1通道上产生电压监控1中断1：当电压下降到Vdet1或低于Vdet1时，使能电压监控1复位。	R/W
b7	RN	电压监视器1复位否定 Select	0：当检测到VCC>Vdet1时，在稳定时间(tLVD1)后取反1：在LVD1复位有效时，在稳定时间(tLVD1)后取反。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器1中断复位使能）

RIE位启用或禁用电压监视器1中断复位。设置该位以确保在闪存的编程或擦除期间不会产生电压监视器1中断或电压监视器1复位。

RN位（电压监视器1复位否定选择）

如果要设置RN位为1（在LVD1复位信号置位后的稳定时间之后取反），则设置MOCOCR.MCSTP位为0（MOCO运行）。此外，如果要转换到软件待机，则RN位唯一可能的值为0（在检测到VCC>Vdet1后的稳定时间后取反）。在这种情况下，请勿将RN位设置为1（在LVD1复位信号置位后的稳定时间之后取反）。

8.3 VCC输入电压监视器

8.3.1 Monitoring Vdet0

电压监视器0的比较结果不可读取。

8.3.2 Monitoring Vdet1

表8.2显示了针对Vdet1设置监控的过程。设置完成后，电压监视器1的比较结果可以通过LVD1SR.MON标志进行监视。

Table 8.2 针对Vdet1设置监控的程序（1个，共2个）

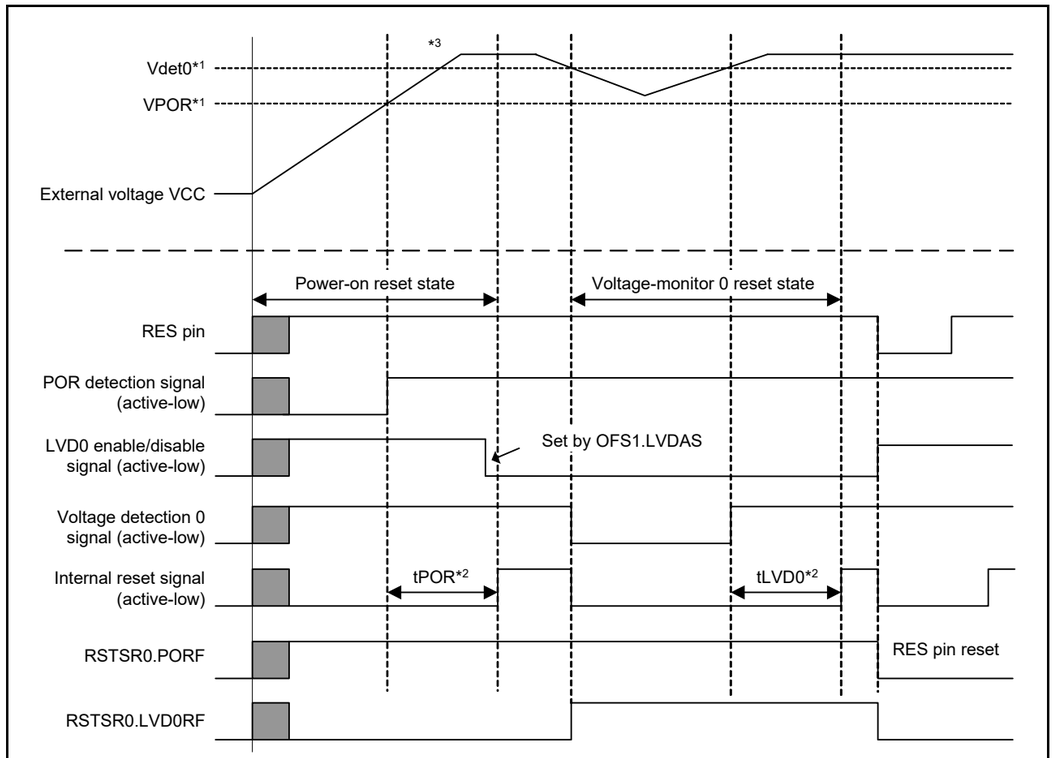
Step		从电压监视器1监视比较结果
设置电压检测1电路	1	设置LVCMPCR.LVD1E=0以在写入LVDLVLR寄存器之前禁用电压检测1。
	2	在LVDLVLR.LVD1LVL[4:0]位中选择检测电压。
	3	设置LVCMPCR.LVD1E=1以启用电压检测1。
	4	启用LVD后，至少等待td(E-A)以使LVD操作稳定。

Table 8.2 Procedures to set up monitoring against Vdet1 (2 of 2)

Step		Monitoring the results of comparison from voltage monitor 1
Enabling output	5	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

8.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit. Figure 8.3 shows an example operation of a voltage monitor 0 reset.



Note: For details of the electrical characteristics, see section 48, Electrical Characteristics.
Note 1. VPOR indicates the detection level for a power-on reset and Vdet0 indicates the detection level for a voltage monitor 0 reset.
Note 2. tPOR indicates the period of a power-on reset and tLVD0 indicates the period of a voltage monitor 0 reset.
Note 3. At power-on, raise VCC to the minimum guaranteed voltage before the POR reset is released.

Figure 8.3 Example of voltage monitor 0 reset operation

8.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the results of comparison from the voltage monitor 1 circuit.

Table 8.3 shows the procedure for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring operates. Table 8.4 shows the procedure for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 8.4 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 6.2 in section 6, Resets.

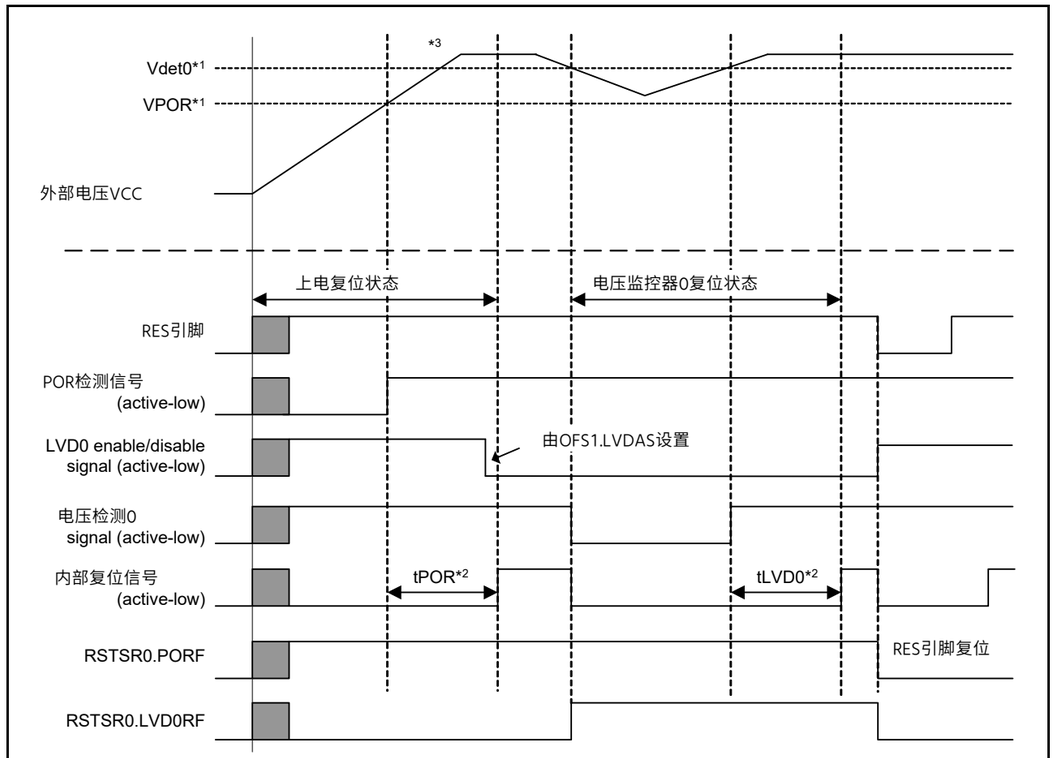
When using the voltage monitor 1 circuit in Software Standby mode, set up the circuit with the following procedures.

Table 8.2 针对Vdet1设置监控的程序（2个中的2个）

Step		从电压监视器1监视比较结果
启用输出	5	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。

8.4 从电压监视器复位0

使用电压监控器0复位时，将OFS1.LVDAS位清零以在复位后启用电压监控器0复位。但是，在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。图8.3显示了电压监视器0复位的示例操作。



Note: 有关电气特性的详细信息，请参见第48节，电气特性。
Note 1. VPOR表示上电复位的检测电平，Vdet0表示电压监视器0复位的检测电平。
Note 2. tPOR表示上电复位周期，tLVD0表示电压监视器0复位周期。
Note 3. 上电时，在POR复位释放前将VCC提升到最低保证电压。

Figure 8.3 电压监视器0复位操作示例

8.5 电压监视器1的中断和复位

响应来自电压监视器1电路的比较结果，可以产生中断或复位。

表8.3显示了设置与电压监控1中断复位相关的位以使电压监控运行的过程。表8.4显示了设置与电压监控1中断复位相关的位以停止电压监控的过程。图8.4显示了电压监视器1中断的操作示例。有关电压监视器1复位的操作，请参见第6节"复位"中的图6.2。

在软件待机模式下使用电压监视器1电路时，请按照以下步骤设置电路。

(1) Setting in Software Standby mode

- When VCC > Vdet1 is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

Table 8.3 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitor operates

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR register.	
	2	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	
	3	Set LVCMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least td(E-A) for LVD operation stabilization after LVD is enabled.*1	
Setting the voltage monitor 1 interrupt/ reset	5	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset • Select the type of reset negation by setting the LVD1CR0.RN bit.
	6	• Select the timing of interrupt requests by setting the LVD1CR1.IDTSEL[1:0] bits • Select the type of interrupt by setting the LVD1CR1.IRQSEL bit.	—
Enabling output	7	Set LVD1SR.DET = 0.	
	8	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*2	
	9	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 8 can be performed during the wait time of step 4. For details of td(E-A), see section 48, Electrical Characteristics.
Note 2. Step 8 is not required if only the ELC event signal is to be output.

Table 8.4 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitor stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Settings to stop enabling of output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 1.
	2	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*1
Stopping the voltage detection 1 circuit	3	Set LVCMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Step 2 is not required if only the ELC event signal is to be output.

If the voltage monitor 1 interrupt or voltage monitor 1 reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 1 circuit is not required if the settings for the voltage detection 1 circuit do not change
- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or voltage monitor 1 reset do not change.

(1) 在软件待机模式下设置

- 当检测到VCC>Vdet1时，在一段稳定时间后取消电压监视器1复位信号(LVD1CR0.RN=0)。

Table 8.3 设置与电压监视器1中断和电压监视器1复位相关的位以使电压监视器工作的步骤

Step		电压监视器1中断（电压监视器1ELC事件输出）	电压监视器1复位
设置电压检测1电路	1	设置LVCMPCR.LVD1E=0以在写入LVDLVLR寄存器之前禁用电压检测1。	
	2	通过设置LVDLVLR.LVD1LVL[3:0]位来选择检测电压。	
	3	设置LVCMPCR.LVD1E=1以启用电压检测1电路。	
	4	启用LVD后，至少等待td(E-A)以使LVD操作稳定。*1	
设置电压监视器1中断复位	5	设置LVD1CR0.RI=0以选择电压监视器1中断。	设置LVD1CR0.RI=1以选择电压监视器1复位 通过设置LVD1CR0.RN位选择复位否定类型。
	6	通过设置LVD1CR1.IDTSEL[1:0]位选择中断请求的时序 通过设置LVD1CR1.IRQSEL位选择中断类型。	—
启用输出	7	Set LVD1SR.DET = 0.	
	8	设置LVD1CR0.RIE=1以启用电压监视器1中断或复位。*2	
	9	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。	

Note 1. 步骤5至8可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参见第48节，电气特性。
Note 2. 如果只输出ELC事件信号，则不需要步骤8。

Table 8.4 设置与电压监视器1中断和电压监视器1复位相关的位以使电压监视器停止的步骤

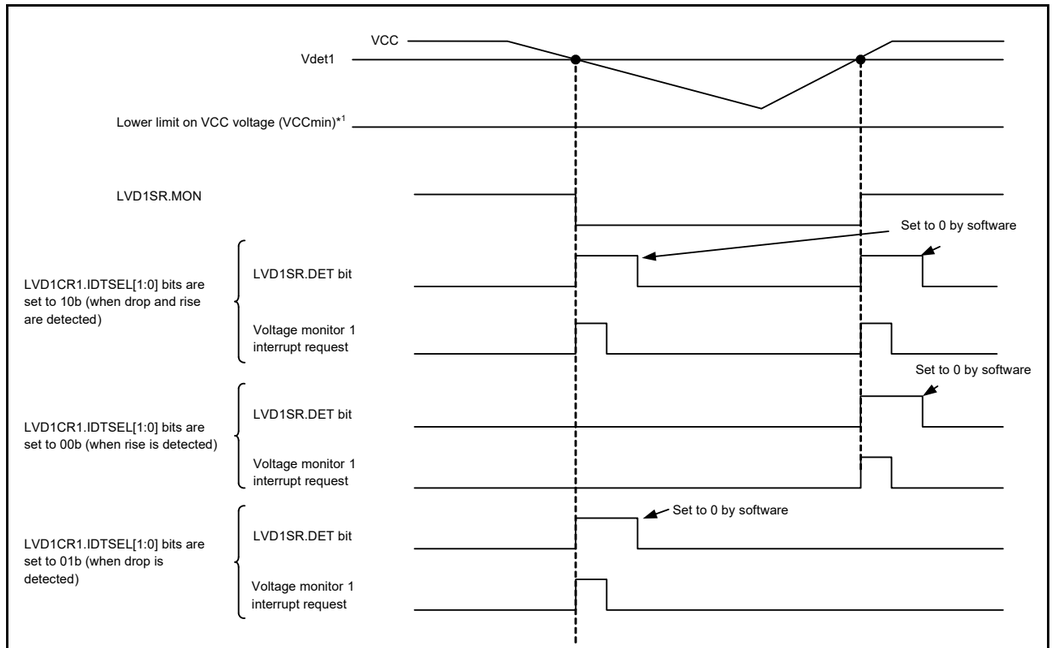
Step		电压监视器1中断（电压监视器1ELC事件输出），电压监视器1复位
停止启用输出的设置	1	设置LVD1CR0.CMPE=0以禁用电压监视器1的比较结果输出。
	2	设置LVD1CR0.RIE=0以禁用电压监视器1中断或复位。*1
停止电压检测1电路	3	设置LVCMPCR.LVD1E=0以禁用电压检测1电路。

Note 1. 如果只输出ELC事件信号，则不需要步骤2。

如果电压监控器1中断或电压监控器1复位设置在使用和停止一次后再次进行，则在停止和设置过程中省略以下步骤，视情况而定：

- 如果电压检测1电路的设置不改变，则不需要设置或停止电压检测1电路
- 如果电压监视器1中断或电压监视器1复位的设置没有改变，则不需要设置电压监视器1中断或复位。

Figure 8.4 shows an example of the voltage monitor 1 interrupt operation.



Note 1. When the voltage monitor 0 reset is not in use, VCC ≥ VCCmin.

Figure 8.4 Voltage monitor 1 interrupt operation example

8.6 Event Link Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) Vdet1 Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the Vdet1 voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.

8.6.1 Interrupt Handling and Event Linking

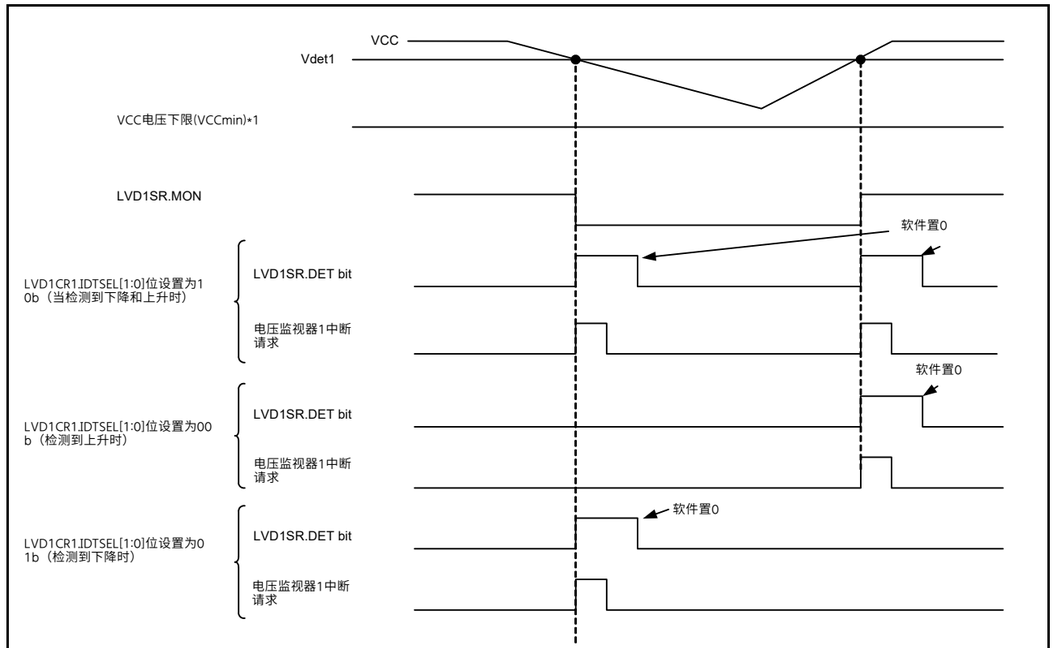
The LVD provides bits to individually enable or disable the voltage monitor 1 interrupt. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal (LVD1CR0.RIE) is output to the CPU.

On the other hand, as soon as an interrupt source is generated, the event link signal is output as the event signal to the other module through the ELC regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 interrupt in Software Standby mode. The event signals for the ELC in Software Standby mode are output as follows:

- When a Vdet1 passage event is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the Vdet1 passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the Vdet1 detection flag

图8.4显示了电压监视器1中断操作的示例。



Note 1. 不使用电压监视器0复位时，VCC VCCmin。

Figure 8.4 电压监视器1中断操作示例

8.6 事件链接输出

LVD可以将事件信号输出到事件链接控制器(ELC)。

(1) Vdet1交叉检测事件

当电压检测1电路和电压监控器1电路比较结果输出都启用时，LVD检测到电压已超过Vdet1电压时输出事件信号。

8.6.1 中断处理和事件链接

LVD提供位来单独启用或禁用电压监视器1中断。当产生中断源并通过中断使能位使能中断时，向CPU输出中断信号（LVD1CR0.RIE）。

另一方面，一旦产生中断源，无论中断使能位的状态如何，事件链接信号都作为事件信号通过ELC输出到其他模块。

在软件待机模式下可以输出电压监视器1中断。软件中ELC的事件信号
待机模式输出如下：

- 当在软件待机模式下检测到Vdet1通过事件时，不会为ELC生成事件信号，因为在软件待机模式下不提供时钟。因为保存了Vdet1通过检测标志，所以当从软件待机模式恢复后恢复时钟供应时，ELC的事件信号将根据Vdet1检测标志的状态输出

9. Clock Generation Circuit

9.1 Overview

The MCU provides a clock generation circuit.

Table 9.1 and Table 9.2 list the clock generation circuit specifications. Figure 9.1 shows a block diagram, and Table 9.3 lists the I/O pins.

Table 9.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specification
Main clock oscillator (MOSC)	Resonator frequency	• 1 MHz to 20 MHz (up to 3.6 V) • 1 MHz to 8 MHz (up to 2.4 V)
	External clock input frequency	Up to 20 MHz
	External resonator or additional circuit: ceramic resonator, crystal	Available
	Connection pins: EXTAL, XTAL	
	Drive capability switching	
	Oscillation stop detection function	
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit: crystal resonator	Available
	Connection pins: XCIN, XCOUT	
	Drive capability switching	
PLL circuit	Input clock source	MOSC
	Input frequency	4 MHz to 12.5 MHz
	Frequency multiplication ratio	Selectable from 8 to 31 (1 step)
	Output pulse frequency division ratio	Selectable from 2, and 4
	PLL output frequency	24 MHz to 64 MHz (output frequency division ratio: 2) 24 MHz to 32 MHz (output frequency division ratio: 4)
High-speed on-chip oscillator (HOCO)	Oscillation frequency	24, 32, 48, 64 MHz
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
	User trimming	Not available
External clock input for JTAG (TCK)	Input clock frequency	Up to 12.5 MHz
External clock input for SWD (SWCLK)	Input clock frequency	Up to 12.5 MHz
Bluetooth-dedicated clock oscillator	Resonator frequency	32 MHz
	additional circuit: crystal	Available
	Connection pins : XTAL1_RF, and XTAL2_RF	
Bluetooth-dedicated low speed clock (BLELOCO)	Oscillation frequency	32.768 kHz
	User trimming	Not available

9. 时钟产生电路

9.1 Overview

MCU提供时钟生成电路。

表9.1和表9.2列出了时钟生成电路规格。图9.1显示了框图，表9.3列出了IO引脚。

Table 9.1 时钟源的时钟生成电路规格

时钟源	Description	Specification
主时钟振荡器(MOSC)	谐振器频率	• 1 MHz to 20 MHz (up to 3.6 V) • 1 MHz to 8 MHz (up to 2.4 V)
	外部时钟输入频率	高达20兆赫
	外部谐振器或附加电路：陶瓷谐振器、晶体	Available
	Connection pins: EXTAL, XTAL	
	驱动能力切换	
	振荡停止检测功能	
Sub-clock oscillator (SOSC)	谐振器频率	32.768 kHz
	外部谐振器或附加电路：晶体谐振器	Available
	Connection pins: XCIN, XCOUT	
	驱动能力切换	
PLL circuit	输入时钟源	MOSC
	输入频率	4 MHz to 12.5 MHz
	倍频比	从8到31可选（1级）
	输出脉冲分频比	可从2和4中选择
	锁相环输出频率	24MHz至64MHz（输出分频比：2）24MHz至32MHz（输出分频比：4）
High-speed on-chip oscillator (HOCO)	振荡频率	24, 32, 48, 64 MHz
	用户修剪	Available
Middle-speed on-chip oscillator (MOCO)	振荡频率	8 MHz
	用户修剪	Available
Low-speed on-chip oscillator (LOCO)	振荡频率	32.768 kHz
	用户修剪	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	振荡频率	15 kHz
	用户修剪	无法使用
外部时钟输入 JTAG (TCK)	输入时钟频率	高达12.5MHz
外部时钟输入 SWD (SWCLK)	输入时钟频率	高达12.5MHz
蓝牙专用时钟振荡器	谐振器频率	32 MHz
	附加电路：水晶	Available
	连接引脚：XTAL1_RF和XTAL2_RF	
蓝牙专用低速时钟(BLELOCO)	振荡频率	32.768 kHz
	用户修剪	无法使用

Table 9.2 Clock Generation Circuit Specifications for the internal clocks

Parameter	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU, DTC, DMAC, Flash, SRAM	Up to 48 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock A (PCLKA)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (SPI, SCI, SCE5, CRC, GPT bus-clock)	Up to 48 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (DAC12, IIC, DOC, CAC, CAN, AGT, POEG, CTSU, ELC, I/O ports, RTC, WDT, IWDT, ADC14, KINT, USBFS, ACMPLP, and SLCDC)	Up to 32 MHz Division ratios: 1,2, 4, 8, 16, 32, 64
Peripheral module clock C (PCLKC)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (ADC14 conversion clock)	Up to 64 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (GPT count clock)	Up to 64 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Flash interface clock (FCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Flash interface	1 MHz to 32 MHz (P/E) Up to 32 MHz (read) Division ratios: 1, 2, 4, 8, 16, 32, 64
USB clock (UCLK)	HOCO*1/PLL	USBFS	48 MHz
CAN clock (CANMCLK)	MOSC	CAN	1 MHz to 20 MHz
Segment LCD clock (LCDSRCCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO	SLCDC	Up to 64 MHz
AGT clock (AGTSCLK/AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	24, 32, 48, 64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick Timer clock (SYSTICCLK)	LOCO	SysTick Timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK pin	JTAG	Up to 12.5 MHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64, 128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz
Trace clock (TRCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU-OCD	Up to 48 MHz Division ratios: 1, 2, 4
Bluetooth-dedicated clock (BLECK)	Bluetooth-dedicated clock oscillator	BLE	32 MHz
Bluetooth-dedicated low speed clock (BLELOCO)	Bluetooth-dedicated low-speed on-chip oscillator	BLE	32.768 kHz

Table 9.2 内部时钟的时钟生成电路规范

Parameter	时钟源	时钟电源	Specification
系统时钟(ICLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU、故障诊断码、DMAC、闪存、 SRAM	高达48MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
外设模块时钟A(PCLKA)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	外设模块（SPI、SCI、SCE5、CRC、GPT总线时钟）	高达48MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
外设模块时钟B(PCLKB)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	外围模块（DAC12、IIC、DOC、CAC、CAN、AGT、POEG、CTSU、ELC、IO口、RTC、WDT、IWDT、ADC14、 KINT, USBFS, ACMPLP, and SLCDC)	高达32MHz Division ratios: 1,2, 4, 8, 16, 32, 64
外设模块时钟C(PCLKC)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	外设模块（ADC14转换时钟）	高达64MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
外设模块时钟D(PCLKD)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	外围模块（GPT计数时钟）	高达64MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
闪存接口时钟(FCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	闪存接口	1MHz至32MHz(PE)高达32MHz（读取） Division ratios: 1, 2, 4, 8, 16, 32, 64
USB时钟(UCLK)	HOCO*1/PLL	USBFS	48 MHz
CAN时钟(CANMCLK)	MOSC	CAN	1 MHz to 20 MHz
段式LCD时钟(LCDSRCCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO	SLCDC	高达64MHz
AGT clock (AGTSCLK/AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC主时钟(CACMCLK)	MOSC	CAC	高达20兆赫
CAC副时钟(CACSCLK)	SOSC	CAC	32.768 kHz
CACLOCO时钟(CACLCLK)	LOCO	CAC	32.768 kHz
CACMOCO时钟(CACMOCLK)	MOCO	CAC	8 MHz
CACHOCO时钟(CACHCLK)	HOCO	CAC	24, 32, 48, 64 MHz
CACIWDTLOCO时钟(CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick定时器时钟(SYSTICCLK)	LOCO	SysTick Timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK pin	JTAG	高达12.5MHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	高达16MHz Division ratios: 1, 2, 4, 8, 16, 32, 64, 128
串行线时钟(SWCLK)	SWCLK pin	OCD	高达12.5MHz
跟踪时钟(TRCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU-OCD	高达48MHz Division ratios: 1, 2, 4
Bluetooth-dedicated clock (BLECK)	蓝牙专用时钟振荡器	BLE	32 MHz
蓝牙专用低速时钟(BLELOCO)	Bluetooth-dedicated low-speed on-chip oscillator	BLE	32.768 kHz

Note: Restrictions on setting the clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB, ICLK ≥ FCLK
Restrictions on the clock frequency ratio: (N: integer, and up to 64)
ICLK:FCLK = N:1, ICLK:PCLKA = N: 1, ICLK:PCLKB = N: 1
ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N
PCLKB:PCLKC = 1:1 or 1:2 or 1:4 or 2:1 or 4:1 or 8:1
Note: Minimum FCLK frequency is 1 MHz in Programming/Erasure (P/E) mode.
Note 1. Only when USBFS is used as the device controller.

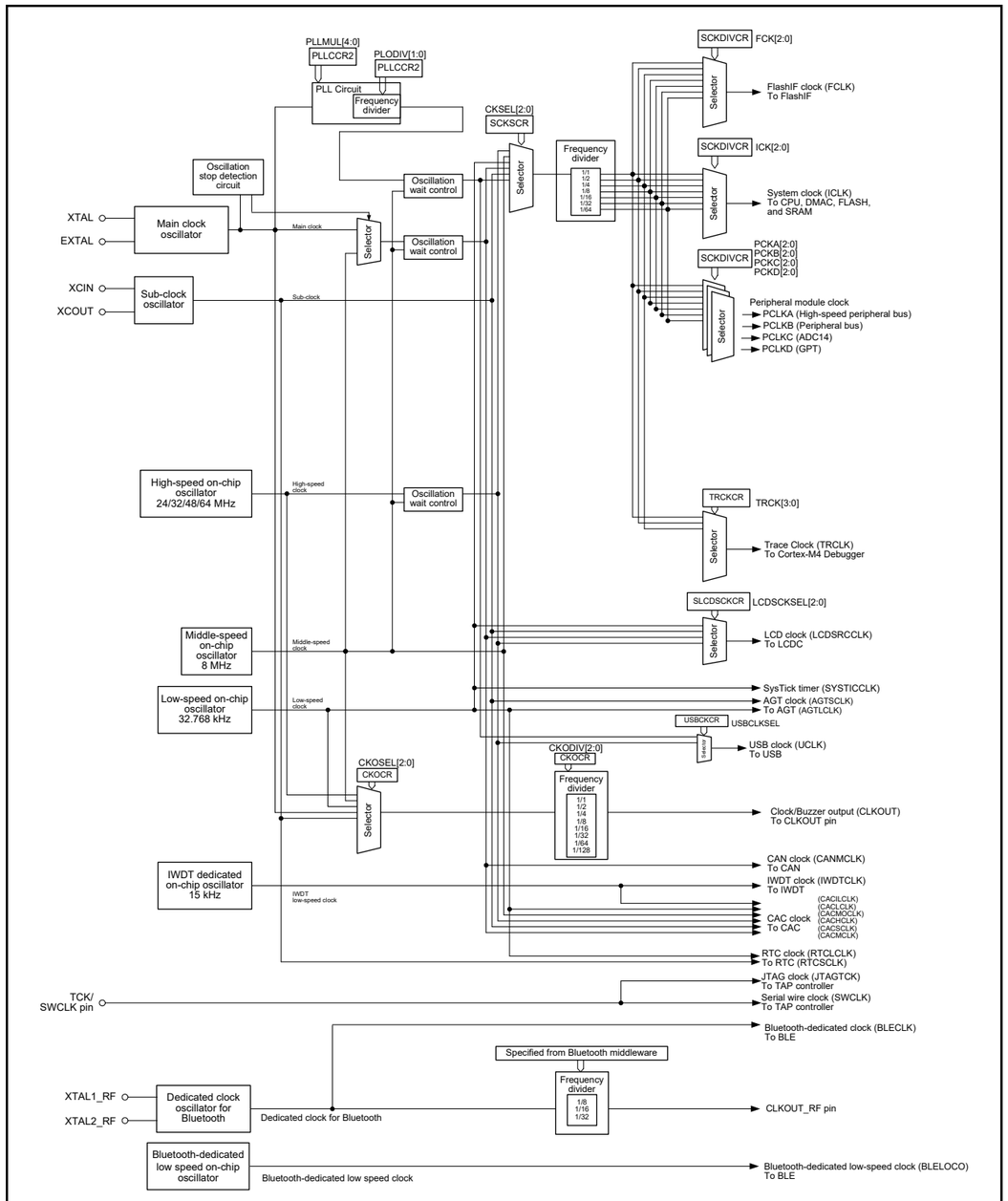


Figure 9.1 Clock generation circuit block diagram

Note: 设置时钟频率的限制：ICLK≥PCLKA≥PCLKB PCLKD≥PCLKA≥PCLKB ICLK≥FCLK
时钟频率比限制：（N：整数，最大为64）
ICLK:FCLK = N:1, ICLK:PCLKA = N: 1, ICLK:PCLKB = N: 1
ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N
PCLKB:PCLKC = 1:1 or 1:2 or 1:4 or 2:1 or 4:1 or 8:1
Note: 在编程擦除(PE)模式下，最小FCLK频率为1MHz。
Note 1. 仅当USBFS用作设备控制器时。

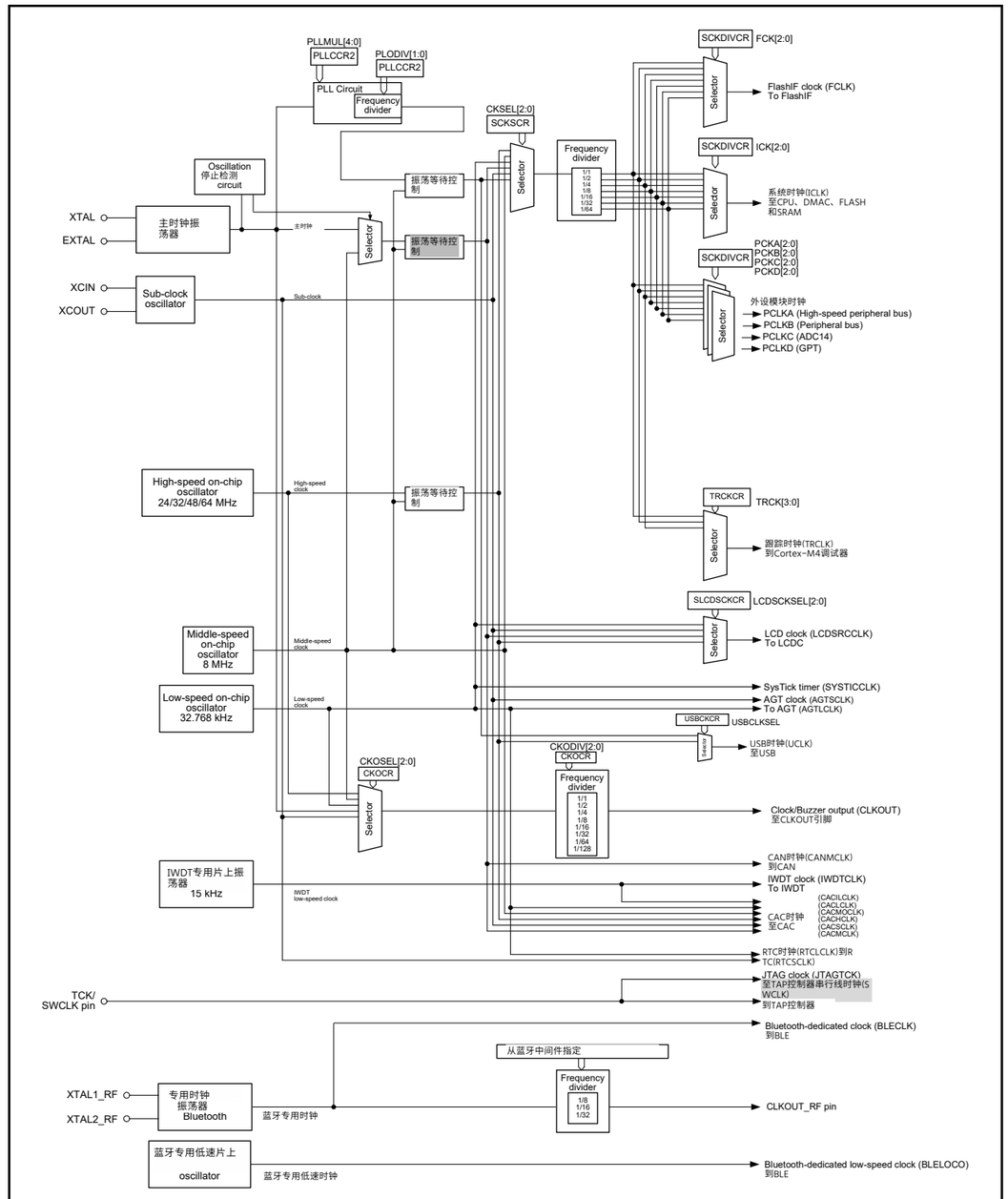


Figure 9.1 时钟产生电路框图

Table 9.3 lists the input and output pins of the clock generation circuit.

Table 9.3 Clock generation circuit input/output pins

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 9.3.2, External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect to a 32.768 kHz crystal resonator
XCOUT	Output	
TCK/SWCLK	Input	This pin is used to input the clock for the JTAG
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock
XTAL1_RF	Input	Connect a 32 MHz oscillator
XTAL2_RF	Output	
CLKOUT_RF	Output	Bluetooth-dedicated clock output pin

9.2 Register Descriptions

9.2.1 System Clock Division Control Register (SCKDIVCR)

Address(es): SYSTEM.SCKDIVCR 4001 E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
Value after reset:	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	PCKD[2:0]	Peripheral Module Clock D (PCLKD) Select*3	b2 b0 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	PCKC[2:0]	Peripheral Module Clock C (PCLKC) Select*3	b6 b4 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

表9.3列出了时钟生成电路的输入和输出引脚。

Table 9.3 时钟生成电路输入输出引脚

引脚名称	I/O	Description
XTAL	Output	这些引脚用于连接晶体谐振器。EXTAL引脚也可用于输入外部时钟。有关详细信息，请参见第9.3.2节，外部时钟输入。
EXTAL	Input	
XCIN	Input	这些引脚用于连接32.768kHz晶体谐振器
XCOUT	Output	
TCK/SWCLK	Input	该引脚用于输入JTAG的时钟
CLKOUT	Output	该引脚用于输出CLKOUTBUZZER时钟
XTAL1_RF	Input	连接32MHz振荡器
XTAL2_RF	Output	
CLKOUT_RF	Output	蓝牙专用时钟输出引脚

9.2 注册说明

9.2.1 系统时钟分频控制寄存器(SCKDIVCR)

Address(es): SYSTEM.SCKDIVCR 4001 E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	—	—	—
重置后的值:	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
重置后的值:	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	PCKD[2:0]	外设模块时钟D(PCLKD)选择*3	b2 b0 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	PCKC[2:0]	外设模块时钟C(PCLKC)选择*3	b6 b4 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b10 to b8	PCKB[2:0]	Peripheral Module Clock B (PCLKB) Select*2	b10 b8 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14 to b12	PCKA[2:0]	Peripheral Module Clock A (PCLKA) Select*2	b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b18 to b16	—	Reserved	These bits should be written the same as PCKB[2:0].	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	ICK[2:0]	System Clock (ICLK) Select*1, *2, *3, *4	b26 b24 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30 to b28	FCK[2:0]	FlashIF Clock (FCLK) Select*1	b30 b28 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The association between the frequencies of the system clock (ICLK) and the flash interface clock (FCLK) should be ICLK:FCLK = N:1 (N: integer)
If a setting is made where ICLK < FCLK, then that setting is ignored.
Note 2. The association between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB) should be ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)
If a setting is made where ICLK < PCLKA or ICLK < PCLKB, then that setting is ignored.
Note 3. The association between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKC, PCLKD) should be ICLK:PCLKC, PCLKD = N:1 or 1:N (N: integer)
Note 4. Selecting division by 1 to ICLK is prohibited when SCKSCR.CKSEL[2:0] bits select the system clock source that is faster than 32 MHz and MEMWAIT.MEMWAIT = 0.

The SCKDIVCR register selects the frequencies of the system clock (ICLK), the peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), and the flash interface clock (FCLK).

PCKD[2:0] bits (Peripheral Module Clock D (PCLKD) Select)

The PCKD[2:0] bits select the frequency of peripheral module clock D (PCLKD).

PCKC[2:0] bits (Peripheral Module Clock C (PCLKC) Select)

The PCKC[2:0] bits select the frequency of peripheral module clock C (PCLKC).

Bit	Symbol	位名称	Description	R/W
b10 to b8	PCKB[2:0]	外设模块时钟B(PCLKB)选择*2	b10 b8 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b14 to b12	PCKA[2:0]	外设模块时钟A(PCLKA)选择*2	b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b18 to b16	—	Reserved	这些位的写入方式应与PCKB[2:0]相同。	R/W
b23 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b24	ICK[2:0]	系统时钟(ICLK)选择*1、*2、*3、*4	b26 b24 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b27	—	Reserved	该位读取为0。写入值应为0。	R/W
b30 to b28	FCK[2:0]	FlashIF Clock (FCLK) Select*1	b30 b28 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 系统时钟(ICLK)和闪存接口时钟(FCLK)的频率之间的关联应该是
ICLK:FCLK = N:1 (N: integer)
如果进行了ICLK<FCLK的设置，则忽略该设置。
Note 2. 系统时钟(ICLK)和外设模块时钟(PCLKA PCLKB)的频率之间的关联应该是ICLK:PCLKA=N:1 ICLK:PCLKB=N:1(N:integer)如果设置如下ICLK<PCLKA或ICLK<PCLKB，则忽略该设置。
Note 3. 系统时钟（ICLK）和外围模块时钟（PCLKC、PCLKD）的频率之间的关联应该是ICLK:PCLKC，PCLKD=N:1或1:N（N:整数）
Note 4. 当SCKSCR.CKSEL[2:0]位选择高于32MHz且MEMWAIT.MEMWAIT=0的系统时钟源时，禁止选择ICLK1分频。

SCKDIVCR寄存器选择系统时钟(ICLK)、外设模块时钟(PCLKA、PCLKB、PCLKC、PCLKD）和闪存接口时钟（FCLK）。

PCKD[2:0]位（外设模块时钟D(PCLKD)选择）

PCKD[2:0]位选择外设模块时钟D(PCLKD)的频率。

PCKC[2:0]位（外设模块时钟C(PCLKC)选择）

PCKC[2:0]位选择外围模块时钟C(PCLKC)的频率。

PCKB[2:0] bits (Peripheral Module Clock B (PCLKB) Select*2)

The PCKB[2:0] bits select the frequency of peripheral module clock B (PCLKB).

PCKA[2:0] bits (Peripheral Module Clock A (PCLKA) Select*2)

The PCKA[2:0] bits select the frequency of peripheral module clock A (PCLKA).

ICK[2:0] bits (System Clock (ICLK) Select*1, *2, *3, *4)

The ICK[2:0] bits select the frequency of the system clock for the CPU, DMAC, and DTC.

FCK[2:0] bits (FlashIF Clock (FCLK) Select*1)

The FCK[2:0] bits select the frequency of the flash interface clock (FCLK).

9.2.2 System Clock Source Control Register (SCKSCR)

Address(es): SYSTEM.SCKSCR 4001 E026h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKSEL[2:0]	Clock Source Select*1	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator (MOSC) 1 0 0: Sub-clock oscillator (SOSC) 1 0 1: PLL. Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Selecting a system clock source that is faster than 32 MHz (system clock source > 32 MHz) is prohibited when the SCKDIVCR.ICK[2:0] bits select division by 1 and MEMWAIT.MEMWAIT = 0.

The SCKSCR register selects the clock source for the system clock.

CKSEL[2:0] bits (Clock Source Select*1)

The CKSEL[2:0] bits select the clock source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- Flash interface clock (FCLK).

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)
- PLL circuit.

The clock sources should be switched when there are no occurring internal asynchronous interrupt.

Transitions to clock sources that are not in operation are prohibited.

PCKB[2:0]位（外设模块时钟B(PCLKB)选择*2）

PCKB[2:0]位选择外设模块时钟B(PCLKB)的频率。

PCKA[2:0]位（外设模块时钟A(PCLKA)选择*2）

PCKA[2:0]位选择外设模块时钟A(PCLKA)的频率。

ICK[2:0]位（系统时钟(ICLK)选择*1、*2、*3、*4）

ICK[2:0]位选择CPU、DMAC和DTC的系统时钟频率。

FCK[2:0]位（FlashIF时钟(FCLK)选择*1）

FCK[2:0]位选择闪存接口时钟(FCLK)的频率。

9.2.2 系统时钟源控制寄存器(SCKSCR)

Address(es): SYSTEM.SCKSCR 4001 E026h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	CKSEL[2:0]	时钟源选择*1	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1：主时钟振荡器（MOSC） 1 0 0: Sub-clock oscillator (SOSC) 01：锁相环。禁止其他设置 。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 禁止选择高于32MHz的系统时钟源（系统时钟源>32MHz），当SCKDIVCR.ICK[2:0]位选择除以1且MEMWAIT.MEMWAIT=0。

SCKSCR寄存器选择系统时钟的时钟源。

CKSEL[2:0]位（时钟源选择*1）

CKSEL[2:0]位选择以下模块的时钟源：

- 系统时钟(ICLK)
- 外围模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）
- 闪存接口时钟(FCLK)。

这些位从以下来源之一中选择：

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- 主时钟振荡器(MOSC)
- Sub-clock oscillator (SOSC)
- PLL circuit.

当没有发生内部异步中断时，应切换时钟源。

禁止转换到未运行的时钟源。

9.2.3 PLL Clock Control Register 2 (PLLCCR2)

Address(es): SYSTEM.PLLCCR2 4001 E02Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	PLODIV[1:0]		—	PLLMUL[4:0]				
Value after reset:	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	PLLMUL[4:0]	PLL Frequency Multiplication Factor Select*1	b4 b0 0 0 1 1 1: × 8 0 1 0 0 0: × 9 0 1 0 0 1: × 10 … 1 1 1 0 1: × 30 1 1 1 1 0: × 31 Other settings are prohibited.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	PLODIV[1:0]	PLL Output Frequency Division Ratio Select*1	b7 b6 0 0: Reserved 0 1: /2 1 0: /4 Other settings are prohibited.	R/W

Note 1. PLLMUL[4:0] and PLODIV[1:0] must be set so that the frequency of the PLL output signal is within the range shown in Table 9.1.

The PLLCCR2 register sets the operation of the PLL circuit. Writing to the PLLCCR2 is prohibited when the PLLCR.PLLSTP bit is 0, that is, when the PLL is operating.

PLLMUL[4:0] bits (PLL Frequency Multiplication Factor Select*1)

The PLLMUL[4:0] bits select the frequency multiplication factor of the PLL circuit.

PLODIV[1:0] bits (PLL Output Frequency Division Ratio Select*1)

The PLODIV[1:0] bits select the frequency division ratio of the PLL output.

9.2.4 PLL Control Register (PLLCR)

Address(es): SYSTEM.PLLCR 4001 E02Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	PLLSTP	PLL Stop Control	0: PLL is operating*1 1: PLL is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When operating the PLL, VCC must be more than 2.4V (VCC ≥ 2.4V), and operation power control mode must be set to High-speed mode or Middle-speed mode.

The PLLCR register controls the operation of the PLL circuit.

9.2.3 PLL时钟控制寄存器2(PLLCCR2)

Address(es): SYSTEM.PLLCCR2 4001 E02Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	PLODIV[1:0]		—	PLLMUL[4:0]				
重置后的值:	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	PLLMUL[4:0]	PLL倍频 因子选择*1	b4b000111:×801000:×9010 01:×10…11101:×3011110:× 31禁止其他设置。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b7, b6	PLODIV[1:0]	PLL输出分频 比率选择*1	b7 b6 0 0: Reserved 0 1: /2 10:4禁止其他设置。	R/W

注1.PLLMUL[4:0]和PLODIV[1:0]必须设置为使PLL输出信号的频率在表9.1所示的范围内。PLLCCR2寄存器设置PLL电路的操作。禁止写入PLLCCR2时

PLLCR.PLLSTP位为0，即当PLL工作时。

PLLMUL[4:0]位（PLL倍频因子选择*1）

PLLMUL[4:0]位选择PLL电路的倍频因子。

PLODIV[1:0]位（PLL输出分频比选择*1）

PLODIV[1:0]位选择PLL输出的分频比。

9.2.4 PLL控制寄存器(PLLCR)

Address(es): SYSTEM.PLLCR 4001 E02Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	PLLSTP	PLL停止控制	0：PLL正在运行*11 ：PLL停止。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

注1.运行PLL时，VCC必须大于2.4V（VCC≥2.4V），并且运行功率控制模式必须设置为高速模式或中速模式。

PLLCR寄存器控制PLL电路的操作。

PLLSTP bit (PLL Stop Control)

The PLLSTP bit starts or stops the PLL circuit.

After setting the PLLSTP bit to 0, confirm that the OSCSF.PLLSF bit is set to 1 before using the PLL clock. A fixed stabilization wait is required after setting the PLL to start operation. A fixed wait for the oscillations to stop is also required after stopping the PLL operation.

The following constraints apply when starting and stopping the PLL operation:

- After stopping the PLL, confirm that the OSCSF.PLLSF bit is 0 before restarting the PLL
- Confirm that the PLL is in operation and that the OSCSF.PLLSF bit is 1 before stopping the PLL
- Regardless of whether the PLL clock is selected as the system clock, after setting the PLL to start operation, confirm that the OSCSF.PLLSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the PLL, confirm that the OSCSF.PLLSF bit is set to 0 before executing the WFI instruction.

Writing 1 to PLLSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL).

Make sure the following conditions apply before writing 0 to PLLSTP:

- OSCSF.MOSCSF bit is 1
- At least 4 µs has elapsed after PLLSTP is set to 1 (PLL is stopped)
- At least 1 µs has elapsed after PLLMUL[4:0] bits are set (to select the PLL frequency multiplication).

9.2.5 Memory Wait Cycle Control Register (MEMWAIT)

Address(es): SYSTEM.MEMWAIT 4001 E031h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MEMWAIT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MEMWAIT	Memory Wait Cycle Select	0: No wait 1: Wait.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing 0 to the MEMWAIT bit is prohibited when SCKDIVCR.ICK selects division by 1 and the SCKSCR.CKSEL[2:0] bits select the system clock source that is faster than 32 MHz (ICLK > 32 MHz).

This register controls the wait cycle of flash read access.

MEMWAIT bit (Memory Wait Cycle Select)

The MEMWAIT bit selects the wait cycle of flash read access. The wait cycle of flash access is set to no wait (MEMWAIT = 0) after a reset is released.

Before writing to the MEMWAIT bit, check the ICLK frequency and operation power control mode. The following constraints apply when setting the ICLK and operation power control mode, and the MEMWAIT bit:

- When setting the ICLK to faster than 32 MHz (ICLK > 32 MHz), set MEMWAIT to 1 while ICLK is 32 MHz or less (ICLK ≤ 32 MHz) and the operation power control mode is High-speed mode (OPCCR.OPCM[1:0] = 00b).
  Setting MEMWAIT to 1 is prohibited in operation modes other than High-speed mode.
  Setting the ICLK faster than 32 MHz is prohibited while MEMWAIT = 0.
- When setting the ICLK from 32 MHz or faster (ICLK > 32 MHz) to 32 MHz or less (ICLK ≤ 32 MHz), the ICLK frequency must be set to 32 MHz or less while MEMWAIT = 1.

PLLSTP位（PLL停止控制）

PLLSTP位启动或停止PLL电路。

将PLLSTP位设置为0后，在使用PLL时钟之前确认OSCSF.PLLSF位设置为1。将PLL设置为开始操作后，需要一个固定的稳定等待。停止PLL操作后，还需要固定等待振荡停止。

启动和停止PLL操作时适用以下约束：

- 停止PLL后，在重启PLL之前确认OSCSF.PLLSF位为0
- 在停止PLL之前确认PLL正在运行并且OSCSF.PLLSF位为1
- 无论是否选择PLL时钟作为系统时钟，在设置PLL开始运行后，确认OSCSF.PLLSF设置为1，然后再执行WFI指令将MCU置于软件待机模式
- 当转换到软件待机模式是按照设置停止PLL时，确认OSCSF.PLLSF位在执行WFI指令之前设置为0。

在以下情况下禁止向PLLSTP写入1：

- SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）。

在将0写入PLLSTP之前，请确保满足以下条件：

- OSCSF.MOSCSF位为1
- PLLSTP设置为1（PLL停止）后至少经过4µs
- 设置PLLMUL[4:0]位（以选择PLL倍频）后至少经过1µs。

9.2.5 内存等待周期控制寄存器(MEMWAIT)

Address(es): SYSTEM.MEMWAIT 4001 E031h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MEMWAIT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MEMWAIT	内存等待周期选择	0：不等待 1：等待。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 当SCKDIVCR.ICK选择除以1并且SCKSCR.CKSEL[2:0]位选择高于32MHz(ICLK>32MHz)的系统时钟源时，禁止向MEMWAIT位写入0。

该寄存器控制闪存读取访问的等待周期。

MEMWAIT位（内存等待周期选择）

MEMWAIT位选择闪存读取访问的等待周期。释放复位后，闪存访问的等待周期设置为无等待(MEMWAIT=0)。

在写入MEMWAIT位之前，请检查ICLK频率和操作功率控制模式。设置ICLK和操作电源控制模式以及MEMWAIT位时，适用以下约束：

- 将ICLK设置为快于32MHz(ICLK>32MHz)时，将MEMWAIT设置为1，同时ICLK为32MHz或更低(ICLK≤32MHz)并且操作功率控制模式为高速模式(OPCCR.OPCM[1:0]=00b)。在高速模式以外的操作模式中禁止将MEMWAIT设置为1。
  当MEMWAIT=0时，禁止将ICLK设置为高于32MHz。
- 将ICLK从32MHz或更快(ICLK>32MHz)设置为32MHz或更低(ICLK≤32MHz)时，ICLK频率必须设置为32MHz或更低，同时MEMWAIT=1。

Setting MEMWAIT to 0 is prohibited while ICLK is faster than 32 MHz. Setting MEMWAIT to 1 is prohibited in operation modes other than High-speed mode. MEMWAIT can be set to 0 while the ICLK frequency is 32 MHz or less and operation power control mode is High-speed mode (OPCCR.OPCM[1:0] = 00b).

Table 9.4 MEMWAIT bit setting

MEMWAIT bit	MCU operation power control		
		High-speed mode	
	Mode: except High-speed mode	ICLK ≤ 32 MHz	ICLK > 32 MHz
0	✓	✓	×
1	×	✓	✓

✓: Setting is possible.
×: Setting is not possible.

Figure 9.2 shows an example flow when setting the ICLK faster than 32 MHz.

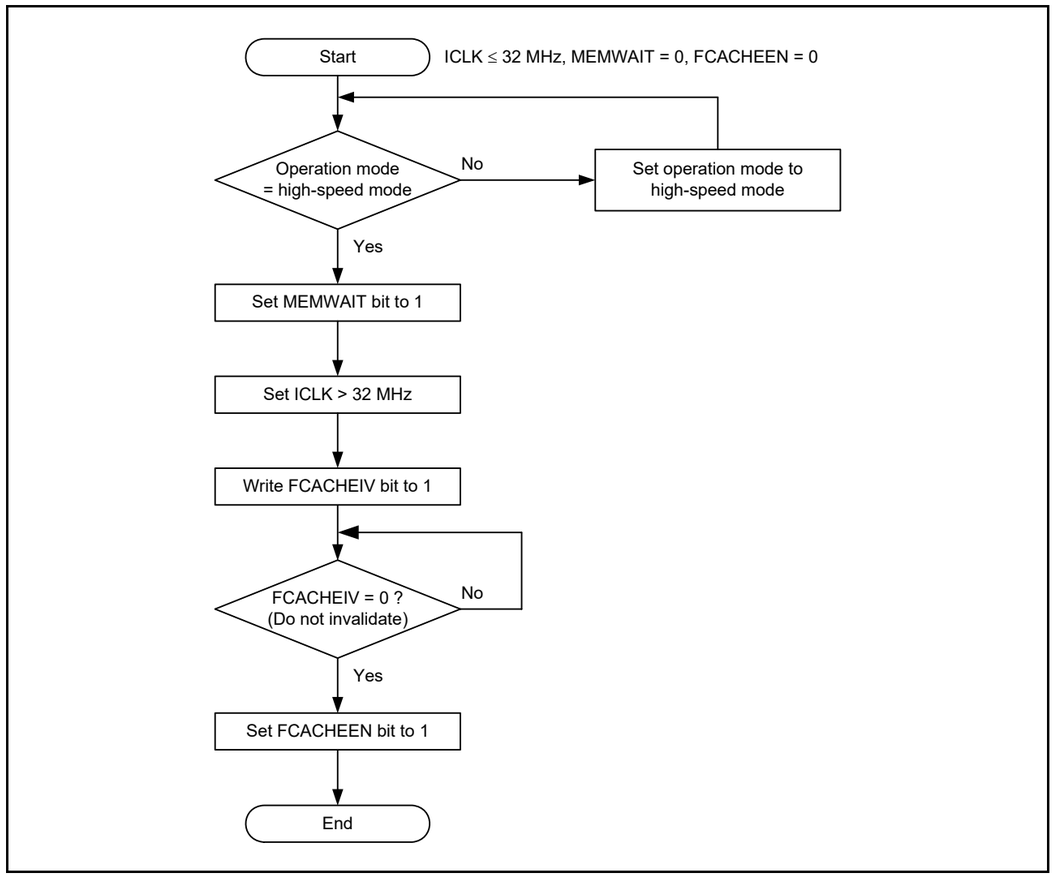


Figure 9.2 When setting the ICLK > 32 MHz

Figure 9.3 shows an example of setting the ICLK less than or equal to 32 MHz when ICLK is greater than 32 MHz.

当ICLK快于32MHz时，禁止将MEMWAIT设置为0。在高速模式以外的操作模式中禁止将MEMWAIT设置为1。当ICLK频率为32MHz或更低且工作功率控制模式为高速模式(OPCCR.OPCM[1:0]=00b)时，可以将MEMWAIT设置为0。

Table 9.4 MEMWAIT位设置

MEMWAIT bit	MCU操作电源控制		
		High-speed mode	
	模式：高速模式除外	ICLK ≤ 32 MHz	ICLK > 32 MHz
0	✓	✓	×
1	×	✓	✓

:可以设置。×：无法设定。图9.2显示了将ICLK设置为快于32MHz时的示例流程。

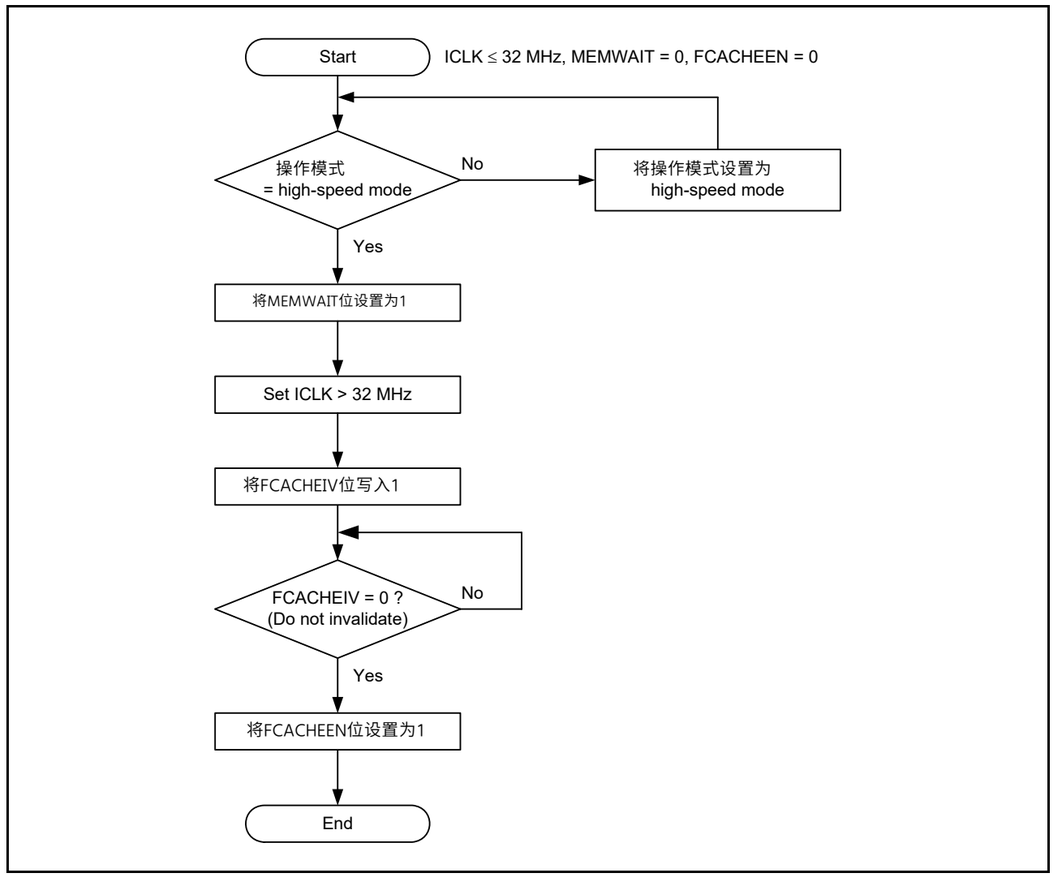


Figure 9.2 当设置ICLK>32MHz

图9.3显示了当ICLK大于32MHz时将ICLK设置为小于或等于32MHz的示例。

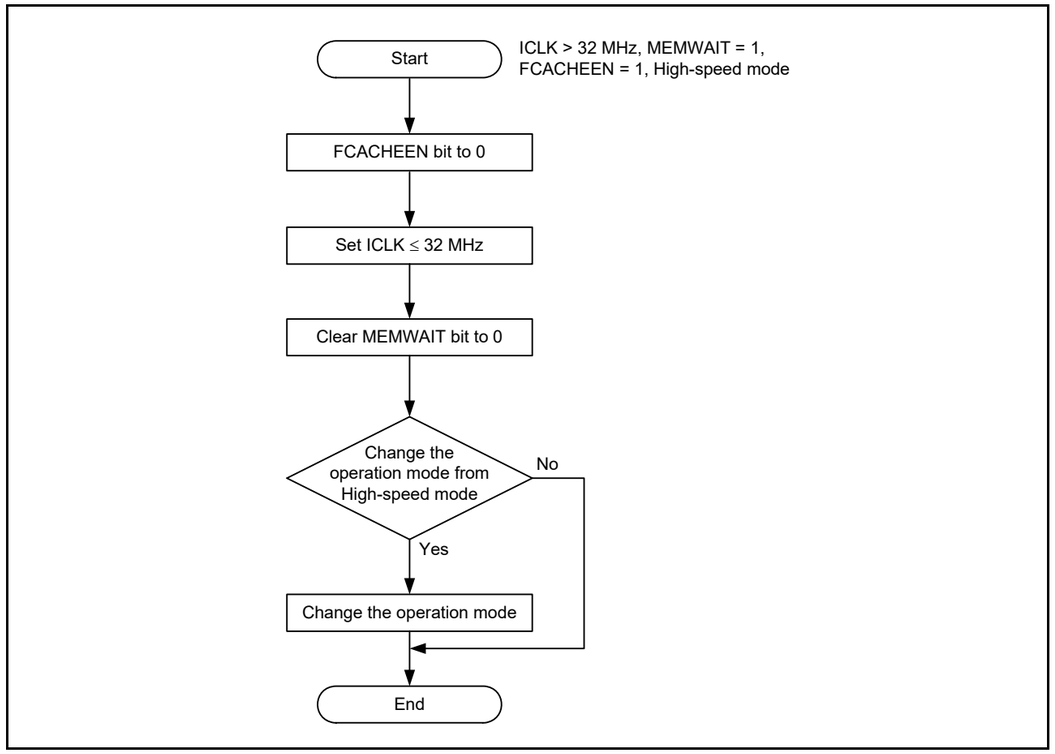


Figure 9.3 When setting the ICLK ≤ 32 MHz from ICLK > 32 MHz

9.2.6 Main Clock Oscillator Control Register (MOSCCR)

Address(es): SYSTEM.MOSCCR 4001 E032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Operate the main clock oscillator*1 1: Stop the main clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator.

The main clock oscillator can be started by setting the MOSTP bit to operate. When changing the value of the MOSTP bit, execute subsequent instructions only after reading the bit to check that its value is updated.

When using the main clock, the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set before setting MOSTP to 0. When the

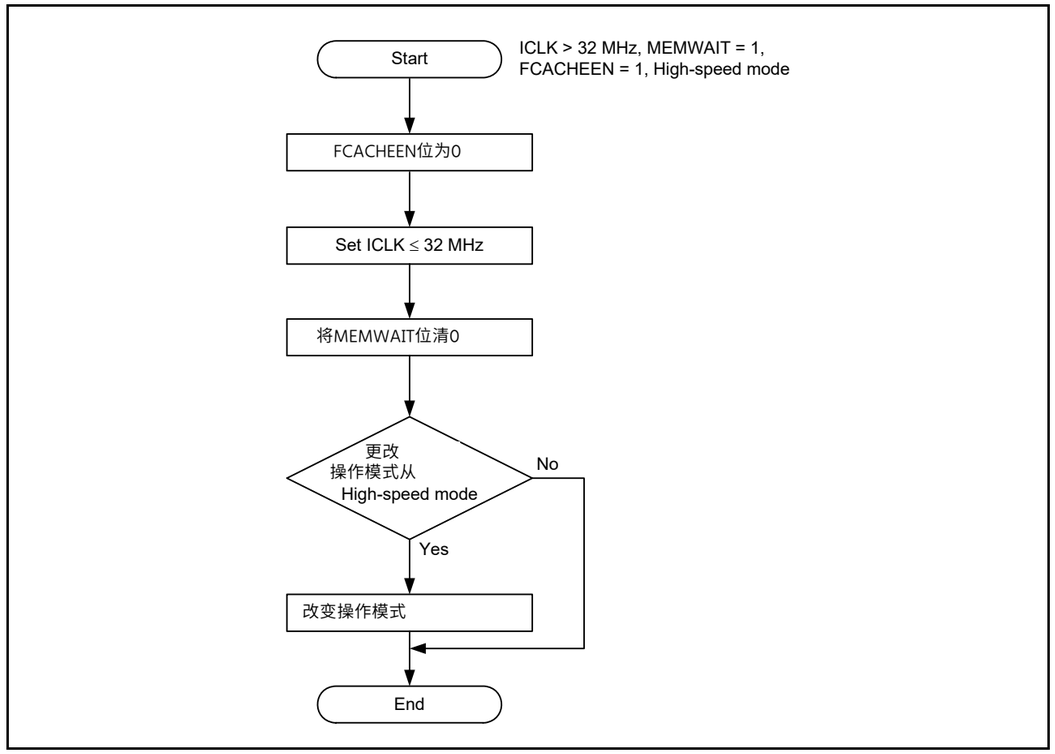


Figure 9.3 当从ICLK>32MHz设置ICLK≤32MHz

9.2.6 主时钟振荡器控制寄存器(MOSCCR)

Address(es): SYSTEM.MOSCCR 4001 E032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	MOSTP	主时钟振荡器停止	0：运行主时钟振荡器*11：停止主时钟振荡器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在将MOSTP设置为0之前，必须设置MOMCR寄存器。

MOSCCR寄存器控制主时钟振荡器。

MOSTP位（主时钟振荡器停止）

MOSTP位启动或停止主时钟振荡器。

可以通过设置MOSTP位来启动主时钟振荡器以进行操作。更改MOSTP位的值时，仅在读取该位后执行后续指令以检查其值是否已更新。

使用主时钟时，主时钟振荡器模式振荡控制寄存器(MOMCR)和主时钟
必须在将MOSTP设置为0之前设置时钟振荡器等待控制寄存器(MOSCWTCR)。当

MOSCCR.MOSTP bit setting is modified for the main clock to run, only use the main clock after confirming that the OSCSF.MOSCSF bit is set to 1.

A fixed time is required for oscillation to become stable after setting the main clock oscillator. A fixed time is also required for oscillation to stop after stopping the main clock oscillator.

The following restrictions apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby modes
- When a transition to Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC)
- SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCR.PLLSTP = 0 (PLL operates).

9.2.7 Sub-Clock Oscillator Control Register (SOSCCR)

Address(es): SYSTEM.SOSCCR 4001 E480h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	SOSTP	Sub-Clock Oscillator Stop	0: Operate the sub-clock oscillator*1, *2 1: Stop the sub-clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The SOMCR register must be set before setting SOSTP to 0.
Note 2. The VBTCR1.BPWSWSTP bit must be set before setting the SOSC to operate when the VBATT function is not used. For VBTCR1.BPWSWSTP, see section 12, Battery Backup Function.

The SOSCCR register controls the sub-clock oscillator.

SOSTP bit (Sub-Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator.

When changing the value of the SOSTP bit, execute subsequent instructions after reading the bit and checking that its value is updated. When the sub clock is used as the source for some modules for example, RTC, use the SOSTP bit.

When using the sub-clock oscillator, set the Sub Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0. After setting SOSTP to 0, use the sub-clock oscillator only after the sub-clock oscillation stabilization time (tSUBOSCOWT) elapses. A fixed time for stabilization is required for oscillation to become stable after selecting the sub-clock operation with the SOSTP bit. A fixed time is also required for oscillation to actually stop after setting the SOSTP bit.

The following restrictions apply when starting and stopping operation:

- When restarting the sub-clock oscillator after it stops, allow an interval of at least 5 SOSC clock cycles for it to remain stopped.

MOSCCR.MOSTP位设置修改为主时钟运行，确认后才使用主时钟
OSCSF.MOSCSF位设置为1。

设置主时钟振荡器后，振荡稳定需要一定的时间。停止主时钟振荡器后，振荡停止也需要一段固定的时间。

启动和停止操作时适用以下限制：

- 停止主时钟振荡器后，在重新启动主时钟振荡器之前确认OSCSF.MOSCSF位为0
- 在停止主时钟振荡器之前，确认主时钟振荡器工作并且OSCSF.MOSCSF位为1
- 无论是否选择主时钟振荡器作为系统时钟，在执行WFI指令之前确认OSCSF.MOSCSF位设置为1以将MCU置于软件待机模式
- 当转换到软件待机模式是按照设置停止主时钟振荡器时，在执行WFI指令之前确认OSCSF.MOSCSF位设置为0。

在以下情况下禁止向MOSTP写入1：

- SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）
- SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）
- PLLCR.PLLSTP = 0 (PLL operates).

9.2.7 副时钟振荡器控制寄存器(SOSCCR)

Address(es): SYSTEM.SOSCCR 4001 E480h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SOSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	SOSTP	副时钟振荡器停止	0：运行副时钟振荡器*1，*21：停止副时钟振荡器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在将SOSTP设置为0之前，必须设置SOMCR寄存器。
Note 2. 当不使用VBATT功能时，必须在设置SOSC之前设置VBTCR1.BPWSWSTP位。为了VBTCR1.BPWSWSTP，见第12节，电池备份功能。

SOSCCR寄存器控制副时钟振荡器。

SOSTP位（副时钟振荡器停止）

SONTP位启动或停止副时钟振荡器。

更改SONTP位的值时，请在读取该位并检查其值是否已更新后执行后续指令。当子时钟用作某些模块（例如RTC）的源时，请使用SOSTP位。

使用副时钟振荡器时，请在设置前设置副时钟振荡器模式控制寄存器(SOMCR)
SOSTP为0。将SOSTP设置为0后，仅在副时钟振荡稳定时间(tSUBOSCOWT)过后才使用副时钟振荡器。通过SOTP位选择子时钟操作后，振荡稳定需要一段固定的时间。在设置SOTP位后，振荡实际停止也需要一个固定的时间。

启动和停止操作时适用以下限制：

- 子时钟振荡器停止后重新启动时，至少要间隔5个SOSC时钟周期，以使其保持停止状态。

- Confirm that the sub-clock oscillator is stable when setting the sub-clock oscillator to stop.
- Regardless of whether the sub-clock oscillator is selected as the system clock, ensure that oscillation by the sub-clock oscillator is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least 3 SOSC clock cycles after setting the sub-clock oscillator to stop and before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

9.2.8 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): SYSTEM.LOCOCR 4001 E490h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	LCSTP	LOCO Stop	0: Operate the LOCO clock*1 1: Stop the LOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The VBTCR1.BPWSWSTP bit must be set before setting the LOCO to operate when VBATT function is not used. For details on VBTCR1.BPWSWSTP, see section 12, Battery Backup Function.

The LOCOCR register controls the LOCO.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO.

After the LCSTP bit is modified to operate the LOCO, only use the clock after the LOCO clock-oscillation stabilization wait time (tLOCOWT) elapses. A fixed time for stabilization of oscillation is required for oscillation to become stable after setting the LOCO clock to start operation. A fixed time is also required for oscillation to stop after setting the oscillator.

The following restrictions apply when starting and stopping operation:

- When restarting the LOCO after it stops, allow an interval of at least 5 LOCO clock cycles for it to remain stopped
- Ensure that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO is selected as the system clock, ensure that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO cycles before executing the WFI instruction.

Writing 1 to LOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

- 设置副时钟振荡器停止时，确认副时钟振荡器稳定。
- 无论是否选择副时钟振荡器作为系统时钟，在执行WFI指令将MCU置于软件待机模式之前，请确保副时钟振荡器的振荡稳定
- 当根据设置转换到软件待机模式以停止副时钟振荡器时，在将副时钟振荡器设置为停止之后和执行WFI指令之前等待至少3个SOSC时钟周期。

在以下情况下禁止向SOTP写入1：

- SCKSCR.CKSEL[2:0]=100b（系统时钟源=SOSC）。

9.2.8 低速片上振荡器控制寄存器(LOCOCR)

Address(es): SYSTEM.LOCOCR 4001 E490h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	LCSTP	机车站	0：运行LOCO时钟*11：停止LOCO时钟。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当不使用VBATT功能时，必须在设置LOCO之前设置VBTCR1.BPWSWSTP位。有关VBTCR1.BPWSWSTP的详细信息，请参见第12节，电池备份功能。

LOCOCR寄存器控制LOCO。

LCSTP位（LOCO停止）

LCSTP位启动或停止LOCO。

在修改LCSTP位以操作LOCO后，仅在LOCO时钟振荡稳定等待时间(tLOCOWT)过去后使用时钟。在将LOCO时钟设置为开始工作后，振荡稳定需要一段固定的时间。在设置振荡器后，振荡停止也需要一个固定的时间。

启动和停止操作时适用以下限制：

- 在LOCO停止后重新启动时，请允许至少5个LOCO时钟周期的间隔以使其保持停止状态
- 在停止LOCO时钟之前确保LOCO振荡稳定
- 无论是否选择LOCO作为系统时钟，在执行WFI指令将MCU置于软件待机模式之前，请确保LOCO振荡稳定
- 当转换到软件待机模式是按照设置停止LOCO时钟时，至少等待3 LOCO在执行WFI指令之前循环。

在以下情况下禁止向LOSTP写入1：

- SCKSCR.CKSEL[2:0]=010b（系统时钟源=LOCO）。

9.2.9 High-Speed On-Chip Oscillator Control Register (HOCOCR)

Address(es): SYSTEM.HOCOCR 4001 E036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2, *3 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).
Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).
Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO. If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.
Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP bit must always be 0.

The HOCOCR register controls the HOCO.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO. For the HOCO to operate, the High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR) must also be set.

After the HCSTP bit setting is modified to run the HOCO, confirm that the OSCSF.HOCOSF is set to 1 before using the oscillator. When OFS1.HOCOEN is set to 1, confirm that the OSCSF.HOCOSF is also set to 1 before using the HOCO clock. A fixed time for stabilization is required for oscillation to become stable after setting the HOCO operation. A fixed time is also required for oscillation to actually stop after setting the HOCO clock to stop.

The following restrictions apply when starting and stopping operation:

- After stopping the HOCO, confirm that the OSCSF.HOCOSF bit is 0 before restarting the HOCO
- Confirm that the HOCO operates and that the OSCSF.HOCOSF bit is 1 before stopping the HOCO
- Regardless of whether the HOCO is selected as the system clock, confirm that the OSCSF.HOCOSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting of the HOCO to stop, confirm that the OSCSF.HOCOSF bit is set to 0 after setting the HOCO and before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO).

9.2.9 高速片上振荡器控制寄存器(HOCOCR)

Address(es): SYSTEM.HOCOCR 4001 E036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
重置后的值：	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	位名称	Description	R/W
b0	HCSTP	HOCO Stop	0：运行HOCO时钟*2、*31：停止HOCO时钟。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 当HOCOCR.HCSTP=0且OSCSF.HOCOSF=0（HOCO处于稳定等待计数中）时，禁止写入OPCCR.OPCM[1:0]。

Note: 当OPCCR.OPCMTSF=1或SOPCCR.SOPCMTSF=1（工作电源控制模式转换期间）或FLSTOP.CFLSTOPF=1（闪存转换期间）时，禁止写入HCSTP。
Note 1. 当OFS1.HOCOEN位为0时复位后的HCSTP位值为0。当OFS1.HOCOEN位为1时为1。
Note 2. 如果HOCO的工作频率为48MHz，则在操作HOCO时，VCC必须大于1.8V（VCC≥1.8V）。如果HOCO的工作频率为64MHz，则在操作HOCO时，VCC必须大于2.4V（VCC≥2.4V）。
Note 3. 使用HOCO(HCSTP=0)时，必须将OFS1.HOCOFRQ1位设置为最佳值。在低电压模式下，HOCOCR.HCSTP位必须始终为0。

HOCOCR寄存器控制HOCO。

HCSTP位（HOCO停止）

HCSTP位启动或停止HOCO。为了使HOCO运行，高速片上振荡器等待控制还必须设置寄存器(HOCOWTCR)。

修改HCSTP位设置以运行HOCO后，在使用振荡器之前确认OSCSF.HOCOSF设置为1。当OFS1.HOCOEN设置为1时，在使用HOCO时钟之前确认OSCSF.HOCOSF也设置为1。在设置HOCO操作后，振荡稳定需要一段固定的时间。在将HOCO时钟设置为停止后，振荡实际停止也需要一个固定的时间。

启动和停止操作时适用以下限制：

- 停止HOCO后，确认OSCSF.HOCOSF位为0再重启HOCO
- 在停止HOCO之前确认HOCO运行并且OSCSF.HOCOSF位为1
- 无论是否选择HOCO作为系统时钟，在执行WFI指令之前确认OSCSF.HOCOSF位设置为1以将MCU置于软件待机模式
- 当转换到软件待机模式是按照HOCO的设置停止时，请确认OSCSF.HOCOSF位在设置HOCO之后和执行WFI指令之前设置为0。

在以下情况下禁止向HCSTP写入1：

- SCKSCR.CKSEL[2:0]=000b（系统时钟源=HOCO）。

9.2.10 Middle-Speed On-Chip Oscillator Control Register (MOCOCR)

Address(es): SYSTEM.MOCOCR 4001 E038h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MCSTP	MOCO Stop	0: Operate MOCO 1: Stop MOCO.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MOCOCR register controls the MOCO.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO.

After setting MCSTP to 0, use the MOCO clock only after the MOCO clock oscillation stabilization time (tMOCOWT) elapses. A fixed time for stabilization of oscillation is required after setting MCSTP to 0. A fixed time is also required for oscillation to stop after setting MCSTP to 1.

The following are limitations when starting and stopping the oscillator:

- When restarting the MOCO after it has been stopped, allow a stop interval of at least 5 MOCO clocks cycle for it to remain stopped
- Ensure that MOCO oscillation is stable when setting the MOCO to stop
- Regardless of whether the MOCO is selected as the system clock, ensure that MOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Enable bit (OSTDCR.OSTDE) in the Oscillation Stop Detection Control Register.

Because the MOCO clock is used to measure the waiting time for other oscillators, the MOCO clock oscillates when the waiting time for other oscillators is measured, regardless of the setting of MOCOCR.MCSTP. The MOCO clock may be unintentionally supplied even when the MCSTP is set to stop.

9.2.11 Oscillation Stabilization Flag Register (OSCSF)

Address(es): SYSTEM.OSCSF 4001 E03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HOCOSF	HOCO Clock Oscillation Stabilization Flag	0: The HOCO clock is stopped or is not yet stable 1: The HOCO clock is stable, so is available for use as the system clock.	R

9.2.10 中速片上振荡器控制寄存器(MOCOCR)

Address(es): SYSTEM.MOCOCR 4001 E038h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MCSTP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MCSTP	MOCO Stop	0：运行MOCO1： 停止MOCO。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

MOCOCR寄存器控制MOCO。

MCSTP位（MOCO停止）

MCSTP位启动或停止MOCO。

将MCSTP设置为0后，仅在MOCO时钟振荡稳定时间(tMOCOWT)过去后使用MOCO时钟。将MCSTP设置为0后需要固定的振荡稳定时间。将MCSTP设置为1后也需要固定的时间停止振荡。

以下是启动和停止振荡器时的限制：

- 在MOCO停止后重新启动时，允许至少5个MOCO时钟周期的停止间隔使其保持停止状态
- 设置MOCO停止时，确保MOCO振荡稳定
- 无论是否选择MOCO作为系统时钟，在执行WFI指令之前确保MOCO振荡稳定，将MCU置于软件待机模式
- 当转换到软件待机模式是按照设置停止MOCO时钟时，至少等待3
执行WFI指令之前的MOCO时钟周期。

在以下情况下禁止向MCSTP写入1：

- SCKSCR.CKSEL[2:0]=001b（系统时钟源=MOCO）。

如果在Oscillation中使能了振荡停止检测，则禁止向MCSTP位写入1（停止MOCO）
振荡停止检测控制寄存器中的停止检测使能位(OSTDCR.OSTDE)。

因为MOCO时钟用于测量其他振荡器的等待时间，所以无论MOCOCR.MCSTP的设置如何，MOCO时钟都会在测量其他振荡器的等待时间时振荡。即使将MCSTP设置为停止，也可能会无意中提供MOCO时钟。

9.2.11 振荡稳定标志寄存器(OSCSF)

Address(es): SYSTEM.OSCSF 4001 E03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
重置后的值:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	位名称	Description	R/W
b0	HOCOSF	HOCO时钟振荡稳定标志	0：HOCO时钟停止或尚未稳定1：HOCO时钟稳定，可用作系统时钟。	R

Bit	Symbol	Bit name	Description	R/W
b2, b1	—	Reserved	These bits are read as 0.	R
b3	MOSCSF	Main Clock Oscillation Stabilization Flag	0: The main clock oscillation is stopped (MOSTP = 1) or is not stable yet*2 1: The main clock oscillator is stable, so is available for use as the system clock.	R
b4	—	Reserved	This bit is read as 0.	R
b5	PLLSF	PLL Clock Oscillation Stabilization Flag	0: The PLL clock is stopped or oscillation of the PLL clock has not yet become stable 1: Oscillation of the PLL clock is stable so the clock is available for use as the system clock.	R
b7, b6	—	Reserved	These bits are read as 0.	R

Note 1. Value after reset depends on the OFS1.HOCOEN bit setting.
When OFS1.HOCOEN = 1, OSCSF.HOCOSF value becomes 0 after reset is released, and OSCSF.HOCOSF value becomes 1 after the HOCO oscillation stabilization time is elapses.

Note 2. An appropriate value is set in the Wait Control register for the given oscillator. If the wait time is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

The OSCSF register contains flags to indicate the operation status of the counters in the oscillation stabilization wait circuits for the individual oscillators.

After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating state of the counter that measures the wait time for the high-speed clock oscillator (HOCO).

When OFS1.HOCOEN is set to 1, confirm that the OSCSF.HOCOSF is also set to 1 before using the HOCO clock.

[Setting condition]

- After the HOCO clock stops and the HOCOCR.HCSTP bit is set to 0, supply of the high-speed clock in the MCU starts after the middle-speed clock cycles set in the HOCOWTCR.HSTS[2:0] bits elapse.

[Clearing condition]

- When the high-speed clock oscillator is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating state of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

- After the main clock oscillator stops and the MOSCCR.MOSTP bit is set to 0, supply of the main clock in the MCU starts after the number of middle-speed clock cycles associated with the setting in the MOSCWTCR.MSTS[3:0] bits are counted.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

PLLSF flag (PLL Clock Oscillation Stabilization Flag)

The PLLSF flag indicates the operating state of the counter that measures the wait time of the PLL.

[Setting condition]

- After the PLL stops and the PLLCR.PLLSTP bit is set to 0, supply of the PLL clock in the MCU starts after 370 cycles of the middle-speed clock are counted. If oscillation by the PLL clock source is not stable when the PLLSTP bit is set to 0, counting of the middle-speed clock cycles continues after the oscillation of the PLL clock source is stabilized.

[Clearing condition]

Bit	Symbol	位名称	Description	R/W
b2, b1	—	Reserved	这些位读为0。	R
b3	MOSCSF	主时钟振荡稳定标志	0：主时钟振荡停止（MOSTP=1）或尚未稳定*21：主时钟振荡器稳定，可用作系统时钟。	R
b4	—	Reserved	该位读为0。	R
b5	PLLSF	PLL时钟振荡稳定Flag	0：PLL时钟停止或PLL时钟的振荡尚未稳定1：PLL时钟的振荡稳定，可用作系统时钟。	R
b7, b6	—	Reserved	这些位读为0。	R

Note 1. 复位后的值取决于OFS1.HOCOEN位设置。
当OFS1.HOCOEN=1时，复位解除后OSCSF.HOCOSF值变为0，经过HOCO振荡稳定时间后OSCSF.HOCOSF值变为1。

Note 2. 在给定振荡器的等待控制寄存器中设置了一个适当的值。如果等待时间不够，则将振荡稳定标志设置为1，并在振荡稳定之前开始向内部电路提供时钟信号。

OSCSF寄存器包含用于指示各个振荡器的振荡稳定等待电路中的计数器的操作状态的标志。

振荡开始后，这些计数器测量等待时间，直到每个振荡器输出时钟被提供给内部电路。计数器溢出表明时钟供应稳定并可用于相关电路。

HOCOSF标志（HOCO时钟振荡稳定标志）

HOCOSF标志指示计数器的操作状态，该计数器测量高速时钟振荡器(HOCO)的等待时间。

当OFS1.HOCOEN设置为1时，在使用HOCO时钟之前确认OSCSF.HOCOSF也设置为1。

[Setting condition]

- 在HOCO时钟停止并且HOCOCR.HCSTP位设置为0后，在经过HOCOWTCR.HSTS[2:0]位设置的中速时钟周期后，MCU中的高速时钟开始供应。

[Clearing condition]

- 当高速时钟振荡器正在运行，然后由于HOCOCR.HCSTP位设置为1而被停用。

MOSCSF标志（主时钟振荡稳定标志）

MOSCSF标志指示测量主时钟振荡器等待时间的计数器的操作状态。

[Setting condition]

- 在主时钟振荡器停止且MOSCCR.MOSTP位设置为0后，MCU中的主时钟在与MOSCWTCR.MSTS[3:0]位设置相关的中速时钟周期数之后开始提供被计算在内。

[Clearing condition]

- 当主时钟振荡器正在运行，然后因为MOSCCR.MOSTP位设置为1而被停用时。

PLLSF标志（PLL时钟振荡稳定标志）

PLLSF标志指示测量PLL等待时间的计数器的操作状态。

[Setting condition]

- 在PLL停止并且PLLCR.PLLSTP位设置为0后，MCU中PLL时钟的供应在中速时钟的370个周期被计数后开始。如果PLLSTP位设置为0时PLL时钟源的振荡不稳定，则在PLL时钟源的振荡稳定后继续计数中速时钟周期。

[Clearing condition]

- When the PLL operates, it is deactivated when the PLLCR.PLLSTP bit is set to 1.

9.2.12 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): SYSTEM.OSTDCR 4001 E040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG).	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Disable the oscillation stop detection function 1: Enable the oscillation stop detection function.	R/W

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is notified to the POEG.

If the Oscillation Stop Detection Flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before OSTDF is set to 0. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. Depending on the number of cycles required to read a given I/O register, a wait time longer than 2 PCLKB cycles might be required.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When this bit is 1 (oscillation stop detection function enabled), the MOCO Stop bit (MOCOCR.MCSTP) is set to 0 and the MOCO operation starts. The MOCO cannot be stopped when the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the Oscillation Stop Detection Flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby mode. To transition to Software Standby mode, first set the OSTDE bit to 0, and then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:

- In Low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, FCLK, PCLKA, PCLKB, PCLKC, PCLKD is prohibited
- In low-voltage mode, selecting division by 1, 2 for ICLK, FCLK, PCLKA, PCLKB, PCLKC, PCLKD is prohibited.

- 当PLL运行时，当PLLCR.PLLSTP位设置为1时，它被禁用。

9.2.12 振荡停止检测控制寄存器(OSTDCR)

Address(es): SYSTEM.OSTDCR 4001 E040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OSTDIE	振荡停止检测中断使能	0：禁止振荡停止检测中断（不通知POEG）1：使能振荡停止检测中断（通知POEG）。	R/W
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	OSTDE	振荡停止检测功能启用	0：禁用振荡停止检测功能1：启用振荡停止检测功能。	R/W

OSTDCR寄存器控制振荡停止检测功能。

OSTDIE位（振荡停止检测中断使能）

OSTDIE位使能振荡停止检测功能中断。它还控制是否将振荡停止检测通知给POEG。

如果振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志需要清零，请在OSTDF设置为0之前将OSTDIE位设置为0。在将OSTDIE位设置为1之前等待至少2个PCLKB周期。取决于根据读取给定IO寄存器所需的周期数，可能需要超过2个PCLKB周期的等待时间。

OSTDE位（振荡停止检测功能使能）

OSTDE位使能振荡停止检测功能。

当该位为1时（使能振荡停止检测功能），MOCO停止位(MOCOCR.MCSTP)设置为0并开始MOCO操作。当振荡停止检测功能启用时，MOCO不能停止。将1写入MOCOCR.MCSTP位（MOCO停止）无效。

当振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志为1（检测到主时钟振荡停止）时，向OSTDE位写入0无效。

在转换到软件待机模式之前，必须将OSTDE位设置为0。要转换到软件待机模式，首先将OSTDE位设置为0，然后执行WFI指令。

使用振荡停止检测功能时有以下限制：

- 在低速模式下，禁止选择ICLK、FCLK、PCLKA、PCLKB、PCLKC、PCLKD的1、2、4、8分频
- 在低电压模式下，禁止为ICLK、FCLK、PCLKA、PCLKB、PCLKC、PCLKD选择1、2分频。

9.2.13 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): SYSTEM.OSTDSR 4001 E041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit can only be set to 0.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF flag is set to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading OSTDF as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 and then returns to 1.

OSTDSR.OSTDF cannot be set to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillation is stopped when OSTDCR.OSTDE is 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are neither 011b (system clock is MOSC) nor 101b (system clock is PLL).

9.2.13 振荡停止检测状态寄存器(OSTDSR)

Address(es): SYSTEM.OSTDSR 4001 E041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OSTDF	振荡停止检测标志	0：未检测到主时钟振荡停止1：检测到主时钟振荡停止。	R(/W)*1
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位只能设置为0。

OSTDSR寄存器指示主时钟振荡器的停止检测状态。

OSTDF标志（振荡停止检测标志）

OSTDF标志指示主时钟振荡器状态。该标志为1时，表示检测到主时钟振荡停止。检测到此停止后，即使重新启动主时钟振荡，OSTDF标志也不会设置为0。OSTDF标志在读取为1后通过写入0设置为0。

从向OSTDF写入0到将OSTDF读取为0之间至少需要3个ICLK周期的等待时间。如果在主时钟振荡停止时将OSTDF标志设置为0，则OSTDF标志变为0，然后返回1。

在以下情况下，OSTDSR.OSTDF不能设置为0：

- SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

将时钟源切换到主时钟振荡器以外的源后，必须将OSTDF标志设置为0，并且
PLL.

[Setting condition]

- 当OSTDCR.OSTDE为1时（使能振荡停止检测功能），主时钟振荡停止。

[Clearing condition]

- 当SCKSCR.CKSEL[2:0]位既不是011b（系统时钟为MOSC）也不是101b（系统时钟为PLL）时，读取1，然后写入0。

9.2.14 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): SYSTEM.MOSCWTCR 4001 E0A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting	b3 b0 0 0 0 0: Wait time = 2 cycles (0.25 µs) 0 0 0 1: Wait time = 1024 cycles (128 µs) 0 0 1 0: Wait time = 2048 cycles (256 µs) 0 0 1 1: Wait time = 4096 cycles (512 µs) 0 1 0 0: Wait time = 8192 cycles (1024 µs) 0 1 0 1: Wait time = 16384 cycles (2048 µs) (value after reset) 0 1 1 0: Wait time = 32768 cycles (4096 µs) 0 1 1 1: Wait time = 65536 cycles (8192 µs) 1 0 0 0: Wait time = 131072 cycles (16384 µs) 1 0 0 1: Wait time = 262144 cycles (32768 µs). Other settings are prohibited. Wait time is calculated at MOCO = 8 MHz (typically 0.125 µs).	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

Set the MSTS[3:0] bits to select the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0000b because the oscillation stabilization time is not required.

The wait time set in the MSTS[3:0] bits is counted using the MOCO clock. The MOCO automatically oscillates when necessary, regardless of the value of the MOCOCR.MCSTP bit. After the set wait time elapses, supply of the main clock starts internally in the MCU, and the OSCSF.MOSCSF flag becomes 1. If the set wait time is short, supply of the main clock starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

9.2.14 主时钟振荡器等待控制寄存器(MOSCWTCR)

Address(es): SYSTEM.MOSCWTCR 4001 E0A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTS[3:0]			
重置后的值:	0	0	0	0	0	1	0	1

Bit	Symbol	位名称	Description	R/W
b3 to b0	MSTS[3:0]	主时钟振荡器等待时间设定	b3 b0 0 0 0 0：等待时间=2个周期(0.25µs) 0 0 0 1：等待时间=1024个周期（128µs） 0 0 1 0：等待时间=2048个周期（256µs） 0 0 1 1：等待时间=4096个周期（512µs） 0 1 0 0：等待时间=8192个周期（1024µs） 0 1 0 1：等待时间=16384个周期（2048µs）（复位后的值） 0 1 1 0：等待时间=32768个周期（4096µs） 0 1 1 1：等待时间=65536个周期（8192µs） 1 0 0 0：等待时间=131072个周期（16384µs） 01：等待时间=262144个周期（32768µs）。禁止 其他设置。 等待时间是在MOCO=8MHz（通常为0.125µs）时计算的。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

MSTS[3:0]位（主时钟振荡器等待时间设置）

设置MSTS[3:0]位以选择主时钟振荡器的振荡稳定等待时间。

将主时钟振荡稳定时间设置为大于或等于振荡器制造商推荐的稳定时间。当主时钟从外部输入时，将这些位设置为0000b，因为不需要振荡稳定时间。

MSTS[3:0]位中设置的等待时间是使用MOCO时钟计算的。MOCO会在必要时自动振荡，无论MOCOCR.MCSTP位的值如何。在设置的等待时间过去后，主时钟在MCU内部开始供应，并且OSCSF.MOSCSF标志变为1。如果设置的等待时间短，则在时钟振荡稳定之前开始供应主时钟。

仅当MOSCCR.MOSTP位为1且OSCSF.MOSCSF标志为0时才重写MOSCWTCR寄存器。在任何其他情况下请勿重写此寄存器。

9.2.15 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR)

Address(es): SYSTEM.HOCOWTCR 4001 E0A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	HSTS[2:0]	HOCO wait time setting	b2 b0 1 0 1: • Wait time = 245 cycles (29.13 µs) When HOCO operating frequency is 24 MHz or 32 MHz, and the operation power control mode is other than low-voltage mode. • Wait time = 287 cycles (35.875 µs) (value after reset) when HOCO operating frequency is 48 MHz and operation power control mode is other than low voltage mode. • Wait time = 679 (84.88 µs) (value after reset) when operation power control mode is low-voltage mode. 1 1 0: • Wait time = 541 cycles (67.63 µs) when HOCO operating frequency is 64 MHz. Other settings are prohibited. Wait time is calculated at MOCO = 8 MHz (typically 0.125 µs).	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

HOCOWTCR controls the wait time until output of the signal from the high-speed clock oscillator to the internal circuits starts. Only write to HOCOWTCR when the HOCOCR.HCSTP bit is 1 or the OSCSF.HOCOSF flag is 1. Do not write to HOCOWTCR under any other conditions.

HSTS[2:0] bits (HOCO wait time setting)

The oscillation stabilization wait circuit measures the wait time and controls the clock supply in the MCU by counting the number of middle-speed clock cycles set in the HOCOWTCR register.

When the high-speed clock oscillator starts, the oscillation stabilization wait circuit starts counting the number of middle-speed clock cycles set in the HOCOWTCR register. The MCU clock supply is disabled until counting of the set number of cycles is complete. After counting completes, supply of the clock signal in the MCU starts and the OSCSF.HOCOSF flag is set to 1.

The oscillation stabilization wait circuit continues to count the middle-speed clock cycles regardless of the MOCOCR.MCSTP bit setting. Hardware automatically controls the running and stopping of the middle-speed oscillator for wait time measurement.

9.2.15 高速片上振荡器等待控制寄存器(HOCOWTCR)

Address(es): SYSTEM.HOCOWTCR 4001 E0A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
重置后的值:	0	0	0	0	0	1	0	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	HSTS[2:0]	HOCO等待时间设置	b2 b0 1 0 1: 等待时间=245个周期(29.13µs) 当HOCO工作频率为24MHz或32 MHz，并且工作功率控制模式不是低电压模式。 等待时间=287个周期（35.875µs）（复位后的值）， 当HOCO工作频率为48MHz且工作功率控制模式不是低电压模式时。 等待时间=679(84.88µs)（复位后的值） 当工作电源控制模式为低压模式时。 1 1 0: 等待时间=541个周期(67.63µs) 当HOCO工作频率为64MHz时。禁止其他设置。 等待时间是在MOCO=8MHz（通常为0.125µs）时计算的。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

HOCOWTCR控制直到信号从高速时钟振荡器输出到内部电路开始的等待时间。仅当HOCOCR.HCSTP位为1或OSCSF.HOCOSF标志为1时才写入HOCOWTCR。在任何其他条件下不要写入HOCOWTCR。

HSTS[2:0]位（HOCO等待时间设置）

振荡稳定等待电路通过计算在HOCOWTCR寄存器中设置的中速时钟周期数来测量等待时间并控制MCU中的时钟供应。

当高速时钟振荡器启动时，振荡稳定等待电路开始计数在HOCOWTCR寄存器中设置的中速时钟周期数。MCU时钟电源被禁用，直到设置的周期数计数完成。计数完成后，MCU中的时钟信号开始提供，并且OSCSF.HOCOSF标志设置为1。

振荡稳定等待电路继续计数中速时钟周期，而不管
MOCOCR.MCSTP位设置。硬件自动控制中速振荡器的运行和停止以进行等待时间测量。

9.2.16 Main Clock Oscillator Mode Oscillation Control Register (MOMCR)

Address(es): SYSTEM.MOMCR 4001 E413h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MOSEL	—	—	MODRV1	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	MODRV1	Main Clock Oscillator Drive Capability 1 Switching	0: 10 MHz to 20 MHz 1: 1 MHz to 10 MHz.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	MOSEL	Main Clock Oscillator Switching	0: Resonator 1: External clock input.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: The EXTAL/XTAL pin is also used as a port. In the initial setting state, the pin is set as a port.
Note: The MOSTP bit must be 1 (MOSC is stopped) before changing this register.

MODRV1 bit (Main Clock Oscillator Drive Capability 1 Switching)

The MODRV1 bit switches the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

9.2.17 Sub-Clock Oscillator Mode Control Register (SOMCR)

Address(es): SYSTEM.SOMCR 4001 E481h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SODRV[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SODRV[1:0]	Sub-Clock Oscillator Drive Capability Switching	b1 b0 0 0: Normal mode 0 1: Low power mode 1 1 0: Low power mode 2 1 1: Low power mode 3.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register must be modified when SOSCCR.SOSTP is 1 (SOSC is stopped).

SODRV[1:0] bits (Sub-Clock Oscillator Drive Capability Switching)

The SODRV[1:0] bits switch the drive capability of the sub-clock oscillator.

9.2.16 主时钟振荡器模式振荡控制寄存器(MOMCR)

Address(es): SYSTEM.MOMCR 4001 E413h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MOSEL	—	—	MODRV1	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	MODRV1	主时钟振荡器驱动能力1切换	0: 10 MHz to 20 MHz 1: 1 MHz to 10 MHz.	R/W
b5, b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	MOSEL	主时钟振荡器切换	0：谐振器1：外部时钟输入。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note: EXTALXTAL引脚也用作端口。在初始设置状态下，该引脚被设置为端口。
Note: 在更改此寄存器之前，MOSTP位必须为1（MOSC停止）。

MODRV1位（主时钟振荡器驱动能力1切换）

MODRV1位切换主时钟振荡器的驱动能力。

MOSEL位（主时钟振荡器切换）

MOSEL位切换主时钟振荡器的源。

9.2.17 副时钟振荡器模式控制寄存器(SOMCR)

Address(es): SYSTEM.SOMCR 4001 E481h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SODRV[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	SODRV[1:0]	副时钟振荡器驱动能力切换	b1 b0 0 0：正常模式 0 1：低功耗模式1 1 0：低功耗模式2 1 1：低功耗模式3。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SOSCCR.SOSTP为1（SOSC停止）时，必须修改该寄存器。

SODRV[1:0]位（副时钟振荡器驱动能力切换）

SODRV[1:0]位切换副时钟振荡器的驱动能力。

9.2.18 Segment LCD Source Clock Control Register (SLCDSCKCR)

Address(es): SYSTEM.SLCDSCKCR 4001 E050h

	b7	b6	b5	b4	b3	b2	b1	b0
	LCDSCKEN	—	—	—	—	LCDSCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	LCDSCKSEL[2:0]	LCD Source Clock (LCDSRCCLK) Select	b2 b0 0 0 0: LOCO 0 0 1: SOSC 0 1 0: MOSC 1 0 0: HOCO. Other settings are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	LCDSCKEN	LCD Source Clock Out Enable	0: LCD source clock out disabled 1: LCD source clock out enabled.	R/W

Setting the LCDSCKEN bit and LCDSCKSEL[2:0] bits at the same time is prohibited.

LCDSCKSEL[2:0] bits (LCD Source Clock (LCDSRCCLK) Select)

Set the LCDSCKSEL[2:0] bits to select the LOCO, SOSC, MOSC, HOCO clock as the LCD clock source. Clear the LCDSCKEN bit to 0 when changing the LCD source clock.

When changing these bits, apply the following steps:

1. Set LCDSCKEN to 0 (LCD source clock out is disabled).
2. Wait for 3 cycles of the LCD source clock and 2 cycles of ICLK before the change.
3. Write the changed value to LCDSCKSEL[2:0] bits.
4. Read LCDSCKSEL[2:0] bits to confirm the LCDSCKSEL[2:0] bits are changed.

LCDSCKEN bit (LCD Source Clock Out Enable)

Set this bit to enable output of the LCD source clock to LCD module.

When this bit is set to 1, the selected clock is output. When changing this bit, confirm that the LCD source clock selected by LCDSCLKSEL[2:0] bits is stable. When transitioning to Software Standby mode after changing this bit, apply the following steps:

1. Change this bit.
2. Wait for at least 2 cycles of the source clock selected by LCDSCKSEL[2:0] bits.
3. Execute the WFI instruction.

When stopping the source clock selected by LCDSCKSEL[2:0] bits after clearing this bit to 0, apply the following steps:

1. Clear this bit to 0 (LCD source clock output is disabled).
2. Wait for at least 2 cycles of the source clock selected by LCDSCKSEL[2:0] bits.
3. Stop the source clock selected by LCDSCKSEL[2:0] bits.

9.2.18 段式LCD源时钟控制寄存器(SLCDSCKCR)

Address(es): SYSTEM.SLCDSCKCR 4001 E050h

	b7	b6	b5	b4	b3	b2	b1	b0
	LCDSCKEN	—	—	—	—	LCDSCKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	LCDSCKSEL[2:0]	LCD源时钟(LCDSRCCLK)选择	b2 b0 0 0 0: LOCO 0 0 1: SOSC 0 1 0: MOSC 00：浩可。禁止其他设置。	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	LCDSCKEN	LCD源时钟输出使能	0：禁用LCD源时钟输出1：启用LCD源时钟输出。	R/W

禁止同时设置LCDSCKEN位和LCDSCKSEL[2:0]位。

LCDSCKSEL[2:0]位（LCD源时钟(LCDSRCCLK)选择）

设置LCDSCKSEL[2:0]位以选择LOCO、SOSC、MOSC、HOCO时钟作为LCD时钟源。清除当改变LCD源时钟时LCDSCKEN位为0。

更改这些位时，应用以下步骤：

1. 将LCDSCKEN设置为0（禁用LCD源时钟输出）。
2. 等待LCD源时钟的3个周期和ICLK的2个周期后才改变。
3. 将更改后的值写入LCDSCKSEL[2:0]位。
4. 读取LCDSCKSEL[2:0]位以确认LCDSCKSEL[2:0]位已更改。

LCDSCKEN位（LCD源时钟输出使能）

设置该位以使能LCD源时钟输出到LCD模块。

当该位设置为1时，输出选定的时钟。更改此位时，请确认LCDSCLKSEL[2:0]位选择的LCD源时钟稳定。在更改该位后转换到软件待机模式时，应用以下步骤：

1. 改变这一点。
2. 等待LCDSCKSEL[2:0]位选择的源时钟的至少2个周期。
3. 执行WFI指令。

在将该位清0后停止由LCDSCKSEL[2:0]位选择的源时钟时，应用以下步骤：

1. 将该位清零（LCD源时钟输出被禁用）。
2. 等待LCDSCKSEL[2:0]位选择的源时钟的至少2个周期。
3. 停止由LCDSCKSEL[2:0]位选择的源时钟。

9.2.19 Clock Out Control Register (CKOCR)

Address(es): SYSTEM.CKOCR 4001 E03Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKOSEL[2:0]	Clock Out Source Select	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC. Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CKODIV[2:0]	Clock Out input frequency Division Select	b6 b4 0 0 0: ×1 0 0 1: /2 0 1 0: /4 0 1 1: /8 1 0 0: /16 1 0 1: /32 1 1 0: /64 1 1 1: /128.	R/W
b7	CKOEN	Clock Out enable	0: Clock Out disabled 1: Clock Out enabled.	R/W

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits specify the HOCO, MOCO, LOCO, MOSC, SOSC clock as the source clock to be output from the CLKOUT pin.

Set the CKOEN bit to 0 when changing the CLKOUT source clock.

CKODIV[2:0] bits (Clock Out input frequency Division Select)

The CKODIV[2:0] bits specify the clock division ratio.

Set the CKOEN bit to 0 when changing the division ratio. The division ratio of the output clock frequency must be set to a value no higher than the characteristics of the CLKOUT pin output frequency. For details on the characteristics of the CLKOUT pin, see section 48, Electrical Characteristics.

CKOEN bit (Clock Out enable)

The CKOEN bit enables output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock source selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

Clear this bit before entering Software Standby mode if the selected clock source is stopped in that mode.

9.2.19 时钟输出控制寄存器(CKOCR)

Address(es): SYSTEM.CKOCR 4001 E03Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CKOSEL[2:0]	时钟输出源选择	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 00：SOSC。禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	CKODIV[2:0]	时钟输出输入频率分区选择	b6 b4 0 0 0: ×1 0 0 1: /2 0 1 0: /4 0 1 1: /8 1 0 0: /16 1 0 1: /32 1 1 0: /64 1 1 1: /128.	R/W
b7	CKOEN	时钟输出使能	0：时钟输出禁用1： 时钟输出使能。	R/W

CKOSEL[2:0]位（时钟输出源选择）

CKOSEL[2:0]位指定HOCO、MOCO、LOCO、MOSC、SOSC时钟作为从CLKOUT引脚输出的源时钟。

更改CLKOUT源时钟时将CKOEN位设置为0。

CKODIV[2:0]位（时钟输出输入分频选择）

CKODIV[2:0]位指定时钟分频比。

更改分频比时将CKOEN位设置为0。输出时钟频率的分频比必须设置为不高于CLKOUT引脚输出频率特性的值。有关CLKOUT引脚特性的详细信息，请参见第48节，电气特性。

CKOEN位（时钟输出使能）

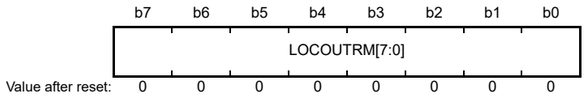
CKOEN位使能CLKOUT引脚的输出。

当该位设置为1时，输出选定的时钟。当该位设置为0时，输出低电平。更改该位时，请确认CKOSEL[2:0]位中选择的时钟源是稳定的。否则，可能会在输出中产生故障。

如果所选时钟源在该模式下停止，则在进入软件待机模式之前清零该位。

9.2.20 LOCO User Trimming Control Register (LOCOUTCR)

Address(es): SYSTEM.LOCOUTCR 4001 E492h



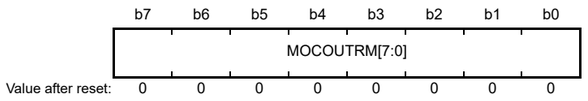
Bit	Symbol	Bit name	Description	R/W
b7 to b0	LOCOUTRM[7:0]	LOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127 These bits are added to the original LOCO trimming bits.	R/W

MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range.

When LOCOUTCR is modified, the time that the frequency is stabilized corresponds to the to the frequency stabilization time at the start of the MCU operation. When the ratio of the LOCO frequency to the other oscillation frequency is an integer value, changing the LOCOUTCR value is prohibited.

9.2.21 MOCO User Trimming Control Register (MOCOUTCR)

Address(es): SYSTEM.MOCOUTCR 4001 E061h



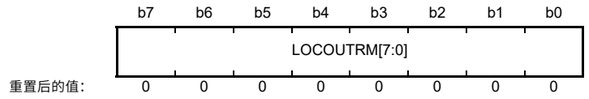
Bit	Symbol	Bit name	Description	R/W
b7 to b0	MOCOUTRM[7:0]	MOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127 These bits are added to the original MOCO trimming bits.	R/W

MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range.

When MOCOUTCR is modified, the time when the frequency is stabilized corresponds to the time when it is stabilized at the start of the MCU operation.

9.2.20 LOCO用户微调控制寄存器(LOCOUTCR)

Address(es): SYSTEM.LOCOUTCR 4001 E492h



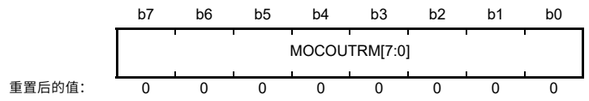
Bit	Symbol	位名称	Description	R/W
b7 to b0	LOCOUTRM[7:0]	LOCO用户修整	b7b010000000：-1281000 0001：-12710000010：-1 26…11111111：-10000000 0：中心代码00000001：+1 …01111101：+1250111111 0：+12601111111:+127 这些位被添加到原始的LOCO修整位。	R/W

当LOCOUTCR设置为导致LOCO频率超出规范范围的值时，MCU操作无法保证。

修改LOCOUTCR时，频率稳定的时间对应于MCU开始工作时的频率稳定时间。当LOCO频率与其他振荡频率之比为整数值时，禁止更改LOCOUTCR值。

9.2.21 MOCO用户微调控制寄存器(MOCOUTCR)

Address(es): SYSTEM.MOCOUTCR 4001 E061h



Bit	Symbol	位名称	Description	R/W
b7 to b0	MOCOUTRM[7:0]	MOCO用户修整	b7b010000000：-12810000001：-12710000010：-126…11111111：-100000000：中心代码00000001：+1…01111101：+12501111110：+12601111111:+127 这些位被添加到原始MOCO修整位中。	R/W

当MOCOUTCR设置为导致MOCO频率超出规格范围的值时，无法保证MCU操作。

修改MOCOUTCR时，频率稳定的时间对应于MCU开始工作时频率稳定的时间。

When the ratio of the MOCO frequency to the other oscillation frequency is an integer value, changing the MOCOUTCR value is prohibited.

9.2.22 HOCO User Trimming Control Register (HOCOUTCR)

Address(es): SYSTEM.HOCOUTCR 4001 E062h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	HOCOUTRM[7:0]	HOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original HOCO trimming bits.	R/W

MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range. When HOCOUTCR is modified, the time taken for the frequency to stabilize corresponds to the time taken for the frequency to stabilize at the start of the MCU operation. When USBCKCR.USBCLKSEL = 1, writing any other value except 00h to HOCOUTCR is prohibited.

9.2.23 Trace Clock Control Register (TRCKCR)

Address(es): SYSTEM.TRCKCR 4001 E03Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRCKEN	—	—	—	TRCK[3:0]			
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	TRCK[3:0]	Trace Clock operation frequency select	b3 b0 0 0 0 0: /1 0 0 0 1: /2 (value after reset) 0 0 1 0: /4. Other settings are prohibited.	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TRCKEN	Trace Clock operating enable	0: Operation disabled 1: Operation enabled.	R/W

Note: The TRCKCR register can be initialized by all resets except VBATT_POR.

The Trace Clock Control Register controls the switching of the trace clock. Set TRCKEN to 0 before changing the TRCLK frequency.

当MOCO频率与其他振荡频率之比为整数值时，禁止更改MOCOUTCR值。

9.2.22 HOCO用户微调控制寄存器(HOCOUTCR)

Address(es): SYSTEM.HOCOUTCR 4001 E062h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	HOCOUTRM[7:0]	HOCO用户修整	b7b010000000：-12810000001：-12710000010：-126…11111111：-100000000：中心代码00000001：+1…01111101：+12501111110：+12601111111：+127。这些位被添加到原始HOCO修整位中。	R/W

当HOCOUTCR设置为导致HOCO频率超出规范范围的值时，MCU操作无法保证。修改HOCOUTCR时，频率稳定所需的时间对应于MCU操作开始时频率稳定所需的时间。当USBCKCR.USBCLKSEL=1时，禁止向HOCOUTCR写入除00h之外的任何其他值。

9.2.23 跟踪时钟控制寄存器(TRCKCR)

Address(es): SYSTEM.TRCKCR 4001 E03Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRCKEN	—	—	—	TRCK[3:0]			
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b3 to b0	TRCK[3:0]	跟踪时钟工作频率选择	b3b00000：10001：2（复位后的值）0010：4。禁止其他设置。	R/W
b6 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	TRCKEN	跟踪时钟操作使能	0：禁止操作1：允许操作。	R/W

Note: TRCKCR寄存器可以通过除VBATT_POR之外的所有复位来初始化。

跟踪时钟控制寄存器控制跟踪时钟的切换。在更改之前将TRCKEN设置为0
TRCLK frequency.

9.2.24 USB Clock Control Register (USBCKCR)

Address(es): SYSTEM.USBCKCR 4001 E0D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	USBCLKSEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USBCLKSEL	USB Clock Source Select	0: PLL (Value after reset) 1: HOCO.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

USBCLKSEL bit (USB Clock Source Select)

The USBCLKSEL bit selects the source of the USB clock (UCLK).

- Rewrite the USBCKCR register while the SYSCFG.SCKE bit is 0.
- The USBCKCR.USBCLKSEL bit can only be set to 1 when USBFS is used as the device controller. Set the USBCKSR.USBCLKSEL bit to 0 to use the host controller.
- The user trimming function cannot be used when the USBCKCR.USBCLKSEL bit is 1. To use the HOCO user trimming function, set the bits HOCOUTCR.HOCOUTRM[7:0] to 00h.

9.3 Main Clock Oscillator

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

9.3.1 Connecting a Crystal Resonator

Figure 9.4 shows an example of connecting a crystal resonator.

A damping resistor (Rd) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 9.1.

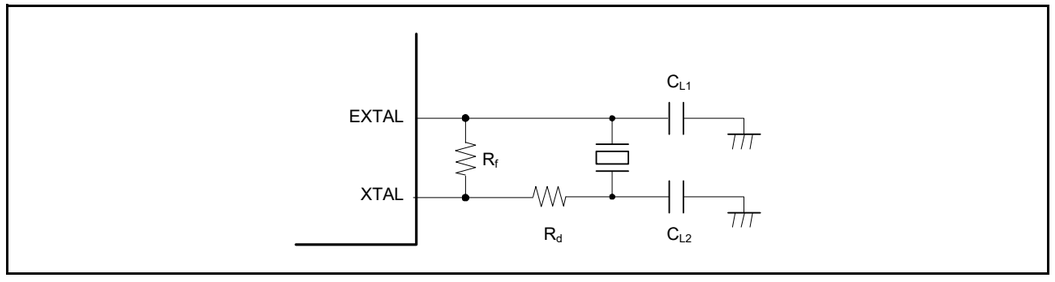


Figure 9.4 Example of crystal resonator connection

9.2.24 USB时钟控制寄存器(USBCKCR)

Address(es): SYSTEM.USBCKCR 4001 E0D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	USBCLKSEL
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	USBCLKSEL	USB时钟源选择	0: PLL (Value after reset) 1: HOCO.	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

USBCLKSEL位（USB时钟源选择）

USBCLKSEL位选择USB时钟(UCLK)的来源。

- 在SYSCFG.SCKE位为0时重写USBCKCR寄存器。
- USBCKCR.USBCLKSEL位只能在USBFS用作设备控制器时设置为1。
  将USBCKSR.USBCLKSEL位设置为0以使用主机控制器。
- 当USBCKCR.USBCLKSEL位为1时，不能使用用户微调功能。要使用HOCO用户微调功能，请将位HOCOUTCR.HOCOUTRM[7:0]设置为00h。

9.3 主时钟振荡器

要将时钟信号提供给主时钟振荡器，请使用以下方法之一：

- 连接振荡器
- 连接外部时钟信号的输入。

9.3.1 连接晶体谐振器

图9.4显示了连接晶体谐振器的示例。

如果需要，可以添加一个阻尼电阻器(Rd)。由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器(Rf)，请按照说明在EXTAL和XTAL之间插入一个Rf。

连接谐振器以提供时钟时，谐振器的频率必须在表9.1中所述的主时钟振荡器的谐振器频率范围内。

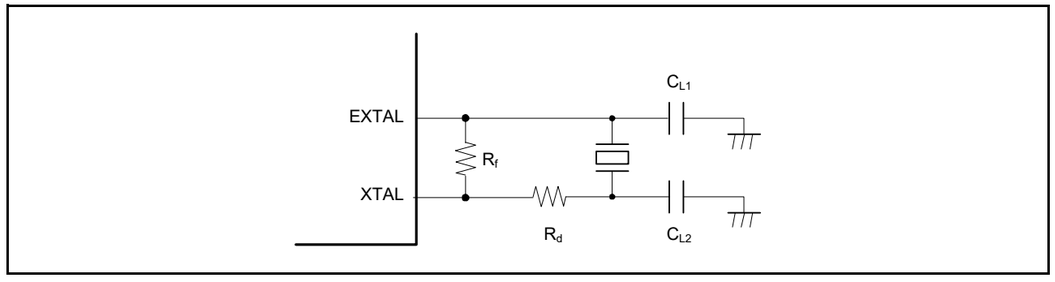


Figure 9.4 晶体谐振器连接示例

9.3.2 External Clock Input

Figure 9.5 show an example of connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin goes to high impedance.

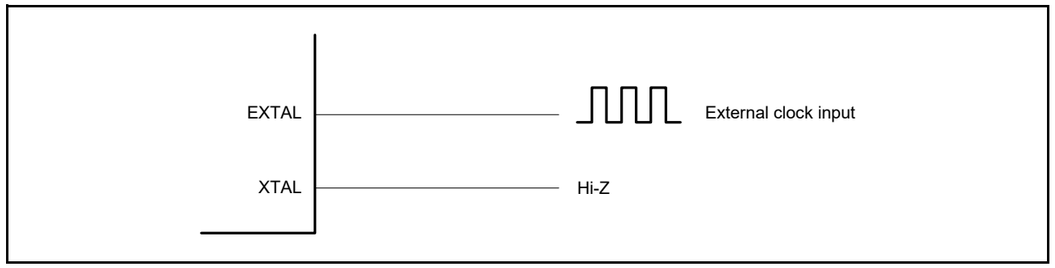


Figure 9.5 Equivalent circuit for external clock

9.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

9.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

9.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator, as shown in Figure 9.6.

A damping resistor (Rd) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the resonator manufacturer recommends the use of an external feedback resistor (Rf), insert an Rf between XCIN and XCOUT by following the instructions. When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 9.1.

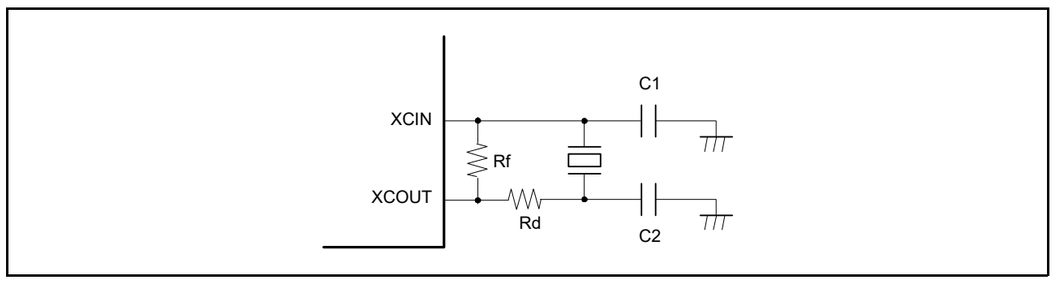


Figure 9.6 Connection example of 32.768-kHz crystal resonator

9.5 Dedicated Clock Oscillator for Bluetooth

Operating Bluetooth requires connection to the 32-MHz clock oscillator.

9.5.1 Connecting the Oscillator

An example of connection of the oscillator is shown in Figure 9.7.

Insert a damping resistor (Rd) as required. Set the resistance to the value recommended by the oscillator manufacturer as the value depends on the oscillator and its driving capability. If the oscillator manufacturer states that the addition of a

9.3.2 外部时钟输入

图9.5显示了连接外部时钟输入的示例。要使用外部时钟信号操作振荡器，请将MOMCR.MOSEL位设置为1。XTAL引脚变为高阻抗。

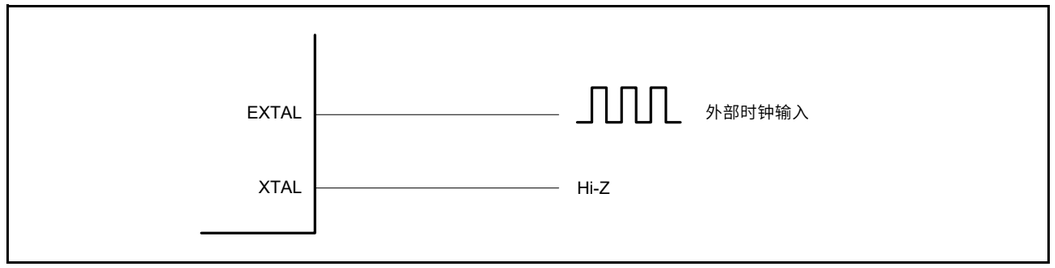


Figure 9.5 外部时钟等效电路

9.3.3 外部时钟输入注意事项

外部时钟输入的频率只有在主时钟振荡器停止时才能改变。当主时钟振荡器停止位(MOSCCR.MOSTP)设置为0时，请勿更改外部时钟输入的频率。

9.4 Sub-Clock Oscillator

向副时钟振荡器提供时钟信号的唯一方法是连接晶体振荡器。

9.4.1 连接32.768kHz晶体谐振器

要为副时钟振荡器提供时钟，请连接一个32.768-kHz晶体谐振器，如图9.6所示。

如果需要，可以添加一个阻尼电阻器(Rd)。由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果谐振器制造商建议使用外部反馈电阻器(Rf)，请按照说明在XCIN和XCOUT之间插入一个Rf。连接谐振器以提供时钟时，谐振器的频率必须在表9.1中所述的副时钟振荡器的谐振器频率范围内。

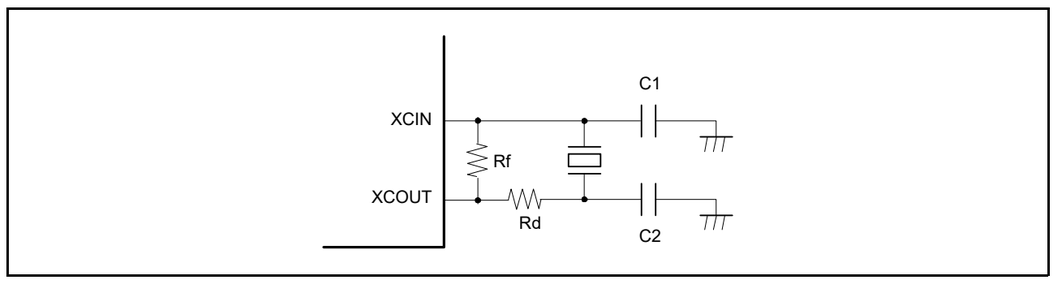


Figure 9.6 32.768-kHz晶体谐振器的连接示例

9.5 蓝牙专用时钟振荡器

运行蓝牙需要连接到32-MHz时钟振荡器。

9.5.1 连接振荡器

振荡器的连接示例如图9.7所示。

根据需要插入阻尼电阻器(Rd)。将电阻设置为振荡器制造商推荐的值，因为该值取决于振荡器及其驱动能力。如果振荡器制造商声明添加一个

feedback resistor (Rf) to the oscillator is required, insert Rf between XTAL1_RF and XTAL2_RF according to the instructions.

To control the oscillator, use the Bluetooth middleware provided by Renesas. The Bluetooth middleware is also able to control the settings of the on-chip variable capacitors, CL1 and CL2, to adjust the frequency of oscillation. Adjustment of the frequency of the Bluetooth-dedicated clock oscillator is explained in the application note Procedure for Adjusting the Frequency of the Bluetooth-Dedicated Clock Oscillator (R01AN4887). Obtain the latest version of this document from the Renesas website.

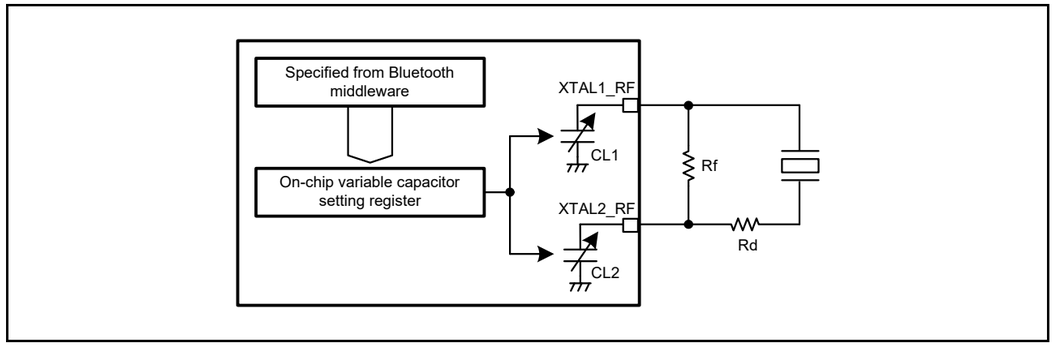


Figure 9.7 Example of the Connection of a 32-MHz Crystal Resonator

9.5.2 Connecting the Bluetooth-Dedicated Clock Output Pin

When the Bluetooth middleware sets up the clock output and the BLE shifts from waiting mode to RF power-down mode, the frequency-divided clock for the Bluetooth-dedicated clock is output. If the BLE subsequently shifts to RF low power mode, the RF clock output is disabled. The Bluetooth middleware is able to specify the frequency-divisor for the Bluetooth-dedicated clock.

The Bluetooth-dedicated clock output can also be used as the input of the external clock for the main clock oscillator by externally connecting the CLKOUT_RF and EXTAL pins on the board. Figure 9.8 shows an example of a configuration where the Bluetooth-dedicated clock output is used as the input of the external clock for the main clock oscillator.

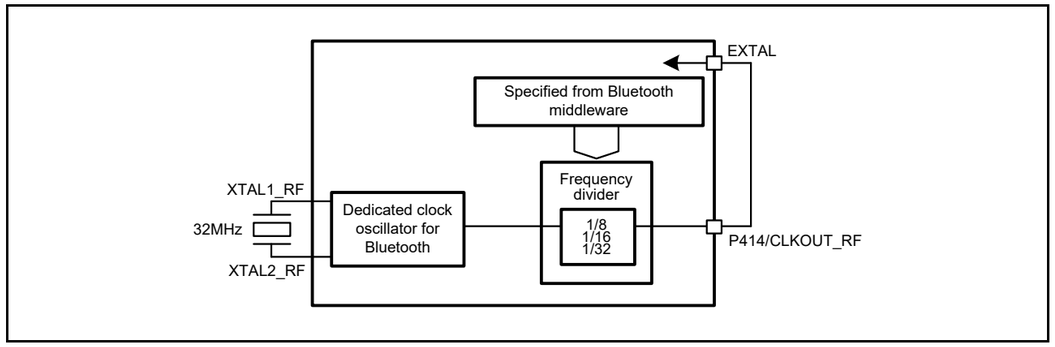


Figure 9.8 Example of Connection of the Bluetooth-dedicated clock output pin

9.6 Oscillation Stop Detection Function

9.6.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function is used to detect the main clock oscillator stop.

When oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system

需要给振荡器提供反馈电阻（Rf），按照说明在XTAL1_RF和XTAL2_RF之间插入Rf。

要控制振荡器，请使用瑞萨电子提供的蓝牙中间件。蓝牙中间件还可以控制片上可变电容CL1和CL2的设置，以调整振荡频率。蓝牙专用时钟振荡器频率的调整在应用笔记"调整蓝牙专用时钟振荡器频率的程序"（R01AN4887）中进行了说明。从瑞萨电子网站获取本文档的最新版本。

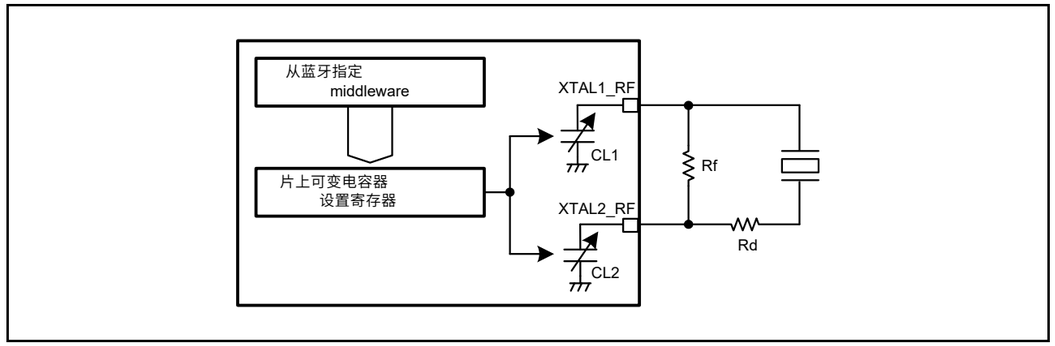


Figure 9.7 32MHz晶体谐振器的连接示例

9.5.2 连接蓝牙专用时钟输出引脚

当蓝牙中间件设置时钟输出并且BLE从等待模式切换到RF掉电模式时，输出蓝牙专用时钟的分频时钟。如果BLE随后切换到RF低功耗模式，RF时钟输出将被禁用。蓝牙中间件能够为蓝牙专用时钟指定分频器。

通过外部连接板上的CLKOUT_RF和EXTAL引脚，蓝牙专用时钟输出也可以用作主时钟振荡器的外部时钟输入。图9.8显示了一个配置示例，其中蓝牙专用时钟输出用作主时钟振荡器的外部时钟输入。

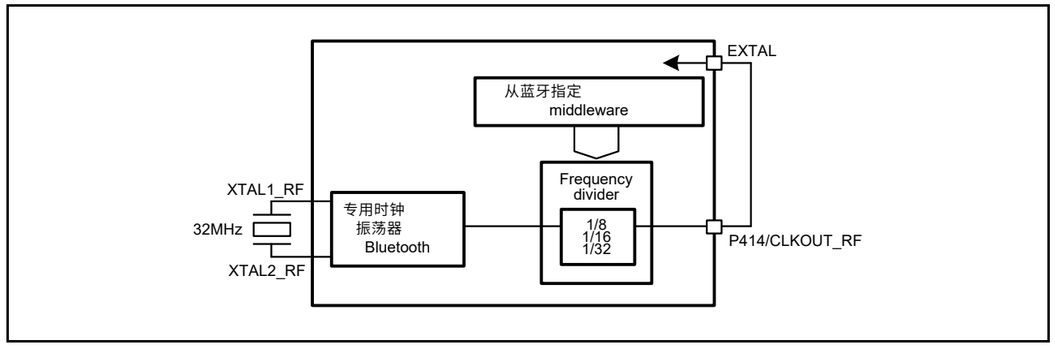


Figure 9.8 蓝牙专用时钟输出引脚的连接示例

9.6 振荡停止检测功能

9.6.1 振荡停止检测和检测后操作

振荡停止检测功能用于检测主时钟振荡器停止。

当检测到振荡停止时，系统时钟切换如下：

- 如果使用SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）检测到振荡停止，则系统

clock source switches to the MOCO clock.

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL), the PLL clock remains the system clock source. The frequency becomes a free-running oscillation frequency and the setting of SCKSCR.CKSEL[2:0] is unchanged.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, due to a malfunction of the main clock oscillator (see section 48, Electrical Characteristics).

Switching between the main clock and MOCO clock or between the PLL clock and PLL free-running clock is controlled by the Oscillation Stop Detection Flag (OSTDSR.OSTDF).

OSTDF controls the switched clock as follows:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  When OSTDF changes from 0 to 1, the clock source switches to MOCO.
  When OSTDF changes from 1 to 0, the clock source switches to MOSC again.
- SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL):
  When OSTDF changes from 0 to 1, the clock source switches to the PLL free-running oscillation clock.
  When OSTDF changes from 1 to 0, the clock source switches to PLL again.

To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock, and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation settling time elapses.

After a reset is released, the main clock oscillator stops and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation settling time elapses.

The oscillation stop detection function detects when the main clock is stopped by an external cause. Therefore, the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or a transition is made to Software Standby mode.

The oscillation stop detection function switches the following clocks to the MOCO clock (when system clock is MOSC):

- All clocks that can select the MOSC or PLL except CLKOUT
- The system clock (ICLK) frequency during the MOCO (when system clock is MOSC) or PLL free-running (when system clock is PLL) operation is specified in the MOCO oscillation frequency and the division ratio set in the System Clock Select bits (SCKDIVCR.ICK[2:0]).

时钟源切换到MOCO时钟。

- 如果在SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）时检测到振荡停止，则PLL时钟保持系统时钟源。频率变为自由振荡频率，SCKSCR.CKSEL[2:0]的设置不变。

当检测到振荡停止时，可以产生一个振荡停止检测中断请求。除此之外
通用PWM定时器(GPT)输出可在检测时强制为高阻抗状态。

当输入时钟在一定时间内保持在0或1时，检测到主时钟振荡停止，例如，由于主时钟振荡器的故障（参见第48节，电气特性）。

主时钟和MOCO时钟之间或PLL时钟和PLL自由运行时钟之间的切换由振荡停止检测标志(OSTDSR.OSTDF)控制。

OSTDF控制切换时钟如下：

- SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）：
  当OSTDF从0变为1时，时钟源切换到MOCO。
  当OSTDF从1变为0时，时钟源再次切换到MOSC。
- SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）：
  当OSTDF从0变为1时，时钟源切换到PLL自由振荡时钟。
  当OSTDF从1变为0时，时钟源再次切换到PLL。

要在检测到振荡停止后再次将时钟源切换为主时钟或PLL时钟，请将CKSEL[2:0]位设置为主时钟或PLL时钟以外的时钟源，并将OSTDF标志清零。另外，检查OSTDF标志不为1，然后在指定的振荡稳定时间过去后将CKSEL[2:0]位设置为主时钟或PLL时钟。

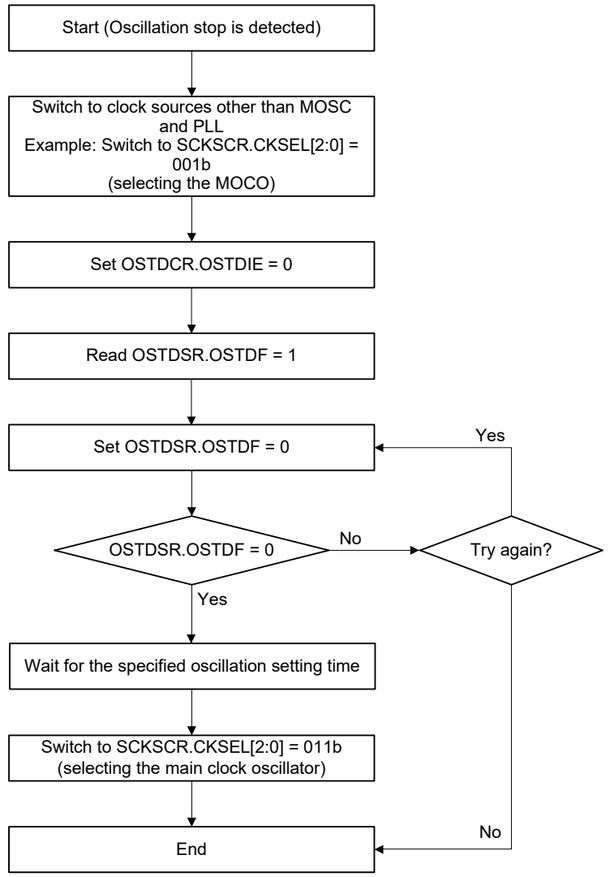
复位解除后，主时钟振荡器停止，振荡停止检测功能被禁用。要使能振荡停止检测功能，激活主时钟振荡器并在经过指定的振荡稳定时间后将1写入振荡停止检测功能使能位(OSTDCR.OSTDE)。

振荡停止检测功能检测主时钟何时因外部原因停止。因此，必须在软件停止主时钟振荡器或转换到软件待机模式之前禁用振荡停止检测功能。

振荡停止检测功能将以下时钟切换为MOCO时钟（系统时钟为MOSC时）：

- 可以选择MOSC或PLL的所有时钟，除了CLKOUT
- MOCO（系统时钟为MOSC时）或PLL自由运行（系统时钟为PLL时）操作期间的系统时钟(ICLK)频率在MOCO振荡频率和系统时钟选择位(SCKDIVCR)中设置的分频比中指定.ICK[2:0])。

Example of returning when CKSEL[2:0] = 011b (selecting the main clock oscillator) after an oscillation stop is detected.



Note: On returning from the oscillation-stopped state, the factor responsible for stopping the main clock oscillation circuit must be removed from the system to allow oscillation to resume.

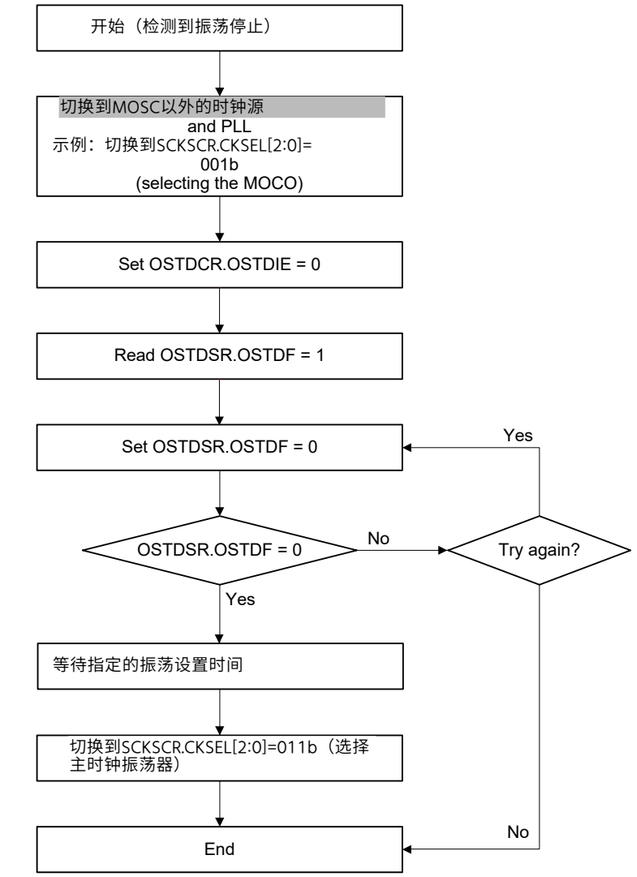
Figure 9.9 Flow of recovery on detection of oscillator stop

9.6.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection Flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B).

After the oscillation stop is detected, wait at least 10 PCLKB cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

检测到振荡停止后CKSEL[2:0]=011b（选择主时钟振荡器）时返回的示例。



Note: 在从振荡停止状态返回时，必须从系统中移除负责停止主时钟振荡电路的因素以允许振荡恢复。

Figure 9.9 检测到振荡器停止时的恢复流程

9.6.2 振荡停止检测中断

当振荡停止检测标志(OSTDSR.OSTDF)为1且振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位为1（使能）时，将产生一个振荡停止检测中断(MOSC_STOP)。GPT端口输出使能(POEG)被通知主时钟振荡器停止。收到通知后，POEG将POEG组n设置寄存器(POEGGn.OSTPF)中的振荡停止检测标志设置为1(n=A B)。

检测到振荡停止后，至少等待10个PCLKB周期，然后再写入POEGGn.OSTPF标志。当需要清除OSTDSR.OSTDF标志时，请在清除振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位后执行此操作。在设置之前至少等待2个PCLKB时钟周期

OSTDCR.OSTDIE位再次为1。可能需要更长的PCLKB等待时间，具体取决于读取给定IO寄存器所需的周期数。

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable the non-maskable interrupts through software before using the oscillation stop detection interrupts. For details, see section 14, Interrupt Controller Unit (ICU).

9.7 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

9.8 Internal Clock

Clock sources for the internal clock signals include:

- Main clock oscillator
- Sub-clock oscillator
- HOCO clock
- MOCO clock
- LOCO clock
- PLL clock
- Dedicated clock for the IWDT
- External clock for JTAG.

The following internal clocks are produced from these sources:

- Operating clock for the CPU, DMAC, DTC, flash memory, and SRAM — system clock (ICLK)
- Operating clocks for peripheral modules — PCLKA, PCLKB, PCLKC, and PCLKD
- Operating clock for the flash interface — FCLK
- Operating clock for the USBFS — UCLK
- Operating clock for the CAN — CANMCLK
- Operating clocks for the CAC — CACCLK
- Operating clock for the RTC LOCO clock — RTCLCLK
- Operating clock for the RTC sub clock — RTCSCLK
- Operating clock for the IWDT — IWDTCLK
- Operating clock for the AGT LOCO clock — AGTLCLK
- Operating clock for the AGT sub clock — AGTSCLK
- Operating clock for the SysTick timer — SYSTICCLK
- Source clock for the SLCDC — LCDSRCCLK
- Clock for external pin output — CLKOUT
- Operating clock for the JTAG — JTAGTCK.

Operating clocks for the BLE: The Bluetooth-dedicated clock (BLECLK), and the Bluetooth-dedicated low-speed clock (BLELOCO).

For details of the registers used to set the frequencies of the internal clocks, see section 9.8.1, System Clock (ICLK) to section 9.8.13, JTAG Clock (JTAGTCK).

If the value of any of these bits is changed, subsequent operation is at a frequency determined by the new value.

9.8.1 System Clock (ICLK)

The system clock, ICLK, is the operating clock for the CPU, DMAC, DTC, flash memory, and SRAM.

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the

振荡停止检测中断是一个不可屏蔽的中断。由于不可屏蔽中断在复位释放后的初始状态下被禁用，因此在使用振荡停止检测中断之前，请通过软件启用不可屏蔽中断。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

9.7 PLL Circuit

PLL电路具有倍增振荡器频率的功能。

9.8 内部时钟

内部时钟信号的时钟源包括：

- 主时钟振荡器
- Sub-clock oscillator
- HOCO clock
- MOCO clock
- 机车时钟
- PLL clock
- IWDT的专用时钟
- JTAG的外部时钟。

以下内部时钟由这些源产生：

- CPU、DMAC、DTC、闪存和SRAM的工作时钟—系统时钟(ICLK)
- 外围模块的工作时钟—PCLKA、PCLKB、PCLKC和PCLKD
- 闪存接口的工作时钟——FCLK
- USBFS的工作时钟—UCLK
- CAN的工作时钟—CANMCLK
- CAC的工作时钟—CACCLK
- RTCLOCO时钟的工作时钟—RTCLCLK
- RTC子时钟的工作时钟—RTCSCLK
- IWDT的工作时钟—IWDTCLK
- AGTLOCO时钟的工作时钟—AGTLCLK
- AGT子时钟的工作时钟—AGTSCLK
- SysTick定时器的工作时钟—SYSTICCLK
- SLCDC的源时钟—LCDSRCCLK
- 外部引脚输出时钟—CLKOUT
- JTAG的工作时钟—JTAGTCK。

BLE的工作时钟：蓝牙专用时钟(BLECLK)和蓝牙专用低速时钟(BLELOCO)。

有关用于设置内部时钟频率的寄存器的详细信息，请参见第9.8.1节，系统时钟(ICLK)至第9.8.13节，JTAG时钟(JTAGTCK)。

如果这些位中的任何一个位的值发生变化，则后续操作将以新值确定的频率进行。

9.8.1 系统时钟(ICLK)

系统时钟ICLK是CPU、DMAC、DTC、闪存和SRAM的工作时钟。

ICLK频率由SCKDIVCR中的ICK[2:0]位、SCKSCR中的CKSEL[2:0]位、

PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2, and the HOCOFRQ1[2:0] bits in OFS1.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 9.10 and Figure 9.11.

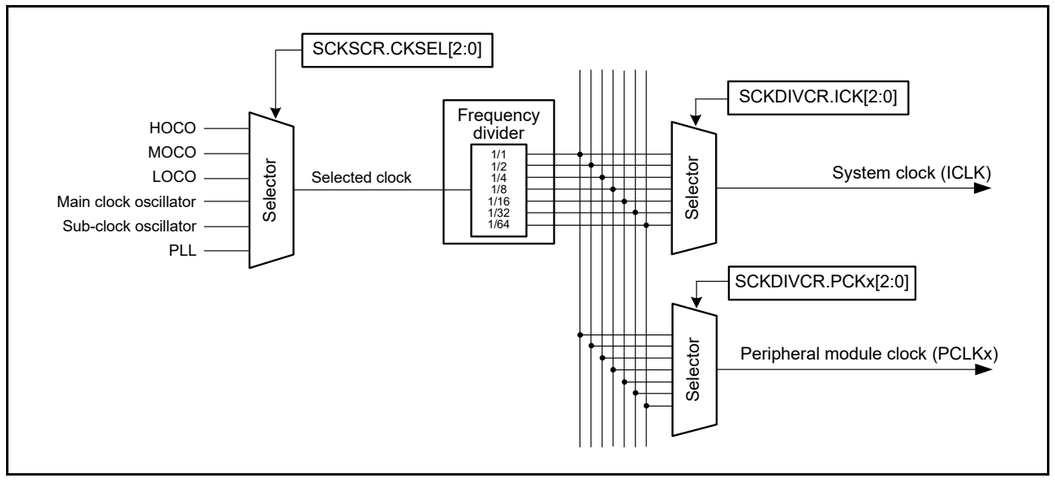


Figure 9.10 Clock source selector block diagram

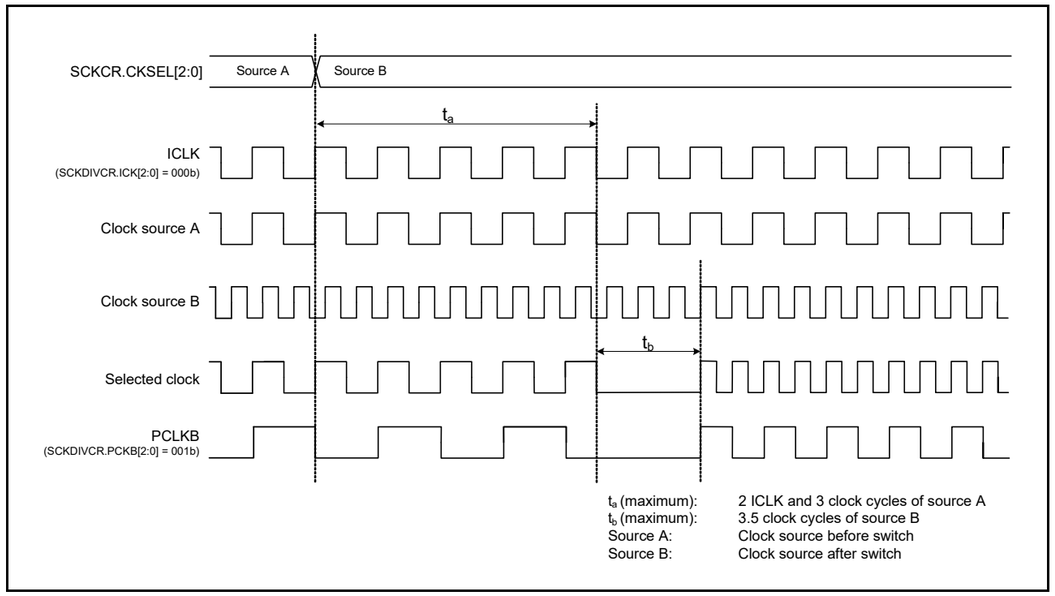


Figure 9.11 Clock source switching timing diagram

9.8.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

The peripheral module clocks, PCLKA, PCLKB, PCLKC, and PCLKD, are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR

PLLCCR2中的PLLMUL[4:0]和PLODIV[1:0]位，以及OFS1中的HOCOFRQ1[2:0]位。

当ICLK时钟源切换时，ICLK时钟周期的持续时间在时钟源转换期间变长。请参见图9.10和图9.11。

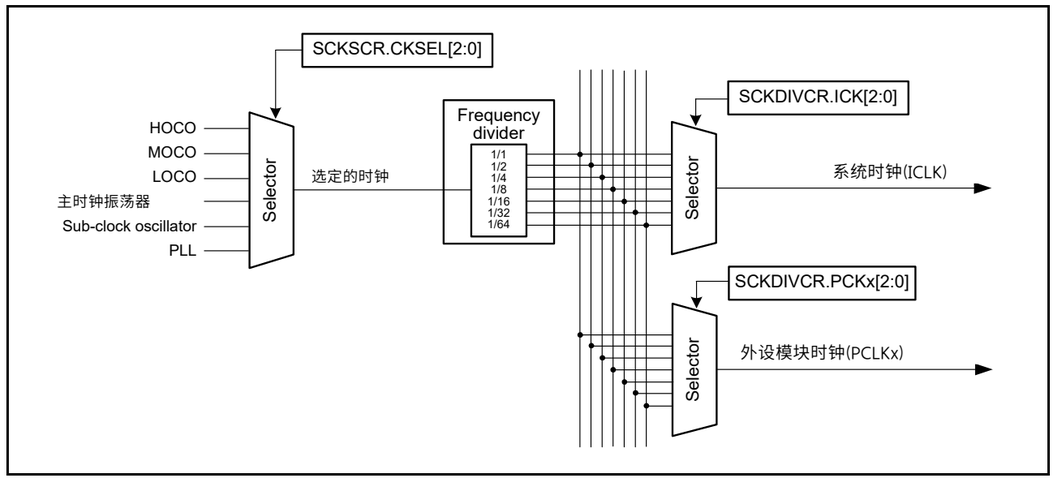


Figure 9.10 时钟源选择器框图

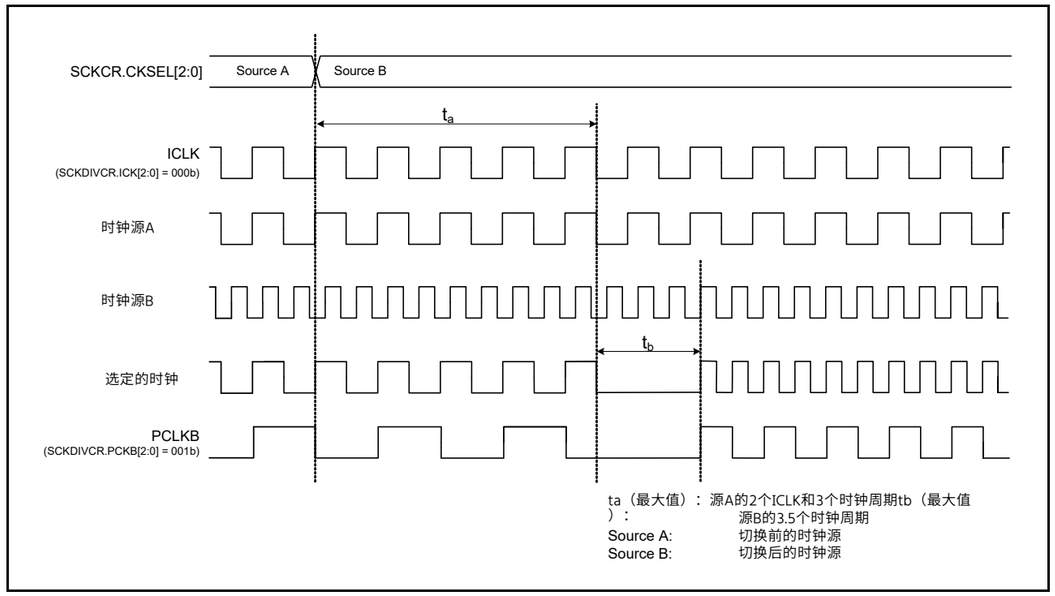


Figure 9.11 时钟源切换时序图

9.8.2 外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）

外围模块时钟PCLKA、PCLKB、PCLKC和PCLKD是外围模块的工作时钟。

给定时钟的频率在以下位中指定：

- SCKDIVCR中的PCKA[2:0]、PCKB[2:0]、PCKC[2:0]和PCKD[2:0]位

- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 9.10 and Figure 9.11.

9.8.3 Flash Interface Clock (FCLK)

The flash interface clock, FCLK, is the operating clock for the flash memory interface. In addition to reading from the data flash, FCLK is used for the programming and erasure of the code flash and data flash.

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

9.8.4 USB Clock (UCLK)

The USB clock, UCLK, is the operating clock for the USBFS module. A 48-MHz clock must be supplied to the USBFS module. When the USBFS module is used, the setting must be 48 MHz for the UCLK clock.

The UCLK frequency is specified in the following bits:

- CKSEL[2:0] bits in the SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

9.8.5 CAN Clock (CANMCLK)

The CAN clock, CANMCLK, is the operating clock for the CAN module. CANMCLK is generated by the main clock oscillator.

9.8.6 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC.

CACCLK is generated by the following:

- Main clock oscillator
- Sub-clock oscillator
- High-speed clock oscillator
- Middle-speed clock oscillator
- Low-speed on-chip oscillator
- IWDT-dedicated on-chip oscillator.

9.8.7 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

The RTC-dedicated clocks, RTCSCLK and RTCLCLK, are the operating clock for the RTC.

RTCSCLK is generated by the sub-clock oscillator, and RTCLCLK is generated by the LOCO.

9.8.8 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock, IWDTCLK, is the operating clock for the IWDT.

IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

- SCKSCR中的CKSEL[2:0]位
- PLLCCR2中的PLLMUL[4:0]和PLODIV[1:0]位
- OFS1中的HOCOFRQ1[2:0]位。

当外围模块时钟的时钟源切换时，外围模块时钟周期的持续时间在时钟源转换期间会变长。请参见图9.10和图9.11。

9.8.3 闪存接口时钟(FCLK)

闪存接口时钟FCLK是闪存接口的工作时钟。除了从数据闪存读取外，FCLK还用于代码闪存和数据闪存的编程和擦除。

FCLK频率在以下位中指定：

- SCKDIVCR中的FCK[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR2中的PLLMUL[4:0]和PLODIV[1:0]位
- OFS1中的HOCOFRQ1[2:0]位。

9.8.4 USB时钟(UCLK)

USB时钟UCLK是USBFS模块的工作时钟。必须为USBFS模块提供48-MHz时钟。使用USBFS模块时，UCLK时钟必须设置为48MHz。

UCLK频率在以下位中指定：

- SCKSCR中的CKSEL[2:0]位
- PLLCCR2中的PLLMUL[4:0]和PLODIV[1:0]位
- OFS1中的HOCOFRQ1[2:0]位。

9.8.5 CAN时钟(CANMCLK)

CAN时钟CANMCLK是CAN模块的工作时钟。CANMCLK由主时钟振荡器产生。

9.8.6 CAC时钟(CACCLK)

CAC时钟CACCLK是CAC的工作时钟。

CACCLK由以下产生：

- 主时钟振荡器
- Sub-clock oscillator
- 高速时钟振荡器
- 中速时钟振荡器
- Low-speed on-chip oscillator
- IWDT-dedicated on-chip oscillator.

9.8.7 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

RTC专用时钟RTCSCLK和RTCLCLK是RTC的工作时钟。

RTCSCLK由副时钟振荡器产生，RTCLCLK由LOCO产生。

9.8.8 IWDT-Dedicated Clock (IWDTCLK)

IWDT专用时钟IWDTCLK是IWDT的工作时钟。

IWDTCLK由IWDT专用的片上振荡器在内部产生。

9.8.9 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clock, AGTSCLK and AGTLCLK, is the operating clock for the AGT.

AGTSCLK is generated by the sub-clock oscillator, and AGTLCLK is generated by the LOCO.

9.8.10 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICKCLK, is the operating clock for the SYSTICCLK.

SYSTICCLK is generated by the LOCO clock.

9.8.11 Segment LCDC Source Clock (LCDSRCCLK)

The Segment LCDC source clock, LCDSRCCLK, is the operating clock of the SLCDC.

The LCDSRCCLK is specified by the LCDSCKSEL[2:0] bits in SLCDSCKCR.

LCDSRCCLK is output when SLCDSCKCR.LCDSCKEN is set to 1. When changing the value of SLCDSCKCR.LCDSCKSEL[2:0], make sure that the value of SLCDSCKCR.LCDSCKEN is 0.

9.8.12 Clock/Buzzer Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin, for the clock or buzzer output.

CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. When changing the value of CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR, make sure that the value of CKOCR.CKOEN is 0.

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

9.8.13 JTAG Clock (JTAGTCK)

The JTAG-dedicated clock, JTAGTCK, is the operating clock for the JTAG.

JTAGTCK is generated by the external clock for JTAG (TCK).

9.8.14 Clocks for BLE

The Bluetooth-dedicated clock (BLECLK) and the Bluetooth-dedicated low-speed clock (BLELOCO) are the operating clocks for the BLE. To control these clocks, use the Bluetooth middleware provided by Renesas.

9.9 Usage Notes

9.9.1 Notes on Clock Generation Circuit

The frequencies of the system clock (ICLK), peripheral module clock (PCLKA to PCLKD), and flash interface clock (FCLK) supplied to each module change according to the settings of SCKDIVCR. Each frequency must meet the following conditions:

- Select each frequency that is within the operation-guaranteed range of the clock cycle time (t_{cyc}) specified in the AC electrical characteristics, see section 48, Electrical Characteristics
- The frequencies must not exceed the ranges listed in Table 9.2
- The peripheral modules operate on the PCLKB and PCLKA. As a result, the operating speed of modules such as the timer and SCI varies before and after the frequency is changed.
- The system clock (ICLK), peripheral module clock (PCLKA to PCLKD), flash interface clock (FCLK), must be set according to Table 9.2.

To ensure correct processing after the clock frequency changes, first modify the pertinent Clock Control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

9.8.9 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

AGT专用时钟AGTSCLK和AGTLCLK是AGT的工作时钟。

AGTSCLK由副时钟振荡器产生，AGTLCLK由LOCO产生。

9.8.10 SysTick Timer-Dedicated Clock (SYSTICCLK)

SysTick定时器专用时钟SYSTICKCLK是SYSTICCLK的工作时钟。

SYSTICCLK由LOCO时钟生成。

9.8.11 段LCDC源时钟(LCDSRCCLK)

段LCDC源时钟LCDSRCCLK是SLCDC的工作时钟。

LCDSRCCLK由SLCDSCKCR中的LCDSCKSEL[2:0]位指定。

当SLCDSCCKCR.LCDSCKEN设置为1时，输出LCDSRCCLK。当改变SLCDSCKCR.LCDSCKSEL[2:0]，确保SLCDSCKCR.LCDSCKEN的值为0。

9.8.12 时钟蜂鸣器输出时钟(CLKOUT)

CLKOUT从CLKOUT引脚外部输出，用于时钟或蜂鸣器输出。

当CKOCR.CKOEN设置为1时，CLKOUT输出到CLKOUT引脚。当改变CKOCR中CKODIV[2:0]或CKOSEL[2:0]位的值时，请确保CKOCR.CKOEN的值是0。

CLKOUT时钟频率在以下位中指定：

- CKOCR中的CKODIV[2:0]或CKOSEL[2:0]
- PLLCCR2中的PLLMUL[4:0]和PLODIV[1:0]位
- OFS1中的HOCOFRQ1[2:0]位。

9.8.13 JTAG Clock (JTAGTCK)

JTAG专用时钟JTAGTCK是JTAG的工作时钟。

JTAGTCK由JTAG的外部时钟(TCK)生成。

9.8.14 BLE时钟

蓝牙专用时钟(BLECLK)和蓝牙专用低速时钟(BLELOCO)是BLE的工作时钟。要控制这些时钟，请使用瑞萨电子提供的蓝牙中间件。

9.9 使用说明

9.9.1 时钟产生电路注意事项

提供给每个模块的系统时钟(ICLK)、外围模块时钟(PCLKA至PCLKD)和闪存接口时钟(FCLK)的频率会根据SCKDIVCR的设置而变化。每个频率必须满足以下条件：

- 选择在AC电气特性中指定的时钟周期时间(tcyc)的操作保证范围内的每个频率，请参见第48节，电气特性
- 频率不得超过表9.2中列出的范围
- 外围模块在PCLKB和PCLKA上运行。结果，定时器和SCI等模块的运行速度在频率改变前后会发生变化。
- 系统时钟（ICLK）、外设模块时钟（PCLKA到PCLKD）、闪存接口时钟（FCLK）必须按照表9.2进行设置。

为保证时钟频率变化后的正确处理，首先修改相关的ClockControl寄存器改变频率，然后从寄存器中读取值，最后进行后续处理。

9.9.2 Notes on Resonator

Because various resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 9.6. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

9.9.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 9.12 to prevent electromagnetic induction from interfering with correct oscillation.

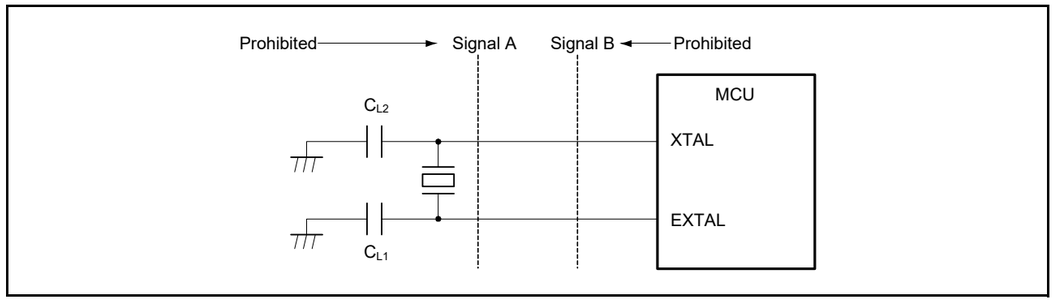


Figure 9.12 Signal routing in board design for oscillation circuit (applicable to the main clock oscillator as well as the sub clock oscillator and bluetooth-dedicated oscillator)

9.9.4 Notes on Resonator Connect Pin

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports P212 and P213. When these pins are used as general ports, the main clock must be stopped (MOSCCR.MOSTP should be set to 1).

9.9.2 谐振器注意事项

由于各种谐振器特性与您的电路板设计密切相关，因此在使用前需要进行充分评估。请参见图9.6中的谐振器连接示例。谐振器的电路常数取决于要使用的谐振器和安装电路的杂散电容。因此，在确定电路常数时，请咨询谐振器制造商。施加在谐振器引脚之间的电压必须在绝对最大额定值范围内。

9.9.3 电路板设计注意事项

使用晶体谐振器时，将谐振器及其负载电容尽可能靠近XTAL和EXTAL引脚。其他信号线应远离振荡电路，如图9.12所示，以防止电磁感应干扰正确的振荡。

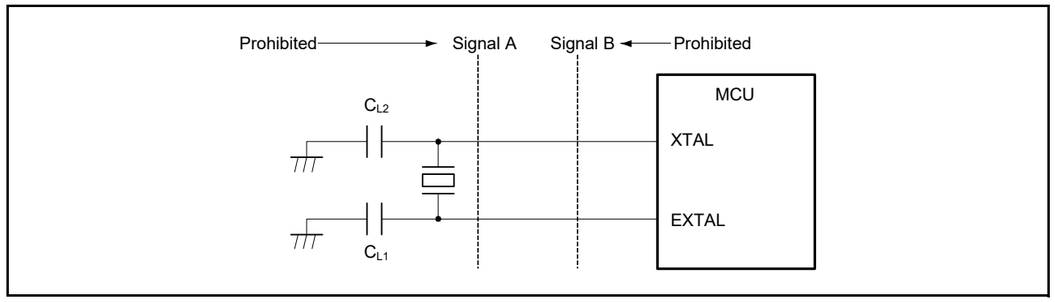


Figure 9.12 振荡电路板设计中的信号路由（适用于主时钟振荡器以及副时钟振荡器和蓝牙专用振荡器）

9.9.4 谐振器连接引脚注意事项

当不使用主时钟时，EXTAL和XTAL引脚可用作通用端口P212和P213。当这些引脚用作通用端口时，必须停止主时钟（MOSCCR.MOSTP应设置为1）。

10. Clock Frequency Accuracy Measurement Circuit (CAC)

10.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.

When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 10.1 lists the CAC specifications, Figure 10.1 shows a block diagram, and Table 10.2 shows the I/O pins.

Table 10.1 CAC specifications

Parameter	Description
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow.
Module-stop function	Module-stop state can be set to reduce power consumption

10. 时钟频率精度测量电路(CAC)

10.1 Overview

时钟频率精度测量电路(CAC)在用作测量基准的时钟（测量基准时钟）生成的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据是否脉冲数在允许范围内。

当测量完成或测量参考时钟在时间内产生的脉冲数不在允许范围内时，将产生中断请求。

表10.1列出了CAC规范，图10.1显示了框图，表10.2显示了IO引脚。

Table 10.1 CAC规格

Parameter	Description
测量目标时钟	可以测量以下频率的频率： 主时钟振荡器 副时钟振荡器 HOCO时钟 MOCO时钟 LOCO时钟 IWDTCLK时钟 外围模块时钟B(PCLKB)。
测量参考时钟	频率可以参考： CACREF引脚的外部时钟输入 主时钟振荡器 副时钟振荡器 HOCO时钟 MOCO时钟 LOCO时钟 IWDTCLK时钟 外设模块时钟B(PCLKB)。
可选择的功能	数字滤波器
中断源	测量结束 频率误差溢出。
Module-stop function	可设置模块停止状态以降低功耗

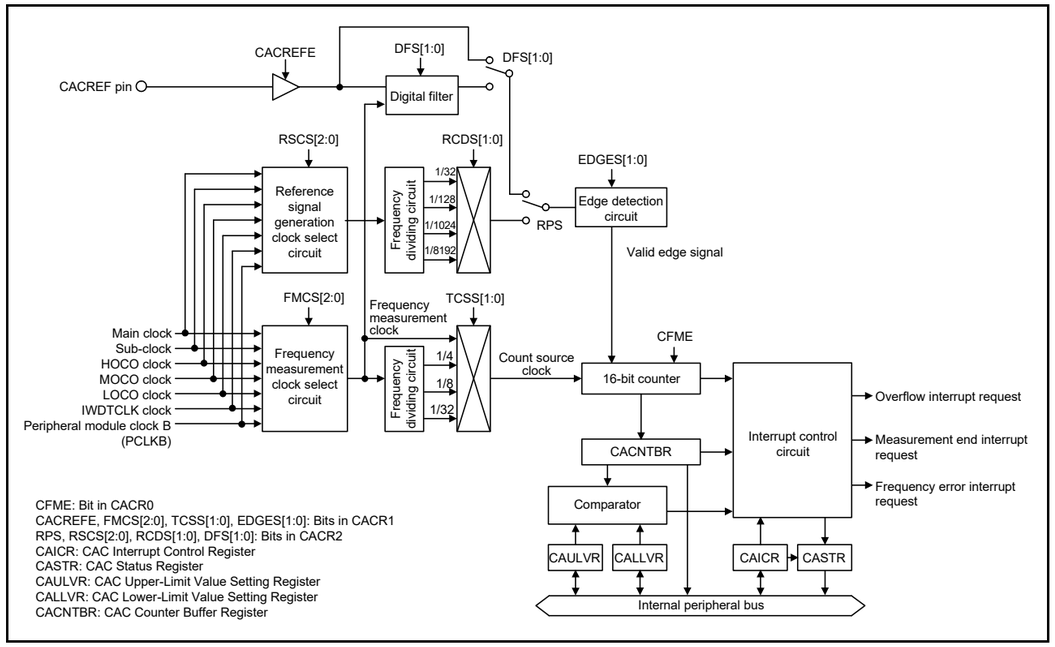


Figure 10.1 CAC block diagram

Table 10.2 CAC pin configuration

Pin name	I/O	Function
CACREF	Input	Measurement reference clock input pin

10.2 Register Descriptions

10.2.1 CAC Control Register 0 (CACR0)

Address(es): CAC.CACR0 4004 4600h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables the clock frequency measurement. Read the CFME bit to confirm that the bit value has changed. Additional write accesses are ignored before the change is complete.

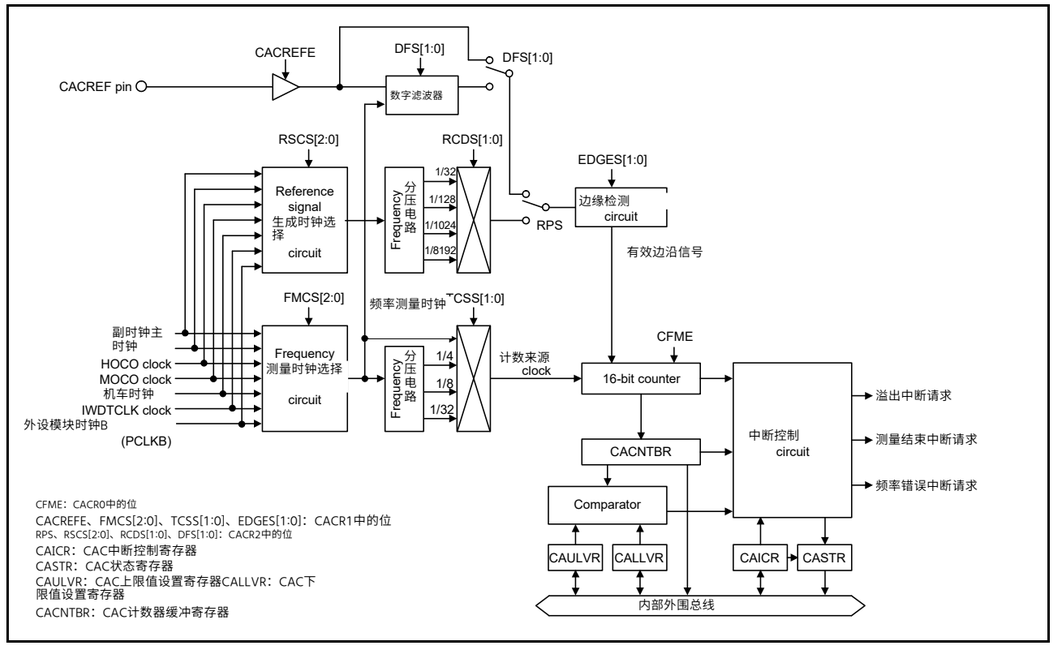


Figure 10.1 CAC框图

Table 10.2 CAC引脚配置

引脚名称	I/O	Function
CACREF	Input	测量参考时钟输入引脚

10.2 注册说明

10.2.1 CAC控制寄存器0(CACR0)

Address(es): CAC.CACR0 4004 4600h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CFME	时钟频率测量启用	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CFME位（时钟频率测量使能）

CFME位使能时钟频率测量。读取CFME位以确认该位值已更改。
在更改完成之前，将忽略其他写入访问。

10.2.2 CAC Control Register 1 (CACR1)

Address(es): CAC.CACR1 4004 4601h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: Disable 1: Enable.	R/W
b3 to b1	FMCS[2:0]	Measurement Target Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	TCSS[1:0]	Measurement Target Clock Frequency Division Ratio Select	b5 b4 0 0: No division 0 1: ×1/4 clock 1 0: ×1/8 clock 1 1: ×1/32 clock.	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited.	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Measurement Target Clock Frequency Division Ratio Select)

The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

10.2.2 CAC控制寄存器1(CACR1)

Address(es): CAC.CACR1 4004 4601h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CACREFE	CACREF引脚输入使能	0：禁用1 ：启用。	R/W
b3 to b1	FMCS[2:0]	测量目标时钟选择	b3b1000：主时钟振荡器001：副时钟振荡器010：HOCO时钟011：MOCO时钟100：LOCO时钟101：外围模块时钟（PCLKB）110：IWDTCLK时钟111：禁止设置。	R/W
b5, b4	TCSS[1:0]	测量目标时钟 分频比选择	b5b400：不分频 01：×14个时钟1 0：×18个时钟11 ：×132个时钟。	R/W
b7, b6	EDGES[1:0]	有效边选择	b7b600：上升沿01：下降沿10：上升沿和下降沿11：禁止设置。	R/W

Note: 当CACR0.CFME位为0时设置CACR1寄存器。

CACREFE位（CACREF引脚输入使能）

CACREFE位使能CACREF引脚输入。

FMCS[2:0]位（测量目标时钟选择）

FMCS[2:0]位选择要测量其频率的测量目标时钟。

TCSS[1:0]位（测量目标时钟分频比选择）

TCSS[1:0]位选择测量目标时钟的分频比。

EDGES[1:0]位（有效边沿选择）

EDGES[1:0]位选择参考信号的有效边沿。

10.2.3 CAC Control Register 2 (CACR2)

Address(es): CAC.CACR2 4004 4602h

	b7	b6	b5	b4	b3	b2	b1	b0
	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internal clock (internally generated signal).	R/W
b3 to b1	RSCS[2:0]	Measurement Reference Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock.	R/W
b7, b6	DFS[1:0]	Digital Filter Select	b7 b6 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the division ratio of the reference clock when an internal reference clock is selected (RPS = 1). When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and select its sampling clock.

10.2.3 CAC控制寄存器2(CACR2)

Address(es): CAC.CACR2 4004 4602h

	b7	b6	b5	b4	b3	b2	b1	b0
	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPS	参考信号选择	0：CACREF引脚输入1：内部时钟（内部产生的信号）。	R/W
b3 to b1	RSCS[2:0]	测量参考时钟 Select	b3b1000：主时钟振荡器001：副时钟振荡器010：HOCO时钟011：MOCO时钟100：LOCO时钟101：外围模块时钟（PCLKB）110：IWDTCLK时钟111：禁止设置。	R/W
b5, b4	RCDS[1:0]	测量参考时钟分频比选择	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock.	R/W
b7, b6	DFS[1:0]	数字滤波器选择	b7b600：禁用数字滤波01：使用数字滤波器的采样时钟作为频率测量时钟10：使用数字滤波器的采样时钟作为频率测量时钟除以411：使用数字滤波器的采样时钟滤波器作为频率测量时钟除以16。	R/W

Note: 当CACR0.CFME位为0时设置CACR2寄存器。

RPS位（参考信号选择）

RPS位选择是使用CACREF引脚输入还是使用内部时钟（内部产生的信号）作为参考信号。

RSCS[2:0]位（测量参考时钟选择）

RSCS[2:0]位选择用于测量的参考时钟。

RCDS[1:0]位（测量参考时钟分频比选择）

TheRCDS[1:0]bitsselectthedivisionratioofthereferececlockwhenaninternalreferenceclockisselected(RPS=1).
当RPS=0（CACREF引脚用作参考时钟源）时，参考时钟不分频。

DFS[1:0]位（数字滤波器选择）

DFS[1:0]位启用或禁用数字滤波器并选择其采样时钟。

10.2.4 CAC Interrupt Control Register (CAICR)

Address(es): CAC.CAICR 4004 4603h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Request Enable	0: Disable frequency error interrupt request 1: Enable frequency error interrupt request.	R/W
b1	MENDIE	Measurement End Interrupt Request Enable	0: Disable measurement end interrupt request 1: Enable measurement end interrupt request.	R/W
b2	OVFIE	Overflow Interrupt Request Enable	0: Disable overflow interrupt request 1: Enable overflow interrupt request.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	When 1 is written to this bit, the FERRF flag is cleared. This bit is read as 0.	R/W
b5	MENDFCL	MENDF Clear	When 1 is written to this bit, the MENDF flag is cleared. This bit is read as 0.	R/W
b6	OVFFCL	OVFF Clear	When 1 is written to this bit, the OVFF flag is cleared. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the OVFF flag.

10.2.4 CAC中断控制寄存器(CAICR)

Address(es): CAC.CAICR 4004 4603h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FERRIE	频率错误中断请求Enable	0：禁止频率错误中断请求1：允许频率错误中断请求。	R/W
b1	MENDIE	测量结束中断请求启用	0：禁止测量结束中断请求1：允许测量结束中断请求。	R/W
b2	OVFIE	溢出中断请求使能	0：禁止溢出中断请求1：使能溢出中断请求。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	FERRFCL	FERRF Clear	当向该位写入1时，FERRF标志被清除。该位读为0。	R/W
b5	MENDFCL	MENDF Clear	向该位写入1时，清除MENDF标志。该位读为0。	R/W
b6	OVFFCL	OVFF Clear	当向该位写入1时，OVFF标志被清除。该位读为0。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

FERRIE位（频率错误中断请求使能）

FERRIE位使能频率错误中断请求。

MENDIE位（测量结束中断请求使能）

MENDIE位使能测量结束中断请求。

OVFIE位（溢出中断请求使能）

OVFIE位使能溢出中断请求。

FERRFCL位（FERRF清除）

将FERRFCL位设置为1会清除FERRF标志。

MENDFCL位（MENDF清除）

将MENDFCL位设置为1会清除MENDF标志。

OVFFCL位（OVFF清除）

将OVFFCL位设置为1会清除OVFF标志。

10.2.5 CAC Status Register (CASTR)

Address(es): CAC.CASTR 4004 4604h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRF	Frequency Error Flag	0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress 1: Measurement ended.	R
b2	OVFF	Overflow Flag	0: The counter has not overflowed 1: The counter overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflowed.

[Clearing condition]

- 1 is written to the OVFFCL bit.

10.2.5 CAC状态寄存器(CASTR)

Address(es): CAC.CASTR 4004 4604h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FERRF	频率错误标志	0：时钟频率在允许范围内1：时钟频率偏离允许范围（频率误差）。	R
b1	MENDF	测量结束标志	0：测量中1：测量结束。	R
b2	OVFF	溢出标志	0：计数器未溢出1：计数器溢出。	R
b7 to b3	—	Reserved	这些位被读为0	R

FERRF标志（频率误差标志）

FERRF标志表示时钟频率与设定值的偏差（频率误差）。

[Setting condition]

- 时钟频率超出CAULVR和CALLVR寄存器中定义的允许范围。

[Clearing condition]

- 1被写入FERRFCL位。

MENDF标志（测量结束标志）

MENDF标志表示测量结束。

[Setting condition]

- 测量结束。

[Clearing condition]

- 1被写入MENDFCL位。

OVFF标志（溢出标志）

OVFF标志表示计数器溢出。

[Setting condition]

- 计数器溢出。

[Clearing condition]

- 1写入OVFFCL位。

10.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address(es): CAC.CAULVR 4004 4606h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value rises above the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

10.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address(es): CAC.CALLVR 4004 4608h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected.

Write to this register when the CACR0.CFME bit is 0.

10.2.8 CAC Counter Buffer Register (CACNTBR)

Address(es): CAC.CACNTBR 4004 460Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR is a 16-bit read-only register that retains the measurement result.

10.3 Operation

10.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or the internal clock as a reference. Figure 10.2 shows an operating example of the CAC.

10.2.6 CAC上限值设置寄存器(CAULVR)

Address(es): CAC.CAULVR 4004 4606h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR是一个16位读写寄存器，用于指定允许范围的上限值。当计数器值高于此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。

存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。

10.2.7 CAC下限值设置寄存器(CALLVR)

Address(es): CAC.CALLVR 4004 4608h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR是一个16位读写寄存器，用于指定允许范围的下限值。当计数器值低于此寄存器中指定的值时，检测到频率错误。

当CACR0.CFME位为0时写入该寄存器。

10.2.8 CAC计数器缓冲寄存器(CACNTBR)

Address(es): CAC.CACNTBR 4004 460Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR是一个16位只读寄存器，用于保存测量结果。

10.3 Operation

10.3.1 测量时钟频率

CAC使用CACREF引脚输入或内部时钟作为参考来测量时钟频率。图10.2显示了CAC的操作示例。

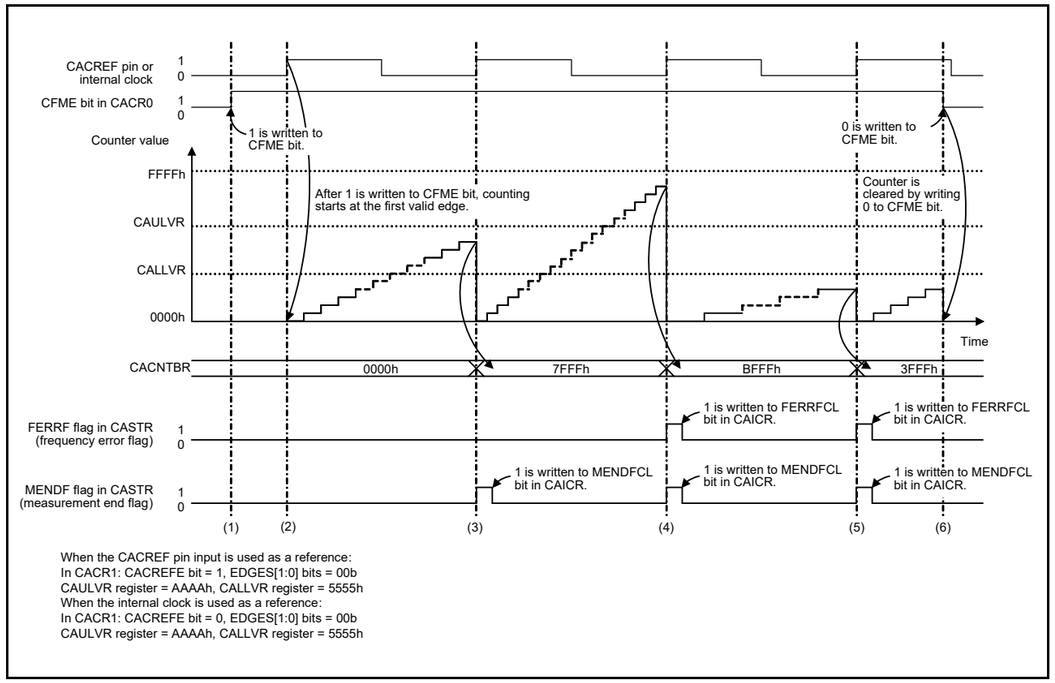


Figure 10.2 CAC operating example

1. Before writing 1 to CACR0.CFME, set CACR1 and CACR2 to define the measurement target clock and measurement reference clock. Writing 1 to the CACR0.CFME bit enables clock frequency measurement.
2. The timer starts counting up if the valid edge selected in the CACR1.EDGES[1:0] bits is input from the measurement reference clock. The valid edge is a rising edge (CACR1.EDGES[1:0] = 00b) as shown in Figure 10.2.
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1 because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values of CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops counting up.

10.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are

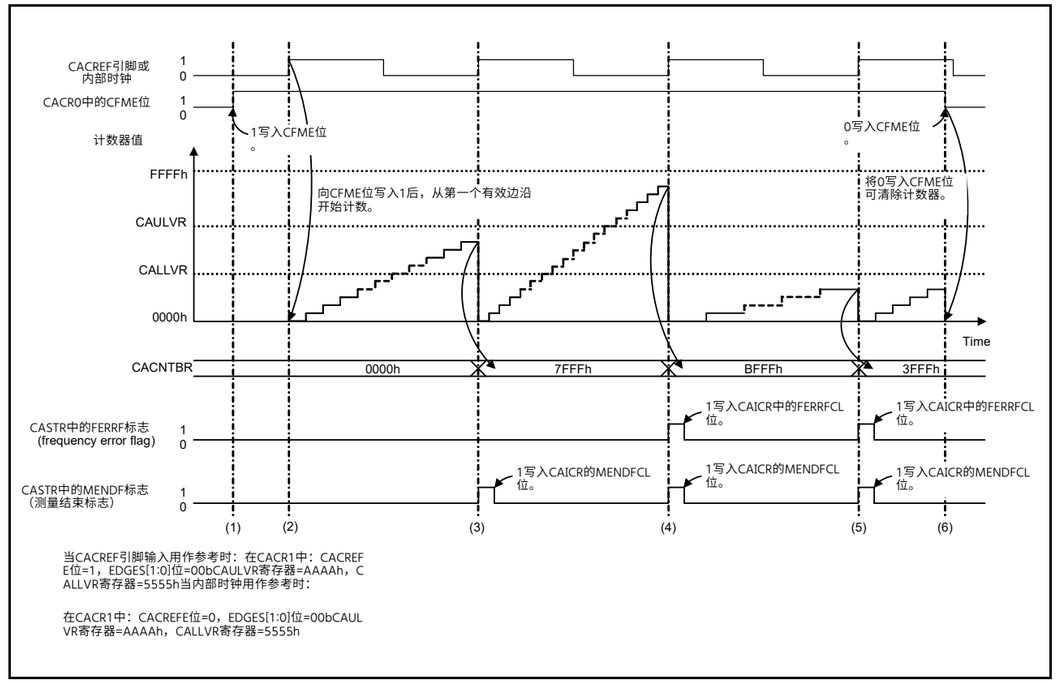


Figure 10.2 CAC操作示例

1. 在向CACR0.CFME写入1之前，设置CACR1和CACR2以定义测量目标时钟和测量参考时钟。向CACR0.CFME位写入1可启用时钟频率测量。
2. 如果在CACR1.EDGES[1:0]位中选择的有效边沿从测量参考时钟输入，则定时器开始计数。有效边沿是上升沿(CACR1.EDGES[1:0]=00b)，如图10.2所示。
3. 当输入下一个有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR的值进行比较。如果CACNTBR≤CAULVR和CACNTBR≥CALLVR都为真，则只有CASTR中的MENDF标志设置为1，因为时钟频率正确。如果CAICR中的MENDIE位为1，则产生测量结束中断。
4. 当输入下一个有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR的值进行比较。如果CACNTBR>CAULVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。
5. 当输入下一个有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR的值进行比较。如果CACNTBR<CALLVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。
6. 当CACR0中的CFME位为1时，每次输入有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR的值进行比较。向CACR0中的CFME位写入0会清除计数器并停止向上计数。

10.3.2 CACREF引脚上的信号数字滤波

CACREF引脚有一个数字滤波器，CACREF引脚上的电平在选定的采样间隔内连续三个匹配后传输到内部电路。同一电平继续在内部传输，直到引脚上的电平再次连续匹配三个。启用或禁用数字滤波器及其采样时钟

selectable.

The counter value transferred in CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock) / (1 cycle of the sampling clock)

10.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt.

When an interrupt source is generated, the associated status flag becomes 1. Table 10.3 provides information on the CAC interrupt requests.

Table 10.3 CAC interrupt requests

Interrupt request	Interrupt enable bit	Status flag	Interrupt source
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit.
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	The counter overflows

10.5 Usage Note

10.5.1 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable CAC operation. The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

selectable.

由于数字滤波器的相位和输入到CACREF引脚的信号之间存在差异，CACNTBR中传输的计数器值可能会出现最多1个采样时钟周期的误差。Whenafrequencydividingclockisselectedasacountsourceclock thecountervaluerrorisobtainedusingthefollowingformula:

计数器值误差=（计数源时钟的1个周期）（采样时钟的1个周期）

10.4 中断请求

CAC产生三种类型的中断请求：

- 频率错误中断
- 测量结束中断
- 溢出中断。

产生中断源时，相关的状态标志变为1。表10.3提供了有关CAC中断请求的信息。

Table 10.3 CAC中断请求

中断请求	中断使能位	状态标志	中断源
频率错误中断	CAICR.FERRIE	CASTR.FERRF	CACNTBR与CAULVR和CALLVR比较的结果是CACNTBR>CAULVR或CACNTBR<CALLVR
测量结束中断	CAICR.MENDIE	CASTR.MENDF	从CACREF引脚或内部时钟输入有效边沿 将1写入CACR0.CFME位后，在第一个有效边沿不会发生测量结束中断。
溢出中断	CAICR.OVFIE	CASTR.OVFF	计数器溢出

10.5 使用说明

10.5.1 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CAC操作。CAC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

11. Low Power Modes

11.1 Overview

The MCU provides several functions for reducing power consumption, such as setting clock dividers, stopping modules, selecting power control mode in normal mode, and transitioning to low power modes.

Table 11.1 lists the specifications of the low power mode functions. Table 11.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DMAC, DTC, and SRAM operate.

Table 11.1 Specifications of the low power mode functions

Parameter	Specification
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD) and flash interface clock (FCLK)*1
Module-stop state	Peripheral module functions can be stopped independently
Low power modes	• Sleep mode • Software Standby mode • Snooze mode.
Power control modes	Power consumption can be reduced in Normal, Sleep, and Snooze mode by selecting an appropriate operating power control mode according to the operating frequency and voltage. Five operating power control modes are available: • High-speed mode • Middle-speed mode • Low-speed mode • Low-voltage mode • Subosc-speed mode.

Note 1. For details, see section 9, Clock Generation Circuit.

Table 11.2 Operating conditions of each low power mode (1 of 2)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1	Snooze request in Software Standby mode. SNZCR.SNZE = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)
State after cancellation by a reset	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*2
Sub-clock oscillator	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable
Middle-speed on-chip oscillator	Selectable	Stop	Selectable
Low-speed on-chip oscillator	Selectable	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*4	Selectable*4	Selectable*4
PLL	Selectable	Stop	Selectable*2
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*3	Selectable
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)
SRAM (ECC SRAM included)	Selectable	Stop (Retained)	Selectable
Flash memory	Operating	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	Operation prohibited
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable

11. 低功耗模式

11.1 Overview

MCU提供了多种降低功耗的功能，例如设置时钟分频器、停止模块、在正常模式下选择电源控制模式以及转换到低功耗模式。

表11.1列出了低功耗模式功能的规格。表11.2列出了转换到低功耗模式的条件、CPU和外围模块的状态以及取消每种模式的方法。复位后，MCU进入程序执行状态，但只有DMAC、DTC和SRAM运行。

Table 11.1 低功耗模式功能的规格

Parameter	Specification
通过切换时钟信号降低功耗	分频比可独立选择系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）和闪存接口时钟（FCLK）*1
Module-stop state	外围模块功能可独立停止
低功耗模式	睡眠模式 软件待机模式 贪睡模式。
电源控制模式	根据工作频率和电压选择合适的工作功率控制模式，可以降低Normal、Sleep和Snooze模式下的功耗。有五种工作功率控制模式可供选择： 高速模式 中速模式 低速模式 低电压模式 Subosc速度模式。

Note 1. 有关详细信息，请参见第9节，时钟生成电路。

Table 11.2 每种低功耗模式的运行条件（2个中的1个）

Parameter	睡眠模式	软件待机模式	Snooze mode*1
过渡条件	WFI指令同时 SBYCR.SSBY = 0	WFI指令同时 SBYCR.SSBY = 1	软件待机模式下的贪睡请求。 SNZCR.SNZE = 1
取消方法	所有中断。 该模式下可用的任何复位。	中断如表11.3所示。该模式下可用的任何复位。	中断如表11.3所示。该模式下可用的任何复位。
中断取消后的状态	程序执行状态（中断处理）	程序执行状态（中断处理）	程序执行状态（中断处理）
通过复位取消后的状态	重置状态	重置状态	重置状态
主时钟振荡器	Selectable	Stop	Selectable*2
Sub-clock oscillator	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable
Middle-speed on-chip oscillator	Selectable	Stop	Selectable
Low-speed on-chip oscillator	Selectable	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*4	Selectable*4	Selectable*4
PLL	Selectable	Stop	Selectable*2
振荡停止检测功能	Selectable	禁止操作	禁止操作
时钟蜂鸣器输出功能	Selectable	Selectable*3	Selectable
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)
SRAM (ECC SRAM included)	Selectable	Stop (Retained)	Selectable
闪存	Operating	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	禁止操作
数据传输控制器(DTC)	Selectable	Stop (Retained)	Selectable

Table 11.2 Operating conditions of each low power mode (2 of 2)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1
USB 2.0 Full-Speed Module (USBFS)	Selectable	Stop (Retained)*5	Operation prohibited*5
Watchdog Timer (WDT)	Selectable*4	Stop (Retained)	Stop (Retained)
Independent Watchdog Timer (IWDT)	Selectable*4	Selectable*4	Selectable*4
Realtime clock (RTC)	Selectable	Selectable	Selectable
Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable	Selectable*6	Selectable*6
14-Bit A/D Converter (ADC14)	Selectable	Stop (Retained)	Selectable*11
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable
Capacitive Touch Sensing Unit (CTSU)	Selectable	Stop (Retained)	Selectable
Segment LCD Controller (SLCDC)	Selectable	Selectable*7	Selectable
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable*10
Serial Communications Interface (SCIn, n = 1, 4, 9)	Selectable	Stop (Retained)	Operation prohibited
I2C Bus Interface (IIC0)	Selectable	Selectable	Selectable
I2C Bus Interface (IIC1)	Selectable	Stop (Retained)	Operation prohibited
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*8
Low-Power Analog Comparator (ACMPLP0)	Selectable	Selectable*9	Selectable*9
Low-Power Analog Comparator (ACMPLP1)	Selectable	Selectable*9	Selectable*9
Operational Amplifier (OPAMP)	Selectable	Selectable	Selectable
NMI, IRQn (n = 0 to 4, 6, 7, 9, 11, 14, 15) pin interrupt	Selectable	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable	Selectable
Low Voltage Detection (LVD)	Selectable	Selectable	Selectable
Power-on reset circuit	Operating	Operating	Operating
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited
I/O ports	Operating	Retained	Operating

Note: Selectable means that operating or not operating can be selected in the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.

Note 1. All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. To avoid an increase in power consumption in Snooze mode, set the module-stop bit of modules that are not required in Snooze mode to 1 before entering Software Standby mode.

Note 2. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP bits must be 1.

Note 3. Stopped when the Clock Output Source Select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).

Note 4. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select Register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in the Option Function Select Register 0 in WDT auto start mode.

Note 5. Detection of USBFS resumption is possible.

Note 6. AGT0 operation is possible when 100b (LOCO) or 110b (SOSC) is selected in the AGT0.AGTMR1.TCK[2:0] bits. AGT1 operation is possible when 100b (LOCO), 110b (SOSC), or 101 (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

Note 7. Operation is possible when 000b (LOCO) or 001b (SOSC) is selected in the SLCDSCKCR.LCDSCKSEL[2:0] bits. Stopping is selected when the SLCDSCKCR.LCDSCKSEL[2:0] bits are set to a value other than 000b or 001b.

Note 8. Event lists the restrictions described in section 11.9.13, ELC Event in Snooze Mode.

Note 9. Only VCOUT function is permitted. The VCOUT pin operates when ACMPLP uses no digital filter. For details on digital filter, see section 38, Low Power Analog Comparator (ACMPLP).

Note 10. Serial communication modes of SCI0 is only in asynchronous mode.

Note 11. When using the ADC14 in Snooze mode, the ADCMPCR.CMPAE or ADCMPCR.CMPBE bit must be 1.

Table 11.2 每种低功耗模式的操作条件（2个中的2个）

Parameter	睡眠模式	软件待机模式	Snooze mode*1
USB2.0全速模块(USBFS)	Selectable	Stop (Retained)*5	Operation prohibited*5
看门狗定时器(WDT)	Selectable*4	Stop (Retained)	Stop (Retained)
独立看门狗定时器(IWDT)	Selectable*4	Selectable*4	Selectable*4
实时时钟(RTC)	Selectable	Selectable	Selectable
异步通用定时器(AGTn n=0 1)	Selectable	Selectable*6	Selectable*6
14-Bit A/D Converter (ADC14)	Selectable	Stop (Retained)	Selectable*11
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable
电容式触控感应单元(CTSU)	Selectable	Stop (Retained)	Selectable
段式LCD控制器(SLCDC)	Selectable	Selectable*7	Selectable
数据运算电路(DOC)	Selectable	Stop (Retained)	Selectable
串行通信接口(SCI0)	Selectable	Stop (Retained)	Selectable*10
串行通信接口(SCIn n=1 4 9)	Selectable	Stop (Retained)	禁止操作
I2C总线接口(IIC0)	Selectable	Selectable	Selectable
I2C总线接口(IIC1)	Selectable	Stop (Retained)	禁止操作
事件链接控制器(ELC)	Selectable	Stop (Retained)	Selectable*8
低功耗模拟比较器(ACMPLP0)	Selectable	Selectable*9	Selectable*9
低功耗模拟比较器(ACMPLP1)	Selectable	Selectable*9	Selectable*9
运算放大器(OPAMP)	Selectable	Selectable	Selectable
NMI IRQn(n=0to4 6 7 9 11 14 15)引脚中断	Selectable	Selectable	Selectable
按键中断功能(KINT)	Selectable	Selectable	Selectable
低电压检测(LVD)	Selectable	Selectable	Selectable
上电复位电路	Operating	Operating	Operating
其他外围模块	Selectable	Stop (Retained)	禁止操作
I/O ports	Operating	Retained	Operating

Note: 可选意味着可以在控制寄存器中选择操作或不操作。
停止（Retained）表示内部寄存器的内容被保留但操作被暂停。
禁止操作意味着在进入软件待机模式之前必须停止该功能。

Note 1. 进入贪睡模式后，一旦提供PCLK，所有模块停止位为0的模块都会启动。为避免贪睡模式下的功耗增加，请在进入软件待机模式之前将贪睡模式下不需要的模块的模块停止位设置为1。

Note 2. 在贪睡模式下使用SCI0时，MOSCCR.MOSTP和PLLCR.PLLSTP位必须为1。

Note 3. 当时钟输出源选择位(CKOCR.CKOSEL[2:0])设置为010b(LOCO)和100b(SOSC)以外的值时停止。

Note 4. 在IWDT专用片内振荡器和IWDT中，在IWDT自动启动模式下，通过设置选项功能选择寄存器0(OFS0)中的IWDT停止控制位(IWDTSTPCL)来选择操作或停止。在WDT中，通过在WDT自动启动模式下设置选项功能选择寄存器0中的WDT停止控制位(WDTSTPCTL)来选择操作或停止。

Note 5. 可以检测USBFS恢复。

Note 6. 当在AGT0.AGTMR1.TCK[2:0]位中选择100b(LOCO)或110b(SOSC)时，可以进行AGT0操作。当在AGT1.AGTMR1.TCK[2:0]位中选择100b(LOCO)、110b(SOSC)或101（来自AGT0的下溢事件信号）时，可以进行AGT1操作。

Note 7. 当在SLCDSCKCR.LCDSCKSEL[2:0]位中选择000b(LOCO)或001b(SOSC)时，可以进行操作。当SLCDSCKCR.LCDSCKSEL[2:0]位设置为000b或001b以外的值时，选择停止。

Note 8. 事件列出了第11.9.13节"贪睡模式下的ELC事件"中描述的限制。

注9.仅允许使用VCOUT功能。当ACMPLP不使用数字滤波器时，VCOUT引脚工作。有关数字滤波器的详细信息，请参见第38节，低功耗模拟比较器(ACMPLP)。注10.SCI0的串行通信模式仅在异步模式下。

注11.在贪睡模式下使用ADC14时，ADCMPCR.CMPAE或ADCMPCR.CMPBE位必须为1。

Table 11.3 Interrupt sources to transition to Normal mode from Snooze mode and Software Standby mode

Interrupt source	Name	Software Standby mode	Snooze mode
NMI		Yes	Yes
VBATT	VBATT_LVD	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes
USBFS	USBFS_USBR	Yes	Yes
RTC	RTC_ALM	Yes	Yes
	RTC_PRD	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPLP	ACMP_LP0	Yes	Yes
IIC0	IIC0_WUI	Yes	Yes
ADC140	ADC140_WCMPM	No	Yes with SELSR0*1,*3
	ADC140_WCMPUM	No	Yes with SELSR0*1,*3
SCI0	SCI0_AM	No	Yes with SELSR0*1,*2
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1,*2
DTC	DTC_COMPLETE	No	Yes with SELSR0*1,*3
DOC	DOC_DOPCI	No	Yes with SELSR0*1
CTSU	CTSU_CTSUFN	No	Yes with SELSR0*1

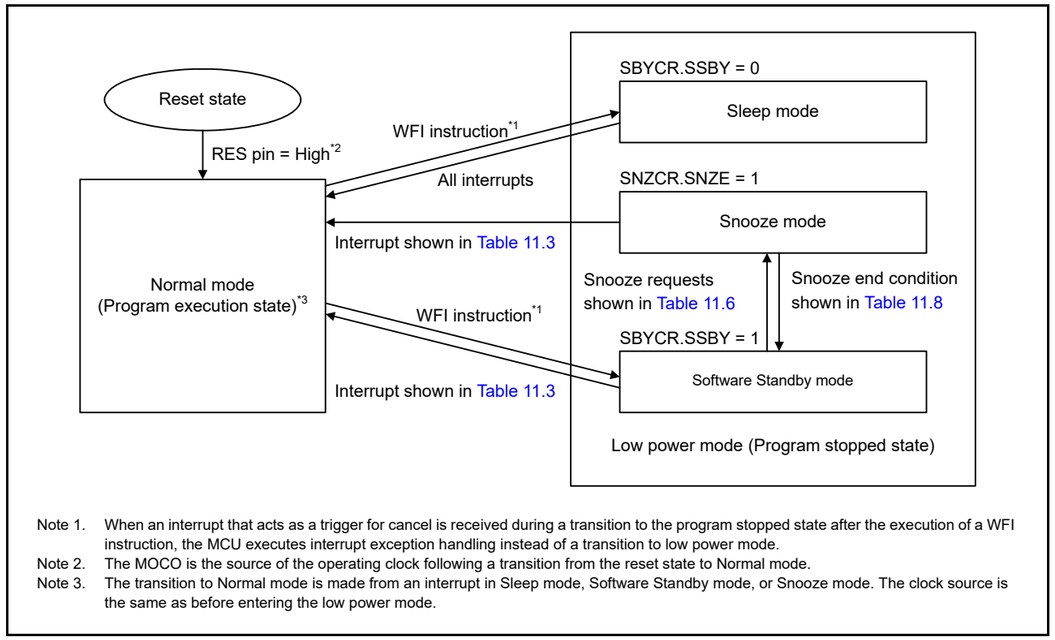
Note 1. To use the interrupt request as a trigger for exiting Snooze mode, the request must be selected in SELSR0. See section 14, Interrupt Controller Unit (ICU). When a trigger selected in SELSR0 occurs after executing a WFI instruction and during the transition from Normal mode to Software Standby mode, whether the request can be accepted depends on the timing of the occurrence.
Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be selected.
Note 3. The event that is enabled by SNZEDCR must not be used.

Table 11.3 从贪睡模式和软件待机模式转换到正常模式的中断源

中断源	Name	软件待机模式	贪睡模式
NMI		Yes	Yes
VBATT	VBATT_LVD	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes
USBFS	USBFS_USBR	Yes	Yes
RTC	RTC_ALM	Yes	Yes
	RTC_PRD	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPLP	ACMP_LP0	Yes	Yes
IIC0	IIC0_WUI	Yes	Yes
ADC140	ADC140_WCMPM	No	是SELSR0*1 *3
	ADC140_WCMPUM	No	是SELSR0*1 *3
SCI0	SCI0_AM	No	是SELSR0*1 *2
	SCI0_RXI_OR_ERI	No	是SELSR0*1 *2
DTC	DTC_COMPLETE	No	是SELSR0*1 *3
DOC	DOC_DOPCI	No	是SELSR0*1
CTSU	CTSU_CTSUFN	No	是SELSR0*1

Note 1. 要将中断请求用作退出贪睡模式的触发器，必须在SELSR0中选择该请求。参见第14节，中断控制器单元(ICU)。当SELSR0中选择的触发发生在执行WFI指令之后以及从正常模式到软件待机模式的转换期间，是否可以接受请求取决于发生的时间。

Note 2. 只能选择SCI0_AM或SCI0_RXI_OR_ERI之一。
Note 3. 不得使用由SNZEDCR启用的事件。



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of a transition to low power mode.
Note 2. The MOCO is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made from an interrupt in Sleep mode, Software Standby mode, or Snooze mode. The clock source is the same as before entering the low power mode.

Figure 11.1 Mode transitions

11.2 Register Descriptions

11.2.1 Standby Control Register (SBYCR)

Address(es): SYSTEM.SBYCR 4001 E00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

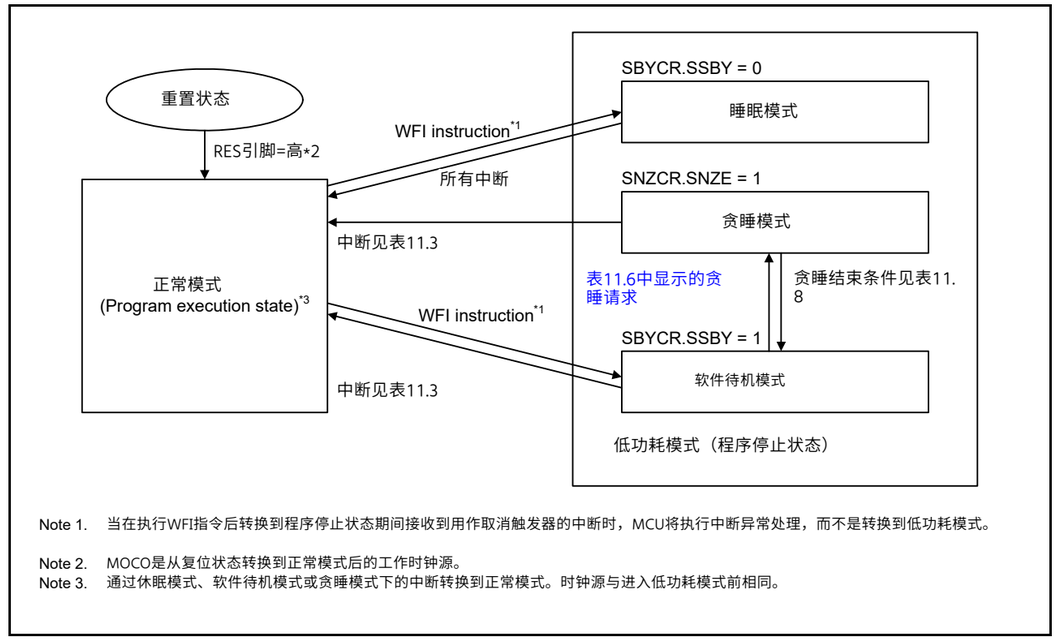
Bit	Symbol	Bit name	Description	R/W
b13 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	OPE	Output Port Enable	0: In Software Standby mode, the address bus and bus control signals are set to the high-impedance state. In Snooze mode, the address bus and bus control signals are the same as before entering Software Standby mode. 1: In Software Standby mode, the address bus and bus control signals retain the output state.	R/W
b15	SSBY	Software Standby	0: Sleep mode 1: Software Standby mode.	R/W

OPE bit (Output Port Enable)

The OPE bit specifies whether to set to the high-impedance state or to retain the output of the address bus and bus control signals (CS0 to CS3, RD, WR0, WR1, WR, BC0, BC1, and ALE) in Software Standby or Snooze mode.

SSBY bit (Software Standby)

The SSBY bit specifies the transition destination after a WFI instruction is executed.



Note 1. 当在执行WFI指令后转换到程序停止状态期间接收到用作取消触发器的中断时，MCU将执行中断异常处理，而不是转换到低功耗模式。
Note 2. MOCO是从复位状态转换到正常模式后的工作时钟源。
Note 3. 通过休眠模式、软件待机模式或贪睡模式下的中断转换到正常模式。时钟源与进入低功耗模式前相同。

Figure 11.1 模式转换

11.2 注册说明

11.2.1 待机控制寄存器(SBYCR)

Address(es): SYSTEM.SBYCR 4001 E00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	OPE	输出端口使能	0：在软件待机模式下，地址总线和总线控制信号设置为高阻状态。在贪睡模式下，地址总线和总线控制信号与进入软件待机模式前相同。1：在软件待机模式下，地址总线和总线控制信号保持输出状态。	R/W
b15	SSBY	软件待机	0：休眠模式1：软件待机模式。	R/W

OPE位（输出端口使能）

OPE位指定在软件待机或软件待机时是否设置为高阻抗状态或保留地址总线和总线控制信号（CS0至CS3、RD、WR0、WR1、WR、BC0、BC1和ALE）的输出。贪睡模式。

SSBY位（软件待机）

SSBY位指定执行WFI指令后的转移目标。

When the SSBY bit is set to 1, the MCU enters Software Standby mode after execution of a WFI instruction. When the MCU returns to Normal mode from Software Standby mode due to an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

When the OSTDCR.OSTDE bit is 1, the SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

When the FENTRYR.FENTRY0 bit is 1 or the FENTRYR.FENTRYD bit is 1, the setting of SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

11.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): SYSTEM.MSTPCRA 4001 E01Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	MSTPA6	—	—	—	—	—	MSTPA0
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	MSTPA0	SRAM0 Module Stop*1	Target module: SRAM0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b5 to b1	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b6	MSTPA6	ECCSRAM Module Stop*1	Target module: ECCSRAM 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPA22	DMA Controller/Data Transfer Controller Module Stop*2	Target module: DMAC/DTC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31 to b23	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. The MSTPA0 and MSTPA6 bit settings must be the same.
Note 2. When rewriting the MSTPA22 bit from 0 to 1, disable the DMAC and DTC before setting the MSTPA22 bit.

11.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): MSTP.MSTPCRB 4004 7000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	—	MSTPB28	MSTPB27	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTPB11	—	MSTPB9	MSTPB8	—	—	—	—	—	MSTPB2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

当SSBY位设置为1时，MCU在执行WFI指令后进入软件待机模式。当MCU由于中断而从软件待机模式返回正常模式时，SSBY位保持为1。SSBY位可以通过向其写入0来清除。

当OSTDCR.OSTDE位为1时，SSBY位被忽略。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

当FENTRYR.FENTRY0位为1或FENTRYR.FENTRYD位为1时，忽略SSBY位的设置。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

11.2.2 模块停止控制寄存器A(MSTPCRA)

Address(es): SYSTEM.MSTPCRA 4001 E01Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	MSTPA6	—	—	—	—	—	MSTPA0
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0

Bit	Symbol	位名称	Description	R/W
b0	MSTPA0	SRAM0 Module Stop*1	目标模块：SRAM00：取消模块停止状态1：进入模块停止状态。	R/W
b5 to b1	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b6	MSTPA6	ECCSRAM Module Stop*1	目标模块：ECCSRAM0：取消模块停止状态1：进入模块停止状态。	R/W
b21 to b7	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b22	MSTPA22	DMA Controller/Data 传输控制器模块 Stop*2	目标模块：DMACDTC0：取消模块停止状态1：进入模块停止状态。	R/W
b31 to b23	—	Reserved	这些位被读取为1。写入值应为1。	R/W

Note 1. MSTPA0和MSTPA6位设置必须相同。
Note 2. 将MSTPA22位从0重写为1时，在设置MSTPA22位之前禁用DMAC和DTC。

11.2.3 模块停止控制寄存器B(MSTPCRB)

Address(es): MSTP.MSTPCRB 4004 7000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	—	MSTPB28	MSTPB27	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTPB11	—	MSTPB9	MSTPB8	—	—	—	—	—	MSTPB2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为1。写入值应为1。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	MSTPB2	Controller Area Network Module Stop*1	Target module: CAN0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7 to b3	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b8	MSTPB8	I2C Bus Interface 1 Module Stop	Target module: IIC1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b9	MSTPB9	I2C Bus Interface 0 Module Stop	Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b11	MSTPB11	Universal Serial Bus 2.0 FS Interface Module Stop*2	Target module: USBFS 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b17 to b12	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b18	MSTPB18	Serial Peripheral Interface 1 Module Stop	Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b19	MSTPB19	Serial Peripheral Interface 0 Module Stop	Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21, b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPB22	Serial Communication Interface 9 Module Stop	Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b26 to b23	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b27	MSTPB27	Serial Communication Interface 4 Module Stop	Target module: SCI4 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b28	MSTPB28	Serial Communication Interface Module stop for BLE*3	Target module: SCI for BLE 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b29	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31	MSTPB31	Serial Communication Interface 0 Module Stop	Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPB2 bit must be written while the oscillation of the clock controlled by this bit is stable. To enter Software Standby mode after writing to this bit, wait for 2 CAN clock (CANMCLK) cycles after writing, then execute a WFI instruction.
Note 2. To enter Software Standby mode after writing to the MSTPB11 bit, wait for 2 USB clock (UCLK) cycles after writing, then execute a WFI instruction.
Note 3. The Bluetooth middleware executes processing in response to this module stop. Do not change the setting of this bit.

Bit	Symbol	位名称	Description	R/W
b2	MSTPB2	控制器局域网 Module Stop*1	目标模块：CAN00：取消模块 停止状态1：进入模块停止状态 。	R/W
b7 to b3	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b8	MSTPB8	I2C总线接口1模块 Stop	目标模块：IIC10：取消模块停 止状态1：进入模块停止状态。	R/W
b9	MSTPB9	I2C总线接口0模块 Stop	目标模块：IIC00：取消模块停 止状态1：进入模块停止状态。	R/W
b10	—	Reserved	该位读取为1。写入值应为1。	R/W
b11	MSTPB11	通用串行总线2.0FS 接口模块停止*2	目标模块：USBFS0：取消模块 停止状态1：进入模块停止状态 。	R/W
b17 to b12	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b18	MSTPB18	串行外设接口1 模块停止	目标模块：SPI10：取消模块停 止状态1：进入模块停止状态。	R/W
b19	MSTPB19	串行外设接口0 模块停止	目标模块：SPI00：取消模块停 止状态1：进入模块停止状态。	R/W
b21, b20	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b22	MSTPB22	串行通讯接口9模块停 止	目标模块：SCI90：取消模块停 止状态1：进入模块停止状态。	R/W
b26 to b23	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b27	MSTPB27	串行通讯接口4模块停 止	目标模块：SCI40：取消模块停 止状态1：进入模块停止状态。	R/W
b28	MSTPB28	串行通信 接口模块停止 BLE*3	目标模块：SCIforBLE0：取消模 块停止状态1：进入模块停止状 态。	R/W
b29	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b30	MSTPB30	串行通讯接口1模块停 止	目标模块：SCI10：取消模块停 止状态1：进入模块停止状态。	R/W
b31	MSTPB31	串行通讯接口0模块停 止	目标模块：SCI00：取消模块停 止状态1：进入模块停止状态。	R/W

Note 1. MSTPB2位必须在该位控制的时钟振荡稳定时写入。要在写入该位后进入软件待机模式，写入后等待2个CAN时钟(CANMCLK)周期，然后执行WFI指令。
Note 2. 要在写入MSTPB11位后进入软件待机模式，写入后等待2个USB时钟(UCLK)周期，然后执行WFI指令。
Note 3. 蓝牙中间件响应该模块停止执行处理。请勿更改该位的设置。

11.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): MSTP.MSTPCRC 4004 7004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	MSTPC4	MSTPC3	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	MSTPC0	Clock Frequency Accuracy Measurement Circuit Module Stop*1	Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop	Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b2	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b3	MSTPC3	Capacitive Touch Sensing Unit Module Stop	Target module: CTSU 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4	MSTPC4	Segment LCD Controller Module Stop	Target module: SLCDC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b12 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b13	MSTPC13	Data Operation Circuit Module Stop	Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b14	MSTPC14	Event Link Controller Module Stop	Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30 to b15	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	MSTPC31	SCE5 Module Stop*2	Target module: SCE5 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPC0 bit must be written while the oscillation of the clock to be controlled by this bit is stable. To enter Software Standby mode after writing to this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, and then execute a WFI instruction.

Note 2. Set the MSTPC31 bit to 0 once at the beginning of the program, to initialize an unused circuit, even if the SCE5 is not used in this MCU. See section 11.9.15, Module-Stop Function for an Unused Circuit.

11.2.4 模块停止控制寄存器C(MSTPCRC)

Address(es): MSTP.MSTPCRC 4004 7004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	MSTPC4	MSTPC3	—	MSTPC1	MSTPC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	MSTPC0	时钟频率精度测量电路模块停止*1	目标模块：CAC0：取消模块停止状态1：进入模块停止状态。	R/W
b1	MSTPC1	循环冗余检查计算器模块Stop	目标模块：CRC0：取消模块停止状态1：进入模块停止状态。	R/W
b2	—	Reserved	该位读取为1。写入值应为1。	R/W
b3	MSTPC3	Capacitive Touch传感单元模块停止	目标模块：CTSU0：取消模块停止状态1：进入模块停止状态。	R/W
b4	MSTPC4	段式液晶控制器模块停止	目标模块：SLCDC0：取消模块停止状态1：进入模块停止状态。	R/W
b12 to b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b13	MSTPC13	数据运算电路模块停止	目标模块：DOC0：取消模块停止状态1：进入模块停止状态。	R/W
b14	MSTPC14	事件链接控制器模块停止	目标模块：ELC0：取消模块停止状态1：进入模块停止状态。	R/W
b30 to b15	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b31	MSTPC31	SCE5 Module Stop*2	目标模块：SCE50：取消模块停止状态1：进入模块停止状态。	R/W

Note 1. MSTPC0位必须在该位控制的时钟振荡稳定时写入。进入软件写入该位后的待机模式，等待振荡器输出时钟中最慢时钟的2个周期，然后执行WFI指令。

Note 2. 在程序开始时将MSTPC31位设置为0一次，以初始化未使用的电路，即使SCE5未在该MCU中使用。请参阅第11.9.15节，未使用电路的模块停止功能。

11.2.5 Module Stop Control Register D (MSTPCRD)

Address(es): MSTP.MSTPCRD 4004 7008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPD31	—	MSTPD29	—	—	—	—	—	—	—	—	MSTPD20	MSTPD19	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPD2	Asynchronous General Purpose Timer 1 Module Stop*1	Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b3	MSTPD3	Asynchronous General Purpose Timer 0 Module Stop*2	Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5	MSTPD5	General PWM Timer 323 to 320 Module Stop	Target module: GPT323 to GPT320 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPD6	General PWM Timer 169 to 164 Module Stop	Target module: GPT168, GPT165, GPT164 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b13 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14	MSTPD14	Port Output Enable for GPT Module Stop	Target module: POEG 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b15	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b16	MSTPD16	14-Bit A/D Converter Module Stop	Target module: ADC140 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b18, b17	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b19	MSTPD19	8-Bit D/A Converter Module Stop*3	Target module: DAC8 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b20	MSTPD20	12-Bit D/A Converter Module Stop	Target module: DAC12 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b28 to b21	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b29	MSTPD29	Low-Power Analog Comparator Module Stop	Target module: ACMPLP 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b31	MSTPD31	Operational Amplifier Module Stop	Target module: OPAMP 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.
Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.
Note 3. When using the 8-bit D/A converter (MSTPD19 = 0), set the MSTPD29 bit in ACMPLP to 0.

11.2.5 模块停止控制寄存器D(MSTPCRD)

Address(es): MSTP.MSTPCRD 4004 7008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPD31	—	MSTPD29	—	—	—	—	—	—	—	—	MSTPD20	MSTPD19	—	—	MSTPD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b2	MSTPD2	异步通用 用途定时器1模块 Stop*1	目标模块：AGT10：取消模块停止状态1：进入模块停止状态。	R/W
b3	MSTPD3	异步通用 用途定时器0模块 Stop*2	目标模块：AGT00：取消模块停止状态1：进入模块停止状态。	R/W
b4	—	Reserved	该位读取为1。写入值应为1。	R/W
b5	MSTPD5	通用PWM定时器323至320模块停止	目标模块：GPT323～GPT3200：取消模块停止状态1：进入模块停止状态。	R/W
b6	MSTPD6	通用PWM定时器169至164模块停止	目标模块：GPT168、GPT165、GPT1640：取消模块停止状态1：进入模块停止状态。	R/W
b13 to b7	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b14	MSTPD14	GPT的端口输出使能模块停止	目标模块：POEG0：取消模块停止状态1：进入模块停止状态。	R/W
b15	—	Reserved	该位读取为1。写入值应为1。	R/W
b16	MSTPD16	14位AD转换器模块停止	目标模块：ADC1400：取消模块停止状态1：进入模块停止状态。	R/W
b18, b17	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b19	MSTPD19	8位DA转换器模块停止*3	目标模块：DAC80：取消模块停止状态1：进入模块停止状态。	R/W
b20	MSTPD20	12位DA转换器模块停止	目标模块：DAC120：取消模块停止状态1：进入模块停止状态。	R/W
b28 to b21	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b29	MSTPD29	低功耗模拟比较器模块停止	目标模块：ACMPLP0：取消模块停止状态1：进入模块停止状态。	R/W
b30	—	Reserved	该位读取为1。写入值应为1。	R/W
b31	MSTPD31	运算放大器模块 Stop	目标模块：OPAMP0：取消模块停止状态1：进入模块停止状态。	R/W

Note 1. 当计数源为副时钟振荡器或LOCO时，即使MSTPD2设置为1，AGT1计数也不会停止。如果计数源为副时钟振荡器或LOCO，则该位必须设置为1，除非访问AGT1寄存器。
Note 2. 当计数源为副时钟振荡器或LOCO时，即使MSTPD3设置为1，AGT0计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非访问AGT0寄存器。
Note 3. 使用8位DA转换器(MSTPD19=0)时，将ACMPLP中的MSTPD29位设置为0。

11.2.6 Operating Power Control Register (OPCCR)

Address(es): SYSTEM.OPCCR 4001 E0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OPCM[1:0]	Operating Power Control Mode Select	b1 b0 0 0: High-speed mode 0 1: Middle-speed mode 1 0: Low-voltage mode*1 1 1: Low-speed mode.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	OPCMTSF	Operating Power Control Mode Transition Status Flag	0: Transition completed 1: Transition in progress.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. HOCOCR.HCSTP must always be 0.

The OPCCR register is used to reduce power consumption in Normal mode, Sleep mode and Snooze mode. Power consumption can be reduced according to the operating frequency and operating voltage used by the OPCCR setting.

For the procedure to change the operating power control modes, see section 11.5, Function for Lower Operating Power Consumption.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal mode, Sleep mode, and Snooze mode.

Table 11.4 shows the relationship between the operating power control modes, the OPCM[1:0] and SOPCM bits settings.

Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP and OSCSF.HOCOSF are 0 as the oscillation of the HOCO clock is not yet stable.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag becomes 1 when the OPCM[1:0] bits are written, and 0 when mode transition completed. Read this flag and confirm that it is 0 before proceeding.

11.2.7 Sub Operating Power Control Register (SOPCCR)

Address(es): SYSTEM.SOPCCR 4001 E0AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOPCM	Sub Operating Power Control Mode Select	0: Not Subosc-speed mode 1: Subosc-speed mode.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SOPCMTSF	Sub Operating Power Control Mode Transition Status Flag	0: Transition completed 1: Transition in progress.	R

11.2.6 工作电源控制寄存器(OPCCR)

Address(es): SYSTEM.OPCCR 4001 E0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b1, b0	OPCM[1:0]	工作功率控制 模式选择	b1 b0 0 0: High-speed mode 0 1: Middle-speed mode 1 0: Low-voltage mode*1 1 1: Low-speed mode.	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	OPCMTSF	工作功率控制 模式转换状态标志	0：转换完成1：转换进 行中。	R
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. HOCOCR.HCSTP必须始终为0。

OPCCR寄存器用于降低正常模式、睡眠模式和贪睡模式下的功耗。根据OPCCR设置使用的工作频率和工作电压，可以降低功耗。

有关更改运行功率控制模式的步骤，请参阅第11.5节，降低运行功率的功能
Consumption.

OPCM[1:0]位（工作电源控制模式选择）

OPCM[1:0]位选择正常模式、睡眠模式和贪睡模式下的工作功率控制模式。

表11.4显示了工作功率控制模式、OPCM[1:0]和SOPCM位设置之间的关系。

当HOCOCR.HCSTP和OSCSF.HOCOSF为0时禁止写入OPCCR.OPCM[1:0]，因为HOCO时钟的振荡还不稳定。

OPCMTSF标志（工作电源控制模式转换状态标志）

OPCMTSF标志指示切换操作功率控制模式时的切换控制状态。当写入OPCM[1:0]位时，该标志变为1，当模式转换完成时变为0。阅读此标志并确认其为0，然后再继续。

11.2.7 副操作功率控制寄存器(SOPCCR)

Address(es): SYSTEM.SOPCCR 4001 E0AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SOPCMTSF	—	—	—	SOPCM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SOPCM	副操作功率控制 模式选择	0：非Subosc速度模式1：S ubosc速度模式。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SOPCMTSF	副操作功率控制 模式转换状态标志	0：转换完成1：转换进 行中。	R

Bit	Symbol	Bit name	Description	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SOPCCR register is used to reduce power consumption in Normal mode, Sleep mode, and Snooze mode. Setting this register initiates the entry to and exit from Subosc-speed mode. Subosc-speed mode is available only when using the sub-clock oscillator or LOCO without dividing the frequency.

The flash cache function should be disabled by setting the CACHEE.FCACHEEN bit to 0 before switching the operating power control mode. For details, see section 43., Flash Memory.

For the procedure to change operating power control modes, see section 11.5, Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal mode, Sleep mode, and Snooze mode. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (operating mode set by OPCCR.OPCM[1:0]) that was active before the transition to Subosc-speed mode.

Table 11.4 shows the relationship between the operating power control modes, the OPCM[1:0] and SOPCM bits settings.

SOPCMTSF flag (Sub Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched from or to Subosc-speed mode. This flag becomes 1 when the SOPCM bit is written, and 0 when mode transition completed. Read this flag and confirm that it is 0 before proceeding.

Table 11.4 shows each operating power control mode.

Table 11.4 Operating power control mode

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High ↓
Middle-speed mode	01b	0	
Low-voltage mode	10b	0	
Low-speed mode	11b	0	
Subosc-speed mode	xxb	1	Low

11.2.8 Snooze Control Register (SNZCR)

Address(es): SYSTEM.SNZCR 4001 E092h

	b7	b6	b5	b4	b3	b2	b1	b0
	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RXDREQEN	RXD0 Snooze Request Enable	0: Ignore RXD0 falling edge in Software Standby mode 1: Detect RXD0 falling edge in Software Standby mode.	R/W
b1	SNZDTCEN	DTC Enable in Snooze mode	Enable DTC operation in Snooze mode: 0: Disable DTC operation 1: Enable DTC operation.	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SNZE	Snooze mode Enable	0: Disable Snooze mode 1: Enable Snooze mode.	R/W

Bit	Symbol	位名称	Description	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SOPCCR寄存器用于降低正常模式、睡眠模式和贪睡模式下的功耗。设置该寄存器可启动进入和退出Subosc速度模式。Subosc速度模式仅在使用副时钟振荡器或LOCO而不分频时可用。

在切换工作电源控制模式之前，应通过将CACHEE.FCACHEEN位设置为0来禁用闪存缓存功能。有关详细信息，请参阅第43节，闪存。

有关更改操作功率控制模式的步骤，请参阅第11.5节，降低操作功率的功能
Consumption.

SOPCM位（副工作功率控制模式选择）

SOPCM位选择正常模式、睡眠模式和贪睡模式下的工作功率控制模式。将此位设置为1允许转换到Subosc速度模式。将此位设置为0允许返回到转换到Subosc速度模式之前处于活动状态的操作模式（由OPCCR.OCM[1:0]设置的操作模式）。

表11.4显示了工作功率控制模式、OPCM[1:0]和SOPCM位设置之间的关系。

SOPCMTSF标志（子工作电源控制模式转换状态标志）

SOPCMTSF标志指示当操作功率控制模式从或切换到Subosc速度模式时的切换控制状态。该标志在写入SOPCM位时变为1，在模式转换完成时变为0。阅读此标志并确认其为0，然后再继续。

表11.4显示了每种工作功率控制模式。

Table 11.4 工作功率控制方式

工作功率控制方式	OPCM[1:0] bits	SOPCM bit	能量消耗
High-speed mode	00b	0	High ↓
Middle-speed mode	01b	0	
Low-voltage mode	10b	0	
Low-speed mode	11b	0	
Subosc-speed mode	xxb	1	Low

11.2.8 贪睡控制寄存器(SNZCR)

Address(es): SYSTEM.SNZCR 4001 E092h

	b7	b6	b5	b4	b3	b2	b1	b0
	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RXDREQEN	RXD0贪睡请求启用	0：在软件待机模式下忽略RXD0下降沿1：在软件待机模式下检测RXD0下降沿。	R/W
b1	SNZDTCEN	在贪睡模式下启用DTC	在贪睡模式下启用DTC操作：0：禁用DTC操作1：启用DTC操作。	R/W
b6 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	SNZE	贪睡模式启用	0：禁用贪睡模式1：启用贪睡模式。	R/W

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit is only available when SCI0 operates in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn (ICU Event Link Setting Register n).

SNZE bit (Snooze mode Enable)

The SNZE bit specifies whether to enable a transition from Software Standby mode to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 11.6 in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby mode or Snooze mode to Normal mode, clear the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 11.8, Snooze Mode.

11.2.9 Snooze End Control Register (SNZEDCR)

Address(es): SYSTEM.SNZEDCR 4001 E094h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AGTUNFED	AGT1 Underflow Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b1	DTCZRED	Last DTC Transmission Completion Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b3	AD0MATED	ADC140 Compare Match Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b4	AD0UMTED	ADC140 Compare Mismatch Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable	0: Disable the snooze end request 1: Enable the snooze end request.	R/W

To use a trigger shown in Table 11.8 as a condition to switch from Snooze mode to Software Standby mode, set the associated bit in the SNZEDCR register to 1.

The event that is used to return to Normal mode from Snooze mode listed in Table 11.3 must not be enabled by SNZEDCR.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an AGT1 underflow. For details of the condition of the trigger, see section 24, Asynchronous General Purpose Timer (AGT).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by completion of the last DTC transmission, that is, CRA or CRB registers in the DTC is 0. For details of the condition of the trigger,

RXDREQEN位（RXD0贪睡请求使能）

RXDREQEN位指定在软件待机模式下是否检测RXD0引脚的下降沿。该位仅在SCI0工作在异步模式时可用。要检测RXD0引脚的下降沿，请在进入软件待机模式之前设置该位。当该位设置为1时，软件待机模式下RXD0引脚的下降沿会导致MCU进入贪睡模式。

SNZDTCEN位（在贪睡模式下启用DTC）

SNZDTCEN位指定是否在贪睡模式下使用DTC和SRAM。使用DTC和SRAM
贪睡模式，在进入软件待机模式之前将该位设置为1。当该位设置为1时，可以通过设置IELSRn（ICU事件链接设置寄存器n）来激活DTC。

SNZE位（贪睡模式启用）

SNZE位指定是否启用从软件待机模式到贪睡模式的转换。要使用贪睡模式，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，软件待机模式下如表11.6所示的触发会导致MCU进入贪睡模式。在MCU从软件待机模式或贪睡模式转换到正常模式后，清除一次SNZE位，然后在重新进入软件待机模式之前将其设置。有关详细信息，请参阅第11.8节，贪睡模式。

11.2.9 贪睡结束控制寄存器(SNZEDCR)

Address(es): SYSTEM.SNZEDCR 4001 E094h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	AGTUNFED	AGT1下溢贪睡结束Enable	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b1	DTCZRED	最后一次DTC传输完成贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b2	DTCNZRED	不是最后一次DTC传输完成贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b3	AD0MATED	ADC140比较匹配贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b4	AD0UMTED	ADC140比较失配贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	SCI0UMTED	SCI0地址不匹配贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W

要将表11.8中所示的触发器用作从贪睡模式切换到软件待机模式的条件，请将SNZEDCR寄存器中的相关位设置为1。

表11.3中列出的用于从贪睡模式返回到正常模式的事件不得由
SNZEDCR.

AGTUNFED位（AGT1下溢贪睡结束使能）

AGTUNFED位指定是否允许通过AGT1下溢从贪睡模式转换到软件待机模式。有关触发条件的详细信息，请参见第24节，异步通用定时器(AGT)。

DTCZRED位（最后一个DTC传输完成贪睡结束使能）

DTCZRED位指定是否通过完成最后一次DTC传输来使能从贪睡模式到软件待机模式的转换，即DTC中的CRA或CRB寄存器为0。有关触发条件的详细信息，

see section 18, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by completion of each DTC transmission, that is, CRA or CRB registers in the DTC is not 0. For details of the condition of the trigger, see section 18, Data Transfer Controller (DTC).

AD0MATED bit (ADC140 Compare Match Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an ADC140 event when a conversion result matches the expected data. For details of the condition of the trigger, see section 34, 14-Bit A/D Converter (ADC14).

AD0UMTED bit (ADC140 Compare Mismatch Snooze End Enable)

The AD0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an ADC140 event when the conversion result does not match the expected data. For details of the condition of the trigger, see section 34, 14-Bit A/D Converter (ADC14).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an SCI0 event when an address received in Software Standby mode does not match the expected data. For details of the condition of the trigger, see section 29, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

11.2.10 Snooze Request Control Register (SNZREQCR)

Address(es): SYSTEM.SNZREQCR 4001 E098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	SNZREQEN23	—	—	—	—	—	SNZREQEN17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SNZREQEN15	SNZREQEN14	—	—	SNZREQEN11	—	SNZREQEN9	—	SNZREQEN7	SNZREQEN6	—	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SNZREQEN0	Snooze Request Enable 0	Enable IRQ0 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b1	SNZREQEN1	Snooze Request Enable 1	Enable IRQ1 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b2	SNZREQEN2	Snooze Request Enable 2	Enable IRQ2 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b3	SNZREQEN3	Snooze Request Enable 3	Enable IRQ3 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b4	SNZREQEN4	Snooze Request Enable 4	Enable IRQ4 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	SNZREQEN6	Snooze Request Enable 6	Enable IRQ6 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W

请参见第18节，数据传输控制器(DTC)。

DTCNZRED位（非最后一个DTC传输完成贪睡结束使能）

DTCNZRED位指定是否通过完成每个DTC传输来使能从贪睡模式到软件待机模式的转换，即DTC中的CRA或CRB寄存器不为0。有关触发条件的详细信息，请参阅第18节，数据传输控制器(DTC)。

AD0MATED位（ADC140比较匹配贪睡结束使能）

AD0MATED位指定是否启用从贪睡模式到软件待机模式的转换
转换结果与预期数据匹配时的ADC140事件。有关触发条件的详细信息，请参见第34节，14位AD转换器(ADC14)。

AD0UMTED位（ADC140比较不匹配贪睡结束使能）

AD0UMTED位指定是否启用从贪睡模式到软件待机模式的转换
转换结果与预期数据不匹配时发生ADC140事件。有关触发条件的详细信息，请参见第34节，14位AD转换器(ADC14)。

SCI0UMTED位（SCI0地址不匹配贪睡结束使能）

SCI0UMTED位指定当在软件待机模式下接收到的地址与预期数据不匹配时，是否通过SCI0事件使能从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第29节，串行通信接口(SCI)。仅当SCI0在异步模式下工作时将该位设置为1。

11.2.10 贪睡请求控制寄存器(SNZREQCR)

Address(es): SYSTEM.SNZREQCR 4001 E098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	SNZREQEN23	—	—	—	—	—	SNZREQEN17	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SNZREQEN15	SNZREQEN14	—	—	SNZREQEN11	—	SNZREQEN9	—	SNZREQEN7	SNZREQEN6	—	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SNZREQEN0	暂停请求启用0	启用IRQ0引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b1	SNZREQEN1	贪睡请求启用1	启用IRQ1引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b2	SNZREQEN2	贪睡请求启用2	EnableIRQ2pinsnoozerequest：0：禁用贪睡请求1：启用贪睡请求。	R/W
b3	SNZREQEN3	贪睡请求启用3	EnableIRQ3pinsnoozerequest：0：禁用贪睡请求1：启用贪睡请求。	R/W
b4	SNZREQEN4	贪睡请求启用4	EnableIRQ4pinsnoozerequest：0：禁用贪睡请求1：启用贪睡请求。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	SNZREQEN6	贪睡请求启用6	启用IRQ6引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	SNZREQEN7	Snooze Request Enable 7	Enable IRQ7 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9	SNZREQEN9	Snooze Request Enable 9	Enable IRQ9 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	SNZREQEN11	Snooze Request Enable 11	Enable IRQ11 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b13, 12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	SNZREQEN14	Snooze Request Enable 14	Enable IRQ14 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b15	SNZREQEN15	Snooze Request Enable 15	Enable IRQ15 pin snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b16	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b17	SNZREQEN17	Snooze Request Enable 17	Enable Key Interrupt snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b22 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b23	SNZREQEN23	Snooze Request Enable 23	Enable ACMPLP0 snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b24	SNZREQEN24	Snooze Request Enable 24	Enable RTC alarm snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b25	SNZREQEN25	Snooze Request Enable 25	Enable RTC period snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	SNZREQEN28	Snooze Request Enable 28	Enable AGT1 underflow snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b29	SNZREQEN29	Snooze Request Enable 29	Enable AGT1 compare match A snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b30	SNZREQEN30	Snooze Request Enable 30	Enable AGT1 compare match B snooze request: 0: Disable the snooze request 1: Enable the snooze request.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SNZREQCR register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPEN register, see section 14, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR register is 1. The setting of the WUPEN register always has a higher priority than the SNZREQCR register settings. For details, see section 11.8, Snooze Mode and section 14, Interrupt Controller Unit (ICU).

Bit	Symbol	位名称	Description	R/W
b7	SNZREQEN7	暂停请求启用7	启用IRQ7引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b8	—	Reserved	该位读取为0。写入值应为0。	R/W
b9	SNZREQEN9	贪睡请求启用9	启用IRQ9引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b10	—	Reserved	该位读取为0。写入值应为0。	R/W
b11	SNZREQEN11	暂停请求启用11	启用IRQ11引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b13, 12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	SNZREQEN14	暂停请求启用14	启用IRQ14引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b15	SNZREQEN15	暂停请求启用15	启用IRQ15引脚贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b16	—	Reserved	该位读取为0。写入值应为0。	R/W
b17	SNZREQEN17	暂停请求启用17	EnableKeyInterrupt贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b22 to b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b23	SNZREQEN23	暂停请求启用23	启用ACMPLP0贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b24	SNZREQEN24	贪睡请求启用24	启用RTC警报贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b25	SNZREQEN25	暂停请求启用25	启用RTC周期贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b27, b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	SNZREQEN28	贪睡请求启用28	启用AGT1下溢贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b29	SNZREQEN29	贪睡请求启用29	启用AGT1比较匹配贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b30	SNZREQEN30	暂停请求启用30	启用AGT1比较匹配B贪睡请求：0：禁用贪睡请求1：启用贪睡请求。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

SNZREQCR寄存器控制哪个触发器导致MCU从软件待机模式切换到贪睡模式。如果通过设置WUPEN寄存器选择触发作为取消软件待机模式的请求，请参见第14节，中断控制器单元(ICU)，当SNZREQCR寄存器的相关位为1时产生触发时，MCU进入正常模式.WUPEN寄存器的设置总是比SNZREQCR寄存器的设置具有更高的优先级。有关详细信息，请参阅第11.8节，贪睡模式和第14节，中断控制器单元(ICU)。

11.2.11 Flash Operation Control Register (FLSTOP)

Address(es): SYSTEM.FLSTOP 4001 E09Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FLSTPF	—	—	—	FLSTOP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FLSTOP	Selecting ON/OFF of the Flash Memory Operation	0: Code flash and data flash memory operates 1: Code flash and data flash memory stops.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	FLSTPF	Flash Memory Operation Status Flag	0: Transition completed 1: During transition (from the flash-stop-status to flash-operating-status or flash-operating-status to flash-stop-status).	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FLSTOP bit (Selecting ON/OFF of the Flash Memory Operation)

The FLSTOP bit enables or disables flash memory. The FLSTOP bit must be written in a program executing in the SRAM. To use an interrupt when the FLSTOP bit is 1, be sure to place the interrupt vector in the SRAM. Set this bit to 0 when Low voltage mode is not selected.

Note: When changing the value of the FLSTOP bit from 1 to 0 to start flash memory operation, ensure the FLSTPF flag is 0 and OSCSF.HOCOSF is 1 before restarting access to the flash memory. After that, instructions can be executed in the code flash memory.

Note: Writing to FLSTOP.FLSTOP is prohibited while HOCOCR.HCSTP and OSCSF.HOCOSF are 0 (HOCO is in stabilization wait counting).

FLSTPF flag (Flash Memory Operation Status Flag)

The FLSTPF flag indicates the status of the transition from the flash-stop-status to flash-operating-status or from the flash-operating-status to the flash-stop-status. When the transition completes, the flag is read as 0. When using flash memory again after stopping it once, make sure that the FLSTPF flag is 0 before proceeding.

11.2.12 Power Save Memory Control Register (PSMCR)

Address(es): SYSTEM.PSMCR 4001 E09Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PSMC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PSMC[1:0]	Power Save Memory Control	b1 b0 0 0: All SRAM are on in Software Standby mode 0 1: 48-KB SRAM (2000 0000h to 2000 BFFFh) is on in Software Standby mode 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PSMC[1:0] bits (Power Save Memory Control)

The SRAM retention area in Software Standby mode is selected with the PSMC[1:0] bits. Supply current can be reduced

11.2.11 闪存操作控制寄存器(FLSTOP)

Address(es): SYSTEM.FLSTOP 4001 E09Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FLSTPF	—	—	—	FLSTOP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FLSTOP	选择闪光灯的ONOFF内存操作	0：代码闪存和数据闪存运行1：代码闪存和数据闪存停止。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	FLSTPF	闪存操作状态标志	0：转换完成1：转换中（从flash-stop-status到flash操作状态或闪存操作状态到闪存停止状态）。	R
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FLSTOP位（选择闪存操作的ON/OFF）

FLSTOP位启用或禁用闪存。FLSTOP位必须写入在执行的程序中SRAM。要在FLSTOP位为1时使用中断，请务必将中断向量放入SRAM。当未选择低电压模式时，将此位设置为0。

Note: 将FLSTOP位的值从1更改为0以启动闪存操作时，请确保FLSTPF标志为0且OSCSF.HOCOSF为1，然后再重新开始对闪存的访问。之后，指令可以在代码闪存中执行。

Note: 当HOCOCR.HCSTP和OSCSF.HOCOSF为0（HOCO处于稳定等待计数中）时，禁止写入FLSTOP.FLSTOP。

FLSTPF标志（闪存操作状态标志）

FLSTPF标志指示从闪存停止状态到闪存操作状态或从闪存操作状态到闪存停止状态的转换状态。转换完成后，该标志被读取为0。在停止一次闪存后再次使用闪存时，请确保FLSTPF标志为0，然后再继续。

11.2.12 省电内存控制寄存器(PSMCR)

Address(es): SYSTEM.PSMCR 4001 E09Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PSMC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PSMC[1:0]	省电记忆控制	b1b000：所有SRAM在软件待机模式下打开01：48KBSRAM（2000 0000h到2000BFFFh）在软件待机模式下打开10：禁止设置11：禁止设置。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PSMC[1:0]位（省电存储器控制）

软件待机模式下的SRAM保留区由PSMC[1:0]位选择。可以降低电源电流

by setting these bits to 01b (48-KB SRAM in Software Standby mode). A WFI instruction must be executed after setting the PSMC register.

11.2.13 System Control OCD Control Register (SYOCDCR)

Address(es): SYSTEM.SYOCDCR 4001 E40Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGEN	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DBGEN	Debugger Enable bit	0: On-chip debugger is disabled 1: On-chip debugger is enabled. Set to 1 first in on-chip debug mode.	R/W

DBGEN bit (Debugger Enable bit)

The DBGEN bit enables the on-chip debug mode. This bit must be set to 1 first in the on-chip debugger mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

11.3 Reducing Power Consumption by Switching Clock Signals

When the SCKDIVCR.FCK[2:0], ICK[2:0], PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits are set, the clock frequency changes. The CPU, DMAC, DTC, flash, and SRAM use the operating clock specified by the ICK[2:0] bits.

Peripheral modules use the operating clock specified in the PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits.

The flash memory interface uses the operating clock specified in the FCK[2:0] bits.

For details, see section 9, Clock Generation Circuit.

11.4 Module-Stop Function

The module-stop function can be set for each on-chip peripheral module.

When the MSTPmi bit (m = A to D, i = 31 to 0) in MSTPCRA to MSTPCRD is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Clearing the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle. The internal states of the modules are retained in the module-stop state.

After a reset is canceled, all modules other than the DMAC, DTC, and SRAMs are placed in the module-stop state. Do not access the module while the corresponding MSTPmi bit is 1, otherwise the read/write data or the operation of the module is not guaranteed. Also, do not set 1 to the MSTPmi bit while the corresponding module is accessed.

11.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage, power consumption can be reduced in Normal mode, Sleep mode, and Snooze mode.

11.5.1 Setting Operating Power Control Mode

Make sure that the operating condition such as the voltage range and the frequency range is always within the specified

通过将这些位设置为01b（软件待机模式下的48-KBSRAM）。设置PSMC寄存器后必须执行WFI指令。

11.2.13 系统控制OCD控制寄存器(SYOCDCR)

Address(es): SYSTEM.SYOCDCR 4001 E40Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGEN	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	DBGEN	调试器使能位	0：禁用片上调试器1：启用片上调试器。在片上调试模式下首先设置为1。	R/W

DBGEN位（调试器启用位）

DBGEN位使能片上调试模式。在片上调试器模式下，该位必须首先设置为1。

[Setting condition]

- 连接调试器时向该位写入1。

[Clearing condition]

- 上电复位产生
- 将0写入该位。

11.3 通过切换时钟信号降低功耗

当SCKDIVCR.FCK[2:0]、ICK[2:0]、PCKA[2:0]、PCKB[2:0]、PCKC[2:0]和PCKD[2:0]位设置时，时钟频率发生变化。CPU、DMAC、DTC、闪存和SRAM使用由ICK[2:0]位指定的工作时钟。

外设模块使用PCKA[2:0]、PCKB[2:0]、PCKC[2:0]和PCKD[2:0]位中指定的工作时钟。

闪存接口使用FCK[2:0]位中指定的工作时钟。

有关详细信息，请参见第9节，时钟生成电路。

11.4 Module-Stop Function

可以为每个片上外围模块设置模块停止功能。

当MSTPCRA到MSTPCRD中的MSTPmi位（m=A到D，i=31到0）设置为1时，指定模块停止运行并进入模块停止状态，但CPU继续独立运行。将MSTPmi位清0可取消模块停止状态，允许模块在总线周期结束时恢复运行。模块的内部状态保持在模块停止状态。

取消复位后，除DMAC、DTC和SRAM之外的所有模块都置于模块停止状态。对应的MSTPmi位为1时请勿访问模块，否则无法保证读写数据或模块的操作。此外，在访问相应模块时不要将MSTPmi位设置为1。

11.5 降低运行功耗的功能

通过根据工作频率和工作电压选择合适的工作功耗控制模式，可以在正常模式、睡眠模式和贪睡模式下降低功耗。

11.5.1 设置工作电源控制模式

确保电压范围和频率范围等工作条件始终在规定范围内

range before and after switching the operating power control modes.

This section provides example procedures for switching operating power control modes.

Table 11.5 Available oscillators in each mode

Mode	Oscillator						
	PLL*1	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Middle-speed	Available	Available	Available	Available	Available	Available	Available
Low-voltage	N/A	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

Note 1. The VCC range for the PLL is 2.4 to 3.6 V.

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

Operation begins in High-speed mode.

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in High-speed mode.
2. Change the oscillator to what is used in Low-speed mode.
3. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.
4. Turn off the oscillator that is not required in Low-speed mode.
5. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
6. Set the OPCCR.OPCM bit to 11b (Low-speed mode).
7. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
8. Perform the following steps when the flash cache is cacheable in Low-speed mode:
   a. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
   b. Check that the FCACHEIV.FCACHEIV bit is 0.
   c. Enable the flash cache by setting the FCACHEE.FCACHEEN bit.

Operation is now in Low-speed mode.

Example 2: From High-speed mode to Subosc-speed mode

Operation begins in High-speed mode.

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in High-speed mode.
2. Switch the clock source to sub-clock oscillator. Turn off HOCO, MOCO, the main oscillator and PLL.
3. Confirm that all the clock sources other than the sub-clock oscillator are stopped.
4. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
5. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
6. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
7. Perform the following steps when the flash cache is cacheable in Subosc-speed mode.

切换操作功率控制模式之前和之后的范围。

本节提供切换操作电源控制模式的示例程序。

Table 11.5 每种模式下可用的振荡器

Mode	Oscillator						
	PLL*1	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	主时钟振荡器	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Middle-speed	Available	Available	Available	Available	Available	Available	Available
Low-voltage	N/A	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

Note 1. PLL的VCC范围是2.4到3.6V。

(1) 从高功率模式切换到低功率模式

示例1：从高速模式到低速模式：

操作以高速模式开始。

1. 当闪存缓存在高速模式下可缓存时，通过重置FCACHEE.FCACHEEN来禁用闪存缓存。
2. 将振荡器更改为低速模式下使用的振荡器。
3. 将每个时钟的频率设置为低于低速模式下的最大工作频率。
4. 关闭低速模式下不需要的振荡器。
5. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
6. 将OPCCR.OPCM位设置为11b（低速模式）。
7. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
8. 当闪存缓存在低速模式下可缓存时，请执行以下步骤：
   一个。通过设置FCACHEIV.FCACHEIV使闪存缓存无效。
   湾。检查FCACHEIV.FCACHEIV位是否为0。
   C。通过设置FCACHEE.FCACHEEN位启用闪存缓存。

操作现在处于低速模式。

示例2：从高速模式到Subosc速度模式

操作以高速模式开始。

1. 当闪存缓存在高速模式下可缓存时，通过重置FCACHEE.FCACHEEN来禁用闪存缓存。
2. 将时钟源切换到子时钟振荡器。关闭HOCO、MOCO、主振荡器和PLL。
3. 确认除副时钟振荡器之外的所有时钟源都已停止。
4. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
5. 将SOPCCR.SOPCM位设置为1（Subosc速度模式）。
6. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
7. 当闪存缓存在Subosc速度模式下可缓存时，请执行以下步骤。

a. Invalidate the flash cache by setting FCACHEIV.FCACHEIV bit.
b. Check that FCACHEIV.FCACHEIV bit is 0.
c. Enable the flash cache by setting FCACHEE.FCACHEEN bit.

Operation is now in Subosc-speed mode.

(2) Switching from a lower power mode to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

Operation begins in Subosc-speed mode.

1. Disable the flash cache by resetting the FCACHEE.FCACHEEN bit when the flash cache is cacheable in Subosc-speed mode.
2. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
3. Set SOPCCR.SOPCM bit to 0 (High-speed mode).
4. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
5. Turn on the oscillator needed in High-speed mode.
6. Set the frequency of each clock to lower than the maximum operating frequency for High-speed mode.
7. Perform the following steps when the flash cache is cacheable in High-speed mode:
   a. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
   b. Check that FCACHEIV.FCACHEIV is 0.
   c. Enable the flash cache by setting FCACHEE.FCACHEEN.

Operation is now in High-speed mode.

Example 2: From Low-speed mode to High-speed mode

Operation begins in Low-speed mode.

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in Low-speed mode.
2. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed).
3. Set the OPCCR.OPCM bit to 00b (High-speed mode).
4. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
5. Turn on any oscillator needed in High-speed mode.
6. Set the frequency of each clock to lower than the maximum operating frequency for High-speed mode.
7. Perform the following steps when the flash cache is cacheable in High-speed mode:
   a. Invalidate the flash cache by setting FCACHEIV.FCACHEIV bit.
   b. Check that FCACHEIV.FCACHEIV bit is 0.
   c. Enable the flash cache by setting FCACHEE.FCACHEEN bit.

Operation is now in High-speed mode.

11.5.2 Operating range

High-speed mode

The maximum operating frequency during flash read is 48 MHz for ICLK and 32 MHz for FCLK. The operating voltage range is 2.4 to 3.6 V during flash read. However, for ICLK and FCLK, the maximum operating frequency during flash read is 16 MHz when the operating voltage is 2.4 V or larger and smaller than 2.7 V.

During flash programming and erasure, the operating frequency range is 1 to 48 MHz and the operating voltage range is 2.7 to 3.6 V.

The PLL can be used when the operating voltage is 2.4 V or above.

一个。通过设置FCACHEIV.FCACHEIV位使闪存缓存无效。湾。检查FCACHEIV.FCACHEIV位是否为0。c．通过设置FCACHEE.FCACHEEN位启用闪存缓存。操作现在处于Subosc速度模式。

(2) 从低功耗模式切换到高功耗模式

示例1：从Subosc速度模式到高速模式

操作以Subosc速度模式开始。

1. 当闪存缓存在Subosc速度模式下可缓存时，通过重置FCACHEE.FCACHEEN位来禁用闪存缓存。
2. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
3. 将SOPCCR.SOPCM位设置为0（高速模式）。
4. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
5. 打开高速模式所需的振荡器。
6. 将每个时钟的频率设置为低于高速模式的最大工作频率。
7. 当Flash缓存在高速模式下可缓存时，请执行以下步骤：
   一个。通过设置FCACHEIV.FCACHEIV使闪存缓存无效。
   湾。检查FCACHEIV.FCACHEIV是否为0。
   C。通过设置FCACHEE.FCACHEEN启用闪存缓存。

操作现在处于高速模式。

示例2：从低速模式到高速模式

操作以低速模式开始。

1. 当闪存缓存在低速模式下可缓存时，通过重置FCACHEE.FCACHEEN来禁用闪存缓存。
2. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
3. 将OPCCR.OPCM位设置为00b（高速模式）。
4. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
5. 打开高速模式所需的任何振荡器。
6. 将每个时钟的频率设置为低于高速模式的最大工作频率。
7. 当Flash缓存在高速模式下可缓存时，请执行以下步骤：

一个。通过设置FCACHEIV.FCACHEIV位使闪存缓存无效。湾。检查FCACHEIV.FCACHEIV位是否为0。c．通过设置FCACHEE.FCACHEEN位启用闪存缓存。操作现在处于高速模式。

11.5.2 工作范围

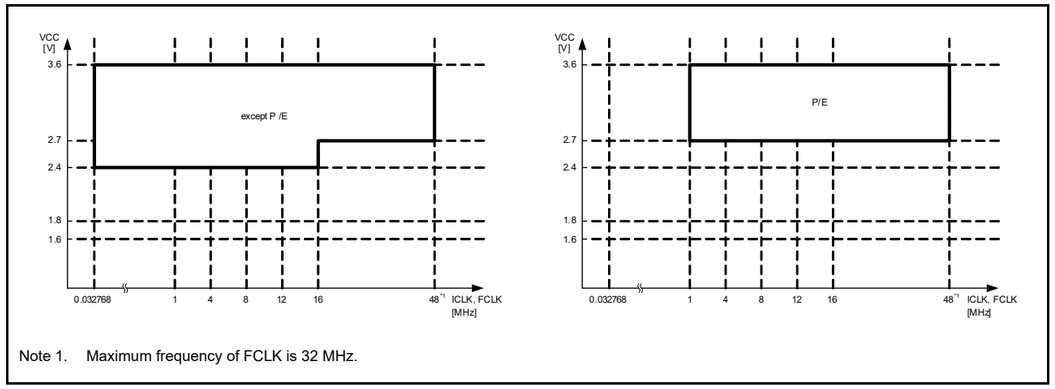
High-speed mode

闪存读取期间的最大工作频率对于ICLK为48MHz，对于FCLK为32MHz。闪存读取期间的工作电压范围为2.4至3.6V。但是，对于ICLK和FCLK，当工作电压为2.4V或更大且小于2.7V时，闪存读取期间的最大工作频率为16MHz。

在闪存编程和擦除期间，工作频率范围为1至48MHz，工作电压范围为2.7至3.6V。

当工作电压为2.4V或以上时，可以使用PLL。

Figure 11.2 shows the operating voltages and frequencies in High-speed mode.



Note 1. Maximum frequency of FCLK is 32 MHz.

Figure 11.2 Operating voltages and frequencies in High-speed mode

Middle-speed mode

The power consumption of this mode is lower than that of High-speed mode under the same conditions.

The maximum operating frequency during flash read is 12 MHz for ICLK and FCLK. The operating voltage range is 1.8 to 3.6 V during flash read. However, for ICLK and FCLK, the maximum operating frequency during flash read is 8 MHz when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

During flash programming and erasure, the operating frequency range is 1 to 12 MHz and the operating voltage range is 1.8 to 3.6 V. The maximum operating frequency during flash programming and erasure is 8 MHz when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

The PLL can be used when the operating voltage is 2.4 V or above.

Figure 11.3 shows the operating voltages and frequencies in Middle-speed mode.

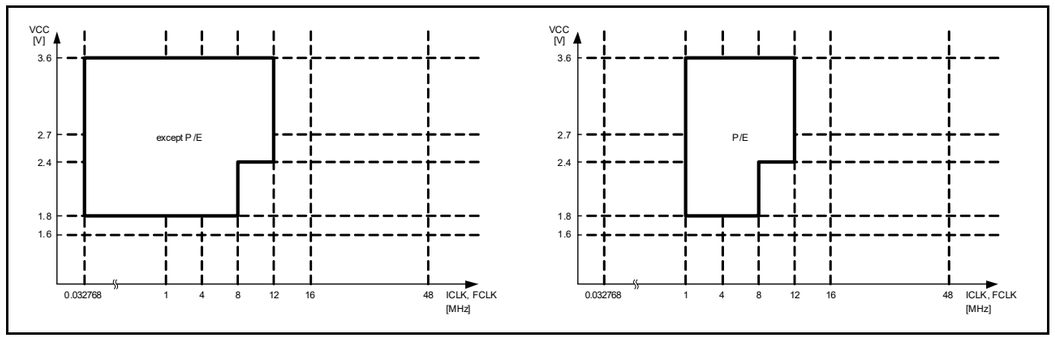


Figure 11.3 Operating voltages and frequencies in Middle-speed mode

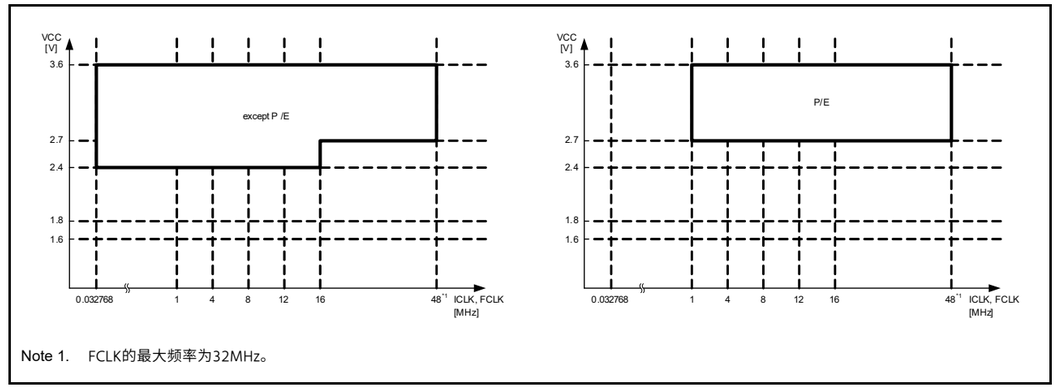
Low-voltage mode

After a reset is canceled, operation is started from this mode. Using the PLL is prohibited.

The maximum operating frequency during flash read is 4 MHz for ICLK and FCLK. The operating voltage range is 1.8 to 3.6 V during flash read.

During flash programming and erasure, the operating frequency range is 1 to 4 MHz and the operating voltage range is 1.8 to 3.6 V. Using the PLL is prohibited.

图11.2显示了高速模式下的工作电压和频率。



Note 1. FCLK的最大频率为32MHz。

Figure 11.2 高速模式下的工作电压和频率

Middle-speed mode

在相同条件下，该模式的功耗低于高速模式。

对于ICLK和FCLK，闪存读取期间的最大工作频率为12MHz。闪存读取期间的工作电压范围为1.8至3.6V。但是，对于ICLK和FCLK，当工作电压为1.8V或更大且小于2.4V时，闪存读取期间的最大工作频率为8MHz。

在闪存编程和擦除期间，工作频率范围为1至12MHz，工作电压范围为1.8至3.6V。闪存编程和擦除期间的最大工作频率为8MHz，当工作电压为1.8V或更大且小于2.4伏。

当工作电压为2.4V或以上时，可以使用PLL。

图11.3显示了中速模式下的工作电压和频率。

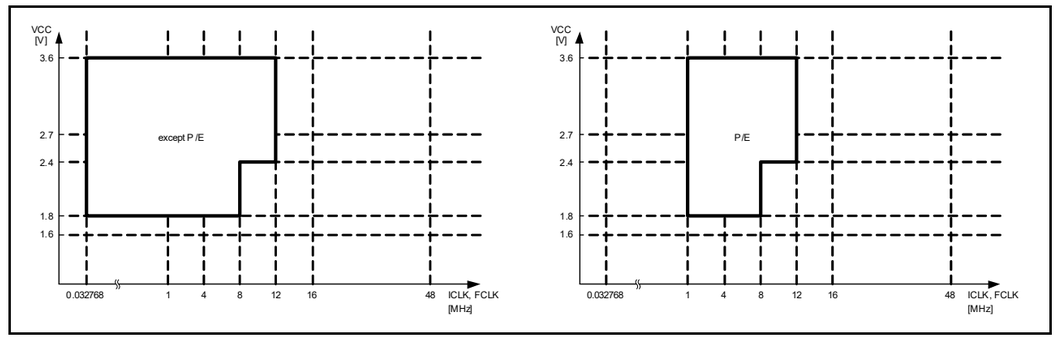


Figure 11.3 中速模式下的工作电压和频率

Low-voltage mode

取消复位后，从该模式开始运行。禁止使用PLL。

对于ICLK和FCLK，闪存读取期间的最大工作频率为4MHz。闪存读取期间的工作电压范围为1.8至3.6V。

在闪存编程和擦除期间，工作频率范围为1至4MHz，工作电压范围为1.8至3.6V。禁止使用PLL。

Figure 11.4 shows the operating voltages and frequencies in Low-voltage mode.

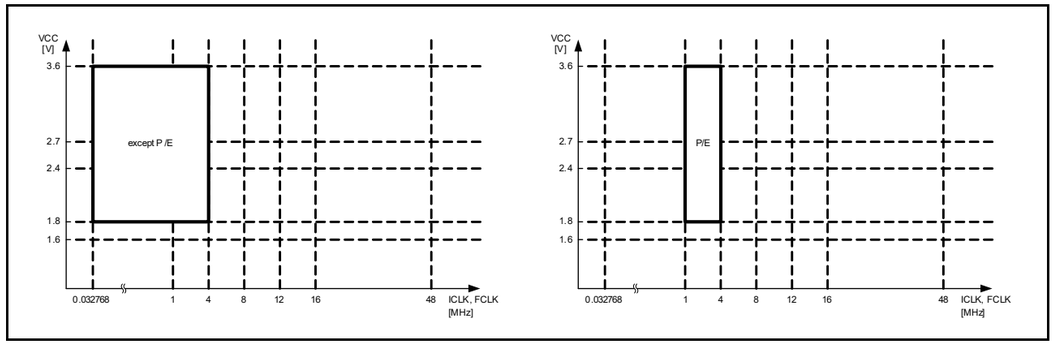


Figure 11.4 Operating voltages and frequencies in Low-voltage mode

Low-speed mode

The maximum operating frequency during flash read is 1 MHz for ICLK and FCLK. The operating voltage range is 1.8 to 3.6 V during flash read.

P/E operations for flash memory are prohibited. Using the PLL is prohibited.

Figure 11.5 shows the operating voltages and frequencies in Low-speed mode.

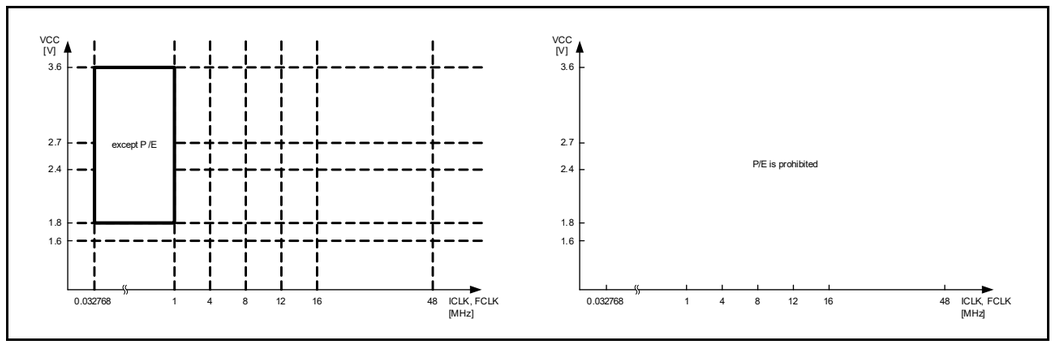


Figure 11.5 Operating voltages and frequencies in Low-speed mode

Subosc-speed mode

The maximum operating frequency during flash read is 37.6832 kHz for ICLK and FCLK. The operating voltage range is 1.8 to 3.6 V during flash read.

P/E operations for flash memory are prohibited. Using the oscillators other than the sub-clock oscillator or low-speed on-chip oscillator is prohibited.

图11.4显示了低电压模式下的工作电压和频率。

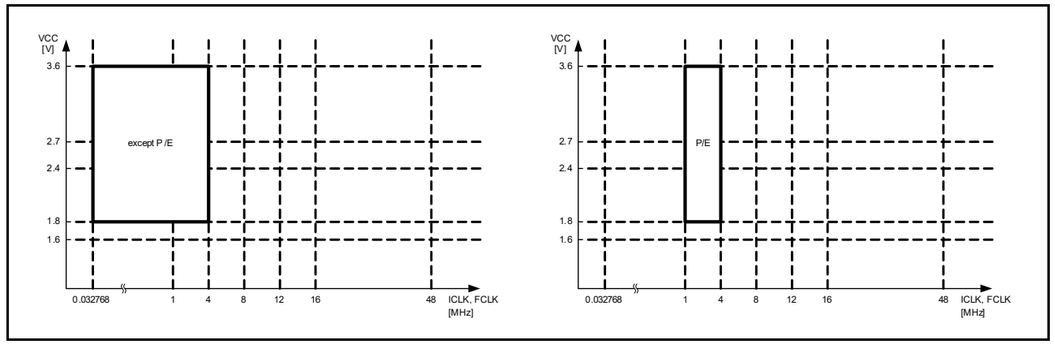


Figure 11.4 低压模式下的工作电压和频率

Low-speed mode

对于ICLK和FCLK，闪存读取期间的最大工作频率为1MHz。闪存读取期间的工作电压范围为1.8至3.6V。

禁止对闪存进行PE操作。禁止使用PLL。

图11.5显示了低速模式下的工作电压和频率。

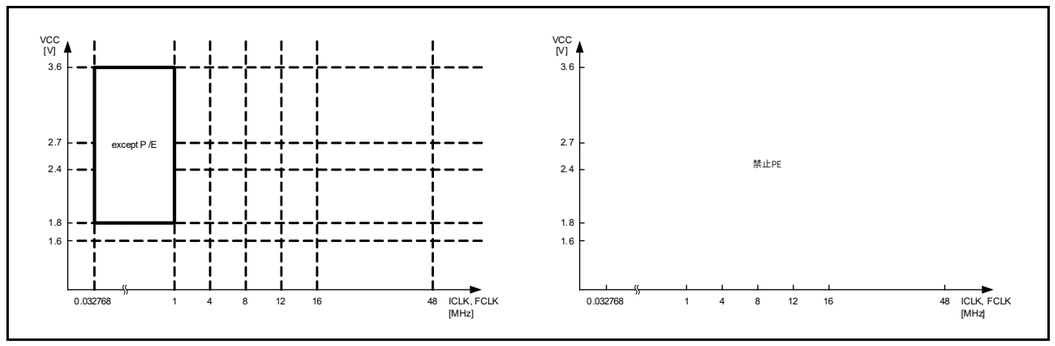


Figure 11.5 低速模式下的工作电压和频率

Subosc-speed mode

对于ICLK和FCLK，闪存读取期间的最大工作频率为37.6832kHz。闪存读取期间的工作电压范围为1.8至3.6V。

禁止对闪存进行PE操作。禁止使用副时钟振荡器或低速片上振荡器以外的振荡器。

Figure 11.6 shows the operating voltages and frequencies in Subosc-speed mode.

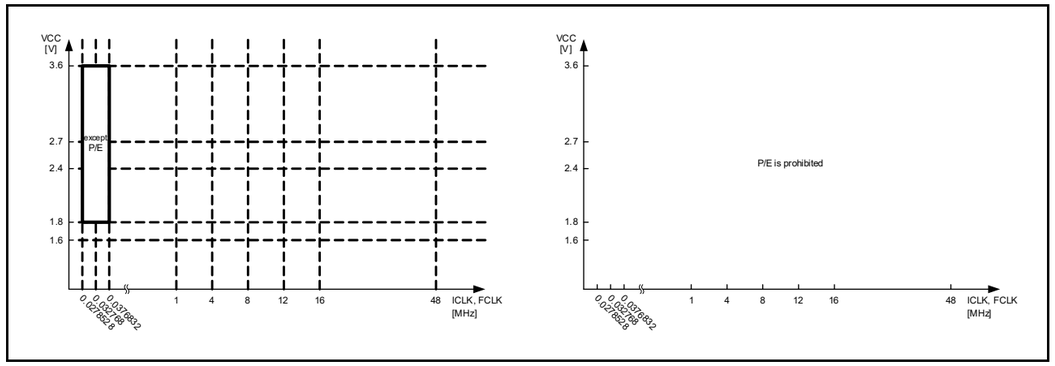


Figure 11.6 Operating voltages and frequencies in Subosc-speed mode

11.6 Sleep Mode

11.6.1 Transition to Sleep Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 14, Interrupt Controller Unit (ICU).

Counting by IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode or Snooze mode). Counting by IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode or Snooze mode).

Counting by WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit in is 1 (WDT stops in Sleep mode).

Counting by WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0. WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

11.6.2 Canceling Sleep Mode

Sleep mode is canceled by:

- An interrupt
- RES pin reset
- A power-on reset
- A voltage monitor reset
- An SRAM parity error reset
- An SRAM ECC error reset
- Bus master MPU error reset
- Bus slave MPU error reset
- A reset caused by an IWDT

图11.6显示了Subosc速度模式下的工作电压和频率。

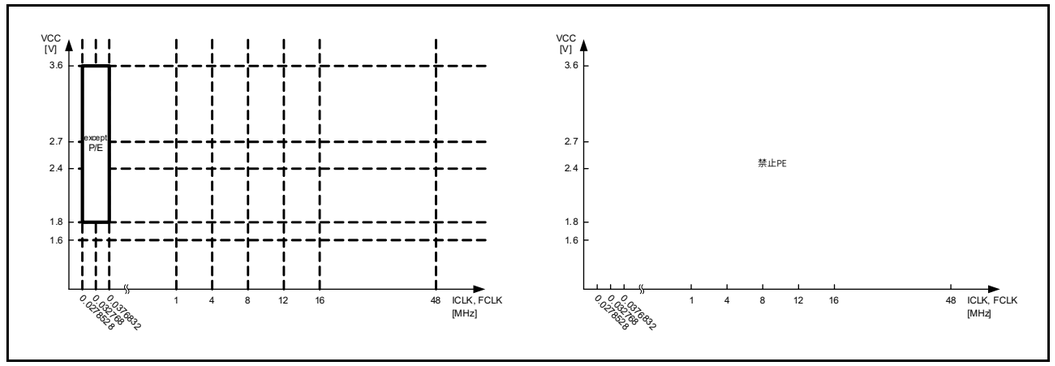


Figure 11.6 Subosc速度模式下的工作电压和频率

11.6 睡眠模式

11.6.1 过渡到睡眠模式

当SBYCR.SSBY位为0时执行WFI指令，MCU进入休眠模式。在这种模式下，CPU停止运行，但其内部寄存器的内容被保留。其他外围功能不会停止。休眠模式下可用的复位或中断会导致MCU取消休眠模式。所有中断源均可用。如果使用中断取消休眠模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

当MCU进入休眠模式且IWDT处于自动启动模式且OFS0.IWDTSTPCL位为1（IWDT在休眠模式、软件待机模式或贪睡模式下停止）。计数当IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为0时，当MCU进入休眠模式时，IWDT继续运行（IWDT在休眠模式、软件待机模式或贪睡模式下不会停止）。

当MCU进入休眠模式且WDT处于自动启动模式且OFS0.WDTSTPCTL位为1（WDT在休眠模式下停止）。同样，当WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为1（WDT在休眠模式下停止）时，当MCU进入休眠模式时，WDT停止计数。

当MCU进入休眠模式，而WDT处于自动启动模式和OFS0时，WDT继续计数。WDTSTPCTL位为0（WDT在休眠模式下不停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为0（休眠模式下WDT不会停止）时，WDT继续计数。

11.6.2 取消睡眠模式

睡眠模式通过以下方式取消：

- 中断
- RES引脚复位
- A power-on reset
- 电压监视器复位
- SRAM奇偶校验错误复位
- SRAMECC错误复位
- 总线主控MPU错误复位
- 总线从机MPU错误复位
- 由IWDT引起的复位

- A WDT underflow.

The operations are as follows:

1. Canceling by an interrupt
   When an available interrupt request is generated, Sleep mode is canceled and the MCU starts the interrupt handling.
2. Canceling by RES pin reset
   When RES pin is driven low, the MCU enters the reset state. Be sure to keep RES pin low for the time period specified in section 48, Electrical Characteristics. When RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   Sleep mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset
   Sleep mode is canceled by an internal reset generated by a WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
   - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
5. Canceling by other resets available in Sleep mode
   Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details of proper setting of the interrupts, see section 14, Interrupt Controller Unit (ICU).

11.7 Software Standby Mode

11.7.1 Transition to Software Standby Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 1, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions and oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O ports are retained. Software Standby mode allows a significant reduction in power consumption because most of the oscillators stop in this mode. Table 11.2 shows the status of each on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode cause the MCU to cancel Software Standby mode. See Table 11.3 for available interrupt sources and section 14.2.9, Wake Up Interrupt Enable Register (WUPEN) for information on how to wake up the MCU from Software Standby mode. If using an interrupt to cancel Software Standby mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 14, Interrupt Controller Unit (ICU).

Clear the DMAST.DMST bit and DTCST.DTCST bit to 0 before executing a WFI instruction, except when using the DTC in Snooze mode. If the DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by IWDT stops when the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode, or Snooze mode). Counting by IWDT continues if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode, or Snooze mode).

WDT stops counting when the MCU enters Software Standby mode.

Do not enter Software Standby mode while OSTDCR.OSTDE = 1 (oscillation stop detection function is enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0). If executing a WFI instruction while OSTDCR.OSTDE = 1, the MCU enters Sleep mode even when SBYCR.SSBY = 1. In addition, do not enter Software Standby mode while the flash memory performs a programming or erasing procedure. To enter Software Standby mode, execute a WFI instruction after the programming or erasing procedure completes.

- A WDT underflow.

操作如下：

1. 通过中断取消
   当产生可用的中断请求时，休眠模式被取消，MCU开始中断处理。
2. 通过RES引脚复位取消
   当RES引脚驱动为低电平时，MCU进入复位状态。请务必在第48节"电气特性"中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间段后被驱动为高电平时，CPU开始复位异常处理。
3. 通过IWDT复位取消
   休眠模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。但是，IWDT在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. 通过WDT复位取消
   睡眠模式由WDT下溢产生的内部复位取消，MCU启动复位异常处理。但是，即使在正常模式下计数，WDT也会在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：
   - OFS0.WDTSTRT=0（自动启动模式）和OFS0.WDTSTPCTL=1
   - OFS0.WDTSTRT=1（寄存器启动模式）和WDTCSTPR.SLCSTP=1。
5. 通过睡眠模式下可用的其他复位取消
   休眠模式被其他复位取消，MCU开始复位异常处理。

Note: 有关正确设置中断的详细信息，请参见第14节，中断控制器单元(ICU)。

11.7 软件待机模式

11.7.1 过渡到软件待机模式

当SBYCR.SSBY位为1时执行WFI指令时，MCU进入软件待机模式。在这种模式下，CPU、大部分片上外围功能和振荡器停止。但是，CPU内部寄存器和SRAM数据的内容、片上外围功能的状态和IO端口的状态会被保留。软件待机模式可显着降低功耗，因为大多数振荡器在此模式下停止。表11.2显示了每个片上外围功能和振荡器的状态。软件待机模式下可用的复位或中断会导致MCU取消软件待机模式。有关可用的中断源，请参见表11.3，有关如何将MCU从软件待机模式唤醒的信息，请参见第14.2.9节，唤醒中断使能寄存器(WUPEN)。如果使用中断取消软件待机模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

在执行WFI指令之前，将DMAST.DMST位和DTCST.DTCST位清零，除非使用
DTC处于贪睡模式。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

当MCU进入软件待机模式而IWDT处于自动启动模式并且
OFS0.IWDTSTPCTL位为1（IWDT在休眠模式、软件待机模式或贪睡模式下停止）。计数
如果在IWDT处于自动启动模式且MCU进入软件待机模式时，IWDT将继续
OFS0.IWDTSTPCTL位为0（IWDT在休眠模式、软件待机模式或贪睡模式下不会停止）。

当MCU进入软件待机模式时，WDT停止计数。

OSTDCR.OSTDE=1时不要进入软件待机模式（振荡停止检测功能启用）。要进入软件待机模式，请在禁用振荡停止检测功能(OSTDCR.OSTDE=0)后执行WFI指令。如果在OSTDCR.OSTDE=1时执行WFI指令，即使SBYCR.SSBY=1，MCU也会进入休眠模式。此外，在闪存执行编程或擦除过程时不要进入软件待机模式。要进入软件待机模式，请在编程或擦除过程完成后执行WFI指令。

11.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 11.3
- RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby mode, the oscillators that operate before the transition to the mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 14.2.9, Wake Up Interrupt Enable Register (WUPEN) for information on waking up the MCU from Software Standby mode.

You can cancel Software Standby mode from any of the following ways:

1. Canceling by an interrupt
   When an available interrupt request (for available interrupts, see Table 11.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode and starts the interrupt handling.
2. Canceling by a RES pin reset
   When RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 48, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by a power-on reset
   Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.
4. Canceling by a voltage monitor reset
   Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
5. Canceling by IWDT reset
   Software Standby mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

11.7.3 Example of Software Standby Mode Application

Figure 11.7 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode by a rising edge of the IRQn pin.

In this example, an IRQn pin interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 01b (falling edge) in Normal mode, and the IRQCRi.IRQMD[1:0] bits set to 10b (rising edge). Follow that, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 14, Interrupt Controller Unit (ICU).

11.7.2 取消软件待机模式

软件待机模式通过以下方式取消：

- 表11.3中显示的可用中断
- RES引脚复位
- A power-on reset
- 电压监视器复位
- 由IWDT下溢引起的复位。

在退出软件待机模式时，在转换到模式之前工作的振荡器会重新启动。在所有振荡器稳定后，MCU从软件待机模式返回到正常模式。有关将MCU从软件待机模式唤醒的信息，请参见第14.2.9节，唤醒中断使能寄存器(WUPEN)。

您可以通过以下任一方式取消软件待机模式：

1. 通过中断取消
   当产生可用中断请求（可用中断请参见表11.3）时，在转换到软件待机模式之前工作的振荡器将重新启动。在所有振荡器稳定后，MCU从软件待机模式返回正常模式并开始中断处理。
2. 通过RES引脚复位取消
   当RES引脚驱动为低电平时，MCU进入复位状态，默认状态为工作的振荡器开始振荡。请务必在第48节"电气特性"中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。
3. 通过上电复位取消
   软件待机模式通过上电复位取消，MCU启动复位异常处理。
4. 通过电压监视器复位取消
   软件待机模式通过电压检测电路的电压监视器复位取消，MCU开始复位异常处理。
5. 通过IWDT复位取消
   软件待机模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。但是，IWDT在软件待机模式下停止，并且在以下情况下不会产生用于取消软件待机模式的内部复位：
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

11.7.3 软件待机模式应用示例

图11.7显示了在检测到IRQn引脚的下降沿进入软件待机模式并在IRQn引脚的上升沿退出软件待机模式的示例。

在本例中，IRQn引脚中断被接受，ICU的IRQCRi.IRQMD[1:0]位在正常模式下设置为01b（下降沿），IRQCRi.IRQMD[1:0]位设置为10b（上升沿）。随后，SBYCR.SSBY位设置为1并执行WFI指令。因此，软件待机模式的进入完成，软件待机模式的退出由IRQn引脚的上升沿启动。

退出软件待机模式也需要设置ICU。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

The oscillation stabilization time in Figure 11.7 is specified in section 48, Electrical Characteristics.

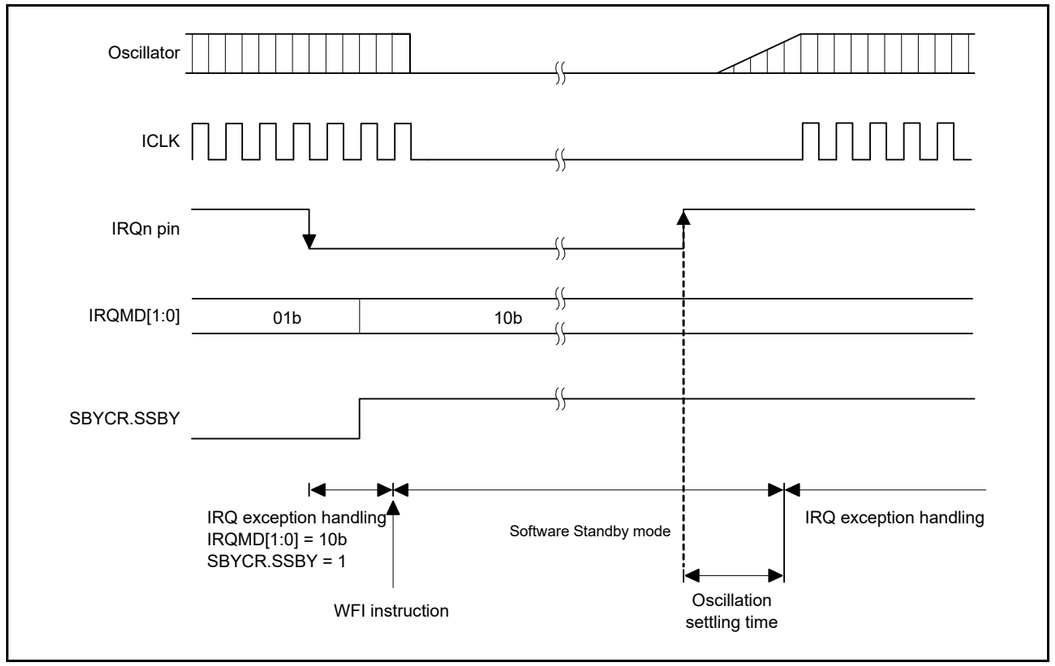


Figure 11.7 Example of Software Standby mode application

图11.7中的振荡稳定时间在第48节"电气特性"中指定。

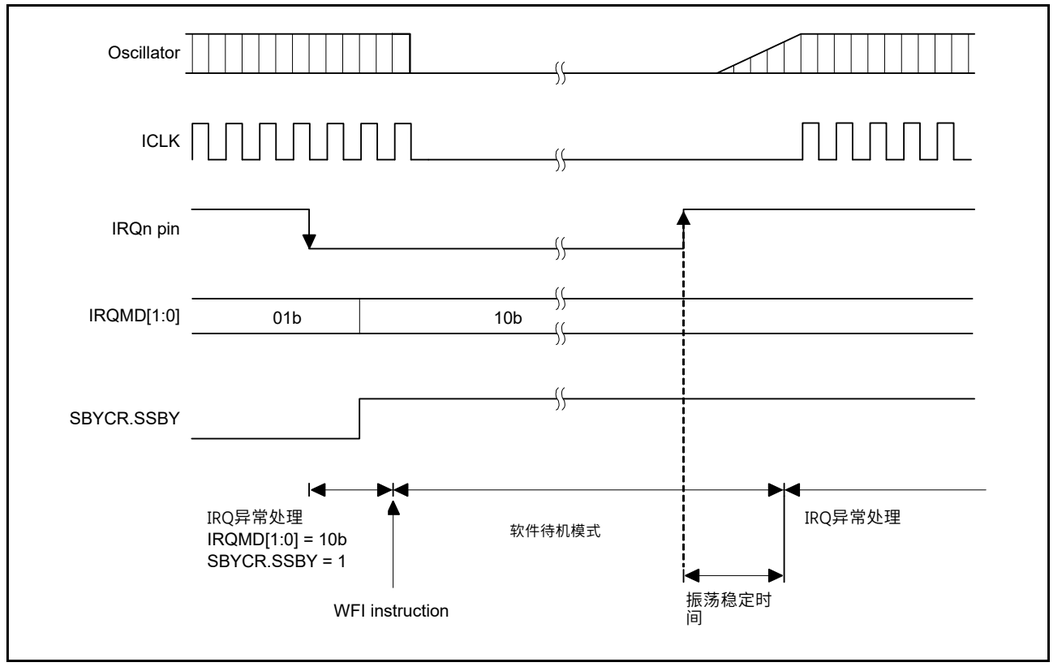


Figure 11.7 软件待机模式应用示例

11.8 Snooze Mode

11.8.1 Transition to Snooze Mode

Figure 11.8 shows snooze mode entry configuration. When the snooze control circuit receives a Snooze request in Software Standby mode, the MCU transitions to Snooze mode. In this mode, some peripheral modules operate without waking up the CPU. The peripheral modules that can operate in Snooze mode are shown in Table 11.2, Operating conditions of each low power mode. DTC operation in Snooze mode can also be selected by setting the SNZCR.SNZDTCEN bit.

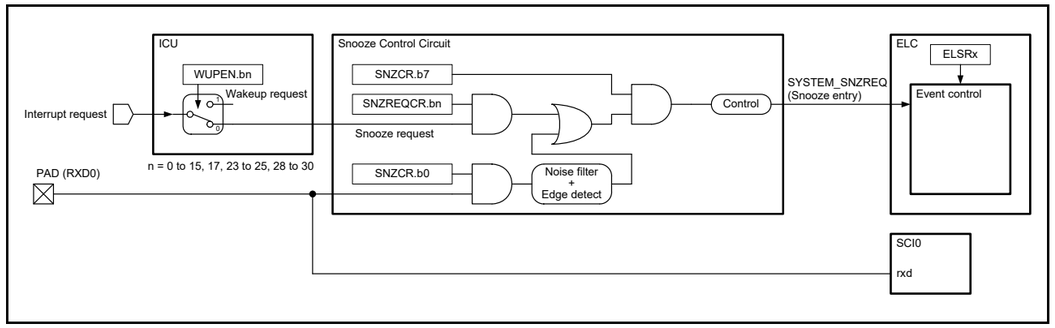


Figure 11.8 Snooze mode entry configuration

Table 11.6 shows the snooze requests to switch the MCU from Software Standby mode to Snooze mode. To use the listed snooze requests as a trigger to switch to Snooze mode, the associated SNZREQENn bit of the SNZREQCR register or RXDREQEN bit of the SNZCR register must be set before entering Software Standby mode. Do not enable multiple snooze requests at the same time.

Table 11.6 Available snooze requests to switch to Snooze mode

	Control Register	
Snooze request	**Register**	**Bit**
PORT_IRQn (n = 0 to 4, 6, 7, 9, 11, 14, 15)	SNZREQCR	SNZREQENn (n = 0 to 15)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_LP0	SNZREQCR	SNZREQEN23
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN*1

Note 1. RXDREQEN bit must not be set to 1 except in asynchronous mode.

11.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or a reset. Table 11.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests that is selected by SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected in IELSRn (n = 0 to 31) to link to the NVIC for the corresponding interrupt handling. See section 14, Interrupt Controller Unit (ICU) for the setting of SELSR0 and IELSRn registers.

11.8 贪睡模式

11.8.1 过渡到贪睡模式

图11.8显示了贪睡模式进入配置。当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转换到贪睡模式。在这种模式下，一些外围模块在不唤醒CPU的情况下运行。可以在贪睡模式下运行的外围模块如表11.2，每种低功耗模式的运行条件中所示。还可以通过设置SNZCR.SNZDTCEN位来选择贪睡模式下的DTC操作。

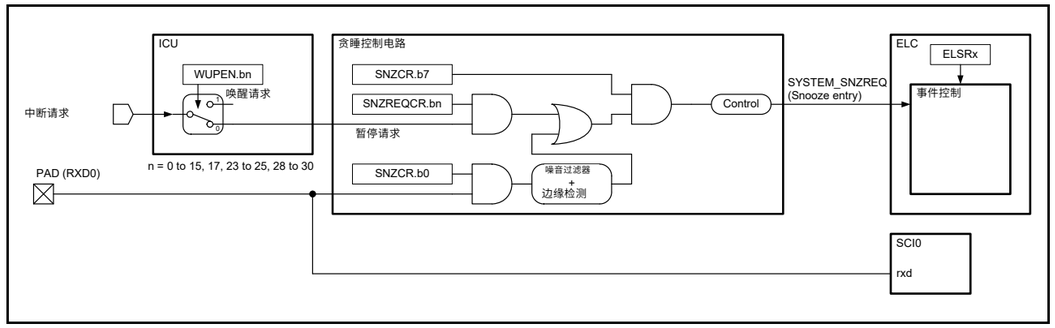


Figure 11.8 贪睡模式进入配置

表11.6显示了将MCU从软件待机模式切换到贪睡模式的贪睡请求。要将列出的贪睡请求用作切换到贪睡模式的触发器，必须在进入软件待机模式之前设置SNZREQCR寄存器的相关SNZREQENn位或SNZCR寄存器的RXDREQEN位。不要同时启用多个贪睡请求。

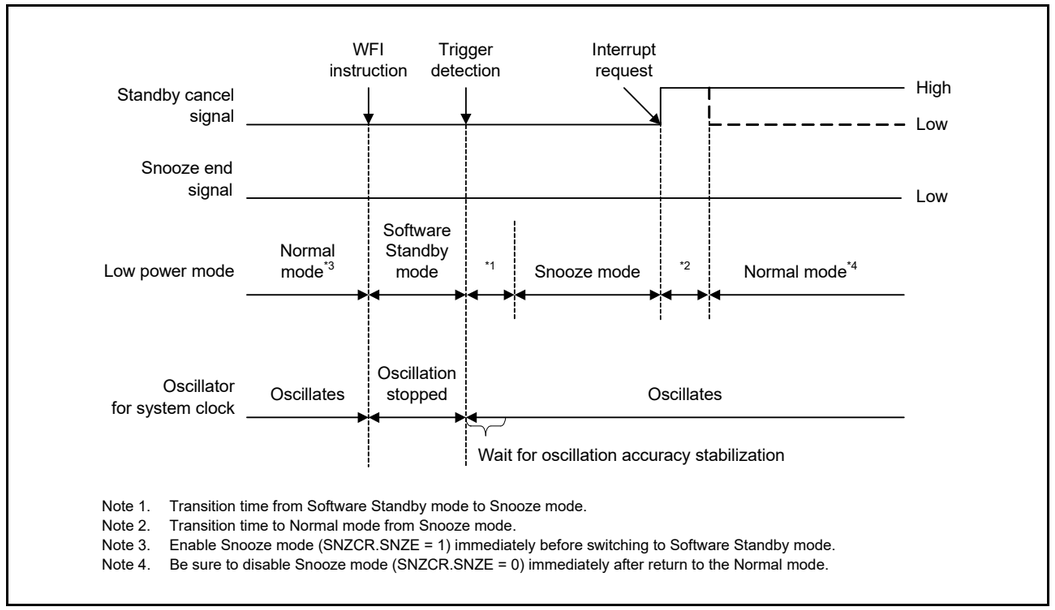
Table 11.6 可用的贪睡请求以切换到贪睡模式

	控制寄存器	
暂停请求	**Register**	**Bit**
PORT_IRQn (n = 0 to 4, 6, 7, 9, 11, 14, 15)	SNZREQCR	SNZREQENn (n = 0 to 15)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_LP0	SNZREQCR	SNZREQEN23
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0下降沿	SNZCR	RXDREQEN*1

Note 1. 除异步模式外，RXDREQEN位不得设置为1。

11.8.2 取消贪睡模式

贪睡模式由软件待机模式下可用的中断请求或复位取消。表11.3显示了可用于退出每种模式的请求。取消贪睡模式后，MCU进入正常模式并继续对给定中断或复位进行异常处理。由SELSR0选择的中断请求触发的动作取消贪睡模式。必须在IELSRn（n=0到31）中选择中断取消贪睡模式以链接到NVIC以进行相应的中断处理。有关SELSR0和IELSRn寄存器的设置，请参见第14节，中断控制器单元(ICU)。



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time to Normal mode from Snooze mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.
Note 4. Be sure to disable Snooze mode (SNZCR.SNZE = 0) immediately after return to the Normal mode.

Figure 11.9 When interrupt request signal is generated in Snooze mode

11.8.3 Return to Software Standby Mode

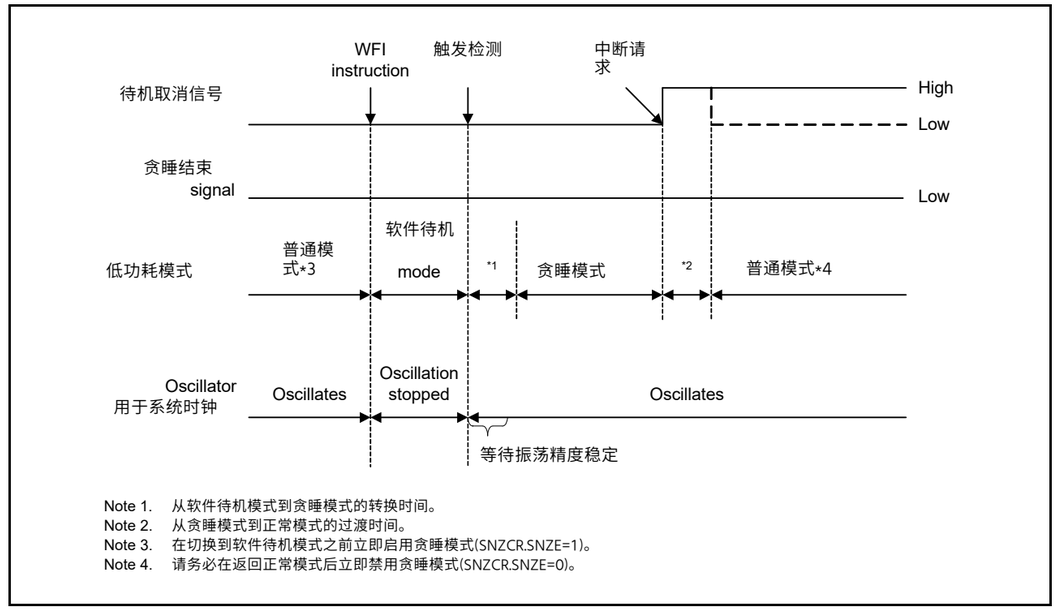
Table 11.7 shows the snooze end request that can be used as a trigger to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 11.8 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The CTSU, SCI0, ADC140, and DTC can keep the MCU in Snooze mode until they complete operation. However, an AGT1 underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 11.10 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to the snooze end requests set in the SNZEDCR register. A snooze request is cleared automatically after the transition to Software Standby mode.

Table 11.7 Available snooze end requests (triggers for transition to Software Standby mode)

	Enable/disable control	
Snooze end request	**Register**	**Bit**
AGT1 underflow or measurement complete (AGT1_AGTI)	SNZEDCR	b0
DTC transfer completion (DTC_COMPLETE)	SNZEDCR	b1
Not DTC transfer completion (DTC_TRANSFER)	SNZEDCR	b2
ADC140 window A/B compare match (ADC140_WCMPM)	SNZEDCR	b3
ADC140 window A/B compare mismatch (ADC140_WCMPUM)	SNZEDCR	b4
SCI0 address mismatch (SCI0_DCUF)	SNZEDCR	b7



Note 1. 从软件待机模式到贪睡模式的转换时间。
Note 2. 从贪睡模式到正常模式的过渡时间。
Note 3. 在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。
Note 4. 请务必在返回正常模式后立即禁用贪睡模式(SNZCR.SNZE=0)。

Figure 11.9 在贪睡模式下产生中断请求信号时

11.8.3 返回软件待机模式

表11.7显示了可用作返回软件待机模式的触发器的贪睡结束请求。贪睡结束请求仅在贪睡模式下可用。如果请求是在MCU未处于贪睡模式时生成的，则它们将被忽略。选择多个请求时，每个请求都会从贪睡模式转移到软件待机模式。

表11.8显示了贪睡结束条件，包括贪睡结束请求和外围模块的条件。CTSU、SCI0、ADC140和DTC可以将MCU保持在贪睡模式，直到它们完成操作。但是，AGT1下溢作为返回到软件待机模式的触发器会取消贪睡模式，而无需等待SCI0操作完成。

图11.10显示了从贪睡模式转换到软件待机模式的时序图。该模式转换根据SNZEDCR寄存器中设置的贪睡结束请求发生。过渡到软件待机模式后，贪睡请求会自动清除。

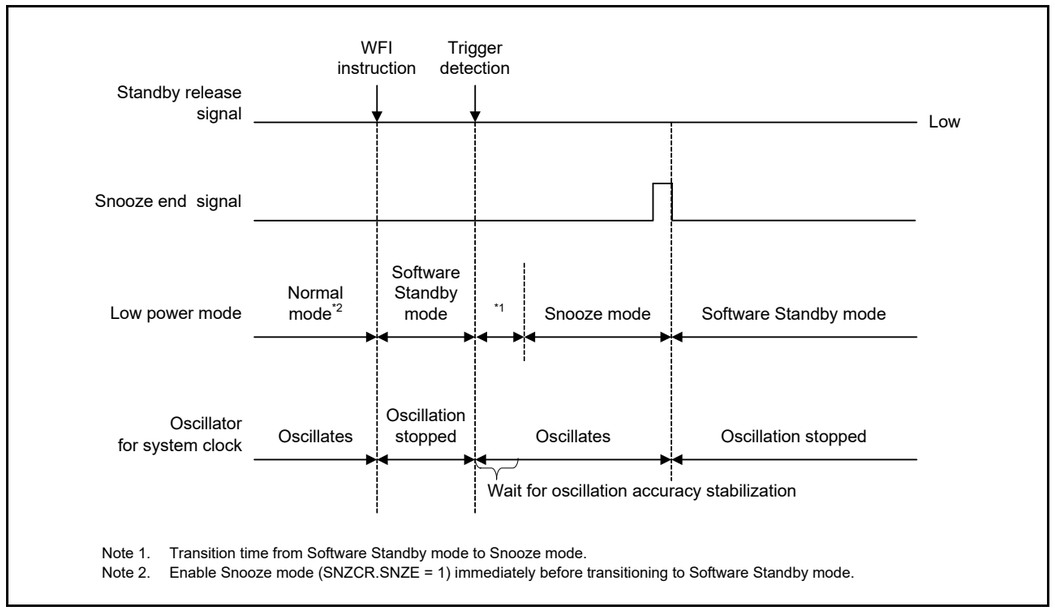
Table 11.7 可用的暂停结束请求（用于转换到软件待机模式的触发器）

	Enable/disable control	
暂停结束请求	**Register**	**Bit**
AGT1下溢或测量完成(AGT1_AGTI)	SNZEDCR	b0
DTC传输完成(DTC_COMPLETE)	SNZEDCR	b1
不是DTC传输完成(DTC_TRANSFER)	SNZEDCR	b2
ADC140窗口AB比较匹配(ADC140_WCMPM)	SNZEDCR	b3
ADC140窗口AB比较不匹配(ADC140_WCMPUM)	SNZEDCR	b4
SCI0地址不匹配(SCI0_DCUF)	SNZEDCR	b7

Table 11.8 Snooze end conditions

Operating module when a snooze end request occurs	Snooze end request	
	AGT1 underflow	Other than AGT1 underflow
DTC	The MCU transitions to Software Standby mode after all of the modules listed to the left of this column complete operation	The MCU transitions to Software Standby mode after all of the modules complete operation
ADC140		
CTSU		
SCI0	The MCU transitions to Software Standby mode immediately after a snooze end request is generated	
Other than above	The MCU transitions to Software Standby mode immediately after a snooze end request is generated	

Note: If the DTC is used to activate the ADC140, CTSU, or SCI, the MCU transitions to Software Standby mode after a snooze end request is generated.



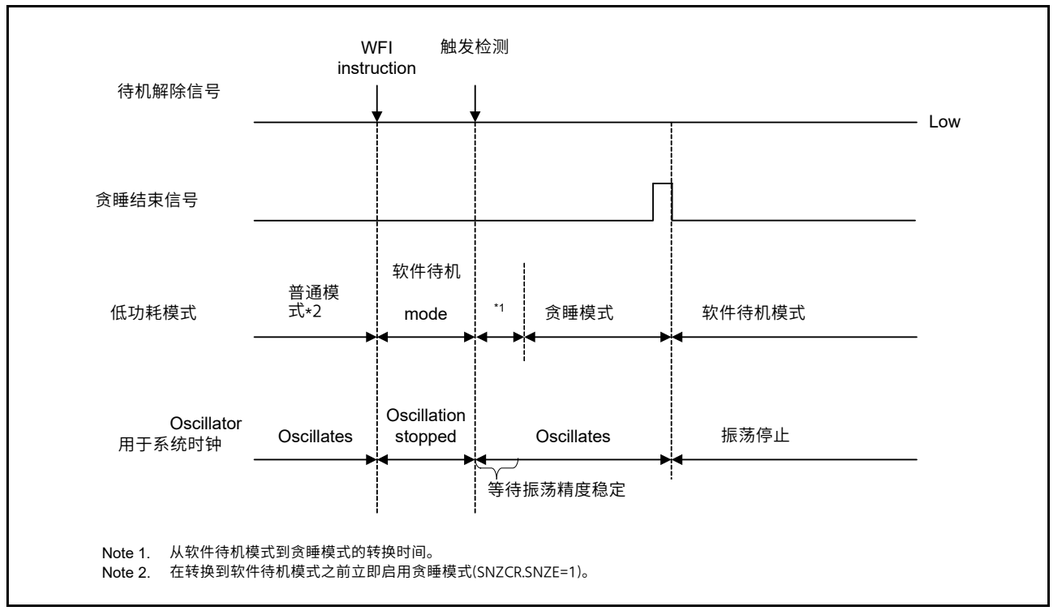
Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before transitioning to Software Standby mode.

Figure 11.10 When interrupt request signal is not generated in Snooze mode

Table 11.8 暂停结束条件

发生贪睡结束请求时的操作模块	暂停结束请求	
	AGT1 underflow	除了AGT1下溢
DTC	在此列左侧列出的所有模块完成操作后，MCU转换到软件待机模式	在所有模块完成操作后，MCU转换到软件待机模式
ADC140		
CTSU		
SCI0	产生贪睡结束请求后，MCU立即转换到软件待机模式	
上述以外	产生贪睡结束请求后，MCU立即转换到软件待机模式	

Note: 如果DTC用于激活ADC140、CTSU或SCI，则MCU在产生贪睡结束请求后转换到软件待机模式。



Note 1. 从软件待机模式到贪睡模式的转换时间。
Note 2. 在转换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。

Figure 11.10 在贪睡模式下不产生中断请求信号时

11.8.4 Snooze Operation Example

Figure 11.11 shows an example setting for using ELC in Snooze mode.

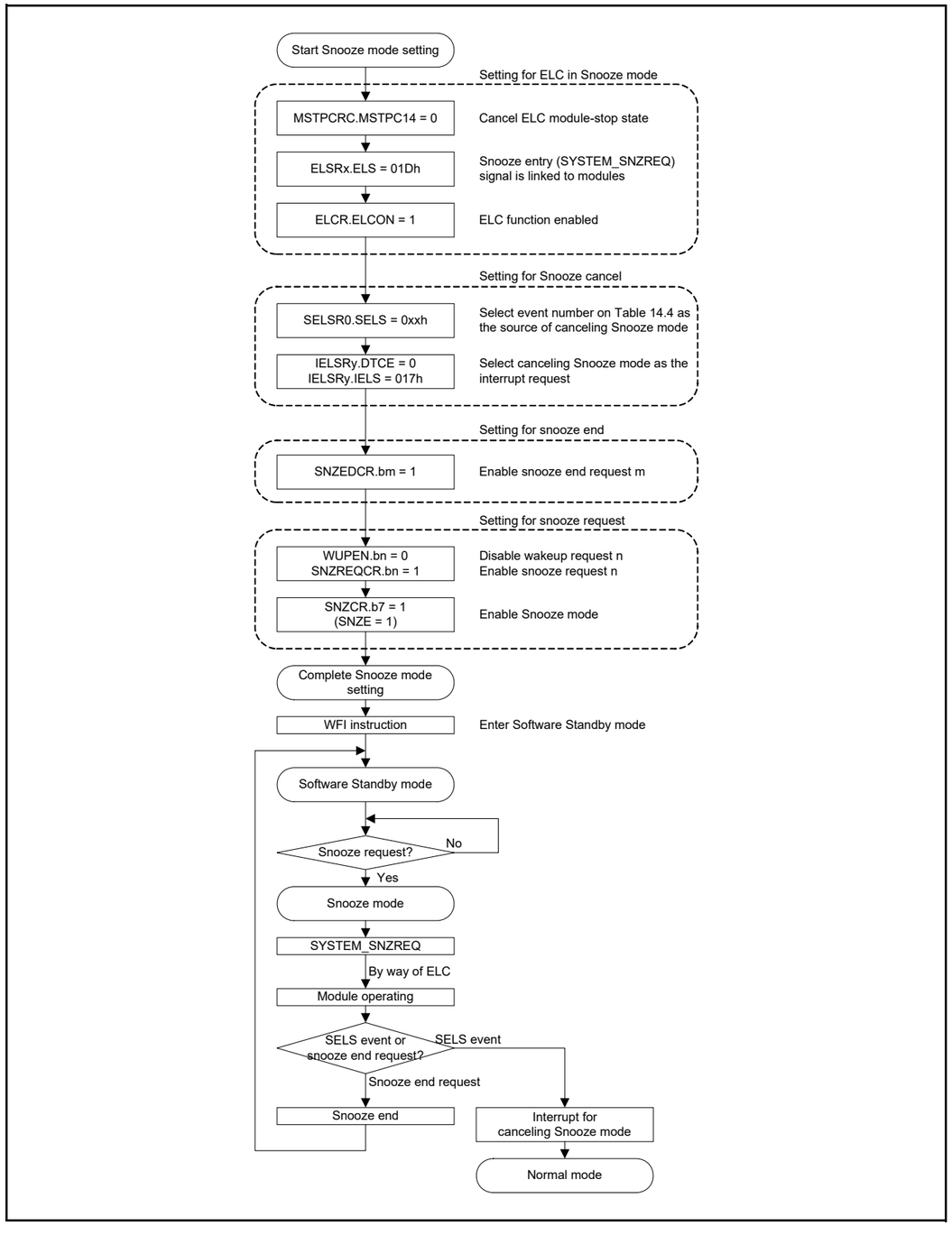


Figure 11.11 Setting example of using ELC in Snooze mode

11.8.4 贪睡操作示例

图11.11显示了在贪睡模式下使用ELC的示例设置。

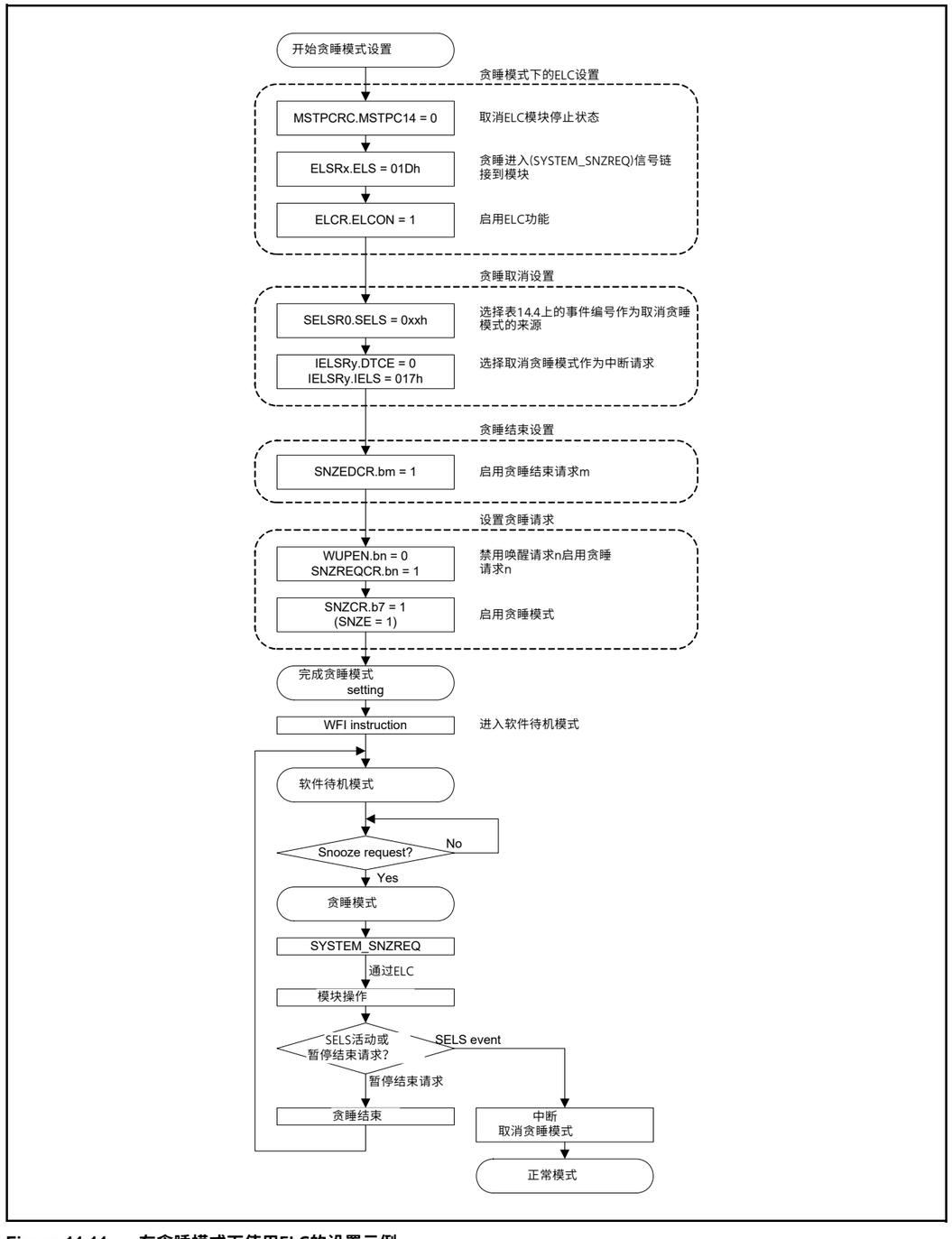


Figure 11.11 在贪睡模式下使用ELC的设置示例

The MCU is capable of data transmission/reception in SCI0 asynchronous mode without CPU intervention. Table 11.9 and Table 11.10 show the maximum transfer rate of the SCI0 in Snooze mode. When using the SCI0 in Snooze mode, use one of the following operating modes:

- High-speed mode
- Middle-speed mode
- Low-speed mode.

Do not use Low-voltage mode or Subosc-speed mode.

Table 11.9 and Table 11.10 show the maximum transfer rate of SCI0 in Snooze mode. When SCI0 is used in the Snooze mode, set the bits BGDM to 0, ABCS to 0, and ABCSE to 0. See section 29, Serial Communications Interface (SCI) for details.

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.9 HOCO: ± 1.0% (Ta = -20 to 85°C) **(Unit: bps)**

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and TRCLK	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	9600*1	-	-	-
2	9600*2	9600*4	4800	-
4	9600*3	9600*5	4800	2400
8	4800	4800	4800	2400
16	4800	4800	4800	2400
32	2400	2400	2400	2400
64	2400	2400	2400	2400

Note 1. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 3Dh, SCI0.MDDR = CEh must be used for 9600 bps.
Note 2. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 1Eh, SCI0.MDDR = CEh must be used for 9600 bps.
Note 3. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0Dh, SCI0.MDDR = BAh must be used for 9600 bps.
Note 4. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 32h, SCI0.MDDR = FEh must be used for 9600 bps.
Note 5. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 18h, SCI0.MDDR = F9h must be used for 9600 bps.

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.10 HOCO: ± 2.0% (Ta = -40 to -20°C) **(Unit: bps)**

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and TRCLK	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	2400	-	-	-
2	2400	2400	2400	-
4	2400	2400	2400	1200
8	2400	2400	2400	1200
16	2400	2400	2400	1200
32	1200	1200	1200	1200
64	1200	1200	1200	1200

MCU能够在SCI0异步模式下进行数据传输接收，无需CPU干预。表11.9和表11.10显示了SCI0在贪睡模式下的最大传输速率。在贪睡模式下使用SCI0时，请使用以下操作模式之一：

- High-speed mode
- Middle-speed mode
- Low-speed mode.

不要使用低电压模式或Subosc速度模式。

表11.9和表11.10显示了Snooze模式下SCI0的最大传输速率。当SCI0用于贪睡模式时，将位BGDM设置为0，ABCS设置为0，ABCSE设置为0。有关详细信息，请参见第29节，串行通信接口(SCI)。

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.9 HOCO: ± 1.0% (Ta = -20 to 85°C) **(Unit: bps)**

ICLK、PCLKA、PCLKB、PCLKC、PCLKD的最大分频比，FCLK, and TRCLK	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	9600*1	-	-	-
2	9600*2	9600*4	4800	-
4	9600*3	9600*5	4800	2400
8	4800	4800	4800	2400
16	4800	4800	4800	2400
32	2400	2400	2400	2400
64	2400	2400	2400	2400

Note 1. SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=3Dh，SCI0.MDDR=CEh必须用于9600bps。
Note 2. SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=1Eh，SCI0.MDDR=CEh必须用于9600bps。
Note 3. SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0Dh，SCI0.MDDR=BAh必须用于9600bps。
Note 4. SCI0.SMR.CKS[1:0]=00b SCI0.SEMR.BRME=1 SCI0.BRR=32h SCI0.MDDR=FEh必须用于9600bps。
Note 5. SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=18h，SCI0.MDDR=F9h必须用于9600bps。

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.10 HOCO: ± 2.0% (Ta = -40 to -20°C) **(Unit: bps)**

ICLK、PCLKA、PCLKB、PCLKC、PCLKD的最大分频比，FCLK, and TRCLK	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	2400	-	-	-
2	2400	2400	2400	-
4	2400	2400	2400	1200
8	2400	2400	2400	1200
16	2400	2400	2400	1200
32	1200	1200	1200	1200
64	1200	1200	1200	1200

Figure 11.12 shows an example setting for using the SCI0 in Snooze mode entry.

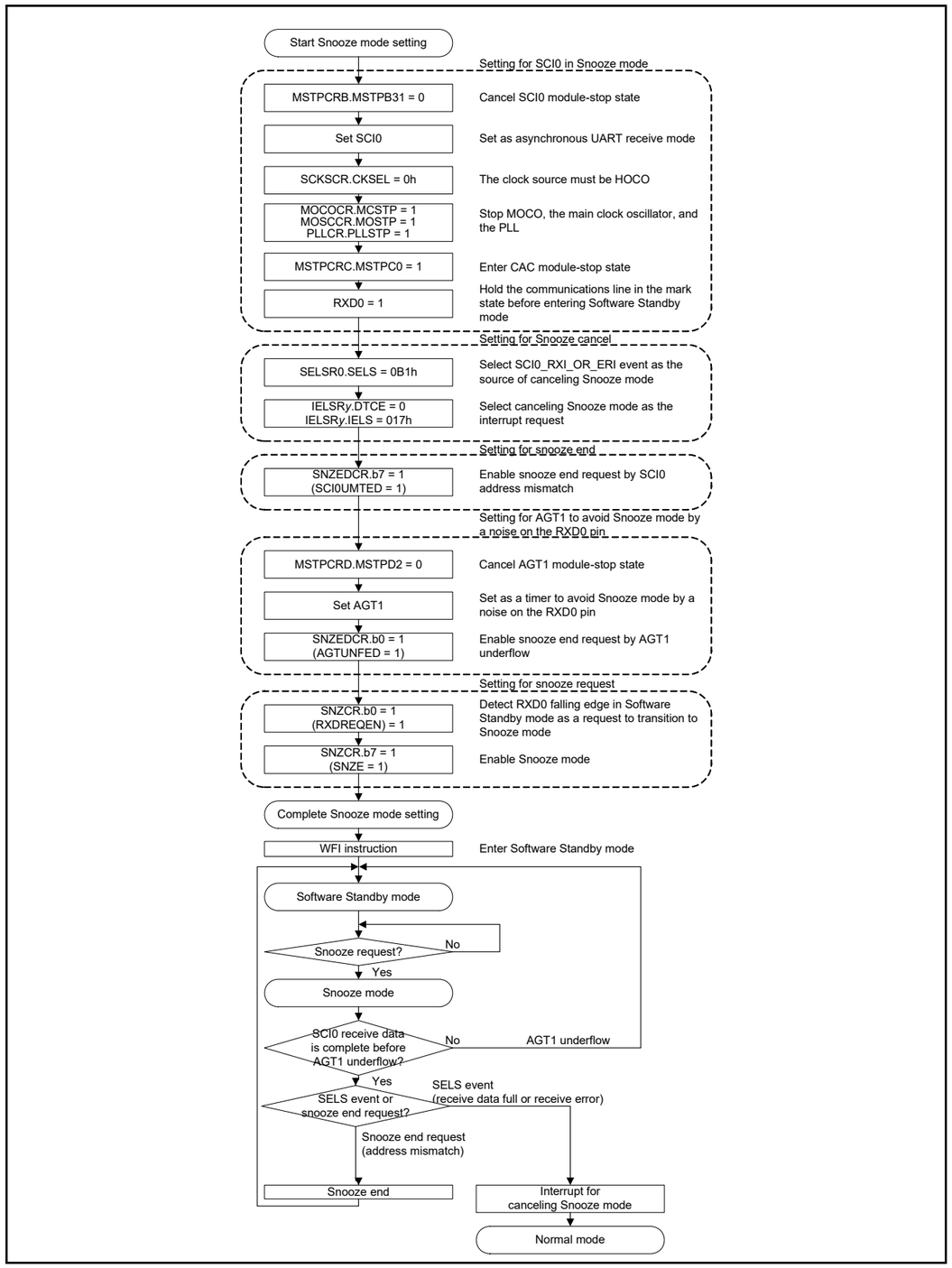


Figure 11.12 Setting example of using SCI0 in Snooze mode entry

图11.12显示了在贪睡模式进入中使用SCI0的示例设置。

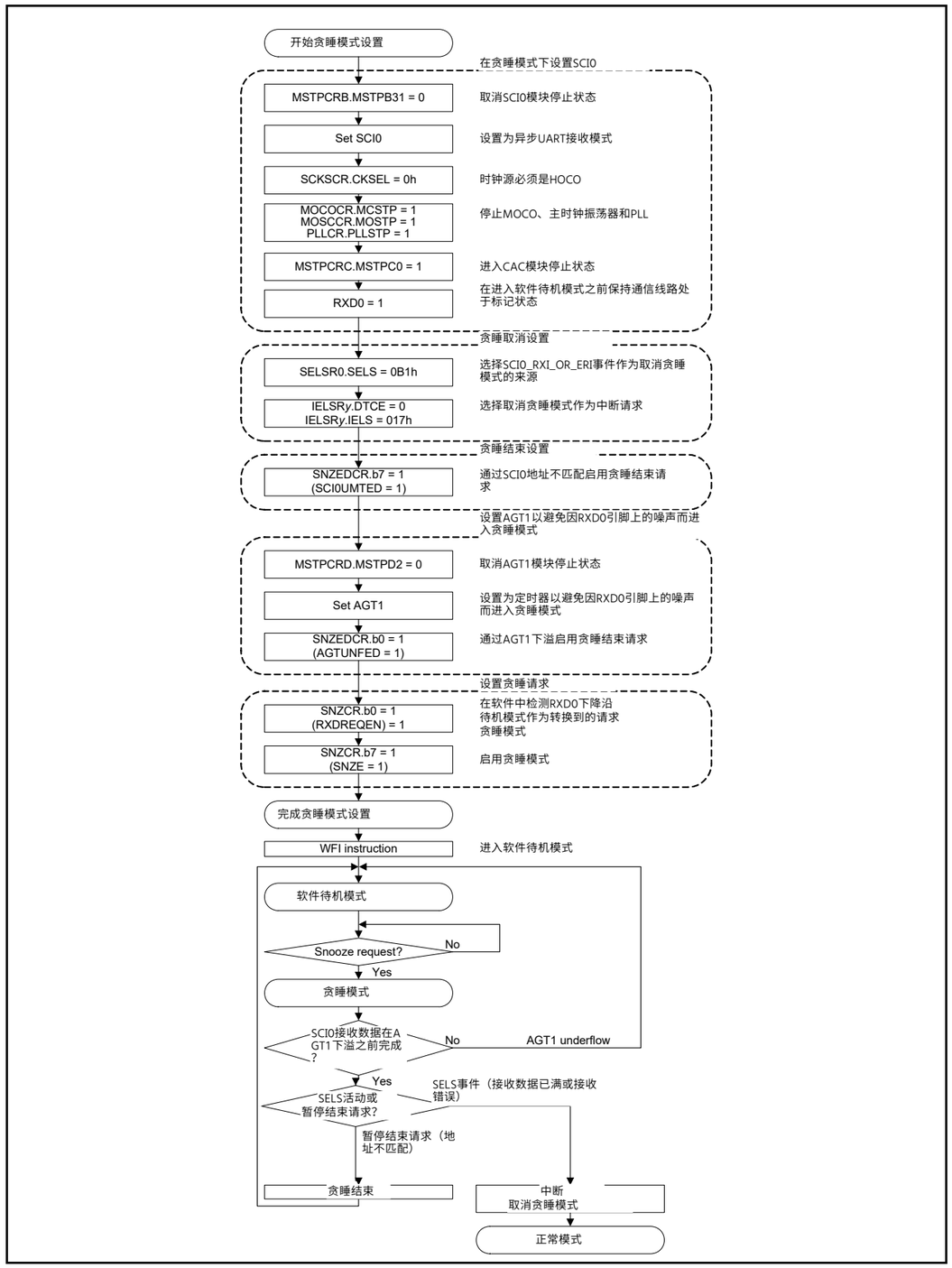


Figure 11.12 在Snooze模式进入使用SCI0的设置示例

11.9 Usage Notes

11.9.1 Register Access

(1) Do not write to registers listed in this section in any of the following conditions:

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)
- Time period from executing a WFI instruction to returning to Normal mode
- FENTRYR.FENTRY0 = 1 or FENTRYR.FENTRYD = 1 (flash P/E mode, data flash P/E mode)
- FLSTOP.FLSTPF = 1 (during transition).

(2) Valid setting of the clock-related registers

Table 11.11 and Table 11.12 show the valid setting of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting, otherwise it is ignored. Additionally, each register has some prohibited settings under certain conditions other than the operating power control modes. See section 9, Clock Generation Circuit for other conditions of each register.

Table 11.11 Valid setting for clock-related registers (1)

Mode	Valid setting								
	SCKSCR.CKSEL[2:0], CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0], SCKDIVCR.ICK[2:0]	SLCDSCKCR.LCDSCKSEL[2:0]	PLLCR.PLLSTP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed, Middle-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC) 101b (PLL)*1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	000b (LOCO) 001b (SOSC) 010b (MOSC) 100b (HOCO)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)
Low-speed, Low-voltage	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC)			1 (stop)					
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	000b (LOCO) 001b (SOSC)	1 (stop)	1 (stop)	1 (stop)	0 (operating) 1 (stop)	1 (stop)	0 (operating) 1 (stop)

Note 1. SCKSCR.CKSEL[2:0] only.

Table 11.12 Valid setting for clock-related registers (2)

Operating oscillator	Valid setting	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
PLL	0	00b, 01b
High-speed on-chip oscillator	0	00b, 01b, 10b, 11b
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	0, 1	00b, 01b, 10b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Do not write to registers listed in this section for the following condition:

[Registers]

11.9 使用说明

11.9.1 注册访问

(1) 在以下任何一种情况下，请勿写入本节中列出的寄存器：

[Registers]

- 外设名称为SYSTEM的所有寄存器。

[Conditions]

- OPCCR.OPCMTSF=1或SOPCCR.SOPCMTSF=1（在工作功率控制模式转换期间）
- 从执行WFI指令到返回正常模式的时间段
- FENTRYR.FENTRY0=1或FENTRYR.FENTRYD=1（闪存PE模式，数据闪存PE模式）
- FLSTOP.FLSTPF = 1 (during transition).

(2) 时钟相关寄存器的有效设置

表11.11和表11.12显示了每种工作电源控制模式下时钟相关寄存器的有效设置。
请勿写入有效设置以外的任何值，否则将被忽略。此外，每个寄存器在某些条件下（除了工作电源控制模式）都有一些禁止设置。有关每个寄存器的其他条件，请参见第9节，时钟生成电路。

Table 11.11 时钟相关寄存器的有效设置(1)

Mode	有效设置								
	SCKSCR.CKSEL[2:0], CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0], SCKDIVCR.ICK[2:0]	SLCDSCKCR.LCDSCKSEL[2:0]	PLLCR.PLLSTP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed, Middle-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC) 101b (PLL)*1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	000b (LOCO) 001b (SOSC) 010b (MOSC) 100b (HOCO)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stop)
Low-speed, 低电压	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC)			1 (stop)					
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	000b (LOCO) 001b (SOSC)	1 (stop)	1 (stop)	1 (stop)	0 (operating) 1 (stop)	1 (stop)	0 (operating) 1 (stop)

Note 1. SCKSCR.CKSEL[2:0] only.

Table 11.12 时钟相关寄存器的有效设置(2)

操作振荡器	有效设置	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
PLL	0	00b, 01b
High-speed on-chip oscillator	0	00b, 01b, 10b, 11b
Middle-speed on-chip oscillator		
主时钟振荡器		
Low-speed on-chip oscillator	0, 1	00b, 01b, 10b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) 对于以下情况，请勿写入本节中列出的寄存器：

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Do not write to registers listed in this section by DTC or DMAC:

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD.

(5) Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode:

[Registers]

- SNZCR, SNZEDCR, SNZREQCR.

(6) Do not set the FLSTOP.FLSTOP bit to 1 in any of the following conditions:

[Conditions]

- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 01b (Middle-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 11b (Low-speed mode)
- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(7) Do not set the MEMWAIT.MEMWAIT bit to 1 in any of the following conditions:

[Conditions]

- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 01 (Middle-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 10 (Low-voltage mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 11 (Low-speed mode)
- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(8) Write access to registers listed in this section is invalid when PRCR.PRC1 bit is 0:

[Registers]

- SBYCR, SNZCR, SNZEDCR, SNZREQCR, FLSTOP, PSMCR, OPCCR, SOPCCR.

11.9.2 I/O Port States

The I/O port states in Software Standby mode and Snooze mode, unless modifying in Snooze mode, are the same before entering the modes. Therefore, the supply current is not reduced while the output signals are held high.

11.9.3 Module-Stop State of DMAC and DTC

Before writing 1 to MSTPCRA.MSTPA22, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0. For details, see section 17, DMA Controller (DMAC) and section 18, Data Transfer Controller (DTC).

11.9.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If setting the module-stop bit while an interrupt request is generated, a CPU interrupt source or a DMAC or DTC startup source cannot be cleared. For this reason, make sure you disable the corresponding interrupts before setting the module-stop bits.

11.9.5 Transition to Low Power Modes

Because the MCU does not support wakeup by event, do not enter low power modes (Sleep mode or Software Standby mode) by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex®-M4 core because the MCU does not support low power modes by SLEEPDEEP.

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) 不要写入DTC或DMAC在本节中列出的寄存器：

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD.

(5) 不要在贪睡模式下写入本节中列出的寄存器。必须在进入软件待机模式之前设置它们：

[Registers]

- SNZCR, SNZEDCR, SNZREQCR.

(6) 在以下任何情况下都不要将FLSTOP.FLSTOP位设置为1：

[Conditions]

- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 01b (Middle-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 11b (Low-speed mode)
- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(7) 在以下任何情况下，请勿将MEMWAIT.MEMWAIT位设置为1：

[Conditions]

- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 01 (Middle-speed mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 10 (Low-voltage mode)
- SOPCCR.SOPCM = 0, OPCCR.OPCM[1:0] = 11 (Low-speed mode)
- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(8) 当PRCR.PRC1位为0时，对本节所列寄存器的写访问无效：

[Registers]

- SBYCR, SNZCR, SNZEDCR, SNZREQCR, FLSTOP, PSMCR, OPCCR, SOPCCR.

11.9.2 IO端口状态

SoftwareStandby模式和Snooze模式下的IO端口状态，除非在Snooze模式下修改，否则在进入这些模式之前是相同的。因此，当输出信号保持高电平时，电源电流不会减少。

11.9.3 DMAC和DTC的模块停止状态

在将1写入MSTPCRA.MSTPA22之前，清除DMAC的DMAST.DMST位和DTCST.DTCST位
DTC为0。有关详细信息，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

11.9.4 内部中断源

中断不会在模块停止状态下运行。如果在产生中断请求时设置模块停止位，则
无法清除CPU中断源或DMAC或DTC启动源。因此，请确保在设置模块停止位之前禁用相应的中断。

11.9.5 过渡到低功耗模式

因为MCU不支持事件唤醒，所以不要通过执行WFE指令进入低功耗模式（睡眠模式或软件待机模式）。此外，不要设置Cortex®-M4内核中系统控制寄存器的SLEEPDEEP位，因为MCU不支持SLEEPDEEP的低功耗模式。

11.9.6 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register and CS area writes are complete, in which case operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an I/O register and CS area. To avoid this problem, it is recommended that you read back the register and CS area that was written to confirm that the write completed. For example, reading the MSTPCRB register before execution of the WFI instruction can secure the period to complete writing to the I/O register.

11.9.7 Writing WDT/IWDT Registers by DMAC or DTC in Sleep Mode or Snooze Mode

Do not write registers in WDT or IWDT by DMAC or DTC while WDT or IWDT stops by entering Sleep mode or Snooze mode.

11.9.8 Oscillators in Snooze Mode

Oscillators that stop by entering Software Standby mode automatically restart when a trigger to switch to Snooze mode is generated. The MCU does not enter Snooze mode until all the oscillators stabilize. If in Snooze mode, make sure to disable oscillators that are not required in Snooze mode before entering Software Standby mode, otherwise it takes longer to transition from Software Standby mode to Snooze mode.

11.9.9 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, noise on the RXD0 pin might cause the MCU transition from Software Standby mode to Snooze mode. Any subsequent RXD0 data can be received in Snooze mode by a noise on the RXD0 pin. If the MCU does not receive RXD0 data after the noise, an interrupt such as SCI0_ERI or SCI0_RXI, and an address mismatch event is not generated, the MCU stays in Snooze mode. To avoid this, an AGT1 underflow interrupt must be used to return to Software Standby mode or Normal mode when using SCI0 in Snooze mode. However, do not use the AGT1 underflow as a source to return to Software Standby mode during an SCI communication. This causes the SCI0 to stop the operation in a half-finished state.

11.9.10 Using SCI0 in Snooze Mode

When using SCI0 in Snooze mode, a wakeup request other than an AGT1 underflow must not be used.

When using SCI0 in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, the main clock oscillator, and the PLL must stop before entering Software Standby mode
- The RXD0 pin must be kept at high level before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

11.9.11 Conditions of A/D Conversion Start in Snooze Mode

The A/D converter can only be triggered by the ELC in Snooze mode. Software trigger or ADTRG0 pin must not be used.

11.9.12 Conditions of CTSU in Snooze Mode

The CTSU can only be started by the ELC in Snooze mode.

11.9.13 ELC Event in Snooze Mode

The ELC events available in Snooze mode are listed in this section. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC140 window A/B compare match (ADC140_WCMPM)

11.9.6 WFI指令的时间安排

WFI指令可能在IO寄存器和CS区域写入完成之前执行，在这种情况下操作可能无法按预期进行。如果在写入IO寄存器和CS区域后立即放置WFI，则会发生这种情况。为避免此问题，建议您回读已写入的寄存器和CS区域以确认写入已完成。例如，在执行WFI指令之前读取MSTPCRB寄存器可以确保完成写入IO寄存器的时间。

11.9.7 在睡眠模式或贪睡模式下通过DMAC或DTC写入WDTIWDT寄存器

当WDT或IWDT通过进入休眠模式或
贪睡模式。

11.9.8 贪睡模式下的振荡器

通过进入软件待机模式停止的振荡器会在生成切换到贪睡模式的触发时自动重新启动。在所有振荡器稳定之前，MCU不会进入贪睡模式。如果处于贪睡模式，请确保在进入软件待机模式之前禁用贪睡模式中不需要的振荡器，否则从软件待机模式转换到贪睡模式需要更长的时间。

11.9.9 通过RXD0下降沿进入贪睡模式

当SNZCR.RXDREQEN位为1时，RXD0引脚上的噪声可能会导致MCU从软件待机模式转换到贪睡模式。任何后续的RXD0数据都可以通过RXD0引脚上的噪声在贪睡模式下接收。如果噪声后MCU没有接收到RXD0数据，如SCI0_ERI或SCI0_RXI等中断，并且没有产生地址不匹配事件，则MCU停留在贪睡模式。为避免这种情况，在贪睡模式下使用SCI0时，必须使用AGT1下溢中断返回到软件待机模式或正常模式。但是，不要将AGT1下溢用作SCI通信期间返回软件待机模式的源。这会导致SCI0在半完成状态下停止操作。

11.9.10 在贪睡模式下使用SCI0

在贪睡模式下使用SCI0时，不得使用除AGT1下溢以外的唤醒请求。

在贪睡模式下使用SCI0时，必须满足以下条件：

- 时钟源必须是HOCO
- MOCO、主时钟振荡器和PLL在进入软件待机模式之前必须停止
- 进入软件待机模式前，RXD0引脚必须保持高电平
- 在SCI通信期间不得转换到软件待机模式
- 在进入软件待机模式之前，MSTPCRC.MSTPC0位必须为1。

11.9.11 贪睡模式下AD转换开始的条件

AD转换器只能由ELC在贪睡模式下触发。不得使用软件触发或ADTRG0引脚。

11.9.12 CTSU在贪睡模式下的情况

CTSU只能由ELC在贪睡模式下启动。

11.9.13 贪睡模式下的ELC事件

本节列出了贪睡模式下可用的ELC事件。不要使用任何其他事件。如果进入贪睡模式后第一次启动外围模块，事件链接设置寄存器（ELSRn）必须设置贪睡模式进入事件（SYSTEM_SNZREQ）作为触发器。

- 贪睡模式进入(SYSTEM_SNZREQ)
- DTC传输结束(DTC_DTCEND)
- ADC140窗口AB比较匹配(ADC140_WCMPM)

- ADC140 window A/B compare mismatch (ADC140_WCMPUM)
- Data operation circuit interrupt (DOC_DOPCI).

11.9.14 Module-Stop Function for ADC140

When entering Software Standby mode, it is recommended that you set the ADC140 module-stop state to reduce power consumption. In this case, the ADC140 can be available in Snooze mode by releasing the ADC140 module-stop using the DTC. Similarly, set the module-stop state using the DTC before returning to Software Standby mode from Snooze mode.

11.9.15 Module-Stop Function for an Unused Circuit

A circuit that is not used in user mode might not be reset, and might operate in an unstable state because the clocks are not supplied during an MCU reset. In this case, when the MCU transitions to Low Speed mode or Software Standby mode, the supply current could increase to a value greater than the specified value (as provided in this User's Manual), by up to 600 µA. So, initialize the unused circuit using the steps shown in Figure 11.13.

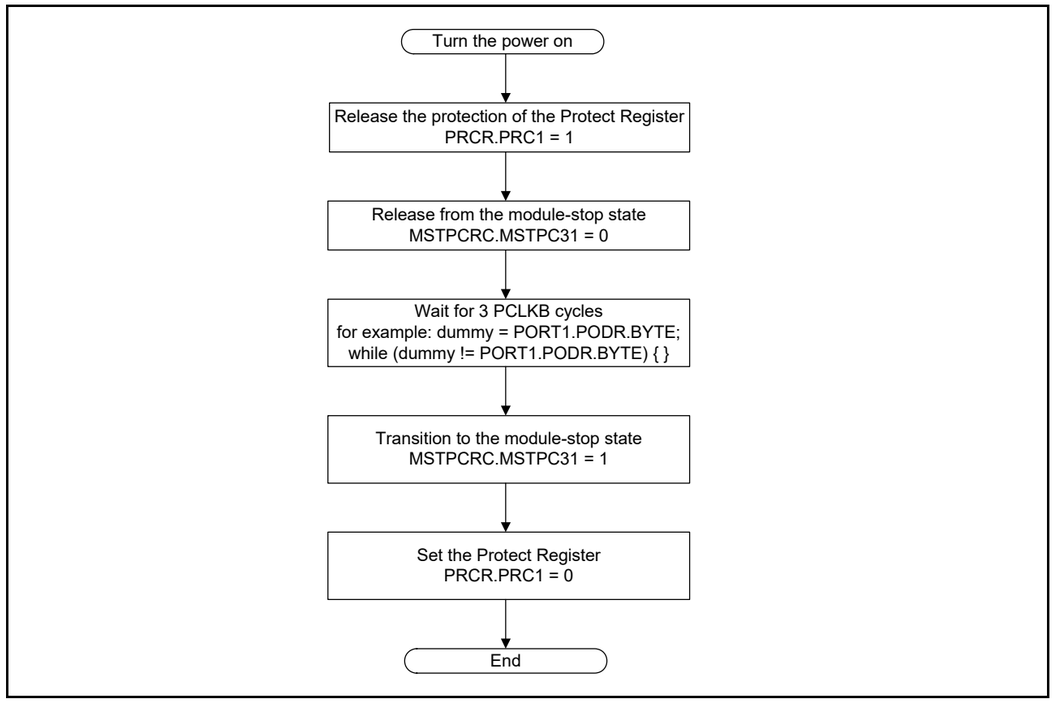


Figure 11.13 Initial setting flow example for an unused circuit

- ADC140窗口AB比较不匹配(ADC140_WCMPUM)
- 数据操作电路中断（DOC_DOPCI）。

11.9.14 ADC140的模块停止功能

进入软件待机模式时，建议您设置ADC140模块停止状态以降低功耗。在这种情况下，通过使用DTC释放ADC140模块停止，ADC140可以在贪睡模式下可用。同样，在从贪睡模式返回软件待机模式之前，使用DTC设置模块停止状态。

11.9.15 未使用电路的模块停止功能

未在用户模式下使用的电路可能不会被复位，并且可能会在不稳定的状态下运行，因为在MCU复位期间没有提供时钟。在这种情况下，当MCU转换到低速模式或软件待机模式时，电源电流可能会增加到大于指定值（如本用户手册中提供的值）的值，最高可达600µA。因此，使用图11.13中所示的步骤初始化未使用的电路。

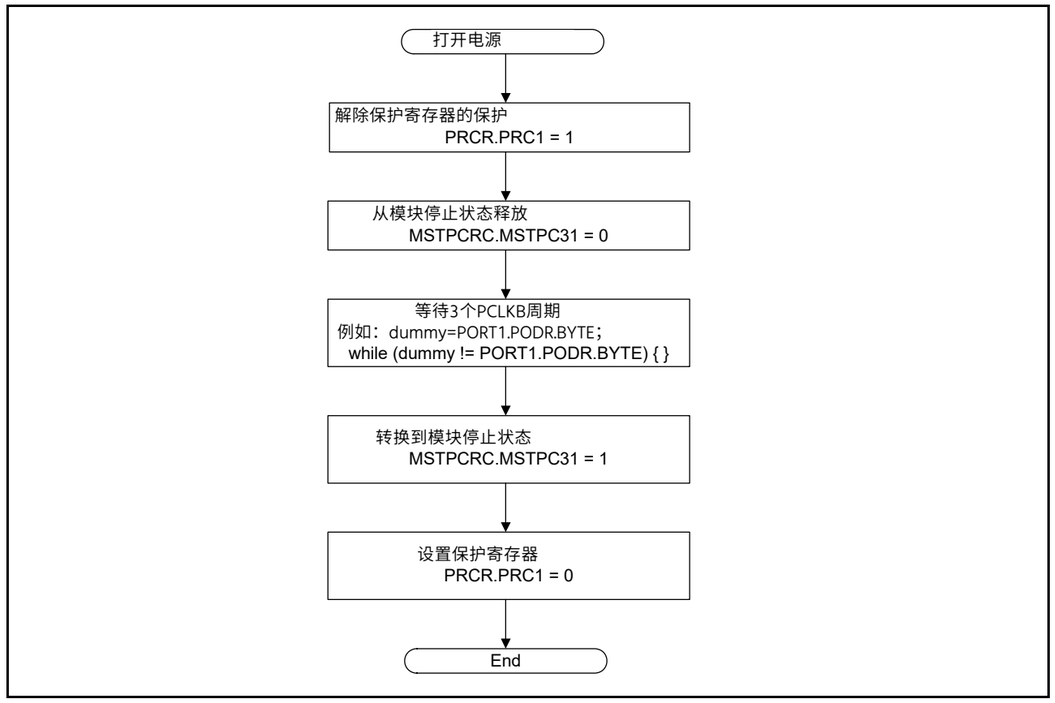


Figure 11.13 未使用电路的初始设置流程示例

12. Battery Backup Function

12.1 Overview

The MCU provides a battery backup function that maintains partial battery powering in the event of a power loss. Switching between VCC and VBATT, the battery-powered area includes RTC, SOSC, LOCO, Wakeup Control/Backup Memory, VBATT_R Low Voltage Detection, and VBATT Low Voltage Detection.

During normal operation, the battery-powered area is powered by the main power supply, the VCC pin. When a VCC voltage drop is detected, the power source switches to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source switches back from VBATT to VCC. Table 12.1 lists the VBATT wakeup I/O pin configuration.

Table 12.1 VBATT wakeup I/O pin configuration

Pin Name	I/O	Function
VBATWIO0	Input/Output	Output wakeup signal for the VBATT Wakeup Control function. External event input for the VBATT Wakeup Control function.

12.1.1 Features of Battery Backup Function

The features include:

- Battery power supply switch
- VBATT pin low voltage detection
- VBATT_R low voltage detection
- Backup registers
- VBATT wakeup control function
- Time capture pin detection.

12.1.2 Battery Power Supply Switch

When the voltage applied to the VCC pin drops, this feature switches the power supply from the VCC pin to the VBATT pin. When the voltage rises, it switches the power supply from the VBATT pin back to the VCC pin. The switch is controlled by the VBTCR1.BPWSWSTP bit. By default, switching is enabled and can be disabled by setting the VBTCR1.BPWSWSTP bit to 1.

12.1.3 VBATT Pin Low Voltage Detection

The VBATT low voltage detection function supports the battery-powered area. This function monitors whether power is supplied to the VBATT pin. It is possible to detect a low voltage condition of the power supply. The VBATT status register includes a flag to check for this low voltage detections.

12.1.4 VBATT_R Low Voltage Detection

VBATT_R low voltage detection function supports the battery-powered area. This function monitors the VBATT_R voltage level. VBATT_R is the output voltage of the battery power supply switch. This low voltage detection causes a VBATT_POR reset and initializes the battery-powered area. See details in each register description. The VBATT status register includes a flag to check for this low voltage detections.

12.1.5 Backup Registers

The battery-powered area provides 512 one-byte backup registers. These registers retain data only when VBATT is supplied and VCC is powered off. This memory is checked by the VBATT pin low voltage detection.

12.1.6 VBATT Wakeup Control Function

The VBATT wakeup control function is a function that can toggle the VBATWIO pin when the RTC alarm, periodic signal is asserted when VBATT_R is powered by the VBATT pin.

12. 电池备份功能

12.1 Overview

MCU提供电池备份功能，可在断电时保持部分电池供电。
在VCC和VBATT之间切换，电池供电区域包括RTC、SOSC、LOCO、WakeupControlBackup
内存、VBATT_R低电压检测和VBATT低电压检测。

在正常工作期间，电池供电区域由主电源VCC引脚供电。当检测到VCC电压下降时，电源切换到专用电池备用电源引脚VBATT引脚。当电压再次上升时，电源从VBATT切换回VCC。表12.1列出了VBATT唤醒IO引脚配置。

Table 12.1 VBATT唤醒IO引脚配置

引脚名称	I/O	Function
VBATWIO0	Input/Output	VBATT唤醒控制功能的输出唤醒信号。 VBATT唤醒控制功能的外部事件输入。

12.1.1 电池备份功能的特点

特点包括：

- 电池供电开关
- VBATT引脚低电压检测
- VBATT_R低电压检测
- 备份寄存器
- VBATT唤醒控制功能
- 时间捕捉引脚检测。

12.1.2 电池电源开关

当施加到VCC引脚的电压下降时，此功能将电源从VCC引脚切换到VBATT引脚。当电压上升时，它将电源从VBATT引脚切换回VCC引脚。该开关由VBTCR1.BPWSWSTP位控制。默认情况下，启用切换，可以通过将VBTCR1.BPWSWSTP位设置为1来禁用切换。

12.1.3 VBATT引脚低电压检测

VBATT低电压检测功能支持电池供电区域。该函数监视是否向VBATT引脚供电。可以检测电源的低电压状态。VBATT状态寄存器包含一个用于检查此低电压检测的标志。

12.1.4 VBATT_R低电压检测

VBATT_R低电压检测功能支持电池供电区域。该函数监控VBATT_R电压电平。VBATT_R是电池电源开关的输出电压。这种低电压检测会导致VBATT_POR复位并初始化电池供电区域。请参阅每个寄存器描述中的详细信息。VBATT状态寄存器包含一个用于检查此低电压检测的标志。

12.1.5 备份寄存器

电池供电区提供512个单字节备份寄存器。这些寄存器仅在提供VBATT且VCC断电时保留数据。该存储器由VBATT引脚低电压检测来检查。

12.1.6 VBATT唤醒控制功能

VBATT唤醒控制功能是一种可以在RTC闹钟时切换VBATWIO引脚的功能，当VBATT_R由VBATT引脚供电时，周期性信号被断言。

Note: The toggle triggered by the wakeup control function does not generate an interrupt at the ICU or a reset to the reset module. The use case of this function is that the output toggle triggers other devices on board to control the VCC power supply. For details, see section 12.3.5, VBATT Wakeup Control Function Usage.

12.1.7 Time capture Pin Detection

The RTC detects input level changes on the time capture pin, RTCIC0.
For the function of the RTCIC0 pin, see section 25, Realtime Clock (RTC). To use RTCIC0 pin, set the VBTICTLR register as described in section 12.2, Register Descriptions.

Note: When the battery backup function is not used, the VBATT pin must be connected to the VCC pin.
Note: When power is turned on, power is not supplied to the RTC, the SOSC (including multiplexed port), or the LOCO before setting the VBTCR1.BPWSWSTP bit to 1. It takes the VBATT_POR reset time tVBATPOR as described in section 48, Electrical Characteristics to supply power to the modules after setting the VBTCR1.BPWSWSTP bit. The VBTCR1.BPWSWSTP bit must be set to 1 after a power-on reset, regardless of whether the VBATT function is used. See section 12.2.1, VBATT Control Register 1 (VBTCR1) for details.

Figure 12.1 shows the configuration of the battery backup function.

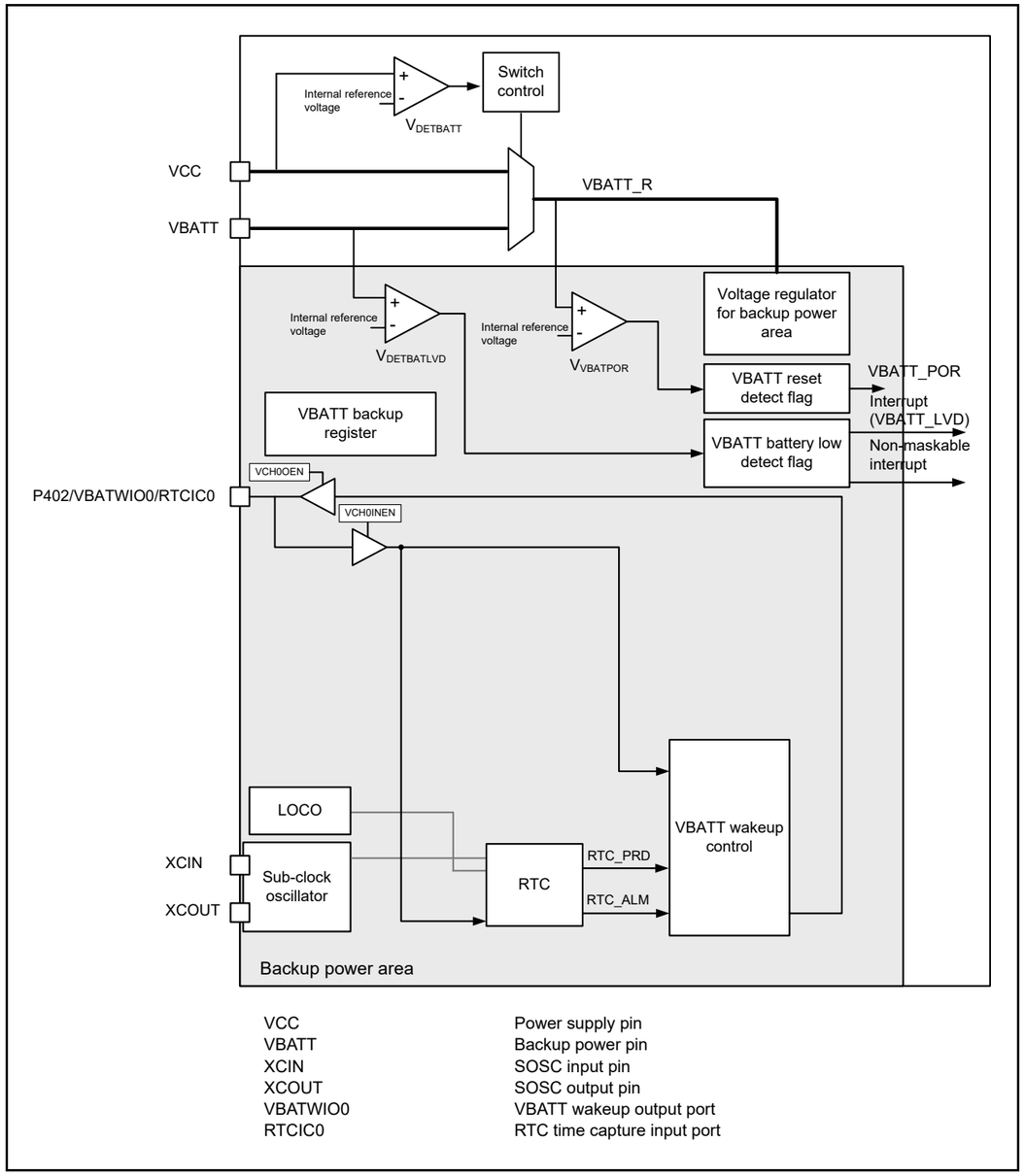
Note: 由唤醒控制功能触发的切换不会在ICU产生中断或对复位模块产生复位。此功能的用例是输出切换触发板上的其他设备来控制VCC电源。有关详细信息，请参见第12.3.5节，VBATT唤醒控制功能使用。

12.1.7 时间捕捉引脚检测

RTC检测时间捕捉引脚RTCIC0上的输入电平变化。
关于RTCIC0引脚的功能，请参见第25节，实时时钟(RTC)。要使用RTCIC0引脚，请按照第12.2节"寄存器说明"中的说明设置VBTICTLR寄存器。

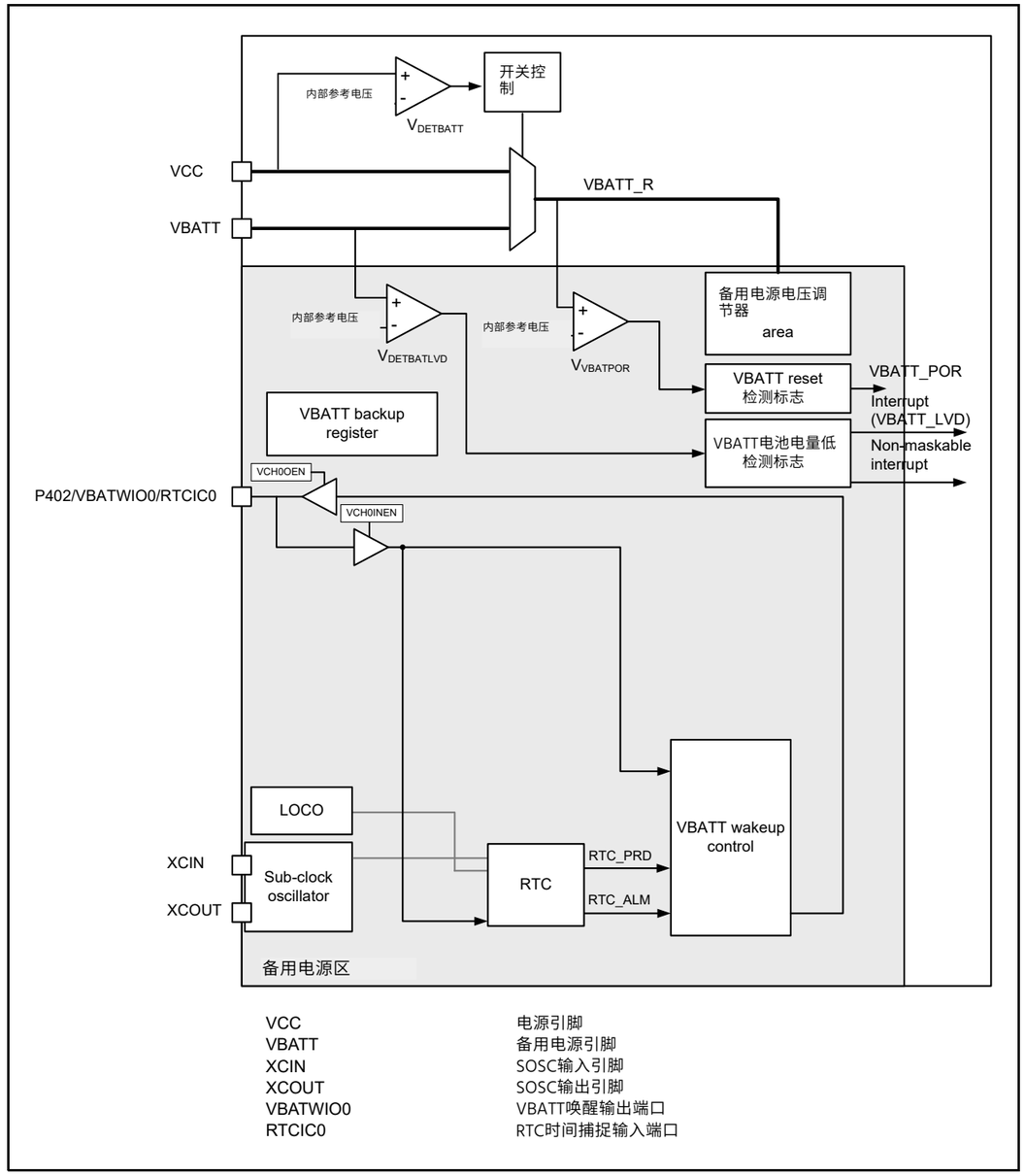
Note: 当不使用电池备份功能时，VBATT引脚必须连接到VCC引脚。
Note: 打开电源时，在将VBTCR1.BPWSWSTP位设置为1之前，不会向RTC、SOSC（包括多路复用端口）或LOCO供电。它需要VBATT_POR复位时间tVBATPOR，如第48节，电气特性中所述在设置VBTCR1.BPWSWSTP位后为模块供电。无论是否使用VBATT功能，上电复位后VBTCR1.BPWSWSTP位都必须设置为1。有关详细信息，请参见第12.2.1节，VBATT控制寄存器1(VBTCR1)。

图12.1显示了电池备份功能的配置。



VCC	Power supply pin
VBATT	Backup power pin
XCIN	SOSC input pin
XCOUT	SOSC output pin
VBATWIO0	VBATT wakeup output port
RTCIC0	RTC time capture input port

Figure 12.1 Configuration of the battery backup function



VCC	电源引脚
VBATT	备用电源引脚
XCIN	SOSC输入引脚
XCOUT	SOSC输出引脚
VBATWIO0	VBATT唤醒输出端口
RTCIC0	RTC时间捕捉输入端口

Figure 12.1 电池备份功能的配置

12.2 Register Descriptions

12.2.1 VBATT Control Register 1 (VBTCR1)

Address(es): SYSTEM.VBTCR1 4001 E41Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BPWSWSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BPWSWSTP	Battery Power Supply Switch Stop	0: Battery power supply switch enable 1: Battery power supply switch stop.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

BPWSWSTP bit (Battery Power Supply Switch Stop)

The BPWSWSTP bit can enable the battery power supply switch to switch the battery backup module supply voltage from VCC to VBATT when the voltage applied to the VCC pin drops. When stopped, the battery backup module power supply is always from VCC. To disable the battery backup function, write 1 to this bit. This bit is initialized only by power-on reset.

Note: This bit can be set without checking the VBATSR.VBTRVLD bit status.

Note: The VBTCR1.BPWSWSTP bit must be set to 1 after a power-on reset, regardless of whether the VBATT function is used. The setting flow of the VBTCR1.BPWSWSTP bit is shown in Figure 12.2. Also, the VBTCR1.BPWSWSTP bit must be cleared after other related registers are set when the VBATT function is used.

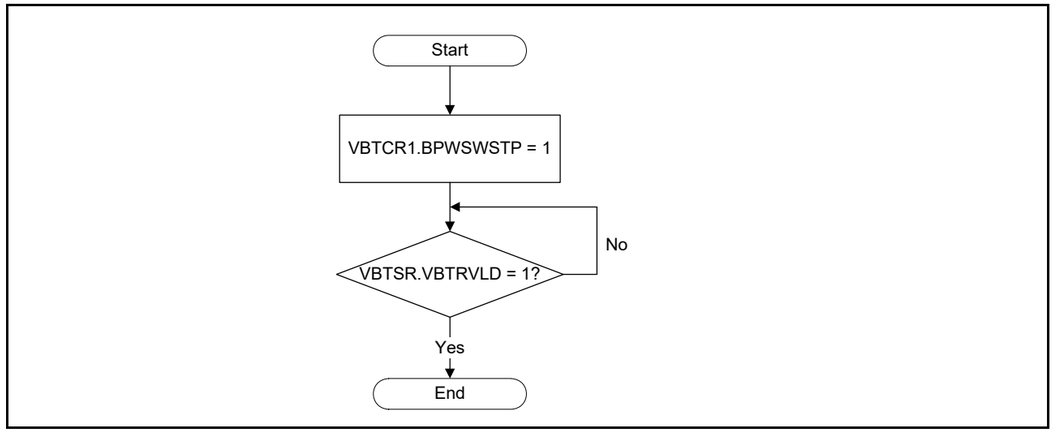


Figure 12.2 Setting flow of the VBTCR1.BPWSWSTP bit

Note: In Figure 12.2, if the VBTSR.VBTRVLD bit is not 1, it takes the VBATT_POR reset time tVBATPOR as described in section 48, Electrical Characteristics to exit the loop.
The following registers cannot be accessed when the VBTSR.VBTRVLD bit is 0. Other registers can be accessed regardless of this condition:

- LOCOCR, LOCOUTCR, SOSCCR, and SOMCR described in section 9, Clock Generation Circuit
- All registers described in this section except for VBTCR1 and the VBTSR.VBTRVLD bit
- All registers described in section 25, Realtime Clock (RTC).

12.2 注册说明

12.2.1 VBATT控制寄存器1(VBTCR1)

Address(es): SYSTEM.VBTCR1 4001 E41Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BPWSWSTP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BPWSWSTP	电池电源开关停止	0：电池供电开关使能1：电池供电开关停止。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

BPWSWSTP位（电池电源开关停止）

当施加到VCC引脚的电压下降时，BPWSWSTP位可以使能电池电源开关，将电池备份模块的电源电压从VCC切换到VBATT。停止时，备用电池模块电源始终来自VCC。要禁用电池备份功能，向该位写入1。该位仅由上电复位初始化。

Note: 无需检查VBATSR.VBTRVLD位状态即可设置该位。

Note: 无论是否使用VBATT功能，上电复位后VBTCR1.BPWSWSTP位都必须设置为1。VBTCR1.BPWSWSTP位的设置流程如图12.2所示。此外，使用VBATT功能时，必须在设置其他相关寄存器后清除VBTCR1.BPWSWSTP位。

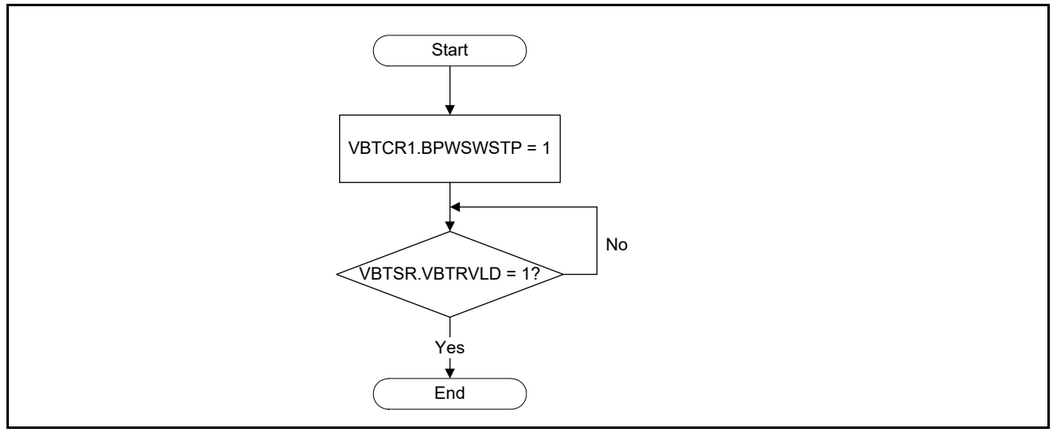


Figure 12.2 VBTCR1.BPWSWSTP位的设置流程

Note: 在图12.2中，如果VBTSR.VBTRVLD位不为1，则需要VBATT_POR复位时间tVBATPOR（如第48节，电气特性中所述）退出循环。当VBTSR.VBTRVLD位为0时，不能访问以下寄存器。无论这种情况如何，都可以访问其他寄存器：

- LOCOCR、LOCOUTCR、SOSCCR和SOMCR在第9节，时钟生成电路中描述
- 本节介绍的所有寄存器，除了VBTCR1和VBTSR.VBTRVLD位
- 第25节，实时时钟(RTC)中描述的所有寄存器。

12.2.2 VBATT Control Register 2 (VBTCR2)

Address(es): SYSTEM.VBTCR2 4001 E4B0h

	b7	b6	b5	b4	b3	b2	b1	b0
	VBTLVDLVL[1:0]		—	VBTLVDEN	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	VBTLVDEN	VBATT Pin Low Voltage Detect Enable	0: VBATT pin low voltage detection disable 1: VBATT pin low voltage detection enable.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	VBTLVDLVL[1:0]	VBATT Pin Low Voltage Detect Level Select	b7 b6 0 0: Reserved 0 1: Setting prohibited 1 0: 2.3 V 1 1: 2.1 V.	R/W

The VBTCR2 register controls the VBATT pin low voltage detection function. VBTCR2 is reset by the VBATT_POR signal.

VBTLVDEN bit (VBATT Pin Low Voltage Detect Enable)

The VBTLVDEN bit controls the VBATT pin low voltage detection.

VBTLVDLVL[1:0] bits (VBATT Pin Low Voltage Detect Level Select)

The VBTLVDLVL[1:0] bits select the VBATT pin low voltage detection level.

12.2.3 VBATT Status Register (VBTSR)

Address(es): SYSTEM.VBTSR 4001 E4B1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	VBTRVLD	—	—	VBTBLDF	VBTRDF
Value after reset:	0	0	0	0*5	0	0	0*2	1*1

Bit	Symbol	Bit name	Description	R/W
b0	VBTRDF	VBATT_R Reset Detect Flag	0: VBATT_R voltage power-on reset not detected 1: VBATT_R selected voltage power-on reset detected.	R/(W) *3
b1	VBTBLDF	VBATT Battery Low Detect Flag*4	0: VBATT pin low voltage not detected 1: VBATT pin low voltage detected.	R/(W) *3
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	VBTRVLD	VBATT_R Valid	0: VBATT_R area not valid 1: VBATT_R area valid.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This flag is only set by the VBATT_POR reset.
Note 2. This flag is only reset by the VBATT_POR reset.
Note 3. Only 0 can be written after reading 1.
Note 4. This flag is only valid when VBTLVDEN is 1. If VBTLVDEN is 0, this flag is read as 0.
Note 5. Depends on the VBATT_R voltage level.

12.2.2 VBATT控制寄存器2(VBTCR2)

Address(es): SYSTEM.VBTCR2 4001 E4B0h

	b7	b6	b5	b4	b3	b2	b1	b0
	VBTLVDLVL[1:0]		—	VBTLVDEN	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	VBTLVDEN	VBATT引脚低电压检测 Enable	0：VBATT引脚低电压检测禁止1：VBATT引脚低电压检测使能。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b7, b6	VBTLVDLVL[1:0]	VBATT引脚低电压检测电平 Select	b7 b6 0 0: Reserved 0 1：禁止设置 1 0: 2.3 V 1 1: 2.1 V.	R/W

VBTCR2寄存器控制VBATT引脚低电压检测功能。VBTCR2由VBATT_POR信号复位。

VBTLVDEN位（VBATT引脚低电压检测使能）

VBTLVDEN位控制VBATT引脚低电压检测。

VBTLVDLVL[1:0]位（VBATT引脚低电压检测电平选择）

VBTLVDLVL[1:0]位选择VBATT引脚低电压检测电平。

12.2.3 VBATT状态寄存器(VBTSR)

Address(es): SYSTEM.VBTSR 4001 E4B1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	VBTRVLD	—	—	VBTBLDF	VBTRDF
重置后的值:	0	0	0	0*5	0	0	0*2	1*1

Bit	Symbol	位名称	Description	R/W
b0	VBTRDF	VBATT_R复位检测标志	0：未检测到VBATT_R电压上电复位1：检测到VBATT_R选择电压上电复位。	R/(W) *3
b1	VBTBLDF	VBATT电池电量低检测标志*4	0：未检测到VBATT引脚低电压1：检测到VBATT引脚低电压。	R/(W) *3
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	VBTRVLD	VBATT_R Valid	0：VBATT_R区域无效1：VBATT_R区域有效。	R
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该标志仅由VBATT_POR复位设置。
Note 2. 该标志仅由VBATT_POR复位复位。
Note 3. 读1后只能写0。
Note 4. 该标志仅在VBTLVDEN为1时有效。如果VBTLVDEN为0，则该标志读为0。
Note 5. 取决于VBATT_R电压电平。

VBTRDF flag (VBATT_R Reset Detect Flag)

The VBTRDF flag indicates that a VBATT_R (selected voltage of VCC or VBATT) power-on reset occurs.

[Setting condition]

- When a VBATT_R voltage power-on reset occurs.

[Clearing condition]

- When VBTRDF is read as 1 and 0 is written to VBTRDF.

VBTBLDF flag (VBATT Battery Low Detect Flag)

The VBTBLDF flag indicates that a VBATT pin low voltage detection occurs.

[Setting condition]

- When VBATT pin low voltage detection occurs.

[Clearing condition]

- When VBTBLDF is read as 1 and 0 can be written to VBTBLDF.

VBTRVLD bit (VBATT_R Valid)

Check whether the VBATT area is valid.

The VBTRVLD bit is used to check whether the VBATT_R area is valid. It must confirm that VBTRVLD bit is 1 before writing to or reading from the following registers:

- LOCOCR, LOCOUTCR, SOSCCR, and SOMCR described in section 9, Clock Generation Circuit
- All registers described in this section except for VBTCR1 and the VBTSR.VBTRVLD bit
- All registers described in section 25, Realtime Clock (RTC).

12.2.4 VBATT Comparator Control register (VBTCMPCR)

Address(es): SYSTEM.VBTCMPCR 4001 E4B2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VBTCMPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VBTCMPE	VBATT Pin Low Voltage Detect Circuit Output Enable	0: VBATT pin low voltage detect circuit output disabled 1: VBATT pin low voltage detect circuit output enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VBTCMPE bit (VBATT Pin Low Voltage Detect Circuit Output Enable)

The VBTCMPE controls the VBATT pin low voltage detection circuit output. This bit is initialized by the VBATT_POR signal.

VBTRDF标志（VBATT_R复位检测标志）

VBTRDF标志指示发生了VBATT_R（选择的VCC或VBATT电压）上电复位。

[Setting condition]

- 当VBATT_R电压上电复位发生时。

[Clearing condition]

- 当VBTRDF被读取为1并且0被写入VBTRDF。

VBTBLDF标志（VBATT电池低电压检测标志）

VBTBLDF标志指示发生VBATT引脚低电压检测。

[Setting condition]

- 当VBATT引脚发生低电压检测时。

[Clearing condition]

- 当VBTBLDF读为1时，可以将0写入VBTBLDF。

VBTRVLD位（VBATT_R有效）

检查VBATT区域是否有效。

VBTRVLD位用于检查VBATT_R区域是否有效。在写入或读取以下寄存器之前，必须确认VBTRVLD位为1：

- LOCOCR、LOCOUTCR、SOSCCR和SOMCR在第9节，时钟生成电路中描述
- 本节介绍的所有寄存器，除了VBTCR1和VBTSR.VBTRVLD位
- 第25节，实时时钟(RTC)中描述的所有寄存器。

12.2.4 VBATT比较器控制寄存器(VBTCMPCR)

Address(es): SYSTEM.VBTCMPCR 4001 E4B2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VBTCMPE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VBTCMPE	VBATT引脚低电压检测电路输出使能	0：VBATT引脚低电压检测电路输出禁用1：VBATT引脚低电压检测电路输出使能。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTCMPE位（VBATT引脚低压检测电路输出使能）

VBTCMPE控制VBATT引脚低电压检测电路输出。该位由VBATT_POR信号初始化。

12.2.5 VBATT Pin Low Voltage Detect Interrupt Control Register (VBTLVDICR)

Address(es): SYSTEM.VBTLVDICR 4001 E4B4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VBTLVDISEL	VBTLVDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VBTLVDIE	VBATT Pin Low Voltage Detect Interrupt Enable	0: VBATT pin low voltage detection interrupt disable 1: VBATT pin low voltage detection interrupt enable.	R/W
b1	VBTLVDISEL	Pin Low Voltage Detect Interrupt Select	0: Non-maskable interrupt 1: Maskable interrupt.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTLVDICR is reset by the VBATT_POR signal.

12.2.6 VBATT Backup Register (VBTBKRn) (n = 0 to 511)

Address(es): SYSTEM.VBTBKR0 4001 E500h to SYSTEM.VBTBKR511 4001 E6FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	VBTBKR[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

VBTBKRn is an 8-bit access read/write register to store data powered by VBATT. The value of this register is retained even in VBATT mode. This register is not initialized by any reset.

Note: When accessing the VBATT backup registers, the VCC level must be over $V_{\_BKBATT}$ as described in section 48, Electrical Characteristics.

12.2.7 VBATT Wakeup Control Register (VBTWCTLR)

Address(es): SYSTEM.VBTWCTLR 4001 E4B6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VWEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VWEN	VBATT Wakeup Enable	0: Disable wakeup function 1: Enable wakeup function.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTWCTLR register controls the VBATT Wakeup function. VBTWCTLR is reset by the VBATT_POR signal.

VWEN bit (VBATT Wakeup Enable)

The VWEN bit enables the VBATT wakeup control function. When the VWEN bit is set to 0 and the VBTOCTLR.VCH0OEN bit is set to 1, the VBATWIO0 pin output is low level. When the VWEN bit is set to 1, the output from the VBATWIO0 pin changes to the level specified by the VBTOCTLR.VOUT0LSEL bit.

12.2.5 VBATT引脚低电压检测中断控制寄存器(VBTLVDICR)

Address(es): SYSTEM.VBTLVDICR 4001 E4B4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VBTLVDISEL	VBTLVDIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VBTLVDIE	VBATT引脚低电压检测中断Enable	0：VBATT引脚低电压检测中断禁止1：VBATT引脚低电压检测中断使能。	R/W
b1	VBTLVDISEL	引脚低电压检测中断选择	0: Non-maskable interrupt 1: Maskable interrupt.	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTLVDICR由VBATT_POR信号复位。

12.2.6 VBATT备份寄存器(VBTBKRn)(n=0至511)

地址：系统。VBTBKR04001E500h到系统。VBTBKR5114001E6FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	VBTBKR[7:0]							
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

VBTBKRn是一个8位访问读写寄存器，用于存储由VBATT供电的数据。即使在VBATT模式下，该寄存器的值也会保留。该寄存器不会被任何复位初始化。

Note: 访问VBATT备份寄存器时，VCC电平必须高于V_BKBATT，如第48节所述，电气特性。

12.2.7 VBATT唤醒控制寄存器(VBTWCTLR)

Address(es): SYSTEM.VBTWCTLR 4001 E4B6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VWEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VWEN	VBATT唤醒使能	0：禁用唤醒功能1：启用唤醒功能。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTWCTLR寄存器控制VBATT唤醒功能。VBTWCTLR由VBATT_POR信号复位。

VWEN位（VBATT唤醒使能）

VWEN位使能VBATT唤醒控制功能。当VWEN位设置为0且VBTOCTLR.VCH0OEN位设置为1时，VBATWIO0引脚输出为低电平。当VWEN位设置为1时，来自VBATWIO0引脚的输出变为由VBTOCTLR.VOUT0LSEL位指定的电平。

Set the VWEN bit to 1 only after setting of the following registers is complete. Set VWEN to 0 first before modifying these registers:

- VBTWCH0OTSR
- VBTICTLR
- VBTOCTLR
- VBTWTER
- VBTWEGR.

12.2.8 VBATT Wakeup I/O 0 Output Trigger Select Register (VBTWCH0OTSR)

Address(es): SYSTEM.VBTWCH0OTSR 4001 E4B8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CH0VRTCATE	CH0VRTCTE	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	CH0VRTCTE	VBATWIO0 Output RTC Periodic Signal Enable	0: VBATT wakeup I/O 0 output trigger by the RTC periodic signal is disabled 1: VBATT wakeup I/O 0 output trigger by the RTC periodic signal is enabled.	R/W
b4	CH0VRTCATE	VBATWIO0 Output RTC Alarm Signal Enable	0: VBATT wakeup I/O 0 output trigger by the RTC alarm signal is disabled 1: VBATT wakeup I/O 0 output trigger by the RTC alarm signal is enabled.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTWCH0OTSR controls the VBATT wakeup I/O 0 output trigger source.

If this register bit is set to 1 and the associated wakeup trigger flag in the VBTWFR register is set, the VBATWIO0 pin outputs a signal based on the VOUT0LSEL bit in the VBTOCTLR register.

The VBTWCH0OTSR register is initialized by the VBATT_POR signal.

12.2.9 VBATT Input Control Register (VBTICTLR)

Address(es): SYSTEM.VBTICTLR 4001 E4BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VCH0INEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VCH0INEN	VBATT Wakeup I/O 0 Input Enable	0: VBATWIO0, RTCIC0 inputs disabled 1: VBATWIO0, RTCIC0 inputs enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTICTLR register selects VBATT wakeup I/O pin input direction. VBTICTLR is reset by the VBATT_POR signal.

只有在以下寄存器的设置完成后，才将VWEN位设置为1。在修改这些寄存器之前先将VWEN设置为0：

- VBTWCH0OTSR
- VBTICTLR
- VBTOCTLR
- VBTWTER
- VBTWEGR.

12.2.8 VBATT唤醒IO0输出触发选择寄存器(VBTWCH0OTSR)

Address(es): SYSTEM.VBTWCH0OTSR 4001 E4B8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CH0VRTCATE	CH0VRTCTE	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	CH0VRTCTE	VBATWIO0输出RTC周期信号使能	0：禁用由RTC周期信号触发的VBATT唤醒IO0输出 1：使能由RTC周期信号触发的VBATT唤醒IO0输出 。	R/W
b4	CH0VRTCATE	VBATWIO0输出RTC报警信号Enable	0：禁用由RTC闹钟信号触发的VBATT唤醒IO0输出 1：使能由RTC闹钟信号触发的VBATT唤醒IO0输出	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTWCH0OTSR控制VBATT唤醒IO0输出触发源。

如果该寄存器位设置为1，并且VBTWFR寄存器中的相关唤醒触发标志被设置，则VBATWIO0引脚根据VBTOCTLR寄存器中的VOUT0LSEL位输出一个信号。

VBTWCH0OTSR寄存器由VBATT_POR信号初始化。

12.2.9 VBATT输入控制寄存器(VBTICTLR)

Address(es): SYSTEM.VBTICTLR 4001 E4BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VCH0INEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VCH0INEN	VBATT唤醒IO0输入使能	0：VBATWIO0、RTCIC0输入禁用1：VBATWIO0、RTCIC0输入启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTICTLR寄存器选择VBATT唤醒IO引脚输入方向。VBTICTLR由VBATT_POR信号复位。

VCH0INEN bit (VBATT Wakeup I/O n Input Enable Bit)

The VCHnINEN bit defines the VBATT wakeup I/O pin input enable. You must set the VBTICTLR register when using only the VBATT wakeup control function but also the time capture function of RTC (RTCIC0). For these functions, see section 25, Realtime Clock (RTC).

12.2.10 VBATT Output Control Register (VBTOCTLR)

Address(es): SYSTEM.VBTOCTLR 4001 E4BCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	VOUT0LSEL	—	—	VCH0OEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VCH0OEN	VBATT Wakeup I/O 0 Output Enable	0: VBATWIO0 output disabled 1: VBATWIO0 output enabled.*1	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	VOUT0LSEL	VBATT Wakeup I/O 0 Output Level Selection	0: Output L before VBATT wakeup trigger 1: Output H before VBATT wakeup trigger.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTOCTLR register selects the VBATT wakeup I/O (VBATWIO0) pin output direction and output level. VBTOCTLR is reset by the VBATT_POR signal.

VCH0OEN bit (VBATT Wakeup I/O 0 Output Enable Bit)

The VCH0OEN bit defines the VBATT output enable.

Note 1. When the VCH0OEN bit is set to 1, P402PFS.PMR bit must be 0.

VOUT0LSEL bit (VBATT Wakeup I/O 0 Output Level Selection)

The VOUT0LSEL bit defines the output level from the VBATT wakeup I/O 0 pin. When the VOUT0LSEL bit is set to 0, VBATWIO0 pin outputs low before receiving the VBATT wakeup trigger and high after receiving the VBATT wakeup trigger. When the VOUT0LSEL bit is set to 1, the VBATWIO0 pin outputs high before the VBATT wakeup trigger and low after receiving the VBATT wakeup trigger.

12.2.11 VBATT Wakeup Trigger Source Enable Register (VBTWTER)

Address(es): SYSTEM.VBTWTER 4001 E4BDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	VRTCAE	VRTCIE	—	—	VCH0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VCH0E	VBATWIO0 Pin Enable	0: VBATT wakeup triggered by the VBATWIO0 pin is disabled 1: VBATT wakeup triggered by the VBATWIO0 pin is enabled.	R/W
b2 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	VRTCIE	RTC Periodic Signal Enable	0: VBATT wakeup triggered by RTC periodic signal is disabled 1: VBATT wakeup triggered by RTC periodic signal is enabled.	R/W
b4	VRTCAE	RTC Alarm Signal Enable	0: VBATT wakeup triggered by RTC alarm signal is disabled 1: VBATT wakeup triggered by RTC alarm signal is enabled.	R/W

VCH0INEN位（VBATT唤醒IOn输入使能位）

VCHnINEN位定义了VBATT唤醒IO引脚输入使能。仅使用VBATT唤醒控制功能和RTC(RTCIC0)的时间捕捉功能时，必须设置VBTICTLR寄存器。对于这些功能，请参见第25节，实时时钟(RTC)。

12.2.10 VBATT输出控制寄存器(VBTOCTLR)

Address(es): SYSTEM.VBTOCTLR 4001 E4BCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	VOUT0LSEL	—	—	VCH0OEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VCH0OEN	VBATT唤醒IO0输出使能	0：VBATWIO0输出禁用1：VBATWIO0输出启用。*1	R/W
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	VOUT0LSEL	VBATT唤醒IO0输出电平Selection	0：VBATT唤醒触发前输出L1：VBATT唤醒触发前输出H。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTOCTLR寄存器选择VBATT唤醒IO(VBATWIO0)引脚输出方向和输出电平。
VBTOCTLR由VBATT_POR信号复位。

VCH0OEN位（VBATT唤醒IO0输出使能位）

VCH0OEN位定义VBATT输出使能。

注1.当VCH0OEN位设置为1时，P402PFS.PMR位必须为0。

VOUT0LSEL位（VBATT唤醒IO0输出电平选择）

VOUT0LSEL位定义VBATT唤醒IO0引脚的输出电平。当VOUT0LSEL位设置为0时，VBATWIO0引脚在收到VBATT唤醒触发前输出低电平，在收到VBATT唤醒触发后输出高电平。当VOUT0LSEL位设置为1时，VBATWIO0引脚在VBATT唤醒触发前输出高电平，在收到VBATT唤醒触发后输出低电平。

12.2.11 VBATT唤醒触发源使能寄存器(VBTWTER)

Address(es): SYSTEM.VBTWTER 4001 E4BDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	VRTCAE	VRTCIE	—	—	VCH0E
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VCH0E	VBATWIO0引脚使能	0：禁用由VBATWIO0引脚触发的VBATT唤醒1：使能由VBATWIO0引脚触发的VBATT唤醒。	R/W
b2 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	VRTCIE	RTC周期信号使能	0：禁止由RTC周期信号触发的VBATT唤醒1：使能由RTC周期信号触发的VBATT唤醒。	R/W
b4	VRTCAE	RTC警报信号启用	0：禁止由RTC闹钟信号触发的VBATT唤醒1：使能由RTC闹钟信号触发的VBATT唤醒。	R/W

b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTWTER register enables or disables the VBATT wakeup trigger. VBTWTER is reset by the VBATT_POR signal.

Multiple trigger source selection is possible.

12.2.12 VBATT Wakeup Trigger Source Edge Register (VBTWEGR)

Address(es): SYSTEM.VBTWEGR 4001 E4BEh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VCH0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VCH0EG	VBATWIO0 Wakeup Trigger Source Edge Select	0: Wakeup trigger is generated at a falling edge 1: Wakeup trigger is generated at a rising edge.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTWEGR register selects the edge of each VBATT wakeup trigger sources. The VBTWEGR register is reset by the VBATT_POR signal.

12.2.13 VBATT Wakeup Trigger Source Flag Register (VBTWFR)

Address(es): SYSTEM.VBTWFR 4001 E4BFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	VRTCAF	VRTCIF	—	—	VCH0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VCH0F	VBATWIO0 Wakeup Trigger Flag	0: No wakeup trigger by the VBATWIO0 pin is generated 1: A wakeup trigger by the VBATWIO0 pin is generated.	R/(W)*1
b2 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	VRTCIF	VBATT RTC-Periodic Wakeup Trigger Flag	0: No wakeup trigger by the RTC periodic signal is generated 1: A wakeup trigger by the RTC periodic signal is generated.	R/(W)*1
b4	VRTCAF	VBATT RTC-Alarm Wakeup Trigger Flag	0: No wakeup trigger by the RTC alarm signal is generated 1: A wakeup trigger by the RTC alarm signal is generated.	R/(W)*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag after reading 1.

The VBTWFR register indicates the triggering factor of the VBATT wakeup control function. This register is protected by the VWEN bit (VBTWCTLR register). VBTWFR is valid 5 PCLKB cycles after writing 1 to VWEN bit enable. Similarly, disabling VBTWFR takes 5 PCLKB cycles after writing 0 to VWEN bit.

Each flag is set to 1 when a trigger request specified by VBTWEGR is generated.

b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTWTER寄存器启用或禁用VBATT唤醒触发器。VBTWTER由VBATT_POR信号复位。

可以选择多个触发源。

12.2.12 VBATT唤醒触发源边沿寄存器(VBTWEGR)

Address(es): SYSTEM.VBTWEGR 4001 E4BEh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VCH0EG
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VCH0EG	VBATWIO0唤醒触发源边沿Select	0：在下降沿产生唤醒触发1：在上升沿产生唤醒触发。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTWEGR寄存器选择每个VBATT唤醒触发源的边沿。VBTWEGR寄存器由VBATT_POR信号复位。

12.2.13 VBATT唤醒触发源标志寄存器(VBTWFR)

Address(es): SYSTEM.VBTWFR 4001 E4BFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	VRTCAF	VRTCIF	—	—	VCH0F
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VCH0F	VBATWIO0唤醒触发标志	0：VBATWIO0引脚不产生唤醒触发1：VBATWIO0引脚产生唤醒触发。	R/(W)*1
b2 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	VRTCIF	VBATTRTC-周期性唤醒触发标志	0：不产生RTC周期信号的唤醒触发1：产生RTC周期信号的唤醒触发。	R/(W)*1
b4	VRTCAF	VBATTRTC-Alarm唤醒触发标志	0：不产生由RTC闹钟信号产生的唤醒触发1：产生由RTC闹钟信号产生的唤醒触发。	R/(W)*1
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 读1后只能写0清除标志。

VBTWFR寄存器指示VBATT唤醒控制功能的触发因素。该寄存器受VWEN位（VBTWCTLR寄存器）保护。VBTWFR在将1写入VWEN位使能后的5个PCLKB周期内有效。同样，在向VWEN位写入0后，禁用VBTWFR需要5个PCLKB周期。

当生成由VBTWEGR指定的触发请求时，每个标志都设置为1。

The VBTWFR register is initialized by VBATT_POR.

VCH0F flags (VBATT Wakeup I/O 0 Wakeup Trigger Flag)

These flags indicate that a trigger request by the VBATWIO0 pin is generated.

[Setting condition]

- A trigger request by the VBATWIO0 pin specified by VBTWEGR is generated.

[Clearing condition]

- Each bit is read as 1 then written as 0.

VRTCIF flag (VBATT RTC-Periodic Wakeup Trigger Flag)

This flag indicates that a trigger request by the RTC periodic signal is generated.

[Setting condition]

- A trigger request by the RTC periodic signal is generated.

[Clearing condition]

- This bit is read as 1 and written as 0.

VRTCAF flag (VBATT RTC-Alarm Wakeup Trigger Flag)

This flag indicates that a trigger request by the RTC alarm signal is generated.

[Setting condition]

- A trigger request by the RTC alarm signal is generated.

[Clearing condition]

- This bit is read as 1 and written as 0.

12.2.14 Backup Register Access Control Register (BKRACR)

Address(es): SYSTEM.BKRACR 4001 E0C6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	BKRACS[2:0]		
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	BKRACS[2:0]	Backup Register Access cycle Select	b2 b0 0 0 0: Access cycle control disable. When System clock source is SOSC or LOCO. 1 1 0: Access cycle control enable. System clock source is other than SOSC or LOCO. Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The BKRACR register controls the access cycle for the backup register to reduce power consumption. When access cycle control is enabled (110b), the access cycle for the backup register is 64 times that of when it is disabled (000b). The BKRACR is initialized by all the resets except for VBATT_POR.

[Setting Procedure]

To change the system clock from other than SOSC/LOCO to SOSC/LOCO:

1. Change the SCKSCR.CKSEL[2:0] bits.
2. Change the BKRACR.BKRACS[2:0] bits to 000b.

VBTWFR寄存器由VBATT_POR初始化。

VCH0F标志（VBATT唤醒IO0唤醒触发标志）

这些标志表明产生了VBATWIO0引脚的触发请求。

[Setting condition]

- 由VBTWEGR指定的VBATWIO0引脚产生一个触发请求。

[Clearing condition]

- 每个位读为1，然后写为0。

VRTCIF标志（VBATTRTC-周期性唤醒触发标志）

该标志表示生成了RTC周期信号的触发请求。

[Setting condition]

- 由RTC周期信号产生一个触发请求。

[Clearing condition]

- 该位读为1，写为0。

VRTCAF标志（VBATTRTC-Alarm唤醒触发标志）

该标志表示生成了RTC警报信号的触发请求。

[Setting condition]

- 由RTC报警信号产生一个触发请求。

[Clearing condition]

- 该位读为1，写为0。

12.2.14 备份寄存器访问控制寄存器(BKRACR)

Address(es): SYSTEM.BKRACR 4001 E0C6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	BKRACS[2:0]		
重置后的值：	0	0	0	0	0	1	1	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	BKRACS[2:0]	备份寄存器访问周期选择	b2 b0 000：访问周期控制禁用。当系统时钟源为SOSC或LOCO时。 110：访问周期控制使能。系统时钟源不是SOSC或LOCO。 禁止其他设置。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

BKRACR寄存器控制备份寄存器的访问周期以降低功耗。当访问周期控制启用时（110b），备份寄存器的访问周期是禁用时（000b）时的访问周期的64倍。BKRACR由除VBATT_POR之外的所有复位进行初始化。

[Setting Procedure]

要将系统时钟从非SOSCLOCO更改为SOSCLOCO：

1. 更改SCKSCR.CKSEL[2:0]位。
2. 将BKRACR.BKRACS[2:0]位更改为000b。

To change the system clock from SOSC/LOCO to other than SOSC/LOCO:

1. Change the BKRACR.BKRACS[2:0] bits to 110b.
2. Change the SCKSCR.CKSEL[2:0] bits.

12.3 Operation

12.3.1 Battery Backup Function

When the voltage at the VCC pin drops, power can be supplied to the RTC, LOCO, and sub-clock oscillator from the VBATT pin. When the power supply drop from the VCC pin is detected, the connection to power is switched from the power supply to the VBATT pin. The power supply from the VCC pin resumes when the voltage at the VCC pin exceeds VDETBATT. This power supply change does not affect the RTC operation. When the voltage level at the VBATT pin voltage drops below the operation-guaranteed voltage, it is possible to monitor the VBTBLDF bit in the VBATT Status Register.

The battery backup function can be used after the voltage monitor 0 reset is enabled.

While VBATT supplies the power, the wakeup control function can toggle the output pin of VBATWIO0 by triggering the RTC alarm/periodic signal.

The RTC supports time capture pin detection when the time capture pin input level changes.

The VBATT pin supplies power to the following modules.

- RTC
- Sub-clock oscillator (including XCIN and XCOUT pins)
- VBATWIO0 pin (including RTCIC0)
- LOCO
- VBATT Backup Register
- VBATT wakeup controller.

Table 12.2 shows the operating states in VBATT mode.

Table 12.2 Operating states in VBATT mode (1 of 2)

Operating state	VBATT mode
Transition condition	Detection of VCC voltage drop
Canceling method other than reset	Detection of VCC voltage rise
Main clock oscillator	Stopped
Sub-clock oscillator	Operation can be selected by SOSCCR.SOSTP bit. The status of the oscillator is the same as before entering VBATT mode.
High-speed on-chip oscillator	Stopped
Middle-speed on-chip oscillator	Stopped
Low-speed on-chip oscillator	Operation or non-operation can be selected in the LOCOCR.LCSTP bit. The status of the oscillator is the same as before entering VBATT mode.
IWDT-dedicated on-chip oscillator	Stopped
PLL	Stopped
CPU	Stopped (undefined)
SRAM (ECC SRAM included)	Stopped (undefined)
VBATT Backup Register	Stopped (retained)
Flash memory	Stopped (retained)
Realtime Clock (RTC)	Selectable when the selecting clock operates as the count source
AGTn (n = 0, 1)	Stopped (undefined)
Low Voltage Detection (LVD)	Stopped

要将系统时钟从SOSCLOCO更改为SOSCLOCO以外的时钟：

1. 将BKRACR.BKRACS[2:0]位更改为110b。
2. 更改SCKSCR.CKSEL[2:0]位。

12.3 Operation

12.3.1 电池备份功能

当VCC引脚的电压下降时，可以从
VBATT引脚。当检测到VCC引脚的电源下降时，电源连接从电源切换到VBATT引脚。当VCC引脚上的电压超过VDETBATT时，来自VCC引脚的电源恢复。此电源更改不会影响RTC操作。当VBATT引脚电压下降到低于操作保证电压时，可以监控VBATT状态寄存器中的VBTBLDF位。

启用电压监控器0复位后，可以使用电池备份功能。

当VBATT供电时，唤醒控制功能可以通过触发RTC闹钟周期信号来切换VBATWIO0的输出引脚。

当时间捕捉引脚输入电平发生变化时，RTC支持时间捕捉引脚检测。

VBATT引脚为以下模块供电。

- RTC
- 副时钟振荡器（包括XCIN和XCOUT引脚）
- VBATWIO0 pin (including RTCIC0)
- LOCO
- VBATT备份寄存器
- VBATT唤醒控制器。

表12.2显示了VBATT模式下的操作状态。

Table 12.2 VBATT模式下的操作状态（1of2）

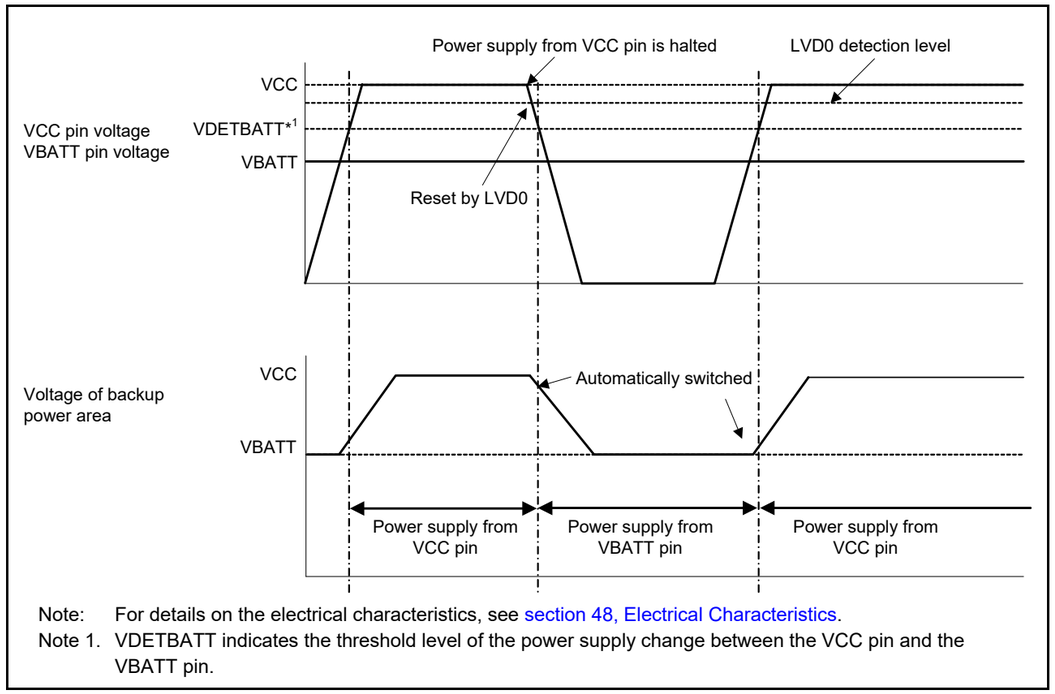
运行状态	VBATT mode
过渡条件	检测VCC电压降
复位以外的取消方法	检测VCC电压上升
主时钟振荡器	Stopped
Sub-clock oscillator	可以通过SOSCCR.SOSTP位选择操作。振荡器的状态与进入VBATT模式前相同。
High-speed on-chip oscillator	Stopped
Middle-speed on-chip oscillator	Stopped
Low-speed on-chip oscillator	可以在LOCOCR.LCSTP位中选择操作或不操作。振荡器的状态与进入VBATT模式前相同。
IWDT-dedicated on-chip oscillator	Stopped
PLL	Stopped
CPU	Stopped (undefined)
SRAM (ECC SRAM included)	Stopped (undefined)
VBATT备份寄存器	Stopped (retained)
闪存	Stopped (retained)
实时时钟(RTC)	选择时钟作为计数源时可选择
AGTn (n = 0, 1)	Stopped (undefined)
低电压检测(LVD)	Stopped

Table 12.2 Operating states in VBATT mode (2 of 2)

Operating state	VBATT mode
Power-on reset circuit	Stopped
Battery backup voltage monitor	Operating
Other peripheral modules	Stopped (undefined)
I/O ports	• RTCIC0 port: Operating • Other than the specified ports: Undefined • VBATWIO0 port: Operating.

Note: Selectable means that operating can be selected in the control register. Some modules are also controlled by the associated module-stop bit.
Stopped (retained) means that the contents of the internal registers are retained but the operations are suspended.
Stopped (undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.

Figure 12.3 shows the switching sequence of the battery backup function.



Note: For details on the electrical characteristics, see section 48, Electrical Characteristics.
Note 1. VDETBATT indicates the threshold level of the power supply change between the VCC pin and the VBATT pin.

Figure 12.3 Switching sequence for the battery backup function

12.3.2 VBATT Battery Power Supply Switch Usage

The battery power supply switch can switch the power supply from the VCC pin to the VBATT pin when the voltage applied to the VCC pin drops. When the voltage rises, this switch changes the power supply from the VBATT pin to the VCC pin. The switch is controlled by the VBTCR1.BPWSWSTP bit.

The BPWSWSTP bit can enable the battery power supply switch which can switch the battery backup module supply voltage from VCC to VBATT when the VCC voltage falls. When the battery power supply switch stops, the battery backup module power supply is always from VCC. If you are not using the battery backup function, you must write 1 to this bit.

Note: You can use the battery backup function after the voltage monitor 0 reset is enabled (OFS1.LVDAS bit is 0). Voltage monitor 0 level should be higher than the VDETBATT level (OFS1.VDSEL1[2:0] bits are 001b, or 010b).
Note: This bit can be set without verifying the VBTSR.VBTRVLD bit status.

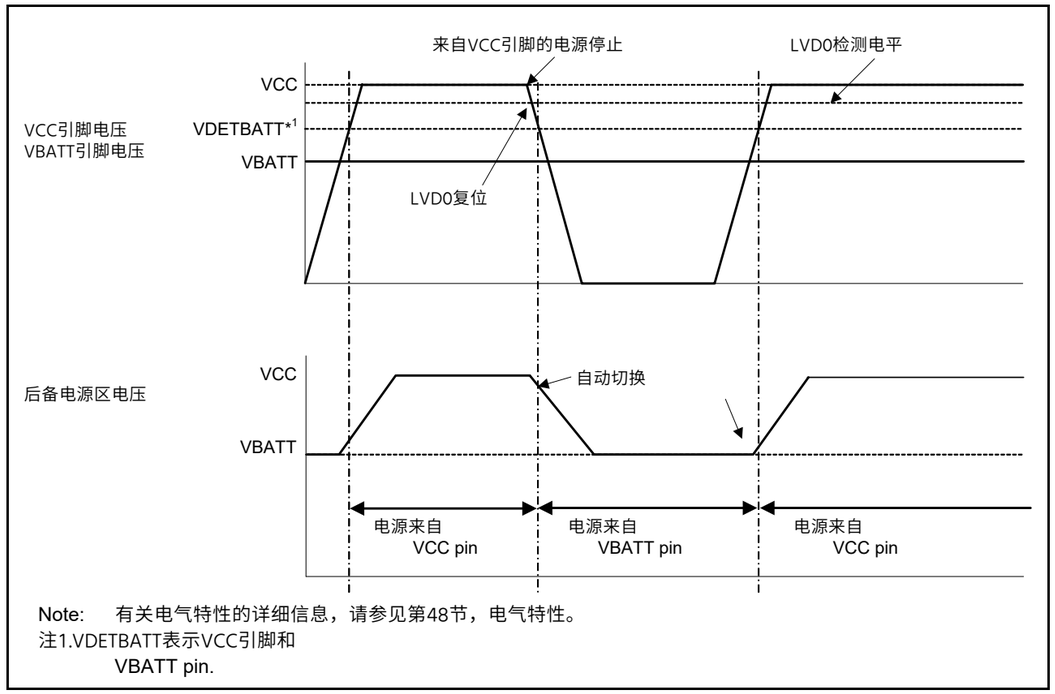
Table 12.2 VBATT模式下的操作状态（2个中的2个）

运行状态	VBATT mode
上电复位电路	Stopped
备用电池电压监测器	Operating
其他外围模块	Stopped (undefined)
I/O ports	RTCIC0端口：运行中 指定端口以外：未定义 VBATWIO0端口：运行中。

Note: Selectable表示可以在控制寄存器中选择操作。一些模块也由相关的模块停止位控制。停止（retained）是指内部寄存器的内容被保留，但操作被暂停。

停止（未定义）表示内部寄存器的内容未定义，内部电路的电源被切断。

图12.3显示了电池备份功能的切换顺序。



Note: 有关电气特性的详细信息，请参见第48节，电气特性。
注1.VDETBATT表示VCC引脚和 VBATT pin.

Figure 12.3 电池备份功能的切换顺序

12.3.2 VBATT电池电源开关使用

当施加到VCC引脚的电压下降时，电池电源开关可以将电源从VCC引脚切换到VBATT引脚。当电压上升时，该开关将电源从VBATT引脚切换到VCC引脚。该开关由VBTCR1.BPWSWSTP位控制。

BPWSWSTP位可以使能电池供电开关，当VCC电压下降时，可以将电池备份模块的供电电压从VCC切换到VBATT。当电池供电开关停止时，电池后备模块电源始终由VCC供电。如果不使用电池备份功能，则必须向该位写入1。

Note: 使能电压监视器0复位（OFS1.LVDAS位为0）后，您可以使用电池备份功能。
电压监视器0电平应高于VDETBATT电平（OFS1.VDSEL1[2:0]位为001b或010b）。
Note: 无需验证VBTSR.VBTRVLD位状态即可设置该位。

12.3.3 VBATT Pin Low Voltage Detection Procedures

The VBTSR.VBTBLDF flag and interrupt can be used to monitor VBATT pin low voltage detection using the procedures described in this section.

The following procedure shows how to enable the VBATT pin low voltage detection:

1. Set the voltage monitor 0 reset. See section 8, Low Voltage Detection (LVD).
2. Set the VBTCR1.BPWSWSTP bit to 1 if the access to this bit is for the first access after a power-on reset.
3. Wait for the VBTSR.VBTRVLD bit to be 1 and ensure that the VBTCR2.VBTLVDEN, VBTLVDICR.VBTLVDIE, and VBTCMPCR.VBTCMPE bits are 0.
4. Specify the detection voltage in the VBTCR2.VBTLVDLVL[1:0] bits (VBATT pin voltage detect level select).
5. Select the type of interrupt in the VBTLVDICR.VBTLVDISEL bit.
6. Set the VBTCR2.VBTLVDEN bit to 1 for enabling VBATT pin low voltage detection.
7. After waiting for the VBATT comparator operation stabilization time (t_{d_vbat}) as described in section 48, Electrical Characteristics, set the VBTCMPCR.VBTCMPE bit to 1 for the VBATT pin voltage detect circuit to be enabled.
8. Make sure that the VBTSR.VBTBLDF flag is 0, and then set the VBTLVDICR.VBTLVDIE bit to 1 for the VBATT pin low voltage detection interrupt output to be enabled.
9. Clear the VBTCR1.BPWSWSTP bit to 0 to enable the battery power switch. See section 12.3.2, VBATT Battery Power Supply Switch Usage.

When the VBATT low voltage is detected, disable the VBATT low voltage detection as shown in Figure 12.4.

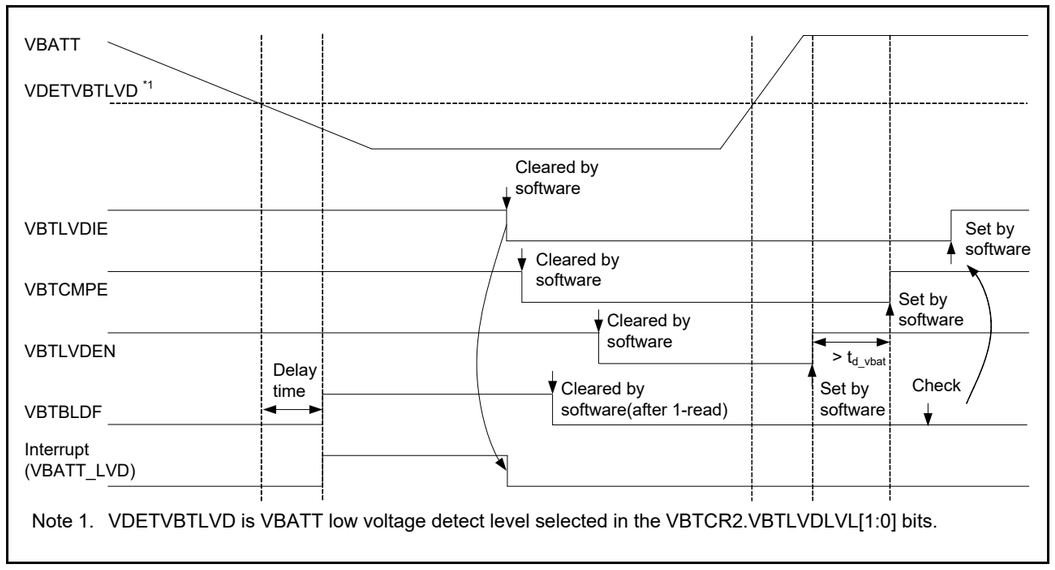


Figure 12.4 Basic operation of VBATT low voltage detection interrupt

The following procedures show how to unset the VBATT pin low voltage detection:

1. Make sure that the VBTSR.VBTRVLD bit is 1.
2. Set the VBTLVDICR.VBTLVDIE bit to 0 to disable voltage detect interrupt.
3. Set the VBTCMPCR.VBTCMPE bit to 0 for VBATT pin voltage detect circuit output to disable.
4. Set the VBTCR2.VBTLVDEN bit to 0 to disable VBATT pin low voltage output to disable.
5. Modify the setting of bits related to the VBATT pin low voltage detection registers other than

12.3.3 VBATT引脚低电压检测程序

VBTSR.VBTBLDF标志和中断可用于监控VBATT引脚低电压检测，使用本节中描述的程序。

以下程序显示如何启用VBATT引脚低电压检测：

1. 设置电压监视器0复位。请参见第8节，低电压检测(LVD)。
2. 如果对该位的访问是上电复位后的第一次访问，则将VBTCR1.BPWSWSTP位设置为1。
3. 等待VBTSR.VBTRVLD位为1，并确保VBTCR2.VBTLVDEN、VBTLVDICR.VBTLVDIE和VBTCMPCR.VBTCMPE位为0。
4. 在VBTCR2.VBTLVDLVL[1:0]位（VBATT引脚电压检测电平选择）中指定检测电压。
5. 在VBTLVDICR.VBTLVDISEL位中选择中断类型。
6. 将VBTCR2.VBTLVDEN位设置为1以启用VBATT引脚低电压检测。
7. 在等待VBATT比较器操作稳定时间(td_vbat)后，如第48节所述，电气特性，将VBTCMPCR.VBTCMPE位设置为1以启用VBATT引脚电压检测电路。
8. 确保VBTSR.VBTBLDF标志为0，然后将VBTLVDICR.VBTLVDIE位设置为1 VBATT引脚低电压检测中断输出被使能。
9. 将VBTCR1.BPWSWSTP位清0以使能电池电源开关。请参阅第12.3.2节，VBATT电池电源开关使用。

当检测到VBATT低电压时，禁用VBATT低电压检测，如图12.4所示。

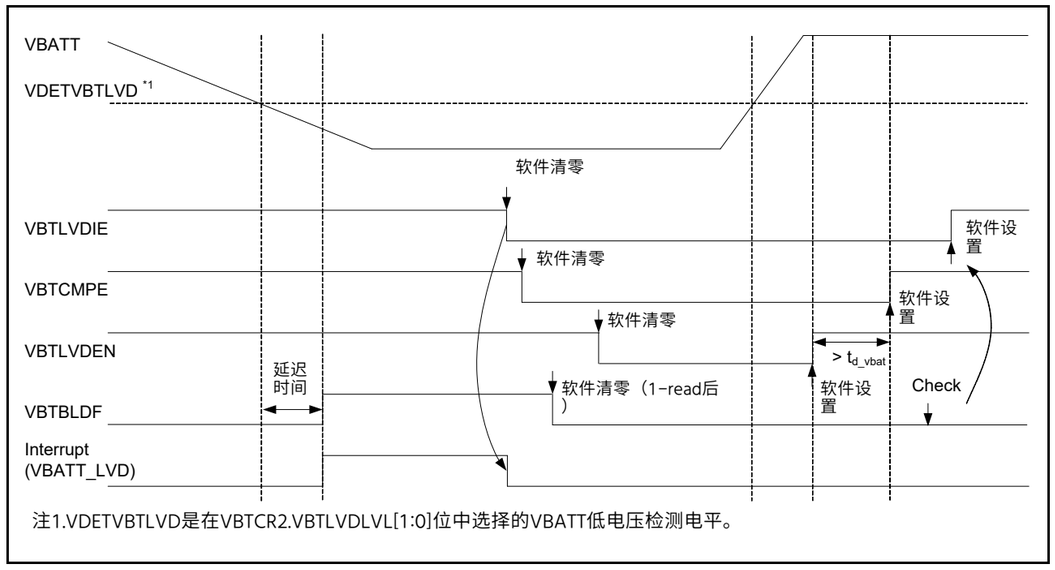


Figure 12.4 VBATT低电压检测中断的基本操作

以下程序显示如何取消设置VBATT引脚低电压检测：

1. 确保VBTSR.VBTRVLD位为1。
2. 将VBTLVDICR.VBTLVDIE位设置为0以禁用电压检测中断。
3. 将VBTCMPCR.VBTCMPE位设置为0以禁用VBATT引脚电压检测电路输出。
4. 将VBTCR2.VBTLVDEN位设置为0以禁用VBATT引脚低电压输出以禁用。
5. 修改VBATT引脚低电压检测寄存器相关位的设置

VBTCR2.VBTLVDEN, VBTCMPCR.VBTCMPE, and VBTLVDICR.VBTLVDIE.

12.3.4 VBATT Backup Register Usage

The VBATT backup register VBTBKRn where n = 0 to 511, can be used to store or restore data as the following procedure describes:

1. The VBTCR1.BPWSWSTP bit must be set to 1 if the access to this bit is for the first access after a power-on reset.
2. Wait for the VBTSR.VBTRVLD bit to be 1.
3. VBTBKRn where n = 0 to 511 can be accessed by an 8-bit read or write operation.
4. Clear the VBTCR1.BPWSWSTP bit to 0 to enable the battery power switch. See section 12.3.2, VBATT Battery Power Supply Switch Usage.

12.3.5 VBATT Wakeup Control Function Usage

The wakeup control function is a function that can toggle the output pin VBATWIO0 when the RTC alarm/periodic signal is asserted when VBATT_R is powered by the VBATT pin.

Note: The toggle that is triggered by the wakeup control function does not generate an interrupt at the ICU or a reset at the reset module.

The following procedures show how to set the registers after the MCU starts up as from a low voltage monitor 0 reset (LVD0) by the VBATT wakeup trigger.

1. Set the VBTCR1.BPWSWSTP bit to 1.
2. Wait for the VBTSR.VBTRVLD bit to be 1 and be sure that the VBTSR.VBTRDF bit is 0.
3. Check the VBATT wakeup trigger source by reading the VBTWFR register. In the example of Figure 12.5, the VBTWFR.VRTCIF bit is set to 1.
4. Clear the corresponding bit in the VBTWFR register to 0, then the toggle output is started on the VBATWIO0 port. In the example of Figure 12.5, it is toggled from high to low on the VBATWIO0 port.
5. Set the I/O registers for the power supply stop control signal to output 0 or 1 to the external power management IC as needed.
6. In case you want to repeat the VBATT wakeup operation, clear the VBTCR1.BPWSWSTP bit to 0 and set the I/O registers for the power supply stop control signal to output 0 or 1 to the external power management IC so as to request stopping the power supply again.
   In case you want to change the wakeup trigger conditions, clear the VBTWCTLR.VWEN bit to 0, and clear the all bit in the VBTWTER register before setting other registers associated with VBATT.

VBTCR2.VBTLVDEN, VBTCMPCR.VBTCMPE, and VBTLVDICR.VBTLVDIE.

12.3.4 VBATT备份寄存器使用

VBATT备份寄存器VBTBKRn，其中n=0到511，可用于存储或恢复数据，过程如下所述：

1. 如果对该位的访问是上电复位后的第一次访问，则必须将VBTCR1.BPWSWSTP位设置为1。
2. 等待VBTSR.VBTRVLD位为1。
3. VBTBKRn其中n=0到511可以通过8位读取或写入操作访问。
4. 将VBTCR1.BPWSWSTP位清0以使能电池电源开关。请参阅第12.3.2节，VBATT电池电源开关使用。

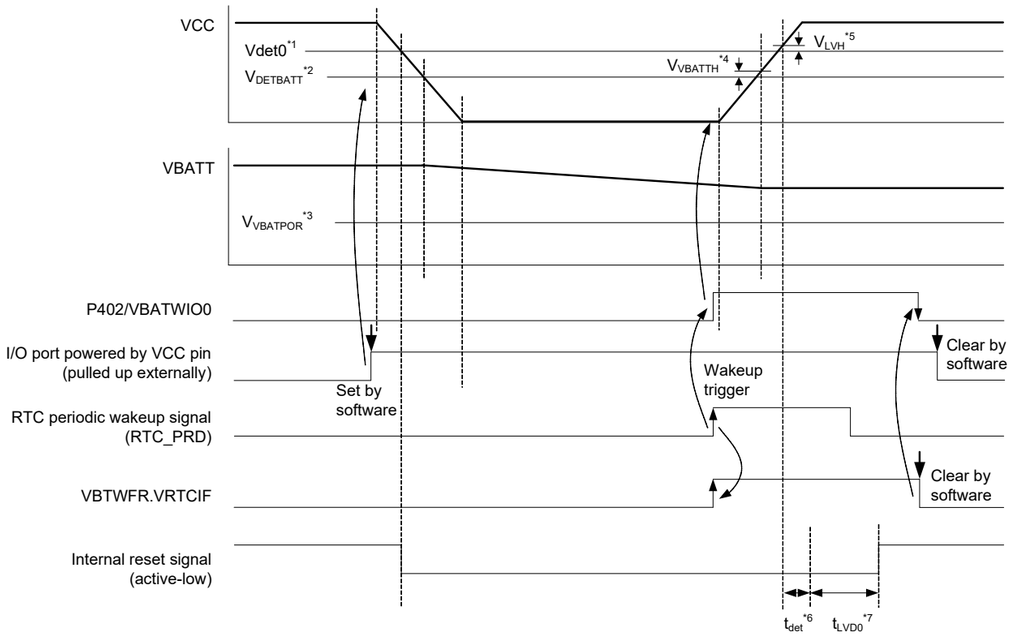
12.3.5 VBATT唤醒控制功能使用

唤醒控制功能是当VBATT_R由VBATT引脚供电时，当RTC闹钟周期信号有效时，可以切换输出引脚VBATWIO0的功能。

Note: 由唤醒控制功能触发的切换不会在ICU产生中断或在复位模块产生复位。

以下过程显示了如何在MCU从低压监视器0复位(LVD0)启动后通过VBATT唤醒触发器设置寄存器。

1. 将VBTCR1.BPWSWSTP位设置为1。
2. 等待VBTSR.VBTRVLD位为1，并确保VBTSR.VBTRDF位为0。
3. 通过读取VBTWFR寄存器检查VBATT唤醒触发源。在图12.5的示例中，VBTWFR.VRTCIF位设置为1。
4. 将VBTWFR寄存器中的相应位清零，然后在VBATWIO0端口上启动切换输出。在图12.5的示例中，它在VBATWIO0端口上从高电平切换到低电平。
5. 根据需要将电源停止控制信号的IO寄存器设置为输出0或1到外部电源管理IC。
6. 如果要重复VBATT唤醒操作，请将VBTCR1.BPWSWSTP位清0，并将电源停止控制信号的IO寄存器设置为向外部电源管理IC输出0或1以请求停止电源再次。如果要更改唤醒触发条件，请将VBTWCTLR.VWEN位清除为0，并在设置与VBATT相关的其他寄存器之前清除VBTWTER寄存器中的所有位。

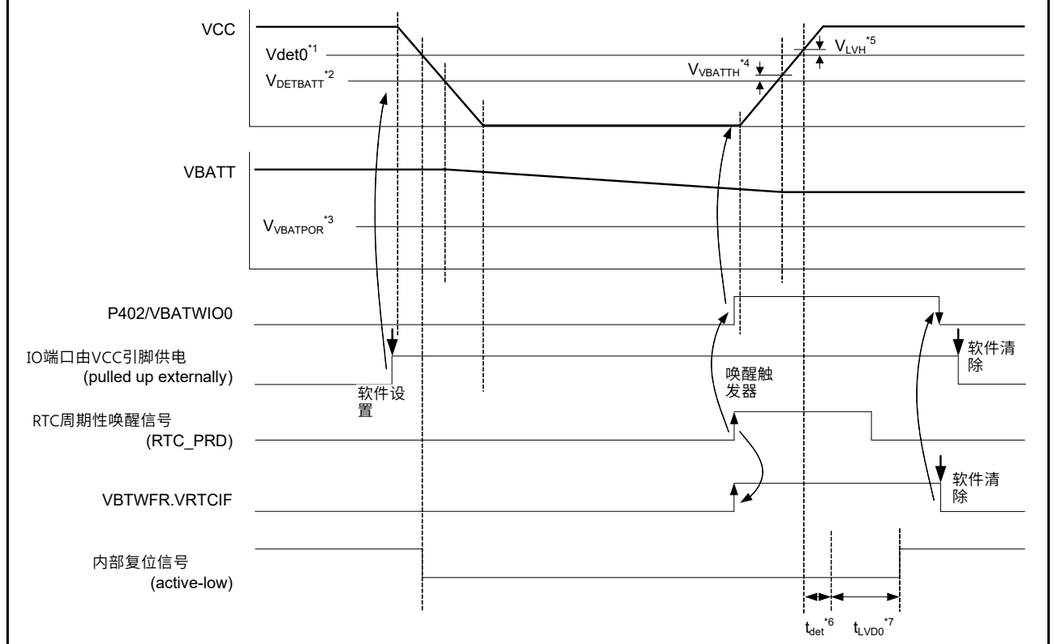


Note 1. V_{det0} is LVD0 voltage detection level selected in the OFS1.VDSEL1[2:0] bits.
Note 2. $V_{DETBATT}$ is voltage level for switching to battery backup.
Note 3. $V_{VBATPOR}$ is voltage detection level VBATT power-on reset (VBAT_POR).
Note 4. V_{VBATTH} is hysteresis width for switching to battery backup.
Note 5. V_{LVH} is hysteresis width of LVD0.
Note 6. t_{det} is response delay time of LVD0.
Note 7. t_{LVD0} is wait time after LVD0 reset cancellation.

Figure 12.5 Timing diagram of VBATT wakeup function

12.4 Usage Notes

1. When the VBATT pin is not in use, connect the VBATT pin to the VCC pin.
2. When the voltage level on VBATT is lower than the guaranteed operation range, operation of the sub-clock oscillator and RTC cannot be guaranteed. This voltage drop can be verified in the VBTSR register.
3. If a reset is generated while writing to the registers described in this section, the register values might be lost.
4. During RTC operation powered by the VBATT pin, RTC supports the calendar/binary count operation, the alarm/periodic trigger for the VBATT wakeup function, and the time capture function.
5. The VBATT wakeup control function can be used when VBATT_R is powered by VBATT pin only.
6. The voltage level on the I/O ports powered by VCC pin transits to high-impedance when the power supply is stopped. If these ports are used as the power supply stop control pins for VBATT wakeup function, these ports should be pulled up or pulled down externally.



注1.Vdet0是在OFS1.VDSEL1[2:0]位中选择的LVD0电压检测电平。
注2.VDETBATT是切换到备用电池的电压电平。
注3.VVBATPOR是电压检测电平VBATT上电复位(VBAT_POR)。
注4.VVBATTH是切换到备用电池的滞后宽度。
注5.VLVH是LVD0的迟滞宽度。
注6.tdet为LVD0的响应延迟时间。
注7.tLVD0是LVD0复位取消后的等待时间。

Figure 12.5 VBATT唤醒功能时序图

12.4 使用说明

1. 当VBATT引脚不使用时，将VBATT引脚连接到VCC引脚。
2. 当VBATT上的电压电平低于保证工作范围时，不能保证子时钟振荡器和RTC的工作。该电压降可以在VBTSR寄存器中验证。
3. 如果在写入本节所述的寄存器时产生复位，则寄存器值可能会丢失。
4. 在由VBATT引脚供电的RTC操作期间，RTC支持日历二进制计数操作、VBATT唤醒功能的闹钟周期触发和时间捕捉功能。
5. 当VBATT_R仅由VBATT引脚供电时，可以使用VBATT唤醒控制功能。
6. 当电源停止时，由VCC引脚供电的IO端口上的电压电平变为高阻态。如果这些端口用作VBATT唤醒功能的电源停止控制引脚，这些端口应从外部上拉或下拉。

13. Register Write Protection

13.1 Overview

The register write protection function protects important registers from being overwritten because of software errors. The registers to be protected are set with the Protect Register (PRCR). Table 13.1 lists the association between the PRCR bits and the registers to be protected.

Table 13.1 Association between PRCR bits and registers to be protected

PRCR bit	Registers to be protected
PRC0	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCR, PLLCCR2, BCKCR, MEMWAIT, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, USBCKCR
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR, SNZREQCR, FLSTOP, PSMCR, OPCCR, SOPCCR, SYOCDCR • Registers related to the battery backup function: VBTCR1, VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTICTLR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR, VBTBKRn (n = 0 to 511), BKRACR
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVCMPCR, LVDLVLR, LVD1CR0

13.2 Register Descriptions

13.2.1 Protect Register (PRCR)

Address(es): SYSTEM.PRCR 4001 E3FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit: 0: Disable writes 1: Enable writes.	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to the low power modes and the battery backup function: 0: Disable writes 1: Enable writes.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD: 0: Disable writes 1: Enable writes.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control write access to the PRCR register. To modify the PRCR register, write A5h to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W*1

Note 1. Write data is not saved. Always reads 00h.

PRCn bits (Protect Bit n) (n = 0, 1, 3)

The PRCn bits enable or disable writing to the protected registers listed in Table 13.1. Setting the PRCn bits to 1 or 0 enables or disables writing, respectively.

13. 寄存器写保护

13.1 Overview

寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。表13.1列出了PRCR位与要保护的寄存器之间的关联。

Table 13.1 PRCR位和要保护的寄存器之间的关联

PRCR bit	受保护的寄存器
PRC0	与时钟产生电路相关的寄存器： SCKDIVCR, SCKSCR, PLLCR, PLLCCR2, BCKCR, MEMWAIT, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, USBCKCR
PRC1	与低功耗模式相关的寄存器： SBYCR、SNZCR、SNZEDCR、SNZREQCR、FLSTOP、PSMCR、OPCCR、SOPCCR、SYOCDCR 与电池备份功能相关的寄存器： VBTCR1, VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTICTLR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR, VBTBKRn (n = 0 to 511), BKRACR
PRC3	与LVD相关的寄存器： LVD1CR1, LVD1SR, LVCMPCR, LVDLVLR, LVD1CR0

13.2 注册说明

13.2.1 保护寄存器(PRCR)

Address(es): SYSTEM.PRCR 4001 E3FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Function	R/W
b0	PRC0	保护位0	允许写入与时钟生成电路相关的寄存器：0：禁止写入1：允许写入。	R/W
b1	PRC1	保护位1	允许写入与低功耗模式和电池备份功能相关的寄存器：0：禁止写入1：允许写入。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	PRC3	保护位3	允许写入与LVD相关的寄存器：0：禁止写入1：允许写入。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	PRKEY[7:0]	中华人民共和国密钥代码	这些位控制对PRCR寄存器的写访问。要修改PRCR寄存器，以16位为单位，将A5h写入高8位，将目标值写入低8位。	W*1

Note 1. 不保存写入数据。始终读取00h。

PRCn位（保护位n）（n=0、1、3）

PRCn位启用或禁用对表13.1中列出的受保护寄存器的写入。将PRCn位设置为1或0分别启用或禁用写入。

14. Interrupt Controller Unit (ICU)

14.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC, DTC, and DMAC modules. The ICU also controls non-maskable interrupts. Table 14.1 lists the ICU specifications. Figure 14.1 shows a block diagram of the ICU, and Table 14.2 lists the I/O pins.

Table 14.1 ICU specifications

Parameter		Description
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 209
	External pin interrupts	• Interrupt detection on low level*4, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter function supported • 11 sources, with interrupts from IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11, IRQ14, IRQ15 pins.
	DTC/DMAC control	The DTC and DMAC can be activated by interrupt sources*1
	Interrupt sources for NVIC	• 32 sources
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported.
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillation has stopped
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Voltage monitor 1 interrupt*3	Voltage monitor interrupt of low voltage detection detector 1 (LVD_LVD1)
	VBATT interrupt	Voltage monitor interrupt of VBATT monitor
	RPEST	Interrupt on SRAM parity error
	RECCST	Interrupt on SRAM ECC error
	BUSSST	Interrupt on MPU bus slave error
	BUSMST	Interrupt on MPU bus master error
	SPEST	Interrupt on CPU stack pointer monitor
Return from low power mode		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source. • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register • Snooze mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SELSR0 and WUPEN registers. See section 14.2.8, SYS Event Link Setting Register (SELSR0) and section 14.2.9, Wake Up Interrupt Enable Register (WUPEN).

Note 1. For the DTC and DMAC activation sources, see Table 14.4, Event table.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as event signals. When used as interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1, set the LVD1CR1.IRQSEL bit to 1. To enable the VBATT monitor interrupt, set the VBTLVDICR.VBTLVDISEL bit to 1.
Note 4. Low level: interrupt detection is not canceled if you do not clear it after a detection.

14. 中断控制器单元(ICU)

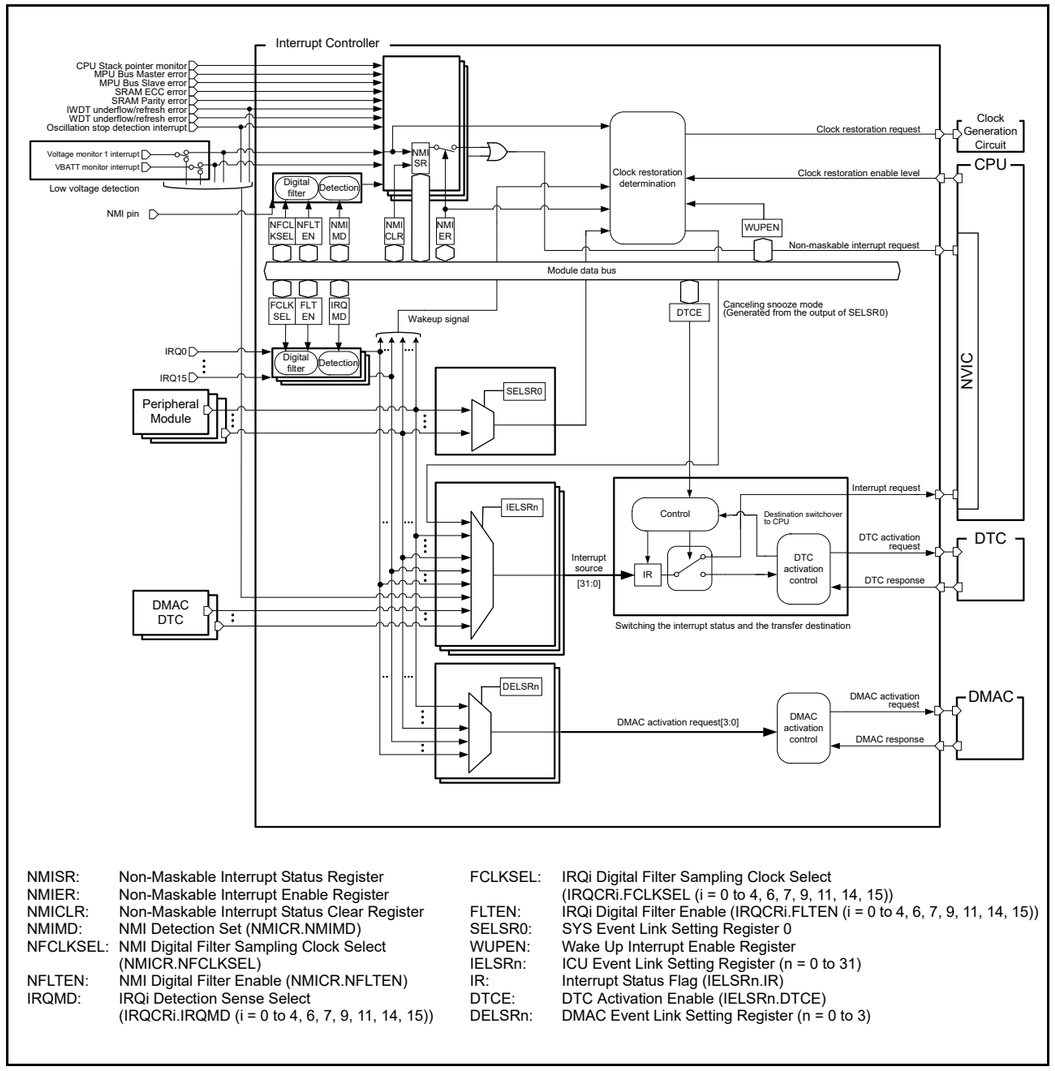
14.1 Overview

中断控制器单元(ICU)控制哪些事件信号链接到NVIC、DTC和DMAC模块。
ICU还控制不可屏蔽的中断。表14.1列出了ICU规格。图14.1显示了ICU的框图，表14.2列出了IO引脚。

Table 14.1 ICU规格

Parameter		Description
Interrupts	外设功能中断	来自外围模块的中断源数：209
	外部引脚中断	低电平中断检测*4、下降沿、上升沿、上升沿和下降沿可以为每个源设置这些检测方法之一。 支持数字滤波器功能 11个源，中断从IRQ0到IRQ4、IRQ6、IRQ7、IRQ9、IRQ11、IRQ14、IRQ15引脚。
	DTC/DMAC control	DTC和DMAC可由中断源激活*1
	NVIC的中断源	• 32 sources
Non-maskable interrupts*2	NMI引脚中断	来自NMI引脚的中断 下降沿或上升沿中断检测 支持数字滤波器功能。
	振荡停止检测中断*3	检测到主振荡停止时中断
	WDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	IWDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	电压监视器1中断*3	低电压检测检测器1(LVD_LVD1)的电压监控中断
	VBATT interrupt	VBATT监视器的电压监视器中断
	RPEST	SRAM奇偶校验错误中断
	RECCST	SRAMECC错误中断
	BUSSST	MPU总线从机错误中断
	BUSMST	MPU总线主机错误中断
	SPEST	CPU堆栈指针监视器中断
从低功耗模式返回		睡眠模式：返回由不可屏蔽中断或任何其他中断源启动。 软件待机模式：返回由不可屏蔽的中断启动。可以在WUPEN寄存器中选择中断 贪睡模式：返回由不可屏蔽的中断启动。 可以在SELSR0和WUPEN寄存器中选择中断。 请参见第14.2.8节，SYS事件链接设置寄存器(SELSR0)和第14.2.9节，唤醒中断启用寄存器(WUPEN)。

Note 1. 对于DTC和DMAC激活源，请参见表14.4，事件表。
Note 2. 不可屏蔽中断只能在复位释放后启用一次。
Note 3. 这些不可屏蔽的中断也可以用作事件信号。当用作中断时，不要从复位状态改变NMIER寄存器的值。要启用电压监视器1，请将LVD1CR1.IRQSEL位设置为1。要启用VBATT监视器中断，请将VBTLVDICR.VBTLVDISEL位设置为1。
Note 4. 低电平：检测后不清除中断检测不取消。



NMISR: Non-Maskable Interrupt Status Register
NMIER: Non-Maskable Interrupt Enable Register
NMICLR: Non-Maskable Interrupt Status Clear Register
NMIMD: NMI Detection Set (NMICR.NMIMD)
NFCLKSEL: NMI Digital Filter Sampling Clock Select (NMICR.NFCLKSEL)
NFLTEN: NMI Digital Filter Enable (NMICR.NFLTEN)
IRQMD: IRQi Detection Sense Select (IRQCRi.IRQMD (i = 0 to 4, 6, 7, 9, 11, 14, 15))

FCLKSEL: IRQi Digital Filter Sampling Clock Select (IRQCRi.FCLKSEL (i = 0 to 4, 6, 7, 9, 11, 14, 15))
FLTEN: IRQi Digital Filter Enable (IRQCRi.FLTEN (i = 0 to 4, 6, 7, 9, 11, 14, 15))
SELSR0: SYS Event Link Setting Register 0
WUPEN: Wake Up Interrupt Enable Register
IELSRn: ICU Event Link Setting Register (n = 0 to 31)
IR: Interrupt Status Flag (IELSRn.IR)
DTCE: DTC Activation Enable (IELSRn.DTCE)
DELSRn: DMAC Event Link Setting Register (n = 0 to 3)

Figure 14.1 ICU block diagram

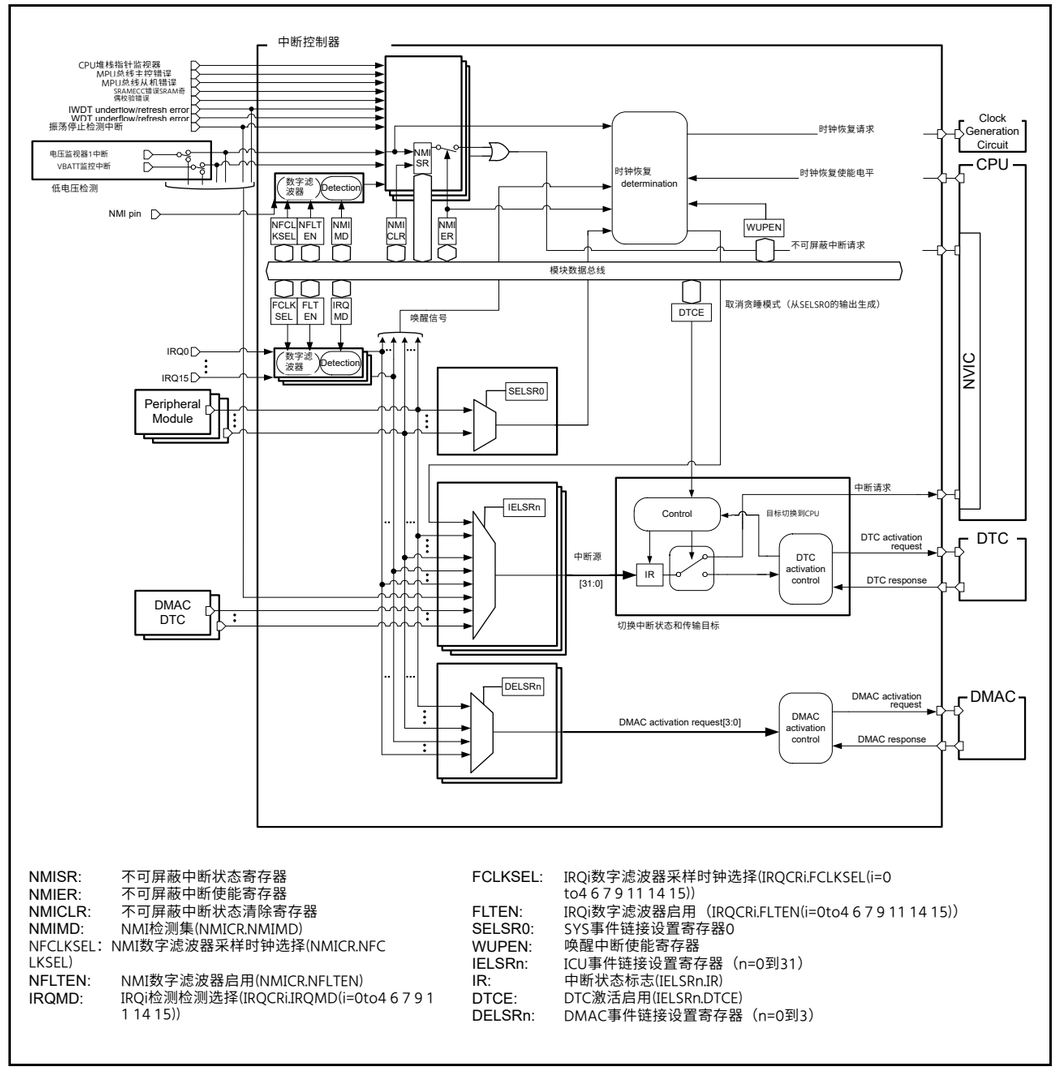
Table 14.2 lists the ICU input/output pins.

Table 14.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11, IRQ14, IRQ15	Input	External interrupt request pins

14.2 Register Descriptions

This chapter does not describe Arm® NVIC internal registers. For information on these registers, see the *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).



NMISR: 不可屏蔽中断状态寄存器
NMIER: 不可屏蔽中断使能寄存器
NMICLR: 不可屏蔽中断状态清除寄存器
NMIMD: NMI检测集(NMICR.NMIMD)
NFCLKSEL：NMI数字滤波器采样时钟选择(NMICR.NFCLKSEL)
NFLTEN: NMI数字滤波器启用(NMICR.NFLTEN)
IRQMD: IRQi检测检测选择(IRQCRi.IRQMD(i=0to4 6 7 9 11 14 15))

FCLKSEL: IRQi数字滤波器采样时钟选择(IRQCRi.FCLKSEL(i=0 to4 6 7 9 11 14 15))
FLTEN: IRQi数字滤波器启用（IRQCRi.FLTEN(i=0to4 6 7 9 11 14 15))
SELSR0: SYS事件链接设置寄存器0
WUPEN: 唤醒中断使能寄存器
IELSRn: ICU事件链接设置寄存器（n=0到31）
IR: 中断状态标志(IELSRn.IR)
DTCE: DTC激活启用(IELSRn.DTCE)
DELSRn: DMAC事件链接设置寄存器（n=0到3）

Figure 14.1 ICU框图

表14.2列出了ICU输入输出引脚。

Table 14.2 ICUIO引脚

引脚名称	I/O	Description
NMI	Input	不可屏蔽中断请求引脚
IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11, IRQ14, IRQ15	Input	外部中断请求引脚

14.2 注册说明

本章不介绍Arm®NVIC内部寄存器。有关这些寄存器的信息，请参阅ARM®Cortex®M4处理器技术参考手册(ARMDDI0439D)。

14.2.1 IRQ Control Register i (IRQCRi) (i = 0 to 4, 6, 7, 9, 11, 14, 15)

Address(es): ICU.IRQCR0 4000 6000h, ICU.IRQCR1 4000 6001h, ICU.IRQCR2 4000 6002h, ICU.IRQCR3 4000 6003h, ICU.IRQCR4 4000 6004h, ICU.IRQCR6 4000 6006h, ICU.IRQCR7 4000 6007h, ICU.IRQCR9 4000 6009h, ICU.IRQCR11 4000 600Bh, ICU.IRQCR14 4000 600Eh, ICU.IRQCR15 4000 600Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	IRQMD[1:0]	IRQi Detection Sense Select	b1 b0 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	FLTEN	IRQi Digital Filter Enable	0: Digital filter disabled 1: Digital filter enabled.	R/W

IRQCRi register changes must satisfy the following:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register setting before setting the target IELSRn (n = 0 to 31).
  You can change the register values only when the IELSRn.IELS[7:0] bits are 00h.
- For a DMAC trigger:
  Change the IRQCRi register setting before setting the target DELSRn (n = 0 to 3).
  You can change the register values only when the DELSRn.DELS[7:0] bits are 00h.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN.IRQWUPEN[n] (n = 0 to 4, 6, 7, 9, 11, 14, 15).
  You can change the register values only when the target WUPEN.IRQWUPENn is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the external pin interrupt sources IRQi. For more information on the settings, see section 14.4.4, External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the external pin interrupt request IRQi, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For the digital filter details, see section 14.4.3, Digital Filter.

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the external pin interrupt sources IRQi. The filter is enabled when the

14.2.1 IRQ控制寄存器i(IRQCRi)(i=0到4 6 7 9 11 14 15)

Address(es): ICU.IRQCR0 4000 6000h, ICU.IRQCR1 4000 6001h, ICU.IRQCR2 4000 6002h, ICU.IRQCR3 4000 6003h, ICU.IRQCR4 4000 6004h, ICU.IRQCR6 4000 6006h, ICU.IRQCR7 4000 6007h, ICU.IRQCR9 4000 6009h, ICU.IRQCR11 4000 600Bh, ICU.IRQCR14 4000 600Eh, ICU.IRQCR15 4000 600Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	IRQMD[1:0]	IRQi检测检测选择	b1 b0 0 0：下降沿 0 1：上升沿 1 0：上升沿和下降沿 1 1：低电平。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	FCLKSEL[1:0]	IRQi数字滤波器采样时钟 Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	FLTEN	IRQi数字滤波器启用	0：禁用数字滤波器1 ：启用数字滤波器。	R/W

IRQCRi寄存器更改必须满足以下条件：

- 对于CPU中断或DTC触发器：
  在设置目标IELSRn（n=0到31）之前更改IRQCRi寄存器设置。仅当IELSRn.IELS[7:0]位为00h时才能更改寄存器值。
- For a DMAC trigger:
  在设置目标DELSRn（n=0到3）之前更改IRQCRi寄存器设置。
  只有当DELSRn.DELS[7:0]位为00h时，您才能更改寄存器值。
- 对于唤醒使能信号：
  在设置目标WUPEN.IRQWUPEN[n]（n=0到4、6、7、9、11、14、15）之前更改IRQCRi寄存器设置。只有当目标WUPEN.IRQWUPENn为0时，您才能更改寄存器值。

IRQMD[1:0]位（IRQi检测检测选择）

IRQMD[1:0]位设置外部引脚中断源IRQi的检测检测方法。有关设置的更多信息，请参见第14.4.4节，外部引脚中断。

FCLKSEL[1:0]位（IRQi数字滤波器采样时钟选择）

FCLKSEL[1:0]位为外部引脚中断请求IRQi选择数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

有关数字滤波器的详细信息，请参阅第14.4.3节，数字滤波器。

FLTEN位（IRQi数字滤波器使能）

FLTEN位使能用于外部引脚中断源IRQi的数字滤波器。过滤器启用时

IRQCRi.FLTEN bit is 1, and disabled when the IRQCRi.FLTEN bit is 0. The IRQi pin level is sampled at the cycle specified in IRQCRi.FCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For the digital filter details, see section 14.4.3, Digital Filter.

14.2.2 Non-Maskable Interrupt Status Register (NMISR)

Address(es): ICU.NMISR 4000 6140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEST	BUSMST	BUSSST	RECCST	RPEST	NMIST	OSTST	—	VBATTST	—	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b1	WDTST	WDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b3	—	Reserved	This bit is read as 0.	R
b4	VBATTST	VBATT monitor Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b5	—	Reserved	This bit is read as 0.	R
b6	OSTST	Oscillation Stop Detection Interrupt Status Flag	0: Interrupt not requested for main oscillation stop 1: Interrupt requested for main oscillation stop.	R
b7	NMIST	NMI Status Flag	0: NMI pin interrupt not requested. 1: NMI pin interrupt requested.	R
b8	RPEST	SRAM Parity Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b9	RECCST	SRAM ECC Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b10	BUSSST	MPU Bus Slave Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b11	BUSMST	MPU Bus Master Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b12	SPEST	CPU Stack Pointer Monitor Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests have occurred during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

This flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

- When an IWDT underflow/refresh error interrupt occurs and this interrupt is enabled.

[Clearing condition]

- When 1 is written to the NMICLR.IWDTCLR bit.

IRQCRi.FLTEN位为1，当IRQCRi.FLTEN位为0时禁用。IRQi引脚电平在IRQCRi.FCLKSEL[1:0]中指定的周期采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息，请参阅第14.4.3节，数字滤波器。

14.2.2 不可屏蔽中断状态寄存器(NMISR)

Address(es): ICU.NMISR 4000 6140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEST	BUSMST	BUSSST	RECCST	RPEST	NMIST	OSTST	—	VBATTST	—	LVD1ST	WDTST	IWDTST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IWDTST	IWDT下溢刷新错误状态标志	0：未请求中断1：请求中断。	R
b1	WDTST	WDT下溢刷新错误状态标志	0：未请求中断1：请求中断。	R
b2	LVD1ST	电压监视器1中断状态标志	0：未请求中断1：请求中断。	R
b3	—	Reserved	该位读为0。	R
b4	VBATTST	VBATT监控中断状态标志	0：未请求中断1：请求中断。	R
b5	—	Reserved	该位读为0。	R
b6	OSTST	振荡停止检测中断状态Flag	0：主振荡停止时不请求中断1：主振荡停止时请求中断。	R
b7	NMIST	NMI状态标志	0：未请求NMI引脚中断。1：请求NMI引脚中断。	R
b8	RPEST	SRAM奇偶校验错误中断状态标志	0：未请求中断1：请求中断。	R
b9	RECCST	SRAMECC错误中断状态标志	0：未请求中断1：请求中断。	R
b10	BUSSST	MPU总线从机错误中断状态标志	0：未请求中断1：请求中断。	R
b11	BUSMST	MPU总线主机错误中断状态标志	0：未请求中断1：请求中断。	R
b12	SPEST	CPU堆栈指针监视器中断状态Flag	0：未请求中断1：请求中断。	R
b15 to b13	—	Reserved	这些位读为0。	R

NMISR寄存器监视不可屏蔽中断源的状态。忽略对NMISR寄存器的写入。
不可屏蔽中断使能寄存器(NMIER)中的设置不会影响该寄存器中的状态标志。
在不可屏蔽中断处理程序结束之前，检查该寄存器中的所有位是否都设置为0，以确认在处理程序处理期间没有发生其他NMI请求。

IWDTST标志（IWDT下溢刷新错误状态标志）

该标志指示IWDT下溢刷新错误中断　　请求。它是只读的并由NMICLR.IWDTCLR bit.

[Setting condition]

- 当IWDT下溢刷新错误中断　　发生并且该中断被使能时。

[Clearing condition]

- 当1写入NMICLR.IWDTCLR位时。

WDTST flag (WDT Underflow/Refresh Error Status Flag)

This flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

- When a WDT underflow/refresh error interrupt occurs.

[Clearing condition]

- When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

This flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

- When a voltage monitor 1 interrupt occurs and this interrupt is enabled.

[Clearing condition]

- When 1 is written to the NMICLR.LVD1CLR bit.

VBATTST flag (VBATT monitor Interrupt Status Flag)

This flag indicates a VBATT monitor interrupt request. It is read-only and cleared by the NMICLR.VBATTCLR bit.

[Setting condition]

- When a VBATT monitor interrupt occurs.

[Clearing condition]

- When 1 is written to the NMICLR.VBATTCLR bit.

OSTST flag (Oscillation Stop Detection Interrupt Status Flag)

This flag indicates a main oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

- When an oscillation stop detection interrupt occurs.

[Clearing condition]

- When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Status Flag)

This flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

- When an edge specified by the NMICR.NMIMD bit is input to the NMI pin.

[Clearing condition]

- When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

This flag indicates an SRAM parity error interrupt request.

[Setting condition]

- When an interrupt occurs in response to an SRAM parity error.

[Clearing condition]

- When 1 is written to the NMICLR.RPECLR bit.

WDTST标志（WDT下溢刷新错误状态标志）

该标志指示WDT下溢刷新错误中断　　请求。它是只读的并由NMICLR.WDTCLR bit.

[Setting condition]

- 当WDT下溢刷新错误中断　　发生时。

[Clearing condition]

- 当1写入NMICLR.WDTCLR位时。

LVD1ST标志（电压监视器1中断状态标志）

该标志指示电压监视器1中断请求。它是只读的，由NMICLR.LVD1CLR位清零。

[Setting condition]

- 当电压监视器1中断发生并且该中断被使能时。

[Clearing condition]

- 当1写入NMICLR.LVD1CLR位时。

VBATTST标志（VBATT监控中断状态标志）

该标志指示VBATT监视中断请求。它是只读的并由NMICLR.VBATTCLR位清零。

[Setting condition]

- 当VBATT监视器中断发生时。

[Clearing condition]

- 当1写入NMICLR.VBATTCLR位时。

OSTST标志（振荡停止检测中断状态标志）

该标志表示主振荡停止检测中断请求。它是只读的并由NMICLR.OSTCLR bit.

[Setting condition]

- 发生振荡停止检测中断时。

[Clearing condition]

- 当1写入NMICLR.OSTCLR位时。

NMIST标志（NMI状态标志）

该标志指示NMI引脚中断请求。它是只读的，由NMICLR.NMICLR位清零。

[Setting condition]

- 当NMICR.NMIMD位指定的边沿输入到NMI引脚时。

[Clearing condition]

- 当1写入NMICLR.NMICLR位时。

RPEST标志（SRAM奇偶校验错误中断状态标志）

该标志指示SRAM奇偶校验错误中断请求。

[Setting condition]

- 当响应SRAM奇偶校验错误而发生中断时。

[Clearing condition]

- 当1写入NMICLR.RPECLR位时。

RECCST flag (SRAM ECC Error Interrupt Status Flag)

This flag indicates an SRAM ECC error interrupt request.

[Setting condition]

- When an interrupt occurs in response to an SRAM ECC error.

[Clearing condition]

- When 1 is written to the NMICLR.RECCCLR bit.

BUSSST flag (MPU Bus Slave Error Interrupt Status Flag)

This flag indicates a bus slave error interrupt request.

[Setting condition]

- When an interrupt occurs in response to a bus slave error.

[Clearing condition]

- When 1 is written to the NMICLR.BUSSCLR bit.

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

This flag indicates a bus master error interrupt request.

[Setting condition]

- When an interrupt occurs in response to a bus master error.

[Clearing condition]

- When 1 is written to the NMICLR.BUSMCLR bit.

SPEST flag (CPU Stack Pointer Monitor Interrupt Status Flag)

This flag indicates a CPU stack pointer monitor interrupt request.

[Setting condition]

- When an interrupt occurs in response to a CPU stack pointer monitor.

[Clearing condition]

- When 1 is written to the NMICLR.SPECLR bit.

14.2.3 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): ICU.NMIER 4000 6120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEEN	BUSMEN	BUSSEN	RECCEN	RPEEN	NMIEN	OSTEN	—	VBATTEN	—	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b2	LVD1EN	Voltage monitor 1 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

RECCST标志（SRAMECC错误中断状态标志）

该标志指示SRAMECC错误中断请求。

[Setting condition]

- 当响应SRAMECC错误而发生中断时。

[Clearing condition]

- 当1写入NMICLR.RECCCLR位时。

BUSSST标志（MPU总线从机错误中断状态标志）

该标志指示总线从机错误中断请求。

[Setting condition]

- 当响应总线从机错误而发生中断时。

[Clearing condition]

- 当1写入NMICLR.BUSSCLR位时。

BUSMST标志（MPU总线主机错误中断状态标志）

该标志指示总线主机错误中断请求。

[Setting condition]

- 当响应总线主机错误而发生中断时。

[Clearing condition]

- 当1写入NMICLR.BUSMCLR位时。

SPEST标志（CPU堆栈指针监视器中断状态标志）

该标志指示CPU堆栈指针监视中断请求。

[Setting condition]

- 当响应CPU堆栈指针监视器而发生中断时。

[Clearing condition]

- 当1写入NMICLR.SPECLR位时。

14.2.3 不可屏蔽中断使能寄存器(NMIER)

Address(es): ICU.NMIER 4000 6120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEEN	BUSMEN	BUSSEN	RECCEN	RPEEN	NMIEN	OSTEN	—	VBATTEN	—	LVD1EN	WDTEN	IWDTEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IWDTEN	IWDT下溢刷新错误中断 Enable	0：禁用1 ：启用。	R/(W) *1, *2
b1	WDTEN	WDT下溢刷新错误中断 Enable	0：禁用1 ：启用。	R/(W) *1, *2
b2	LVD1EN	电压监视器1中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b3	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b4	VBATTEN	VBATT monitor Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	OSTEN	Oscillation Stop Detection Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b7	NMIEN	NMI Pin Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b8	RPEEN	SRAM Parity Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b9	RECCEN	SRAM ECC Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b10	BUSSEN	MPU Bus Slave Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b11	BUSMEN	MPU Bus Master Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b12	SPEEN	CPU Stack Pointer Monitor Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupt as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupt as an NMI trigger.

LVD1EN bit (Voltage monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupt as an NMI trigger.

VBATTEN bit (VBATT monitor Interrupt Enable)

The VBATTEN bit enables VBATT monitor interrupt as an NMI trigger.

OSTEN bit (Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM Parity error interrupt as an NMI trigger.

RECCEN bit (SRAM ECC Error Interrupt Enable)

The RECCEN bit enables SRAM ECC error interrupt as an NMI trigger.

BUSSEN bit (MPU Bus Slave Error Interrupt Enable)

The BUSSEN bit enables bus slave error interrupt as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupt as an NMI trigger.

SPEEN bit (CPU Stack Pointer Monitor Interrupt Enable)

The SPEEN bit enables CPU stack pointer monitor interrupt as an NMI trigger.

Bit	Symbol	位名称	Description	R/W
b4	VBATTEN	VBATT监视器中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	OSTEN	振荡停止检测中断 Enable	0：禁用1 ：启用。	R/(W) *1, *2
b7	NMIEN	NMI引脚中断使能	0：禁用1 ：启用。	R/(W) *1
b8	RPEEN	SRAM奇偶校验错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b9	RECCEN	SRAMECC错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b10	BUSSEN	MPU总线从机错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b11	BUSMEN	MPU总线主机错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b12	SPEEN	CPU堆栈指针监视器中断 Enable	0：禁用1 ：启用。	R/(W) *1, *2
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后您只能向该位写入1一次。随后的写访问无效。向该位写入0无效。
Note 2. 当源用作事件信号时，不要向该位写入1。

IWDTEN位（IWDT下溢刷新错误中断　　使能）

IWDTEN位使能IWDT下溢刷新错误中断　　作为NMI触发。

WDTEN位（WDT下溢刷新错误中断　　使能）

WDTEN位使能WDT下溢刷新错误中断　　作为NMI触发。

LVD1EN位（电压监视器1中断使能）

LVD1EN位使能电压监视器1中断作为NMI触发。

VBATTEN位（VBATT监控中断使能）

VBATTEN位使能VBATT监视器中断作为NMI触发。

OSTEN位（振荡停止检测中断使能）

OSTEN位使能主振荡停止检测中断作为NMI触发。

NMIEN位（NMI引脚中断允许）

NMIEN位使能NMI引脚中断作为NMI触发器。

RPEEN位（SRAM奇偶校验错误中断使能）

RPEEN位启用SRAM奇偶校验错误中断作为NMI触发器。

RECCEN位（SRAMECC错误中断使能）

RECCEN位启用SRAMECC错误中断作为NMI触发器。

BUSSEN位（MPU总线从机错误中断使能）

BUSSEN位使能总线从机错误中断作为NMI触发器。

BUSMEN位（MPU总线主机错误中断使能）

BUSMEN位使能总线主机错误中断作为NMI触发器。

SPEEN位（CPU堆栈指针监视器中断使能）

SPEEN位使能CPU堆栈指针监视中断作为NMI触发器。

14.2.4 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): ICU.NMICLR 4000 6130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPECLR	BUSMCLR	BUSSCLR	RECCCLR	RPECLR	NMICLR	OSTCLR	—	VBATTCLR	—	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTCLR	IWDT Clear	0: No effect 1: Clear the NMISR.IWDTST flag.	R/(W)*1
b1	WDTCLR	WDT Clear	0: No effect 1: Clear the NMISR.WDTST flag.	R/(W)*1
b2	LVD1CLR	LVD1 Clear	0: No effect 1: Clear the NMISR.LVD1ST flag.	R/(W)*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	VBATTCLR	VBATT Clear	0: No effect 1: Clear the NMISR.VBATTST flag.	R/(W)*1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	OSTCLR	OST Clear	0: No effect 1: Clear the NMISR.OSTST flag.	R/(W)*1
b7	NMICLR	NMI Clear	0: No effect 1: Clear the NMISR.NMIST flag.	R/(W)*1
b8	RPECLR	SRAM Parity Error Clear	0: No effect 1: Clear the NMISR.RPEST flag.	R/(W)*1
b9	RECCCLR	SRAM ECC Error Clear	0: No effect 1: Clear the NMISR.RECCST flag.	R/(W)*1
b10	BUSSCLR	Bus Slave Error Clear	0: No effect 1: Clear the NMISR.BUSSST flag.	R/(W)*1
b11	BUSMCLR	Bus Master Error Clear	0: No effect 1: Clear the NMISR.BUSMST flag.	R/(W)*1
b12	SPECLR	CPU Stack Pointer Monitor Interrupt Clear	0: No effect. 1: Clear the NMISR.SPEST flag.	R/(W)*1
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. The IWDTCLR bit is read as 0.

WDTCLR bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. The WDTCLR bit is read as 0.

LVD1CLR bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. The LVD1CLR bit is read as 0.

VBATTCLR bit (VBATT Clear)

Writing 1 to the VBATTCLR bit clears the NMISR.VBATTST flag. The VBATTCLR bit is read as 0.

OSTCLR bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. The OSTCLR bit is read as 0.

14.2.4 不可屏蔽中断状态清除寄存器(NMICLR)

Address(es): ICU.NMICLR 4000 6130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPECLR	BUSMCLR	BUSSCLR	RECCCLR	RPECLR	NMICLR	OSTCLR	—	VBATTCLR	—	LVD1CLR	WDTCLR	IWDTCLR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IWDTCLR	IWDT Clear	0：无效1：清除NMISR.IWDTST标志。	R/(W)*1
b1	WDTCLR	WDT Clear	0：无效1：清除NMISR.WDTST标志。	R/(W)*1
b2	LVD1CLR	LVD1 Clear	0：无效1：清除NMISR.LVD1ST标志。	R/(W)*1
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	VBATTCLR	VBATT Clear	0：无效1：清除NMISR.VBATTST标志。	R/(W)*1
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	OSTCLR	原声清除	0：无效1：清除NMISR.OSTST标志。	R/(W)*1
b7	NMICLR	NMI Clear	0：无效1：清除NMISR.NMIST标志。	R/(W)*1
b8	RPECLR	SRAM奇偶校验错误清除	0：无效1：清除NMISR.RPEST标志。	R/(W)*1
b9	RECCCLR	SRAMECC错误清除	0：无效1：清除NMISR.RECCST标志。	R/(W)*1
b10	BUSSCLR	总线从机错误清除	0：无效1：清除NMISR.BUSSST标志。	R/(W)*1
b11	BUSMCLR	总线主机错误清除	0：无效1：清除NMISR.BUSMST标志。	R/(W)*1
b12	SPECLR	CPU堆栈指针监视器中断Clear	0：无效果。1：清除NMISR.SPEST标志。	R/(W)*1
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅向该位写入1。

IWDTCLR位（IWDT清除）

将1写入IWDTCLR位会清除NMISR.IWDTST标志。IWDTCLR位读为0。

WDTCLR位（WDT清除）

将1写入WDTCLR位会清除NMISR.WDTST标志。WDTCLR位读为0。

LVD1CLR位（LVD1清零）

将1写入LVD1CLR位会清除NMISR.LVD1ST标志。LVD1CLR位读为0。

VBATTLR位（VBATT清除）

将1写入VBATTCLR位会清除NMISR.VBATTST标志。VBATTLR位读为0。

OSTCLR位（OST清除）

将1写入OSTCLR位会清除NMISR.OSTST标志。OSTCLR位读为0。

NMICLR bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. The NMICLR bit is read as 0.

RPECLR bit (SRAM Parity Error Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. The RPECLR bit is read as 0.

RECCCLR bit (SRAM ECC Error Clear)

Writing 1 to the RECCCLR bit clears the NMISR.RECCST flag. The RECCCLR bit is read as 0.

BUSSCLR bit (Bus Slave Error Clear)

Writing 1 to the BUSSCLR bit clears the NMISR.BUSSST flag. The BUSSCLR bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMSST flag. The BUSMCLR bit is read as 0.

SPECLR bit (CPU Stack Pointer Monitor Interrupt Clear)

Writing 1 to the SPECLR bit clears the NMISR.SPEST flag. The SPECLR bit is read as 0.

14.2.5 NMI Pin Interrupt Control Register (NMICR)

Address(es): ICU.NMICR 4000 6100h

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Digital filter is disabled 1: Digital filter is enabled.	R/W

Change the NMICR register settings before enabling NMI pin interrupt (before setting NMIER.NMIEN to 1).

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for the NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for the NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For details of the digital filter, see section 14.4.3, Digital Filter.

NMICLR位（NMI清除）

将1写入NMICLR位会清除NMISR.NMIST标志。NMICLR位读为0。

RPECLR位（SRAM奇偶校验错误清除）

将1写入RPECLR位会清除NMISR.RPEST标志。RPECLR位读为0。

RECCCLR位（SRAMECC错误清除）

将1写入RECCCLR位会清除NMISR.RECCST标志。RECCCLR位读为0。

BUSSCLR位（总线从机错误清除）

将1写入BUSSCLR位会清除NMISR.BUSSST标志。BUSSCLR位读为0。

BUSMCLR位（总线主机错误清除）

将1写入BUSMCLR位会清除NMISR.BUSMSST标志。BUSMCLR位读为0。

SPECLR位（CPU堆栈指针监视器中断清除）

将1写入SPECLR位会清除NMISR.SPEST标志。SPECLR位读为0。

14.2.5 NMI引脚中断控制寄存器(NMICR)

Address(es): ICU.NMICR 4000 6100h

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	NMIMD	NMI检测集	0：下降沿1： 上升沿。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟 Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	NFLTEN	NMI数字滤波器启用	0：禁用数字滤波器1： 启用数字滤波器。	R/W

在启用NMI引脚中断之前更改NMICR寄存器设置（在将NMIER.NMIEN设置为1之前）。

NMIMD位（NMI检测集）

NMIMD位选择NMI引脚中断的检测检测方法。

NFCLKSEL[1:0]位（NMI数字滤波器采样时钟选择）

NFCLKSEL[1:0]位选择用于NMI引脚中断的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

有关数字滤波器的详细信息，请参阅第14.4.3节“数字滤波器”。

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1 and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NMIFLTC.NFCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 14.4.3, Digital Filter.

14.2.6 ICU Event Link Setting Register n (IELSRn)

Address(es): ICU.IELSR0 4000 6300h, ICU.IELSR1 4000 6304h, ICU.IELSR2 4000 6308h, ICU.IELSR3 4000 630Ch.....
.....ICU.IELSR28 4000 6370h, ICU.IELSR29 4000 6374h, ICU.IELSR30 4000 6378h, ICU.IELSR31 4000 637Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	IELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	IELS[7:0]	ICU Event Link Select	b7 b0 00000000: Disable interrupts to the associated NVIC/DTC module 00000001 to 11011001: Event signal number to be linked. For details, see Table 14.4.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag	0: No interrupt request occurred 1: An interrupt request occurred.	R/(W)*1
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DTCE	DTC Activation Enable	0: DTC activation is disabled 1: DTC activation is enabled.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword or word access.
Note: The Bluetooth middleware executes processing in response to IELSR31 register. Do not change the setting of IELSR31.
Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQ source used by the NVIC. For details, see Table 14.4, Event table. IELSRn, where n = 0 to 31, corresponds to the NVIC IRQ input source numbers 0 to 31.

IELS[7:0] bits (ICU Event Link Select)

The IELS[7:0] bits link an event signal to the associated NVIC/DTC module.

IR flag (Interrupt Status Flag)

The IR status flag indicates an individual interrupt request from the event specified in IELS[7:0].

[Setting condition]

- When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag. DTCE must be set to 0 before writing 0 to the IR flag.

To clear the IR flag:

1. Negate the input signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.

NFLTEN位（NMI数字滤波器使能）

NFLTEN位使能用于NMI引脚中断的数字滤波器。滤波器在NFLTEN为1时启用，在NFLTEN为0时禁用。NMI引脚电平在NMIFLTC.NFCLKSEL[1:0]中指定的时钟周期进行采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息，请参阅第14.4.3节"数字滤波器"。

14.2.6 ICU事件链接设置寄存器n(IELSRn)

Address(es): ICU.IELSR0 4000 6300h, ICU.IELSR1 4000 6304h, ICU.IELSR2 4000 6308h, ICU.IELSR3 4000 630Ch.....
.....ICU.IELSR28 4000 6370h, ICU.IELSR29 4000 6374h, ICU.IELSR30 4000 6378h, ICU.IELSR31 4000 637Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	IELS[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	IELS[7:0]	ICU事件链接选择	b7b000000000：禁用对相关NVICDTC模块的中断00000001至11011001：要链接的事件信号编号。详见表14.4。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	IR	中断状态标志	0：未发生中断请求1：发生了中断请求。	R/(W)*1
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	DTCE	DTC激活启用	0：禁用DTC激活1：启用DTC激活。	R/W
b31 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 该寄存器需要半字或字访问。
Note: 蓝牙中间件响应IELSR31寄存器执行处理。请勿更改IELSR31的设置。
Note 1. 禁止向IR标志写入1。

IELSRn寄存器选择NVIC使用的IRQ源。有关详细信息，请参阅表14.4，事件表。IELSRn，其中n=0到31，对应于NVICIRQ输入源编号0到31。

IELS[7:0]位（ICU事件链接选择）

IELS[7:0]位将事件信号链接到相关的NVICDTC模块。

IR标志（中断状态标志）

IR状态标志指示来自IELS[7:0]中指定事件的单个中断请求。

[Setting condition]

- 当从相关外设模块或IRQi引脚接收到中断请求时。

[Clearing conditions]

- 当0写入标志时。在将0写入IR标志之前，必须将DTCE设置为0。

清除IR标志：

1. 否定输入信号。
2. 读取访问外设一次并等待目标模块时钟的2个时钟周期。

3. Clear the IR flag by writing 0.

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

- When 1 is written to the DTCE bit.

[Clearing conditions]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete
- When 0 is written to the bit.

14.2.7 DMAC Event Link Setting Register n (DELSRn)

Address(es): ICU.DELSR0 4000 6280h, ICU.DELSR1 4000 6284h, ICU.DELSR2 4000 6288h, ICU.DELSR3 4000 628Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DELS[7:0]	DMAC Event Link Select	b7 b0 00000000: Disable DMA start request to the associated DMAC module is disabled. 00000001 to 11011001: Event signal number to be linked. Other settings are prohibited. For details, see Table 14.4, Event table.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag for DMAC	0: No interrupt request is generated 1: An interrupt request is generated.	R/W*1
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword or word access.
Note 1. Writing 1 to the IR flag is prohibited.

DELS[7:0] bits (DMAC Event Link Select)

The DELS[7:0] bits link an event signal for the DMAC module.

IR flag (Interrupt Status Flag for DMAC)

The IR flag is the status flag of an individual DMA transfer request. This flag corresponds to DELS[7:0] bits of the same register.

[Setting condition]

- The flag is set to 1 when a DMA transfer request is generated from the corresponding peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag
- At the start of the DMA transfer after the DMA transfer request is issued.

3. 通过写入0清除IR标志。

DTCE位（DTC激活使能）

当DTCE位设置为1时，相关事件被选为DTC激活源。

[Setting condition]

- 当1写入DTCE位时。

[Clearing conditions]

- 当指定数量的传输完成时。对于链转移，当最后一次链转移的指定转移次数完成时
- 当0写入该位时。

14.2.7 DMAC事件链接设置寄存器n(DELSRn)

Address(es): ICU.DELSR0 4000 6280h, ICU.DELSR1 4000 6284h, ICU.DELSR2 4000 6288h, ICU.DELSR3 4000 628Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DELS[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DELS[7:0]	DMAC事件链接选择	b7b000000000：禁用对相关DMAC模块的禁用DMA启动请求。00000001至11011001：要链接的事件信号编号。禁止其他设置。详见表14.4，事件表。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	IR	DMAC的中断状态标志	0：不产生中断请求1：产生中断请求。	R/W*1
b31 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 该寄存器需要半字或字访问。
Note 1. 禁止向IR标志写入1。

DELS[7:0]位（DMAC事件链接选择）

DELS[7:0]位链接DMAC模块的事件信号。

IR标志（DMAC的中断状态标志）

IR标志是单个DMA传输请求的状态标志。该标志对应于同一寄存器的DELS[7:0]位。

[Setting condition]

- 当相应外设模块或IRQi引脚产生DMA传输请求时，该标志设置为1。

[Clearing conditions]

- 当0写入标志时
- 在发出DMA传输请求后开始DMA传输。

14.2.8 SYS Event Link Setting Register (SELSR0)

Address(es): ICU.SELSR0 4000 6200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SELS[7:0]	SYS Event Link Select	b7 b0 00000000: Disable event output to the associated low-power mode module 00000001 to 11011001: Event signal number to be linked. Other settings are prohibited. For details, see Table 14.4, Event table.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can only use the events listed in Table 14.4 checked as "Canceling Snooze using SELSR0". Events specified in this register are defined as ICU_SNZCANCEL (017h) in Table 14.4. When 017h is set in IELSRn.IELS, an SELSR0 event interrupt occurs.

14.2.9 Wake Up Interrupt Enable Register (WUPEN)

Address(es): ICU.WUPEN 4000 61A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFSWUPEN	—	RTCPRDWUPEN	RTCALMWUPEN	ACMPLP0WUPEN	—	—	VBATTWUPEN	—	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQWUPEN[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	IRQWUPEN[15:0]	IRQ Interrupt Software Standby Returns Enable	0: Disable Software standby returns by IRQ interrupt 1: Enable Software standby returns by IRQ interrupt.	R/W
b16	IWDTWUPEN	IWDT Interrupt Software Standby Returns Enable	0: Disable Software standby returns by IWDT interrupt 1: Enable Software standby returns by IWDT interrupt.	R/W
b17	KEYWUPEN	Key Interrupt Software Standby Returns Enable	0: Disable Software standby returns by KEY interrupt 1: Enable Software standby returns by KEY interrupt.	R/W
b18	LVD1WUPEN	LVD1 Interrupt Software Standby Returns Enable	0: Disable Software standby returns by LVD1 interrupt 1: Enable Software standby returns by LVD1 interrupt.	R/W
b19	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b20	VBATTWUPEN	VBATT Monitor Interrupt Software Standby Returns Enable	0: Disable Software standby returns by VBATT monitor interrupt disabled 1: Enable Software standby returns by VBATT monitor interrupt.	R/W
b22, b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b23	ACMPLP0WUPEN	ACMPLP0 Interrupt Software Standby Returns Enable	0: Disable Software standby returns by ACMPLP0 interrupt 1: Enable Software standby returns by ACMPLP0 interrupt.	R/W

14.2.8 SYS事件链接设置寄存器(SELSR0)

Address(es): ICU.SELSR0 4000 6200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SELS[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	SELS[7:0]	SYS事件链接选择	b7b000000000：禁用到相关低功耗模式模块的事件输出000 00001至11011001：要链接的事件信号编号。禁止其他设置 。详见表14.4， 事件表。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SELSR0寄存器选择将CPU从贪睡模式唤醒的事件。您只能使用中列出的事件
表14.4选中"使用SELSR0取消贪睡"。该寄存器中指定的事件定义为
ICU_SNZCANCEL(017h)在表14.4中。在IELSRn.IELS中设置017h时，将发生SELSR0事件中断。

14.2.9 唤醒中断使能寄存器(WUPEN)

Address(es): ICU.WUPEN 4000 61A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFSWUPEN	—	RTCPRDWUPEN	RTCALMWUPEN	ACMPLP0WUPEN	—	—	VBATTWUPEN	—	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQWUPEN[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	IRQWUPEN[15:0]	IRQ中断软件待机返回使能	0：禁止通过IRQ中断返回软件待机1：使能通过IRQ中断返回软件待机。	R/W
b16	IWDTWUPEN	IWDT中断软件待机返回使能	0：禁止通过IWDT中断返回软件待机1：使能通过IWDT中断返回软件待机。	R/W
b17	KEYWUPEN	按键中断软件待机返回使能	0：禁止通过KEY中断返回软件待机1：使能通过KEY中断返回软件待机。	R/W
b18	LVD1WUPEN	LVD1中断软件待机返回使能	0：禁止通过LVD1中断返回软件待机1：使能通过LVD1中断返回软件待机。	R/W
b19	—	Reserved	该位读取为0。写入值应为0。	R/W
b20	VBATTWUPEN	VBATT监视器中断软件待机返回Enable	0：禁止通过VBATT监视中断返回软件待机1：使能通过VBATT监视中断返回软件待机。	R/W
b22, b21	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b23	ACMPLP0WUPEN	ACMPLP0 Interrupt软件待机返回Enable	0：禁止通过ACMPLP0中断返回软件待机1：使能通过ACMPLP0中断返回软件待机。	R/W

Bit	Symbol	Bit name	Description	R/W
b24	RTCALMWUPEN	RTC Alarm Interrupt Software Standby Returns Enable	0: Disable Software standby returns by RTC alarm interrupt 1: Enable Software standby returns by RTC alarm interrupt.	R/W
b25	RTCPRDWUPEN	RTC Period Interrupt Software Standby Returns Enable	0: Disable Software standby returns by RTC period interrupt 1: Enable Software standby returns by RTC period interrupt.	R/W
b26	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b27	USBFSWUPEN	USBFS Interrupt Software Standby Returns Enable	0: Disable Software standby returns by USBFS interrupt 1: Enable Software standby returns by USBFS interrupt.	R/W
b28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby Returns Enable	0: Disable Software standby returns by AGT1 underflow interrupt 1: Enable Software standby returns by AGT1 underflow interrupt.	R/W
b29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby Returns Enable	0: Disable Software standby returns by AGT1 compare match A interrupt 1: Enable Software standby returns by AGT1 compare match A interrupt.	R/W
b30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby Returns Enable	0: Disable Software standby returns by AGT1 compare match B interrupt 1: Enable Software standby returns by AGT1 compare match B interrupt.	R/W
b31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby Returns Enable	0: Disable Software standby returns by IIC0 address match interrupt 1: Enable Software standby returns by IIC0 address match interrupt.	R/W

The bits in this register control whether the associated interrupt can wake up the CPU from Software Standby mode.

IRQWUPEN[15:0] bits (IRQ Interrupt Software Standby Returns Enable)

The IRQWUPEN[15:0] bits enable the use of IRQn interrupts to cancel Software Standby mode. Only 0 to 4, 6, 7, 9, 11, 14, 15 bits can be used.

IWDTWUPEN bit (IWDT Interrupt Software Standby Returns Enable)

The IWDTWUPEN bit enables the use of IWDT interrupts to cancel Software Standby mode.

KEYWUPEN bit (Key Interrupt Software Standby Returns Enable)

The KEYWUPEN bit enables the use of Key interrupts to cancel Software Standby mode.

LVD1WUPEN bit (LVD1 Interrupt Software Standby Returns Enable)

The LVD1WUPEN bit enables the use of LVD1 interrupts to cancel Software Standby mode.

VBATTWUPEN bit (VBATT Monitor Interrupt Software Standby Returns Enable)

The VBATTWUPEN bit enables the use of VBATT monitor interrupt to cancel Software Standby mode.

ACMPLP0WUPEN bit (ACMPLP0 Interrupt Software Standby Returns Enable)

The ACMPLP0WUPEN bit enables the use of ACMPLP0 interrupt to cancel Software Standby mode.

RTCALMWUPEN bit (RTC Alarm Interrupt Software Standby Returns Enable)

The RTCALMWUPEN bit enables the use of RTC alarm interrupts to cancel Software Standby mode.

RTCPRDWUPEN bit (RTC Period Interrupt Software Standby Returns Enable)

The RTCPRDWUPEN bit enables the use of RTC period interrupt to cancel Software Standby mode.

Bit	Symbol	位名称	Description	R/W
b24	RTCALMWUPEN	RTC闹钟中断 软件待机返回 Enable	0：禁止通过RTC报警中断返回软件待机1：使能通过RTC报警中断返回软件待机。	R/W
b25	RTCPRDWUPEN	RTC周期中断 软件待机返回 Enable	0：禁止通过RTC周期中断返回软件待机1：使能通过RTC周期中断返回软件待机。	R/W
b26	—	Reserved	该位读取为0。写入值应为0。	R/W
b27	USBFSWUPEN	USBFS中断软件 待机返回启用	0：禁止通过USBFS中断返回软件待机1：使能通过USBFS中断返回软件待机。	R/W
b28	AGT1UDWUPEN	AGT1下溢中断软件待机返回 Enable	0：禁止通过AGT1下溢中断返回软件待机1：使能通过AGT1下溢中断返回软件待机。	R/W
b29	AGT1CAWUPEN	AGT1比较匹配A 中断软件待机 退货启用	0：禁止通过AGT1比较匹配A中断返回软件待机1：启用通过AGT1比较匹配A中断返回软件待机。	R/W
b30	AGT1CBWUPEN	AGT1比较匹配B 中断软件待机 退货启用	0：禁止通过AGT1比较匹配B中断返回软件待机1：启用通过AGT1比较匹配B中断返回软件待机。	R/W
b31	IIC0WUPEN	IIC0地址匹配 中断软件待机 退货启用	0：禁止通过IIC0地址匹配中断返回软件待机1：使能通过IIC0地址匹配中断返回软件待机。	R/W

该寄存器中的位控制相关中断是否可以将CPU从软件待机模式唤醒。

IRQWUPEN[15:0]位（IRQ中断软件待机返回使能）

IRQWUPEN[15:0]位允许使用IRQn中断来取消软件待机模式。只能使用0到4、6、7、9、11、14、15位。

IWDTWUPEN位（IWDT中断软件待机返回使能）

IWDTWUPEN位允许使用IWDT中断来取消软件待机模式。

KEYWUPEN位（按键中断软件待机返回使能）

KEYWUPEN位允许使用按键中断来取消软件待机模式。

LVD1WUPEN位（LVD1中断软件待机返回使能）

LVD1WUPEN位允许使用LVD1中断来取消软件待机模式。

VBATTWUPEN位（VBATT监控中断软件待机返回使能）

VBATTWUPEN位允许使用VBATT监控中断来取消软件待机模式。

ACMPLP0WUPEN位（ACMPLP0中断软件待机返回使能）

ACMPLP0WUPEN位允许使用ACMPLP0中断来取消软件待机模式。

RTCALMWUPEN位（RTC闹钟中断软件待机返回使能）

RTCALMWUPEN位允许使用RTC闹钟中断来取消软件待机模式。

RTCPRDWUPEN位（RTC周期中断软件待机返回使能）

RTCPRDWUPEN位允许使用RTC周期中断来取消软件待机模式。

USBFSWUPEN bit (USBFS Interrupt Software Standby Returns Enable)

The USBFSWUPEN bit enables the use of USBFS interrupt to cancel Software Standby mode.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby Returns Enable)

The AGT1UDWUPEN bit enables the use of AGT1 underflow interrupt to cancel Software Standby mode.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby Returns Enable)

The AGT1CAWUPEN bit enables the use of AGT1 compare match A interrupt to cancel Software Standby mode.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby Returns Enable)

The AGT1CBWUPEN bit enables the use of AGT1 compare match B interrupt to cancel Software Standby mode.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby Returns Enable)

The IIC0WUPEN bit enables the use of IIC0 interrupt to cancel Software Standby mode.

14.3 Vector Table

The ICU detects maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. For information about these registers, see the NVIC chapter of the *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).

14.3.1 Interrupt Vector Table

Table 14.3 describes the interrupt vector table. The interrupt vector addresses conform to the NVIC specifications.

Table 14.3 Interrupt vector table (1 of 2)

Exception number	IRQ number	Vector offset	Source	Description
0	—	000h	Arm	Initial stack pointer
1	—	004h	Arm	Initial program counter (reset vector)
2	—	008h	Arm	Non-Maskable Interrupt (NMI)
3	—	00Ch	Arm	Hard Fault
4	—	010h	Arm	MemManage Fault
5	—	014h	Arm	Bus Fault
6	—	018h	Arm	Usage Fault
7	—	01Ch	Arm	Reserved
8	—	020h	Arm	Reserved
9	—	024h	Arm	Reserved
10	—	028h	Arm	Reserved
11	—	02Ch	Arm	Supervisor Call (SVCall)
12	—	030h	Arm	Debug Monitor
13	—	034h	Arm	Reserved
14	—	038h	Arm	Pendable request for system service (PendableSrvReq)
15	—	03Ch	Arm	System Tick Timer (SysTick)
16	0	040h	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	044h	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	048h	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	04Ch	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	050h	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	054h	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	058h	ICU.IELSR6	Event selected in the ICU.IELSR6 register

USBFSWUPEN位（USBFS中断软件待机返回使能）

USBFSWUPEN位允许使用USBFS中断来取消软件待机模式。

AGT1UDWUPEN位（AGT1下溢中断软件待机返回使能）

AGT1UDWUPEN位允许使用AGT1下溢中断来取消软件待机模式。

AGT1CAWUPEN位（AGT1比较匹配中断软件待机返回使能）

AGT1CAWUPEN位允许使用AGT1比较匹配A中断来取消软件待机模式。

AGT1CBWUPEN位（AGT1比较匹配B中断软件待机返回使能）

AGT1CBWUPEN位允许使用AGT1比较匹配B中断来取消软件待机模式。

IIC0WUPEN位（IIC0地址匹配中断软件待机返回使能）

IIC0WUPEN位允许使用IIC0中断来取消软件待机模式。

14.3 向量表

ICU检测可屏蔽和不可屏蔽中断。中断优先级在ArmNVIC中设置。有关这些寄存器的信息，请参阅ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)的NVIC章节。

14.3.1 中断向量表

表14.3描述了中断向量表。中断向量地址符合NVIC规范。

Table 14.3 中断向量表(1of2)

异常编号	IRQ number	矢量偏移	Source	Description
0	—	000h	Arm	初始堆栈指针
1	—	004h	Arm	初始程序计数器（复位向量）
2	—	008h	Arm	Non-Maskable Interrupt (NMI)
3	—	00Ch	Arm	硬故障
4	—	010h	Arm	MemManage Fault
5	—	014h	Arm	总线故障
6	—	018h	Arm	使用错误
7	—	01Ch	Arm	Reserved
8	—	020h	Arm	Reserved
9	—	024h	Arm	Reserved
10	—	028h	Arm	Reserved
11	—	02Ch	Arm	主管呼叫(SVCall)
12	—	030h	Arm	调试监视器
13	—	034h	Arm	Reserved
14	—	038h	Arm	系统服务的挂起请求(PendableSrvReq)
15	—	03Ch	Arm	系统滴答计时器(SysTick)
16	0	040h	ICU.IELSR0	在ICU.IELSR0寄存器中选择的事件
17	1	044h	ICU.IELSR1	在ICU.IELSR1寄存器中选择的事件
18	2	048h	ICU.IELSR2	在ICU.IELSR2寄存器中选择的事件
19	3	04Ch	ICU.IELSR3	在ICU.IELSR3寄存器中选择的事件
20	4	050h	ICU.IELSR4	在ICU.IELSR4寄存器中选择的事件
21	5	054h	ICU.IELSR5	在ICU.IELSR5寄存器中选择的事件
22	6	058h	ICU.IELSR6	在ICU.IELSR6寄存器中选择的事件

Table 14.3 Interrupt vector table (2 of 2)

Exception number	IRQ number	Vector offset	Source	Description
23	7	05Ch	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	060h	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	064h	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	068h	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	06Ch	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	070h	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	074h	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	078h	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	07Ch	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	080h	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	084h	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	088h	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	08Ch	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	090h	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	094h	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	098h	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	09Ch	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0A0h	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0A4h	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0A8h	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0ACh	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0B0h	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0B4h	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0B8h	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0BCh	ICU.IELSR31	Event selected in the ICU.IELSR31 register

14.3.2 Event Number

The following table lists heading details for Table 14.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Form of interrupt detection (signal)	"Edge" or "level" as the method for detection of the interrupt. "✓" indicates usability as anNMI interrupt.
Connect to NVIC	"✓" indicates the interrupt can be used as a CPU interrupt (IELSRn setting)
Invoke DTC	"✓" indicates the interrupt can be used to request DTC activation (IELSRn setting)
Invoke DMAC	"✓" indicates the interrupt can be used to request DMAC activation (DELSRn setting)
Canceling Snooze mode	"✓" indicates the interrupt can be used to request a return from Snooze mode using SELSR0. Otherwise, "✓" indicates that it can be used directly.
Canceling Software Standby mode	"✓" indicates the interrupt can be used to request a return from Software Standby mode

Table 14.3 中断向量表(2of2)

异常编号	IRQ number	矢量偏移	Source	Description
23	7	05Ch	ICU.IELSR7	在ICU.IELSR7寄存器中选择的事件
24	8	060h	ICU.IELSR8	在ICU.IELSR8寄存器中选择的事件
25	9	064h	ICU.IELSR9	在ICU.IELSR9寄存器中选择的事件
26	10	068h	ICU.IELSR10	在ICU.IELSR10寄存器中选择的事件
27	11	06Ch	ICU.IELSR11	在ICU.IELSR11寄存器中选择的事件
28	12	070h	ICU.IELSR12	在ICU.IELSR12寄存器中选择的事件
29	13	074h	ICU.IELSR13	在ICU.IELSR13寄存器中选择的事件
30	14	078h	ICU.IELSR14	在ICU.IELSR14寄存器中选择的事件
31	15	07Ch	ICU.IELSR15	在ICU.IELSR15寄存器中选择的事件
32	16	080h	ICU.IELSR16	在ICU.IELSR16寄存器中选择的事件
33	17	084h	ICU.IELSR17	在ICU.IELSR17寄存器中选择的事件
34	18	088h	ICU.IELSR18	在ICU.IELSR18寄存器中选择的事件
35	19	08Ch	ICU.IELSR19	在ICU.IELSR19寄存器中选择的事件
36	20	090h	ICU.IELSR20	在ICU.IELSR20寄存器中选择的事件
37	21	094h	ICU.IELSR21	在ICU.IELSR21寄存器中选择的事件
38	22	098h	ICU.IELSR22	在ICU.IELSR22寄存器中选择的事件
39	23	09Ch	ICU.IELSR23	在ICU.IELSR23寄存器中选择的事件
40	24	0A0h	ICU.IELSR24	在ICU.IELSR24寄存器中选择的事件
41	25	0A4h	ICU.IELSR25	在ICU.IELSR25寄存器中选择的事件
42	26	0A8h	ICU.IELSR26	在ICU.IELSR26寄存器中选择的事件
43	27	0ACh	ICU.IELSR27	在ICU.IELSR27寄存器中选择的事件
44	28	0B0h	ICU.IELSR28	在ICU.IELSR28寄存器中选择的事件
45	29	0B4h	ICU.IELSR29	在ICU.IELSR29寄存器中选择的事件
46	30	0B8h	ICU.IELSR30	在ICU.IELSR30寄存器中选择的事件
47	31	0BCh	ICU.IELSR31	在ICU.IELSR31寄存器中选择的事件

14.3.2 事件编号

下表列出了表14.4的标题详细信息，其中描述了每个事件编号。

Heading	Description
中断请求源	产生中断请求的源名称
Name	中断名称
中断检测形式（信号）	"边缘"或"电平"作为检测中断的方法。" "表示作为NMI中断的可用性。
连接到NVIC	" "表示该中断可以作为CPU中断使用（IELSRn设置）
Invoke DTC	" "表示中断可用于请求DTC激活（IELSRn设置）
Invoke DMAC	" "表示中断可用于请求DMAC激活（DELSRn设置）
取消贪睡模式	" "表示该中断可用于使用SELSR0请求从贪睡模式返回。否则，" "表示可以直接使用。
取消软件待机模式	" "表示中断可用于请求从软件待机模式返回

Table 14.4 Event table (1 of 4)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
001h	Port	PORT_IRQ0	✓	✓	✓	✓	✓
002h		PORT_IRQ1	✓	✓	✓	✓	✓
003h		PORT_IRQ2	✓	✓	✓	✓	✓
004h		PORT_IRQ3	✓	✓	✓	✓	✓
005h		PORT_IRQ4	✓	✓	✓	✓	✓
007h		PORT_IRQ6	✓	✓	✓	✓	✓
008h		PORT_IRQ7	✓	✓	✓	✓	✓
009h	BLE	BLEIRQ *5	✓	✓	✓	✓	✓
00Ah	Port	PORT_IRQ9	✓	✓	✓	✓	✓
00Ch		PORT_IRQ11	✓	✓	✓	✓	✓
00Fh		PORT_IRQ14	✓	✓	✓	✓	✓
010h		PORT_IRQ15	✓	✓	✓	✓	✓
011h	DMAC0	DMAC0_INT	✓	✓			
012h	DMAC1	DMAC1_INT	✓	✓			
013h	DMAC2	DMAC2_INT	✓	✓			
014h	DMAC3	DMAC3_INT	✓	✓			
015h	DTC	DTC_COMPLETE	✓			✓*4	
017h	ICU	ICU_SNZCANCEL	✓			✓	
018h	FCU	FCU_FRDYI	✓				
019h	LVD	LVD_LVD1	✓			✓	✓
01Bh	VBATT	VBATT_LVD	✓			✓	✓
01Ch	MOSC	MOSC_STOP	✓				
01Dh	Low power mode	SYSTEM_SNZREQ		✓			
01Eh	AGT0	AGT0_AGTI	✓	✓	✓		
01Fh		AGT0_AGTCMAI	✓	✓	✓		
020h		AGT0_AGTCMBI	✓	✓	✓		
021h	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓
022h		AGT1_AGTCMAI	✓	✓	✓	✓	✓
023h		AGT1_AGTCMBI	✓	✓	✓	✓	✓
024h	IWDT	IWDT_NMIUNDF	✓			✓	✓
025h	WDT	WDT_NMIUNDF	✓				
026h	RTC	RTC_ALM	✓			✓	✓
027h		RTC_PRD	✓			✓	✓
028h		RTC_CUP	✓				
029h	ADC140	ADC140_ADI	✓	✓	✓		
02Ah		ADC140_GBADI	✓	✓	✓		
02Bh		ADC140_CMPAI	✓				
02Ch		ADC140_CMPBI	✓				
02Dh		ADC140_WCMPM		✓	✓	✓*4	
02Eh		ADC140_WCMPUM		✓	✓	✓*4	
02Fh	ACMPLP	ACMP_LP0	✓			✓	✓
030h		ACMP_LP1	✓				

Table 14.4 事件表（4个中的1个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling Snooze	取消软件待机
			连接至NVIC	Invoke DTC	Invoke DMAC		
001h	Port	PORT_IRQ0	✓	✓	✓	✓	✓
002h		PORT_IRQ1	✓	✓	✓	✓	✓
003h		PORT_IRQ2	✓	✓	✓	✓	✓
004h		PORT_IRQ3	✓	✓	✓	✓	✓
005h		PORT_IRQ4	✓	✓	✓	✓	✓
007h		PORT_IRQ6	✓	✓	✓	✓	✓
008h		PORT_IRQ7	✓	✓	✓	✓	✓
009h	BLE	BLEIRQ *5	✓	✓	✓	✓	✓
00Ah	Port	PORT_IRQ9	✓	✓	✓	✓	✓
00Ch		PORT_IRQ11	✓	✓	✓	✓	✓
00Fh		PORT_IRQ14	✓	✓	✓	✓	✓
010h		PORT_IRQ15	✓	✓	✓	✓	✓
011h	DMAC0	DMAC0_INT	✓	✓			
012h	DMAC1	DMAC1_INT	✓	✓			
013h	DMAC2	DMAC2_INT	✓	✓			
014h	DMAC3	DMAC3_INT	✓	✓			
015h	DTC	DTC_COMPLETE	✓			✓*4	
017h	ICU	ICU_SNZCANCEL	✓			✓	
018h	FCU	FCU_FRDYI	✓				
019h	LVD	LVD_LVD1	✓			✓	✓
01Bh	VBATT	VBATT_LVD	✓			✓	✓
01Ch	MOSC	MOSC_STOP	✓				
01Dh	低功耗模式	SYSTEM_SNZREQ		✓			
01Eh	AGT0	AGT0_AGTI	✓	✓	✓		
01Fh		AGT0_AGTCMAI	✓	✓	✓		
020h		AGT0_AGTCMBI	✓	✓	✓		
021h	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓
022h		AGT1_AGTCMAI	✓	✓	✓	✓	✓
023h		AGT1_AGTCMBI	✓	✓	✓	✓	✓
024h	IWDT	IWDT_NMIUNDF	✓			✓	✓
025h	WDT	WDT_NMIUNDF	✓				
026h	RTC	RTC_ALM	✓			✓	✓
027h		RTC_PRD	✓			✓	✓
028h		RTC_CUP	✓				
029h	ADC140	ADC140_ADI	✓	✓	✓		
02Ah		ADC140_GBADI	✓	✓	✓		
02Bh		ADC140_CMPAI	✓				
02Ch		ADC140_CMPBI	✓				
02Dh		ADC140_WCMPM		✓	✓	✓*4	
02Eh		ADC140_WCMPUM		✓	✓	✓*4	
02Fh	ACMPLP	ACMP_LP0	✓			✓	✓
030h		ACMP_LP1	✓				

Table 14.4 Event table (2 of 4)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
031h	USBFS	USBFS_D0FIFO	✓	✓	✓		
032h		USBFS_D1FIFO	✓	✓	✓		
033h		USBFS_USBI	✓				
034h		USBFS_USBR	✓			✓	✓
035h	IIC0	IIC0_RXI	✓	✓	✓		
036h		IIC0_TXI	✓	✓	✓		
037h		IIC0_TEI	✓				
038h		IIC0_EEI	✓				
039h		IIC0_WUI	✓			✓	✓
03Ah	IIC1	IIC1_RXI	✓	✓	✓		
03Bh		IIC1_TXI	✓	✓	✓		
03Ch		IIC1_TEI	✓				
03Dh		IIC1_EEI	✓				
046h	CTSU	CTSU_CTSUWR	✓	✓	✓		
047h		CTSU_CTSURD	✓	✓	✓		
048h		CTSU_CTSUFN	✓			✓*4	
049h	KINT	KEY_INTKR	✓			✓*1	✓*1
04Ah	DOC	DOC_DOPCI	✓			✓*4	
04Bh	CAC	CAC_FERRI	✓				
04Ch		CAC_MENDI	✓				
04Dh		CAC_OVFI	✓				
04Eh	CAN0	CAN0_ERS	✓				
04Fh		CAN0_RXF	✓				
050h		CAN0_TXF	✓				
051h		CAN0_RXM	✓				
052h		CAN0_TXM	✓				
053h	I/O port	IOPORT_GROUP1	✓	✓*2	✓*2		
054h		IOPORT_GROUP2	✓	✓*2	✓*2		
055h		IOPORT_GROUP3	✓	✓*2	✓*2		
056h		IOPORT_GROUP4	✓	✓*2	✓*2		
057h	ELC	ELC_SWEVT0	✓*3	✓			
058h		ELC_SWEVT1	✓*3	✓			
059h	POEG	POEG_GROUP0	✓				
05Ah		POEG_GROUP1	✓				
05Bh	GPT320	GPT0_CCMPA	✓	✓	✓		
05Ch		GPT0_CCMPB	✓	✓	✓		
05Dh		GPT0_CMPC	✓	✓	✓		
05Eh		GPT0_CMPD	✓	✓	✓		
05Fh		GPT0_CMPE	✓	✓	✓		
060h		GPT0_CMPF	✓	✓	✓		
061h		GPT0_OVF	✓	✓	✓		
062h		GPT0_UDF	✓	✓	✓		

Table 14.4 事件表（2个，共4个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling Snooze	取消软件待机
			连接至NVIC	Invoke DTC	Invoke DMAC		
031h	USBFS	USBFS_D0FIFO	✓	✓	✓		
032h		USBFS_D1FIFO	✓	✓	✓		
033h		USBFS_USBI	✓				
034h		USBFS_USBR	✓			✓	✓
035h	IIC0	IIC0_RXI	✓	✓	✓		
036h		IIC0_TXI	✓	✓	✓		
037h		IIC0_TEI	✓				
038h		IIC0_EEI	✓				
039h		IIC0_WUI	✓			✓	✓
03Ah	IIC1	IIC1_RXI	✓	✓	✓		
03Bh		IIC1_TXI	✓	✓	✓		
03Ch		IIC1_TEI	✓				
03Dh		IIC1_EEI	✓				
046h	CTSU	CTSU_CTSUWR	✓	✓	✓		
047h		CTSU_CTSURD	✓	✓	✓		
048h		CTSU_CTSUFN	✓			✓*4	
049h	KINT	KEY_INTKR	✓			✓*1	✓*1
04Ah	DOC	DOC_DOPCI	✓			✓*4	
04Bh	CAC	CAC_FERRI	✓				
04Ch		CAC_MENDI	✓				
04Dh		CAC_OVFI	✓				
04Eh	CAN0	CAN0_ERS	✓				
04Fh		CAN0_RXF	✓				
050h		CAN0_TXF	✓				
051h		CAN0_RXM	✓				
052h		CAN0_TXM	✓				
053h	I/O port	IOPORT_GROUP1	✓	✓*2	✓*2		
054h		IOPORT_GROUP2	✓	✓*2	✓*2		
055h		IOPORT_GROUP3	✓	✓*2	✓*2		
056h		IOPORT_GROUP4	✓	✓*2	✓*2		
057h	ELC	ELC_SWEVT0	✓*3	✓			
058h		ELC_SWEVT1	✓*3	✓			
059h	POEG	POEG_GROUP0	✓				
05Ah		POEG_GROUP1	✓				
05Bh	GPT320	GPT0_CCMPA	✓	✓	✓		
05Ch		GPT0_CCMPB	✓	✓	✓		
05Dh		GPT0_CMPC	✓	✓	✓		
05Eh		GPT0_CMPD	✓	✓	✓		
05Fh		GPT0_CMPE	✓	✓	✓		
060h		GPT0_CMPF	✓	✓	✓		
061h		GPT0_OVF	✓	✓	✓		
062h		GPT0_UDF	✓	✓	✓		

Table 14.4 Event table (3 of 4)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
063h	GPT321	GPT1_CCMPA	✓	✓	✓		
064h		GPT1_CCMPB	✓	✓	✓		
065h		GPT1_CMPC	✓	✓	✓		
066h		GPT1_CMPD	✓	✓	✓		
067h		GPT1_CMPE	✓	✓	✓		
068h		GPT1_CMPF	✓	✓	✓		
069h		GPT1_OVF	✓	✓	✓		
06Ah		GPT1_UDF	✓	✓	✓		
06Bh	GPT322	GPT2_CCMPA	✓	✓	✓		
06Ch		GPT2_CCMPB	✓	✓	✓		
06Dh		GPT2_CMPC	✓	✓	✓		
06Eh		GPT2_CMPD	✓	✓	✓		
06Fh		GPT2_CMPE	✓	✓	✓		
070h		GPT2_CMPF	✓	✓	✓		
071h		GPT2_OVF	✓	✓	✓		
072h		GPT2_UDF	✓	✓	✓		
073h	GPT323	GPT3_CCMPA	✓	✓	✓		
074h		GPT3_CCMPB	✓	✓	✓		
075h		GPT3_CMPC	✓	✓	✓		
076h		GPT3_CMPD	✓	✓	✓		
077h		GPT3_CMPE	✓	✓	✓		
078h		GPT3_CMPF	✓	✓	✓		
079h		GPT3_OVF	✓	✓	✓		
07Ah		GPT3_UDF	✓	✓	✓		
07Bh	GPT164	GPT4_CCMPA	✓	✓	✓		
07Ch		GPT4_CCMPB	✓	✓	✓		
07Dh		GPT4_CMPC	✓	✓	✓		
07Eh		GPT4_CMPD	✓	✓	✓		
07Fh		GPT4_CMPE	✓	✓	✓		
080h		GPT4_CMPF	✓	✓	✓		
081h		GPT4_OVF	✓	✓	✓		
082h		GPT4_UDF	✓	✓	✓		
083h	GPT165	GPT5_CCMPA	✓	✓	✓		
084h		GPT5_CCMPB	✓	✓	✓		
085h		GPT5_CMPC	✓	✓	✓		
086h		GPT5_CMPD	✓	✓	✓		
087h		GPT5_CMPE	✓	✓	✓		
088h		GPT5_CMPF	✓	✓	✓		
089h		GPT5_OVF	✓	✓	✓		
08Ah		GPT5_UDF	✓	✓	✓		

Table 14.4 事件表（3个，共4个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling Snooze	取消软件待机
			连接至NVIC	Invoke DTC	Invoke DMAC		
063h	GPT321	GPT1_CCMPA	✓	✓	✓		
064h		GPT1_CCMPB	✓	✓	✓		
065h		GPT1_CMPC	✓	✓	✓		
066h		GPT1_CMPD	✓	✓	✓		
067h		GPT1_CMPE	✓	✓	✓		
068h		GPT1_CMPF	✓	✓	✓		
069h		GPT1_OVF	✓	✓	✓		
06Ah		GPT1_UDF	✓	✓	✓		
06Bh	GPT322	GPT2_CCMPA	✓	✓	✓		
06Ch		GPT2_CCMPB	✓	✓	✓		
06Dh		GPT2_CMPC	✓	✓	✓		
06Eh		GPT2_CMPD	✓	✓	✓		
06Fh		GPT2_CMPE	✓	✓	✓		
070h		GPT2_CMPF	✓	✓	✓		
071h		GPT2_OVF	✓	✓	✓		
072h		GPT2_UDF	✓	✓	✓		
073h	GPT323	GPT3_CCMPA	✓	✓	✓		
074h		GPT3_CCMPB	✓	✓	✓		
075h		GPT3_CMPC	✓	✓	✓		
076h		GPT3_CMPD	✓	✓	✓		
077h		GPT3_CMPE	✓	✓	✓		
078h		GPT3_CMPF	✓	✓	✓		
079h		GPT3_OVF	✓	✓	✓		
07Ah		GPT3_UDF	✓	✓	✓		
07Bh	GPT164	GPT4_CCMPA	✓	✓	✓		
07Ch		GPT4_CCMPB	✓	✓	✓		
07Dh		GPT4_CMPC	✓	✓	✓		
07Eh		GPT4_CMPD	✓	✓	✓		
07Fh		GPT4_CMPE	✓	✓	✓		
080h		GPT4_CMPF	✓	✓	✓		
081h		GPT4_OVF	✓	✓	✓		
082h		GPT4_UDF	✓	✓	✓		
083h	GPT165	GPT5_CCMPA	✓	✓	✓		
084h		GPT5_CCMPB	✓	✓	✓		
085h		GPT5_CMPC	✓	✓	✓		
086h		GPT5_CMPD	✓	✓	✓		
087h		GPT5_CMPE	✓	✓	✓		
088h		GPT5_CMPF	✓	✓	✓		
089h		GPT5_OVF	✓	✓	✓		
08Ah		GPT5_UDF	✓	✓	✓		

Table 14.4 Event table (4 of 4)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC		
09Bh	GPT168	GPT8_CCMPA	✓	✓	✓		
09Ch		GPT8_CCMPB	✓	✓	✓		
09Dh		GPT8_CMPC	✓	✓	✓		
09Eh		GPT8_CMPD	✓	✓	✓		
09Fh		GPT8_CMPE	✓	✓	✓		
0A0h		GPT8_CMPF	✓	✓	✓		
0A1h		GPT8_OVF	✓	✓	✓		
0A2h		GPT8_UDF	✓	✓	✓		
0ABh	GPT	GPT_UVWEDGE	✓				
0ACh	SCI0	SCI0_RXI	✓	✓	✓		
0ADh		SCI0_TXI	✓	✓	✓		
0AEh		SCI0_TEI	✓				
0AFh		SCI0_ERI	✓				
0B0h		SCI0_AM	✓			✓*4	
0B1h		SCI0_RXI_OR_ERI				✓*4	
0B2h	SCI1	SCI1_RXI	✓	✓	✓		
0B3h		SCI1_TXI	✓	✓	✓		
0B4h		SCI1_TEI	✓				
0B5h		SCI1_ERI	✓				
0B6h		SCI1_AM	✓				
0C1h	SCI4	SCI4_RXI	✓	✓	✓		
0C2h		SCI4_TXI	✓	✓	✓		
0C3h		SCI4_TEI	✓				
0C4h		SCI4_ERI	✓				
0C5h		SCI4_AM	✓				
0C6h	SCI9	SCI9_RXI	✓	✓	✓		
0C7h		SCI9_TXI	✓	✓	✓		
0C8h		SCI9_TEI	✓				
0C9h		SCI9_ERI	✓				
0CAh		SCI9_AM	✓				
0CBh	SPI0	SPI0_SPRI	✓	✓	✓		
0CCh		SPI0_SPTI	✓	✓	✓		
0CDh		SPI0_SPII	✓				
0CEh		SPI0_SPEI	✓				
0CFh		SPI0_SPTEND	✓				
0D0h	SPI1	SPI1_SPRI	✓	✓	✓		
0D1h		SPI1_SPTI	✓	✓	✓		
0D2h		SPI1_SPII	✓				
0D3h		SPI1_SPEI	✓				
0D4h		SPI1_SPTEND	✓				

Note 1. Only supported when KRCTL.KRMD = 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.
Note 5. The Bluetooth middleware executes processing in response to BLEIRQ. Do not use this source.

Table 14.4 事件表（4个，共4个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling Snooze	取消软件待机
			连接至NVIC	Invoke DTC	Invoke DMAC		
09Bh	GPT168	GPT8_CCMPA	✓	✓	✓		
09Ch		GPT8_CCMPB	✓	✓	✓		
09Dh		GPT8_CMPC	✓	✓	✓		
09Eh		GPT8_CMPD	✓	✓	✓		
09Fh		GPT8_CMPE	✓	✓	✓		
0A0h		GPT8_CMPF	✓	✓	✓		
0A1h		GPT8_OVF	✓	✓	✓		
0A2h		GPT8_UDF	✓	✓	✓		
0ABh	GPT	GPT_UVWEDGE	✓				
0ACh	SCI0	SCI0_RXI	✓	✓	✓		
0ADh		SCI0_TXI	✓	✓	✓		
0AEh		SCI0_TEI	✓				
0AFh		SCI0_ERI	✓				
0B0h		SCI0_AM	✓			✓*4	
0B1h		SCI0_RXI_OR_ERI				✓*4	
0B2h	SCI1	SCI1_RXI	✓	✓	✓		
0B3h		SCI1_TXI	✓	✓	✓		
0B4h		SCI1_TEI	✓				
0B5h		SCI1_ERI	✓				
0B6h		SCI1_AM	✓				
0C1h	SCI4	SCI4_RXI	✓	✓	✓		
0C2h		SCI4_TXI	✓	✓	✓		
0C3h		SCI4_TEI	✓				
0C4h		SCI4_ERI	✓				
0C5h		SCI4_AM	✓				
0C6h	SCI9	SCI9_RXI	✓	✓	✓		
0C7h		SCI9_TXI	✓	✓	✓		
0C8h		SCI9_TEI	✓				
0C9h		SCI9_ERI	✓				
0CAh		SCI9_AM	✓				
0CBh	SPI0	SPI0_SPRI	✓	✓	✓		
0CCh		SPI0_SPTI	✓	✓	✓		
0CDh		SPI0_SPII	✓				
0CEh		SPI0_SPEI	✓				
0CFh		SPI0_SPTEND	✓				
0D0h	SPI1	SPI1_SPRI	✓	✓	✓		
0D1h		SPI1_SPTI	✓	✓	✓		
0D2h		SPI1_SPII	✓				
0D3h		SPI1_SPEI	✓				
0D4h		SPI1_SPTEND	✓				

Note 1. 仅当KRCTL.KRMD=1时支持。
Note 2. 只有第一个边缘检测有效。
Note 3. 仅支持DTC传输后的中断。
Note 4. Using SELSR0.
Note 5. 蓝牙中间件响应BLEIRQ执行处理。请勿使用此来源。

14.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation, or DMAC activation.

14.4.1 Detecting Interrupts

External pin interrupt requests are detected in either:

- Edges (falling edge, rising edge, or rising and falling edges) of the interrupt signal
- Level (low level) of the interrupt signal.

Set the IRQMD[1:0] bits in the IRQCRi register to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see section 14.3.2, Event Number. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

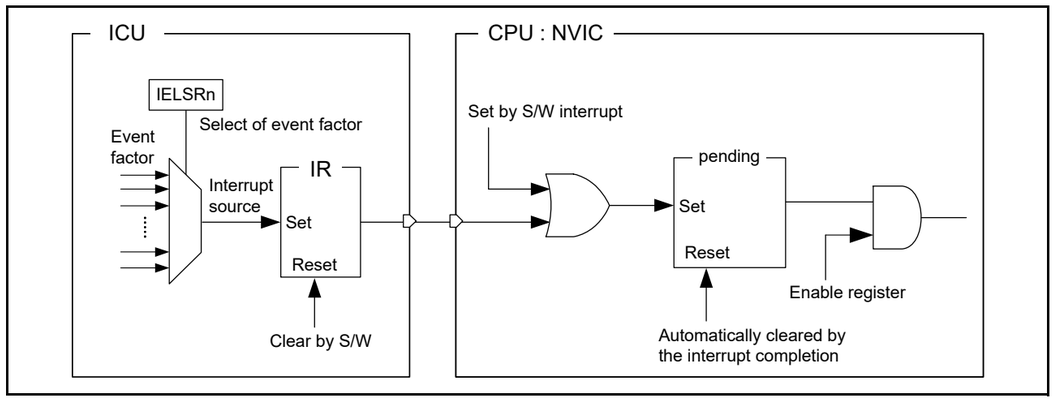


Figure 14.2 Interrupt path of the ICU and CPU (NVIC)

Use the following procedures for detecting interrupts:

- General operations during an interrupt:
  - When a non-software interrupt occurs:
    The IELSRn.IR flag and Interrupt Set/Clear-Pending register (NVIC) are set.
  - When a software interrupt occurs:
    Set the Interrupt Set-Pending register.
  - When an interrupt is complete:
    Clear the IELSRn.IR flag with software.
    The Interrupt Set/Clear-Pending register clears automatically.
- When interrupts are enabled:
  1) Set the Interrupt Set-Enable register.
  2) Set the IELSRn.IELS bits as interrupt source.
  3) Specify the operation settings for the event source.
- When interrupts are disabled:
  1) Disable the settings for the event source.
  2) Clear the IELSRn.IELS bits (IELSRn.IELS[7:0] = 000h). Clear the IELSRn.IR flag as required.

14.4 中断操作

ICU执行以下功能：

- 检测中断
- 启用和禁用中断
- 选择中断请求目标，例如CPU中断、DTC激活或DMAC激活。

14.4.1 检测中断

在以下任一情况下检测到外部引脚中断请求：

- 中断信号的边沿（下降沿、上升沿或上升沿和下降沿）
- 中断信号的电平（低电平）。

设置IRQCRi寄存器中的IRQMD[1:0]位以选择IRQi引脚的检测模式。对于与外围模块相关的中断源，请参见第14.3.2节，事件编号。事件必须在中断发生之前被NVIC接受并被CPU接受。

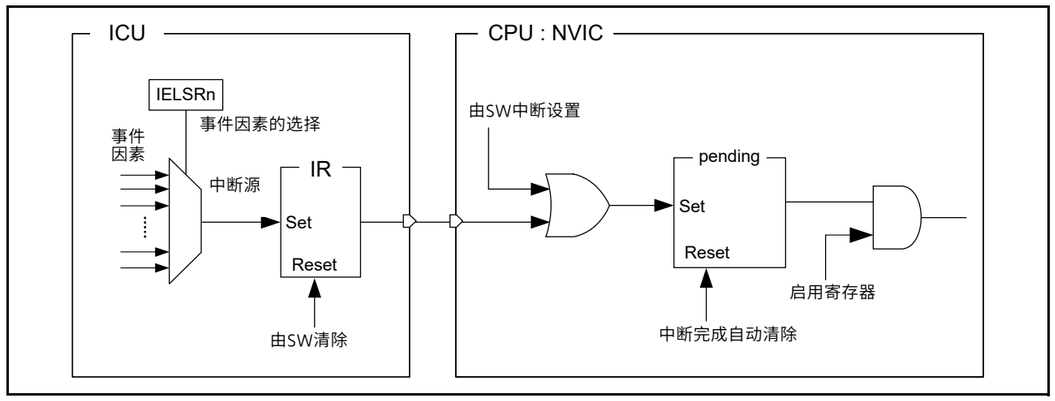


Figure 14.2 ICU和CPU(NVIC)的中断路径

使用以下过程检测中断：

- 中断期间的一般操作：
  - 当发生非软件中断时：
    IELSRn.IR标志和中断设置清除挂起寄存器(NVIC)已设置。
  - 当发生软件中断时：
    设置中断设置挂起寄存器。
  - 当中断完成时：
    用软件清除IELSRn.IR标志。
    中断设置清除挂起寄存器自动清除。
- 启用中断时：
  1) 设置中断设置启用寄存器。
  2) 将IELSRn.IELS位设置为中断源。
  3) 指定事件源的操作设置。
- 当中断被禁用时：
  1) 禁用事件源的设置。
  2) 清零IELSRn.IELS位（IELSRn.IELS[7:0]=000h）。根据需要清除IELSRn.IR标志。

3) Clear the Interrupt Clear-Enable register. Clear the Interrupt Clear-Pending register as required.

- When polling for interrupts:

1) Set the Interrupt Clear-Enable register (disabling interrupts).
2) Set the IELSRn.IELS bits (selecting the source).
3) Specify the operation settings for the event source.
4) Poll the Interrupt Set-Pending register.
5) When polling is no longer required, follow the procedure for clearing an interrupt when it is complete.

14.4.2 Selecting Interrupt Request Destinations

The interrupt output destination, CPU, DTC or DMAC, can be independently selected for each interrupt source. The available destinations are fixed for each interrupt, as described in Table 14.4, Event table.

Note: Do not use an interrupt request destination setting that is not indicated by a check, ✓, in the event list (Table 14.4).

If you select the CPU or DTC in one IELSRn register, setting the same interrupt factor in any other IELSRn register is prohibited. Similarly, if you select the DMAC in one DELSRn register, setting the same interrupt factor in any other DELSRn register is prohibited.

Note: Setting the same interrupt factor for IELSRn and DELSRn is prohibited.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin, be sure to set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.

14.4.2.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Set the IELSRn.IELS bits and IELSRn.DTCE bit to 0.

14.4.2.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. After DTC transmission completes, the associated interrupt occurs. Use the following procedure:

1. Set the IELSRn.IELS bits to the target event and the IELSRn.DTCE bit to 1.
2. Set the DTC module activation bit DTCST.DTCST to 1.

Table 14.5 shows operation when the DTC is the request destination.

Table 14.5 Operations when DTC is activated

Interrupt request destination	DISEL*1	Remaining transfer operations	Operations per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer data	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination

Note 1. Set the interrupt request mode for the DTC in the DTC.MRB.DISEL bit.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.

3) 清除中断清除启用寄存器。根据需要清除中断清除挂起寄存器。

- 轮询中断时：

1) 设置中断清除启用寄存器（禁用中断）。
2) 设置IELSRn.IELS位（选择源）。
3) 指定事件源的操作设置。
4) 轮询中断设置挂起寄存器。
5) 当不再需要轮询时，按照完成后清除中断的过程。

14.4.2 选择中断请求目标

可以为每个中断源独立选择中断输出目标CPU、DTC或DMAC。每个中断的可用目的地都是固定的，如表14.4，事件表中所述。

Note: 请勿使用事件列表（表14.4）中未通过勾号 指示的中断请求目标设置。

如果在一个IELSRn寄存器中选择CPU或DTC，则禁止在任何其他IELSRn寄存器中设置相同的中断因子。同样，如果您在一个DELSRn寄存器中选择DMAC，则禁止在任何其他DELSRn寄存器中设置相同的中断因子。

Note: 禁止为IELSRn和DELSRn设置相同的中断因子。

如果选择DMAC或DTC作为来自IRQi引脚的请求的目的地，请务必将IRQMD[1:0]位设置为IRQCRi用于选择边缘检测的中断。

14.4.2.1 CPU中断请求

当IELSRn.DTCE=0时，将IELSRn寄存器中指定的事件输出到NVIC。将IELSRn.IELS位和IELSRn.DTCE位设置为0。

14.4.2.2 DTC activation

当IELSRn.DTCE=1时，将IELSRn寄存器中指定的事件输出到DTC。DTC传输完成后，将发生相关中断。使用以下过程：

1. 将IELSRn.IELS位设置为目标事件，并将IELSRn.DTCE位设置为1。
2. 将DTC模块激活位DTCST.DTCST设置为1。

表14.5显示了DTC是请求目的地时的操作。

Table 14.5 DTC激活时的操作

中断请求目的地	DISEL*1	剩余的转移操作	每个请求的操作	IR*2	传输后的中断请求目的地
DTC*3	1	≠ 0	DTC transfer → CPU中断	CPU接受中断时清零	DTC
		= 0	DTC transfer → CPU中断	CPU接受中断时清零	IELSRn.DTCE位清零，CPU成为目标
	0	≠ 0	DTC transfer	读取DTC传输数据后，在DTC数据传输开始时清零	DTC
		= 0	DTC transfer → CPU中断	CPU接受中断时清零	IELSRn.DTCE位清零，CPU成为目标

Note 1. 在DTC.MRB.DISEL位中设置DTC的中断请求模式。
Note 2. IELSRn.IR标志为1时，忽略再次发生的中断请求（DTC激活请求）。

Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. The DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 18.3, Chain transfer conditions in section 18, Data Transfer Controller (DTC).

14.4.2.3 DMAC activation

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. To set the interrupt source for DMAC, use the following procedure:

1. Set the DELSRn.DELS[7:0].
2. Set the IELSRn.IELS bits to the target event and the IELSRn.DTCE bit to 1.
3. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
4. Set the DMAC transfer enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.
5. Set the DMAC operation enable bit (DMAST.DMST) to 1.

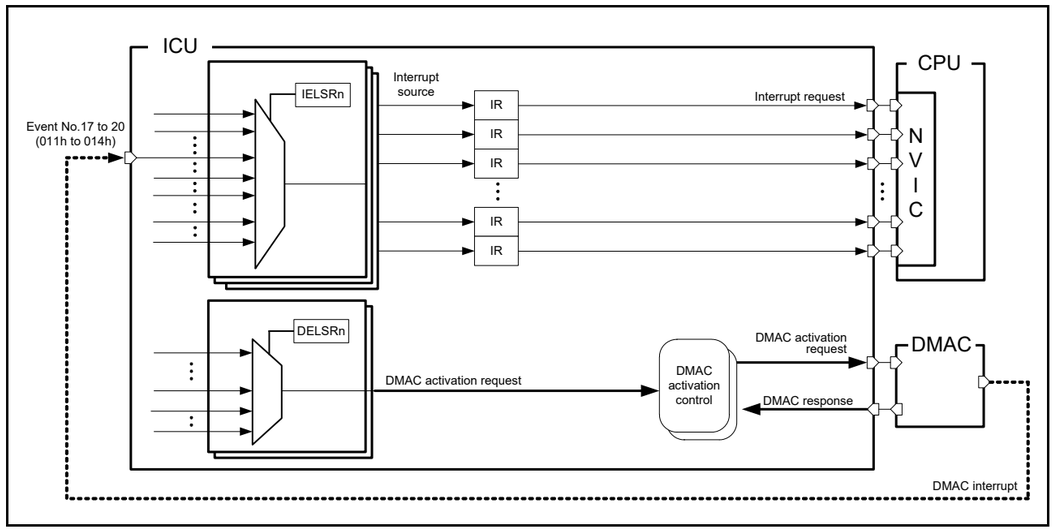


Figure 14.3 DMAC request trigger and interrupt path

14.4.3 Digital Filter

A digital filter function is provided for the external interrupt request pins (IRQi, i = 0 to 4, 6, 7, 9, 11, 14, 15) and the NMI pin interrupt. It samples input signals on the filter PCLKB sampling clock and removes any signal with a pulse width less than 3 sampling cycles.

- To use the digital filter for a IRQi pin:

1)	Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits (i = 0 to 4, 6, 7, 9, 11, 14, 15).
2)	Set the IRQCRi.FLTEN bit (i = 0 to 4, 6, 7, 9, 11, 14, 15) to 1 (digital filter enabled).

- To use the digital filter for the NMI pin:

1)	Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2)	Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 14.4 shows an example of digital filter operation.

Note 3. 对于链式传输，DTC传输将持续到最后一个链式传输结束。DISEL位状态和剩余传输计数决定是否发生CPU中断、IELSRn.IR标志清除时序以及传输后的中断请求目的地。请参阅第18节，数据传输控制器(DTC)中的表18.3，链传输条件。

14.4.2.3 DMAC activation

当IELSRn.DTCE=0时，将IELSRn寄存器中指定的事件输出到NVIC。要为DMAC设置中断源，请使用以下过程：

1. 设置DELSRn.DELS[7:0]。
2. 将IELSRn.IELS位设置为目标事件，并将IELSRn.DTCE位设置为1。
3. 将目标DMAC通道(DMACm.DMTMD.DCTG[1:0])的激活源设置为01b（中断模块检测）。
4. 将目标DMAC通道(DMACm.DMCNT.DTE)的DMAC传输使能位设置为1。
5. 将DMAC操作使能位(DMAST.DMST)设置为1。

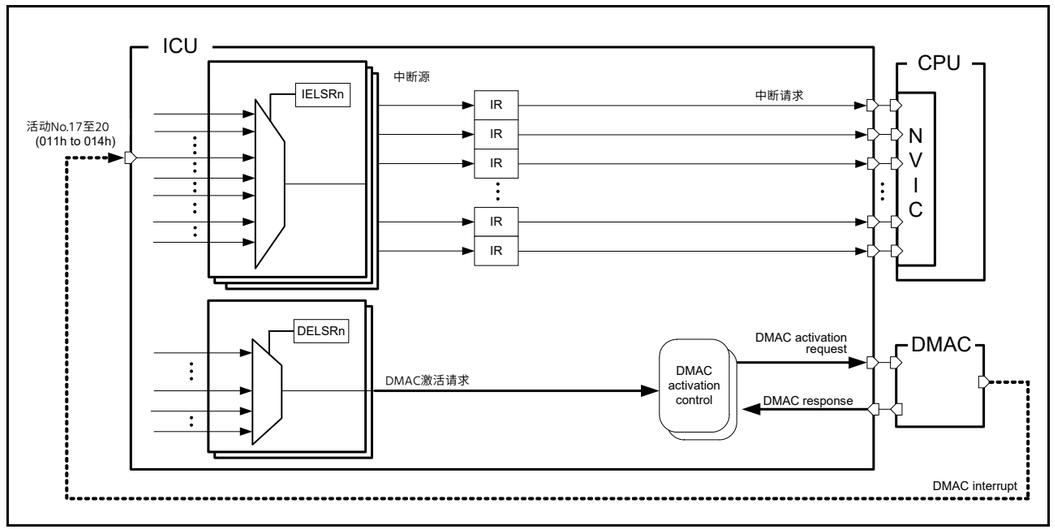


Figure 14.3 DMAC请求触发和中断路径

14.4.3 数字滤波器

为外部中断请求引脚（IRQi，i=0至4、6、7、9、11、14、15）和NMI引脚中断提供了数字过滤功能。它在滤波器PCLKB采样时钟上对输入信号进行采样，并去除脉冲宽度小于3个采样周期的任何信号。

- 为IRQi引脚使用数字滤波器：

1)	在IRQCRi.FCLKSEL[1:0]位（i=0到4、6、7、9、11、14、15）中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。
2)	将IRQCRi.FLTEN位（i=0到4、6、7、9、11、14、15）设置为1（启用数字滤波器）。

- 为NMI引脚使用数字滤波器：

1)	在NMICR.NFCLKSEL[1:0]位中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。
2)	将NMICR.NFLTEN位设置为1（启用数字滤波器）。

图14.4显示了数字滤波器操作的示例。

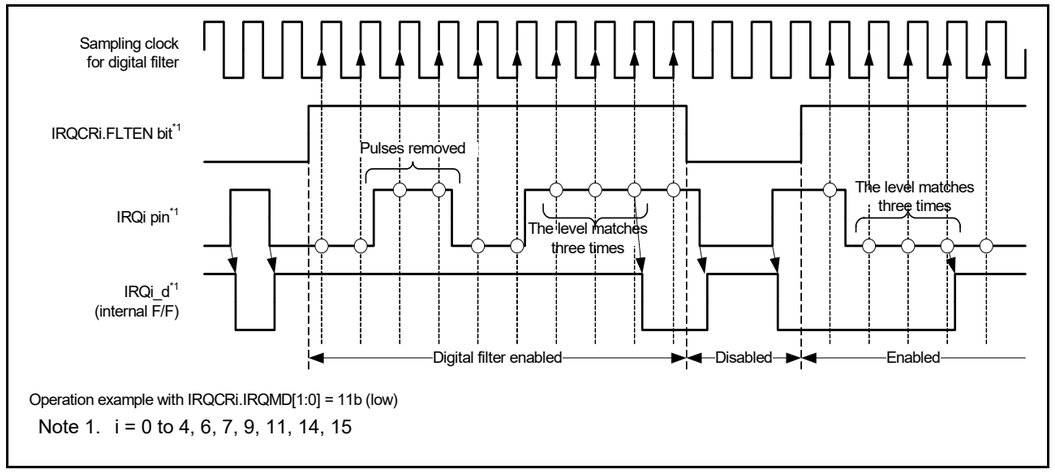


Figure 14.4 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The ICU clock stops in Software Standby. On exiting Software Standby, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby, an incorrect edge might be detected. You can enable the digital filters again after exiting Software Standby mode.

14.4.4 External Pin Interrupts

To use external pin interrupts:

1. Clear the IRQCRi.FLTEN bit (0 to 4, 6, 7, 9, 11, 14, 15) to 0 (digital filter disabled).
2. Set or confirm the I/O port settings.
3. Set the IRQMD[1:0] bits, FCLKSEL[1:0] bits and FLTEN bit of the IRQCRi register.
4. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt request, set the IELSRn.IELS[7:0] bits and IELSRn.DTCE bit to 0
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS[7:0] bits and IELSRn.DTCE bit to 1
   - If the IRQ pin is to be used for DMAC activation, set the DELSRn.DELS bits.

14.5 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- VBATT monitor interrupt
- SRAM parity error interrupt
- SRAM ECC error interrupt
- MPU bus master error interrupt
- MPU bus slave error interrupt

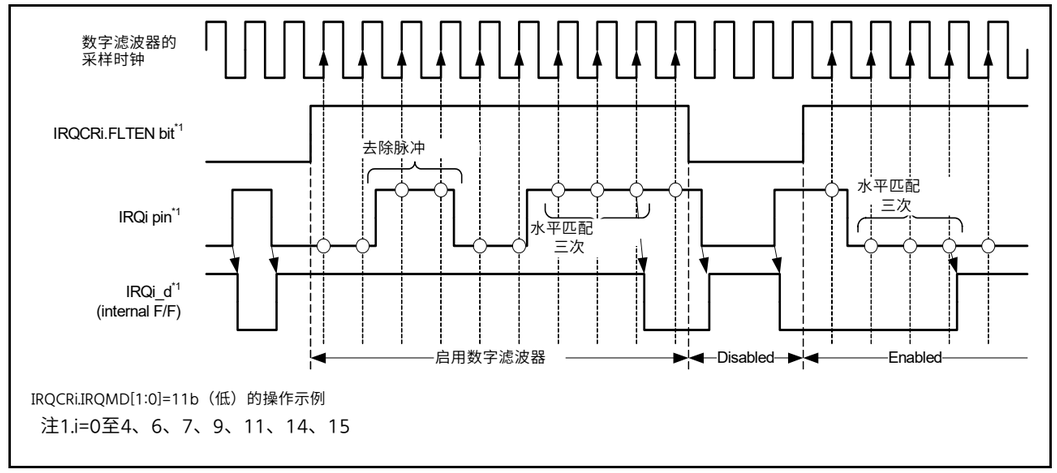


Figure 14.4 数字滤波器操作示例

在进入软件待机模式之前，通过清除IRQCRi.FLTEN和NMICR.NFLTEN位来禁用数字滤波器。ICU时钟在软件待机中停止。在退出软件待机时，电路通过将待机前的状态与待机释放后的状态进行比较来检测边沿。如果在软件待机期间输入发生变化，则可能会检测到不正确的边沿。您可以在退出软件待机模式后再次启用数字滤波器。

14.4.4 外部引脚中断

要使用外部引脚中断：

1. 将IRQCRi.FLTEN位（0到4、6、7、9、11、14、15）清除为0（禁用数字滤波器）。
2. 设置或确认IO端口设置。
3. 设置IRQCRi寄存器的IRQMD[1:0]位、FCLKSEL[1:0]位和FLTEN位。
4. 选择IRQ引脚如下：
   - 如果IRQ引脚用于CPU中断请求，请将IELSRn.IELS[7:0]位和IELSRn.DTCE位设置为0
   - 如果IRQ引脚用于DTC激活，请将IELSRn.IELS[7:0]位和IELSRn.DTCE位设置为1
   - 如果IRQ引脚用于DMAC激活，则设置DELSRn.DELS位。

14.5 不可屏蔽中断操作

以下源可以触发不可屏蔽中断：

- NMI引脚中断
- 振荡停止检测中断
- WDT下溢刷新错误中断
- IWDT下溢刷新错误中断
- 电压监视器1中断
- VBATT监控中断
- SRAM奇偶校验错误中断
- SRAMECC错误中断
- MPU总线主机错误中断
- MPU总线从机错误中断

- CPU stack pointer monitor interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC or DMAC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts, use the following procedure:

To use the NMI pin, follow steps 1. to 3.

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. Set the NMIMD bit, NFCLKSEL[1:0] bits and NFLTEN bit of NMICR register.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI interrupt cannot be disabled when enabled, except by a reset.

14.6 Return from Low Power Mode

Table 14.4, Event table lists the interrupt sources you can use to exit Sleep or Software Standby mode. For details, see section 11, Low Power Modes. Sections 14.6.1 to 14.6.3 describe how to use interrupts to return from Sleep, Software Standby, and Snooze modes.

14.6.1 Return from Sleep mode

To return from Sleep mode in response to an interrupt:

1. Select the CPU as the interrupt request destination.
2. Enable the interrupt in the NVIC.

To return from Sleep mode in response to a non-maskable interrupt, use the NMIER register to enable the target interrupt request.

14.6.2 Return from Software Standby mode

The ICU can return from Software Standby mode using a non-maskable interrupt or an interrupt selected in the WUPEN register. See section 14.2.9, Wake Up Interrupt Enable Register (WUPEN).

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby.
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.
2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQ pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

14.6.3 Return from Snooze mode

The ICU can return to Normal mode from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Use either of the following methods to select the event that you want to trigger a return to Normal mode from Snooze mode:

- CPU堆栈指针监视中断。

不可屏蔽中断只能用于CPU，不能激活DTC或DMAC。不可屏蔽中断优先于所有其他中断。不可屏蔽中断状态可以在不可屏蔽中断状态寄存器(NMISR)中验证。在从NMI处理程序返回之前，确认NMISR中的所有位都为0。

默认情况下禁用不可屏蔽中断。要使用不可屏蔽中断，请使用以下过程：

要使用NMI引脚，请执行步骤1.至3。

1. 将NMICR.NFLTEN位清除为0（禁用数字滤波器）。
2. 设置NMICR寄存器的NMIMD位、NFCLKSEL[1:0]位和NFLTEN位。
3. 将1写入NMICLR.NMICLR位以将NMISR.NMIST标志清零。
4. 通过将1写入不可屏蔽中断启用寄存器(NMIER)中的相关位来启用不可屏蔽中断。

将1写入NMIER寄存器后，随后对NMIER中的NMIEN位的写访问将被忽略。启用时不能禁用NMI中断，除非通过复位。

14.6 从低功耗模式返回

表14.4，事件表列出了可用于退出睡眠或软件待机模式的中断源。有关详细信息，请参阅第11节，低功耗模式。14.6.1到14.6.3节描述了如何使用中断从休眠、软件待机和贪睡模式返回。

14.6.1 从睡眠模式返回

从睡眠模式返回以响应中断：

1. 选择CPU作为中断请求目标。
2. 在NVIC中启用中断。

要从休眠模式返回以响应不可屏蔽的中断，请使用NMIER寄存器来启用目标中断请求。

14.6.2 从软件待机模式返回

ICU可以使用不可屏蔽中断或在WUPEN寄存器中选择的中断从软件待机模式返回。请参见第14.2.9节，唤醒中断使能寄存器(WUPEN)。

从软件待机模式返回：

1. 选择允许从软件待机返回的中断源。
   - 对于不可屏蔽中断，使用NMIER寄存器启用目标中断请求
   - 对于可屏蔽中断，使用WUPEN寄存器启用目标中断请求。
2. 选择CPU作为中断请求目标。
3. 在NVIC中启用中断。

不满足这些条件的通过IRQ引脚的中断请求在时钟停止时不会被检测到
软件待机模式。

14.6.3 从贪睡模式返回

ICU可以使用为该模式提供的中断从贪睡模式返回到正常模式。

要从贪睡模式返回正常模式：

1. 使用以下任一方法选择要触发返回正常模式的事件
Snooze mode:

a. Set the event that you want to trigger a return to Normal mode from Snooze mode in SELSR0.SEL and set the value 017h (ICU_SNZCANCEL) in IELSRn.IELS.

b. Set the event that you want to trigger a return to Normal mode from Snooze mode in IELSRn.IELS.

2. Select the CPU as the interrupt request destination.

3. Enable the interrupt in the NVIC.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU acknowledges the interrupt after returning to Normal mode from Software Standby mode. If an event selected in DELSRn is detected, the DMAC acknowledges the interrupt after returning to Normal mode from Software Standby mode.

14.7 Using the WFI instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

14.8 Reference

ARM® Cortex®-M4 Processor Technical Reference Manual (ARM DDI 0439D).

一个。在SELSR0.SEL中设置要触发从贪睡模式返回到正常模式的事件，并在IELSRn.IELS中设置值017h(ICU_SNZCANCEL)。

湾。在IELSRn.IELS中设置要触发从贪睡模式返回到正常模式的事件。

2. 选择CPU作为中断请求目标。

3. 在NVIC中启用中断。

Note: 在贪睡模式下，向ICU提供时钟。如果检测到在IELSRn中选择的事件，CPU在从软件待机模式返回到正常模式后确认中断。如果检测到在DELSRn中选择的事件，则DMAC在从软件返回到正常模式后确认中断

待机模式。

14.7 将WFI指令与不可屏蔽中断一起使用

每当执行WFI指令时，请确认NMISR寄存器中的所有状态标志为0。

14.8 Reference

ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)。

15. Buses

15.1 Overview

Table 15.1 lists the bus specifications, Figure 15.1 shows the bus configuration, and Table 15.2 lists the addresses assigned for each bus.

Table 15.1 Bus specifications

Bus type		Description
Main bus	ICode bus (CPU)	• Connected to the CPU • Connected to on-chip memory (code flash memory).
	DCode bus (CPU)	• Connected to the CPU • Connected to on-chip memory (code flash memory).
	System bus (CPU)	• Connected to the CPU • Connected to on-chip memory, internal peripheral bus.
	DMA bus	• Connected to the DMAC/DTC • Connected to on-chip memory, internal peripheral bus.
Slave interface	Memory bus 1	• Connected to code flash memory
	Memory bus 3	• Connected to code flash memory by DMA bus
	Memory bus 4	• Connected to SRAM0
	Internal peripheral bus 1	• Connected to system control related to peripheral modules
	Internal peripheral bus 3	• Connected to peripheral modules (CAC, ELC, I/O ports, POEG, RTC, WDT, IWDT, IIC, CAN, ADC14, DAC12, and DOC)
	Internal peripheral bus 4	• Connected to peripheral modules (SCI, SPI, CRC, and GPT)
	Internal peripheral bus 5	• Connected to peripheral modules (KINT, AGT, USBFS, OPAMP, ACMPLP, DAC8, SLCDC, and CTSU)
	Internal peripheral bus 7	• Connected to SecureIPs
	Internal peripheral bus 9	• Connected to flash memory (in P/E)*1 and data flash memory

Note 1. P/E = Programming/Erasure.

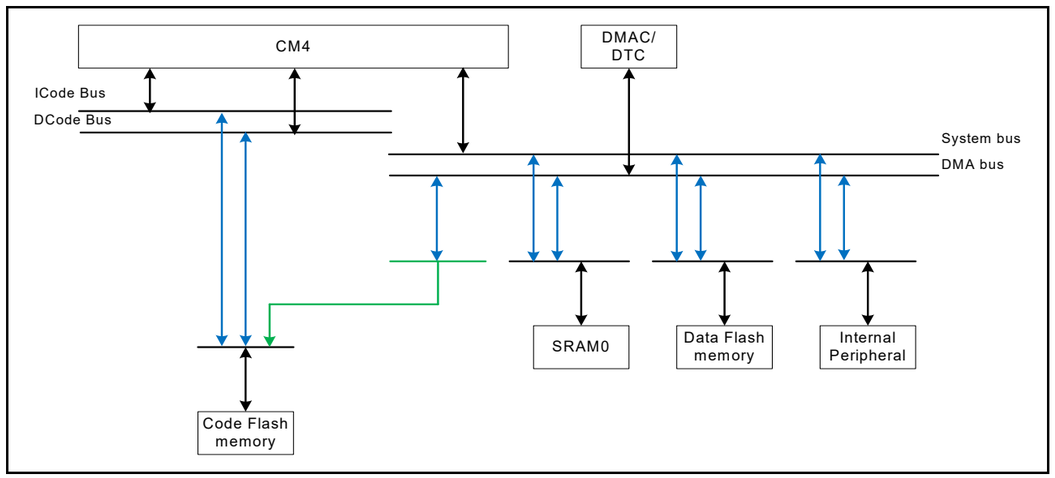


Figure 15.1 Bus configuration

15. Buses

15.1 Overview

表15.1列出了总线规格，图15.1显示了总线配置，表15.2列出了分配给每个总线的地址。

Table 15.1 总线规格

巴士类型		Description
主要总线	ICode bus (CPU)	连接到CPU 连接到片上存储器（代码闪存）。
	DCode bus (CPU)	连接到CPU 连接到片上存储器（代码闪存）。
	系统总线(CPU)	连接到CPU 连接到片上存储器、内部外围总线。
	DMA bus	连接到DMACDTC 连接到片上存储器、内部外围总线。
从接口	内存总线1	连接到代码闪存
	内存总线3	通过DMA总线连接到代码闪存
	内存总线4	连接到SRAM0
	内部外围总线1	连接到与外围模块相关的系统控制
	内部外围总线3	连接外围模块（CAC、ELC、IO端口、POEG、RTC、WDT、IWDT、IIC、CAN、ADC14、DAC12和DOC）
	内部外围总线4	连接到外围模块（SCI、SPI、CRC和GPT）
	内部外围总线5	连接到外围模块（KINT、AGT、USBFS、OPAMP、ACMPLP、DAC8、SLCDC和CTSU）
	内部外围总线7	连接到SecureIP
	内部外围总线9	连接到闪存（在PE中）*1和数据闪存

Note 1. P/E = Programming/Erasure.

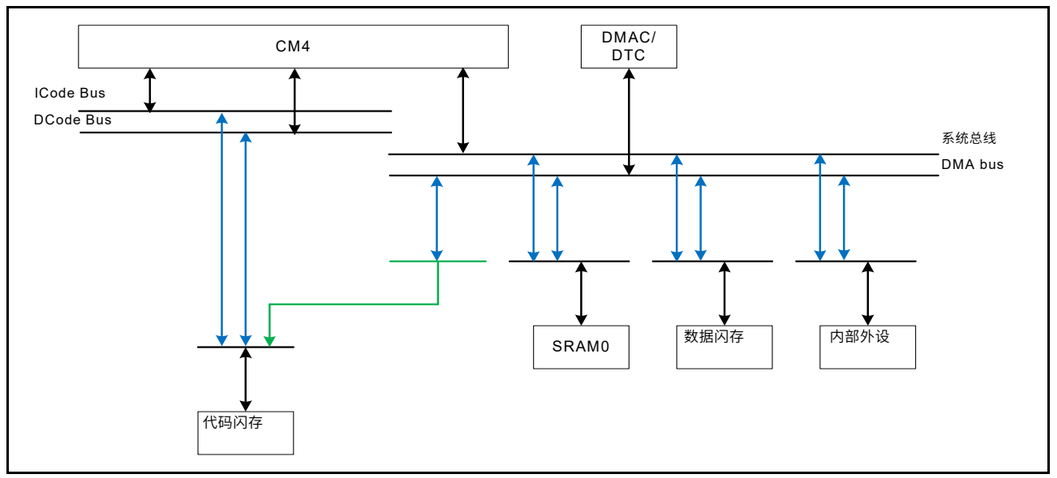


Figure 15.1 总线配置

Table 15.2 Addresses assigned for each bus

Address	Bus	Area
0000 0000h to 01FF FFFFh	Memory bus 1, 3	Code flash memory
2000 0000h to 2001 7FFFh	Memory bus 4	SRAM0
4000 0000h to 4001 FFFFh	Internal peripheral bus 1	Peripheral I/O registers
4004 0000h to 4005 FFFFh	Internal peripheral bus 3	
4006 0000h to 4007 FFFFh	Internal peripheral bus 4	
4008 0000h to 4009 FFFFh	Internal peripheral bus 5	
400C 0000h to 400D FFFFh	Internal peripheral bus 7	Secure IPs
4010 0000h to 407F FFFFh	Internal peripheral bus 9	Flash memory (in P/E)*1 and data flash memory

Note 1. P/E = Programming/Erasure.

15.2 Description of Buses

15.2.1 Main Buses

The main buses for the CPU consist of the ICode bus, DCode bus, and system bus.

- The ICode bus and the DCode bus are connected to the code flash memory. The ICode bus is used for instruction access to the CPU and the DCode bus is used for data access to the CPU.
- The system bus is connected to SRAM0, the data flash memory, and the internal peripheral bus. The system bus is used for instruction and data accesses to the CPU.

The main bus for modules other than the CPU consists of the DMA bus. The DMA bus is connected to the code flash memory, SRAM0, data flash memory, internal peripheral bus.

Different master and slave transfer combinations can proceed simultaneously.

Arbitration between DMAC and DTC for the mastership of the DMA bus occurs in the DMAC and DTC. The following fixed-priority order is used:

DMAC0, DMAC1, DMAC2, DMAC3, then DTC.

Only one DTC and DMAC channels that have accepted the activation requests can issue the bus mastership request. In addition, requests for bus access from masters other than the DTC are not accepted during reads of transfer control information for the DTC.

15.2.2 Slave Interface

Product using the Cortex®-M4 core contain ICode and DCode bus areas and a system bus area. To create the ICode and DCode bus areas, a bus matrix connects the ICode bus, the DCode bus, and the Memory bus 3 from the main bus to the slave interface of the code flash memory. To create a system bus area, a bus matrix connects the system bus and DMA bus from the main bus to the slave interfaces of SRAM0, the data flash memory, and the internal peripheral bus. For connections from the main bus to the slave interfaces, see the slave interfaces in Table 15.1.

Arbitration between the ICode bus, the DCode bus, and the Memory bus 3 occurs in the slave interface of the ICode and the DCode bus areas. The arbitration method is selectable from fixed priority and round-robin. For more information, see section 15.3.2.

Arbitration between the system bus and DMA bus occurs in the slave interface of the system bus area. The arbitration method is selectable from fixed priority and round-robin. For more information, see section 15.3.2.

Different master and slave transfer combinations can proceed simultaneously.

15.2.3 Parallel Operation

Parallel operation is possible when different bus masters request access to different slave modules. For example, if the CPU fetches an instruction from the flash and an operand from the SRAM, the DMAC can handle transfers from a peripheral bus at the same time.

Table 15.2 为每条总线分配的地址

Address	Bus	Area
0000 0000h to 01FF FFFFh	内存总线1、3	代码闪存
2000 0000h to 2001 7FFFh	内存总线4	SRAM0
4000 0000h to 4001 FFFFh	内部外围总线1	外设IO寄存器
4004 0000h to 4005 FFFFh	内部外围总线3	
4006 0000h to 4007 FFFFh	内部外围总线4	
4008 0000h to 4009 FFFFh	内部外围总线5	
400C 0000h to 400D FFFFh	内部外围总线7	安全IP
4010 0000h to 407F FFFFh	内部外围总线9	闪存（在PE中）*1和数据闪存

Note 1. P/E = Programming/Erasure.

15.2 巴士的描述

15.2.1 主要巴士

CPU的主要总线包括ICode总线、DCode总线和系统总线。

- ICode总线和DCode总线连接到代码闪存。ICode总线用于对CPU的指令访问，而DCode总线用于对CPU的数据访问。
- 系统总线连接到SRAM0、数据闪存和内部外围总线。系统总线用于对CPU的指令和数据访问。

CPU以外的模块的主总线由DMA总线组成。DMA总线连接到代码闪存、SRAM0、数据闪存、内部外设总线。

不同的主从传输组合可以同时进行。

DMAC和DTC之间对DMA总线的主控权的仲裁发生在DMAC和DTC中。使用以下固定优先级顺序：

DMAC0, DMAC1, DMAC2, DMAC3, then DTC.

只有一个接受激活请求的DTC和DMAC通道可以发出总线主控请求。此外，在读取DTC的传输控制信息期间，不接受来自DTC以外的主机的总线访问请求。

15.2.2 从接口

使用Cortex®-M4内核的产品包含ICode和DCode总线区域以及一个系统总线区域。为了创建ICode和DCode总线区域，总线矩阵将ICode总线、DCode总线和存储器总线3从主总线连接到代码闪存的从接口。为了创建系统总线区域，总线矩阵将系统总线和DMA总线从主总线连接到SRAM0的从接口、数据闪存和内部外围总线。对于从主总线到从接口的连接，请参见表15.1中的从接口。

ICode总线、DCode总线和Memory总线3之间的仲裁发生在ICode的从接口和DCode总线区域中。仲裁方法可以从固定优先级和循环中选择。有关详细信息，请参阅第15.3.2节。

系统总线和DMA总线之间的仲裁发生在系统总线区域的从接口中。仲裁方法可以从固定优先级和循环中选择。有关详细信息，请参阅第15.3.2节。

不同的主从传输组合可以同时进行。

15.2.3 并联运行

当不同的总线主机请求访问不同的从模块时，并行操作是可能的。例如，如果CPU从闪存中获取指令并从SRAM中获取操作数，DMAC可以同时处理来自外设总线的传输。

Figure 15.2 shows an example of parallel operations. In this example, the CPU uses the instruction and operand buses for simultaneous access to the flash and SRAM, respectively. Additionally, the DMAC/DTC simultaneously use the DMA bus for access to a peripheral bus during access to the flash and SRAM by the CPU.

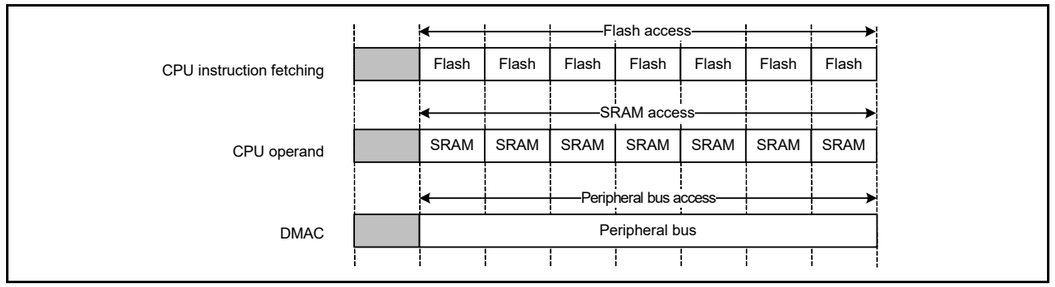


Figure 15.2 Example of parallel operations

15.2.4 Restriction on Endianness

Memory space must be little-endian to execute code on the Cortex®-M4 core.

15.3 Register Descriptions

15.3.1 Master Bus Control Register (BUSMCNT<master>)

Address(es): BUS.BUSMCNTM4I 4000 4000h, BUS.BUSMCNTM4D 4000 4004h, BUS.BUSMCNTSYS 4000 4008h, BUS.BUSMCNTDMA 4000 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	IERES	Ignore Error Responses	0: A bus error is reported 1: A bus error is not reported.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

IERES bit (Ignore Error Responses)

The IERES bit specifies the enable or disable of an error response of the AHB-Lite protocol.

Table 15.3 lists the registers associated with each bus type.

图15.2显示了并行操作的示例。在本例中，CPU使用指令和操作数总线分别同时访问闪存和SRAM。此外，在CPU访问闪存和SRAM期间，DMACDTC同时使用DMA总线访问外围总线。

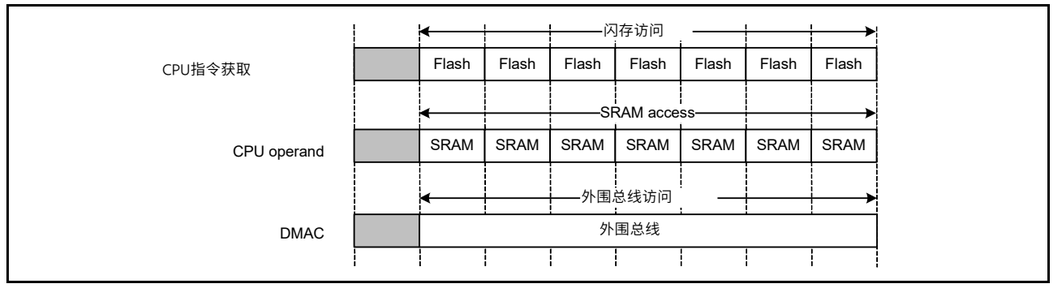


Figure 15.2 并行操作示例

15.2.4 字节序限制

内存空间必须是little-endian才能在Cortex®-M4内核上执行代码。

15.3 注册说明

15.3.1 主总线控制寄存器(BUSMCNT<master>)

Address(es): BUS.BUSMCNTM4I 4000 4000h, BUS.BUSMCNTM4D 4000 4004h, BUS.BUSMCNTSYS 4000 4008h, BUS.BUSMCNTDMA 4000 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b14 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	IERES	忽略错误响应	0：上报总线错误1：不上报总线错误。	R/W

Note: 禁止从初始值0更改保留位。不保证更改期间的操作。

IERES位（忽略错误响应）

IERES位指定启用或禁用AHB-Lite协议的错误响应。

表15.3列出了与每种总线类型相关的寄存器。

Table 15.3 Associations between bus types and registers

Bus type	Master Bus Control Register	Slave Bus Control Register	Bus Error Address Register	Bus Error Status Register
ICode bus (CPU)	BUSMCNTM4I	-	BUS1ERRADD	BUS1ERRSTAT
DCode bus (CPU)	BUSMCNTM4D	-	BUS2ERRADD	BUS2ERRSTAT
System bus (CPU)	BUSMCNTSYS	-	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	-	BUS4ERRADD	BUS4ERRSTAT
Memory bus 1	-	BUSSCNTFLI	-	-
Memory bus 3	-	BUSSCNTMBIU	-	-
Memory bus 4	-	BUSSCNTRAM0	-	-
Internal peripheral bus 1, 3, 4, 5, 7	-	BUSSCNTPnB [n = 0, 2, 3, 4, 6]	-	-
Internal peripheral bus 9	-	BUSSCNTFBU	-	-

15.3.2 Slave Bus Control Register (BUSSCNT<slave>)

Address(es): BUS.BUSSCNTFLI 4000 4100h, BUS.BUSSCNTMBIU 4000 4108h, BUS.BUSSCNTRAM0 4000 410Ch, BUS.BUSSCNTP0B 4000 4114h, BUS.BUSSCNTP2B 4000 4118h, BUS.BUSSCNTP3B 4000 411Ch, BUS.BUSSCNTP4B 4000 4120h, BUS.BUSSCNTP6B 4000 4128h, BUS.BUSSCNTFBU 4000 4130h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	—	—	ARBMET[1:0]		—	—	—	—
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	ARBMET[1:0]	Arbitration Method	Specify the priority between groups: b5 b4 0 0: Fixed priority 0 1: Round-robin 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

ARBMET[1:0] bits (Arbitration Method)

The ARBMET[1:0] bits specify the arbitration method, with priority defined for all bus masters. For fixed priority, see Table 15.4. For round-robin, see Table 15.5. For the associations between bus types and registers, see Table 15.3.

Table 15.4 Fixed priority (ARBMET[1:0] = 00b)

Slave Bus Control Register	Slave interface	Priority
BUSSCNTFLI	Memory bus 1	Memory bus 3 > DCode bus (CPU) > ICode bus (CPU)
BUSSCNTRAM0	Memory bus 4	DMA bus > System bus (CPU)
BUSSCNTPnB [n = 0, 2, 3, 4, 6]	Internal peripheral bus 1, 3, 4, 5, 7	DMA bus > System bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	DMA bus > System bus (CPU)

Table 15.3 总线类型和寄存器之间的关联

巴士类型	主总线控制 Register	从总线控制 Register	总线错误地址 Register	总线错误状态 Register
ICode bus (CPU)	BUSMCNTM4I	-	BUS1ERRADD	BUS1ERRSTAT
DCode bus (CPU)	BUSMCNTM4D	-	BUS2ERRADD	BUS2ERRSTAT
系统总线(CPU)	BUSMCNTSYS	-	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	-	BUS4ERRADD	BUS4ERRSTAT
内存总线1	-	BUSSCNTFLI	-	-
内存总线3	-	BUSSCNTMBIU	-	-
内存总线4	-	BUSSCNTRAM0	-	-
内部外围总线1、3、4、5、7	-	BUSSCNTPnB [n = 0, 2, 3, 4, 6]	-	-
内部外围总线9	-	BUSSCNTFBU	-	-

15.3.2 从总线控制寄存器(BUSSCNT<slave>)

Address(es): BUS.BUSSCNTFLI 4000 4100h, BUS.BUSSCNTMBIU 4000 4108h, BUS.BUSSCNTRAM0 4000 410Ch, BUS.BUSSCNTP0B 4000 4114h, BUS.BUSSCNTP2B 4000 4118h, BUS.BUSSCNTP3B 4000 411Ch, BUS.BUSSCNTP4B 4000 4120h, BUS.BUSSCNTP6B 4000 4128h, BUS.BUSSCNTFBU 4000 4130h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	—	—	ARBMET[1:0]		—	—	—	—
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

重置后的值:

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	ARBMET[1:0]	仲裁方式	指定组间优先级：b5b400：固定优先级01：循环10：禁止设置11：禁止设置。	R/W
b15 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 禁止从初始值0更改保留位。不保证更改期间的操作。

ARBMET[1:0]位（仲裁方法）

ARBMET[1:0]位指定仲裁方法，并为所有总线主机定义优先级。对于固定优先级，请参阅表15.4。对于循环，请参见表15.5。总线类型与寄存器的关联见表15.3。

Table 15.4 固定优先级（ARBMET[1:0]=00b）

从总线控制寄存器	从接口	Priority
BUSSCNTFLI	内存总线1	内存总线3>DCode总线(CPU)> ICode bus (CPU)
BUSSCNTRAM0	内存总线4	DMA总线>系统总线(CPU)
BUSSCNTPnB [n = 0, 2, 3, 4, 6]	内部外围总线1、3、4、5、7	DMA总线>系统总线(CPU)
BUSSCNTFBU	内部外围总线9	DMA总线>系统总线(CPU)

Table 15.5 Round-robin priority (ARBMET[1:0] = 01b)

Slave Bus Control Register	Slave interface	Priority "↔": Round-robin
BUSSCNTFLI	Memory bus 1	Memory bus 3 ↔ DCode bus (CPU) ↔ ICode bus (CPU)
BUSSCNTRAM0	Memory bus 4	DMA bus ↔ System bus (CPU)
BUSSCNTPnB [n = 0, 2, 3, 4, 6]	Internal peripheral bus 1, 3, 4, 5, 7	DMA bus ↔ System bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	DMA bus ↔ System bus (CPU)

15.3.3 Bus Error Address Register (BUSnERRADD) (n = 1 to 4)

Address(es): BUS.BUS1ERRADD 4000 4800h, BUS.BUS2ERRADD 4000 4810h, BUS.BUS3ERRADD 4000 4820h, BUS.BUS4ERRADD 4000 4830h

	b31	b30	b29	b28	b27	b26	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]														
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Bit name	Description	R/W
b31 to b0	BERAD[31:0]	Bus Error Address	When a bus error occurs, these bits store the error address	R

Note: This register is only cleared by resets other than MPU related resets. For more information, see section 6, Resets and section 16, Memory Protection Unit (MPU).

Table 15.3 lists the registers associated with each bus type.

BERAD[31:0] bits (Bus Error Address)

The BERAD[31:0] bits store the accessed address when a bus error occurred. For more information, see BUSnERRSTAT.ERRSTAT and section 15.4, Bus Error Monitoring Section.

The value of the BUSnERRADD.BERAD[31:0] bits (n = 1 to 4) is valid only when BUSnERRSTAT.ERRSTAT bit (n = 1 to 4) is set to 1.

15.3.4 Bus Error Status Register (BUSnERRSTAT) (n = 1 to 4)

Address(es): BUS.BUS1ERRSTAT 4000 4804h, BUS.BUS2ERRSTAT 4000 4814h, BUS.BUS3ERRSTAT 4000 4824h, BUS.BUS4ERRSTAT 4000 4834h

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	—	—	—	—	—	—	ACCSTAT
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Bit name	Description	R/W
b0	ACCSTAT	Error Access Status	Access status when the error occurred: 1: Write access 0: Read access.	R
b6 to b1	—	Reserved	These bits are read as 0	R

Table 15.5 Round-robin priority (ARBMET[1:0] = 01b)

从总线控制寄存器	从接口	Priority "↔": Round-robin
BUSSCNTFLI	内存总线1	内存总线3 DCode总线(CPU) ICode bus (CPU)
BUSSCNTRAM0	内存总线4	DMA总线 系统总线(CPU)
BUSSCNTPnB [n = 0, 2, 3, 4, 6]	内部外围总线1、3、4、5、7	DMA总线 系统总线(CPU)
BUSSCNTFBU	内部外围总线9	DMA总线 系统总线(CPU)

15.3.3 总线错误地址寄存器(BUSnERRADD)(n=1到4)

Address(es): BUS.BUS1ERRADD 4000 4800h, BUS.BUS2ERRADD 4000 4810h, BUS.BUS3ERRADD 4000 4820h, BUS.BUS4ERRADD 4000 4830h

	b31	b30	b29	b28	b27	b26	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]														
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	位名称	Description	R/W
b31 to b0	BERAD[31:0]	总线错误地址	当发生总线错误时，这些位存储错误地址	R

Note: 该寄存器仅由MPU相关复位以外的复位清除。有关详细信息，请参阅第6节，复位和第16节，内存保护单元(MPU)。

表15.3列出了与每种总线类型相关的寄存器。

BERAD[31:0]位（总线错误地址）

BERAD[31:0]位存储发生总线错误时访问的地址。有关详细信息，请参阅BUSnERRSTAT.ERRSTAT和第15.4节，总线错误监控部分。

BUSnERRADD.BERAD[31:0]位（n=1至4）的值仅在BUSnERRSTAT.ERRSTAT位（n=1至4）设置为1时有效。

15.3.4 总线错误状态寄存器(BUSnERRSTAT)(n=1到4)

Address(es): BUS.BUS1ERRSTAT 4000 4804h, BUS.BUS2ERRSTAT 4000 4814h, BUS.BUS3ERRSTAT 4000 4824h, BUS.BUS4ERRSTAT 4000 4834h

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	—	—	—	—	—	—	ACCSTAT
重置后的值:	0	0	0	0	0	0	0	x

Bit	Symbol	位名称	Description	R/W
b0	ACCSTAT	错误访问状态	发生错误时的访问状态：1：写访问0：读访问。	R
b6 to b1	—	Reserved	这些位被读为0	R

Bit	Symbol	Bit name	Description	R/W
b7	ERRSTAT	Bus Error Status	0: No bus error occurred 1: Bus error occurred.	R

Note: This register is only cleared by resets other than MPU-related resets. For more information, see section 6, Resets and section 16, Memory Protection Unit (MPU).

Table 15.3 lists the registers associated with each bus type.

ACCSTAT bit (Error Access Status)

The ACCSTAT bit indicates the access status, write access or read access, when a bus error occurs. For more information, see BUSnERRSTAT.ERRSTAT and section 15.4, Bus Error Monitoring Section.

The value is valid only when the BUSnERRSTAT.ERRSTAT bit (n = 1 to 4) is set to 1.

ERRSTAT bit (Bus Error Status)

The ERRSTAT bit indicates whether a bus error occurred. When an error occurs, the access address and status of write or read access are stored. The BUSnERRSTAT.ERRSTAT bit (n = 1 to 4) is set to 1.

Four types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Time out.

When detecting bus master MPU errors or bus slave MPU errors, and reset is selected in the OAD bit, if the bus access that caused the MPU error completes later than the internal reset signal being generated, which can occur with the wait setting, BUSnERRSTAT.ERRSTAT (n = 1 to 4) is not set to 1.

When detecting bus master MPU errors or bus slave MPU errors, and NMI is selected in the OAD bit, BUSnERRSTAT.ERRSTAT (n = 1 to 4) is set to 1 after the bus access that caused the MPU error completes.

For more information on bus errors, see section 15.4, Bus Error Monitoring Section, and section 16, Memory Protection Unit (MPU).

15.4 Bus Error Monitoring Section

This monitoring system monitors each individual area, and whenever it detects an error, it returns the error to the requesting master IP using the AHB-Lite error response protocol.

15.4.1 Error Type that Occurs by Bus

Four types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Timeout.

Table 15.6 lists the address ranges where access leads to illegal address access errors. However, the reserved area in the slave does not trigger an illegal address access error. For more information on bus master MPU and bus slave MPU, see section 16, Memory Protection Unit (MPU).

15.4.2 Operation when a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP. The bus error information occurred in each master is stored in the BUSnERRADD and BUSnERRSTAT registers. These registers must be cleared by reset only. For more information, see sections 15.3.3 and 15.3.4.

Bit	Symbol	位名称	Description	R/W
b7	ERRSTAT	总线错误状态	0：未发生总线错误1： 发生总线错误。	R

Note: 该寄存器仅由MPU相关复位以外的复位清除。有关详细信息，请参阅第6节，复位和第16节，内存保护单元(MPU)。

表15.3列出了与每种总线类型相关的寄存器。

ACCSTAT位（错误访问状态）

当发生总线错误时，ACCSTAT位指示访问状态、写访问或读访问。有关详细信息，请参阅BUSnERRSTAT.ERRSTAT和第15.4节，总线错误监视部分。

该值仅在BUSnERRSTAT.ERRSTAT位（n=1至4）设置为1时有效。

ERRSTAT位（总线错误状态）

ERRSTAT位指示是否发生总线错误。当发生错误时，存储访问地址和写入或读取访问的状态。BUSnERRSTAT.ERRSTAT位（n=1到4）设置为1。

每条总线上可能出现四种类型的错误：

- 非法地址访问
- 总线主控MPU错误
- 总线从机MPU错误
- 暂停。

当检测到总线主控MPU错误或总线从属MPU错误，并且在OAD位中选择复位时，如果导致MPU错误的总线访问完成晚于内部复位信号生成，这可能与等待设置BUSnERRSTAT一起发生。ERRSTAT（n=1到4）未设置为1。

当检测到总线主控MPU错误或总线从属MPU错误，并且在OAD位中选择NMI，在导致MPU错误的总线访问完成后，BUSnERRSTAT.ERRSTAT（n=1到4）设置为1。

有关总线错误的更多信息，请参阅第15.4节，总线错误监控部分和第16节，内存保护Unit (MPU).

15.4 总线错误监控部分

该监控系统监控每个单独的区域，当它检测到错误时，它会使用AHB-Lite错误响应协议将错误返回给请求的主IP。

15.4.1 总线发生的错误类型

每条总线上可能出现四种类型的错误：

- 非法地址访问
- 总线主控MPU错误
- 总线从机MPU错误
- Timeout.

表15.6列出了访问导致非法地址访问错误的地址范围。但是，从机中的保留区域不会触发非法地址访问错误。有关总线主MPU和总线从MPU的更多信息，请参阅第16节，内存保护单元(MPU)。

15.4.2 发生总线错误时的操作

当发生总线错误时，无法保证操作，错误会返回到请求的主IP。每个主机中发生的总线错误信息存储在BUSnERRADD和BUSnERRSTAT寄存器中。这些寄存器只能通过复位来清除。有关详细信息，请参阅第15.3.3和15.3.4节。

Note: The DMAC and DTC do not receive bus errors. If the DMAC or DTC accesses the bus, the transfer continues.

15.4.3 Conditions Leading to Illegal Address Access Errors

Table 15.6 lists the address spaces for each bus that trigger illegal address access errors.

Table 15.6 Conditions leading to illegal address access errors

Address	Slave bus name	Master bus	
		CPU (ICode/DCode/ System)	DMA
0000 0000h to 01FF FFFFh	Memory bus 1 Memory bus 3	—	—
0200 0000h to 027F FFFFh	Memory mirror area	*1	E
0280 0000h to 1FFF FFFFh	Reserved	E	E
2000 0000h to 2001 7FFFh	Memory bus 4	—	—
2001 8000h to 3FFF FFFFh	Reserved	E	E
4000 0000h to 4001 FFFFh	Peripheral bus 1	—	—
4002 0000h to 4003 FFFFh	Reserved	E	E
4004 0000h to 4005 FFFFh	Peripheral bus 3	—	—
4006 0000h to 4007 FFFFh	Peripheral bus 4	—	—
4008 0000h to 4009 FFFFh	Peripheral bus 5	—	—
400A 0000h to 400B FFFFh	Reserved	—	—
400C 0000h to 400D FFFFh	Peripheral bus 7	—	—
400E 0000h to 400F FFFFh	Reserved	E	E
4010 0000h to 407F FFFFh	Peripheral bus 9	—	—
4080 0000h to 5FFF FFFFh	Reserved	E	E
6000 0000h to 67FF FFFFh	Reserved	—	—
6800 0000h to 7FFF FFFFh	Reserved	E	E
8000 0000h to 97FF FFFFh	Reserved	—	—
9800 0000h to DFFF FFFFh	Reserved	E	E
E000 0000h to FFFF FFFFh	System for Cortex-M4	—	E

E indicates the path where an illegal address access error occurs.

— indicates the path where an illegal address access error does not occur or path that access does not occur.

Note: If MMF (Memory Mirror Function) is enabled, the access to mapped area (0200 0000h to 027F FFFFh) is switched to the user specific area (MMF output address = CPU output address + offset).
The bus module does not detect whether the MMF switched the address. Therefore if the MMF is enabled and the CPU accesses 0200 0000h, no error can occur (depends on the switched address). If the MMF is disabled and the CPU accesses 0200 0000h, the bus module can detect the error.

Note 1. The bus module does not detect whether the MMF switched the address. Therefore if the MMF is enabled and the CPU accesses 0200 0000h, no error occurs (depends on the switched address).
If the MMF is disabled and the CPU accesses 0200 0000h, the bus module can detect the error.

Note 2. The bus module detects an access error resulting from access to reserved area, for example if no area is assigned for the slave.
0280 0000h to 1FFF FFFFh: Access error detection.
0000 0000h to 01FF FFFFh: Memory bus 1 no access error detection.

15.4.4 Timeout

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain period of time, a timeout error is detected. A timeout error is returned to the requesting master IP using the AHB-Lite error response protocol.

Note: DMAC和DTC不接收总线错误。如果DMAC或DTC访问总线，则传输继续。

15.4.3 导致非法地址访问错误的条件

表15.6列出了触发非法地址访问错误的每条总线的地址空间。

Table 15.6 导致非法地址访问错误的条件

Address	从总线名称	主总线	
		CPU (ICode/DCode/ System)	DMA
0000 0000h to 01FF FFFFh	内存总线1内 存总线3	—	—
0200 0000h to 027F FFFFh	内存镜像区	*1	E
0280 0000h to 1FFF FFFFh	Reserved	E	E
2000 0000h to 2001 7FFFh	内存总线4	—	—
2001 8000h to 3FFF FFFFh	Reserved	E	E
4000 0000h to 4001 FFFFh	外围总线1	—	—
4002 0000h to 4003 FFFFh	Reserved	E	E
4004 0000h to 4005 FFFFh	外围总线3	—	—
4006 0000h to 4007 FFFFh	外围总线4	—	—
4008 0000h to 4009 FFFFh	周边总线5	—	—
400A 0000h to 400B FFFFh	Reserved	—	—
400C 0000h to 400D FFFFh	周边总线7	—	—
400E 0000h to 400F FFFFh	Reserved	E	E
4010 0000h to 407F FFFFh	周边总线9	—	—
4080 0000h to 5FFF FFFFh	Reserved	E	E
6000 0000h to 67FF FFFFh	Reserved	—	—
6800 0000h to 7FFF FFFFh	Reserved	E	E
8000 0000h to 97FF FFFFh	Reserved	—	—
9800 0000h to DFFF FFFFh	Reserved	E	E
E000 0000h to FFFF FFFFh	Cortex-M4系统	—	E

E表示发生非法地址访问错误的路径。

—表示不发生非法地址访问错误的路径或不发生访问的路径。

Note: 如果启用MMF（内存镜像功能），则对映射区域（02000000h到027FFFFFh）的访问切换到用户特定区域（MMF输出地址=CPU输出地址+偏移量）。总线模块不检测MMF是否切换了地址。因此，如果启用MMF并且CPU访问02000000h，则不会发生错误（取决于切换的地址）。如果MMF被禁用并且CPU访问02000000h，则总线模块可以检测到错误。

Note 1. 总线模块不检测MMF是否切换了地址。因此，如果启用MMF并且CPU访问02000000h，则不会发生错误（取决于切换的地址）。如果MMF被禁用并且CPU访问02000000h，则总线模块可以检测到错误。

Note 2. 总线模块检测到访问保留区域导致的访问错误，例如，如果没有为从站分配区域。02800000h至1FFFFFFFh：访问错误检测。00000000h至01FFFFFFh：内存总线1无访问错误检测。

15.4.4 Timeout

对于某些外围模块，模块停止功能会发生超时错误。当从机在一段时间内没有响应时，检测到超时错误。使用AHB-Lite错误响应协议将超时错误返回给请求的主IP。

15.5 Notes on using Flash Cache

When using flash cache by access from the CPU, Arm® MPU should also be set to cacheable. See references 1. and 2. for more information.

15.6 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D)
2. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A)
3. *ARM® AMBA® 3 AHB-Lite Protocol v1.0 Specification* (ARM IHI 0033A).

15.5 使用FlashCache的注意事项

当通过CPU访问使用闪存缓存时，Arm®MPU也应设置为可缓存。有关详细信息，请参阅参考文献1.和2.。

15.6 References

1. ARM®v7-M架构参考手册(ARMDDI0403D)
2. ARM®Cortex®-M4设备通用用户指南(ARMDUI0553A)
3. ARM®AMBA®3AHB-Lite协议v1.0规范(ARMIHI0033A)。

16. Memory Protection Unit (MPU)

16.1 Overview

The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function. Table 16.1 lists the supported MPU specifications, and Table 16.2 shows the behavior on detection of each MPU error.

Table 16.1 MPU specifications

Classification	Module/Function	Description
Illegal memory access	Arm® Cortex®-M4 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs. • The MPU can change a default memory map.
	CPU stack pointer monitor	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Memory protection	Arm MPU	Memory protection function for the CPU: • 8 MPU regions with subregions and background region.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • Bus master MPU group A: 16 regions.
	Bus slave MPU	Memory protection function for each bus slave
Security	Security MPU	Protects accesses from non-secure programs to the following secure regions: • 2 regions (PC) • 4 regions (code flash, SRAM, 2 secure functions).

Table 16.2 Behavior on MPU error detection

MPU type	Notification type	Bus access on error detection	Storing of error access information
CPU stack pointer monitor	Reset or non-maskable interrupt	Don't care	Not stored
Arm MPU	Hard fault	• Does not correctly have write access • Does not correctly have read access.	Stored in the Cortex-M4 processor
Bus master MPU	Reset or non-maskable interrupt	• Write access to the protection region • Read access to the protection region.	Stored
Bus slave MPU	• Reset or non-maskable interrupt • Hard fault	• Write access ignored • Read access is read as 0.	Stored
Security MPU	Not notified	• Does not correctly have write access • Does not correctly have read access.	Not stored

For information on error access for Arm MPU, see section 16.7. For information on error access for other MPUs, see 15.3.3 and 15.3.4 in section 15, Buses.

16.2 CPU Stack Pointer Monitor

The CPU stack pointer monitor detects underflows and overflows of the stack pointer. Because the Arm CPU has two stack pointers, a Main Stack Pointer (MSP) and a Process Stack Pointer (PSP), it supports two CPU stack pointer monitors. If a stack pointer underflow or overflow is detected, the CPU stack pointer monitor generates a reset or a non-maskable interrupt. The CPU stack pointer monitor is enabled by setting the Stack Pointer Monitor Enable bit in the Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL) to 1.

Table 16.3 lists the specifications of the CPU stack pointer monitor. Figure 16.1 shows a block diagram, and Figure 16.2 shows the register setting flow.

Table 16.3 CPU stack pointer monitor specifications (1 of 2)

Parameter	Description
SRAM region	Region to be covered by memory protection

16. 内存保护单元(MPU)

16.1 Overview

MCU具有四个内存保护单元(MPU)和一个CPU堆栈指针监控功能。表16.1列出了支持的MPU规格，表16.2显示了检测每个MPU错误的行为。

Table 16.1 MPU specifications

Classification	Module/Function	Description
非法内存访问	Arm®Cortex®-M4CPU	ArmCPU有一个默认的内存映射。如果CPU进行非法访问，则会发生异常中断。MPU可以更改默认内存映射。
	CPU堆栈指针监视器	2个区域： 主堆栈指针(MSP) 进程堆栈指针(PSP)。
内存保护	Arm MPU	CPU的内存保护功能： 8个带有子区域和背景区域的MPU区域。
	总线主控MPU	除CPU外的每个总线主控的内存保护功能： 总线主控MPU组A：16个区域。
	总线从机MPU	每个总线从机的内存保护功能
Security	Security MPU	保护非安全程序对以下安全区域的访问： 2个区域(PC) 4个区域（代码闪存、SRAM、2个安全功能）。

Table 16.2 MPU错误检测的行为

MPU type	通知类型	错误检测时的总线访问	存储错误访问信息
CPU堆栈指针监视器	复位或不可屏蔽中断	Don't care	未存储
Arm MPU	硬故障	没有正确的写入权限 没有正确的读取权限。	存储在Cortex-M4处理器中
总线主控MPU	复位或不可屏蔽中断	对保护区域的写访问权限 对保护区域的读访问权限。	Stored
总线从机MPU	复位或不可屏蔽中断 硬故障	写访问被忽略 读访问被读为0。	Stored
Security MPU	未通知	没有正确的写入权限 没有正确的读取权限。	未存储

有关ArmMPU的错误访问的信息，请参阅第16.7节。有关其他MPU的错误访问的信息，请参阅第15节"总线"中的15.3.3和15.3.4。

16.2 CPU堆栈指针监视器

CPU堆栈指针监视器检测堆栈指针的下溢和溢出。由于ArmCPU有两个堆栈指针，一个主堆栈指针(MSP)和一个进程堆栈指针(PSP)，因此它支持两个CPU堆栈指针监视器。如果检测到堆栈指针下溢或溢出，CPU堆栈指针监视器会生成复位或不可屏蔽中断。CPU堆栈指针监视器通过将堆栈指针监视器访问控制寄存器(MSPMPUCTL PSPMPUCTL)中的堆栈指针监视器启用位设置为1来启用。

表16.3列出了CPU堆栈指针监视器的规格。图16.1显示了框图，图16.2显示了寄存器设置流程。

Table 16.3 CPU堆栈指针监视器规格(1of2)

Parameter	Description
SRAM region	内存保护要覆盖的区域

Table 16.3 CPU stack pointer monitor specifications (2 of 2)

Parameter	Description
Number of regions	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Address specification for individual regions	Specifying start and end addresses for individual regions
Stack pointer monitor enable or disable setting for individual regions	Enabling or disabling stack pointer monitor for individual regions
Operation on error detection	Reset or non-maskable interrupts can be generated
Register protection	Protecting registers from illegal writes

Table 16.3 CPU堆栈指针监视器规格(2of2)

Parameter	Description
地区数量	2个区域： 主堆栈指针(MSP) 进程堆栈指针(PSP)。
个别地区的地址规范	为各个区域指定开始和结束地址
堆栈指针监视器启用或禁用各个区域的设置	启用或禁用各个区域的堆栈指针监视器
错误检测操作	可以产生复位或不可屏蔽中断
注册保护	保护寄存器免受非法写入

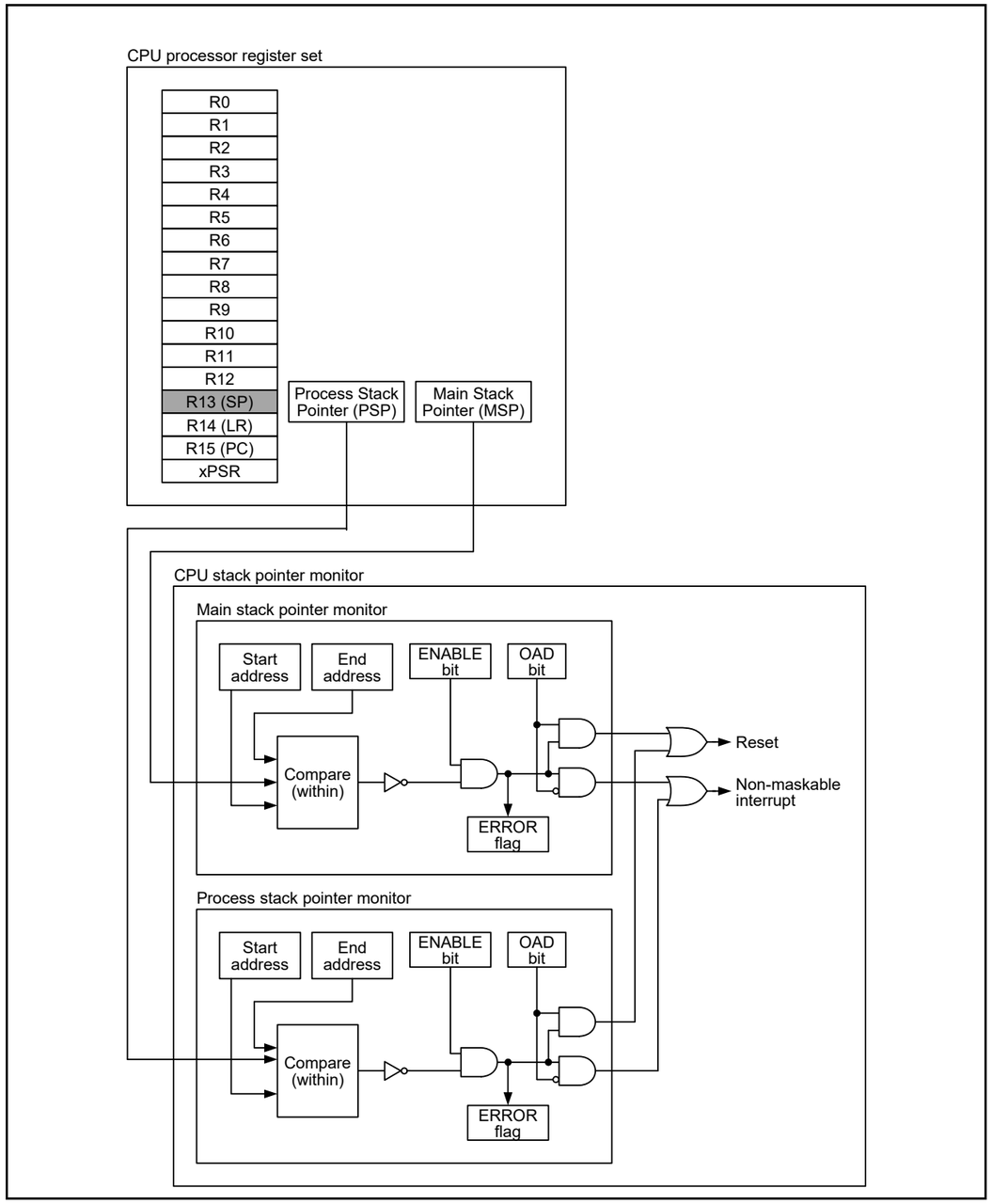


Figure 16.1 CPU stack pointer monitor block diagram

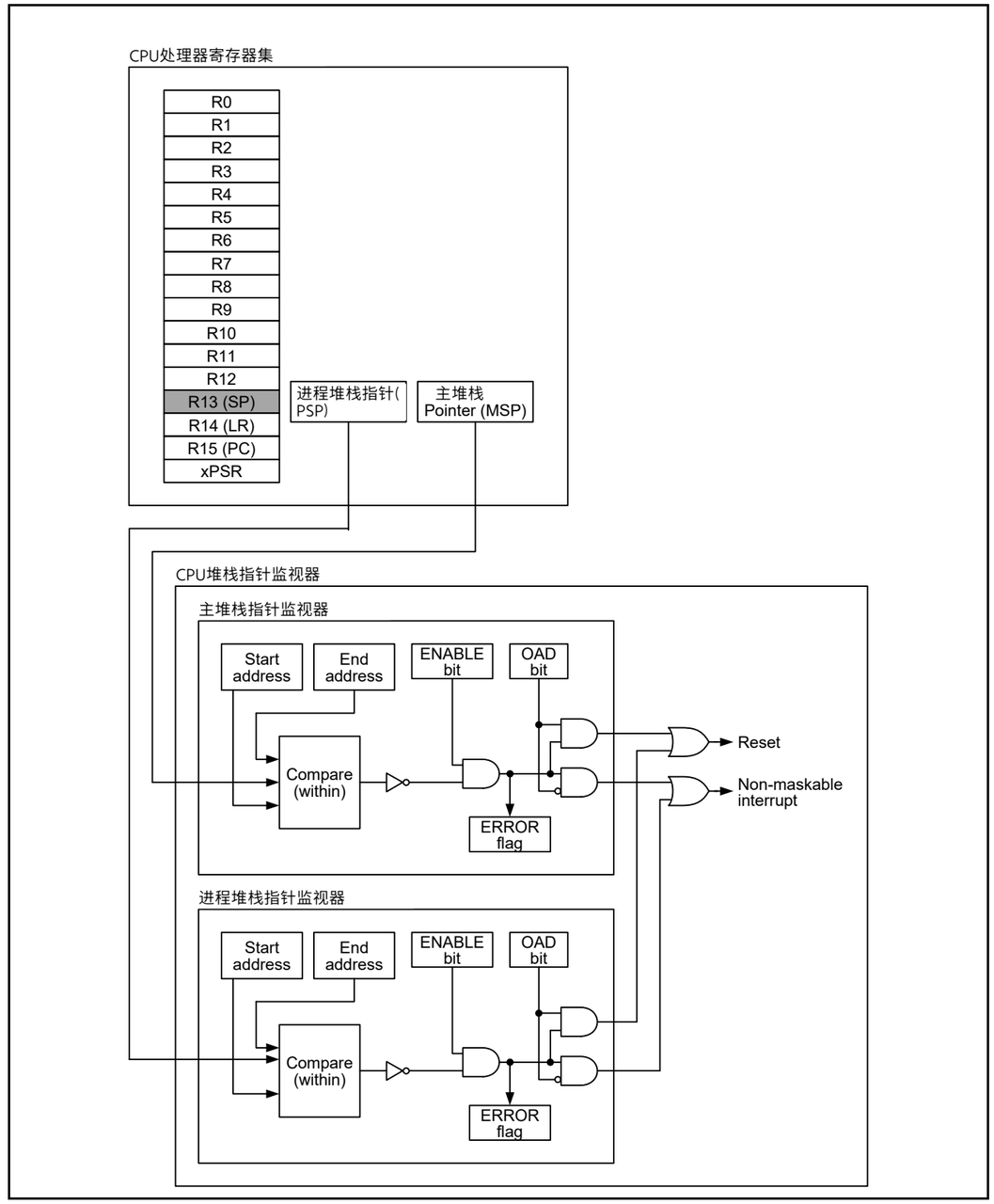


Figure 16.1 CPU堆栈指针监视器框图

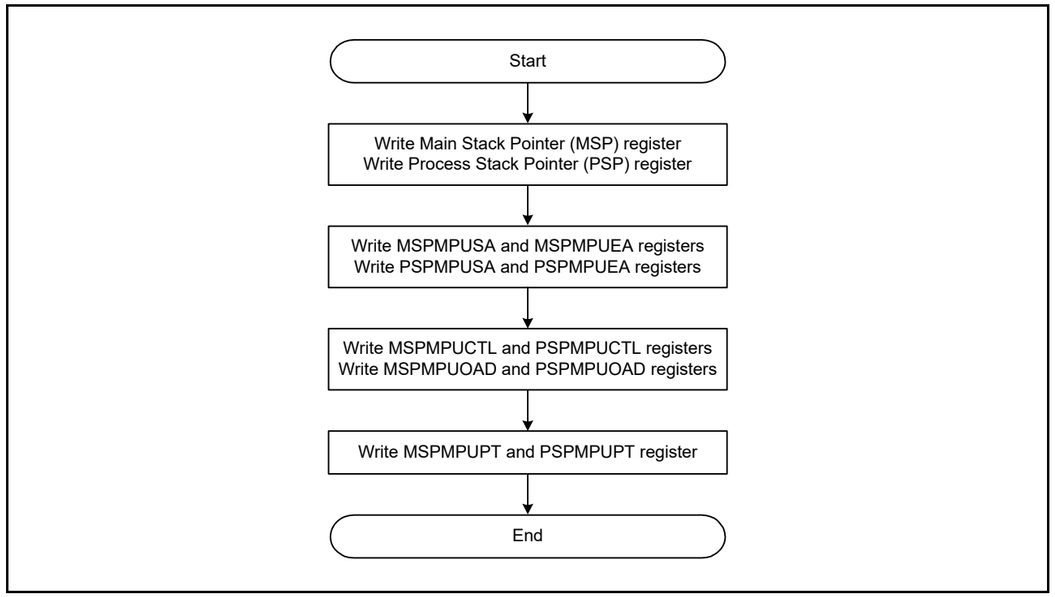


Figure 16.2 Register setting flow

16.2.1 Protection of Registers

Registers related to the CPU stack pointer monitor can be protected with the PROTECT bit.

16.2.2 Overflow/Underflow Error

If an overflow or underflow is detected, the CPU stack pointer monitor generates an overflow or underflow error. A memory protection error can choose between non-maskable interrupt or reset in the OAD bit setting.

The non-maskable interrupt status is indicated in ICU.NMISR.SPEST. For details, see section 14, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.SPERF. For details, see section 6, Resets.

When ICU.NMISR.SPEST indicates that a CPU stack pointer monitor interrupt occurred, check the ERROR bits in the MSPMPUCTL and PSPMPUCTL registers to determine whether it is a main stack pointer monitor error or a process stack pointer monitor error.

A non-maskable interrupt is generated continuously while the stack pointer overflows or underflows. To clear the non-maskable interrupt flag, set the stack pointer within the specified region and then clear the non-maskable interrupt flag by setting the ICU.NMICLR.SPECLR bit to 1. Then, write 0 to the ERROR bits in the MSPMPUCTL and PSPMPUCTL registers.

16.2.3 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

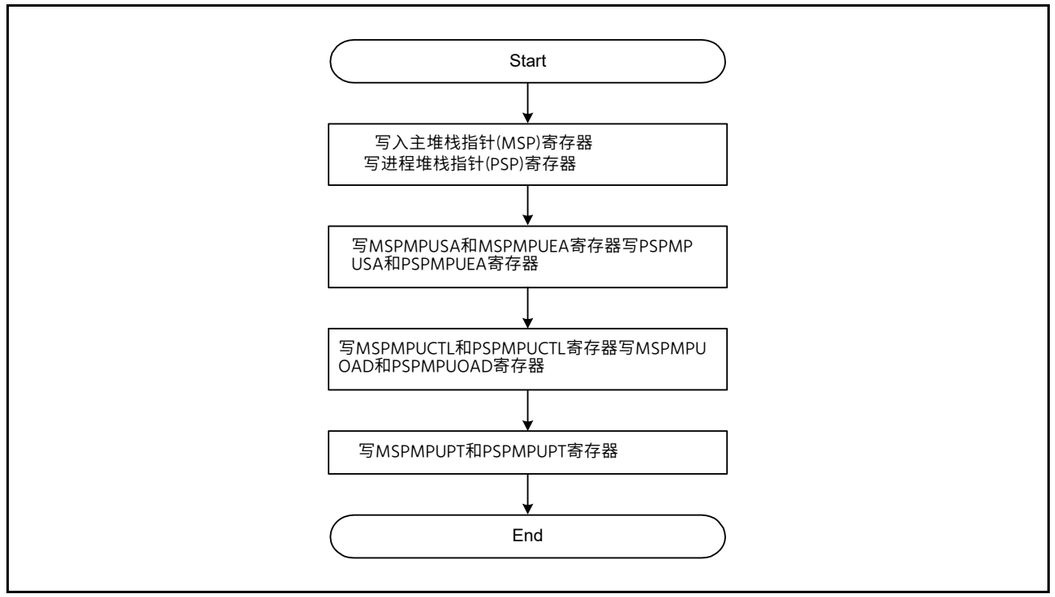


Figure 16.2 注册设置流程

16.2.1 保护寄存器

与CPU堆栈指针监视器相关的寄存器可以使用PROTECT位进行保护。

16.2.2 Overflow/Underflow Error

如果检测到上溢或下溢，CPU堆栈指针监视器会生成上溢或下溢错误。内存保护错误可以在OAD位设置中选择不可屏蔽中断或复位。

不可屏蔽中断状态在ICU.NMISR.SPEST中指示。有关详细信息，请参见第14节，中断控制器单位（ICU）。复位状态在SYSTEM.RSTSR1.SPERF中指示。有关详细信息，请参阅第6节，重置。

当ICU.NMISR.SPEST指示发生CPU堆栈指针监视器中断时，检查MSPMPUCTL和PSPMPUCTL寄存器来确定是主堆栈指针监视器错误还是进程堆栈指针监视器错误。

当堆栈指针上溢或下溢时，会连续产生一个不可屏蔽的中断。要清除不可屏蔽中断标志，请将堆栈指针设置在指定区域内，然后通过将ICU.NMICLR.SPECLR位设置为1来清除不可屏蔽中断标志。然后，将0写入MSPMPUCTL和PSPMPUCTL寄存器中的ERROR位.

16.2.3 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

16.2.3.1 Main Stack Pointer (MSP) Monitor Start Address Register (MSPMPUSA)

Address(es): SPMON.MSPMPUSA 4000 0D08h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range is from 2000 0000h to 200F FFFCh, excluding reserved areas.	R/W

The MSPMPUSA and MSPMPUEA registers specify the CPU stack region of SRAM (2000 0000h to 200F FFFFh, excluding reserved areas). For SRAM area to be covered, see Figure 4.1, Memory map.

16.2.3.2 Main Stack Pointer (MSP) Monitor End Address Register (MSPMPUEA)

Address(es): SPMON.MSPMPUEA 4000 0D0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range must be 2000 0003h to 200F FFFFh, excluding reserved areas.	R/W

16.2.3.1 主堆栈指针(MSP)监视器起始地址寄存器(MSPMPUSA)

Address(es): SPMON.MSPMPUSA 4000 0D08h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUSA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUSA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MSPMPUSA[31:0]	区域起始地址	区域开始的地址，用于区域确定。 低2位应为0。取值范围为20000000h到200FFFFCh，不包括保留区。	R/W

MSPMPUSA和MSPMPUEA寄存器指定SRAM的CPU堆栈区域（20000000h到200FFFFFh，不包括保留区域）。对于要覆盖的SRAM区域，请参见图4.1，存储器映射。

16.2.3.2 主堆栈指针(MSP)监视器结束地址寄存器(MSPMPUEA)

Address(es): SPMON.MSPMPUEA 4000 0D0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUEA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUEA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MSPMPUEA[31:0]	区域结束地址	区域结束的地址，用于区域确定。 低2位应为1。取值范围必须为20000003h到200FFFFFh，不包括保留区域。	R/W

16.2.3.3 Process Stack Pointer (PSP) Monitor Start Address Register (PSPMPUSA)

Address(es): SPMON.PSPMPUSA 4000 0D18h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range must be 2000 0000h to 200F FFFCh, excluding reserved areas.	R/W

The PSPMPUSA and PSPMPUEA registers specify the CPU stack region of SRAM (2000 0000h to 200F FFFFh, excluding reserved areas). For SRAM area to be covered, see Figure 4.1, Memory map.

16.2.3.4 Process Stack Pointer (PSP) Monitor End Address Register (PSPMPUEA)

Address(es): SPMON.PSPMPUEA 4000 0D1Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 2000 0003h to 200F FFFFh, excluding reserved areas.	R/W

16.2.3.3 进程堆栈指针(PSP)监视器起始地址寄存器(PSPMPUSA)

Address(es): SPMON.PSPMPUSA 4000 0D18h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUSA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUSA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	PSPMPUSA[31:0]	区域起始地址	区域开始的地址，用于区域确定。 低2位应为0。取值范围必须为20000000h到200FFFFCh，不包括保留区。	R/W

PSPMPUSA和PSPMPUEA寄存器指定SRAM的CPU堆栈区域（20000000h到200FFFFFh，不包括保留区域）。对于要覆盖的SRAM区域，请参见图4.1，存储器映射。

16.2.3.4 进程堆栈指针(PSP)监视器结束地址寄存器(PSPMPUEA)

Address(es): SPMON.PSPMPUEA 4000 0D1Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUEA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUEA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	PSPMPUEA[31:0]	区域结束地址	区域结束的地址，用于区域确定。 低2位应为1。取值范围为20000003h到200FFFFFh，不包括保留区。	R/W

16.2.3.5 Stack Pointer Monitor Operation After Detection Register (MSPMPUOAD, PSPMPUOAD)

Address(es): SPMON.MSPMPUOAD 4000 0D00h, SPMON.PSPMPUOAD 4000 0D10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD bit	R/(W)*1

Note 1. Write data is not saved.

OAD bit (Operation after Detection)

The OAD bit selects either a reset or a non-maskable interrupt to occur when a stack pointer underflow or overflow is detected by the CPU stack pointer monitor. The main and the process stack pointer monitors each uses an OAD bit to determine which signal is generated when a stack pointer underflow or overflow is detected. Write A5h in KEY[7:0] bits in halfword access simultaneously when setting the OAD bit.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD bit. When writing to the OAD bit, simultaneously write A5h to KEY[7:0]. When values other than A5h are written to the KEY[7:0] bits, the OAD bit is not updated. The KEY[7:0] bits are always read as 00h.

16.2.3.6 Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL)

Address(es): SPMON.MSPMPUCTL 4000 0D04h, SPMON.PSPMPUCTL 4000 0D14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Stack Pointer Monitor Enable	0: Stack pointer monitor is disabled 1: Stack pointer monitor is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ERROR	Stack Pointer Monitor Error Flag	0: Stack pointer has not overflowed or underflowed 1: Stack pointer has overflowed or underflowed.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value depends on the reset generation sources.

ENABLE bit (Stack Pointer Monitor Enable)

The ENABLE bit enables or disables the stack pointer monitor function, independently set for the main stack pointer monitor and the process stack pointer monitor.

When the MSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- MSPMPUSA

16.2.3.5 检测寄存器后的堆栈指针监视器操作（MSPPUOAD，PSPMPUOAD）

Address(es): SPMON.MSPMPUOAD 4000 0D00h, SPMON.PSPMPUOAD 4000 0D10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后的操作	0：不可屏蔽中断1：复位 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对OAD位的写入	R/(W)*1

Note 1. 不保存写入数据。

OAD位（检测后操作）

当CPU堆栈指针监视器检测到堆栈指针下溢或溢出时，OAD位选择发生复位或不可屏蔽中断。主堆栈指针监视器和进程堆栈指针监视器各自使用一个OAD位来确定在检测到堆栈指针下溢或溢出时生成哪个信号。在设置OAD位时，同时在半字访问中将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对OAD位的写入。写入OAD位时，同时将A5h写入KEY[7:0]。将A5h以外的值写入KEY[7:0]位时，不会更新OAD位。KEY[7:0]位总是读为00h。

16.2.3.6 堆栈指针监视器访问控制寄存器(MSMPPUCTL PSPMPUCTL)

Address(es): SPMON.MSPMPUCTL 4000 0D04h, SPMON.PSPMPUCTL 4000 0D14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
重置后的值：	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENABLE	堆栈指针监视器 Enable	0：堆栈指针监视器禁用1：堆栈指 针监视器启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	ERROR	堆栈指针监视器 错误标志	0：堆栈指针未上溢或下溢1：堆栈指针已上溢或下 溢。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 初始值取决于复位产生源。

ENABLE位（堆栈指针监视器启用）

ENABLE位启用或禁用堆栈指针监视器功能，分别为主堆栈指针监视器和进程堆栈指针监视器设置。

当MSMPPUCTL.ENABLE位设置为1时，以下寄存器可用：

- MSPMPUSA

- MSPMPUEA
- MSPMPUOAD.

When the PSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR bit (Stack Pointer Monitor Error Flag)

The ERROR bit indicates the status of the stack pointer monitor. Each stack point monitor has an independent ERROR bit.

[Setting condition]

- Overflow or underflow of the stack pointer.

[Clearing conditions]

- 0 is written to this bit
- A reset other than the bus master MPU error reset, bus slave MPU error reset, and stack pointer error reset.

Note: Only 0 can be written to the ERROR bit.

16.2.3.7 Stack Pointer Monitor Protection Register (MSPMPUPT, PSPMPUPT)

Address(es): SPMON.MSPMPUPT 4000 0D06h, SPMON.PSPMPUPT 4000 0D16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of register	0: Stack pointer monitor register writes are possible 1: Stack pointer monitor register writes are protected. Reads are permitted.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit	R/(W)*1

Note 1. Write data is not saved.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected, independently set for the Main Stack Pointer Monitor and the Process Stack Pointer monitor.

MSPMPUPT.PROTECT controls the following main stack pointer protection registers:

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUPT.PROTECT controls the following process stack pointer protection registers:

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

- MSPMPUEA
- MSPMPUOAD.

当PSPMPUCTL.ENABLE位设置为1时，以下寄存器可用：

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR位（堆栈指针监视器错误标志）

ERROR位指示堆栈指针监视器的状态。每个堆栈点监视器都有一个独立的ERROR位。

[Setting condition]

- 堆栈指针上溢或下溢。

[Clearing conditions]

- 0写入该位
- 总线主MPU错误复位、总线从MPU错误复位和堆栈指针错误复位以外的复位。

Note: ERROR位只能写入0。

16.2.3.7 堆栈指针监视器保护寄存器(MSPMPUPT PSPMPUPT)

Address(es): SPMON.MSPMPUPT 4000 0D06h, SPMON.PSPMPUPT 4000 0D16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PROTECT	注册保护	0：可以写堆栈指针监视寄存器1：保护堆栈指针监视寄存器写。允许读取。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对PROTECT位的写入	R/(W)*1

Note 1. 不保存写入数据。

PROTECT位（保护寄存器）

PROTECT位启用或禁用对要保护的相关寄存器的写入，独立设置为Main
堆栈指针监视器和进程堆栈指针监视器。

MSPMPUPT.PROTECT控制以下主堆栈指针保护寄存器：

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUPT.PROTECT控制以下进程堆栈指针保护寄存器：

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

When writing to the PROTECT bit, simultaneously write A5h to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write A5h to KEY[7:0] simultaneously. When values other than A5h are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0.

16.3 Arm MPU

The Arm MPU has eight region MPUs and provides full support for:

- Protected regions
- Overlapping protected regions, with ascending region priority:
  7 = highest priority
  0 = lowest priority.
- Access permissions
- Exporting memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (HardFault) handler. For details, see 2. in section 16.7, References.

16.4 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus master in the entire address space (0000 0000h to FFFF FFFFh). The access control information, consisting of read and write permissions, can be independently set for up to 16 regions. The bus master MPU monitors access to each region based on these settings. If access to a protected region is detected, the bus master MPU generates an internal reset or a non-maskable interrupt. For information on error access, see section 15.3.3 and section 15.3.4 in section 15, Buses.

Table 16.4 lists the specifications of the bus master MPU, and Figure 16.3 shows a block diagram.

Table 16.4 Bus master MPU specifications

Parameter	Description
Protected master groups	Bus master MPU group A: DMA bus
Protected region	0000 0000h to FFFF FFFFh
Number of regions	Bus master MPU group A: 16 regions
Address specification for individual regions	Specifying start and end address for individual regions
Enable or disable setting for memory protection in individual regions	Enabling or disabling setting for the associated region
Access-control settings for individual regions	Permission to read and write
Operation on error detection	Reset or non-maskable interrupts
Register protection	Register can be protected from illegal writes

写入PROTECT位时，同时使用半字访问将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将A5h写入KEY[7:0]。当A5h以外的值写入KEY[7:0]位时，PROTECT位不会更新。KEY[7:0]位总是读为0。

16.3 Arm MPU

ArmMPU有8个区域MPU，并为以下方面提供全面支持：

- 保护区
- 重叠的受保护区域，区域优先级升序：7=最高优先级0=
  最低优先级。
- 访问权限
- 将内存属性导出到系统。

ArmMPU不匹配和权限违规调用可编程优先级MemManage故障(HardFault)处理程序。有关详细信息，请参阅第16.7节，参考中的2.。

16.4 总线主控MPU

总线主控MPU在整个地址空间（00000000h到
FFFFFFFFh）。访问控制信息，由读写权限组成，最多可以为16个区域独立设置。总线主控MPU根据这些设置监控对每个区域的访问。如果检测到对受保护区域的访问，总线主控MPU会产生内部复位或不可屏蔽中断。有关错误访问的信息，请参阅第15节"总线"中的第15.3.3节和第15.3.4节。

表16.4列出了总线主控MPU的规格，图16.3显示了框图。

Table 16.4 总线主控MPU规格

Parameter	Description
受保护的主组	总线主控MPU组A：DMA总线
保护区	0000 0000h to FFFF FFFFh
地区数量	总线主控MPUA组：16个区域
个别地区的地址规范	指定各个区域的开始和结束地址
在各个区域启用或禁用内存保护设置	启用或禁用关联区域的设置
各个区域的访问控制设置	读写权限
错误检测操作	复位或不可屏蔽中断
注册保护	可以保护寄存器免受非法写入

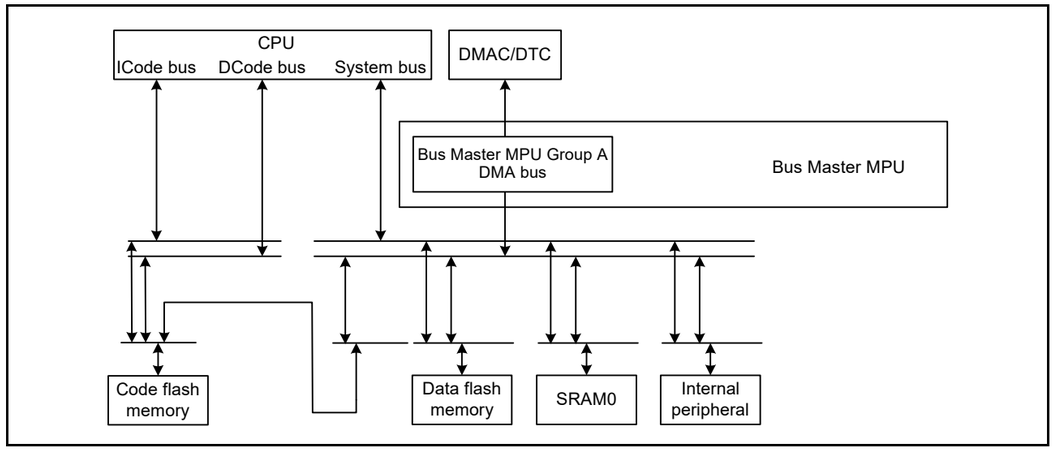


Figure 16.3 MPU bus master block diagram

Figure 16.4 shows the MPU bus master group A.

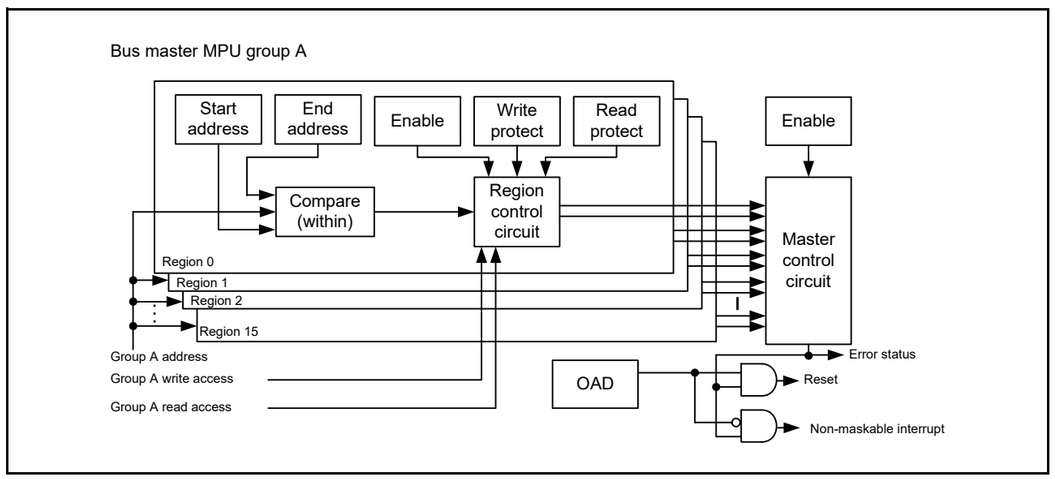


Figure 16.4 MPU bus master group A

16.4.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

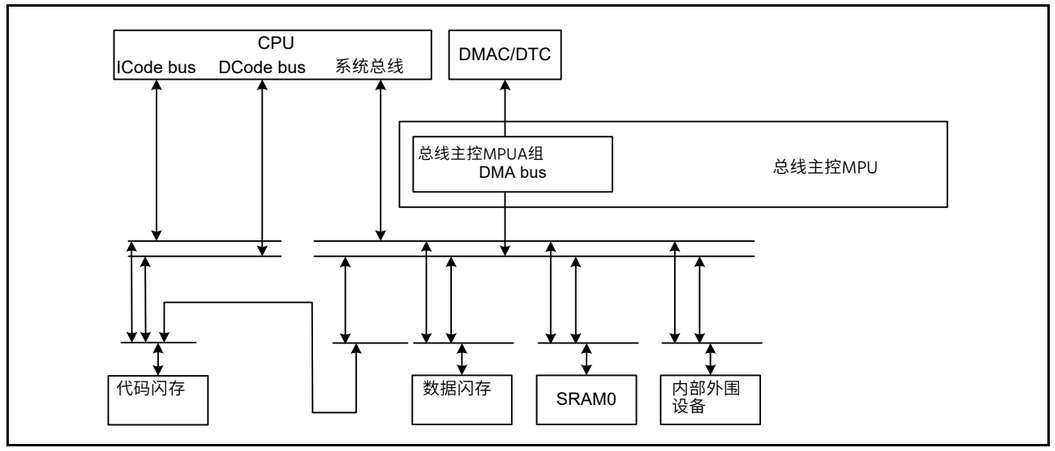


Figure 16.3 MPU总线主控框图

图16.4显示了MPU总线主控组A。

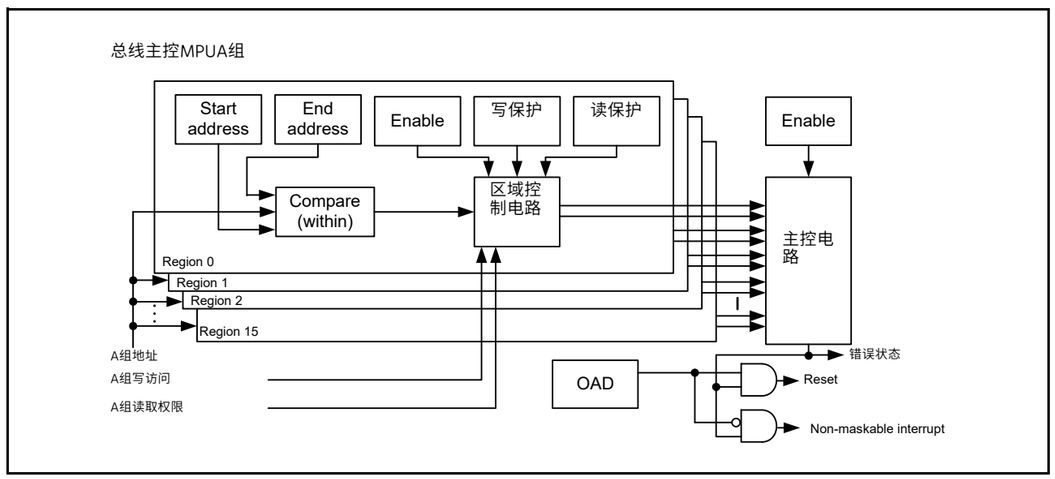


Figure 16.4 MPU总线主控组A

16.4.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

16.4.1.1 Group A Region n Start Address Register (MMPUSAn) (n = 0 to 15)

Address(es): MMPU.MMPUSA0 4000 0204h, MMPU.MMPUSA1 4000 0214h, MMPU.MMPUSA2 4000 0224h, MMPU.MMPUSA3 4000 0234h, MMPU.MMPUSA4 4000 0244h, MMPU.MMPUSA5 4000 0254h, MMPU.MMPUSA6 4000 0264h, MMPU.MMPUSA7 4000 0274h, MMPU.MMPUSA8 4000 0284h, MMPU.MMPUSA9 4000 0294h, MMPU.MMPUSA10 4000 02A4h, MMPU.MMPUSA11 4000 02B4h, MMPU.MMPUSA12 4000 02C4h, MMPU.MMPUSA13 4000 02D4h, MMPU.MMPUSA14 4000 02E4h, MMPU.MMPUSA15 4000 02F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	MMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0.	R/W

16.4.1.2 Group A Region n End Address Register (MMPUEAn) (n = 0 to 15)

Address(es): MMPU.MMPUEA0 4000 0208h, MMPU.MMPUEA1 4000 0218h, MMPU.MMPUEA2 4000 0228h, MMPU.MMPUEA3 4000 0238h, MMPU.MMPUEA4 4000 0248h, MMPU.MMPUEA5 4000 0258h, MMPU.MMPUEA6 4000 0268h, MMPU.MMPUEA7 4000 0278h, MMPU.MMPUEA8 4000 0288h, MMPU.MMPUEA9 4000 0298h, MMPU.MMPUEA10 4000 02A8h, MMPU.MMPUEA11 4000 02B8h, MMPU.MMPUEA12 4000 02C8h, MMPU.MMPUEA13 4000 02D8h, MMPU.MMPUEA14 4000 02E8h, MMPU.MMPUEA15 4000 02F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1.	R/W

16.4.1.3 Group A Region n Access Control Register (MMPUACAn) (n = 0 to 15)

Address(es): MMPU.MMPUACA0 4000 0200h, MMPU.MMPUACA1 4000 0210h, MMPU.MMPUACA2 4000 0220h, MMPU.MMPUACA3 4000 0230h, MMPU.MMPUACA4 4000 0240h, MMPU.MMPUACA5 4000 0250h, MMPU.MMPUACA6 4000 0260h, MMPU.MMPUACA7 4000 0270h, MMPU.MMPUACA8 4000 0280h, MMPU.MMPUACA9 4000 0290h, MMPU.MMPUACA10 4000 02A0h, MMPU.MMPUACA11 4000 02B0h, MMPU.MMPUACA12 4000 02C0h, MMPU.MMPUACA13 4000 02D0h, MMPU.MMPUACA14 4000 02E0h, MMPU.MMPUACA15 4000 02F0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Region Enable	0: Group A region n unit disabled 1: Group A region n unit enabled.	R/W

16.4.1.1 A组区域n起始地址寄存器(MMPUSan)（n=0到15）

Address(es): MMPU.MMPUSA0 4000 0204h, MMPU.MMPUSA1 4000 0214h, MMPU.MMPUSA2 4000 0224h, MMPU.MMPUSA3 4000 0234h, MMPU.MMPUSA4 4000 0244h, MMPU.MMPUSA5 4000 0254h, MMPU.MMPUSA6 4000 0264h, MMPU.MMPUSA7 4000 0274h, MMPU.MMPUSA8 4000 0284h, MMPU.MMPUSA9 4000 0294h, MMPU.MMPUSA10 4000 02A4h, MMPU.MMPUSA11 4000 02B4h, MMPU.MMPUSA12 4000 02C4h, MMPU.MMPUSA13 4000 02D4h, MMPU.MMPUSA14 4000 02E4h, MMPU.MMPUSA15 4000 02F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUSA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUSA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MMPUSA[31:0]	区域起始地址	区域开始的地址，用于区域确定。低2位应为0。	R/W

16.4.1.2 A组区域n结束地址寄存器(MMPUEAn)(n=0到15)

Address(es): MMPU.MMPUEA0 4000 0208h, MMPU.MMPUEA1 4000 0218h, MMPU.MMPUEA2 4000 0228h, MMPU.MMPUEA3 4000 0238h, MMPU.MMPUEA4 4000 0248h, MMPU.MMPUEA5 4000 0258h, MMPU.MMPUEA6 4000 0268h, MMPU.MMPUEA7 4000 0278h, MMPU.MMPUEA8 4000 0288h, MMPU.MMPUEA9 4000 0298h, MMPU.MMPUEA10 4000 02A8h, MMPU.MMPUEA11 4000 02B8h, MMPU.MMPUEA12 4000 02C8h, MMPU.MMPUEA13 4000 02D8h, MMPU.MMPUEA14 4000 02E8h, MMPU.MMPUEA15 4000 02F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUEA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUEA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MMPUEA[31:0]	区域结束地址	区域结束的地址，用于区域确定。低2位应为1。	R/W

16.4.1.3 A组区域n访问控制寄存器(MMPUACAn)(n=0到15)

Address(es): MMPU.MMPUACA0 4000 0200h, MMPU.MMPUACA1 4000 0210h, MMPU.MMPUACA2 4000 0220h, MMPU.MMPUACA3 4000 0230h, MMPU.MMPUACA4 4000 0240h, MMPU.MMPUACA5 4000 0250h, MMPU.MMPUACA6 4000 0260h, MMPU.MMPUACA7 4000 0270h, MMPU.MMPUACA8 4000 0280h, MMPU.MMPUACA9 4000 0290h, MMPU.MMPUACA10 4000 02A0h, MMPU.MMPUACA11 4000 02B0h, MMPU.MMPUACA12 4000 02C0h, MMPU.MMPUACA13 4000 02D0h, MMPU.MMPUACA14 4000 02E0h, MMPU.MMPUACA15 4000 02F0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENABLE	区域启用	0：A组区域n单元禁用1：A组区域n单元启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	RP	Read Protection	0: Read access permitted 1: Read access protected.	R/W
b2	WP	Write Protection	0: Write access permitted 1: Write access protected.	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ENABLE, RP, and WP bits are individually configurable for each group A region n.

ENABLE bit (Region Enable)

The ENABLE bit enables or disables group A region n unit.

When the ENABLE bit is set to 1, the RP bit and the WP bit can be set to permit or protect access to the region that is set in MMPUSAn and MMPUEAn. When the ENABLE bit is set to 0, no region is specified for group A region n access.

RP bit (Read Protection)

The RP bit enables or disables read protection for group A region n. The RP bit is available when the ENABLE bit is set to 1.

WP bit (Write Protection)

The WP bit enables or disables write protection for group A region n. The WP bit is available when the ENABLE bit is set to 1.

Table 16.5 Function of region control circuit

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	Output of group A region n unit
0	—	—	Read	—	Outside of region
			Write		Outside of region
1	0	0	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	0	1	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Protection region
				Outside	Outside of region
	1	0	Read	Inside	Protection region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	1	1	Read	Inside	Protection region
				Outside	Outside of region
			Write	Inside	Protection region
				Outside	Outside of region

n = 0 to 15

Bit	Symbol	位名称	Description	R/W
b1	RP	读保护	0：允许读访问1：读访问受保护。	R/W
b2	WP	写保护	0：允许写访问1：写访问受保护。	R/W
b15 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ENABLE、RP和WP位可针对每个A组区域n单独配置。

ENABLE位（区域启用）

ENABLE位启用或禁用A组区域n单元。

当ENABLE位设置为1时，可以设置RP位和WP位以允许或保护对MMPUSan和MMPUEAn中设置的区域的访问。
当ENABLE位设置为0时，没有为组A区域n访问指定区域。

RP位（读保护）

RP位启用或禁用组A区域n的读保护。当ENABLE位设置为1时，RP位可用。

WP位（写保护）

WP位启用或禁用A组区域n的写保护。当ENABLE位设置为1时，WP位可用。

Table 16.5 区域控制电路的功能

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	A组区域n单元的输出
0	—	—	Read	—	区域外
			Write		区域外
1	0	0	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	0	1	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外
	1	0	Read	Inside	保护区
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	1	1	Read	Inside	保护区
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外

n = 0 to 15

Table 16.6 Function of master control circuit

MMPUCTLA.ENABLE	Output of group A region 0 unit	Output of group A region 1 unit	Output of group A region 2 to 15 unit	Function of group A
1	Protected region	Don't care	Don't care	Generate error
1	Don't care	Protected region	Don't care	Generate error
1	Don't care	Don't care	Protected region	Generate error
1	Outside of region	Outside of region	Outside of region	Generate error
Other case				No error

A master MPU error occurs on the following conditions:

- MMPUCTLA.ENABLE = 1, and output of one or more region n units is to a protected region
- MMPUCTLA.ENABLE = 1, and output of all region n units is outside of region.

Other cases are for permitted regions.

16.4.1.4 Bus Master MPU Control Register (MMPUCTLA)

Address(es): MMPU.MMPUCTLA 4000 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Master Group Enable	0: Master group A disabled 1: Master group A enabled.	R/W
b1	OAD	Operation After Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b2	—	Reserved	These bits are read as 0.The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and ENABLE bits	R/(W)*1

Note 1. Write data is not saved.

ENABLE bit (Master Group Enable)

The ENABLE bit enables or disables the bus master MPU function of master group A.

When this bit is set to 1, MMPUACAn is available. When this bit is set to 0, MMPUACAn is unavailable, including permission for all regions. When the ENABLE bit is set, write A5h to the KEY[7:0] bits simultaneously, using halfword access.

OAD bit (Operation After Detection)

The OAD bit generates either a reset or non-maskable interrupt when access to the protected region is detected by the bus master MPU. When the OAD bit is set, write A5h to the KEY[7:0] bits simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the ENABLE and OAD bits. When writing to the ENABLE and OAD bits, write A5h to the KEY[7:0] bits simultaneously. When values other than A5h are written to the KEY[7:0] bits, the ENABLE and the OAD bits are not updated. The KEY[7:0] bits are always read as 00h.

Table 16.6 主控电路功能

MMPUCTLA.ENABLE	A组区域0单元的输出	A组地区1单位产量	A组区域2至15单元的输出	A组功能
1	保护区	Don't care	Don't care	产生错误
1	Don't care	保护区	Don't care	产生错误
1	Don't care	Don't care	保护区	产生错误
1	区域外	区域外	区域外	产生错误
其他情况				没有错误

主控MPU错误发生在以下情况：

- MMPUCTLA.ENABLE=1，并且一个或多个区域n个单元的输出到受保护区域
- MMPUCTLA.ENABLE=1，所有区域n个单元的输出都在区域之外。

其他情况适用于允许的区域。

16.4.1.4 总线主控MPU控制寄存器(MMPUCTLA)

Address(es): MMPU.MMPUCTLA 4000 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENABLE	主组启用	0：主控组A禁用1：主控组A启用。	R/W
b1	OAD	检测后的操作	0：不可屏蔽中断1：复位。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对OAD的写入和使能位	R/(W)*1

Note 1. 不保存写入数据。

ENABLE位（主组启用）

ENABLE位启用或禁用主机组A的总线主机MPU功能。

当该位设置为1时，MMPUACan可用。当该位设置为0时，MMPUACan不可用，包括所有区域的权限。当ENABLE位置位时，使用半字访问同时将A5h写入KEY[7:0]位。

OAD位（检测后操作）

当总线主控MPU检测到对受保护区域的访问时，OAD位会产生复位或不可屏蔽中断。当OAD位置位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对ENABLE和OAD位的写入。写入ENABLE和OAD位时，同时将A5h写入KEY[7:0]位。当A5h以外的值写入KEY[7:0]位时，ENABLE和OAD位不会更新。KEY[7:0]位总是读为00h。

16.4.1.5 Group A Protection of Register (MMPUPTA)

Address(es): MMPU.MMPUPTA 4000 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of register	0: All bus master MPU group A register writes are permitted 1: All bus master MPU group A register writes are protected. Reads are possible.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit	R/(W)*1

Note 1. Write data is not saved.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPUPTA.PROTECT controls the bus master MPU group A protection registers. The following registers are protected by MMPUPTA.PROTECT:

- MMPUSAn
- MMPUEAn
- MMPUACAn
- MMPUCTLA.

When the PROTECT bit is set, write A5h to the KEY[7:0] bits simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write A5h to the KEY[7:0] bits simultaneously. When values other than A5h are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 00h.

16.4.2 Operation

16.4.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

The bus master MPU can be set for up to 16 protected regions. Protected regions include those with overlapping permitted and protected regions, and those with two overlapping permitted regions.

The bus master MPU has group A. The memory protection function checks the address of the bus for the master group and all master group accesses are protected. The bus master MPU sets the permission for all of the regions after reset. Setting MMPUCTLA.ENABLE to 1 protects all of the regions. Each region sets up a permitted region within the protected region. If access to the protected region is detected, the bus master MPU generates an error.

16.4.1.5 A组注册保护(MMPUPTA)

Address(es): MMPU.MMPUPTA 4000 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PROTECT	注册保护	0：允许所有总线主控MPUA组寄存器写入1：所有总线主控MPUA组寄存器写入受到保护。读取是可能的。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对PROTECT位的写入	R/(W)*1

Note 1. 不保存写入数据。

PROTECT位（保护寄存器）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPUPTA.PROTECT控制总线主控MPUA组保护寄存器。以下寄存器受MMPUPTA.PROTECT保护：

- MMPUSAn
- MMPUEAn
- MMPUACAn
- MMPUCTLA.

当PROTECT位置位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将A5h写入KEY[7:0]位。当A5h以外的值写入KEY[7:0]位时，PROTECT位不会更新。KEY[7:0]位总是读为00h。

16.4.2 Operation

16.4.2.1 内存保护

总线主控MPU使用为访问控制区域单独进行的控制设置来监视内存访问。如果检测到对受保护区域的访问，则总线主控MPU会产生内存保护错误。

总线主控MPU最多可设置16个受保护区域。保护区包括允许区域和保护区域重叠的区域，以及两个允许区域重叠的区域。

总线主控MPU具有A组。内存保护功能检查主控组的总线地址，并保护所有主控组访问。总线主控MPU在复位后设置所有区域的权限。将MMPUCTLA.ENABLE设置为1可以保护所有区域。每个区域在受保护区域内设置一个允许区域。如果检测到对受保护区域的访问，则总线主控MPU会产生错误。

Figure 16.5 shows the use case of a bus master MPU.

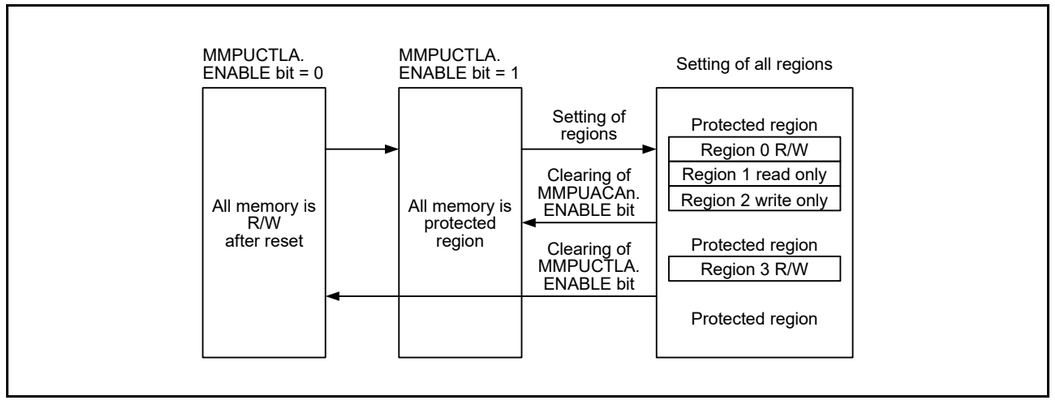


Figure 16.5 Use case of bus master MPU

Figure 16.6 shows the access permission or protection for the overlapping bus master MPU regions.

Access control for the overlapping regions is as follows:

- The region is handled as a protected region when output of one or more region units is a protected region
- The region is handled as a protected region when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

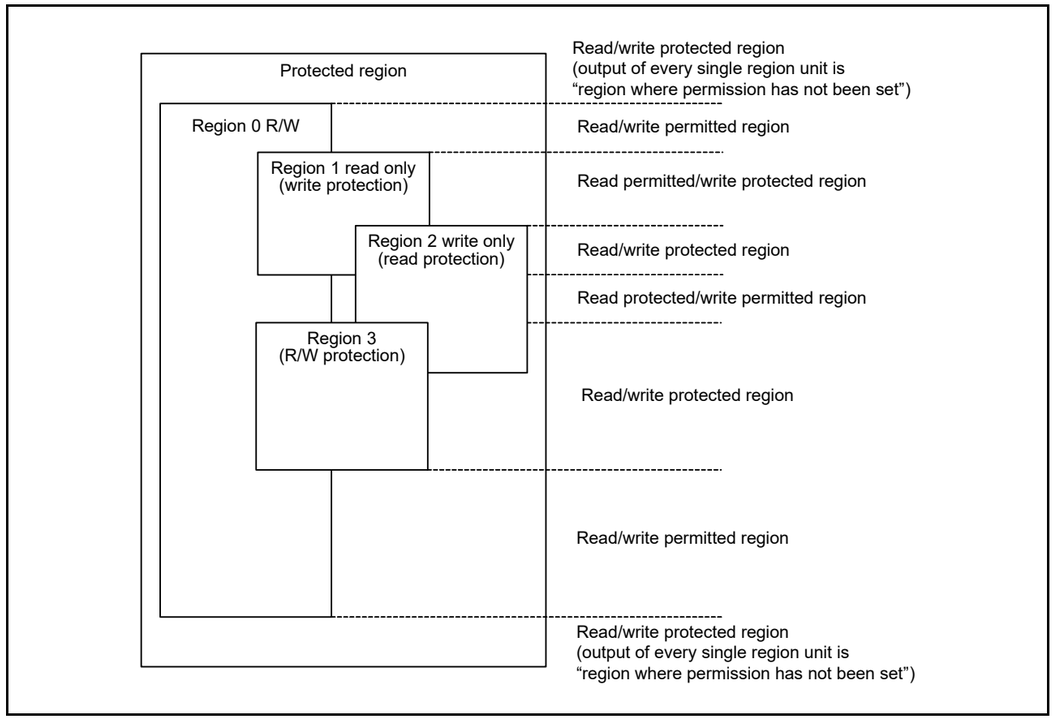


Figure 16.6 Access permission or protection by overlap of the bus master MPU regions

图16.5显示了总线主控MPU的用例。

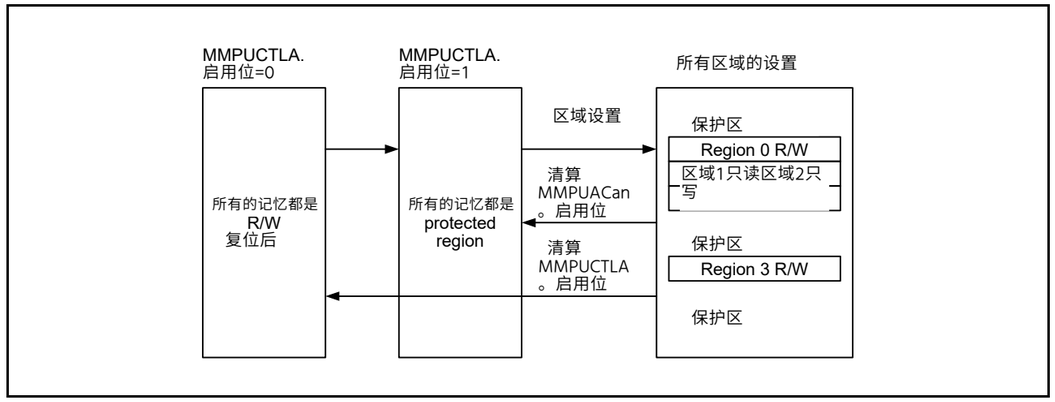


Figure 16.5 总线主控MPU用例

图16.6显示了重叠总线主控MPU区域的访问许可或保护。

重叠区域的访问控制如下：

- 当一个或多个区域单元的输出是受保护区域时，该区域被视为受保护区域
- 当所有区域单元的输出都在区域之外时，该区域被视为受保护区域
- 其他情况按许可区域处理。

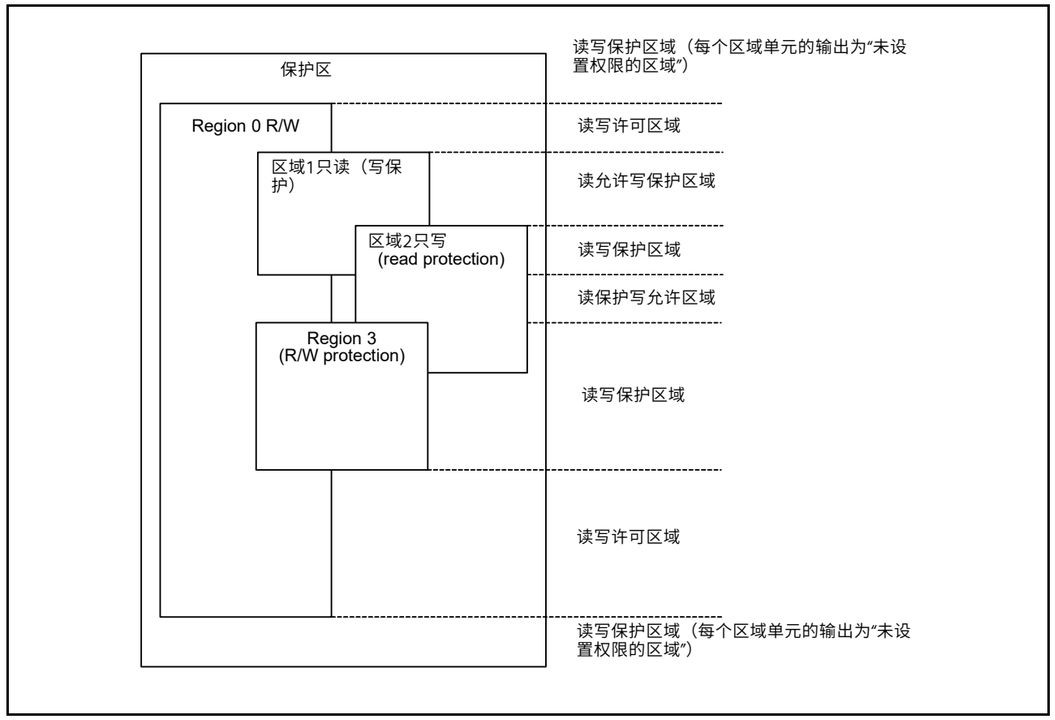


Figure 16.6 通过总线主控MPU区域的重叠访问许可或保护

Figure 16.7 shows the register setting flow after reset. During this register setting, stop all the masters except the CPU.

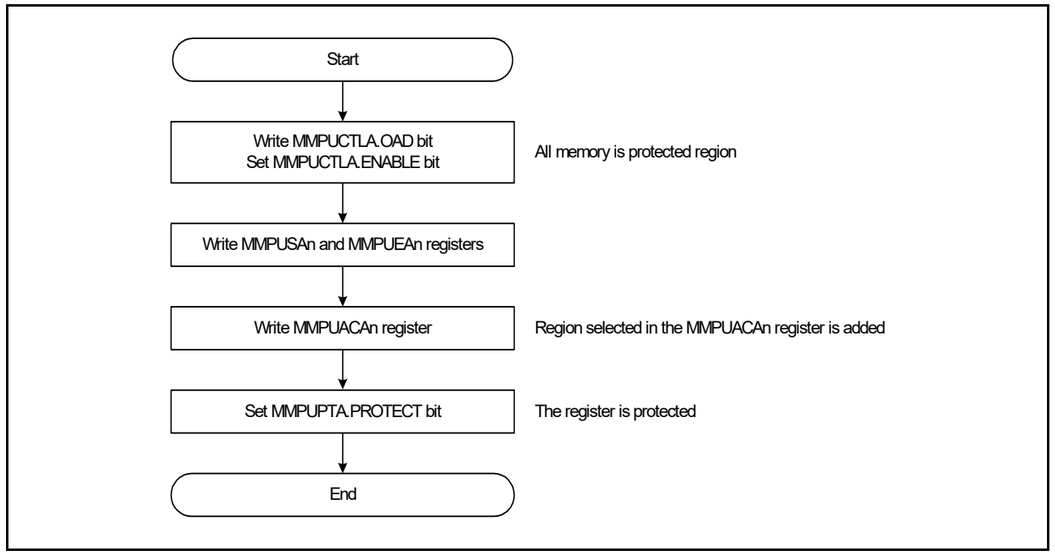


Figure 16.7 Register setting flow after reset

Figure 16.8 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

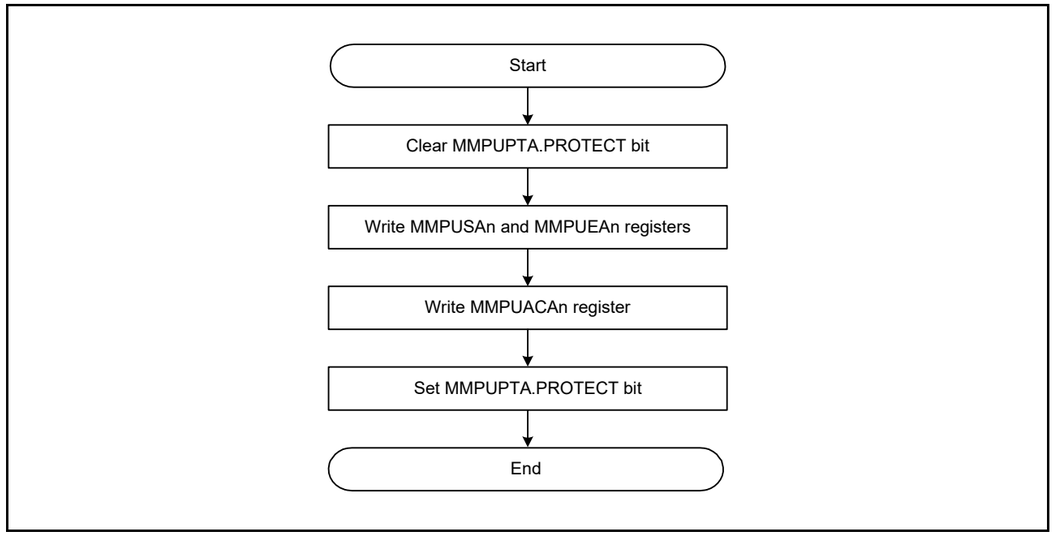


Figure 16.8 Register setting flow for region addition

16.4.2.2 Protecting the registers

To protect the registers related to the bus master MPU, set the PROTECT bit in the MMPUPTA register.

16.4.2.3 Memory protection error

If access to the protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether

图16.7显示了复位后的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有主机。

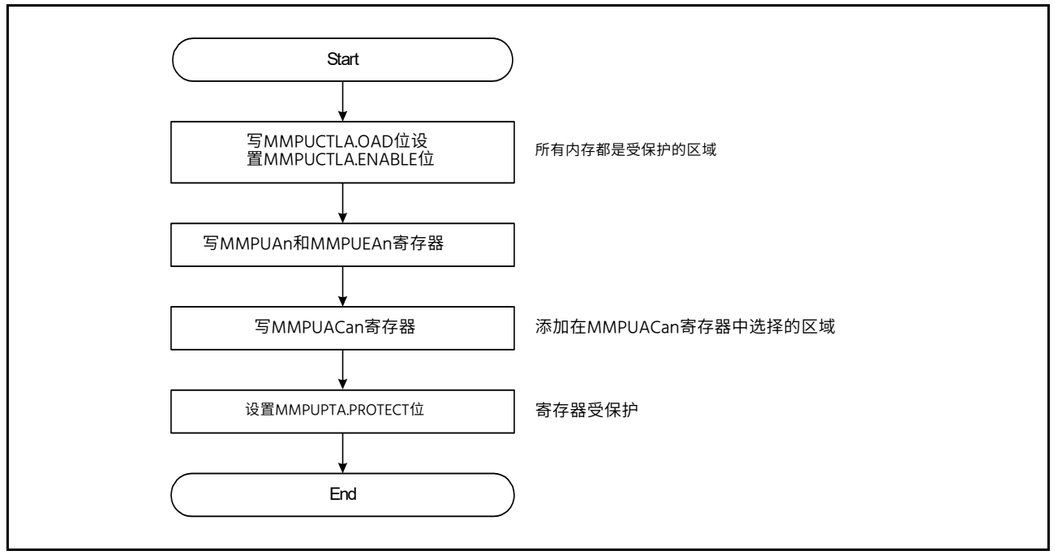


Figure 16.7 复位后的寄存器设置流程

图16.8显示了添加区域的寄存器设置流程。在此寄存器设置期间，停止除CPU.

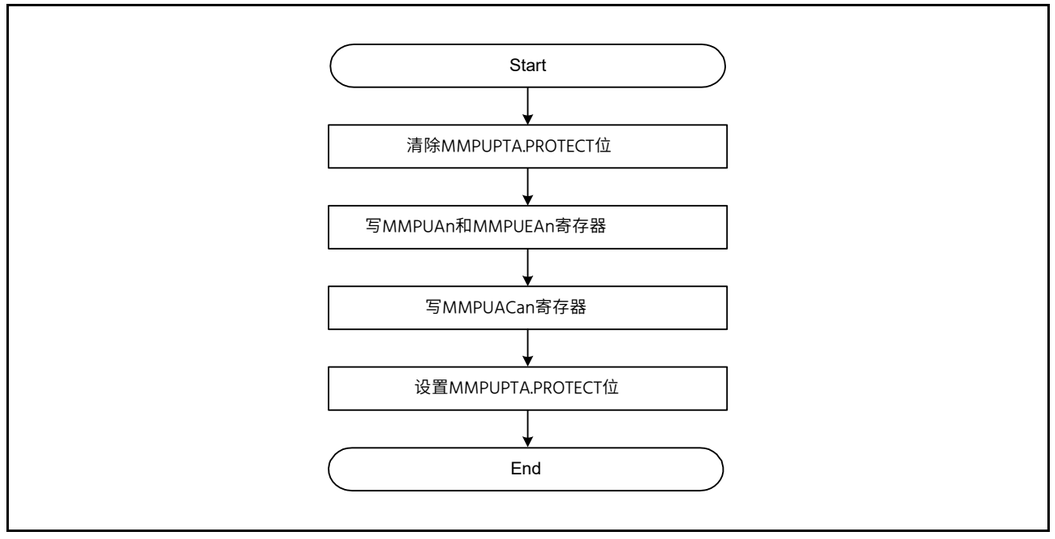


Figure 16.8 区域添加的注册设置流程

16.4.2.2 保护寄存器

为了保护与总线主控MPU相关的寄存器，设置MMPUPTA寄存器中的PROTECT位。

16.4.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线主控MPU会产生错误。设置OAD位以选择是否

the error is reported as a non-maskable interrupt or reset. The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST. For details, see section 14, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 6, Resets.

16.5 Bus Slave MPU

The bus slave MPU monitors access to the bus slave functions, such as flash or SRAM. The bus slave function can be accessed from two bus masters, the CPU, and the bus master MPU group A. The bus slave MPU has a separate protection register for each of the two bus masters, with individual access protection control. If access to a protected region is detected, the bus slave MPU generates a reset or a non-maskable interrupt, and can store the bus error status, error access status, and bus error address in the I/O Registers. For details, see 15.3.3 and 15.3.4 in section 15, Buses. The supported access control information for the individual regions consists of permissions to read and write.

Table 16.7 lists the specifications of the bus slave MPU and Figure 16.9 shows a block diagram.

Table 16.7 Specifications of bus slave MPU

Specifications	Description
Protected bus master	Bus master MPU group A: DMA bus
Protected slave functions	Memory bus 3: Code flash memory Memory bus 4: SRAM0 Internal peripheral bus 1: Connected to peripheral modules related system control Internal peripheral bus 3: Connected to peripheral modules (CAC, ELC, I/O ports, POEG, RTC, WDT, IWDT, IIC, CAN, ADC14, DAC12, and DOC) Internal peripheral bus 4: Connected to peripheral modules (SCI, SPI, and CRC) Internal peripheral bus 5: Connected to peripheral modules (KINT, AGT, USBFS, DAC8, OPAMP, ACMPLP, and CTSU) Internal peripheral bus 7: Connected to SecureIP (SCE5) Internal peripheral bus 9: Flash memory (in P/E) and data flash memory
Access-control information settings for individual regions	Permission to read and write
Operation after detection	Reset, non-maskable interrupt, or exception
Protection of register	Register can be protected from illegal writes

The bus slave MPU is located on each bus slave side and controls the permission or protection of access from each bus master to each bus slave.

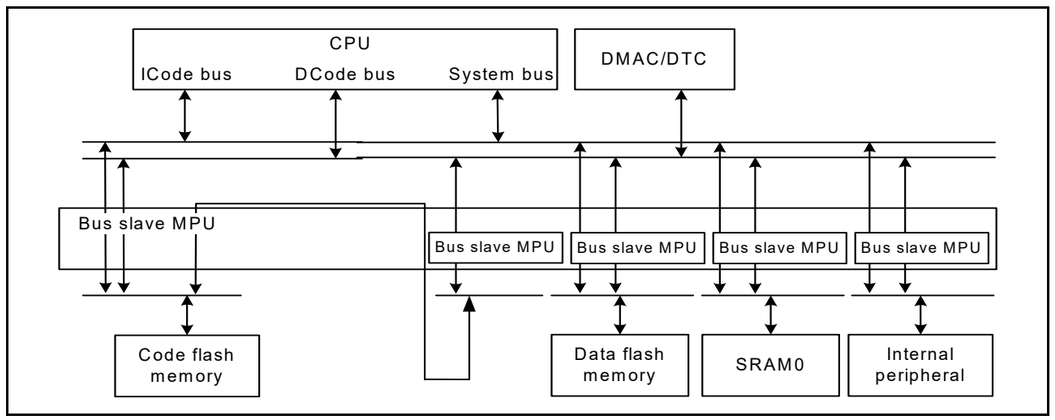


Figure 16.9 Bus slave MPU block diagram

该错误被报告为不可屏蔽的中断或复位。不可屏蔽中断状态在ICU.NMISR.BUSMST中指示。有关详细信息，请参阅第14节，中断控制器单元(ICU)。复位状态显示在SYSTEM.RSTSR1.BUSMRF。有关详细信息，请参阅第6节，重置。

16.5 总线从MPU

总线从机MPU监控对总线从机功能的访问，例如闪存或SRAM。总线从机功能可以从两个总线主机CPU和总线主机MPU组A访问。总线从机MPU对两个总线主机中的每一个都有一个单独的保护寄存器，具有单独的访问保护控制。如果检测到对受保护区域的访问，则总线从MPU会产生复位或不可屏蔽中断，并将总线错误状态、错误访问状态和总线错误地址存储在IO寄存器中。有关详细信息，请参阅第15节"总线"中的15.3.3和15.3.4。各个区域支持的访问控制信息包括读写权限。

表16.7列出了总线从MPU的规格，图16.9显示了框图。

Table 16.7 总线从机MPU规格

Specifications	Description
受保护的总线主机	总线主控MPU组A：DMA总线
受保护的从属功能	内存总线3：代码闪存 内存总线4：SRAM0 内部外围总线1：连接外围模块相关系统控制内部外围总线3：连接外围模块（CAC、ELC、IO端口、POEG、RTC、WDT、IWDT、IIC、CAN、ADC14、DAC12和DOC） 内部外围总线4：连接到外围模块（SCI、SPI和CRC）内部外围总线5：连接到外围模块（KINT、AGT、USBFS、DAC8, OPAMP, ACMPLP, and CTSU） 内部外围总线7：连接到SecureIP(SCE5) 内部外设总线9：闪存（在PE中）和数据闪存
各个区域的访问控制信息设置	读写权限
检测后操作	复位、不可屏蔽中断或异常
注册保护	可以保护寄存器免受非法写入

总线从机MPU位于每个总线从机侧，并控制从每个总线主机到每个总线从机的访问的许可或保护。

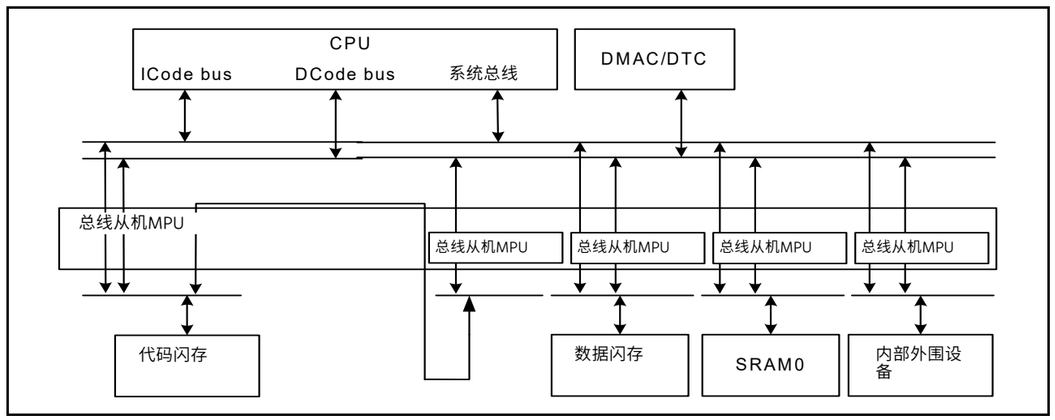


Figure 16.9 总线从机MPU框图

16.5.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

16.5.1.1 Access Control Register for Memory Bus 3 (SMPUMBIU)

Address(es): SMPU.SMPUMBIU 4000 0C10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Master group A read memory protection disabled 1: Master group A read memory protection enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Master group A write memory protection disabled 1: Master group A write memory protection enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master group A reads on memory bus 3.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master group A writes on memory bus 3.

16.5.1.2 Access Control Register for Internal Peripheral Bus 9 (SMPUFBIU)

Address(es): SMPU.SMPUFBIU 4000 0C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled.	R/W
b2	RPGRPA	Master Group A Read protection	0: Memory protection for master group A read disabled 1: Memory protection for master group A read enabled.	R/W
b3	WPGRPA	Master Group A Write protection	0: Memory protection for master group A write disabled 1: Memory protection for master group A write enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 9.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 9.

16.5.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

16.5.1.1 内存总线3的访问控制寄存器(SMPUMBIU)

Address(es): SMPU.SMPUMBIU 4000 0C10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	RPGRPA	大师组A读Protection	0：主机组A读存储器保护禁用1：主机组A读存储器保护启用。	R/W
b3	WPGRPA	大师组A写Protection	0：主机组A写内存保护禁用1：主机组A写内存保护启用。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内存总线3上主组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A写入内存总线3的内存保护。

16.5.1.2 内部外围总线9(SMPUFBIU)的访问控制寄存器

Address(es): SMPU.SMPUFBIU 4000 0C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写内存保护1：启用CPU写内存保护。	R/W
b2	RPGRPA	主组A读保护	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	主组A写保护	0：主组A写禁止内存保护1：主组A写允许内存保护。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外围总线9上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外围总线9上CPU写入的内存保护。

RPGRPA bit (Master Group A Read protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral Bus 9.

WPGRPA bit (Master Group A Write protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 9.

16.5.1.3 Access Control Register for Memory Bus 4 (SMPUSRAM0)

Address(es): SMPU.SMPUSRAM0 4000 0C18h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read protection	0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled.	R/W
b1	WPCPU	CPU Write protection	0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled.	R/W
b2	RPGRPA	Master Group A Read protection	0: Memory protection for master group A read disabled 1: Memory protection for master group A read enabled.	R/W
b3	WPGRPA	Master Group A Write protection	0: Memory protection for master group A write disabled 1: Memory protection for master group A write enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read protection)

The RPCPU bit enables or disables memory protection for CPU reads on memory bus 4.

WPCPU bit (CPU Write protection)

The WPCPU bit enables or disables memory protection for CPU writes on memory bus 4.

RPGRPA bit (Master Group A Read protection)

The RPGRPA bit enables or disables memory protection for master group A reads on memory bus 4.

WPGRPA bit (Master Group A Write protection)

The WPGRPA bit enables or disables memory protection for master group A writes on memory bus 4.

16.5.1.4 Access Control Register for Internal Peripheral Bus 1 (SMPUP0BIU)

Address(es): SMPU.SMPUP0BIU 4000 0C20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read protection	0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled.	R/W
b1	WPCPU	CPU Write protection	0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled.	R/W

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外设总线9上主组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A写入内部外围总线9的内存保护。

16.5.1.3 存储器总线4的访问控制寄存器(SMPUSRAM0)

Address(es): SMPU.SMPUSRAM0 4000 0C18h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写内存保护1：启用CPU写内存保护。	R/W
b2	RPGRPA	主组A读保护	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	主组A写保护	0：主组A写禁止内存保护1：主组A写允许内存保护。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内存总线4上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内存总线4上CPU写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内存总线4上主组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A写入内存总线4的内存保护。

16.5.1.4 内部外围总线1(SMPUP0BIU)的访问控制寄存器

Address(es): SMPU.SMPUP0BIU 4000 0C20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写内存保护1：启用CPU写内存保护。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	RPGRPA	Master Group A Read protection	0: Memory protection for master group A read disabled 1: Memory protection for master group A read enabled.	R/W
b3	WPGRPA	Master Group A Write protection	0: Memory protection for master group A write disabled 1: Memory protection for master group A write enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 1.

WPCPU bit (CPU Write protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 1.

RPGRPA bit (Master Group A Read protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 1.

WPGRPA bit (Master Group A Write protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 1.

16.5.1.5 Access Control Register for Internal Peripheral Bus 3 (SMPUP2BIU)

Address(es): SMPU.SMPUP2BIU 4000 0C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read protection	0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled.	R/W
b1	WPCPU	CPU Write protection	0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled.	R/W
b2	RPGRPA	Master Group A Read protection	0: Memory protection for master group A read disabled 1: Memory protection for master group A read enabled.	R/W
b3	WPGRPA	Master Group A Write protection	0: Memory protection for master group A write disabled 1: Memory protection for master group A write enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 3, internal peripheral bus 4, and internal peripheral bus 5.

WPCPU bit (CPU Write protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 3, internal peripheral bus 4, and internal peripheral bus 5.

RPGRPA bit (Master Group A Read protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 3, internal peripheral bus 4, and internal peripheral bus 5.

WPGRPA bit (Master Group A Write protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 3, internal peripheral bus 4, and internal peripheral bus 5.

Bit	Symbol	位名称	Description	R/W
b2	RPGRPA	主组A读保护	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	主组A写保护	0：主组A写禁止内存保护1：主组A写允许内存保护。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外设总线1上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外设总线1上CPU写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用主机组A读取内部外围总线1的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A写入内部外围总线1的内存保护。

16.5.1.5 内部外围总线3(SMPUP2BIU)的访问控制寄存器

Address(es): SMPU.SMPUP2BIU 4000 0C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写内存保护1：启用CPU写内存保护。	R/W
b2	RPGRPA	主组A读保护	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	主组A写保护	0：主组A写禁止内存保护1：主组A写允许内存保护。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外围总线3、内部外围总线4和内部外围总线5上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用对内部外围总线3、内部外围总线4和内部外围总线5上的CPU写入的存储器保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用主机组A读取内部外围总线3、内部外围总线4和内部外围总线5的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A写入内部外围总线3、内部外围总线4和内部外围总线5的存储器保护。

16.5.1.6 Access Control Register for Internal Peripheral Bus 7 (SMPUP6BIU)

Address(es): SMPU.SMPUP6BIU 4000 0C28h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read protection	0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled.	R/W
b1	WPCPU	CPU Write protection	0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled.	R/W
b2	RPGRPA	Master Group A Read protection	0: Memory protection for master group A read disabled 1: Memory protection for master group A read enabled.	R/W
b3	WPGRPA	Master Group A Write protection	0: Memory protection for master group A write disabled 1: Memory protection for master group A write enabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 7.

WPCPU bit (CPU Write protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 7.

RPGRPA bit (Master Group A Read protection)

The RPGRPA bit enables or disables memory protection for master group A reads on internal peripheral bus 7.

WPGRPA bit (Master Group A Write protection)

The WPGRPA bit enables or disables memory protection for master group A writes on internal peripheral bus 7.

16.5.1.7 Slave MPU Control Register (SMPUCTL)

Address(es): SMPU.SMPUCTL 4000 0C00h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after detection	0: Non-maskable interrupt 1: Reset.	R/W
b1	PROTECT	Protection of register	0: All bus slave register writes are permitted 1: All bus slave register writes are protected. Reads are permitted.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits are used to enable or disable writes to the OAD and PROTECT bits.	R/(W)*1

Note 1. Write data is not saved.

16.5.1.6 内部外设总线7的访问控制寄存器(SMPUP6BIU)

Address(es): SMPU.SMPUP6BIU 4000 0C28h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写内存保护1：启用CPU写内存保护。	R/W
b2	RPGRPA	主组A读保护	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	主组A写保护	0：主组A写禁止内存保护1：主组A写允许内存保护。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外围总线7上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外围总线7上CPU写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外围总线7上主组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A写入内部外围总线7的内存保护。

16.5.1.7 从MPU控制寄存器(SMPUCTL)

Address(es): SMPU.SMPUCTL 4000 0C00h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后操作	0：不可屏蔽中断1：复位 。	R/W
b1	PROTECT	注册保护	0：允许所有总线从属寄存器写入1：所有总线从属寄存器写入受到保护。允许读取。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位用于启用或禁用对OAD的写入和保护位。	R/(W)*1

Note 1. 不保存写入数据。

OAD bit (Operation after detection)

The OAD bit generates either a reset or non-maskable interrupt when access to the protected region is detected by the bus slave MPU. When the OAD bit is set, write A5h to the KEY[7:0] bits simultaneously using halfword access.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected. The following registers are protected by SMPUCTL.PROTECT:

- SMPUMBIU
- SMPUFBIU
- SMPUSRAM0
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU

When the PROTECT bit is set, write A5h to the KEY[7:0] bits simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD and PROTECT bits. When writing to the OAD and PROTECT bits, write A5h to KEY[7:0] simultaneously. When values other than A5h are written to the KEY[7:0] bits, the OAD and the PROTECT bits are not updated. The KEY[7:0] bits are always read as 00h.

16.5.2 Functions

16.5.2.1 Memory protection

The bus slave MPU monitoring uses access control information that is set for the individual access control registers, whether or not access by the bus slaves violates the access control settings. If access to the protected region is detected, the bus slave MPU generates a memory protection error.

The bus slave MPU is enabled by writing 1 to the Write Protect (WPCPU or WPGRPA) bit or the Read Protect (RPCPU or RPGRPA) bit in the access control registers (SMPUMBIU, SMPUFBIU, SMPUSRAM0, SMPUP0BIU, SMPUP2BIU, and SMPUP6BIU).

16.5.2.2 Protecting the registers

Registers related to the bus slave MPU can be protected with the PROTECT bit in the SMPUCTL register.

16.5.2.3 Memory protection error

If access to a protected region is detected, the bus slave MPU generates a memory protection error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSSST. For details, see section 14, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSSRF. For details, see section 6, Resets.

16.6 Security MPU

The MCU incorporates a security MPU with four secure regions that include the code flash, the SRAM, and two security functions. The secure regions can be protected from non-secure program accesses. A non-secure program cannot access a protected region.

Table 16.8 lists the specifications of the security MPU and Figure 16.10 shows a block diagram.

Table 16.8 Security MPU specifications (1 of 2)

Specifications	Description
Secure regions	Code flash, SRAM, two security functions

OAD位（检测后操作）

当总线从机MPU检测到对受保护区域的访问时，OAD位会产生复位或不可屏蔽中断。当OAD位置位时，使用半字访问同时将A5h写入KEY[7:0]位。

PROTECT位（保护寄存器）

PROTECT位启用或禁用对要保护的相关寄存器的写入。以下寄存器受SMPUCTL.PROTECT保护：

- SMPUMBIU
- SMPUFBIU
- SMPUSRAM0
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU

当PROTECT位置位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对OAD和PROTECT位的写入。写入OAD和PROTECT位时，同时将A5h写入KEY[7:0]。当A5h以外的值写入KEY[7:0]位时，OAD和PROTECT位不会更新。KEY[7:0]位总是读为00h。

16.5.2 Functions

16.5.2.1 内存保护

总线从机MPU监控使用为各个访问控制寄存器设置的访问控制信息，无论总线从机的访问是否违反访问控制设置。如果检测到对受保护区域的访问，则总线从MPU会产生内存保护错误。

通过将1写入访问控制寄存器（SMPUMBIU、SMPUFBIU、SMPUSRAM0、SMPUP0BIU、SMPUP2BIU和SMPUP6BIU）中的写保护（WPCPU或WPGRPA）位或读保护（RPCPU或RPGRPA）位来启用总线从MPU。

16.5.2.2 保护寄存器

与总线从MPU相关的寄存器可以通过SMPUCTL寄存器中的PROTECT位进行保护。

16.5.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线从MPU会产生内存保护错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。

不可屏蔽中断状态在ICU.NMISR.BUSSST中指示。有关详细信息，请参见第14节，中断控制器单位（ICU）。复位状态在SYSTEM.RSTSR1.BUSSRF中指示。有关详细信息，请参阅第6节，重置。

16.6 Security MPU

MCU包含一个安全MPU，它具有四个安全区域，包括代码闪存、SRAM和两个安全功能。可以保护安全区域免受非安全程序访问。非安全程序无法访问受保护区域。

表16.8列出了安全MPU的规格，图16.10显示了框图。

Table 16.8 安全MPU规格(1of2)

Specifications	Description
安全区域	代码闪存、SRAM、两个安全功能

Table 16.8 Security MPU specifications (2 of 2)

Specifications	Description
Protected regions	0000 0000h to 00FF FFFFh (Code flash memory) 1FF0 0000h to 200F FFFFh (SRAM) 400C 0000h to 400D FFFFh 4010 0000h to 407F FFFFh (secure data of security functions)
Number of regions	Program Counter = 2 regions Data Access = 4 regions
Address specification for individual regions	Setting the address where regions start and end
Enable or disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region

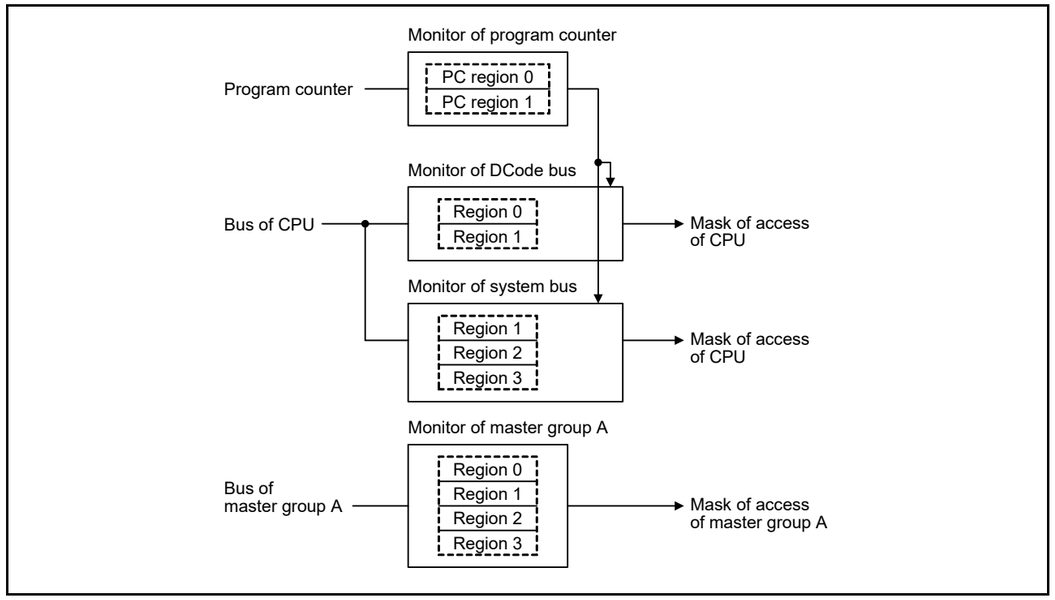


Figure 16.10 Security MPU block diagram

16.6.1 Register Descriptions (Option-Setting Memory)

All security MPU registers are option-setting memory. Option-setting memory refers to a set of registers that are available for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the flash.

Table 16.8 安全MPU规格（2个中的2个）

Specifications	Description
保护区	00000000h至00FFFFFFh（代码闪存）1FF00000h至200FFFFFh（SRAM）400C0000h至400DFFFFh40100000h至407FFFFFh（安全功能的安全数据）
地区数量	程序计数器=2个区域 数据访问=4个区域
个别地区的地址规范	设置区域开始和结束的地址
在各个区域启用或禁用内存保护设置	为关联区域启用或禁用的设置

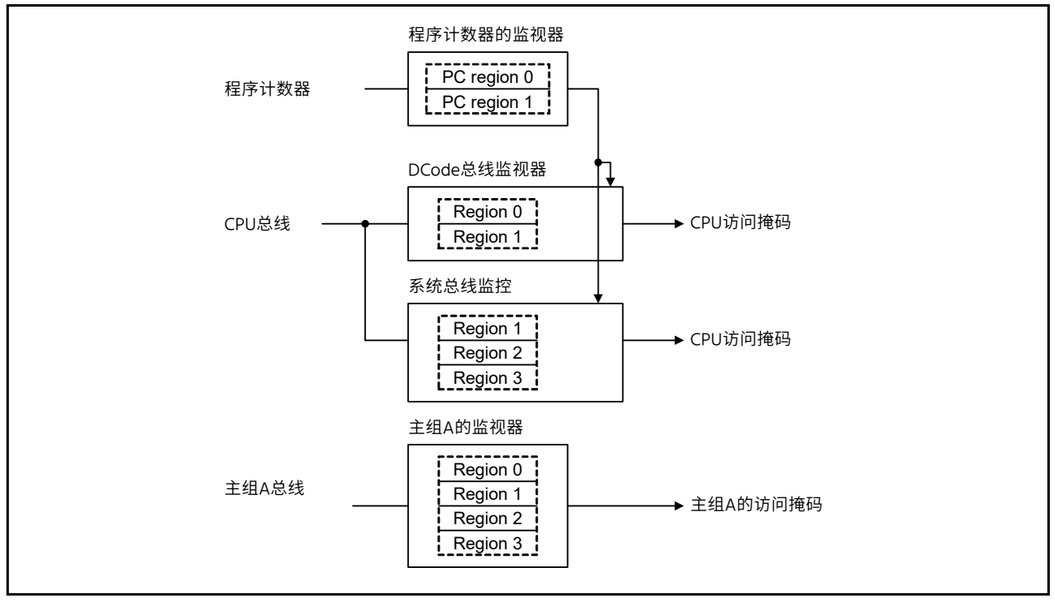


Figure 16.10 安全MPU框图

16.6.1 寄存器说明（选项设置存储器）

所有安全MPU寄存器都是选项设置存储器。选项设置存储器是指一组寄存器，可用于在复位后选择微控制器的状态。选项设置内存在闪存中分配。

16.6.1.1 Security MPU Program Counter Start Address Register (SECMPUPCSn) (n = 0, 1)

Address(es): SECMPUPCS0 0000 0408h, SECMPUPCS1 0000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCS[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCS[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUPCS[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. The value range should be 0000 0000h to 00FF FFFCh and 1FF0 0000h to 200F FFFCh, excluding reserved areas. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 0.	R

The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region for the code flash (0000 0000h to 00FF FFFFh, not including the reserved areas) or SRAM (1FF0 0000h to 200F FFFFh, not including the reserved areas). The secure program is executed in the memory space defined by the SECMPUPCSn and SECMPUPCEn registers and can access the secure data specified in the SECMPUSm and SECMPUEm registers (m = 0 to 3). The set up of memory mirror space (0200 0000h to 027F FFFFh) for MMF is not allowed.

Address space of greater than 12 bytes is required between the last instruction of the non-secure program and the first instruction of the secure program.

16.6.1.1 安全MPU程序计数器起始地址寄存器(SECMPUPCSn)(n=0 1)

Address(es): SECMPUPCS0 0000 0408h, SECMPUPCS1 0000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCS[31:16]															
重置后的值：	用户设置的值															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCS[15:0]															
重置后的值：	用户设置的值															

Bit	Symbol	位名称	Description	R/W
b31 to b0	SECMPUPCS[31:0]	区域起始地址	区域开始的地址，用于区域确定。低2位读为0。取值范围应为00000000h到00FFFFFCh和1FF00000h到200FFFFCh，不包括保留区。在选项设置存储器中设置该寄存器值时，低2位的写入值应为0。	R

SECMPUPCSn和SECMPPCEn寄存器指定代码闪存（00000000h到00FFFFFFh，不包括保留区域）或SRAM（1FF00000h到200FFFFFh，不包括保留区域）的安全提取区域。安全程序在由SECMPUPCSn和SECMPPCEn寄存器定义的存储空间中执行，并且可以访问在SECMPUSm和SECMPUEm寄存器（m=0到3）中指定的安全数据。不允许为MMF设置内存镜像空间（02000000h到027FFFFFh）。

在非安全程序的最后一条指令和安全程序的第一条指令之间需要大于12字节的地址空间。

16.6.1.2 Security MPU Program Counter End Address Register (SECMPUPCEn) (n = 0, 1)

Address(es): SECMPUPCE0 0000 040Ch, SECMPUPCE1 0000 0414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCE[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCE[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUPCE[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. The value range should be 0000 0003h to 00FF FFFFh and 1FF0 0003h to 200F FFFFh, excluding reserved areas. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 1.	R

16.6.1.3 Security MPU Region 0 Start Address Register (SECMPUS0)

Address(es): SECMPUS0 0000 0418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SECMPUS0[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	The value set by user							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS0[15:0]															
Value after reset:	The value set by user															

Bit	Symbol	Bit name	Description	R/W
b23 to b0	SECMPUS0[23:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. The value range should be 0000 0000h to 00FF FFFCh, excluding reserved areas. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 0.	R
b31 to b24	—	Reserved	These bits are read as 0. When setting this register value in the option-setting memory, the write value of these bits should be 0.	R

The SECMPUS0 and SECMPUE0 registers specify the secure program and the flash data (0000 0000h to 00FF FFFFh, not including the reserved areas). The memory space defined in the SECMPUS0 and SECMPUE0 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

Setting of the vector table area is prohibited.

16.6.1.2 安全MPU程序计数器结束地址寄存器(SECMPUPCEn)(n=0 1)

Address(es): SECMPUPCE0 0000 040Ch, SECMPUPCE1 0000 0414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUPCE[31:16]															
重置后的值：	用户设置的值															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUPCE[15:0]															
重置后的值：	用户设置的值															

Bit	Symbol	位名称	Description	R/W
b31 to b0	SECMPUPCE[31:0]	区域结束地址	区域结束的地址，用于区域确定。低2位读为1。取值范围应为00000003h到00FFFFFFh和1FF00003h到200FFFFFh，不包括保留区。在选项设置存储器中设置该寄存器值时，低2位的写入值应为1。	R

16.6.1.3 安全MPU区域0起始地址寄存器(SECMPUS0)

Address(es): SECMPUS0 0000 0418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SECMPUS0[23:16]							
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS0[15:0]															
重置后的值：	用户设置的值															

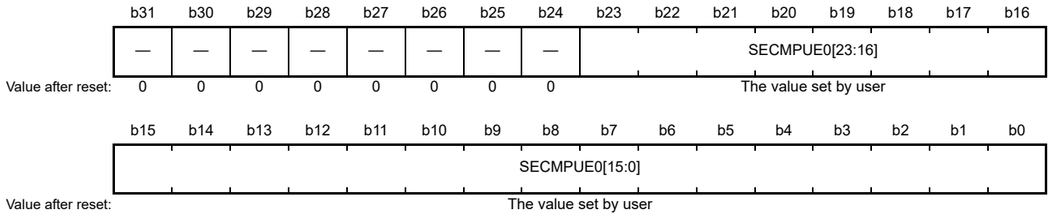
Bit	Symbol	位名称	Description	R/W
b23 to b0	SECMPUS0[23:0]	区域起始地址	区域开始的地址，用于区域确定。低2位读为0。取值范围应为00000000h到00FFFFFCh，不包括保留区。在选项设置存储器中设置该寄存器值时，低2位的写入值应为0。	R
b31 to b24	—	Reserved	这些位读为0。 在选项设置存储器中设置该寄存器值时，这些位的写入值应为0。	R

SECMPUS0和SECMPUE0寄存器指定安全程序和闪存数据（00000000h到00FFFFFFh，不包括保留区域）。SECMPUS0和SECMPUE0寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

禁止设置向量表区域。

16.6.1.4 Security MPU Region 0 End Address Register (SECMPUE0)

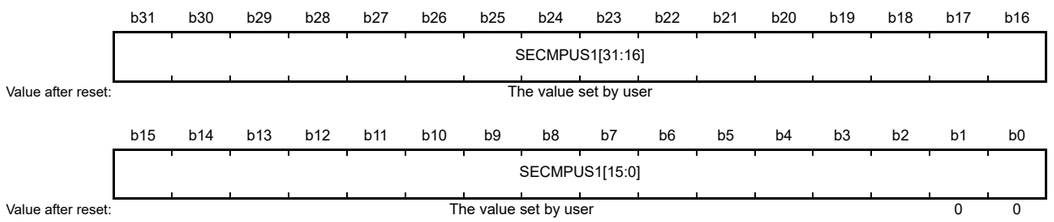
Address(es): SECMPUE0 0000 041Ch



Bit	Symbol	Bit name	Description	R/W
b23 to b0	SECMPUE0[23:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. The value range should be 0000 0003h to 00FF FFFFh, excluding reserved areas. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 1.	R
b31 to b24	—	Reserved	These bits are read as 0. When setting this register value in the option-setting memory, the write value of these bits should be 0.	R

16.6.1.5 Security MPU Region 1 Start Address Register (SECMPUS1)

Address(es): SECMPUS1 0000 0420h



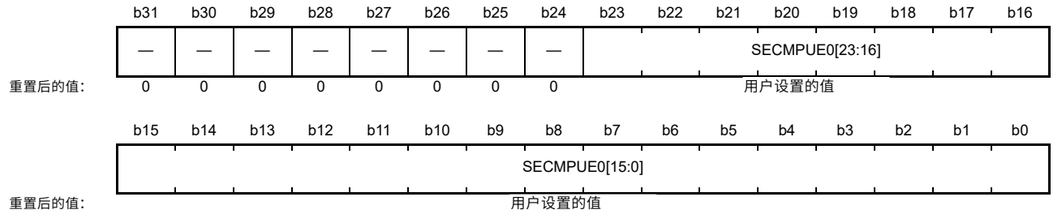
Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUS1[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. The value range should be 1FF0 0000h to 200F FFFCh, excluding reserved areas. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 0, and the write value of bits [31:20] should be 1FFh or 200h.	R

The SECMPUS1 and SECMPUE1 registers specify the secure data of the SRAM (1FF0 0000h to 200F FFFFh, not including the reserved areas). The memory space defined in the SECMPUS1 and SECMPUE1 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

Setting of the stack area and the vector table are prohibited.

16.6.1.4 安全MPU区域0结束地址寄存器(SECMPUE0)

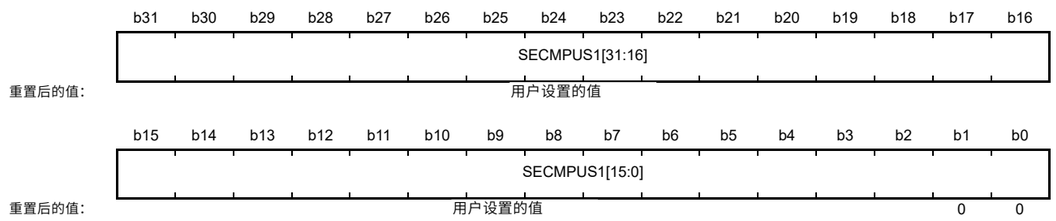
Address(es): SECMPUE0 0000 041Ch



Bit	Symbol	位名称	Description	R/W
b23 to b0	SECMPUE0[23:0]	区域结束地址	区域结束的地址，用于区域确定。低2位读为1。取值范围应为00000003h到00FFFFFFh，不包括保留区。在选项设置存储器中设置该寄存器值时，低2位的写入值应为1。	R
b31 to b24	—	Reserved	这些位读为0。 在选项设置存储器中设置该寄存器值时，这些位的写入值应为0。	R

16.6.1.5 安全MPU区域1起始地址寄存器(SECMPUS1)

Address(es): SECMPUS1 0000 0420h



Bit	Symbol	位名称	Description	R/W
b31 to b0	SECMPUS1[31:0]	区域起始地址	区域开始的地址，用于区域确定。低2位读为0。取值范围应为1FF00000h到200FFFFCh，不包括保留区。在选项设置存储器中设置该寄存器值时，低2位的写入值应为0，位[31:20]的写入值应为1FFh或200h。	R

SECMPUS1和SECMPUE1寄存器指定SRAM的安全数据（1FF00000h到200FFFFFh，不包括保留区域）。SECMPUS1和SECMPUE1寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

禁止设置堆栈区和向量表。

16.6.1.6 Security MPU Region 1 End Address Register (SECMPUE1)

Address(es): SECMPUE1 0000 0424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUE1[31:16]															
Value after reset:	The value set by user															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE1[15:0]															
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SECMPUE1[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. The value range should be 1FF0 0003h to 200F FFFFh, excluding reserved areas. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 1, and the write value of bits [31:20] should be 1FFh or 200h.	R

16.6.1.7 Security MPU Region 2 Start Address Register (SECMPUS2)

Address(es): SECMPUS2 0000 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS2[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS2[15:0]															
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b22 to b0	SECMPUS2[22:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. The value range should be 400C 0000h to 400D FFFCh and 4010 0000h to 407F FFFCh. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 0.	R
b31 to b23	—	Reserved	These bits are read as 0100 0000 0b. When setting this register value in the option-setting memory, the write value of these bits should be 0100 0000 0b.	R

The SECMPUS2 and SECMPUE2 registers specify the secure data of security functions (400C 0000 to 400D FFFFh and 4010 0000 to 407F FFFFh). The memory space defined in the SECMPUS2 and SECMPUE2 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

16.6.1.6 安全MPU区域1结束地址寄存器(SECMPUE1)

Address(es): SECMPUE1 0000 0424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECMPUE1[31:16]															
重置后的值：	用户设置的值															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE1[15:0]															
重置后的值：	用户设置的值														1	1

Bit	Symbol	位名称	Description	R/W
b31 to b0	SECMPUE1[31:0]	区域结束地址	区域结束的地址，用于区域确定。低2位读为1。取值范围应为1FF00003h到200FFFFFh，不包括保留区。在选项设置存储器中设置该寄存器值时，低2位的写入值应为1，位[31:20]的写入值应为1FFh或200h。	R

16.6.1.7 安全MPU区域2起始地址寄存器(SECMPUS2)

Address(es): SECMPUS2 0000 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS2[22:16]						
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS2[15:0]															
重置后的值：	用户设置的值														0	0

Bit	Symbol	位名称	Description	R/W
b22 to b0	SECMPUS2[22:0]	区域起始地址	区域开始的地址，用于区域确定。低2位读为0。取值范围应为400C0000h到400DFFFCh和40100000h到407FFFFCh。在选项设置存储器中设置该寄存器值时，低2位的写入值应为0。	R
b31 to b23	—	Reserved	这些位被读取为010000000b。在选项设置存储器中设置该寄存器值时，这些位的写入值应为010000000b。	R

SECMPUS2和SECMPUE2寄存器指定安全功能的安全数据（400C0000到400DFFFFh和40100000到407FFFFFh）。SECMPUS2和SECMPUE2寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

16.6.1.8 Security MPU Region 2 End Address Register (SECMPUE2)

Address(es): SECMPUE2 0000 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE2[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE2[15:0]															
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b22 to b0	SECMPUE2[22:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. The value range should be 400C 0003h to 400D FFFFh and 4010 0003h to 407F FFFFh. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 1.	R
b31 to b23	—	Reserved	These bits are read as 0100 0000 0b. When setting this register value in the option-setting memory, the write value of these bits should be 0100 0000 0b.	R

16.6.1.9 Security MPU Region 3 Start Address Register (SECMPUS3)

Address(es): SECMPUS3 0000 0430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS3[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS3[15:0]															
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b22 to b0	SECMPUS3[22:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits are read as 0. The value range should be 400C 0000h to 400D FFFCh and 4010 0000h to 407F FFFCh. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 0.	R
b31 to b23	—	Reserved	These bits are read as 0100 0000 0b. When setting this register value in the option-setting memory, the write value of these bits should be 0100 0000 0b.	R

The SECMPUS3 and SECMPUE3 registers specify the secure data of the security functions (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS3 and SECMPUE3 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

16.6.1.8 安全MPU区域2结束地址寄存器(SECMPUE2)

Address(es): SECMPUE2 0000 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE2[22:16]						
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE2[15:0]															
重置后的值：	用户设置的值														1	1

Bit	Symbol	位名称	Description	R/W
b22 to b0	SECMPUE2[22:0]	区域结束地址	区域结束的地址，用于区域确定。低2位读为1。取值范围应为400C0003h到400DFFFFh和40100003h到407FFFFFh。在选项设置存储器中设置该寄存器值时，低2位的写入值应为1。	R
b31 to b23	—	Reserved	这些位被读取为010000000b。在选项设置存储器中设置该寄存器值时，这些位的写入值应为010000000b。	R

16.6.1.9 安全MPU区域3起始地址寄存器(SECMPUS3)

Address(es): SECMPUS3 0000 0430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS3[22:16]						
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS3[15:0]															
重置后的值：	用户设置的值														0	0

Bit	Symbol	位名称	Description	R/W
b22 to b0	SECMPUS3[22:0]	区域起始地址	区域开始的地址，用于区域确定。低2位读为0。取值范围应为400C0000h到400DFFFCh和40100000h到407FFFFCh。在选项设置存储器中设置该寄存器值时，低2位的写入值应为0。	R
b31 to b23	—	Reserved	这些位被读取为010000000b。在选项设置存储器中设置该寄存器值时，这些位的写入值应为010000000b。	R

SECMPUS3和SECMPUE3寄存器指定安全功能的安全数据（400C0000h到400DFFFFh和40100000h到407FFFFFh）。SECMPUS3和SECMPUE3寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

16.6.1.10 Security MPU Region 3 End Address Register (SECMPUE3)

Address(es): SECMPUE3 0000 0434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22 to b0
	—	—	—	—	—	—	—	—	—	SECMPUE3[22:16]
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE3[15:0]															
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b22 to b0	SECMPUE3[22:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits are read as 1. The value range should be 400C 0003h to 400D FFFFh and 4010 0003h to 407F FFFFh. When setting this register value in the option-setting memory, the write value of the lower 2 bits should be 1.	R
b31 to b23	—	Reserved	These bits are read as 0100 0000 0b. When setting this register value in the option-setting memory, the write value of these bits should be 0100 0000 0b.	R

16.6.1.11 Security MPU Access Control Register (SECMPUAC)

Address(es): SECMPUAC 0000 0438h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
Value after reset:	1	1	1	1	1	1	The value set by user		1	1	1	1	The value set by user			

Bit	Symbol	Bit name	Description	R/W
b0	DIS0	Region 0 Disable	0: Security MPU region 0 enabled 1: Security MPU region 0 disabled.	R
b1	DIS1	Region 1 Disable	0: Security MPU region 1 enabled 1: Security MPU region 1 disabled.	R
b2	DIS2	Region 2 Disable	0: Security MPU region 2 enabled 1: Security MPU region 2 disabled.	R
b3	DIS3	Region 3 Disable	0: Security MPU region 3 enabled 1: Security MPU region 3 disabled.	R
b7 to b4	—	Reserved	These bits are read as 1. When setting this register value in the option-setting memory, the write value of bits [7:4] should be 1.	R
b8	DISPC0	PC Region 0 Disable	0: Security MPU PC region 0 enabled 1: Security MPU PC region 0 disabled.	R
b9	DISPC1	PC Region 1 Disable	0: Security MPU PC region 1 enabled 1: Security MPU PC region 1 disabled.	R
b15 to b10	—	Reserved	These bits are read as 1. When setting this register value in the option-setting memory, the write value of bits [15:10] should be 1.	R

Note: When flash memory is erased, the security MPU is disabled.

16.6.1.10 安全MPU区域3结束地址寄存器(SECMPUE3)

Address(es): SECMPUE3 0000 0434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22 to b0
	—	—	—	—	—	—	—	—	—	SECMPUE3[22:16]
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE3[15:0]															
重置后的值：	用户设置的值														1	1

Bit	Symbol	位名称	Description	R/W
b22 to b0	SECMPUE3[22:0]	区域结束地址	区域结束的地址，用于区域确定。低2位读为1。取值范围应为400C0003h到400DFFFFh和40100003h到407FFFFFh。在选项设置存储器中设置该寄存器值时，低2位的写入值应为1。	R
b31 to b23	—	Reserved	这些位被读取为010000000b。在选项设置存储器中设置该寄存器值时，这些位的写入值应为010000000b。	R

16.6.1.11 安全MPU访问控制寄存器(SECPUAC)

Address(es): SECMPUAC 0000 0438h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
重置后的值：	1	1	1	1	1	1	用户设置的值		1	1	1	1	用户设置的值			

Bit	Symbol	位名称	Description	R/W
b0	DIS0	区域0禁用	0：启用安全MPU区域01：禁用安全MPU区域0。	R
b1	DIS1	区域1禁用	0：启用安全MPU区域11：禁用安全MPU区域1。	R
b2	DIS2	区域2禁用	0：启用安全MPU区域21：禁用安全MPU区域2。	R
b3	DIS3	区域3禁用	0：启用安全MPU区域31：禁用安全MPU区域3。	R
b7 to b4	—	Reserved	这些位读为1。 在选项设置存储器中设置该寄存器值时，位[7:4]的写入值应为1。	R
b8	DISPC0	PC区域0禁用	0：启用安全MPUPC区域01：禁用安全MPUPC区域0。	R
b9	DISPC1	PC区域1禁用	0：启用安全MPUPC区域11：禁用安全MPUPC区域1。	R
b15 to b10	—	Reserved	这些位读为1。 在选项设置存储器中设置该寄存器值时，位[15:10]的写入值应为1。	R

Note: 当闪存被擦除时，安全MPU被禁用。

Note: To enable or disable the security MPU, see section 16.6.2, Memory Protection.

DIS0 bit (Region 0 Disable)

The DIS0 bit enables or disables the security MPU region 0. If security MPU region 0 is enabled, the code flash region within the limits set up by the SECMPUS0 and SECMPUE0 is secure data.

DIS1 bit (Region 1 Disable)

The DIS1 bit enables or disables the security MPU region 1. If security MPU region 1 is enabled, the SRAM region within the limits set up by the SECMPUS1 and SECMPUE1 is secure data.

DIS2 bit (Region 2 Disable)

The DIS2 bit enables or disables the security MPU region 2. If security MPU region 2 is enabled, the secure data of the security function region within the limits set up by the SECMPUS2 and the SECMPUE2 is secure data.

DIS3 bit (Region 3 Disable)

The DIS3 bit enables or disables the security MPU region 3. If security MPU region 3 is enabled, the secure data of the security function region within the limits set up by the SECMPUS3 and the SECMPUE3 is secure data.

DISPC0 bit (PC Region 0 Disable)

The DISPC0 bit enables or disables the security MPU PC region 0. If security MPU PC region 0 is enabled, the code flash or the SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0 contains a secure program.

DISPC1 bit (PC Region 1 Disable)

The DISPC1 bit enables or disables the security MPU PC region 1. If security MPU PC region 1 is enabled, the code flash or the SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1 contains a secure program.

16.6.2 Memory Protection

The security MPU protects the secured regions (the code flash, the SRAM, two security functions) from being accessed by programs other than a secure program. If access to a protected region is detected, the access becomes invalid.

When the security MPU is enabled, DISPC0 or DISPC1 in the Security MPU Access Control Register (SECMPUAC) must be set to 0, and DIS0, DIS1, DIS2, or DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 0.

When the security MPU is disabled, all bits in DISPC0, DISPC1, DIS0, DIS1, DIS2 and DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 1.

Other settings in the Security MPU Access Control Register (SECMPUAC) are prohibited.

The security MPU provides access protection in the following conditions:

- Secure data is accessed from a non-secure program
- Secure data is accessed from other than the CPU (DMAC, DTC)
- Secure data is accessed from the debugger.

Secure data is accessible only from a secure program.

Note: Secure program: Code flash or SRAM regions within the limits set up by the SECMPUPCS0 and SECMPUPCE0, Code flash or SRAM regions within the limits set up by SECMPUPCS1 and SECMPUPCE1.
Non-secure program: All regions outside the secure program.
Secure data: Code flash region within the limits set up by SECMPUS0 and SECMPUE0.
SRAM region within the limits set up by SECMPUS1 and SECMPUE1,
Security function region within the limits set up by SECMPUS2 and SECMPUE2,
Security function region within the limits set up by SECMPUS3 and SECMPUE3.

Note: 要启用或禁用安全MPU，请参阅第16.6.2节，内存保护。

DIS0位（区域0禁用）

DIS0位启用或禁用安全MPU区域0。如果启用安全MPU区域0，则在SECMPUS0和SECMPUE0设置的限制范围内的代码闪存区域是安全数据。

DIS1位（区域1禁用）

DIS1位启用或禁用安全MPU区域1。如果启用安全MPU区域1，则在SECMPUS1和SECMPUE1设置的限制范围内的SRAM区域是安全数据。

DIS2位（区域2禁用）

DIS2位启用或禁用安全MPU区域2。如果启用安全MPU区域2，则在SECMPUS2和SECMPUE2设置的限制范围内的安全功能区域的安全数据是安全数据。

DIS3位（区域3禁用）

DIS3位启用或禁用安全MPU区域3。如果启用安全MPU区域3，则在SECMPUS3和SECMPUE3设置的范围内的安全功能区域的安全数据是安全数据。

DISPC0位（PC区域0禁用）

DISPC0位启用或禁用安全MPUPC区域0。如果启用安全MPUPC区域0，则在SECMPUPCS0和SECMPUPCE0设置的限制范围内的代码闪存或SRAM区域包含安全程序。

DISPC1位（PC区域1禁用）

DISPC1位启用或禁用安全MPUPC区域1。如果启用安全MPUPC区域1，则在SECMPUPCS1和SECMPUPCE1设置的限制范围内的代码闪存或SRAM区域包含安全程序。

16.6.2 内存保护

安全MPU保护安全区域（代码闪存、SRAM、两个安全功能）不被安全程序以外的程序访问。如果检测到对受保护区域的访问，则访问变为无效。

启用安全MPU时，必须将安全MPU访问控制寄存器(SECMPUAC)中的DISPC0或DISPC1设置为0，并且必须将安全MPU访问控制寄存器(SECMPUAC)中的DIS0、DIS1、DIS2或DIS3设置为0.

禁用安全MPU时，安全MPU中DISPC0、DISPC1、DIS0、DIS1、DIS2和DIS3中的所有位访问控制寄存器(SECMPUAC)必须设置为1。

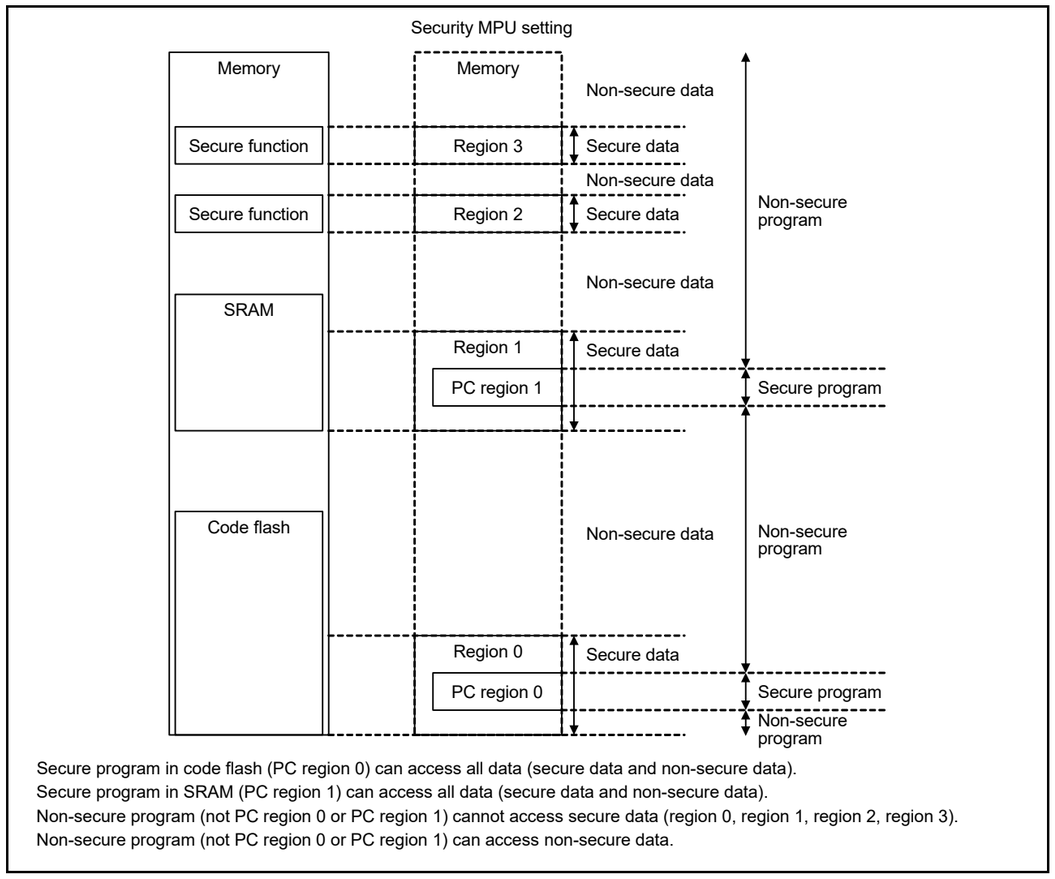
禁止安全MPU访问控制寄存器(SECMPUAC)中的其他设置。

安全MPU在以下情况下提供访问保护：

- 从非安全程序访问安全数据
- 从CPU以外的地方访问安全数据（DMAC、DTC）
- 从调试器访问安全数据。

安全数据只能从安全程序访问。

Note: 安全程序：在SECMPUPCS0和SECMPUPCE0设置的限制范围内对闪存或SRAM区域进行编码，
在SECMPUPCS1和SECMPUPCE1设置的限制范围内对闪存或SRAM区域进行编码。
非安全程序：安全程序之外的所有区域。
安全数据：在SECMPUS0和SECMPUE0设置的限制范围内编码闪存区域。
SRAM区域在SECMPUS1和SECMPUE1设置的范围内，
在SECMPUS2和SECMPUE2设置的范围内的安全功能区域，在SECMPUS3和SECMPUE3设置的范围内的安全功能区域。



Secure program in code flash (PC region 0) can access all data (secure data and non-secure data).
Secure program in SRAM (PC region 1) can access all data (secure data and non-secure data).
Non-secure program (not PC region 0 or PC region 1) cannot access secure data (region 0, region 1, region 2, region 3).
Non-secure program (not PC region 0 or PC region 1) can access non-secure data.

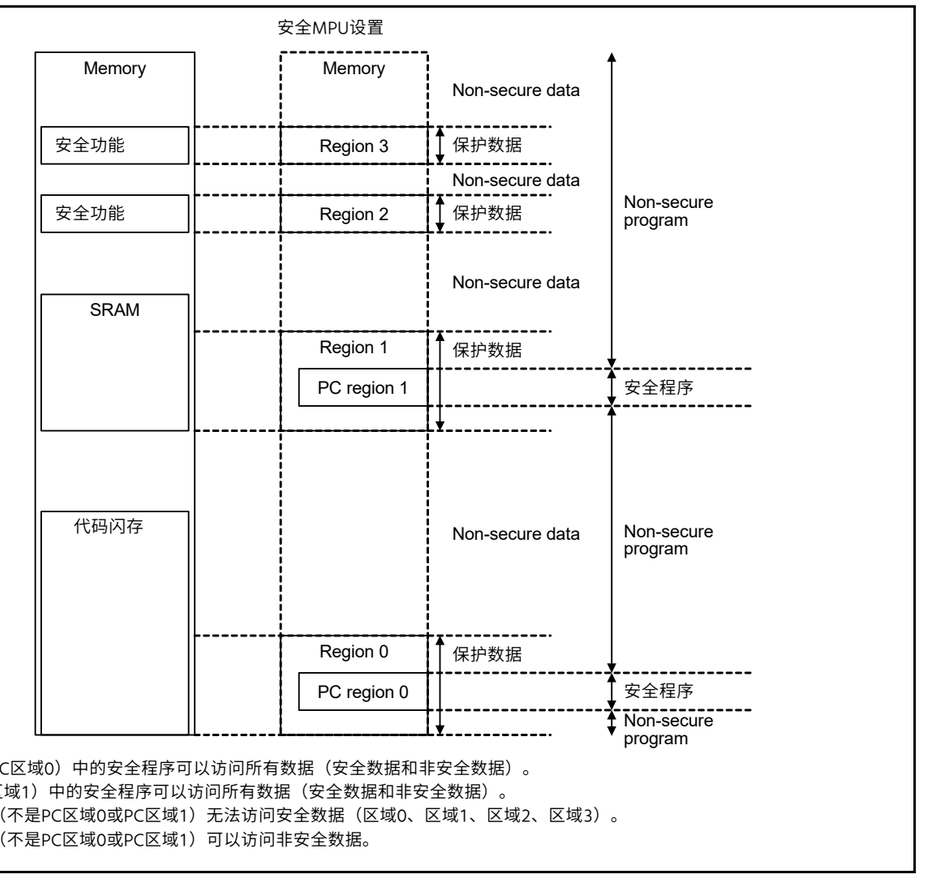
Figure 16.11 Use case of security MPU

16.6.3 Notes on Debug

The protected memory cannot be debugged if the security MPU is enabled. Disable the security MPU when debugging a secure program.

16.7 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D)
2. *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D)
3. *ARM®Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).



代码闪存（PC区域0）中的安全程序可以访问所有数据（安全数据和非安全数据）。
SRAM（PC区域1）中的安全程序可以访问所有数据（安全数据和非安全数据）。
非安全程序（不是PC区域0或PC区域1）无法访问安全数据（区域0、区域1、区域2、区域3）。
非安全程序（不是PC区域0或PC区域1）可以访问非安全数据。

Figure 16.11 安全MPU用例

16.6.3 调试注意事项

如果启用了安全MPU，则无法调试受保护的内存。调试安全程序时禁用安全MPU。

16.7 References

1. ARM®v7-M架构参考手册(ARMDDI0403D)
2. ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)
3. ARM®Cortex®-M4设备通用用户指南(ARMDUI0553A)。

17. DMA Controller (DMAC)

17.1 Overview

The MCU includes a 4-channel DMA Controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. Table 17.1 lists the DMAC specifications and Figure 17.1 shows a block diagram.

Table 17.1 DMAC specifications

Parameter		Description
Number of channels		4 channels (DMACm, m = 0 to 3)
Transfer space		4 GB (0000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer volume		64M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA activation source		Selectable for each channel: • Software trigger • Interrupt requests from peripheral modules or trigger from external interrupt input pins.*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Selectable free running mode (total number of data transfers is not specified).
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024.
	Block transfer mode	• One data block transfer by one DMA transfer request • Maximum settable block size: 1,024 data.
Selective functions	Extended repeat area function	• Allows data to be transferred by repeating the address values in the specified range, with the upper bit values in the transfer address register remaining fixed • Area of 2 bytes to 128 MB individually selectable as the extended repeat area for transfer source and destination.
Interrupt request (DMACm_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when: • The repeat size of data transfer is complete • The source address of the extended repeat area overflows • The destination address of the extended repeat area overflows.
Event link activation (DMACm_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred)
Module-stop function		Module-stop state can be set to reduce power consumption

Note 1. For details on DMAC activation sources, see Table 14.3, Interrupt Vector Table in section 14, Interrupt Controller Unit (ICU).

17. DMA Controller (DMAC)

17.1 Overview

MCU包括一个4通道DMA控制器(DMAC)，无需CPU干预即可传输数据。
当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。表17.1列出了DMAC规范，图17.1显示了框图。

Table 17.1 DMAC specifications

Parameter		Description
通道数		4个通道（DMACm，m=0到3）
转移空间		4GB（00000000h到FFFFFFFFh，不包括保留区域）
最大传输量		64M数据单元（块传输模式下的最大传输数：1 024个数据单元×65 536个块）
DMA激活源		每个通道可选择： 软件触发 来自外围模块的中断请求或来自外部中断输入引脚的触发。*1
通道优先级		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: highest)
传输数据	单一数据	位长：8、16、32位
	块大小	数据数量：1至1 024
传输模式	正常传输模式	一个DMA传输请求传输一个数据 可选择的自由运行模式（未指定数据传输的总数）。
	重复传输模式	通过一个DMA传输请求进行一次数据传输 完成为传输源或目标指定的重复数据传输大小后，程序返回传输起始地址 最大可设置重复大小：1 024。
	块传输模式	一个DMA传输请求传输一个数据块 最大可设置块大小：1 024个数据。
选择性功能	扩展重复区域功能	允许通过重复指定范围内的地址值来传输数据，传输地址寄存器中的高位值保持固定。 2字节到128MB的区域可以单独选择作为传输源和目标的扩展重复区域。
中断请求(DMACm_INT)	传输结束中断	在传输计数器指定的传输数据量完成时生成。
	传输转义结束中断	在以下情况下生成： 数据传输的重复大小已完成 扩展重复区域的源地址溢出 扩展重复区域的目标地址溢出。
事件链接激活(DMACm_INT)		每次数据传输后都会产生一个事件链接请求（对于块传输，在每个块传输后）
Module-stop function		可设置模块停止状态以降低功耗

Note 1. 有关DMAC激活源的详细信息，请参见第14节中断控制器单元(ICU)中的表14.3中断向量表。

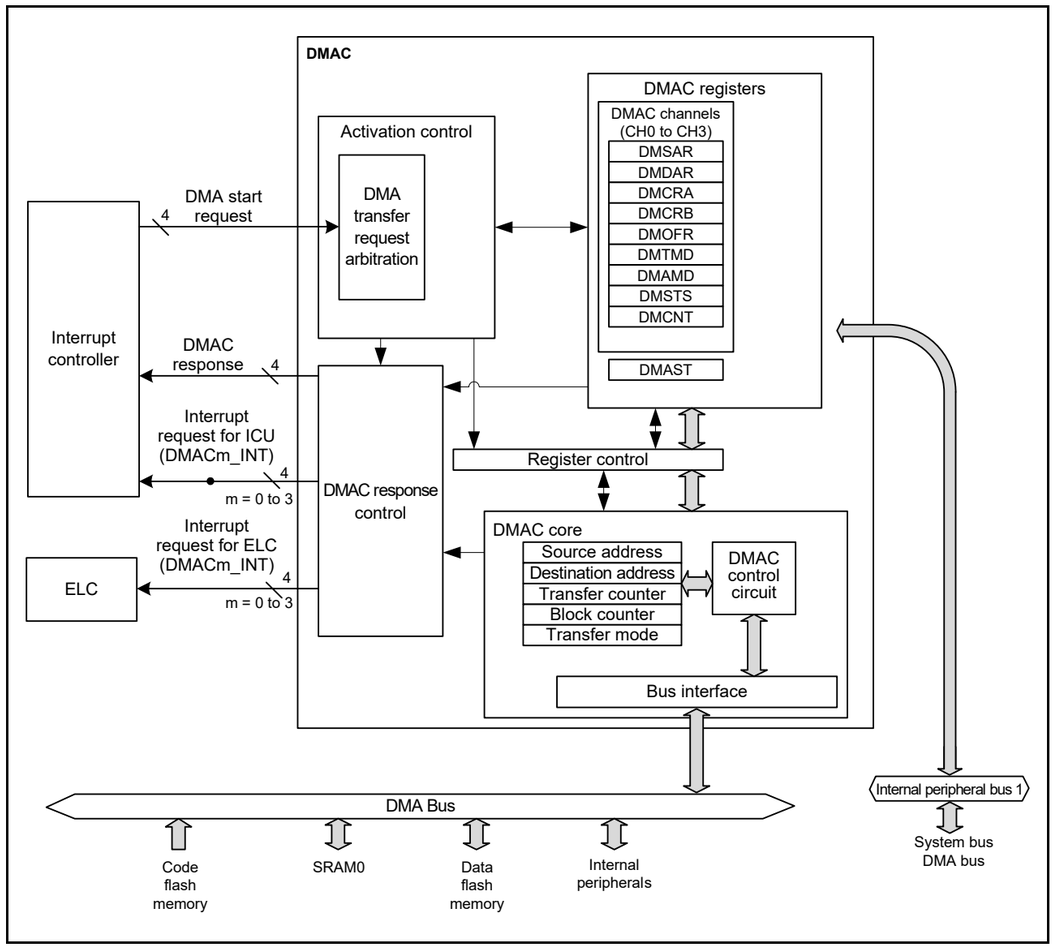


Figure 17.1 DMAC block diagram

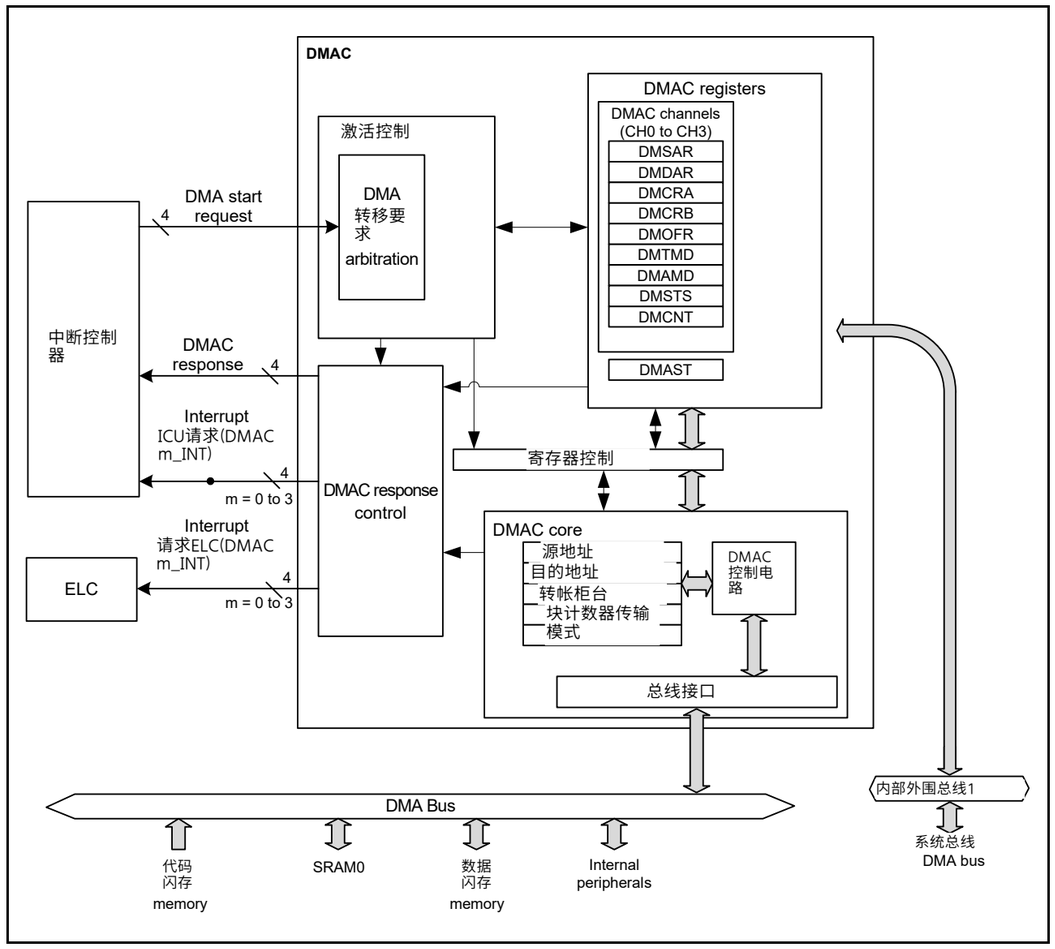


Figure 17.1 DMAC框图

17.2 Register Descriptions

17.2.1 DMA Source Address Register (DMSAR)

Address(es): DMAC0.DMSAR 4000 5000h, DMAC1.DMSAR 4000 5040h, DMAC2.DMSAR 4000 5080h, DMAC3.DMSAR 4000 50C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the transfer source start address	0000 0000h to FFFF FFFFh (4 GB)	R/W

Set DMSAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Note: Address alignment in this register must match the transfer data size value selected in the SZ bit in DMTMD.

17.2.2 DMA Destination Address Register (DMDAR)

Address(es): DMAC0.DMDAR 4000 5004h, DMAC1.DMDAR 4000 5044h, DMAC2.DMDAR 4000 5084h, DMAC3.DMDAR 4000 50C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the transfer destination start address	0000 0000h to FFFF FFFFh (4 GB)	R/W

Set DMDAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Note: Address alignment in this register must match the transfer data size value selected in the SZ bit in DMTMD.

17.2 注册说明

17.2.1 DMA源地址寄存器(DMSAR)

Address(es): DMAC0.DMSAR 4000 5000h, DMAC1.DMSAR 4000 5040h, DMAC2.DMSAR 4000 5080h, DMAC3.DMSAR 4000 50C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b31 to b0	指定传输源起始地址	0000 0000h to FFFF FFFFh (4 GB)	R/W

在禁用DMAC激活（DMAST中的DMST位=0）或禁用DMA传输（DMCNT中的DTE位=0）时设置DMSAR。

Note: 该寄存器中的地址对齐必须与在DMTMD的SZ位中选择的传输数据大小值相匹配。

17.2.2 DMA目标地址寄存器(DMDAR)

Address(es): DMAC0.DMDAR 4000 5004h, DMAC1.DMDAR 4000 5044h, DMAC2.DMDAR 4000 5084h, DMAC3.DMDAR 4000 50C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b31 to b0	指定传输目标起始地址	0000 0000h to FFFF FFFFh (4 GB)	R/W

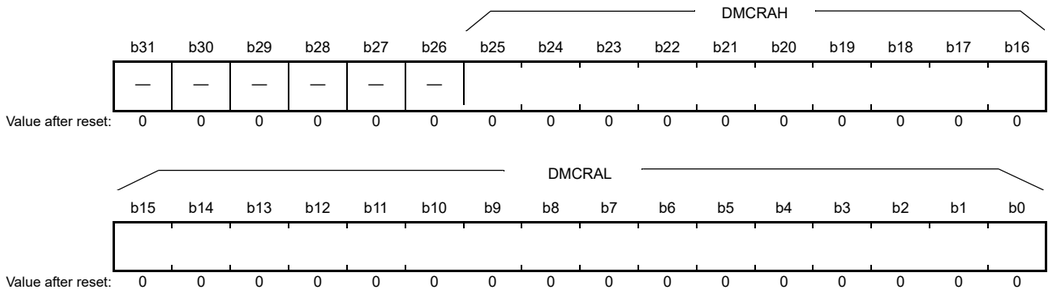
在禁用DMAC激活（DMAST中的DMST位=0）或禁用DMA传输（DMCNT中的DTE位=0）时设置DMDAR。

Note: 该寄存器中的地址对齐必须与在DMTMD的SZ位中选择的传输数据大小值相匹配。

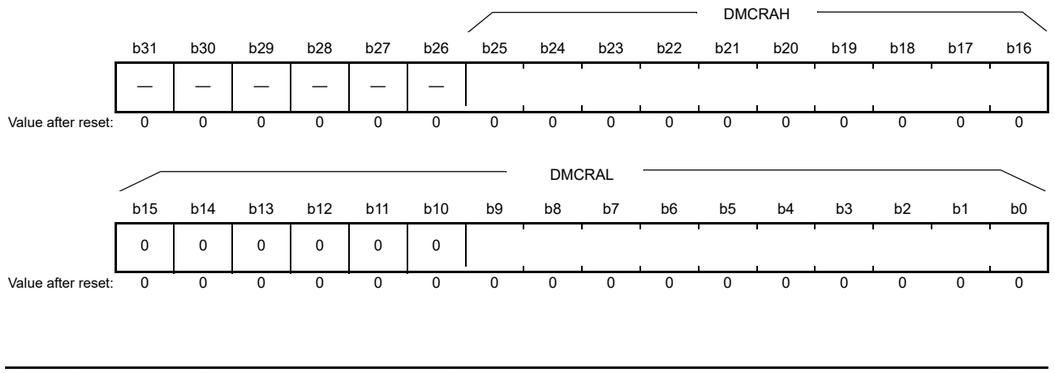
17.2.3 DMA Transfer Count Register (DMCRA)

Address(es): DMAC0.DMCRA 4000 5008h, DMAC1.DMCRA 4000 5048h, DMAC2.DMCRA 4000 5088h, DMAC3.DMCRA 4000 50C8h

- Normal transfer mode



- Repeat transfer mode, block transfer mode



Symbol	Bit name	Description	R/W
DMCRAL	Lower bits of transfer count	Specifies the number of transfer operations	R/W
DMCRAH	Upper bits of transfer count		R/W

Note: In repeat and block transfer modes, set the same value for DMCRAH and DMCRAL.

(1) Normal transfer mode (MD[1:0] bits in DMACm.DMTMD = 00b)

In normal transfer mode, DMCRAL functions as a 16-bit transfer counter. The number of transfer operations is one when the setting is 0001h, and 65,535 when it is FFFFh. The value is decremented by one each time data is transferred. A setting of 0000h indicates an unspecified number of transfer operations. Data transfer is performed with the transfer counter stopped, that is, in free running mode.

Do not use DMCRAH in normal transfer mode. Write 0000h to DMCRAH.

(2) Repeat transfer mode (MD[1:0] bits in DMACm.DMTMD = 01b)

In repeat transfer mode, DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter. The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In this mode, a value in the range of 000h to 3FFh (1 to 1024) can be set for DMCRAH and DMCRAL.

Setting bits [15:10] in DMCRAL is invalid. Write 0 to these bits. The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which time the value in DMCRAH is loaded into DMCRAL.

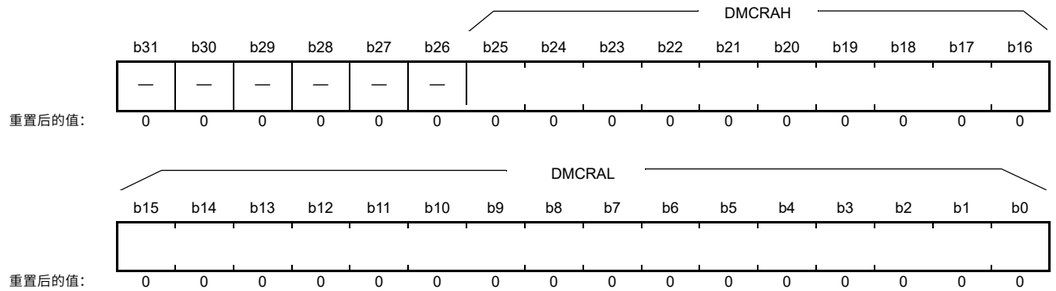
(3) Block transfer mode (MD[1:0] bits in DMACm.DMTMD = 10b)

In block transfer mode, DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter. The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In this mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.

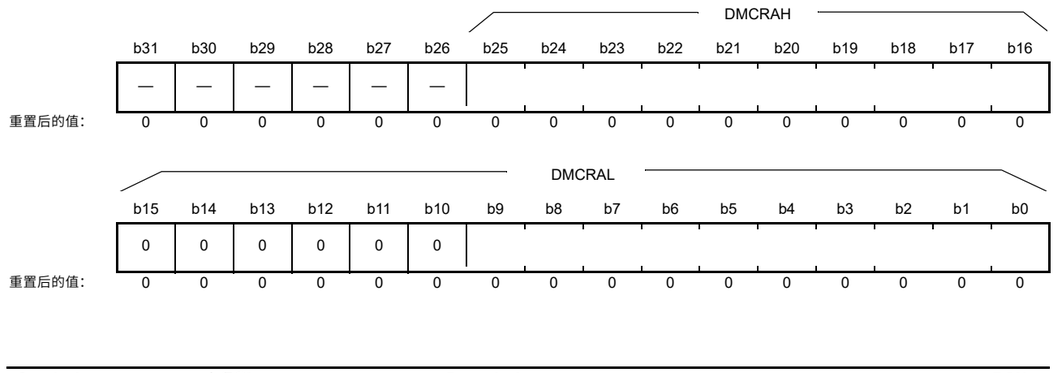
17.2.3 DMA传输计数寄存器(DMCRA)

Address(es): DMAC0.DMCRA 4000 5008h, DMAC1.DMCRA 4000 5048h, DMAC2.DMCRA 4000 5088h, DMAC3.DMCRA 4000 50C8h

正常传输模式



重复传输模式、块传输模式



Symbol	位名称	Description	R/W
DMCRAL	传输计数的低位	指定传输操作的次数	R/W
DMCRAH	传输计数的高位		R/W

Note: 在重复和块传输模式下，为DMCRAH和DMCRAL设置相同的值。

(1) 正常传输模式（DMACm.DMTMD=00b中的MD[1:0]位）

在正常传输模式下，DMCRAL用作16位传输计数器。设置为0001h时传输操作数为1，设置为FFFFh时为65 535。每次传输数据时，该值减一。设置为0000h表示未指定数量的传输操作。数据传输是在传输计数器停止的情况下执行的，即在自由运行模式下。

不要在正常传输模式下使用DMCRAH。将0000h写入DMCRAH。

(2) 重复传输模式（DMACm.DMTMD=01b中的MD[1:0]位）

在重复传输模式下，DMCRAH指定重复大小，DMCRAL用作10位传输计数器。设置为001h时传输操作数为1，设置为3FFh时为1023，设置为000h时为1024。在此模式下，可以为DMCRAH和DMCRAL设置000h到3FFh（1到1024）范围内的值。

在DMCRAL中设置位[15:10]无效。将0写入这些位。每次传输数据时，DMCRAL中的值减1，直到到达000h，此时DMCRAH中的值被加载到DMCRAL中。

(3) 块传输模式（DMACm.DMTMD=10b中的MD[1:0]位）

在块传输模式下，DMCRAH指定块大小，DMCRAL用作10位块大小计数器。设置为001h时块大小为1，设置为3FFh时为1023，设置为000h时为1024。在此模式下，可以为DMCRAH和DMCRAL设置000h到3FFh范围内的值。

Setting bits [15:10] in DMCRAL is invalid. Write 0 to these bits. The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which time the value in DMCRAH is loaded into DMCRAL.

17.2.4 DMA Block Transfer Count Register (DMCRB)

Address(es): DMAC0.DMCRB 4000 500Ch, DMAC1.DMCRB 4000 504Ch, DMAC2.DMCRB 4000 508Ch, DMAC3.DMCRB 4000 50CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b15 to b0	Specifies the number of block transfer or repeat transfer operations	0001h to FFFFh (1 to 65,535) 0000h (65,536).	R/W

DMCRB specifies the number of operations in block and repeat transfer modes. The number of transfer operations is one when the setting is 0001h, 65,535 when it is FFFFh, and 65,536 when it is 0000h.

In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred. In block transfer mode, the value is decremented by one when the final data of one block size is transferred. Do not use DMCRB in normal transfer mode as the setting is invalid.

17.2.5 DMA Transfer Mode Register (DMTMD)

Address(es): DMAC0.DMTMD 4000 5010h, DMAC1.DMTMD 4000 5050h, DMAC2.DMTMD 4000 5090h, DMAC3.DMTMD 4000 50D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DCTG[1:0]	Transfer Request Source Select	b1 b0 0 0: Software 0 1: Interrupts*1 from peripheral modules or external interrupt input pins 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SZ[1:0]	Transfer Data Size Select	b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	DTS[1:0]	Repeat Area Select	b13 b12 0 0: The destination is specified as the repeat area or block area 0 1: The source is specified as the repeat area or block area 1 0: The repeat area or block area is not specified 1 1: Setting prohibited.	R/W
b15, b14	MD[1:0]	Transfer Mode Select	b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Setting prohibited.	R/W

Note 1. To select the DMAC activation source, use the DELSRn registers of the ICU. For details on DMAC activation sources, see Table 14.4, Event table in section 14, Interrupt Controller Unit (ICU).

在DMCRAL中设置位[15:10]无效。将0写入这些位。每次传输数据时，DMCRAL中的值减1，直到到达000h，此时DMCRAH中的值被加载到DMCRAL中。

17.2.4 DMA块传输计数寄存器(DMRCB)

Address(es): DMAC0.DMCRB 4000 500Ch, DMAC1.DMCRB 4000 504Ch, DMAC2.DMCRB 4000 508Ch, DMAC3.DMCRB 4000 50CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b15 to b0	指定块传输或重复传输操作的次数	0001h to FFFFh (1 to 65,535) 0000h (65,536).	R/W

DMCRB指定块和重复传输模式中的操作数。设置为0001h时传输操作数为1，设置为FFFFh时为65 535，设置为0000h时为65 536。

在重复传输模式下，当传输一个重复大小的最终数据时，该值减一。在块传输模式下，当传输一个块大小的最终数据时，该值减一。请勿在正常传输模式下使用DMCRB，因为该设置无效。

17.2.5 DMA传输模式寄存器(DMTMD)

Address(es): DMAC0.DMTMD 4000 5010h, DMAC1.DMTMD 4000 5050h, DMAC2.DMTMD 4000 5090h, DMAC3.DMTMD 4000 50D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DCTG[1:0]	转移要求 来源选择	b1b000：软件01：来自外围模块或外部中断输入引脚的中断*110：禁止设置11：禁止设置。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	SZ[1:0]	传输数据大小 Select	b9b800：8位01：16位 10：32位11：禁止设置 。	R/W
b11, b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13, b12	DTS[1:0]	重复区域选择	b13b1200：目标指定为重复区域或块区域01：源指定为重复区域或块区域10：不指定重复区域或块区域11：禁止设置。	R/W
b15, b14	MD[1:0]	传输模式选择	b15b1400：正常传送0 1：重复传送10：块传 送11：禁止设置。	R/W

Note 1. 要选择DMAC激活源，请使用ICU的DELSRn寄存器。有关DMAC激活源的详细信息，请参阅表14.4，第14节中的事件表，中断控制器单元(ICU)。

DTS[1:0] bits (Repeat Area Select)

The DTS[1:0] bits select either the source or destination as the repeat area in repeat transfer mode and the block area in block transfer mode. In normal transfer mode, these bit settings are invalid.

17.2.6 DMA Interrupt Setting Register (DMINT)

Address(es): DMAC0.DMINT 4000 5013h, DMAC1.DMINT 4000 5053h, DMAC2.DMINT 4000 5093h, DMAC3.DMINT 4000 50D3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable	0: Disable 1: Enable.	R/W
b1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable	0: Disable 1: Enable.	R/W
b2	RPTIE	Repeat Size End Interrupt Enable	0: Disable 1: Enable.	R/W
b3	ESIE	Transfer Escape End Interrupt Enable	0: Disable 1: Enable.	R/W
b4	DTIE	Transfer End Interrupt Enable	0: Disable 1: Enable.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0	R/W

DARIE bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow occurs on the destination address while this bit is set to 1, the DTE bit in DMCNT is set to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate an interrupt triggered by an extended repeat area overflow on the destination address.

When block transfer mode is used with the extended repeat area function, an interrupt occurs after completion of a 1-block size transfer. When the DTE bit is set to 1 in DMACm.DMCNT of the channel associated with the stopped transfer, the transfer resumes from the state it was in when the transfer stopped. When the extended repeat area is not specified for the destination address, this bit is ignored.

SARIE bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow occurs on the source address while this bit is set to 1, the DTE bit in DMCNT is set to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate an interrupt request triggered by an extended repeat area overflow on the source address.

When block transfer mode is used with the extended repeat area function, an interrupt occurs after completion of a 1-block size transfer. When the DTE bit is set to 1 in DMACm.DMCNT of the channel associated with the stopped transfer, the transfer resumes from the state it was in when the transfer stopped. When the extended repeat area is not specified for the source address, this bit is ignored.

RPTIE bit (Repeat Size End Interrupt Enable)

When the RPTIE bit is set to 1 in repeat transfer mode, the DTE bit in DMCNT is set to 0 after completion of a 1-repeat size data transfer. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request occurred. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (repeat area or block area is not specified).

When the RPTIE bit is set to 1 in block transfer mode, the DTE bit in DMCNT is set to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request occurred. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (repeat area or block area is not specified).

DTS[1:0]位（重复区域选择）

DTS[1:0]位在重复传输模式中选择源或目标作为重复区域，在块传输模式中选择块区域。在正常传输模式下，这些位设置无效。

17.2.6 DMA中断设置寄存器(DMINT)

Address(es): DMAC0.DMINT 4000 5013h, DMAC1.DMINT 4000 5053h, DMAC2.DMINT 4000 5093h, DMAC3.DMINT 4000 50D3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DARIE	目标地址扩展重复区域溢出中断使能	0：禁用1：启用。	R/W
b1	SARIE	源地址扩展重复区溢出中断使能	0：禁用1：启用。	R/W
b2	RPTIE	重复大小结束中断使能	0：禁用1：启用。	R/W
b3	ESIE	传输转义结束中断使能	0：禁用1：启用。	R/W
b4	DTIE	传输结束中断使能	0：禁用1：启用。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0	R/W

DARIE位（目标地址扩展重复区域溢出中断使能）

当该位为1时，当目的地址发生扩展重复区溢出时，DMCNT中的DTE位为0。同时，DMSTS中的ESIF标志位为1，表示由目标地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后会发生中断。当与停止传输关联的通道的DMACm.DMCNT中的DTE位设置为1时，传输将从传输停止时的状态恢复。当没有为目标地址指定扩展重复区域时，该位被忽略。

SARIE位（源地址扩展重复区溢出中断使能）

当该位为1时源地址发生扩展重复区溢出时，DMCNT中的DTE位为0。同时，DMSTS中的ESIF标志位为1，表示有中断请求由源地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后会发生中断。当与停止传输关联的通道的DMACm.DMCNT中的DTE位设置为1时，传输将从传输停止时的状态恢复。当源地址没有指定扩展重复区域时，该位被忽略。

RPTIE位（重复大小结束中断使能）

当RPTIE位在重复传输模式下设置为1时，DMCNT中的DTE位在完成1次重复大小的数据传输后设置为0。同时，DMSTS中的ESIF标志设置为1，表示发生了重复大小结束中断请求。即使DMTMD中的DTS[1:0]位为10b（未指定重复区域或块区域），也可以产生重复大小结束中断请求。

当RPTIE位在块传输模式下设置为1时，DMCNT中的DTE位在完成1块数据传输后设置为0，方法与重复传输模式相同。同时，DMSTS中的ESIF标志设置为1，表示发生了重复大小结束中断请求。即使DMTMD中的DTS[1:0]位为10b（未指定重复区域或块区域），也可以产生重复大小结束中断请求。

ESIE bit (Transfer Escape End Interrupt Enable)

The ESIE bit enables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that occur during DMA transfer. The interrupt occurs when this bit is 1 and the ESIF flag in DMSTS is set to 1. To clear the transfer escape end interrupt, clear this bit or the ESIF flag in DMSTS to 0.

DTIE bit (Transfer End Interrupt Enable)

The DTIE bit enables the transfer end interrupt request that occurs on completion of a specified number of data transfers. The interrupt occurs when this bit is 1 and the DTIF flag in DMSTS is set to 1. To clear the transfer end interrupt, clear this bit or the DTIF flag in DMSTS to 0.

17.2.7 DMA Address Mode Register (DMAMD)

Address(es): DMAC0.DMAMD 4000 5014h, DMAC1.DMAMD 4000 5054h, DMAC2.DMAMD 4000 5094h, DMAC3.DMAMD 4000 50D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SM[1:0]		—	SARA[4:0]					DM[1:0]		—	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DARA[4:0]	Destination Address Extended Repeat Area	Specifies the extended repeat area on the destination address. For details on the settings, see Table 17.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	DM[1:0]	Destination Address Update Mode	b7 b6 0 0: Destination address is fixed 0 1: Offset addition 1 0: Destination address is incremented 1 1: Destination address is decremented.	R/W
b12 to b8	SARA[4:0]	Source Address Extended Repeat Area	Specifies the extended repeat area on the source address. For details on the settings, see Table 17.2.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15, b14	SM[1:0]	Source Address Update Mode	b15 b14 0 0: Source address is fixed 0 1: Offset addition 1 0: Source address is incremented 1 1: Source address is decremented.	R/W

DARA[4:0] bits (Destination Address Extended Repeat Area)

The DARA[4:0] bits specify the extended repeat area on the destination address. The extended repeat area function is realized through an update of the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 MB. The start address of the extended repeat area is set when the lower address overflows the extended repeat area on an address increment. Similarly, the end address of the extended repeat area is set when the lower address underflows the extended repeat area on an address decrement.

Do not specify the extended repeat area on the destination address when a repeat area or block area is specified as the transfer destination. When repeat or block transfer is selected, and when DMACm.DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat or block area), write 00000b in the DARA[4:0] bits.

To request an interrupt when an overflow or underflow occurs in the extended repeat area, set the DARIE bit in DMINT to 1. Table 17.2 lists the extended repeat areas associated with each setting.

DM[1:0] bits (Destination Address Update Mode)

The DM[1:0] bits select the update mode for the destination address:

- When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively
- When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is

ESIE位（传输转义结束中断使能）

ESIE位使能在DMA传输期间发生的传输转义结束中断请求（重复大小结束中断请求和扩展重复区域溢出中断请求）。该位为1且DMSTS中的ESIF标志设置为1时发生中断。要清除传输转义结束中断，请将该位或DMSTS中的ESIF标志清除为0。

DTIE位（传输结束中断使能）

DTIE位使能在完成指定数量的数据传输时发生的传输结束中断请求。当该位为1且DMSTS中的DTIF标志设置为1时发生中断。要清除传输结束中断，请将该位或DMSTS中的DTIF标志清除为0。

17.2.7 DMA地址模式寄存器(DMAMD)

Address(es): DMAC0.DMAMD 4000 5014h, DMAC1.DMAMD 4000 5054h, DMAC2.DMAMD 4000 5094h, DMAC3.DMAMD 4000 50D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SM[1:0]		—	SARA[4:0]					DM[1:0]		—	DARA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DARA[4:0]	目标地址扩展 重复区	指定目标地址上的扩展重复区域。 有关设置的详细信息，请参见表17.2。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b7, b6	DM[1:0]	目的地地址更新 Mode	b7b600：目标地址固定01：偏移量加法1 0：目标地址增加11：目标地址减少。	R/W
b12 to b8	SARA[4:0]	源地址扩展 重复区	指定源地址上的扩展重复区域。有关设置的详细信息，请参见表17.2。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b15, b14	SM[1:0]	源地址更新模式	b15b1400：源地址固定01：偏移量加法10：源地址递增11：源地址递减。	R/W

DARA[4:0]位（目标地址扩展重复区域）

DARA[4:0]位指定目标地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，而其余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意二的幂。当低地址在地址增量上溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，在地址减量时，当低位地址下溢扩展重复区域时，设置扩展重复区域的结束地址。

将重复区域或块区域指定为传送目标时，请勿在目标地址上指定扩展重复区域。选择重复或块传输时，并且当DMACm.DMTMD.DTS[1:0]=00b（传输目标指定为重复或块区域）时，将00000b写入DARA[4:0]位。

要在扩展重复区域发生上溢或下溢时请求中断，请将DMINT中的DARIE位设置为1。表17.2列出了与每个设置相关的扩展重复区域。

DM[1:0]位（目标地址更新模式）

DM[1:0]位选择目标地址的更新模式：

- WhenincrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thedestinationaddressisincrementedby1 2 and4 respectively
- WhendecrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thedestinationaddressis

decremented by 1, 2, and 4, respectively

- When offset addition is selected, the offset specified in the DMACm.DMOFR register is added to the address.

SARA[4:0] bits (Source Address Extended Repeat Area)

The SARA[4:0] bits specify the extended repeat area on the source address. The extended repeat area function is realized through an update of the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 MB. The start address of the extended repeat area is set when the lower address overflows the extended repeat area on an address increment. Similarly, the end address of the extended repeat area is set when the lower address underflows the extended repeat area on an address decrement.

Do not specify the extended repeat area on the source address when the repeat or block area is specified as a transfer source. When repeat or block transfer is selected, and when DMACm.DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat area or block area), write 00000b in the SARA[4:0] bits.

To request an interrupt when an overflow or underflow occurs in the extended repeat area, set the SARIE bit in DMINT to 1. Table 17.2 lists the extended repeat areas associated with each setting.

SM[1:0] (Source Address Update Mode)

The SM[1:0] bits select the update mode for the source address:

- When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively
- When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively
- When offset addition is selected, the offset specified in the DMACm.DMOFR register is added to the address.

Table 17.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (1 of 2)

SARA[4:0] or DARA[4:0]	Extended repeat area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 KB specified as extended repeat area by the lower 10 bits of the address
01011b	2 KB specified as extended repeat area by the lower 11 bits of the address
01100b	4 KB specified as extended repeat area by the lower 12 bits of the address
01101b	8 KB specified as extended repeat area by the lower 13 bits of the address
01110b	16 KB specified as extended repeat area by the lower 14 bits of the address
01111b	32 KB specified as extended repeat area by the lower 15 bits of the address
10000b	64 KB specified as extended repeat area by the lower 16 bits of the address
10001b	128 KB specified as extended repeat area by the lower 17 bits of the address
10010b	256 KB specified as extended repeat area by the lower 18 bits of the address
10011b	512 KB specified as extended repeat area by the lower 19 bits of the address
10100b	1 MB specified as extended repeat area by the lower 20 bits of the address
10101b	2 MB specified as extended repeat area by the lower 21 bits of the address
10110b	4 MB specified as extended repeat area by the lower 22 bits of the address

分别递减1、2和4

- 选择偏移添加后，将dmacm.dmofr寄存器中指定的偏移添加到地址中。

SARA[4:0]位（源地址扩展重复区）

SARA[4:0]位指定源地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，而其余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意二的幂。当低地址在地址增量上溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，在地址减量时，当低位地址下溢扩展重复区域时，设置扩展重复区域的结束地址。

当重复或块区域被指定为传输源时，不要在源地址上指定扩展重复区域。Whenrepeatorblocktransferisselected andwhenDMACm.DMTMD.DTS[1:0]=01b(thetransfersourceisspecifiedastherepeatareaorblockarea) write00000bintheSARA[4:0]bits.

要在扩展重复区域发生上溢或下溢时请求中断，请将DMINT中的SARIE位设置为1。表17.2列出了与每个设置相关的扩展重复区域。

SM[1:0]（源地址更新模式）

SM[1:0]位选择源地址的更新模式：

- WhenincrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thesourceaddressisincrementedby1 2 and4 respectively
- WhendecrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thesourceaddressisdecrementedby1 2 and4 respectively
- 选择偏移添加后，将dmacm.dmofr寄存器中指定的偏移添加到地址中。

Table 17.2 SARA[4:0]或DARA[4:0]设置和相应的重复区域（1of2）

SARA[4:0] or DARA[4:0]	扩展重复区域
00000b	未指定
00001b	由地址的低1位指定为扩展重复区域的2个字节
00010b	由地址的低2位指定为扩展重复区域的4个字节
00011b	由地址的低3位指定为扩展重复区域的8个字节
00100b	由地址的低4位指定为扩展重复区域的16个字节
00101b	由地址的低5位指定为扩展重复区域的32个字节
00110b	由地址的低6位指定为扩展重复区域的64个字节
00111b	由地址的低7位指定为扩展重复区域的128个字节
01000b	由地址的低8位指定为扩展重复区域的256个字节
01001b	由地址的低9位指定为扩展重复区域的512个字节
01010b	1KB由地址的低10位指定为扩展重复区域
01011b	2KB由地址的低11位指定为扩展重复区域
01100b	4KB由地址的低12位指定为扩展重复区域
01101b	8KB由地址的低13位指定为扩展重复区域
01110b	16KB由地址的低14位指定为扩展重复区域
01111b	32KB由地址的低15位指定为扩展重复区域
10000b	64KB由地址的低16位指定为扩展重复区域
10001b	128KB由地址的低17位指定为扩展重复区域
10010b	256KB由地址的低18位指定为扩展重复区域
10011b	512KB由地址的低19位指定为扩展重复区域
10100b	1MB由地址的低20位指定为扩展重复区域
10101b	2MB由地址的低21位指定为扩展重复区域
10110b	4MB由地址的低22位指定为扩展重复区域

Table 17.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (2 of 2)

SARA[4:0] or DARA[4:0]	Extended repeat area
10111b	8 MB specified as extended repeat area by the lower 23 bits of the address
11000b	16 MB specified as extended repeat area by the lower 24 bits of the address
11001b	32 MB specified as extended repeat area by the lower 25 bits of the address
11010b	64 MB specified as extended repeat area by the lower 26 bits of the address
11011b	128 MB specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited

17.2.8 DMA Offset Register (DMOFR)

Address(es): DMAC0.DMOFR 4000 5018h, DMAC1.DMOFR 4000 5058h, DMAC2.DMOFR 4000 5098h, DMAC3.DMOFR 4000 50D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination	0000 0000h to 00FF FFFFh (0 bytes to (16 MB – 1 byte)) FF00 0000h to FFFF FFFFh (-16 MB to -1 byte)	R/W

Only write to this register while the DMAC operation is stopped or DMA transfer is disabled, but not during data transfer. Setting bits [31:25] is invalid. The value in bit [24] is extended to bits [31:25]. Reading DMOFR returns the extended value.

17.2.9 DMA Transfer Enable Register (DMCNT)

Address(es): DMAC0.DMCNT 4000 501Ch, DMAC1.DMCNT 4000 505Ch, DMAC2.DMCNT 4000 509Ch, DMAC3.DMCNT 4000 50DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTE	DMA Transfer Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTE bit (DMA Transfer Enable)

The DTE bit enables DMA transfer. To enable DMA transfer, set the DMST bit in DMAST to 1 to enable DMAC activation, and then set the DTE bit to 1 to enable DMA transfer for the associated channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

Table 17.2 SARA[4:0]或DARA[4:0]设置和相应的重复区域(2of2)

SARA[4:0] or DARA[4:0]	扩展重复区域
10111b	8MB由地址的低23位指定为扩展重复区域
11000b	16MB由地址的低24位指定为扩展重复区域
11001b	32MB由地址的低25位指定为扩展重复区域
11010b	64MB由地址的低26位指定为扩展重复区域
11011b	128MB由地址的低27位指定为扩展重复区域
11100b to 11111b	禁止设定

17.2.8 DMA偏移寄存器(DMOFR)

Address(es): DMAC0.DMOFR 4000 5018h, DMAC1.DMOFR 4000 5058h, DMAC2.DMOFR 4000 5098h, DMAC3.DMOFR 4000 50D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b31 to b0	Specifiestheoffsetwhenoffsetadditionisselectedastheaddressupdatemodefortransfersourceordestination	00000000h至00FFFFFFh（0字节至（16MB 1字节））FF000000h至FFFFFFFFh（-16MB至-1字节）	R/W

仅当DMAC操作停止或禁用DMA传输时才写入该寄存器，而不是在数据传输期间。设置位[31:25]无效。位[24]中的值扩展到位[31:25]。读取DMOFR返回扩展值。

17.2.9 DMA传输使能寄存器(DMCNT)

Address(es): DMAC0.DMCNT 4000 501Ch, DMAC1.DMCNT 4000 505Ch, DMAC2.DMCNT 4000 509Ch, DMAC3.DMCNT 4000 50DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DTE	DMA传输使能	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DTE位（DMA传输使能）

DTE位启用DMA传输。要启用DMA传输，请将DMAST中的DMST位设置为1以启用DMAC激活，然后将DTE位设置为1以启用相关通道的DMA传输。

[Setting condition]

- 当1写入该位时。

[Clearing conditions]

- When 0 is written to this bit
- When the specified total volume of data transfer is complete
- When DMA transfer is stopped by a repeat size end interrupt
- When DMA transfer is stopped by an extended repeat area overflow interrupt.

17.2.10 DMA Software Start Register (DMREQ)

Address(es): DMAC0.DMREQ 4000 501Dh, DMAC1.DMREQ 4000 505Dh, DMAC2.DMREQ 4000 509Dh, DMAC3.DMREQ 4000 50DDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SWREQ	DMA Software Start	0: DMA transfer is not requested 1: DMA transfer is requested.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CLRS	DMA Software Start Bit Auto Clear Select	0: SWREQ bit is cleared after DMA transfer is started by software 1: SWREQ bit is not cleared after DMA transfer is started by software.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SWREQ bit (DMA Software Start)

Writing 1 to the SWREQ bit generates a DMA transfer request. After the DMA transfer starts, SWREQ is set to 0 if the CLRS bit is set to 0. SWREQ does not clear if CLRS bit is 1. The DMA transfer request can be issued again after the transfer is complete.

Note: Setting this bit is valid and DMA transfer by software is enabled only when the DCTG[1:0] bits in DMTMD are set to 00b, specifying software as the DMA activation source. Setting this bit is invalid when the DCTG[1:0] bits in DMTMD are set to any value other than 00b.

To start DMA transfer by software with the CLRS bit set to 0, ensure that the SWREQ bit is 0, and then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started with the CLRS bit set to 0 (the SWREQ bit is cleared after DMA transfer is started by software)
- When 0 is written to this bit.

CLRS bit (DMA Software Start Bit Auto Clear Select)

When an SWREQ setting of 1 triggers a transfer request, the CLRS bit specifies whether to clear the SWREQ bit to 0 after the DMA transfer starts. When the CLRS bit is set to 0, SWREQ is set to 0 after the DMA transfer starts. When the CLRS bit is set to 1, SWREQ does not clear to 0. The DMA transfer request can be issued again after the transfer is complete.

- 当0写入该位时
- 当指定的总数据传输量完成时
- 当DMA传输因重复大小结束中断而停止时
- 当DMA传输因扩展重复区域溢出中断而停止时。

17.2.10 DMA软件启动寄存器(DMREQ)

Address(es): DMAC0.DMREQ 4000 501Dh, DMAC1.DMREQ 4000 505Dh, DMAC2.DMREQ 4000 509Dh, DMAC3.DMREQ 4000 50DDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CLRS	—	—	—	SWREQ
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SWREQ	DMA软件启动	0：不请求DMA传输1：请求DMA传输。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	CLRS	DMA软件启动位自动清除选择	0：软件启动DMA传输后SWREQ位清零1：软件启动DMA传输后SWREQ位不清零。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SWREQ位（DMA软件启动）

将1写入SWREQ位会生成DMA传输请求。DMA传输开始后，SWREQ设置为0，如果CLRS位设置为0。如果CLRS位为1，则SWREQ不会清除。传输完成后可以再次发出DMA传输请求。

Note: 只有当DMTMD中的DCTG[1:0]位设置为00b时，设置该位才有效，并且通过软件启用DMA传输，将软件指定为DMA激活源。当DMTMD中的DCTG[1:0]位设置为00b以外的任何值时，设置该位无效。

在CLRS位设置为0的情况下通过软件启动DMA传输，确保SWREQ位为0，然后将1写入SWREQ bit.

[Setting condition]

- 当1写入该位时。

[Clearing conditions]

- 当软件的DMA传输请求被接受并且DMA传输开始时CLRS位设置为0（SWREQ位在软件启动DMA传输后清零）
- 当0写入该位时。

CLRS位（DMA软件起始位自动清除选择）

当SWREQ设置为1触发传输请求时，CLRS位指定在DMA传输开始后是否将SWREQ位清除为0。当CLRS位设置为0时，在DMA传输开始后SWREQ设置为0。当CLRS位设置为1时，SWREQ不会清为0。传输完成后可以再次发出DMA传输请求。

17.2.11 DMA Status Register (DMSTS)

Address(es): DMAC0.DMSTS 4000 501Eh, DMAC1.DMSTS 4000 505Eh, DMAC2.DMSTS 4000 509Eh, DMAC3.DMSTS 4000 50DEh

	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ESIF	Transfer Escape End Interrupt Flag	0: No interrupt occurred 1: Interrupt occurred.	R/W*1
b3 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R/W
b4	DTIF	Transfer End Interrupt Flag	0: No interrupt occurred 1: Interrupt occurred.	R/W*1
b6, b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R/W
b7	ACT	DMA Active Flag	0: DMAC operation suspended 1: DMAC operating.	R

Note 1. Only 0 can be written, to clear the flag.

ESIF flag (Transfer Escape End Interrupt Flag)

The ESIF flag indicates that the transfer escape end interrupt occurred.

[Setting conditions]

- In repeat transfer mode, when one repeat size data transfer completes with the RPTIE bit in DMINT set to 1
- In block transfer mode, when one block data transfer completes with the RPTIE bit in DMINT set to 1
- When an extended repeat area overflow on the source address occurs with the SARIE bit in DMINT is set to 1, and the SARA[4:0] bits in DMAMD set to any value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs with the DARIE bit in DMINT set to 1 and the DARA[4:0] bits in DMAMD set to any value other than 00000b (extended repeat area is specified on the transfer destination address).

[Clearing conditions]

- When 0 is written to this flag
- When 1 is written to the DTE bit in DMCNT.

DTIF flag (Transfer End Interrupt Flag)

The DTIF flag indicates that a transfer end interrupt occurred.

[Setting conditions]

- In normal transfer mode, when the specified number of unit transfers completes (DMCRAL becomes 0 on completion of transfer)
- In repeat transfer mode, when the specified number of repeat transfer operations completes (DMCRB becomes 0 on completion of transfer)
- In block transfer mode, when the specified number of blocks is transferred (DMCRB becomes 0 on completion of transfer).

[Clearing conditions]

- When 0 is written to this flag
- When 1 is written to the DTE bit in DMCNT.

17.2.11 DMA状态寄存器(DMSTS)

Address(es): DMAC0.DMSTS 4000 501Eh, DMAC1.DMSTS 4000 505Eh, DMAC2.DMSTS 4000 509Eh, DMAC3.DMSTS 4000 50DEh

	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	DTIF	—	—	—	ESIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ESIF	传输转义结束中断 Flag	0：未发生中断1：发生中断。	R/W*1
b3 to b1	—	Reserved	这些位被读取为0。写入这些位无效。	R/W
b4	DTIF	传输结束中断标志	0：未发生中断1：发生中断。	R/W*1
b6, b5	—	Reserved	这些位被读取为0。写入这些位无效。	R/W
b7	ACT	DMA活动标志	0：DMAC操作暂停1：DMAC操作。	R

Note 1. 只能写入0，以清除标志。

ESIF标志（传输转义结束中断标志）

ESIF标志表示发生了传输转义结束中断。

[Setting conditions]

- 在重复传输模式下，当一个重复大小的数据传输完成且DMINT中的RPTIE位设置为1时
- 在块传输模式下，当一个块数据传输完成且DMINT中的RPTIE位设置为1
- 当DMINT中的SARIE位设置为1且DMAMD中的SARA[4:0]位设置为00000b以外的任何值时，源地址发生扩展重复区域溢出时（扩展重复区域在传输源上指定地址）
- 当DMINT中的DARIE位设置为1且DMAMD中的DARA[4:0]位设置为00000b以外的任何值时，目标地址发生扩展重复区域溢出时（扩展重复区域在传输目标地址上指定）.

[Clearing conditions]

- 当0写入此标志时
- 当1写入DMCNT中的DTE位时。

DTIF标志（传输结束中断标志）

DTIF标志表示发生了传输结束中断。

[Setting conditions]

- 在正常传输模式下，当指定数量的单元传输完成时（传输完成后DMCRAL变为0）
- 在重复传输模式下，当指定数量的重复传输操作完成时（DMCRB在传输完成时变为0）
- 在块传输模式下，当传输指定数量的块时（DMCRB在传输完成时变为0）。

[Clearing conditions]

- 当0写入此标志时
- 当1写入DMCNT中的DTE位时。

ACT flag (DMA Active Flag)

The ACT flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts a data transfer.

[Clearing condition]

- When the data transfer in response to one transfer request completes.

17.2.12 DMAC Module Activation Register (DMAST)

Address(es): DMA.DMAST 4000 5200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DMST	DMAC Operation Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMST bit (DMAC Operation Enable)

Setting the DMST bit to 1 enables DMAC activation for all channels. When the DMST bit is set to 1 (DMAC activation is enabled), and 1 is written to the DMACm.DMCNT.DTE bit (DMA transfer is enabled) for multiple channels, all of the associated channels can be placed in the transfer request ready state at the same time.

When the DMST bit is set to 0 during DMA transfer, the DMA transfer is suspended after the current data transfer associated with a single transfer request is complete. To resume the DMA transfer, set the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit.

[Clearing condition]

- When 0 is written to this bit.

17.3 Operation

17.3.1 Transfer Mode

(1) Normal transfer mode

In normal transfer mode, one data unit is transferred for one transfer request. You can specify the number of transfer operations, up to a maximum of 65,535, in DMACm.DMCRAL. When these bits are set to 0000h, no number of operations is specified and data transfer is performed with the transfer counter stopped (free running mode). A transfer end interrupt request can be generated after completion of the specified number of transfer operations, except when in free running mode. Setting DMACm.DMCRB is invalid in normal transfer mode.

Table 17.3 summarizes the register update operation in normal transfer mode.

Table 17.3 Register update operation in normal transfer mode (1 of 2)

Register	Function	Update operation after completion of a transfer for one transfer request
DMACm.DMSAR	Transfer source address	Increment, decrement, fixed, or offset addition
DMACm.DMDAR	Transfer destination address	Increment, decrement, fixed, or offset addition

ACT标志（DMA活动标志）

ACT标志指示DMAC是处于空闲状态还是活动状态。

[Setting condition]

- 当DMAC开始数据传输时。

[Clearing condition]

- 当响应一个传输请求的数据传输完成时。

17.2.12 DMAC模块激活寄存器(DMAST)

Address(es): DMA.DMAST 4000 5200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DMST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DMST	DMAC操作使能	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DMST位（DMAC操作使能）

将DMST位设置为1启用所有通道的DMAC激活。当DMST位设置为1（启用DMAC激活），并为多个通道向DMA Cm.DMCNT.DTE位写入1（启用DMA传输）时，所有相关通道都可以置于传输请求就绪状态同时状态。

如果在DMA传输期间将DMST位设置为0，则在与单个传输请求相关的当前数据传输完成后，DMA传输将暂停。要恢复DMA传输，请再次将DMST位设置为1。

[Setting condition]

- 当1写入该位时。

[Clearing condition]

- 当0写入该位时。

17.3 Operation

17.3.1 传输模式

(1) 正常传输模式

在正常传输模式下，对于一个传输请求传输一个数据单元。您可以在DMACm.DMCRAL中指定传输操作的数量，最多为65 535。当这些位设置为0000h时，不指定操作数，并且在传输计数器停止的情况下执行数据传输（自由运行模式）。在完成指定数量的传输操作后，可以生成传输结束中断请求，自由运行模式除外。在正常传输模式下设置DMACm.DMCRB无效。

表17.3总结了正常传输模式下的寄存器更新操作。

Table 17.3 正常传输模式下的寄存器更新操作（1of2）

Register	Function	一个传输请求的传输完成后的更新操作
DMACm.DMSAR	传输源地址	递增、递减、固定或偏移添加
DMACm.DMDAR	转移目的地地址	递增、递减、固定或偏移添加

Table 17.3 Register update operation in normal transfer mode (2 of 2)

Register	Function	Update operation after completion of a transfer for one transfer request
DMACm.DMCRAL	Transfer count	Decremented by one or not updated (in free running mode)
DMACm.DMCRAH	-	Not updated (not used in normal transfer mode)
DMACm.DMCRB	-	Not updated (not used in normal transfer mode)

Figure 17.2 shows the operation in normal transfer mode.

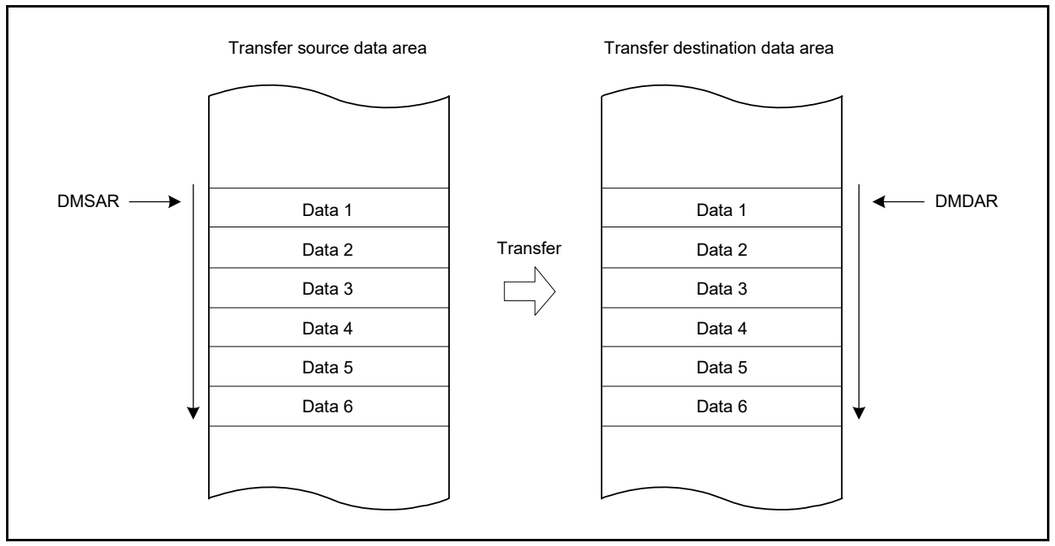


Figure 17.2 Operation in normal transfer mode

(2) Repeat transfer mode

In repeat transfer mode, one data unit is transferred for one transfer request.

The repeat transfer size, up to a maximum of 1K data units, is set in DMACm.DMCRA. The number of repeat transfers, up to a maximum number of 64K, is set in DMACm.DMCRB. The total data transfer size can be set to a maximum of 64M data units (1K data units × 64K repeat transfers).

You can specify either the transfer source or destination as a repeat area. When transfer of the repeat size data is complete, the address of the specified repeat area (DMSAR or DMDAR in DMACm) returns to the transfer start address. In this mode, when all data of the specified repeat size is transferred, the DMA transfer can be stopped and a repeat size end interrupt can be requested. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfers.

Table 17.4 summarizes the register update operation in repeat transfer mode, and Figure 17.3 shows the operation in repeat transfer mode.

Table 17.3 正常传输模式下的寄存器更新操作(2of2)

Register	Function	一个传输请求的传输完成后的更新操作
DMACm.DMCRAL	转移计数	减一或不更新（在自由运行模式下）
DMACm.DMCRAH	-	未更新（ 未在正常传输模式下使用）
DMACm.DMCRB	-	未更新（ 未在正常传输模式下使用）

图17.2显示了正常传输模式下的操作。

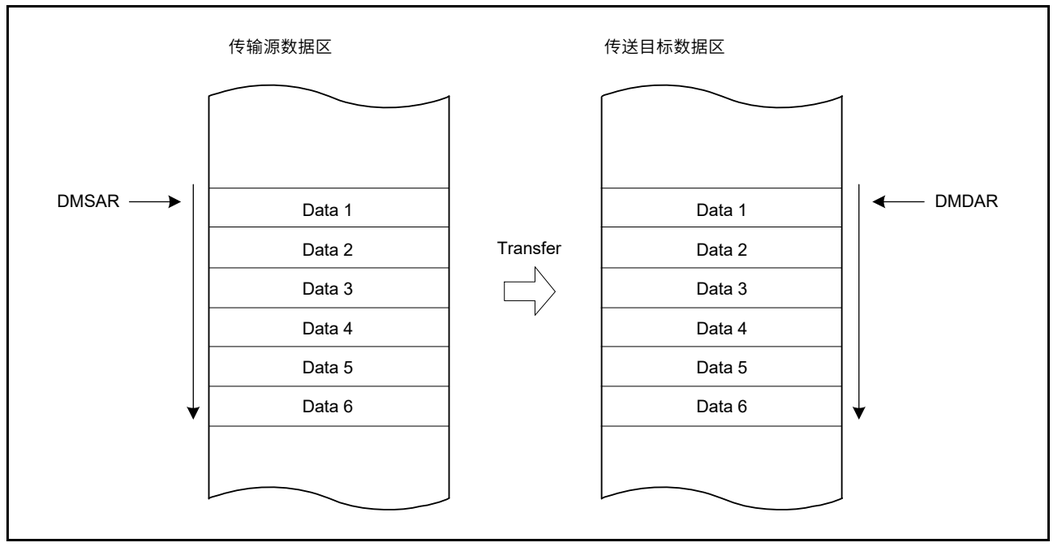


Figure 17.2 正常传输模式下的操作

(2) 重复传输模式

在重复传输模式中，对于一个传输请求传输一个数据单元。

在DMACm.DMCRA中设置了最多1K数据单元的重复传输大小。在DMACm.DMCRB中设置重复传输的数量，最大为64K。总数据传输大小最多可设置为64M数据单元（1K数据单元×64K重复传输）。

您可以将传输源或目标指定为重复区域。当重复大小数据的传输完成时，指定的重复区域（DMACm中的DMSAR或DMDAR）的地址返回到传输起始地址。在此模式下，当指定重复大小的所有数据都传输完毕后，可以停止DMA传输并请求重复大小结束中断。要恢复DMA传输，请在重复大小结束中断处理期间将1写入DMACm.DMCNT中的DTE位。

完成指定次数的重复传输后，可以产生传输结束中断请求。

表17.4总结了重复传输模式下的寄存器更新操作，图17.3显示了重复传输模式下的操作。

Table 17.4 Register update operation in repeat transfer mode

		Update operation after completion of a transfer for one transfer request	
Register	**Function**	**When DMACm.DMCRAL is not 1**	**When DMACm.DMCRAL is 1 (transfer of the last repeat size data unit)**
DMACm.DMSAR	Transfer source address	Increment, decrement, fixed, or offset addition	• DMACm.DMTMD.DTS[1:0] = 00b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMDAR	Transfer destination address	Increment, decrement, fixed, or offset addition	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment, decrement, fixed, offset addition • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMCRAH	Repeat size	Not updated	Not updated
DMACm.DMCRAL	Transfer count	Decremented by one	DMACm.DMCRAH
DMACm.DMCRB	Count of repeat transfer operations	Not updated	Decremented by one

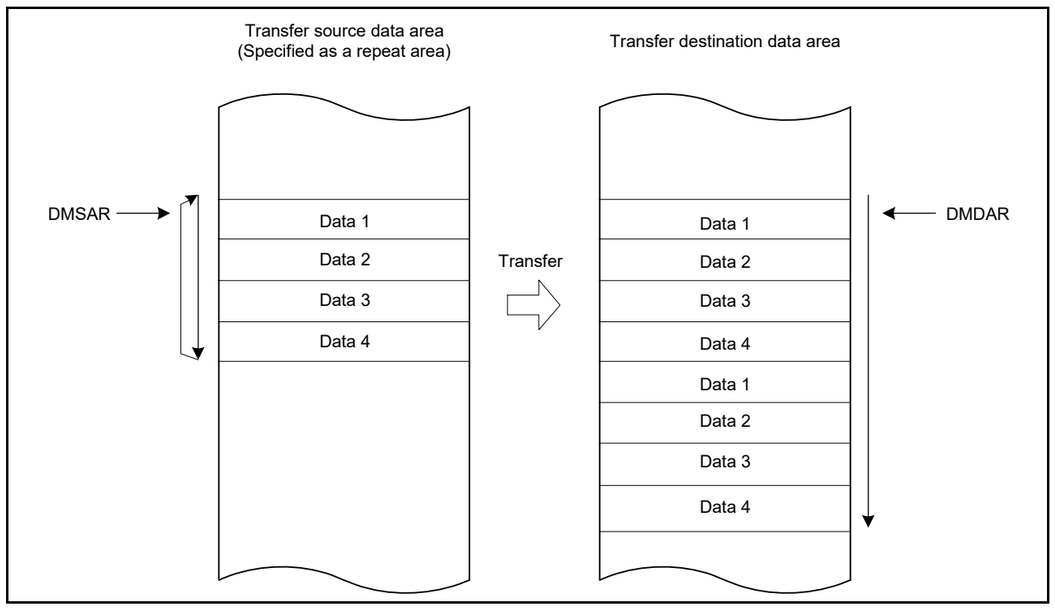


Figure 17.3 Operation in repeat transfer mode

(3) Block transfer mode

In block transfer mode, a single data block is transferred for one transfer request. The block transfer size, up to a maximum of 1K data units, is set in DMACm.DMCRA. The number of blocks transfers, up to a maximum of 64K, is set in DMACm.DMCRB. A total data transfer size up to a maximum of 64M data units (1K data units × 64K block transfers) can be set.

You can specify either the transfer source or destination as a block area. When transfer of a single data block is complete, the address of the specified block area (DMSAR or DMDAR in DMACm) returns to the transfer start address. In this

Table 17.4 重复传输模式下的寄存器更新操作

		一个传输请求的传输完成后的更新操作	
Register	**Function**	**当DMACm.DMCRAL不为1时**	**当DMACm.DMCRAL为1时（传输最后一个重复大小数据单元）**
DMACm.DMSAR	传输源地址	递增、递减、固定或偏移添加	• DMACm.DMTMD.DTS[1:0] = 00b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=01bDMACm.DMSAR的初始值 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加。
DMACm.DMDAR	转移目的地地址	递增、递减、固定或偏移添加	DMACm.DMTMD.DTS[1:0]=00bDMACm.DMDAR的初始值 DMACm.DMTMD.DTS[1:0]=01b 递增、递减、固定、偏移加法 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加。
DMACm.DMCRAH	重复大小	未更新	未更新
DMACm.DMCRAL	转移计数	减一	DMACm.DMCRAH
DMACm.DMCRB	重复传输操作的计数	未更新	减一

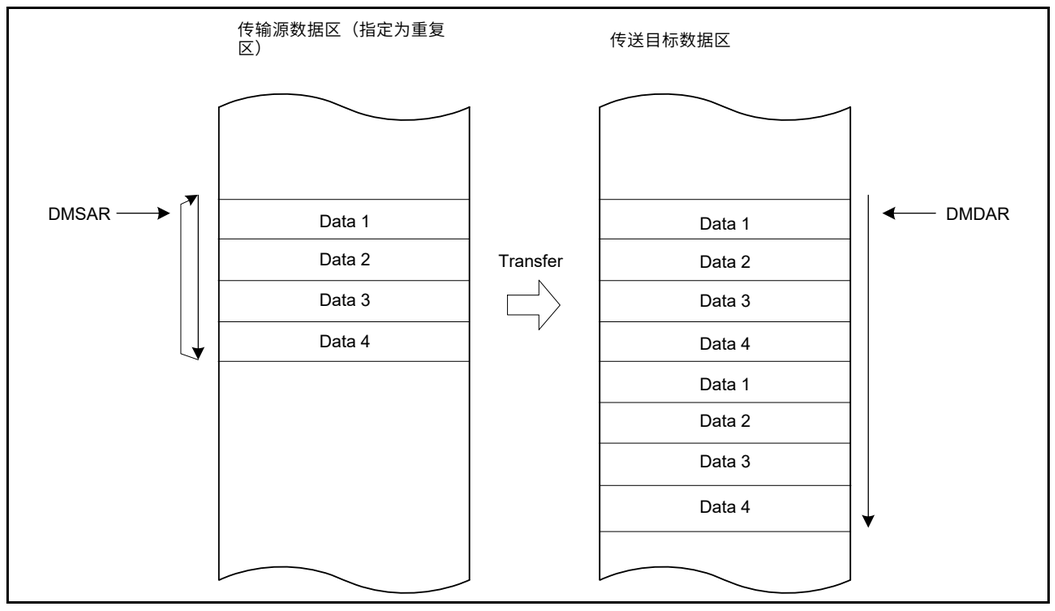


Figure 17.3 重复传输模式下的操作

(3) 块传输模式

在块传输模式下，为一个传输请求传输一个数据块。在DMACm.DMCRA中设置了最多1K个数据单元的块传输大小。在DMACm.DMCRB中设置了最多64K的块传输数。总数据传输大小最多可设置为64M数据单元（1K数据单元×64K块传输）。

您可以将传输源或目标指定为块区域。当单个数据块的传输完成时，指定块区域的地址（DMACm中的DMSAR或DMDAR）返回到传输起始地址。在这个

mode, when all data in a single block is transferred, you can stop DMA transfer and request a repeat size end interrupt. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of block transfers. Table 17.5 summarizes the register update operation in block transfer mode, and Figure 17.4 shows the operation in block transfer mode.

Table 17.5 Register update operation in block transfer mode

Register	Function	Update operation after completion of single-block transfer for one transfer request
DMACm.DMSAR	Transfer source address	• DMACm.DMTMD.DTS[1:0] = 00b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMDAR	Transfer destination address	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment, decrement,fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement,fixed, or offset addition.
DMACm.DMCRAH	Block size	Not updated
DMACm.DMCRAL	Transfer count	DMACm.DMCRAH
DMACm.DMCRB	Count of block transfer operations	Decremented by one

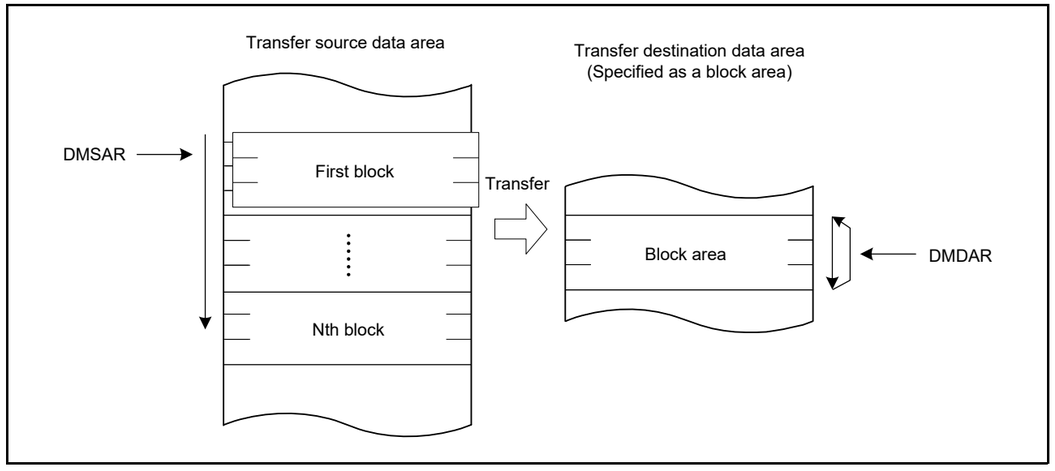


Figure 17.4 Operation in block transfer mode

17.3.2 Extended Repeat Area Function

The DMAC supports extended repeat areas on the transfer source and destination addresses, specified separately in the DMA Source Address Register (DMSAR) and DMA Destination Address Register (DMDAR) of DMACm. When this function is set, the address registers repeatedly indicate the addresses of the specified extended repeat areas. The extended repeat area on the source address is specified by the SARA[4:0] bits in DMACm.DMAMD.

The extended repeat area on the destination address is specified by the DARA[4:0] bits in DMACm.DMAMD. You can specify different sizes for the source and destination. However, you must not specify a transfer source or destination that is set as the repeat or block area as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an extended repeat area overflow interrupt can be requested. When an overflow

模式下，当单个块中的所有数据都传输完毕后，可以停止DMA传输并请求重复大小结束中断。要恢复DMA传输，请在重复大小结束中断处理期间将1写入DMACm.DMCNT中的DTE位。

完成指定数量的块传输后，可以产生传输结束中断请求。表17.5总结了块传输模式下的寄存器更新操作，图17.4显示了块传输模式下的操作。

Table 17.5 块传输模式下的寄存器更新操作

Register	Function	一个传输请求的单块传输完成后的更新操作
DMACm.DMSAR	传输源地址	• DMACm.DMTMD.DTS[1:0] = 00b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=01bDMACm.DMSAR的初始值 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加。
DMACm.DMDAR	转移目的地地址	DMACm.DMTMD.DTS[1:0]=00bDMACm.DMDAR的初始值 DMACm.DMTMD.DTS[1:0]=01b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加。
DMACm.DMCRAH	块大小	未更新
DMACm.DMCRAL	转移计数	DMACm.DMCRAH
DMACm.DMCRB	块传输操作的计数	减一

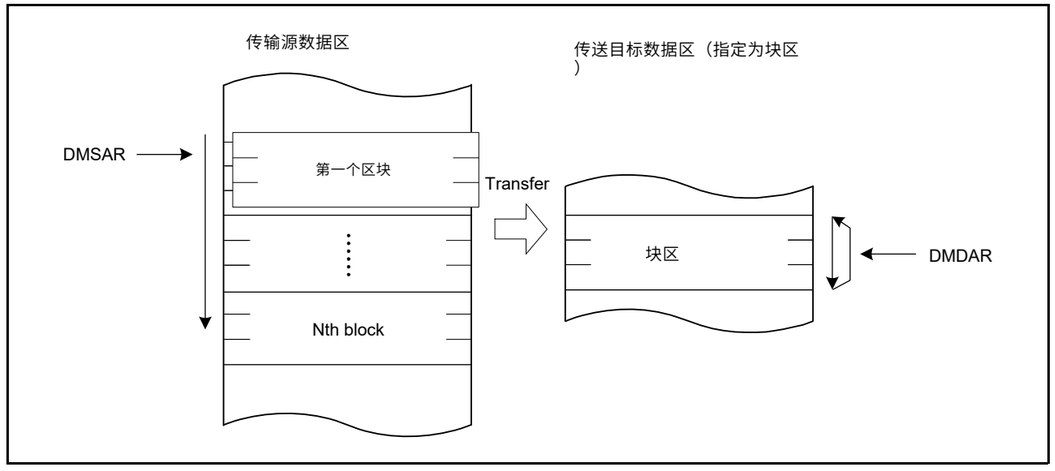


Figure 17.4 块传输模式下的操作

17.3.2 扩展重复区域功能

DMAC支持传输源地址和目标地址上的扩展重复区域，分别在DMACm的DMA源地址寄存器(DMSAR)和DMA目标地址寄存器(DMDAR)中指定。设置此功能时，地址寄存器重复指示指定扩展重复区域的地址。源地址上的扩展重复区域由DMACm.DMAMD中的SARA[4:0]位指定。

目标地址上的扩展重复区域由DMACm.DMAMD中的DARA[4:0]位指定。您可以为源和目标指定不同的大小。但是，您不能将设置为重复或块区域的传输源或目标指定为扩展重复区域。

当地址寄存器值到达扩展重复区的结束地址且扩展重复区溢出时，停止DMA传输，可以请求扩展重复区溢出中断。当溢出

occurs in the extended repeat area on the transfer source while the SARIE bit in DMACm.DMINT is set to 1, the ESIF flag in DMACm.DMSTS is set to 1 and the DTE bit in DMACm.DMCNT is set to 0 to stop DMA transfer. At this point, if the ESIE bit in DMACm.DMINT is set to 1, an interrupt by an extended repeat area overflow is requested. When the DARIE bit in DMINT of DMACm is set to 1, the destination address register becomes a target for the function. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during interrupt handling.

Figure 17.5 shows an example of the extended repeat area operation.

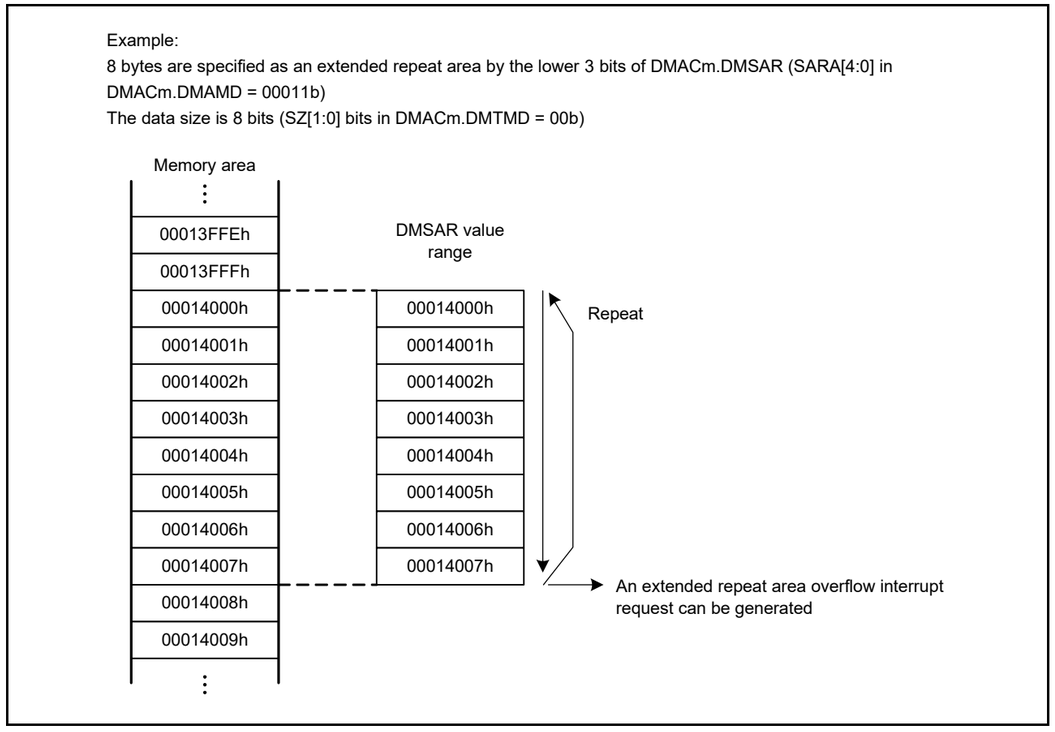


Figure 17.5 Example of extended repeat area operation

When using an extended repeat area overflow interrupt in block transfer mode, consider the following points:

- When a transfer is stopped by an extended repeat area overflow interrupt, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the overflow interrupt is suspended until transfer of the block is complete, and the transfer overruns.

当DMACm.DMINT中的SARIE位设置为1，DMACm.DMSTS中的ESIF标志设置为1，DMACm.DMCNT中的DTE位设置为0时，发生在传输源的扩展重复区域中以停止DMA传输.此时，如果DMACm.DMINT中的ESIE位设置为1，则请求由扩展重复区域溢出引起的中断。当DMACm的DMINT中的DARIE位设置为1时，目标地址寄存器成为函数的目标。要恢复DMA传输，请在中断处理期间将1写入DMACm.DMCNT中的DTE位。

图17.5显示了扩展重复区域操作的示例。

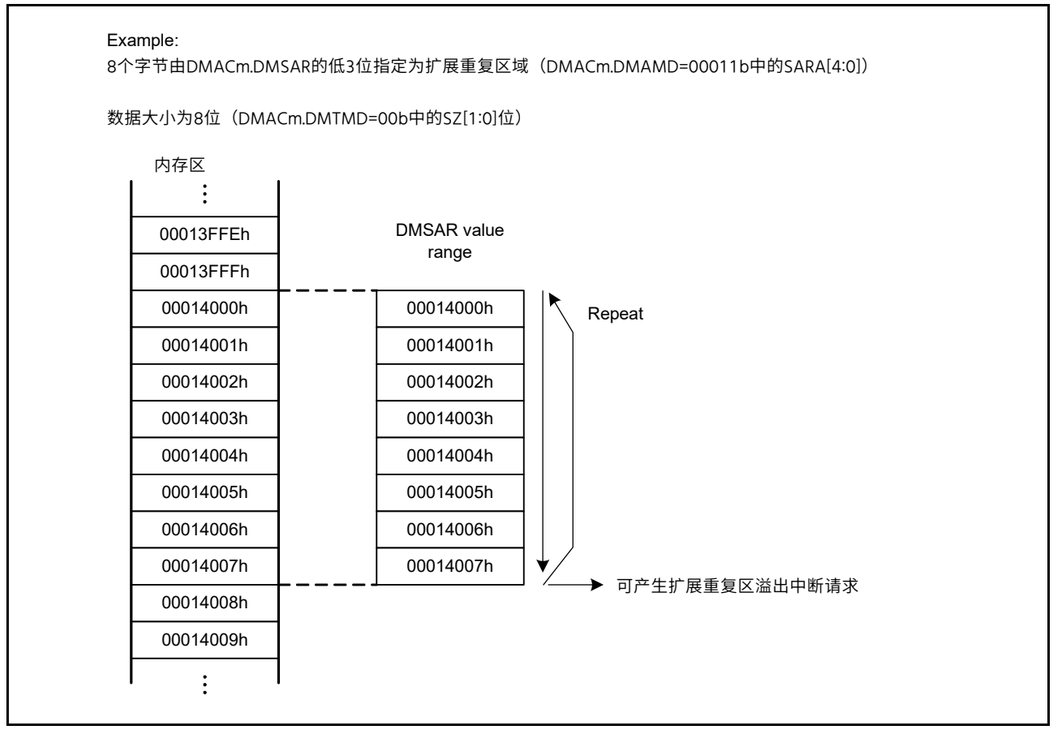


Figure 17.5 扩展重复区域操作示例

在块传输模式下使用扩展重复区域溢出中断时，请考虑以下几点：

- 当传输由扩展重复区域溢出中断停止时，地址寄存器必须设置为块大小为2的幂或块大小边界与扩展重复区域边界对齐。当一个块的传输过程中扩展重复区域发生溢出时，溢出中断被暂停，直到块的传输完成，传输溢出。

Figure 17.6 shows an example of using the extended repeat area function in block transfer mode.

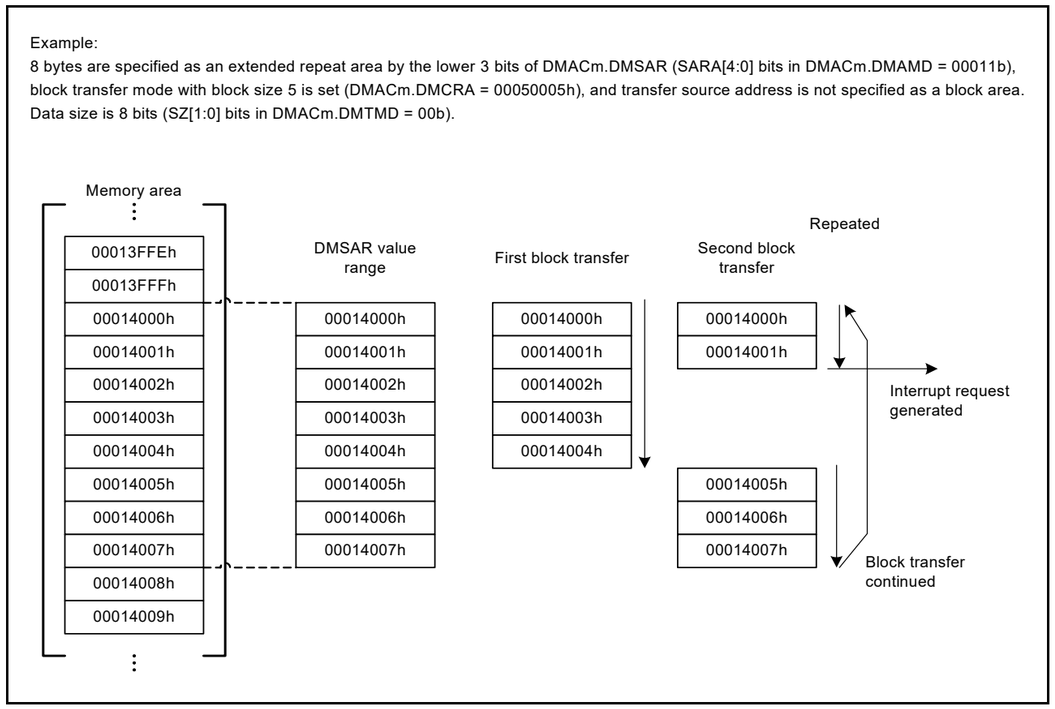


Figure 17.6 Example of extended repeat area function in block transfer mode

17.3.3 Address Update Function Using Offset

The source and destination addresses can be updated by fixing, incrementing, decrementing, or adding an offset. When offset addition is selected, the offset specified in the DMA Offset Register (DMACm.DMOFR) is added to the address every time the DMAC performs one data transfer. This function performs a data transfer when addresses are allocated to separated areas. You can also subtract an offset by setting a negative value in DMACm.DMOFR. The negative value must be in two's complement.

Table 17.6 shows the address update method in each address update mode.

Table 17.6 Address update method in each address update mode

Address update mode	Settings of DMACm.DMAMD.SM[1:0] and DMACm.DMAMD.DM[1:0] for address update modes	Address update method for different SZ[1:0] settings in DMACm.DMTMD		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

Note 1. When setting a negative value in the DMA Offset Register, the value must be in two's complement, obtained by the following formula:
two's complement of a negative offset value = ~ (offset) + 1 (~: bit inversion)

(1) Basic transfer using offset addition

Figure 17.7 shows an example of address updating using offset addition.

图17.6显示了在块传输模式下使用扩展重复区域功能的示例。

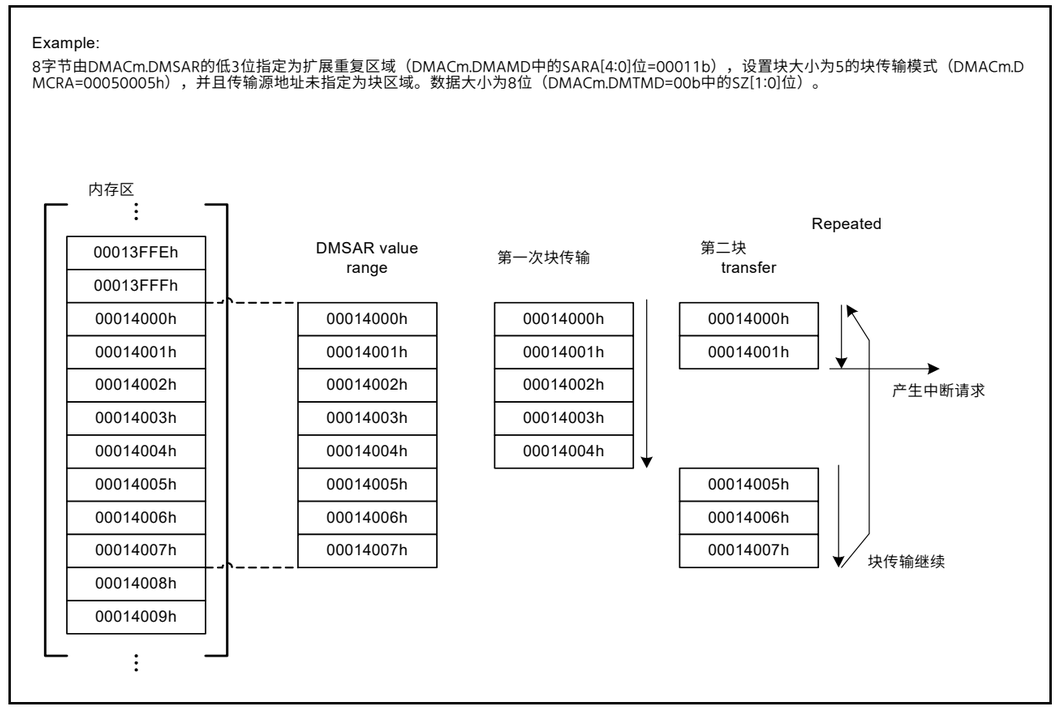


Figure 17.6 块传输模式下的扩展重复区域功能示例

17.3.3 使用偏移的地址更新功能

可以通过固定、递增、递减或添加偏移量来更新源地址和目标地址。选择偏移添加时，DMA偏移寄存器(DMACm.DMOFR)中指定的偏移会在每次DMAC执行一次数据传输时添加到地址。当地址被分配到不同的区域时，该函数执行数据传输。您还可以通过在DMACm.DMOFR中设置负值来减去偏移量。负值必须是二进制补码。

表17.6显示了每种地址更新模式下的地址更新方法。

Table 17.6 各地址更新模式下的地址更新方法

地址更新方式	的设置 DMACm.DMAMD.SM[1:0]和DMACm.DMAMD.DM[1:0]用于地址更新模式	不同SZ[1:0]设置的地址更新方法 DMACm.DMTMD		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
地址固定	00b	Fixed		
偏移量加法	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

Note 1. 在DMA偏移寄存器中设置负值时，该值必须是二进制补码，由以下公式获得：负偏移值的二进制补码=~（偏移量）+1（~：位反转）

(1) 使用偏移加法的基本传输

图17.7显示了使用偏移量加法进行地址更新的示例。

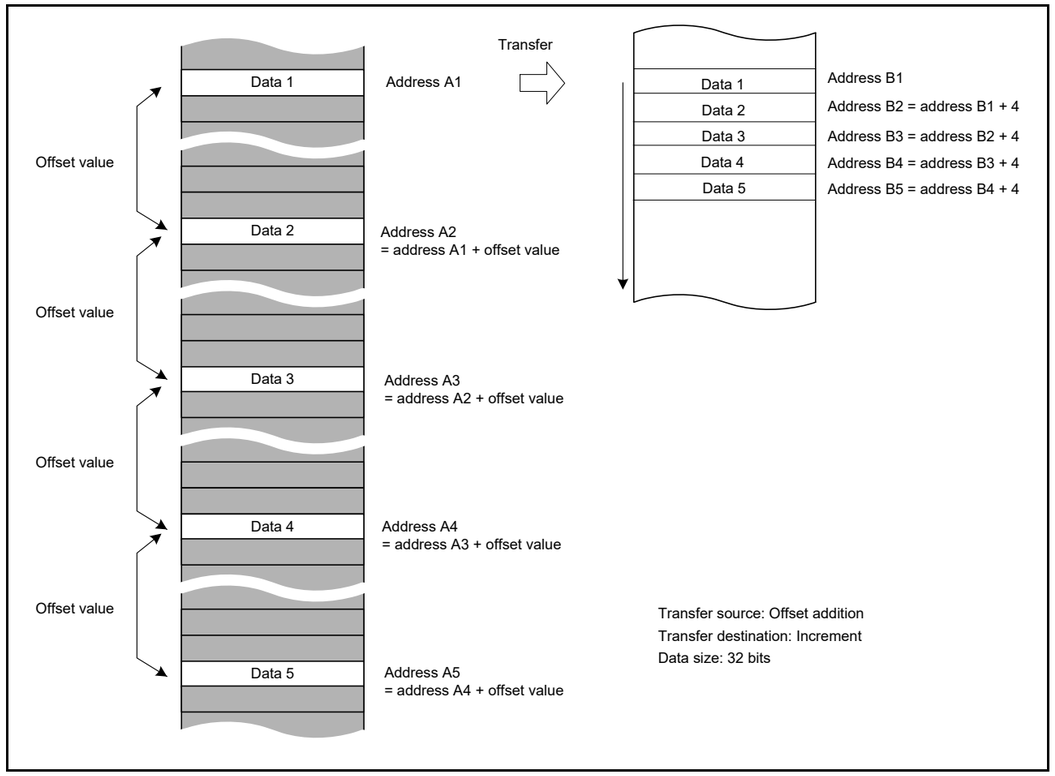


Figure 17.7 Example of address updating through offset addition

In Figure 17.7:

- The transfer data is 32 bits long
- Offset addition is set as the transfer source address update mode
- Increment is set as the transfer destination address update mode.

The second and subsequent data units are each read from the source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to continuous locations on the destination.

(2) Example of XY conversion using offset addition

Figure 17.8 shows the XY conversion using offset addition in repeat transfer mode. The settings are as follows:

- DMAC0.DMAMD — Transfer source address update mode: offset addition
- DMAC0.DMAMD — Transfer destination address update mode: destination address is incremented
- DMAC0.DMTMD — Transfer data size select: 32 bits
- DMAC0.DMTMD — Transfer mode select: repeat transfer
- DMAC0.DMTMD — Repeat area select: the source is specified as the repeat area
- DMAC0.DMOFR — Offset address: 10h
- DMAC0.DMCRA — Repeat size: 4h
- DMAC0.DMINT — The repeat size end interrupt is enabled.

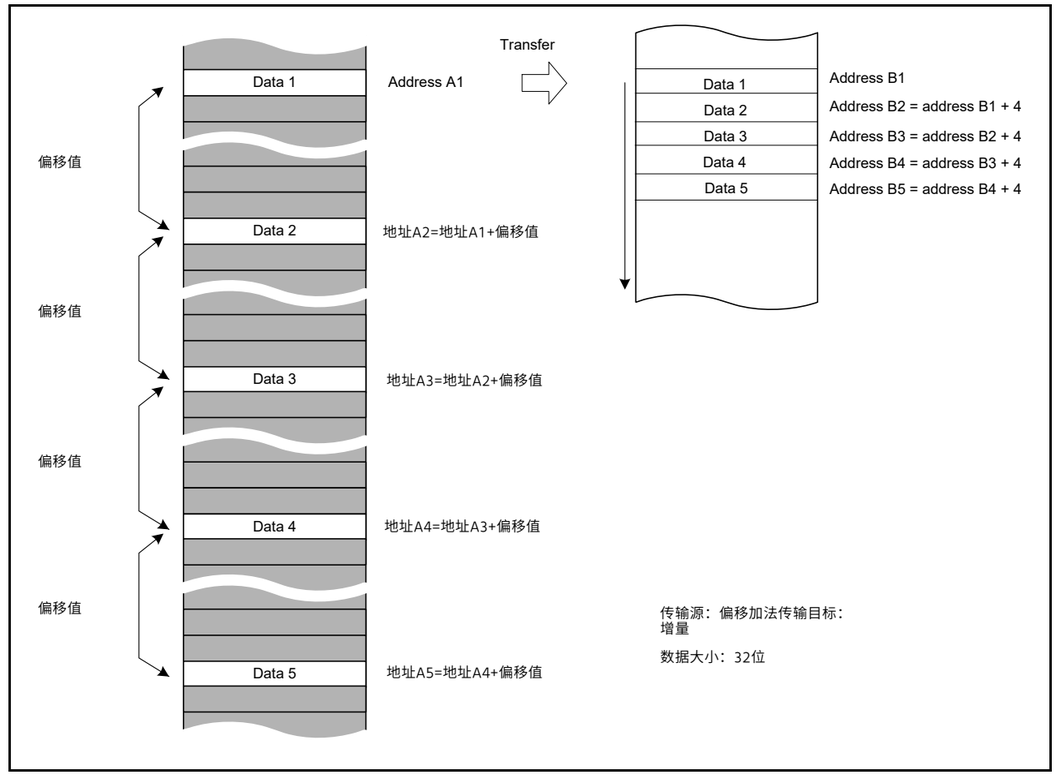


Figure 17.7 通过偏移量添加来更新地址的示例

在图17.7中：

- 传输数据为32位长
- 偏移量加法设置为传输源地址更新方式
- 增量设置为传送目的地地址更新模式。

第二个和随后的数据单元分别从通过将偏移值与前一个地址相加而获得的源地址读取。以指定间隔从地址读取的数据被写入目标上的连续位置。

(2) 使用偏移加法的XY转换示例

图17.8显示了在重复传输模式下使用偏移添加的XY转换。设置如下：

- DMAC0.DMAMD—传输源地址更新模式：偏移量加法
- DMAC0.DMAMD—传输目标地址更新模式：目标地址递增
- DMAC0.DMTMD—传输数据大小选择：32位
- DMAC0.DMTMD—传输模式选择：重复传输
- DMAC0.DMTMD—重复区域选择：源指定为重复区域
- DMAC0.DMOFR — Offset address: 10h
- DMAC0.DMCRA — Repeat size: 4h
- DMAC0.DMINT—启用重复大小结束中断。

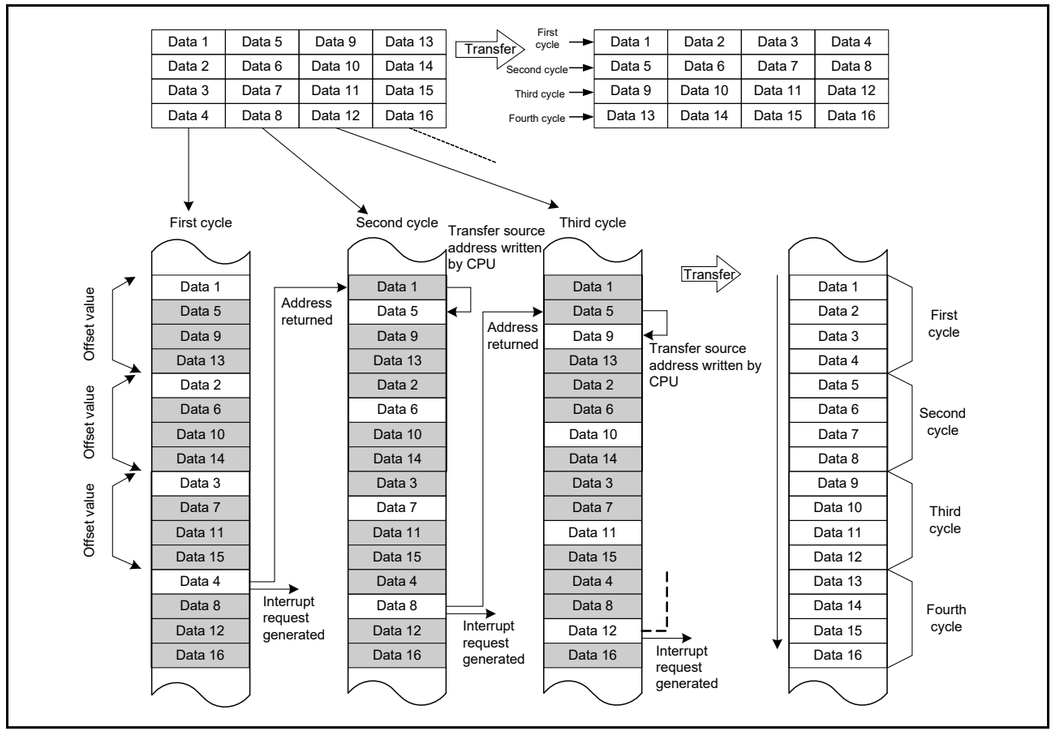


Figure 17.8 XY conversion operation using offset addition in repeat transfer mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to continuous destination addresses. When data 4 is transferred:

- The repeat size of the transfers is complete
- The transfer source address returns to the transfer start address (the address of data 1 on the transfer source)
- A repeat size end interrupt is requested.

During the time this interrupt pauses the transfer, perform the following:

- DMAC0.DMSAR — Rewrite the DMA transfer source address to the address of data 5 (in this example, the data 1 address + 4)
- DMAC0.DMCNT — Set the DTE bit to 1.

The DMA transfer resumes from the state when the DMA transfer was stopped. The same operations are repeated until the transfer source data is transposed to the destination area (XY conversion).

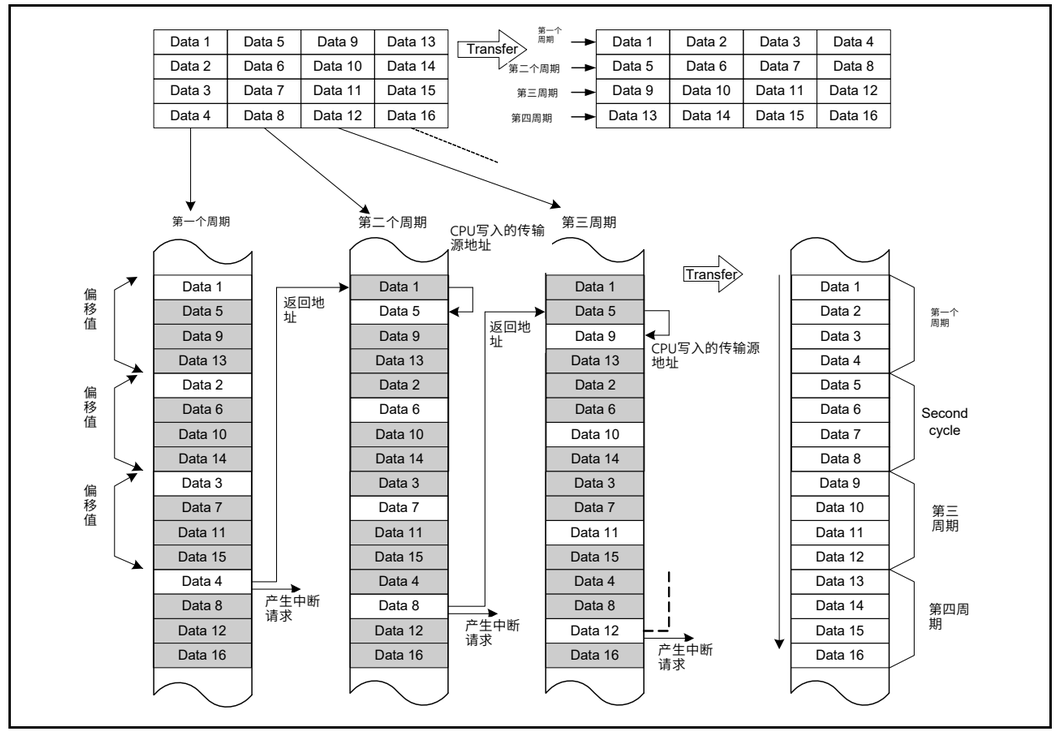


Figure 17.8 重复传输模式下使用偏移加法的XY转换操作

传输开始时，每次传输数据时，都会将偏移值添加到传输源地址。传输数据被写入连续的目标地址。传输数据4时：

- 传输的重复大小已完成
- 传输源地址返回传输起始地址（传输源上数据1的地址）
- 请求重复大小结束中断。

在此中断暂停传输期间，请执行以下操作：

- DMAC0.DMSAR—将DMA传输源地址重写为数据5的地址（在本例中，数据1地址+4）
- DMAC0.DMCNT—将DTE位设置为1。

DMA传输从DMA传输停止时的状态恢复。重复相同的操作，直到将传输源数据转置到目标区域（XY转换）。

Figure 17.9 shows a flow of the XY conversion.

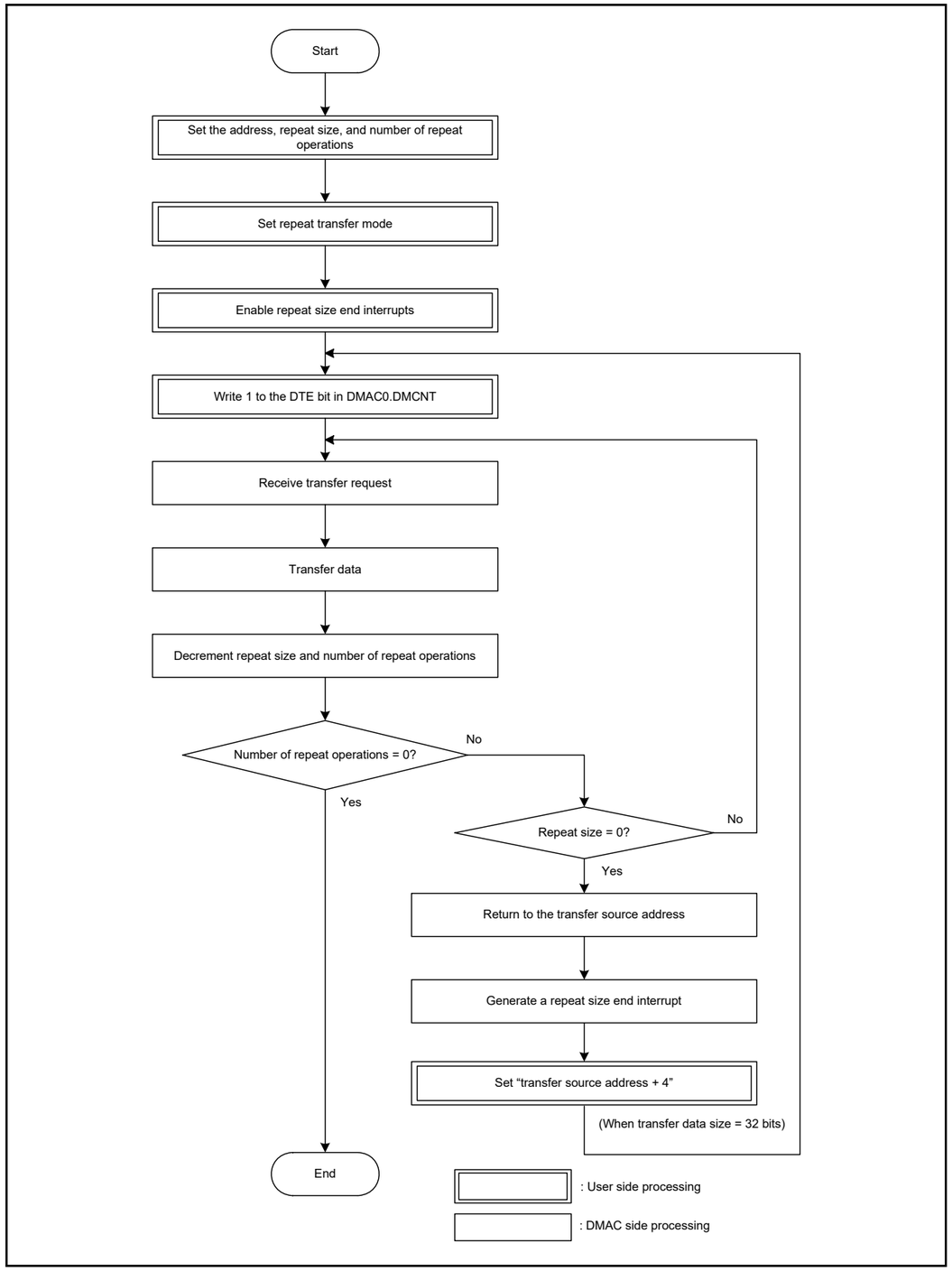


Figure 17.9 XY conversion flow using offset addition in repeat transfer mode

图17.9显示了XY转换的流程。

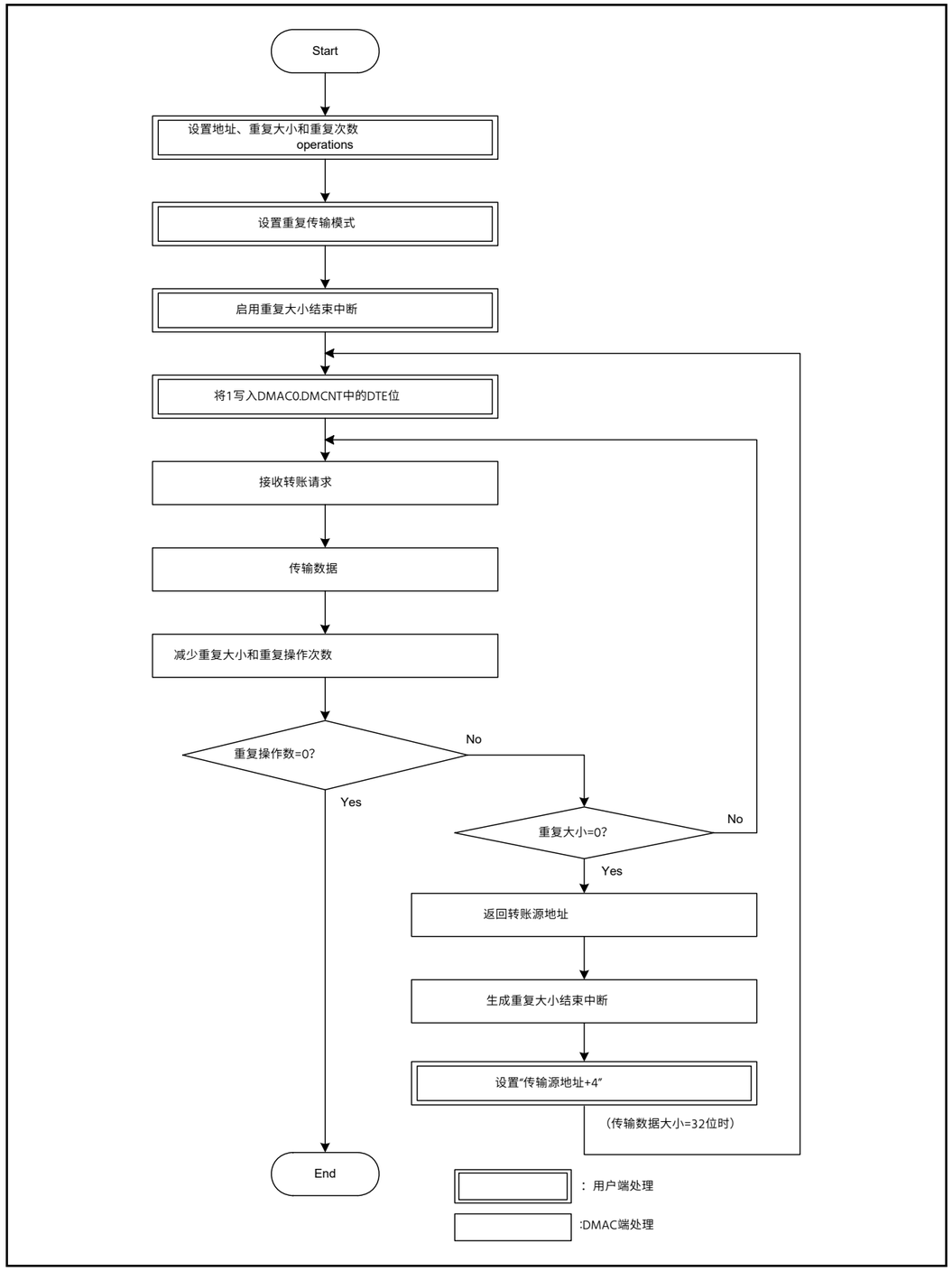


Figure 17.9 在重复传输模式中使用偏移添加的XY转换流程

17.3.4 Activation Sources

Software, the interrupt requests from the peripheral modules, and external interrupt requests can all be specified as DMAC activation sources. Set the DCTG[1:0] bits in DMACm.DMTMD to select the activation source.

(1) DMAC activation through software

To start DMA transfer through software:

1. Set the DCTG[1:0] bits in DMACm.DMTMD to 00b.
2. Set the DTE bit in DMACm.DMCNT to 1 (enable DMA transfer).
3. Set the DMST bit in DMAST to 1 (enable DMAC activation).
4. Set the SWREQ bit in DMACm.DMREQ to 1 (request DMA).

When the DMAC is activated by software while the CLRS bit in DMACm.DMREQ is 0, the SWREQ bit in DMACm.DMREQ is set to 0 after the data transfer starts in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, SWREQ does not clear to 0 after data transfer starts. A DMA transfer request is issued again after completion of a transfer.

(2) DMAC activation through interrupt requests from on-chip peripheral modules or external interrupt requests

You can specify interrupt requests from on-chip peripheral modules and external interrupt requests as DMAC activation sources. The activation source can be individually selected for each channel in ICU.DELSRn.DELS[7:0] (n = 0 to 3).

To start DMAC transfer through an interrupt request from an on-chip peripheral module or an external interrupt request:

1. Set the DCTG[1:0] bits in DMACm.DMTMD to 01b (select interrupts from the peripheral modules and the external interrupt pins).
2. Set the DTE bit in DMACm.DMCNT to 1 (enable DMA transfer).
3. Set ICU.DELSRn.DSEL to the event number (select the DMAC event link).
4. Set the DMST bit in DMAST to 1 (enable DMAC activation).

For interrupt requests specified as DMAC activation sources, see Table 14.3, Interrupt vector table in section 14, Interrupt Controller Unit (ICU).

17.3.5 Operation Timing

The following timing diagrams show the minimum number of execution cycles.

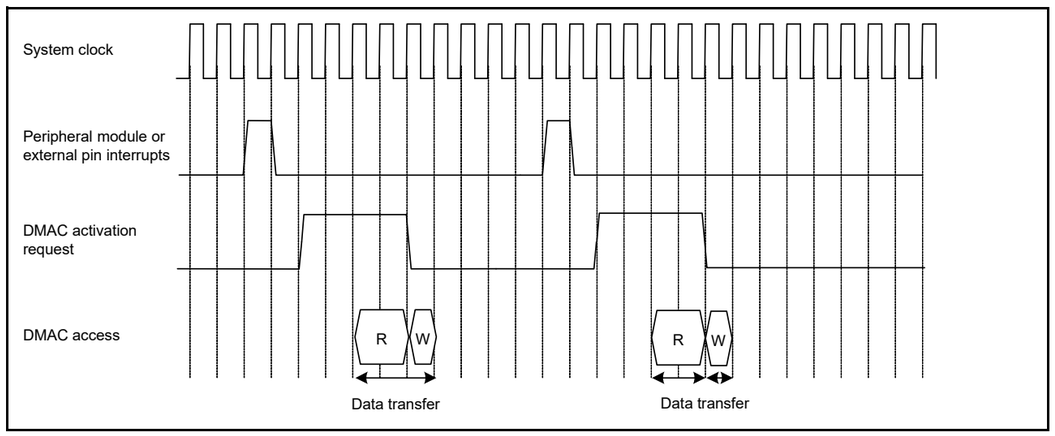


Figure 17.10 DMAC operation timing example 1 with DMA activation by interrupt from peripheral module/ external interrupt input pin, in normal transfer mode or repeat transfer mode

17.3.4 激活源

软件、外设模块的中断请求和外部中断请求都可以指定为DMAC激活源。设置DMACm.DMTMD中的DCTG[1:0]位以选择激活源。

(1) 通过软件激活DMAC

通过软件启动DMA传输：

1. 将DMACm.DMTMD中的DCTG[1:0]位设置为00b。
2. 将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）。
3. 将DMAST中的DMST位设置为1（启用DMAC激活）。
4. 将DMACm.DMREQ中的SWREQ位设置为1（请求DMA）。

当DMACm.DMREQ中的CLRS位为0时由软件激活DMAC，则DMACm.DMREQ中的SWREQ位在响应DMA传输请求而开始数据传输后，DMACm.DMREQ设置为0。

当CLRS位为1时由软件激活DMAC时，数据传输开始后SWREQ不会清为0。传输完成后再次发出DMA传输请求。

(2) 通过来自片上外围模块的中断请求或外部中断请求激活DMAC

您可以将来自片上外围模块的中断请求和外部中断请求指定为DMAC激活源。可以在ICU.DELSRn.DELS[7:0]（n=0到3）中为每个通道单独选择激活源。

通过来自片上外围模块的中断请求或外部中断请求启动DMAC传输：

1. 将DMACm.DMTMD中的DCTG[1:0]位设置为01b（从外围模块和外部中断引脚选择中断）。
2. 将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）。
3. 将ICU.DELSRn.DSEL设置为事件编号（选择DMAC事件链接）。
4. 将DMAST中的DMST位设置为1（启用DMAC激活）。

对于指定为DMAC激活源的中断请求，请参见表14.3，第14节中的中断向量表，中断控制器单元（ICU）。

17.3.5 操作时间

以下时序图显示了最小执行周期数。

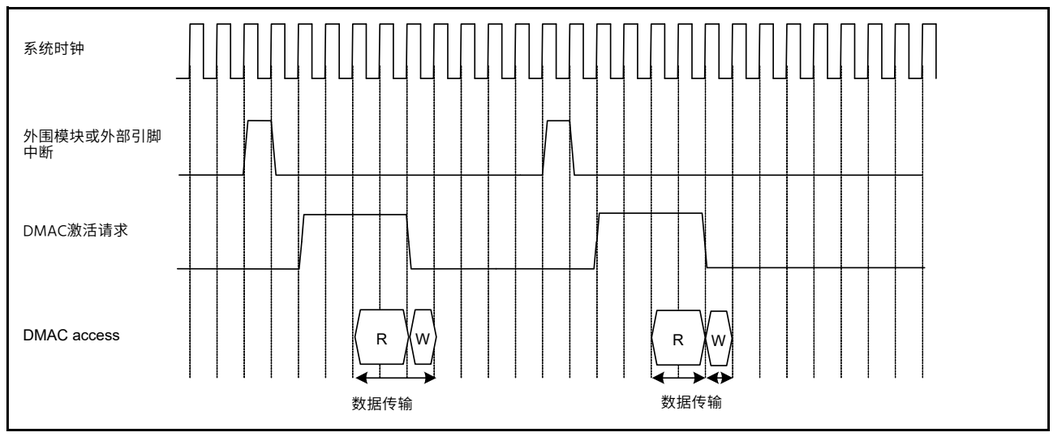


Figure 17.10 DMAC操作时序示例1通过来自外围模块外部中断输入引脚的中断激活DMA，处于正常传输模式或重复传输模式

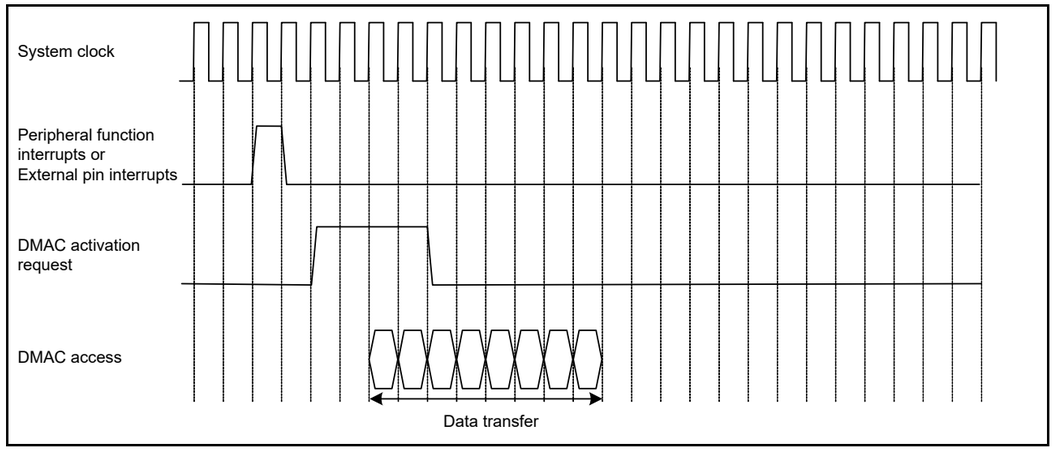


Figure 17.11 DMAC operation timing example 2 with DMA activation by interrupt from peripheral module/ external interrupt input pin, in block transfer mode with block size = 4

17.3.6 Execution Cycles of DMAC

Table 17.7 lists the execution cycles in one DMAC data transfer operation.

Table 17.7 DMAC execution cycles

Transfer mode	Data transfer (read)	Data transfer (write)
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P = Block size (DMCRAH register setting).
Cr = Read destination access cycle.
Cw = Data write destination access cycle.
Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle applies.

Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 42, SRAM, section 43, Flash Memory, and section 15, Buses. The frequency ratio of the system clock and the peripheral clock is also taken into consideration.

The unit for +1 in the data transfer (read) column is 1 system clock cycle, ICLK. For the operation example, see section 17.3.5, Operation Timing.

The DMAC response time is the time from when the DMAC activation source is detected until the DMAC transfer starts. Table 17.7 does not include the time until the DMAC data transfer starts after the DMAC activation source becomes active.

17.3.7 Activating DMAC

Figure 17.12 shows the register setting procedure.

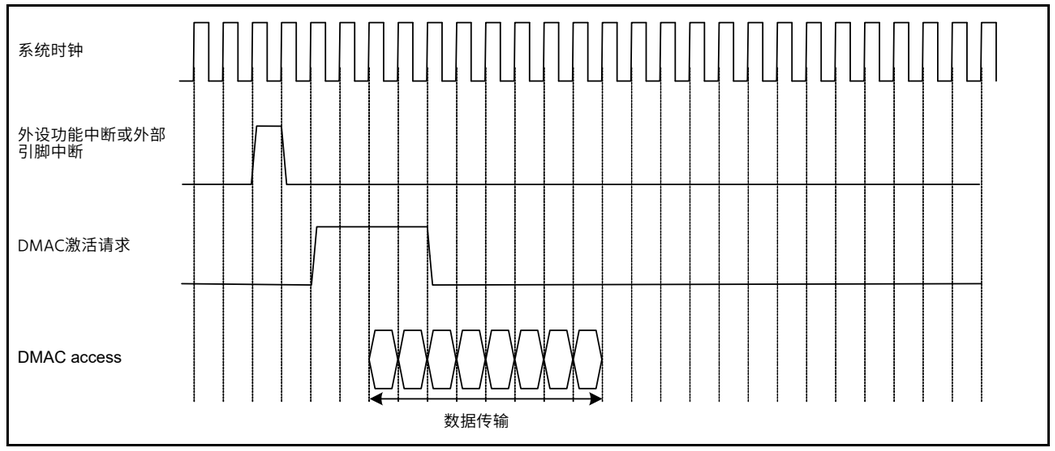


Figure 17.11 DMAC操作时序示例2，通过来自外围模块外部中断输入引脚的中断激活DMA，在块大小=4的块传输模式下

17.3.6 DMAC的执行周期

表17.7列出了一个DMAC数据传输操作中的执行周期。

Table 17.7 DMAC执行周期

传输模式	数据传输（读取）	数据传输（写入）
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P=块大小（DMCRAH寄存器设置）。Cr=
读取目标访问周期。
Cw=数据写入目标访问周期。
Note 1. 当块大小为2或更大时就是这种情况。当块大小为1时，应用正常传输周期。

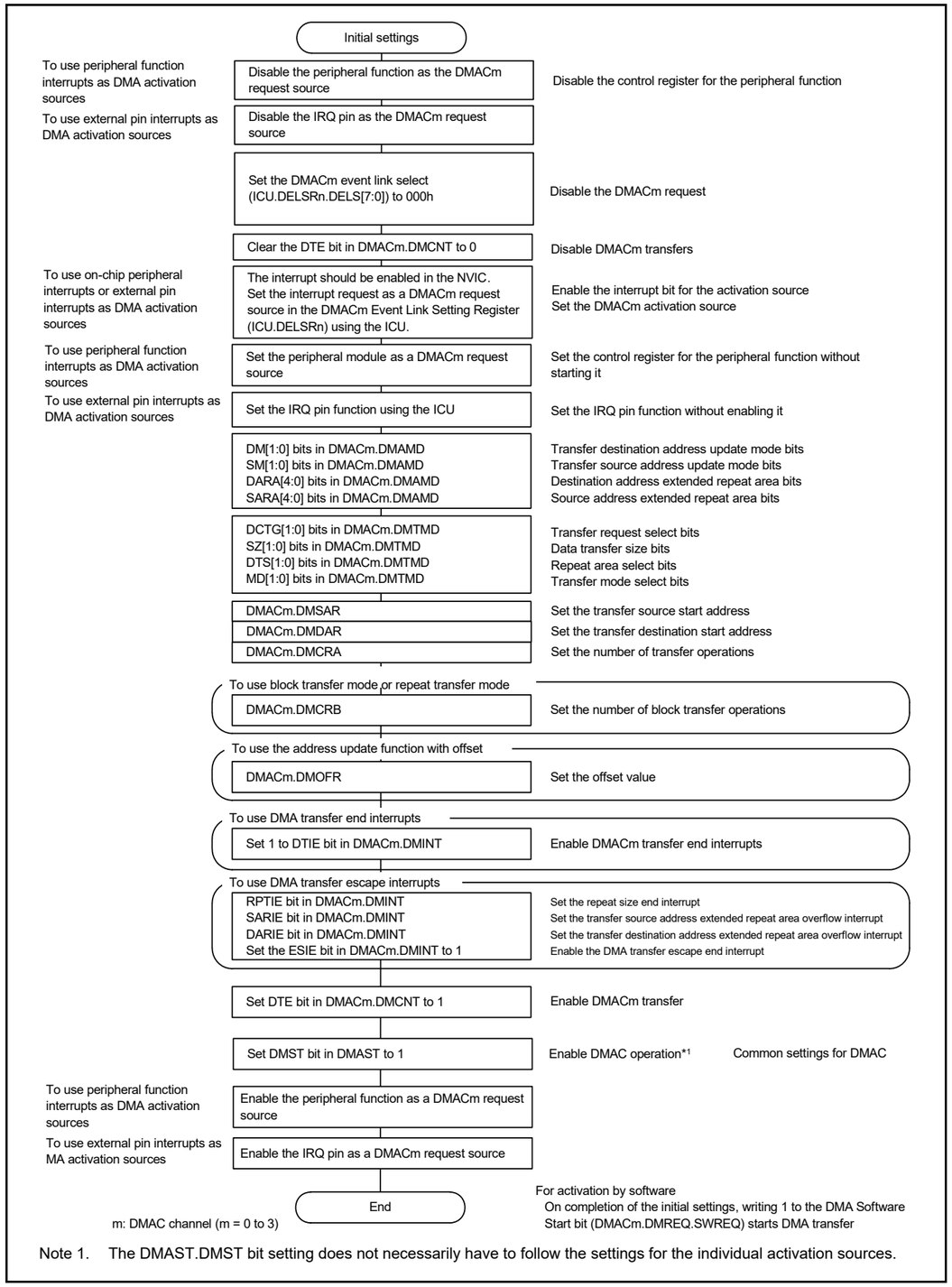
Cr和Cw取决于访问目的地。对于每个访问目的地的周期数，请参阅第42节，
SRAM，第43节，闪存和第15节，总线。系统时钟和外设时钟的频率比也被考虑在内。

数据传输（读取）列中+1的单位是1个系统时钟周期，ICLK。有关操作示例，请参阅第17.3.5节，操作时序。

DMAC响应时间是从检测到DMAC激活源到DMAC传输开始的时间。
表17.7不包括从DMAC激活源激活到DMAC数据传输开始的时间。

17.3.7 Activating DMAC

图17.12显示了寄存器设置过程。



Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

Figure 17.12 Register setting procedure

Note 1. DMAST.DMST位设置不一定必须遵循各个激活源的设置。

Figure 17.12 注册设置步骤

17.3.8 Starting DMA Transfer

To enable a DMA transfer of channel m, set the DTE bit in DMACm.DMCNT to 1 (DMA transfer enabled) and set the DMST bit in DMAST to 1 (DMAC start enabled). New activation requests are not accepted during the transfer of another DMAC channel or DTC. When the proceeding transfer is complete, channel arbitration selects the DMA transfer request of the highest priority channel, and DMA transfer of that channel starts. When DMA transfer starts, the ACT flag in DMACm.DMSTS is set to 1 (the DMAC is in the active state).

17.3.9 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated changes according to the other settings and the transfer state. The registers to be updated are DMSAR, DMDAR, DMCRA, DMCRB, DMCNT, and DMACm.DMSTS, described in the following sections. For details on register update operation in each transfer mode, see Table 17.3 to Table 17.5.

(1) DMA Source Address Register (DMACm.DMSAR)

After the data for one transfer request is transferred, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

(2) DMA Destination Address Register (DMACm.DMDAR)

After the data for one transfer request is transferred, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

(3) DMA Transfer Count Register (DMACm.DMCRA)

After the data for one transfer request is transferred, the count value is updated. The update operation depends on the transfer mode selected.

(4) DMA Block Transfer Count Register (DMACm.DMCRB)

After the data for one transfer request is transferred, the count value is updated. The update operation depends on the transfer mode selected.

(5) DMA Transfer Enable bit (DMACm.DMCNT.DTE)

The DMACm.DMCNT.DTE bit enables or disables data transfer through register write access. It is automatically set to 0 by the DMAC based on the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is complete
- When DMA transfer is stopped by a repeat size end interrupt
- When DMA transfer is stopped by an extended repeat area overflow interrupt.

Writing to the registers for channels whose associated DMACm.DMCNT.DTE bit is set to 1 is prohibited except for DMACm.DMCNT. Writes are only possible after the bit is set to 0.

(6) DMA Active Flag (DMACm.DMSTS.ACT)

The ACT flag in DMSTS of DMACm indicates whether the DMACm is in the idle or active state. This flag is set to 1 when the DMAC starts data transfer, and is set to 0 when data transfer for one transfer request is complete. Even when DMA transfer is stopped by write of 0 to the DTE bit in DMACm.DMCNT, this flag remains 1 until DMA transfer is complete.

(7) Transfer End Interrupt Flag (DMACm.DMSTS.DTIF)

The DTIF flag in DMACm.DMSTS is set to 1 after DMA transfer of the total transfer size is complete. When both this flag and the DTIE bit in DMACm.DMINT are 1, a transfer end interrupt is requested. This flag is set to 1 when the DMA transfer bus cycle is complete and the ACT flag in DMACm.DMSTS is set to 0, indicating the DMA transfer end. The flag is automatically set to 0 when the DTE bit in DMACm.DMCNT is set to 1 during interrupt handling.

(8) Transfer Escape End Interrupt Flag (DMACm.DMSTS.ESIF)

The ESIF flag in DMACm.DMSTS is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt

17.3.8 启动DMA传输

要启用通道m的DMA传输，请将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）并将DMAST中的DMST位设置为1（启用DMAC启动）。在传输另一个DMAC通道或DTC期间不接受新的激活请求。当正在进行的传输完成时，通道仲裁选择最高优先级通道的DMA传输请求，并开始该通道的DMA传输。当DMA传输开始时，DMACm.DMSTS中的ACT标志设置为1（DMAC处于活动状态）。

17.3.9 DMA传输期间的寄存器

DMAC寄存器由DMA传输更新。要更新的值根据其他设置和传输状态而变化。要更新的寄存器是DMSAR、DMDAR、DMCRA、DMRCB、DMCNT和DMACm.DMSTS，如下节所述。每种传输模式下寄存器更新操作的详细信息，请参见表17.3至表17.5。

(1) DMA源地址寄存器(DMACm.DMSAR)

一个传输请求的数据传输完成后，DMSAR的内容被更新为下一个传输请求访问的地址。

(2) DMA目标地址寄存器(DMACm.DMDAR)

一个传输请求的数据被传输后，DMDAR的内容被更新为下一个传输请求要访问的地址。

(3) DMA传输计数寄存器(DMACm.DMCRA)

在传输一个传输请求的数据后，更新计数值。更新操作取决于选择的传输模式。

(4) DMA块传输计数寄存器(DMACm.DMCRB)

在传输一个传输请求的数据后，更新计数值。更新操作取决于选择的传输模式。

(5) DMA传输使能位(DMACm.DMCNT.DTE)

DMACm.DMCNT.DTE位通过寄存器写访问启用或禁用数据传输。它由DMAC根据DMA传输状态自动设置为0。

DMAC清除该位的条件如下：

- 当指定的总数据传输量完成时
- 当DMA传输因重复大小结束中断而停止时
- 当DMA传输因扩展重复区域溢出中断而停止时。

禁止写入相关DMACm.DMCNT.DTE位设置为1的通道的寄存器，除非DMACm.DMCNT。只有在该位设置为0后才能写入。

(6) DMA活动标志(DMACm.DMSTS.ACT)

DMACm的DMSTS中的ACT标志指示DMACm是处于空闲状态还是活动状态。该标志在DMAC开始数据传输时设置为1，当一个传输请求的数据传输完成时设置为0。即使通过将0写入DMACm.DMCNT中的DTE位来停止DMA传输，该标志仍　　保持为1，直到DMA传输完成。

(7) 传输结束中断标志(DMACm.DMSTS.DTIF)

在完成总传输大小的DMA传输后，DMACm.DMSTS中的DTIF标志设置为1。当该标志和DMACm.DMINT中的DTIE位都为1时，请求传输结束中断。当DMA传输总线周期完成并且DMACm.DMSTS中的ACT标志设置为0时，该标志设置为1，表示DMA传输结束。当DMACm.DMCNT中的DTE位在中断处理期间设置为1时，该标志自动设置为0。

(8) 传输转义结束中断标志(DMACm.DMSTS.ESIF)

当重复大小结束中断或扩展重复区域溢出中断时，DMACm.DMSTS中的ESIF标志设置为1

is requested. When this bit and the ESIE bit in DMACm.DMINT are 1, a transfer escape end interrupt is requested. This flag is set to 1 when the bus cycle of the DMA transfer that caused the interrupt request is complete and the ACT flag in DMACm.DMSTS is set to 0, indicating the DMA transfer end. The flag is automatically set to 0 when the DTE bit in DMACm.DMCNT is set to 1 during interrupt handling.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 14, Interrupt Controller Unit (ICU).

17.3.10 Channel Priority

When multiple DMA transfer requests occur, the DMAC determines the priority of channels that have DMA transfer requests.

The priority is fixed as channel 0 > channel 1 > channel 2 > channel 3 (channel 0 is the highest).

When a DMA transfer request occurs during data transfer, channel arbitration starts after the final data unit is transferred, and DMA transfer of the highest-priority channel starts.

17.4 Ending DMA Transfer

The operation for ending a DMA transfer depends on the transfer end conditions. When a DMA transfer ends, the DTE bit in DMCNT and the ACT flag in DMACm.DMSTS change from 1 to 0.

17.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In normal transfer mode (DMACm.DMTMD.MD[1:0] = 00b)

When DMACm.DMCRAL changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT is set to 0, and the DTIF flag in DMACm.DMSTS is set to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, a transfer end interrupt request is sent to the CPU or the DTC.

(2) In repeat transfer mode (DMACm.DMTMD.MD[1:0] = 01b)

When DMACm.DMCRB changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT is set to 0, and the DTIF flag in DMACm.DMSTS is set to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

(3) In block transfer mode (DMACm.DMTMD.MD[1:0] = 10b)

When DMACm.DMCRB changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT is set to 0, and the DTIF flag in DMACm.DMSTS is set to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 14, Interrupt Controller Unit (ICU).

17.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, if the RPTIE bit in DMACm.DMINT is 1, a repeat size end interrupt is requested when transfer of a single repeat size of data is complete. The DTE bit in DMACm.DMCNT is set to 0 and the ESIF flag in DMACm.DMSTS is set to 1. If the ESIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC. To resume the transfer, write 1 to the DTE bit in DMACm.DMCNT.

A repeat size end interrupt can also be requested in block transfer mode. When transfer of a single block size of data is complete, the interrupt is requested in the same way as in repeat transfer mode.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 14, Interrupt Controller Unit (ICU).

17.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the SARIE or DARIE bit in DMACm.DMINT is 1, an extended repeat area overflow interrupt is requested. The DMA transfer is terminated, the DTE bit in DMACm.DMCNT is set to 0, and the ESIF flag in DMACm.DMSTS is set to 1. If the ESIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

被要求。当该位和DMACm.DMINT中的ESIE位为1时，请求传输转义结束中断。当导致中断请求的DMA传输的总线周期完成并且DMACm.DMSTS中的ACT标志设置为0时，该标志设置为1，表示DMA传输结束。当DTE位在

DMACm.DMCNT在中断处理期间设置为1。

在从DMAC向CPU或DTC发送中断请求之前，您必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.3.10 频道优先级

当出现多个DMA传输请求时，DMAC确定有DMA传输请求的通道的优先级。

优先级固定为通道0>通道1>通道2>通道3（通道0最高）。

当数据传输过程中出现DMA传输请求时，在传输完最后一个数据单元后开始通道仲裁，并开始最高优先级通道的DMA传输。

17.4 结束DMA传输

结束DMA传输的操作取决于传输结束条件。当DMA传输结束时，DMCNT中的DTE位和DMACm.DMSTS中的ACT标志从1变为0。

17.4.1 完成指定的转移操作总数后转移结束

(1) 在正常传输模式下（DMACm.DMTMD.MD[1:0]=00b）

当DMACm.DMCRAL从1变为0时，DMA传输在相关通道上结束，DTE位在DMACm.DMCNT置0，DMACm.DMSTS中的DTIF标志置1。如果此时DMACm.DMINT中的DTIE位为1，则向CPU或DTC发送传输结束中断请求。

(2) 在重复传输模式下（DMACm.DMTMD.MD[1:0]=01b）

当DMACm.DMCRB从1变为0时，DMA传输在相关通道上结束，DTE位在DMACm.DMCNT置0，DMACm.DMSTS中的DTIF标志置1。如果此时DMACm.DMINT中的DTIE位为1，则向CPU或DTC发送中断请求。

(3) 在块传输模式下（DMACm.DMTMD.MD[1:0]=10b）

当DMACm.DMCRB从1变为0时，DMA传输在相关通道上结束，DTE位在DMACm.DMCNT置0，DMACm.DMSTS中的DTIF标志置1。如果此时DMACm.DMINT中的DTIE位为1，则向CPU或DTC发送中断请求。

在从DMAC向CPU或DTC发送中断请求之前，您必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.4.2 按重复大小结束传输结束中断

在重复传输模式下，如果DMACm.DMINT中的RPTIE位为1，则在单个重复大小的数据传输完成时请求重复大小结束中断。DMACm.DMCNT中的DTE位设置为0，DMACm.DMSTS中的ESIF标志位设置为1。如果此时DMACm.DMINT中的ESIE位为1，则向CPU或DTC发送中断请求。要恢复传输，请将1写入DMACm.DMCNT中的DTE位。

在块传输模式下也可以请求重复大小结束中断。当单个块大小的数据传输完成时，以与重复传输模式相同的方式请求中断。

在从DMAC向CPU或DTC发送中断请求之前，您必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.4.3 扩展重复区溢出中断传输结束

如果在指定扩展重复区域且DMACm.DMINT中的SARIE或DARIE位为1时扩展重复区域发生溢出，则请求扩展重复区域溢出中断。DMA传输终止，DMACm.DMCNT中的DTE位设置为0，DMACm.DMSTS中的ESIF标志位设置为1。如果此时DMACm.DMINT中的ESIE位为1，则发送中断请求到CPU或DTC。

If this interrupt is requested during a read cycle, the subsequent write cycle is performed. In block transfer mode, if the interrupt is requested during a 1-block transfer, the remaining data in the block is transferred before transfer stops.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For more information, see section 14, Interrupt Controller Unit (ICU).

17.4.4 Precautions for the End of DMA Transfer

A DMA activation request source might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMA activation request is held in DMAC. To prevent this, stop the DMA activation requests by clearing the DELSRn.DELS[7:0] bits in the ICU to 0.

When a DMA activation request occurs after the last round of the DMA transfer is generated, clear the DMA activation request.

17.5 Interrupts

Each DMAC channel can output an interrupt request (DMACm_INT) to the CPU or DTC after transfer for one request is complete.

Table 17.8 lists the interrupt sources and their associated status flags and enable bits. Figure 17.13 shows the schematic logic diagram of the interrupt outputs (DMAC0 to DMAC3). Figure 17.14 shows the DMAC interrupt handling routine for resuming and terminating DMA transfers.

Table 17.8 Association between interrupt sources, interrupt status flags, and interrupt enable bits

Interrupt sources		Interrupt enable bits	Interrupt status flags	Request output enable bits
Transfer end		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
Escape transfer end	Repeat size end	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	Source address extended repeat area overflow	DMACm.DMINT.SARIE		
	Destination address extended repeat area overflow	DMACm.DMINT.DARIE		

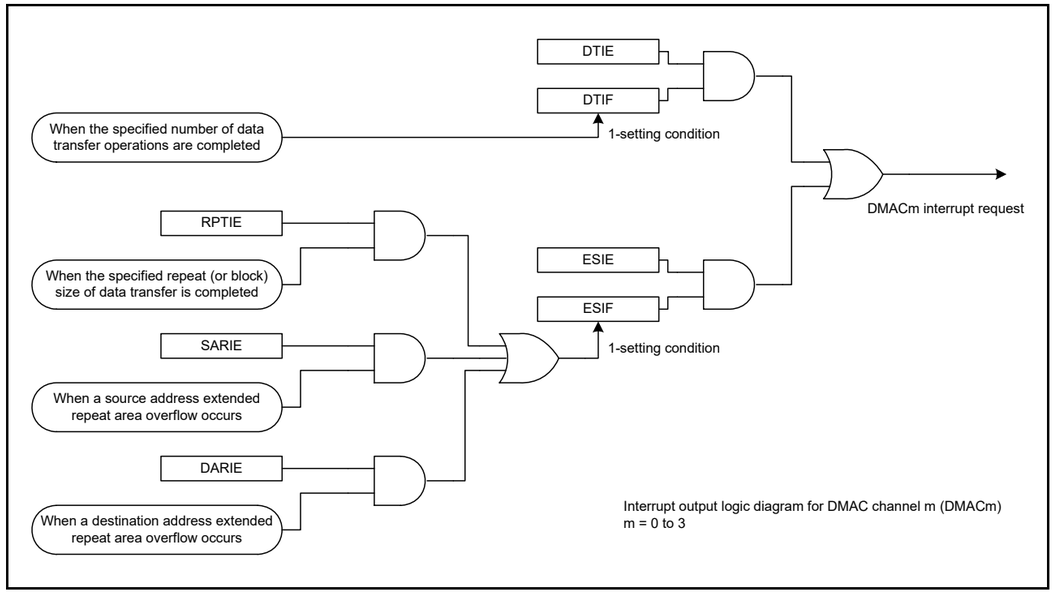


Figure 17.13 Schematic logic diagram of interrupt outputs for DMAC0 to DMAC3

如果在读周期内请求此中断，则执行后续写周期。在块传输模式下，如果在1块传输期间请求中断，则在传输停止之前传输块中剩余的数据。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.4.4 DMA传输结束的注意事项

DMA传输完成后的下一个请求中可能会出现DMA激活请求源。如果发生这种情况，
DMA传输开始，DMA激活请求保存在DMAC中。为防止这种情况，通过将ICU中的DELSRn.DELS[7:0]位清除为0来停止DMA激活请求。

当最后一轮DMA传输产生后出现DMA激活请求时，清除DMA激活请求。

17.5 Interrupts

每个DMAC通道可以在一个请求的传输完成后向CPU或DTC输出一个中断请求(DMACm_INT)。

表17.8列出了中断源及其相关的状态标志和使能位。图17.13显示了中断输出（DMAC0到DMAC3）的逻辑示意图。图17.14显示了用于恢复和终止DMA传输的DMAC中断处理程序。

Table 17.8 中断源、中断状态标志和中断使能位之间的关联

中断源		中断使能位	中断状态标志	请求输出使能位
转账结束		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
逃生转移结束	重复大小结束	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	源地址扩展重复区溢出	DMACm.DMINT.SARIE		
	目的地址扩展重复区溢出	DMACm.DMINT.DARIE		

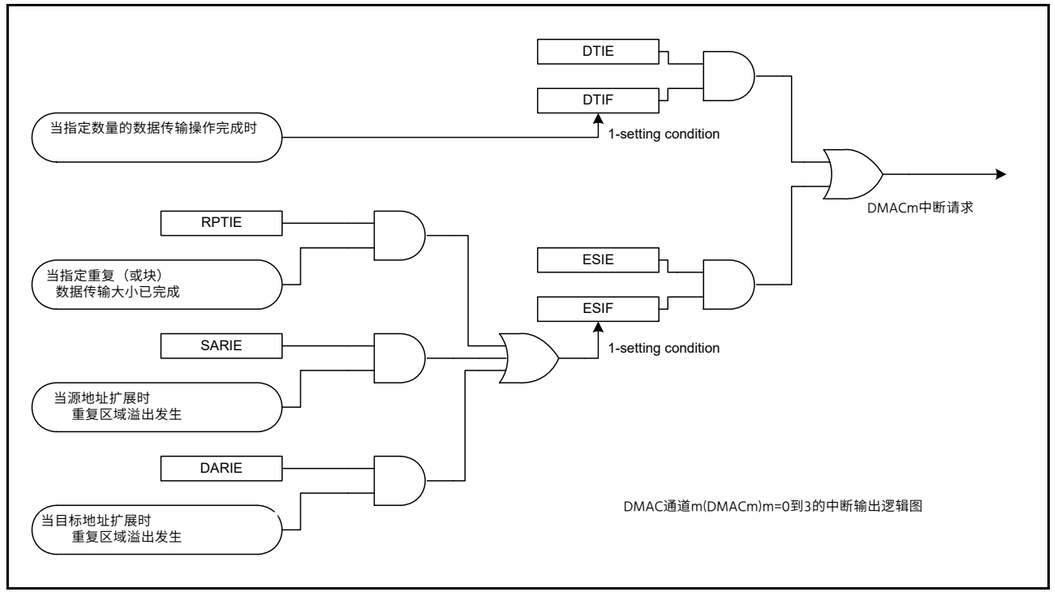


Figure 17.13 DMAC0到DMAC3的中断输出逻辑示意图

Different procedures are used for canceling an interrupt to restart a DMA transfer in the following cases:

- When terminating a DMA transfer
- When continuing a DMA transfer.

(1) When terminating a DMA transfer

Write 0 to the DTIF flag in DMACm.DMSTS to clear a transfer end interrupt, and to the ESIF flag in DMACm.DMSTS to clear a repeat size interrupt or an extended repeat area overflow interrupt. DMACm remains in the stopped state. When starting another DMA transfer, set the appropriate registers and set the DTE bit in DMACm.DMCNT to 1 (DMA transfer enabled).

(2) When continuing a DMA transfer

Write 1 to the DTE bit in DMACm.DMCNT. The ESIF flag in DMSTS of DMACm automatically is set to 0 (interrupt source cleared), and the DMA transfer resumes.

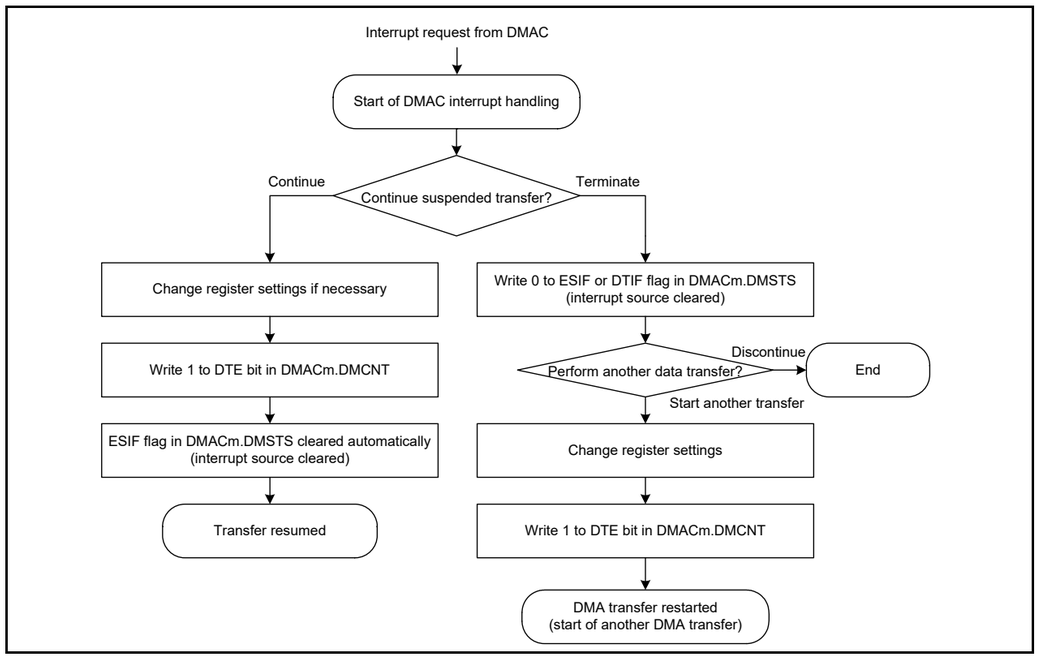


Figure 17.14 DMAC interrupt handling routine to resume or terminate a DMA transfer

17.6 Event Link

Each DMAC channel outputs an event link request signal (DMACm_INT) every time it completes a data transfer, or a block transfer in block transfer mode. For more information, see section 19, Event Link Controller (ELC).

17.7 Low Power Consumption Function

Before entering the module-stop state or Software Standby mode, you must first clear the DMST bit in DMAST to 0 (DMAC suspended), and use the settings in the sections that follow.

(1) Module-stop function

Writing 1 to the MSTPA22 bit in MSTPCRA enables the module-stop function of the DMAC. If a DMA transfer is in progress when 1 is written to the MSTPA22 bit, the transition to the module-stop state continues after DMA transfer ends. Access to the DMAC registers is prohibited while the MSTPA22 bit is 1. Writing 0 to the MSTPA22 bit releases the DMAC from the module-stop state.

在以下情况下，不同的程序用于取消中断以重新启动DMA传输：

- 终止DMA传输时
- 继续DMA传输时。

(1) 终止DMA传输时

将0写入DMACm.DMSTS中的DTIF标志以清除传输结束中断，并写入DMACm.DMSTS中的ESIF标志以清除重复大小中断或扩展重复区域溢出中断。DMACm保持在停止状态。当开始另一个DMA传输时，设置适当的寄存器并将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）。

(2) 继续DMA传输时

将1写入DMACm.DMCNT中的DTE位。DMACm的DMSTS中的ESIF标志自动设置为0（中断源清除），DMA传输恢复。

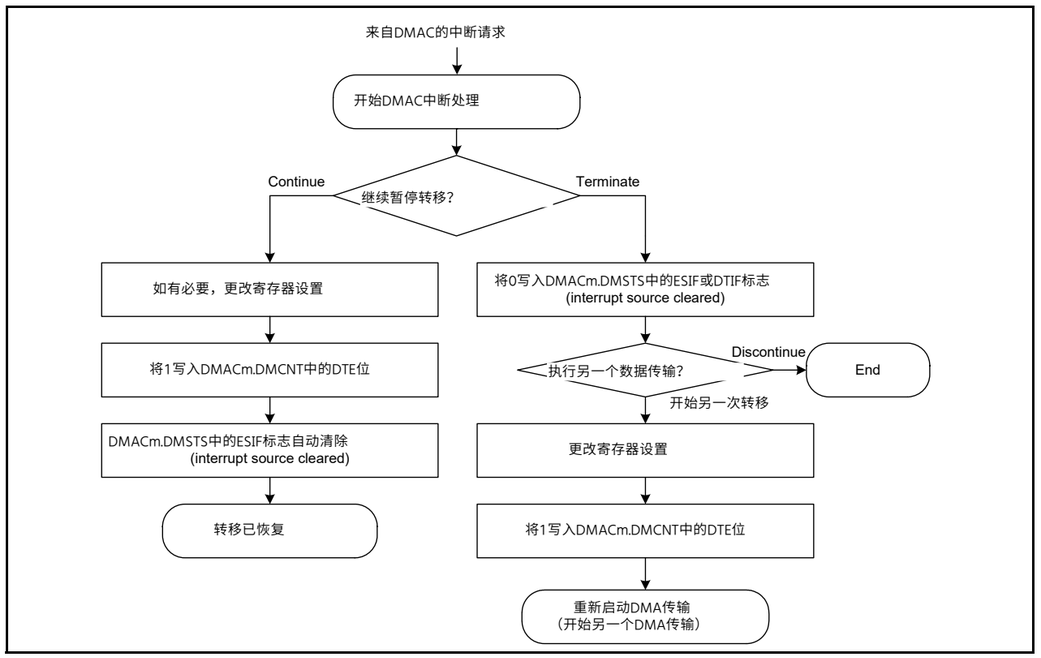


Figure 17.14 用于恢复或终止DMA传输的DMAC中断处理例程

17.6 活动链接

每个DMAC通道在每次完成数据传输或块传输模式下的块传输时都会输出一个事件链接请求信号(DMACm_INT)。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

17.7 低功耗功能

在进入模块停止状态或软件待机模式之前，必须先将DMAST中的DMST位清为0（DMAC挂起），并使用后面部分中的设置。

(1) Module-stop function

向MSTPCRA中的MSTPA22位写入1使能DMAC的模块停止功能。如果在向MSTPA22位写入1时正在进行DMA传输，则在DMA传输结束后继续转换到模块停止状态。当MSTPA22位为1时，禁止访问DMAC寄存器。将0写入MSTPA22位可将DMAC从模块停止状态释放。

(2) Software Standby mode

Use the settings described in section 11.7.1, Transition to Software Standby Mode.

If DMA transfer operations are in progress when the WFI instruction is executed, the DMA transfer completes before the transition to Software Standby mode.

(3) Notes on low power consumption function

For information on the WFI instruction and register settings, see section 11.9.6, Timing of WFI Instruction.

To perform DMA transfer after returning from low power consumption mode, set the DMST bit in DMAST to 1 again. To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination, as described in section 14.4.2, Selecting Interrupt Request Destinations, and then execute the WFI instruction.

17.8 Usage Notes

17.8.1 Access to Registers during DMA Transfer

Do not write to the following registers of DMACm while the ACT flag in DMSTS of the associated channel is set to 1 (DMAC active state) or the DTE bit in DMCNT of the associated channel is set to 1 (DMA transfer enabled):

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR.

17.8.2 DMA Transfer to Reserved Areas

DMA transfer to reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on reserved areas, see section 4, Address Space.

17.8.3 Setting the DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU.DELSRn)

Before setting the DMAC Event Link Setting Register (ICU.DELSRn), make sure the DMA Transfer Enable bit (DMACm.DMCNT.DTE) is set to 0, disabling DMA transfer. Additionally, ensure that the DTC Activation Enable bit (ICU.IELSRn.DTCE) associated with the event number set in the ICU.DELSRn register is not set to 1. For details on ICU.IELSRn.DTCE and ICU.DELSRn, see section 14, Interrupt Controller Unit (ICU).

17.8.4 Suspending or Restarting DMA Activation

To suspend a DMA activation request, write 0 to the DMAC Event Link Select (ICU.DELSRn.DELS[7:0]) bit. To restart the DMA transfer, write the event number to the ICU.DELSRn.DELS[7:0] bit with the settings shown in section 17.3.7, Activating DMAC.

(2) 软件待机模式

使用第11.7.1节，转换到软件待机模式中描述的设置。

如果在执行WFI指令时DMA传输操作正在进行，则DMA传输在转换到软件待机模式之前完成。

(3) 低功耗功能注意事项

有关WFI指令和寄存器设置的信息，请参阅第11.9.6节，WFI指令的时序。

要在从低功耗模式返回后执行DMA传输，请将DMAST中的DMST位再次设置为1。要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DMAC启动请求，请将CPU指定为中断请求目标，如第14.4.2节，选择中断请求目标中所述，然后执行WFI指令。

17.8 使用说明

17.8.1 在DMA传输期间访问寄存器

当相关通道的DMSTS中的ACT标志设置为1（DMAC活动状态）或相关通道的DMCNT中的DTE位设置为1（启用DMA传输）时，请勿写入DMACm的以下寄存器：

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR.

17.8.2 DMA传输到保留区域

禁止对保留区域进行DMA传输。如果进行此类访问，则无法保证传输结果。有关保留区域的详细信息，请参阅第4节，地址空间。

17.8.3 设置中断控制器单元(ICU.DELSRn)的DMAC事件链接设置寄存器

在设置DMAC事件链接设置寄存器(ICU.DELSRn)之前，请确保DMA传输启用位(DMACm.DMCNT.DTE)设置为0，禁用DMA传输。此外，确保与ICU.DELSRn寄存器中设置的事件编号相关的DTC激活启用位(ICU.IELSRn.DTCE)未设置为1。有关ICU.IELSRn.DTCE和ICU.DELSRn的详细信息，请参阅第14节，中断控制器单元（ICU）。

17.8.4 暂停或重新启动DMA激活

要暂停DMA激活请求，请将0写入DMAC事件链接选择(ICU.DELSRn.DELS[7:0])位。要重新启动DMA传输，请将事件编号写入ICU.DELSRn.DELS[7:0]位，设置如第17.3.7节，激活DMAC中所示。

18. Data Transfer Controller (DTC)

18.1 Overview

The MCU includes a Data Transfer Controller (DTC) that performs data transfers when activated by an interrupt request. Table 18.1 lists the DTC specifications and Figure 18.1 shows a block diagram.

Table 18.1 DTC specifications

Parameter	Description
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes). • Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) • Multiple data units can be transferred on a single activation source (chain transfer) • Chain transfers are selectable to either execute when the counter is 0, or always execute.
Transfer space	• 4 GB area from 0000 0000h to FFFF FFFFh, not including reserved areas
Data transfer units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) • Single block size: 1 to 256 data units
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt • An interrupt request can be generated to the CPU after a single data transfer • An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
Module-stop function	Module-stop state can be set to reduce power consumption

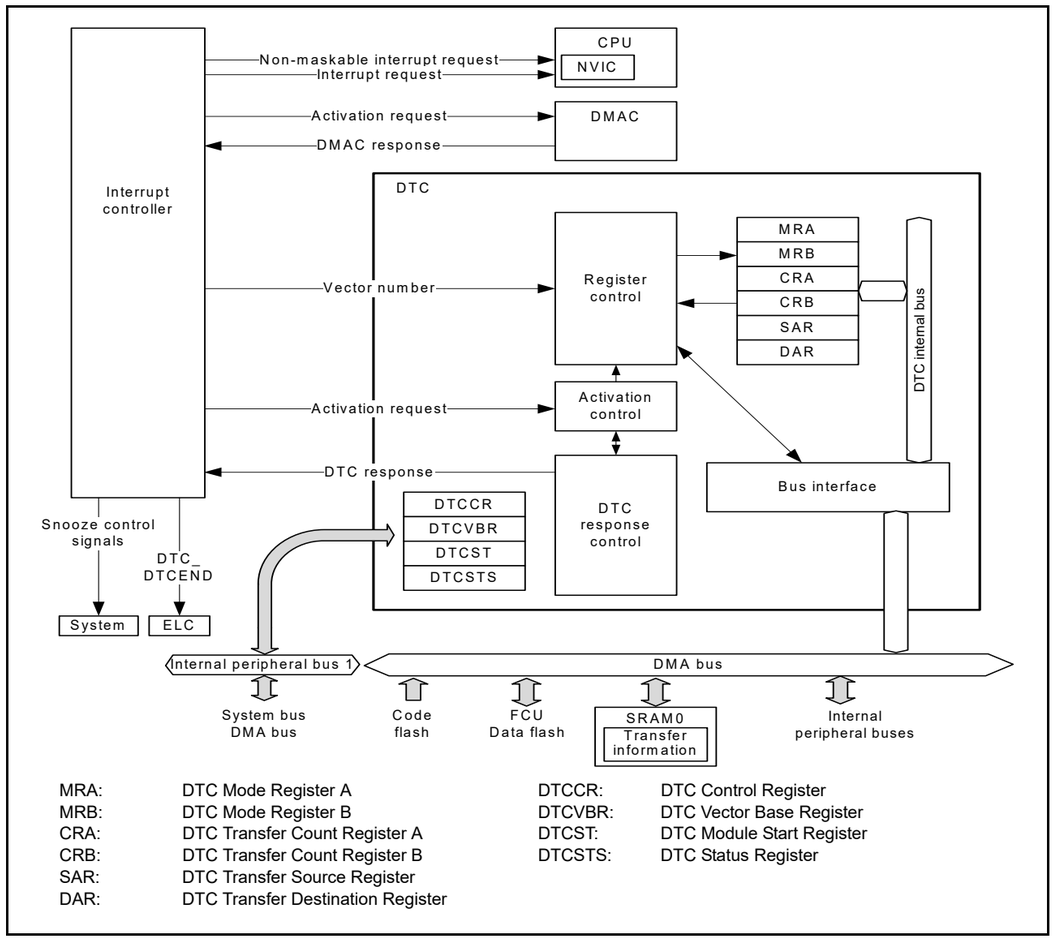
18. 数据传输控制器(DTC)

18.1 Overview

MCU包括一个数据传输控制器(DTC)，它在被中断请求激活时执行数据传输。
表18.1列出了DTC规范，图18.1显示了框图。

Table 18.1 DTC specifications

Parameter	Description
传输模式	正常传输模式 单次激活导致单次数据传输。 重复传输模式 单次激活导致单次数据传输。 数据传输次数达到指定的重复大小后，传输地址返回起始地址。最大重复传输次数为256，最大数据传输大小为256×32位（1024字节）。 块传输模式 单个激活导致单个块的传输。最大块大小为256×32位=1024字节。
传输通道	通道传输可以与中断源相关联（通过来自ICU的DTC激活请求传输） 多个数据单元可以在单个激活源上传输（链传输） 可以选择在计数器为0时执行链传输，或始终执行。
转移空间	4GB区域，从00000000h到FFFFFFFFh，不包括保留区域
数据传输单元	单个数据单元：1个字节（8位）、1个半字（16位）、1个字（32位） 单个块大小：1到256个数据单元
CPU中断源	可以在DTC激活中断时向CPU生成中断请求 可以在单次数据传输后向CPU生成中断请求 可以在指定量的数据传输后向CPU生成中断请求。
事件链接功能	一次数据传输后产生事件链接请求（对于块，在一次块传输后）
阅读跳过	可以跳过读取传输信息
Write-back skip	当传输源或目标地址指定为固定时，可以跳过传输信息的回写
Module-stop function	可设置模块停止状态以降低功耗



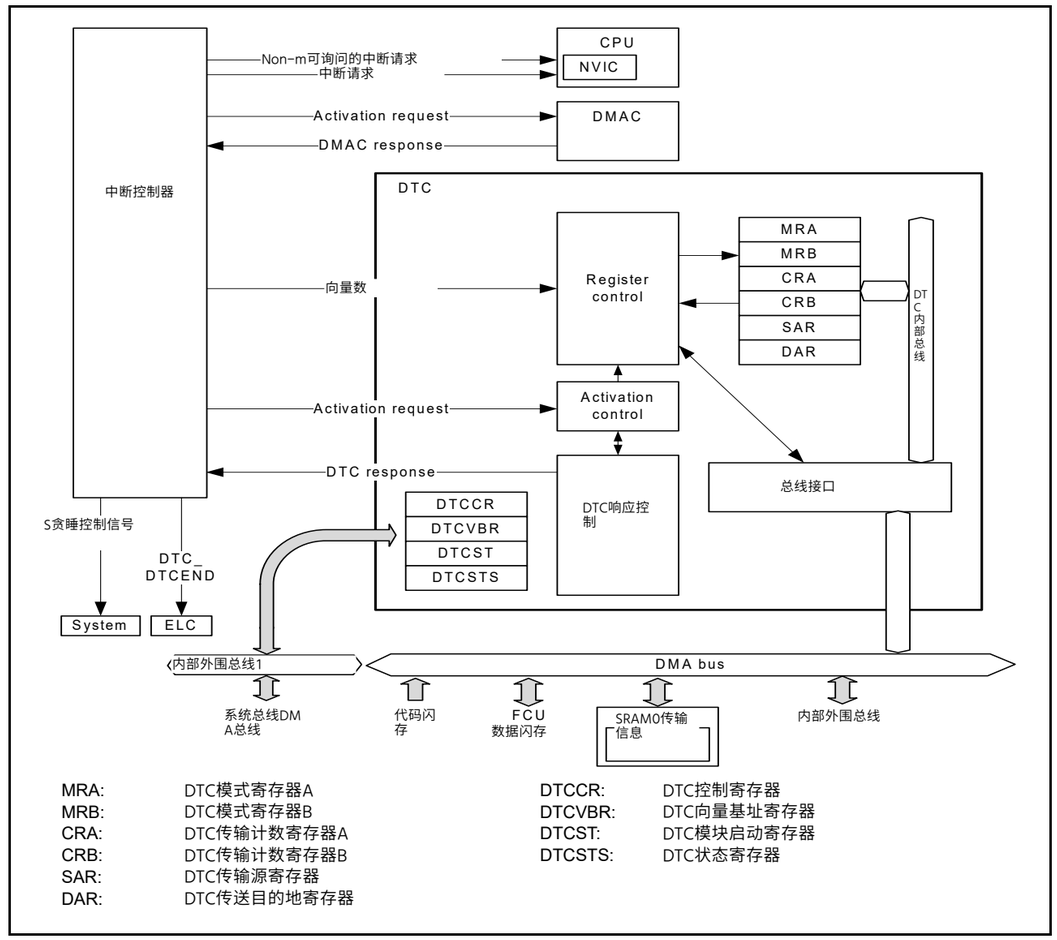
MRA:	DTC Mode Register A	DTCCR:	DTC Control Register
MRB:	DTC Mode Register B	DTCVBR:	DTC Vector Base Register
CRA:	DTC Transfer Count Register A	DTCST:	DTC Module Start Register
CRB:	DTC Transfer Count Register B	DTCSTS:	DTC Status Register
SAR:	DTC Transfer Source Register		
DAR:	DTC Transfer Destination Register		

Figure 18.1 DTC block diagram

See section 14.1, Overview in section 14, Interrupt Controller Unit (ICU) for the connections between the DTC and NVIC in the CPU.

18.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.



MRA:	DTC模式寄存器A	DTCCR:	DTC控制寄存器
MRB:	DTC模式寄存器B	DTCVBR:	DTC向量基址寄存器
CRA:	DTC传输计数寄存器A	DTCST:	DTC模块启动寄存器
CRB:	DTC传输计数寄存器B	DTCSTS:	DTC状态寄存器
SAR:	DTC传输源寄存器		
DAR:	DTC传送目的地寄存器		

Figure 18.1 故障诊断代码框图

有关DTC和
CPU中的NVIC。

18.2 注册说明

MRA、MRB、SAR、DAR、CRA、CRB都是DTC内部寄存器，不能直接从CPU访问。在这些DTC内部寄存器中设置的值作为传输信息放置在SRAM区域中。当产生激活请求时，DTC从SRAM区域读取传输信息并将其设置在其内部寄存器中。数据传输结束后，内部寄存器内容作为传输信息回写到SRAM区域。

18.2.1 DTC Mode Register A (MRA)

Address(es): (inaccessible directly from the CPU. See section 18.3.1)

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: Address in the SAR register is fixed (write-back to SAR is skipped.) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped.) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] bits = 00b +2 when SZ[1:0] bits = 01b +4 when SZ[1:0] bits = 10b. 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] bits = 00b -2 when SZ[1:0] bits = 01b -4 when SZ[1:0] bits = 10b.	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited.	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited.	—

The MRA cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 03h) and the DTC automatically transfers the MRA transfer information to and from the MRA register. See section 18.3.1, Allocating Transfer Information and DTC Vector Table.

18.2.2 DTC Mode Register B (MRB)

Address(es): (inaccessible directly from the CPU. See section 18.3.1)

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—

18.2.1 DTC模式寄存器A(MRA)

地址：（无法直接从CPU访问。参见第18.3.1节）

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为未定义。写入值应为0。	—
b3, b2	SM[1:0]	传输源地址寻址 Mode	b3b200：SAR寄存器中的地址固定（跳过对SAR的回写。）01：SAR寄存器中的地址固定（跳过对SAR的回写。）10：SAR值在之后递增数据传输：当SZ[1:0]位=00b时+1当SZ[1:0]位=01b时+2当SZ[1:0]位=10b时+4。11：SAR值在数据传输后递减：−1当SZ[1:0]位=00b时−2当SZ[1:0]位=01b时−4当SZ[1:0]位=10b时。	—
b5, b4	SZ[1:0]	DTC数据传输大小	b5b400：字节（8位）传送01：半字（16位）传送10：字（32位）传送11：禁止设置。	—
b7, b6	MD[1:0]	DTC传输模式选择	b7b600：正常传输模式01：重复传输模式10：块传输模式11：禁止设置。	—

MRA不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+03h），并且DTC会自动将MRA传输信息传输到MRA寄存器或从MRA寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

18.2.2 DTC模式寄存器B(MRB)

地址：（无法直接从CPU访问。参见第18.3.1节）

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为未定义。写入值应为0。	—

Bit	Symbol	Bit name	Description	R/W
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] bits = 00b +2 when SZ[1:0] bits = 01b +4 when SZ[1:0] bits = 10b. 1 1: DAR value is decremented after data transfer: –1 when MRA.SZ[1:0] bits = 00b –2 when SZ[1:0] bits = 01b –4 when SZ[1:0] bits = 10b.	—
b4	DTS	DTC Transfer Mode Select	0: Select transfer destination as repeat or block area 1: Select transfer source as repeat or block area.	—
b5	DISEL	DTC Interrupt Select	0: Generate an interrupt request to the CPU when specified data transfer is complete 1: Generate an interrupt request to the CPU each time DTC data transfer is performed.	—
b6	CHNS	DTC Chain Transfer Select	0: Select continuous chain transfer 1: Select chain transfer to occur only when the transfer counter is changed from 1 to 0 or 1 to CRAH.	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer disabled 1: Chain transfer enabled.	—

The MRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 02h) and the DTC automatically transfers the MRB transfer information to and from the MRB register. See section 18.3.1, Allocating Transfer Information and DTC Vector Table.

DTS bit (DTC Transfer Mode Select)

The DTS bit selects either the transfer source or transfer destination as the repeat area or block area in repeat or block transfer mode.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When the CHNE bit is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 18.3, Chain transfer conditions.

When the next transfer is a chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected in the CHNS bit. For details, see section 18.4.6, Chain Transfer.

18.2.3 DTC Transfer Source Register (SAR)

Address(es): (inaccessible directly from the CPU. See section 18.3.1)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The SAR sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU can

Bit	Symbol	位名称	Description	R/W
b3, b2	DM[1:0]	转移目的地地址寻址方式	b3b200：DAR寄存器中的地址固定（跳过回写DAR）01：固定DAR寄存器中的地址（跳过回写DAR）10：数据传输后DAR值递增：当MRA.SZ[1:0]位=00b时+1当SZ[1:0]位=01b时+2当SZ[1:0]位=10b时+4。11：数据传输后DAR值递减： 1当MRA.SZ[1:0]位=00b 2当SZ[1:0]位=01b 4当SZ[1:0]位=10b。	—
b4	DTS	DTC传输模式选择	0：选择传输目标为重复或块区域1：选择传输源为重复或块区域。	—
b5	DISEL	DTC中断选择	0：指定数据传输完成时向CPU产生中断请求1：每次执行DTC数据传输时，向CPU产生中断请求。	—
b6	CHNS	DTC链转移选择	0：选择连续链转移1：选择链转移仅在转移计数器从1变为0或从1变为CRAH时发生。	—
b7	CHNE	DTC链转移启用	0：禁止链转移1：允许链转移。	—

MRB寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+02h），并且DTC自动将MRB传输信息传输到MRB寄存器或从MRB寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

DTS位（DTC传输模式选择）

在重复或块传输模式下，DTS位选择传输源或传输目标作为重复区域或块区域。

CHNS位（DTC链传输选择）

CHNS位选择链传输条件。当CHNE位为0时，忽略CHNS设置。有关链转移条件的详细信息，请参见表18.3，链转移条件。

当下一次传输是链式传输时，指定传输次数的完成未确定，激活源标志未清零，也不向CPU产生中断请求。

CHNE位（DTC链传输使能）

CHNE位启用链式传输。在CHNS位中选择链传输条件。有关详细信息，请参阅第18.4.6节，链转移。

18.2.3 DTC传输源寄存器(SAR)

地址：（无法直接从CPU访问。参见第18.3.1节）

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

SAR设置传输源起始地址，不能直接从CPU访问。但是，CPU可以

access the SRAM area (transfer information (n) start address + 04h) and the DTC automatically transfers the transfer information to and from the SAR register. See section 18.3.1, Allocating Transfer Information and DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers.
Bit [0] must be 0 when MRA.SZ[1:0] = 01b. Bits [1] and [0] must be 0 when MRA.SZ[1:0] = 10b.

18.2.4 DTC Transfer Destination Register (DAR)

Address(es): (inaccessible directly from the CPU. See section 18.3.1)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The DAR register sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 08h) and the DTC automatically transfers the transfer information to and from the DAR register. See section 18.3.1, Allocating Transfer Information and DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers. Bit [0] must be 0 when MRA.SZ[1:0] = 01b. Bits [1] and [0] must be 0 when MRA.SZ[1:0] = 10b.

18.2.5 DTC Transfer Count Register A (CRA)

Address(es): (inaccessible directly from the CPU. See section 18.3.1)

- Normal transfer mode

	CRA															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

- Repeat transfer mode/block transfer mode

	CRAH								CRAL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Symbol	Register name	Description	R/W
CRAL	Transfer Counter A Lower Register	Set the transfer count	—
CRAH	Transfer Counter A Upper Register		—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0Eh) and the DTC automatically transfers the transfer information to and from the CRA

访问SRAM区域（传输信息(n)起始地址+04h），DTC会自动将传输信息传入和传出SAR寄存器。请参阅第18.3.1节，分配传输信息和DTC向量表。

Note: DTC传输禁止错位。
当MRA.SZ[1:0]=01b时，位[0]必须为0。当MRA.SZ[1:0]=10b时，位[1]和[0]必须为0。

18.2.4 DTC传输目的地寄存器(DAR)

地址：（无法直接从CPU访问。参见第18.3.1节）

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

DAR寄存器设置传输目标起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+08h），并且DTC会自动将传输信息传输到DAR寄存器或从DAR寄存器传输传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

Note: DTC传输禁止错位。当MRA.SZ[1:0]=01b时，位[0]必须为0。当MRA.SZ[1:0]=10b时，位[1]和[0]必须为0。

18.2.5 DTC传输计数寄存器A(CRA)

地址：（无法直接从CPU访问。参见第18.3.1节）

正常传输模式

	CRA															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

重复传输模式块传输模式

	CRAH								CRAL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Symbol	注册名称	Description	R/W
CRAL	传送计数器A低位寄存器	设置传输计数	—
CRAH	传送计数器A高位寄存器		—

Note: 该功能取决于传输模式。
Note: 在重复传输模式和块传输模式下，将CRAH和CRAL设置为相同的值。

CRA寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0Eh）并且DTC自动将传输信息传输到CRA和从CRA传输信息

register. See section 18.3.1, Allocating Transfer Information and DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] bits = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65,535, and 65,536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] bits = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (–1) on each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] bits = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (–1) on each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

18.2.6 DTC Transfer Count Register B (CRB)

Address(es): (inaccessible directly from the CPU. See section 18.3.1)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The CRB register sets the block transfer count for block transfer mode. The transfer count is 1, 65,535, and 65,536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRB value is decremented (–1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

The CRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0Ch) and the DTC automatically transfers the transfer information to and from the CRB register. See section 18.3.1, Allocating Transfer Information and DTC Vector Table.

18.2.7 DTC Control Register (DTCCR)

Address(es): DTC.DTCCR 4000 5400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Information Read Skip Enable	0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

登记。请参阅第18.3.1节，分配传输信息和DTC向量表。

(1) 正常传输模式（MRA.MD[1:0]位=00b）

在正常传输模式下，CRA用作16位传输计数器。当设置值为0001h、FFFFh和0000h时，传输计数分别为1、65 535和65 536。CRA值在每次数据传输时递减(–1)。

(2) 重复传输模式（MRA.MD[1:0]位=01b）

在重复传输模式下，CRAH寄存器保存传输计数，CRAL寄存器用作8位传输计数器。当设置值为01h、FFh和00h时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(1)。当它达到00h时，CRAH值被传送到CRAL。

(3) 块传输模式（MRA.MD[1:0]位=10b）

在块传输模式下，CRAH寄存器保存块大小，CRAL寄存器用作8位块大小计数器。当设置值为01h、FFh和00h时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(1)。当它达到00h时，CRAH值被传送到CRAL。

18.2.6 DTC传输计数寄存器B(CRB)

地址：（无法直接从CPU访问。参见第18.3.1节）

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

CRB寄存器设置块传输模式的块传输计数。当设置值为0001h、FFFFh和0000h时，传输计数分别为1、65 535和65 536。当传输单个块大小的最终数据时，CRB值递减(1)。Whennormaltransfermodeorrepeattransfermodeisselected thisregisterisnotusedandthesetvalueisignored.

CRB寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0Ch），并且DTC自动将传输信息传输到CRB寄存器和从CRB寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

18.2.7 DTC控制寄存器(DTCCR)

Address(es): DTC.DTCCR 4000 5400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	—	Reserved	该位读取为1。写入值应为1。	R/W
b4	RRS	DTC传输信息 读取跳过启用	0：不跳过传输信息读取1：当向量编号匹配时，跳过传输信息读取。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RRS位（DTC传输信息读取跳过使能）

当向量编号匹配时，RRS位允许跳过传输信息读取。将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量编号匹配并且RRS位设置为1时，执行DTC数据传输而不读取传输信息。但是，当前一次传输是链式传输时，无论RRS位如何，都会读取传输信息。

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

18.2.8 DTC Vector Base Register (DTCVBR)

Address(es): DTC.DTCVBR 4000 5404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit name	Description	R/W
b31 to b0	DTC Vector Base Address	Set the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR register sets the base address for calculating the DTC vector table address, which can be set in the range of 0000 0000h to FFFF FFFFh (4 GB) in 1-KB units.

18.2.9 DTC Module Start Register (DTCST)

Address(es): DTC.DTCST 4000 540Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module stopped 1: DTC module started.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When the DTCST bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until processing is complete.

DTCST must be set to 0 before transitioning to one of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition.

For details on these transitions, see section 18.10, Module-Stop Function, and section 11, Low Power Modes.

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位的值如何，都将读取传输信息。

18.2.8 DTC向量基址寄存器(DTCVBR)

Address(es): DTC.DTCVBR 4000 5404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	位名称	Description	R/W
b31 to b0	DTC向量基地址	设置DTC向量基地址。低10位应为0。	R/W

DTCVBR寄存器设置计算DTC向量表地址的基地址，可以设置在00000000h到FFFFFFFFh(4GB)的范围内，以1KB为单位。

18.2.9 DTC模块启动寄存器(DTCST)

Address(es): DTC.DTCST 4000 540Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DTCST	DTC模块启动	0：DTC模块停止1：DTC模块启动。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DTCST位（DTC模块启动）

将DTCST位设置为1以使DTC接受传输请求。当DTCST位设置为0时，不再接受传输请求。如果在数据传输期间该位设置为0，则接受的传输请求将处于活动状态，直到处理完成。

在转换到以下状态或模式之一之前，必须将DTCST设置为0：

- Module-stop state
- 没有贪睡模式转换的软件待机模式。

有关这些转换的详细信息，请参阅第18.10节，模块停止功能和第11节，低功耗模式。

18.2.10 DTC Status Register (DTCSTS)

Address(es): DTC.DTCSTS 4000 540Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector Number Monitoring	These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0.	R
b15	ACT	DTC Active Flag	0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress.	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the ACT flag is 1, indicating a DTC transfer is in progress, and invalid if the ACT flag is 0, indicating no current DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

18.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 31. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number n is selected by ICU.IELSRn.IELS[7:0], where n = 0 to 31, as listed in Table 14.4, Event table in section 14, Interrupt Controller Unit (ICU). For activation by software, see section 19.2.2, Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepted an activation request, it does not accept another activation request until transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DMAC or DTC transfer, a highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC Module Start bit (DTCST.DTCST) is 0, the DTC accepts the highest priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0 and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR bit of the activation source is set to 0 at the start of the data transfer.

18.2.10 DTC状态寄存器(DTCSTS)

Address(es): DTC.DTCSTS 4000 540Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector 号码监控	当DTC传输正在进行时，这些位指示激活源的向量编号。该值仅在DTC传输正在进行（ACT标志为1）时有效。	R
b14 to b8	—	Reserved	这些位读为0。	R
b15	ACT	DTC活动标志	0：未进行DTC传输操作1：正在进行DTC传输操作。	R

VECN[7:0]位（DTC–激活向量编号监控）

当DTC进行传输时，VECN[7:0]位指示与传输激活源相关的向量编号。如果ACT标志为1，则从VECN[7:0]位读取的值有效，表示正在进行DTC传输；如果ACT标志为0，则表示当前没有正在进行DTC传输，则该值无效。

ACT标志（DTC活动标志）

ACT标志指示DTC传输操作的状态。

[Setting condition]

- 当DTC被传输请求激活时。

[Clearing condition]

- 当DTC响应传输请求传输完成时。

18.3 激活源

DTC由中断请求激活。将ICU.IELSRn.DTCE位设置为1可以通过相关中断激活DTC。ICU.IELSRn中设置的选择器输出n个数被定义为中断向量号，其中n=0到31。对于一个使能的中断，与每个中断向量号n关联的具体DTC中断源由ICU.IELSRn.IELS选择[7:0]，其中n=0到31，如表14.4，第14节中的事件表中所列，中断控制器单元(ICU)。对于软件激活，请参见第19.2.2节，事件链接软件事件生成

Register n (ELSEGRn) (n = 0, 1).

中断向量编号相当于DTC向量表编号。在DTC接受激活请求后，它不会接受另一个激活请求，直到该单个请求的传输完成，无论请求的优先级如何。如果在DMAC或DTC传输期间生成多个激活请求，则在传输完成时接受最高优先级的请求。当DTC模块起始位(DTCST.DTCST)为0时产生多个激活请求时，当DTCST.DTCST随后设置为1时，DTC接受最高优先级请求。较小的中断向量编号具有较高的优先级。

DTC在单次数据传输开始时执行以下操作，或者对于链式传输，在最后一次连续传输之后执行以下操作：

- 完成指定的一轮数据传输后，ICU.IELSRn.DTCE位设置为0，并向CPU发送中断请求
- 如果MRB.DISEL位为1，则在数据传输完成时向CPU发送中断请求
- 对于其他传输，激活源的ICU.IELSRn.IR位在数据传输开始时设置为0。

18.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 18.2 shows the relationship between the DTC vector table and transfer information. Figure 18.3 shows the allocation of transfer information in the SRAM area.

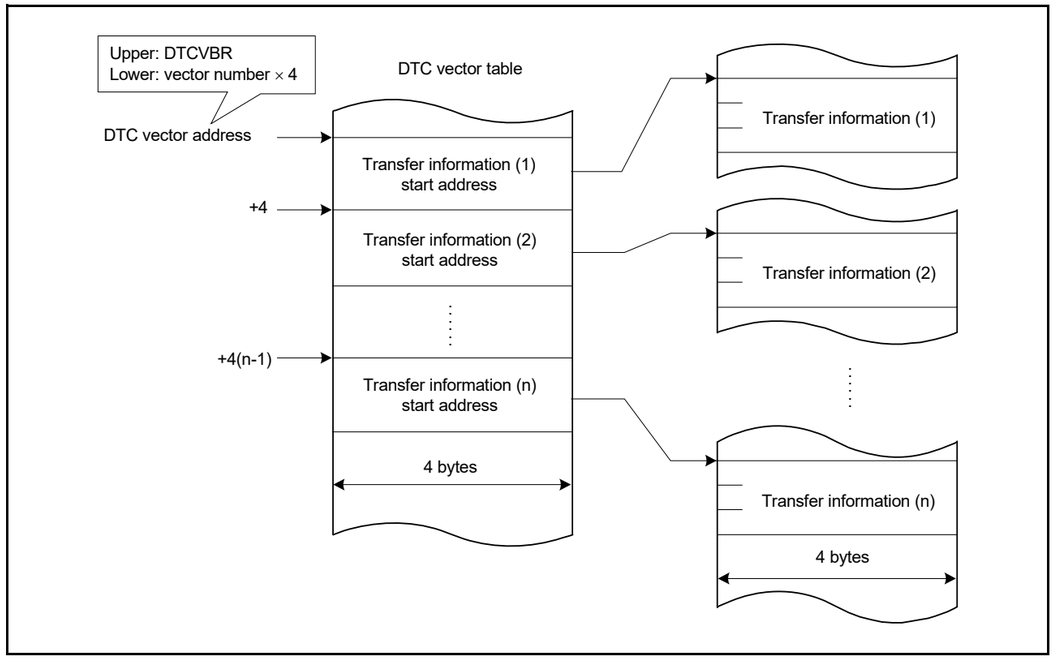


Figure 18.2 DTC vector table and transfer information

18.3.1 分配传输信息和DTC向量表

DTC从向量表中读取与每个激活源相关联的传输信息的起始地址，并读取从该地址开始的传输信息。

向量表的位置必须使基地址（起始地址）的低10位为0。使用DTC向量
基址寄存器(DTCVBR)用于设置DTC向量表的基地址。传输信息分配在SRAM区域中。在SRAM区域中，向量编号为n的传输信息n的起始地址必须与向量表中的基地址相加4n。

图18.2显示了DTC向量表和传输信息之间的关系。图18.3显示了SRAM区域中传输信息的分配。

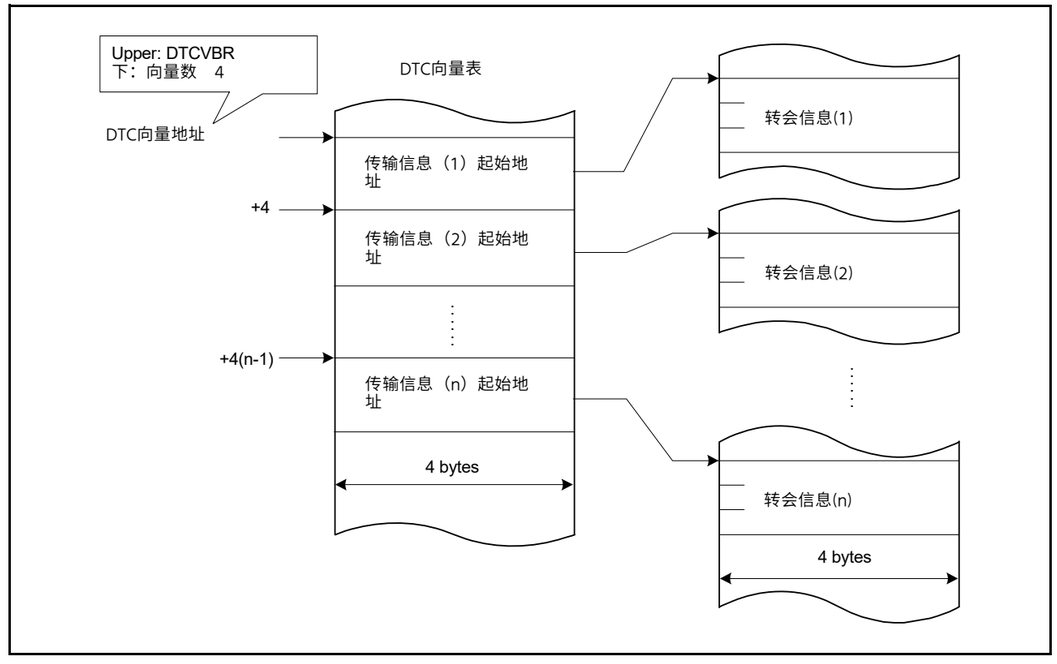


Figure 18.2 DTC向量表和传输信息

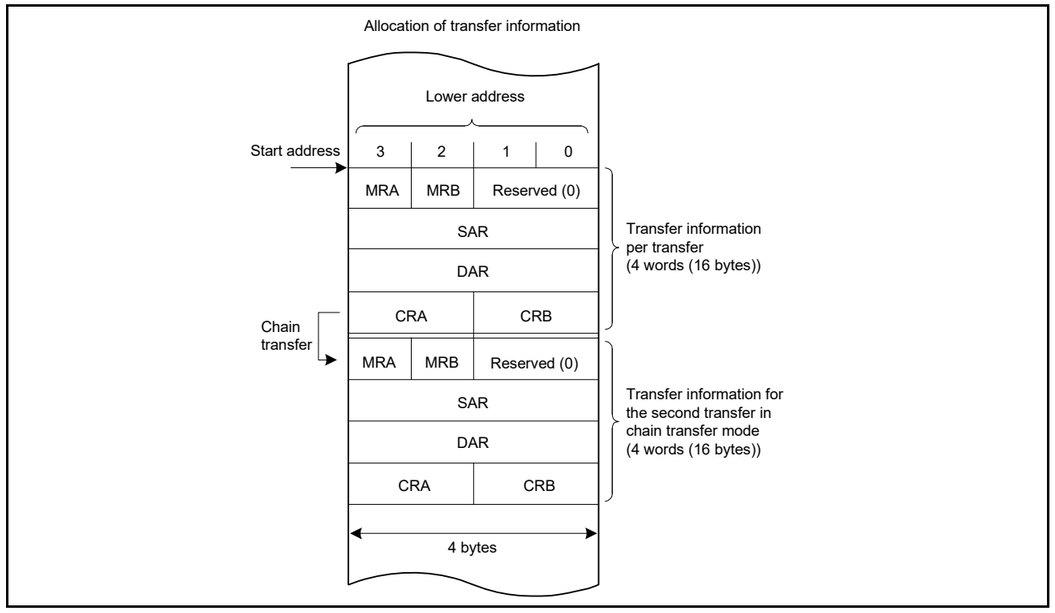


Figure 18.3 Allocation of transfer information in the SRAM area

18.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC then reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

There are three transfer modes:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values of these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 18.2 describes the DTC transfer modes.

Table 18.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bit), 1 halfword (16 bit), or 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65,536
Repeat transfer mode*1	1 byte (8 bit), 1 halfword (16 bit), or 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65,536

Note 1. Set the transfer source or transfer destination as the repeat area.
Note 2. Set the transfer source or transfer destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

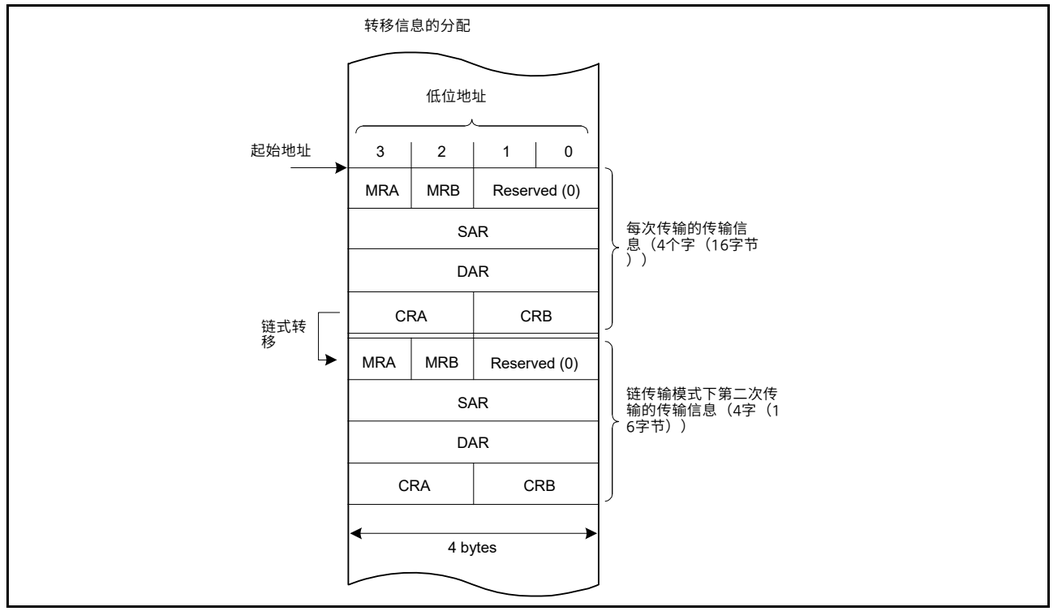


Figure 18.3 SRAM区域中传输信息的分配

18.4 Operation

DTC根据传输信息传输数据。在进行DTC操作之前，需要在SRAM区域中存储传输信息。当DTC被激活时，它会读取与向量编号相关联的DTC向量。然后DTC从DTC向量引用的传输信息存储地址中读取传输信息并传输数据。数据传输后，DTC写回传输信息。将传输信息存储在SRAM区域中可以实现任意数量的通道的数据传输。

共有三种传输方式：

- 正常传输模式
- 重复传输模式
- 块传输模式。

DTC指定SAR寄存器中的传输源地址和DAR寄存器中的传输目标地址。
这些寄存器的值在数据传输后独立地递增、递减或固定地址。

表18.2描述了DTC传输模式。

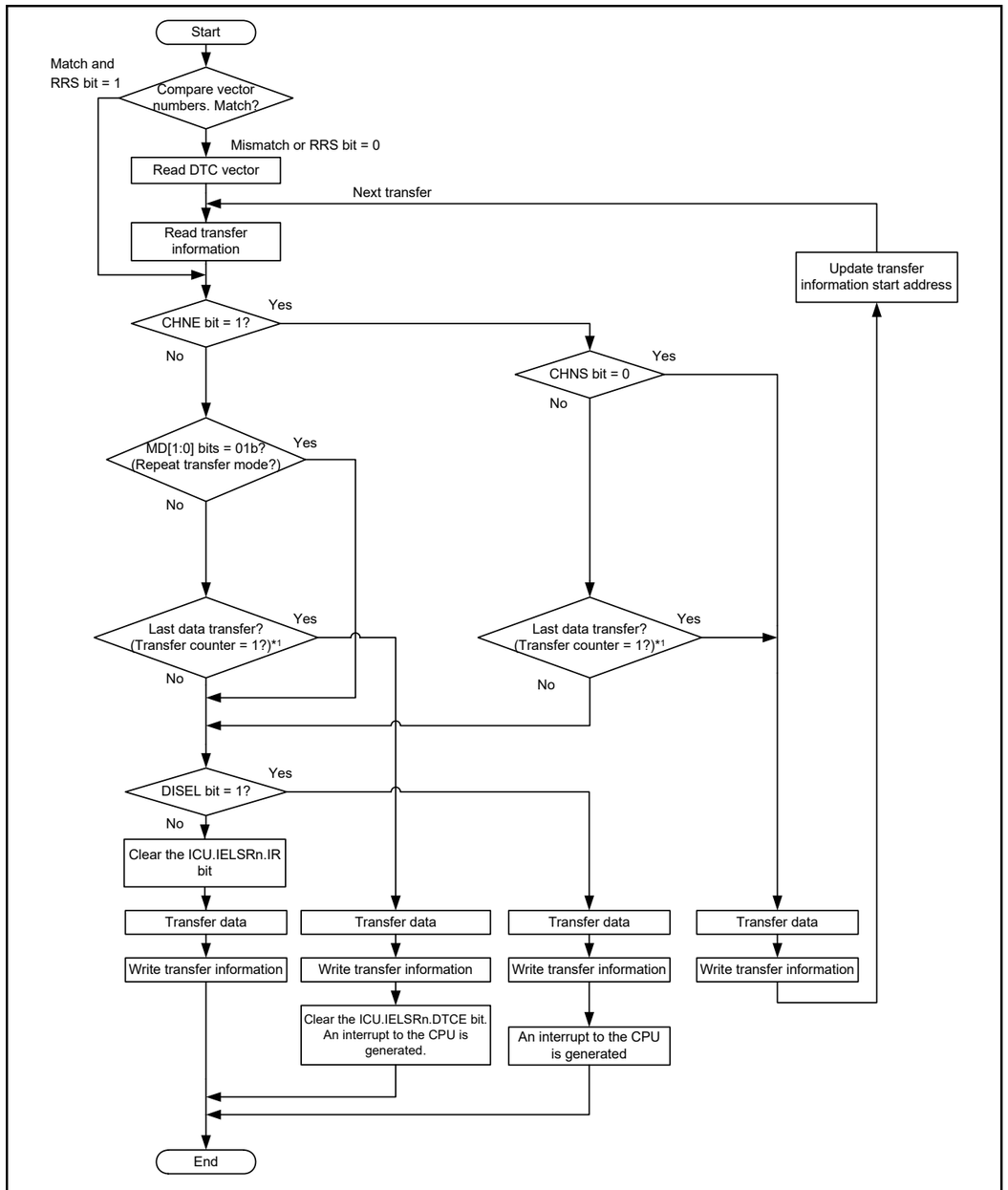
Table 18.2 DTC传输模式

传输模式	在单个传输请求上传输的数据大小	内存地址的递增或递减	可设置的传输次数
正常传输模式	1个字节（8位）、1个半字（16位）或1个字（32位）	递增或递减1、2或4或固定地址	1 to 65,536
重复传输模式*1	1个字节（8位）、1个半字（16位）或1个字（32位）	递增或递减1、2或4或固定地址	1 to 256*3
块传输模式*2	CRAH中指定的块大小（1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节））	递增或递减1、2或4或固定地址	1 to 65,536

Note 1. 将传输源或传输目标设置为重复区域。
Note 2. 将传输源或传输目标设置为块区域。
Note 3. 在指定计数的数据传输后，恢复初始状态并重新开始操作。

Setting the MRB.CHNE bit to 1 allows multiple transfers or chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 18.4 shows the operation flow of the DTC. Table 18.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

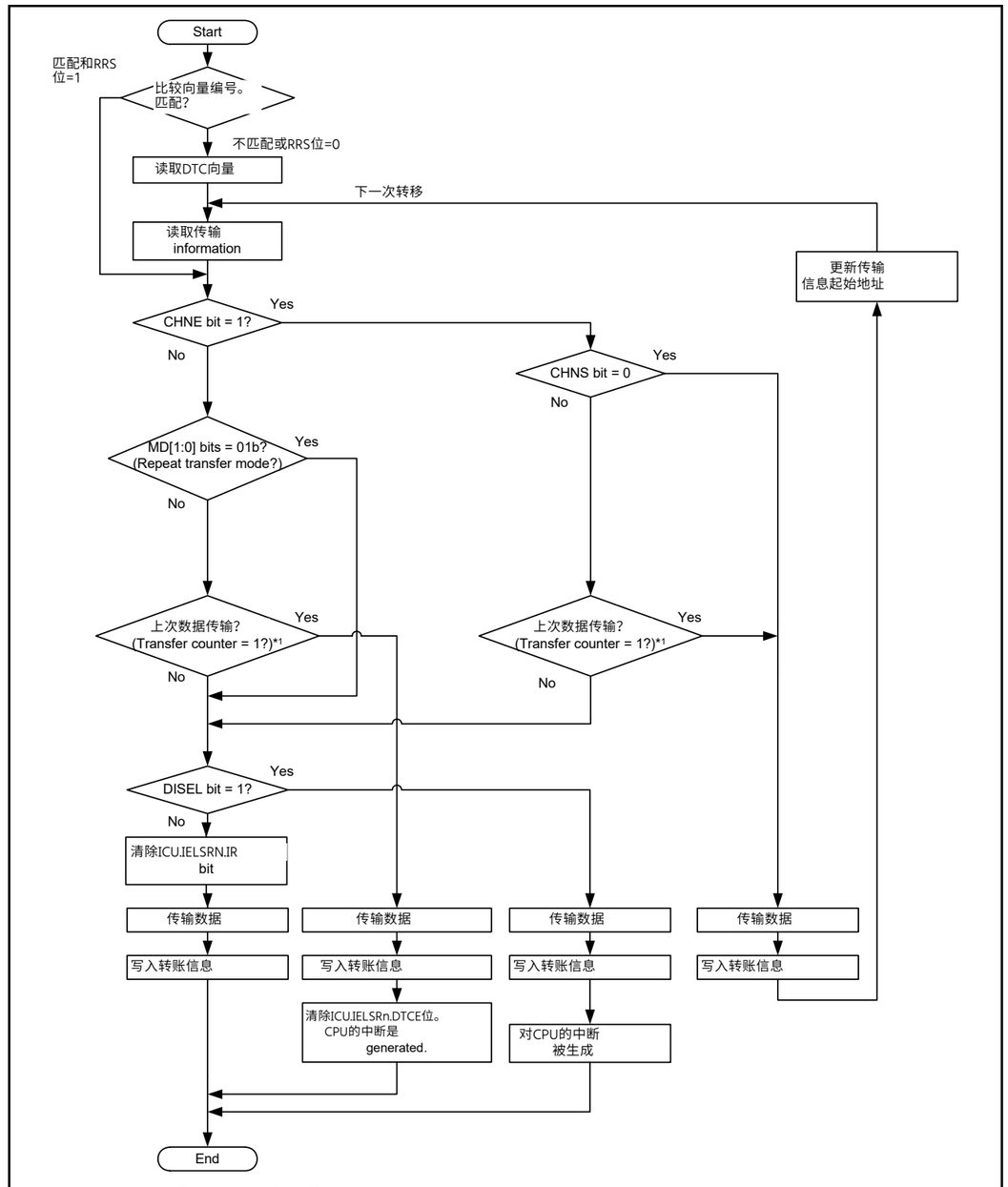


Note 1. Counter value before starting data transfer.

Figure 18.4 DTC operation flow

将MRB.CHNE位设置为1允许在单个激活源上进行多次传输或链式传输。当指定的数据传输完成时，它还启用链式传输。

图18.4显示了DTC的操作流程。表18.3列出了链转移条件。该表中省略了用于第二次和后续传输的控制信息的组合。



Note 1. 开始数据传输之前的计数器值。

Figure 18.4 DTC操作流程

Table 18.3 Chain transfer conditions

First transfer				Second transfer*3				
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	DTC transfer
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE bit = 1 is omitted.

18.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared to the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, or when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the RRS bit. Figure 18.12 shows an example of a transfer information read skip.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, and then set the RRS bit to 1. The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

18.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 18.4 lists the transfer information write-back skip conditions and the associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 18.3 链转移条件

首次转让				Second transfer*3				
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	DTC transfer
0	—	0	（1→0）以外	—	—	—	—	在第一次传输后结束
0	—	0	(1 → 0)	—	—	—	—	在第一次传输后结束，向CPU发出中断请求
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	0	(1→*)以外	—	—	—	—	在第一次传输后结束
1	1	—	(1 → *)	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	1	(1→*)以外	—	—	—	—	在第一次传输后结束，向CPU发出中断请求

Note 1. 使用的传输计数器取决于传输模式，如下所示：
正常传输模式—CRA寄存器重复传输模式—CRAL寄存器
块传输模式——CRB寄存器

Note 2. 数据传输完成后，计数器操作如下：1→0在正常和块传输模式下1→CRAH在重复传输模式下(1→*)表中表示这两种操作，具体取决于模式。

Note 3. 可以为第二次或后续转移选择链转移。省略了第二次传输和CHNE位=1的组合条件。

18.4.1 传输信息读取跳过功能

通过设置DTCCR.RRS位可以跳过向量地址和传输信息的读取。当产生一个DTC激活请求时，当前的DTC向量编号将与之前激活过程中的DTC向量编号进行比较。当这些向量编号匹配且RRS位设置为1时，执行DTC数据传输而不读取向量地址和传输信息。但是，当上一次传输是链式传输时，会读取向量地址和传输信息。此外，如果在上次正常传输期间传输计数器（CRA寄存器）变为0，或者在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位如何，都将读取传输信息。图18.12显示了传输信息读取跳过的示例。

要更新向量表和传输信息，请将RRS位设置为0，更新向量表和传输信息，然后将RRS位设置为1。通过将RRS位设置为0，丢弃存储的向量编号。更新的DTC向量表和传输信息在下一个激活过程中被读取。

18.4.2 传输信息回写跳过功能

当MRA.SM[1:0]位或MRB.DM[1:0]位设置为地址固定时，部分传输信息不会被写回。表18.4列出了传输信息回写跳过条件和相关寄存器。回写CRA和CRB寄存器，跳过回写MRA和MRB寄存器。

Table 18.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR register	DAR register
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

18.4.3 Normal Transfer Mode

The normal transfer mode allows a 1-byte (8 bit), 1-halfword (16 bit), 1-word (32 bit) data transfer on a single activation source. The transfer count can be set from 1 to 65536. Transfer source and transfer destination addresses can be independently set to increment, decrement, or remain fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 18.5 lists register functions in normal transfer mode, and Figure 18.5 shows the memory map of normal transfer mode.

Table 18.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, or fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

Table 18.4 传输信息回写跳过条件和适用寄存器

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR寄存器	DAR寄存器
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

18.4.3 正常传输模式

正常传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）、1字（32位）数据。传输计数可以设置为1到65536。传输源地址和传输目标地址可以独立设置为递增、递减或保持固定。此模式允许在指定计数传输结束时向CPU生成中断请求。

表18.5列出了正常传输模式下的寄存器功能，图18.5显示了正常传输模式下的内存映射。

Table 18.5 正常传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	递增、递减或固定*1
DAR	转移目的地地址	递增、递减或固定*1
CRA	转帐柜台A	CRA - 1
CRB	转帐柜台B	未更新

Note 1. 在地址固定模式下会跳过回写操作。

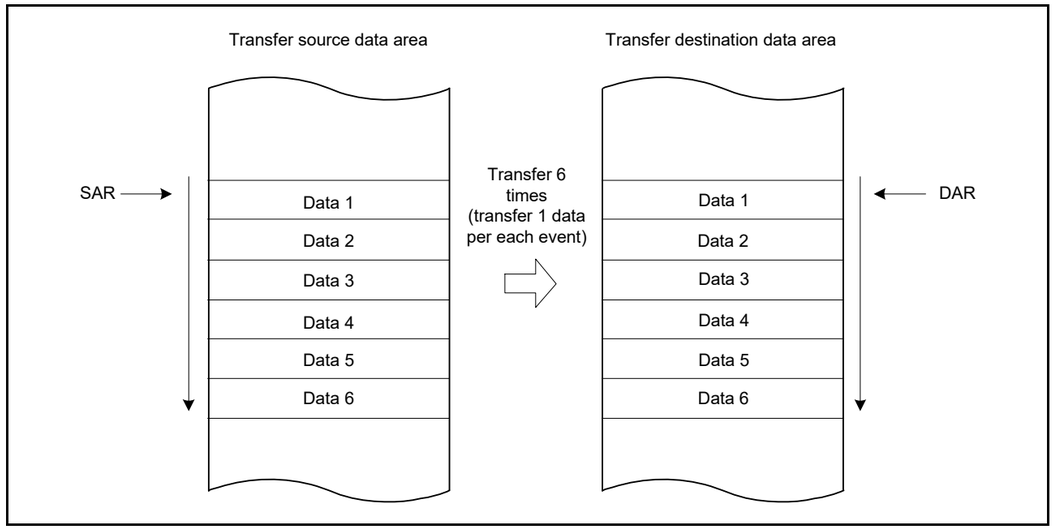


Figure 18.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0006h)

18.4.4 Repeat Transfer Mode

The repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Transfer source or transfer destination for the repeat area must be specified in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified-count transfer is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 00h in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not become 00h, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer is complete.

Table 18.6 lists the register functions in repeat transfer mode, and Figure 18.6 shows the memory map of repeat transfer mode.

Table 18.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed*1.
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

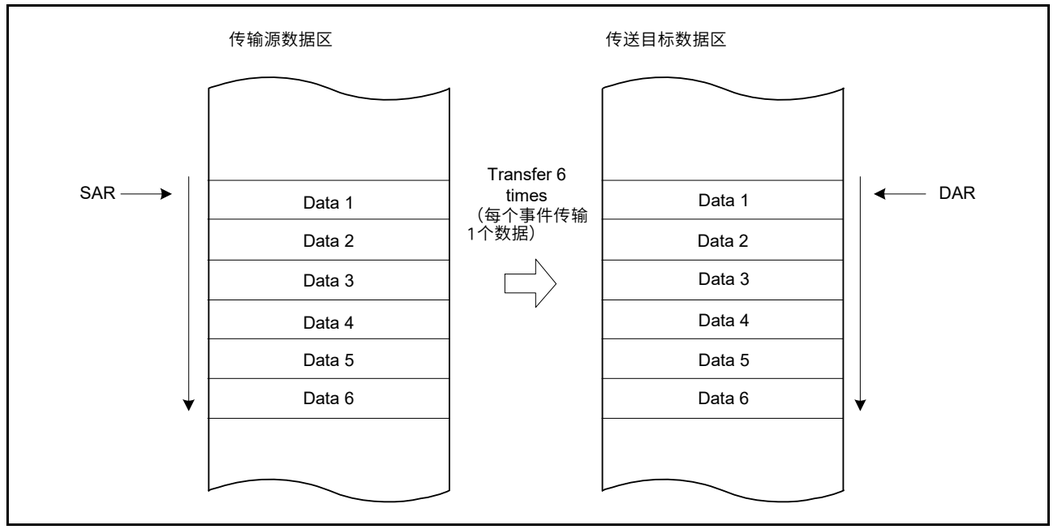


Figure 18.5 正常传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRA=0006h)

18.4.4 重复传输模式

重复传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）或1字（32位）数据。重复区域的传输源或传输目标必须在MRB.DTS位中指定。传送计数可设置为1到256。当指定计数传送完成时，重复区域中指定的地址寄存器的初始值被恢复，传送计数器的初始值被恢复，并重复传送。另一个地址寄存器连续递增或递减或保持不变。

当传输计数器CRAL在重复传输模式下递减到00h时，CRAL值将更新为CRAH寄存器中设置的值。因此，传输计数器不会变为00h，这会在MRB.DISEL位设置为0时禁用对CPU的中断请求。当指定的数据传输完成时，会向CPU发出中断请求。

表18.6列出了重复传输模式下的寄存器功能，图18.6显示了重复传输模式的内存映射。

Table 18.6 重复传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值	
		当CRAL不为1时	当CRAL为1时
SAR	传输源地址	递增、递减或固定*1	当MRB.DTS位为0时递增、递减或固定*1 当MRB.DTS位为1时SAR寄存器初始值。
DAR	转移目的地地址	递增、递减或固定*1	当MRB.DTS位为0时DAR寄存器初始值 当MRB.DTS位为1时递增、递减或固定*1。
CRAH	保留转帐计数器	CRAH	CRAH
CRAL	转帐柜台A	CRAL - 1	CRAH
CRB	转帐柜台B	未更新	未更新

Note 1. 在地址固定模式下会跳过回写。

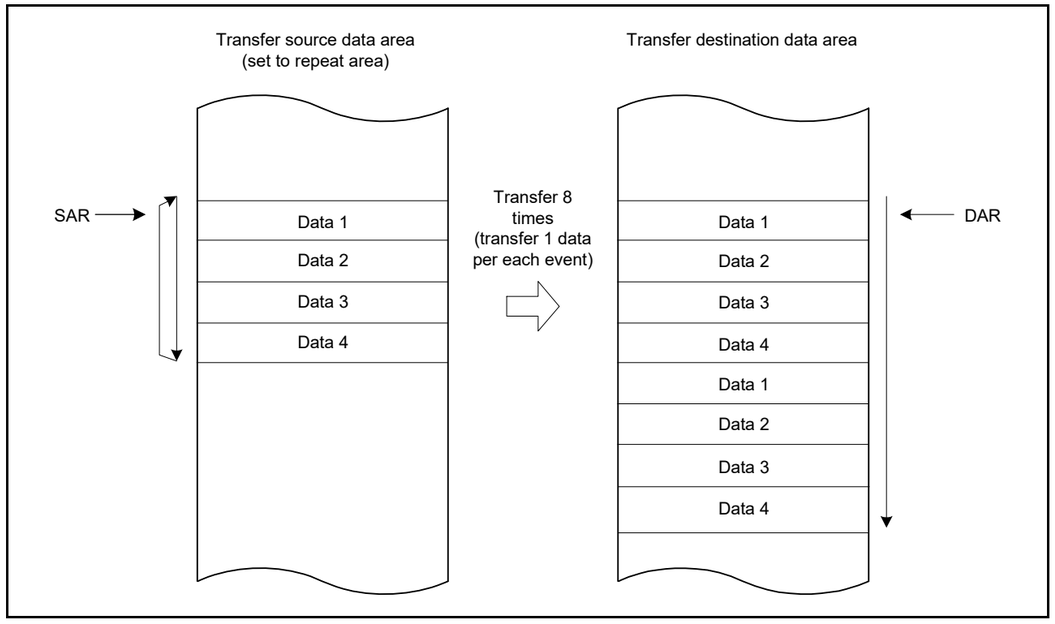


Figure 18.6 Memory map of repeat transfer mode when transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 04h)

18.4.5 Block Transfer Mode

The block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS bit is 1 or the DAR register when the DTS bit is 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65,536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 18.7 lists register functions in block transfer mode, and Figure 18.7 shows the memory map for block transfer mode.

Table 18.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed*1.
CRAH	Retains block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

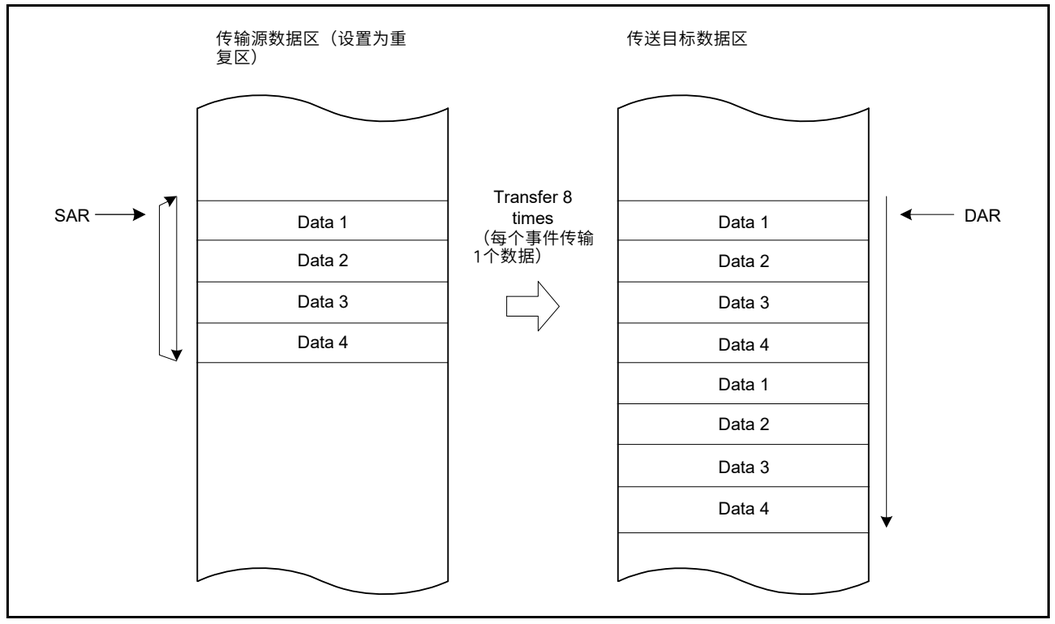


Figure 18.6 传输源为重复区域时重复传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0] = 10b, CRAH = 04h)

18.4.5 块传输模式

块传输模式允许在单个激活源上进行单块数据传输。块区域的传输源或传输目标必须在MRB.DTS位中指定。块大小可以设置为1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节）。当指定块的传输完成时，块区域中指定的块大小计数器CRAL和地址寄存器（MRB.DTS位为1时为SAR寄存器或DTS位为0时为DAR寄存器）的初始值是恢复。另一个地址寄存器连续递增或递减或保持不变。

传输计数（块计数）可以设置为1到65 536。此模式允许在指定计数块传输结束时向CPU生成中断请求。

表18.7列出了块传输模式下的寄存器功能，图18.7显示了块传输模式下的存储器映射。

Table 18.7 块传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	当MRB.DTS位为0时递增、递减或固定*1 当MRB.DTS位为1时SAR寄存器初始值。
DAR	转移目的地地址	当MRB.DTS位为0时DAR寄存器初始值 当MRB.DTS位为1时递增、递减或固定*1。
CRAH	保留块大小	CRAH
CRAL	块大小计数器	CRAH
CRB	块传输计数器	CRB - 1

Note 1. 在地址固定模式下会跳过回写。

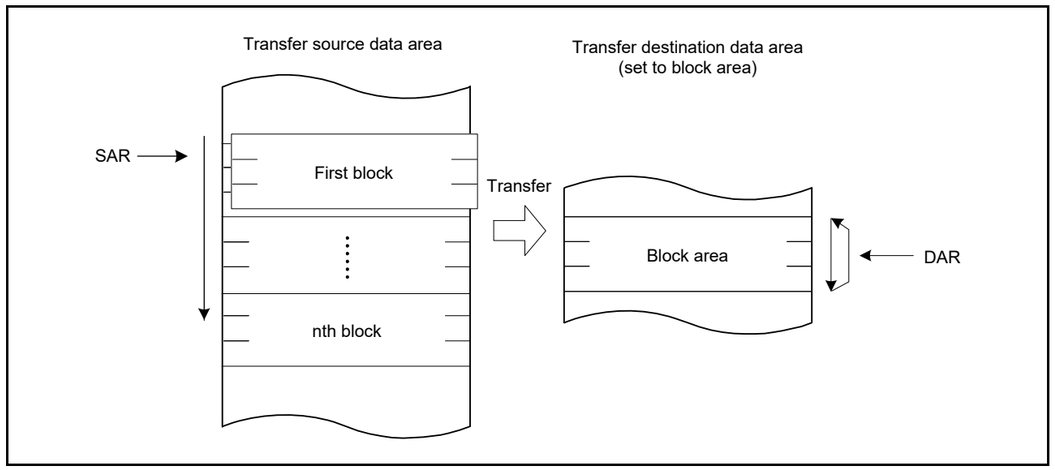


Figure 18.7 Memory map of block transfer mode

18.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR bit of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define data transfer. Figure 18.8 shows a chain transfer operation.

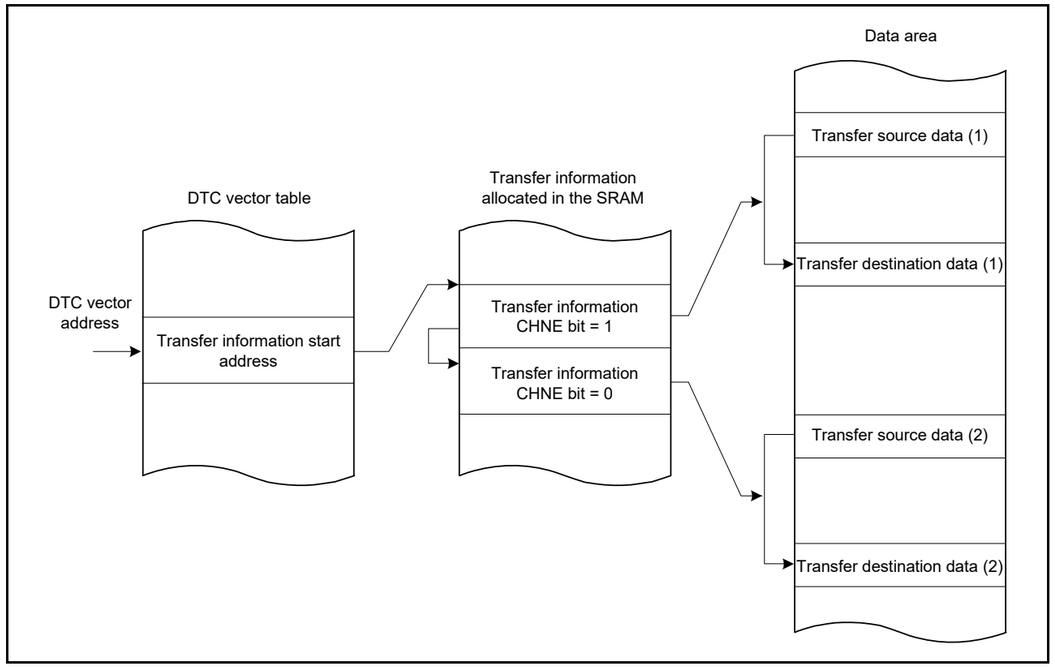


Figure 18.8 Chain transfer operation

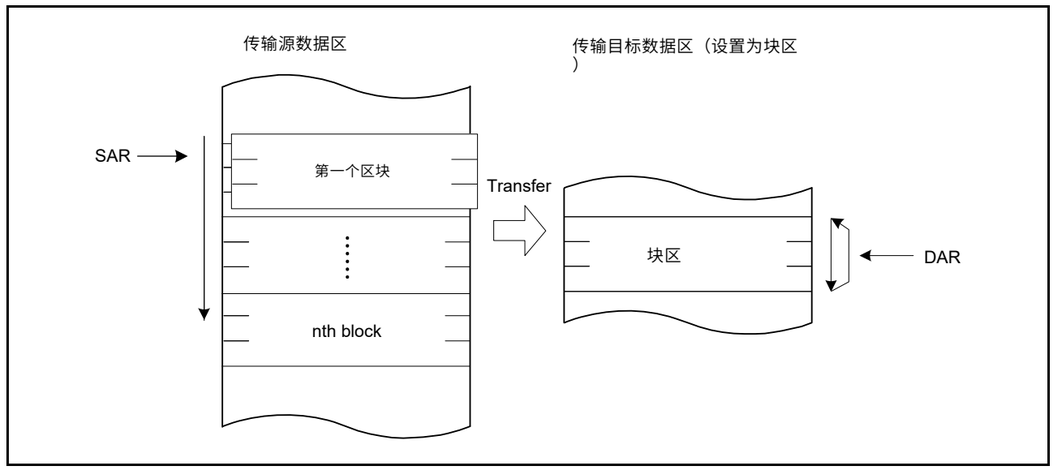


Figure 18.7 块传输模式的内存映射

18.4.6 链转移

将MRB.CHNE位设置为1允许在单个激活源上连续执行链传输。如果
MRB.CHNE设置为1，CHNS设置为0，在完成指定的传输轮数或将MRB.DISEL位设置为1时不会向CPU产生中断请求。向CPU发送中断请求每次执行DTC数据传输。数据传输对激活源的ICU.IELSRn.IR位没有影响。

SAR、DAR、CRA、CRB、MRA和MRB寄存器可以相互独立设置以定义数据传输。
图18.8显示了一个链式转移操作。

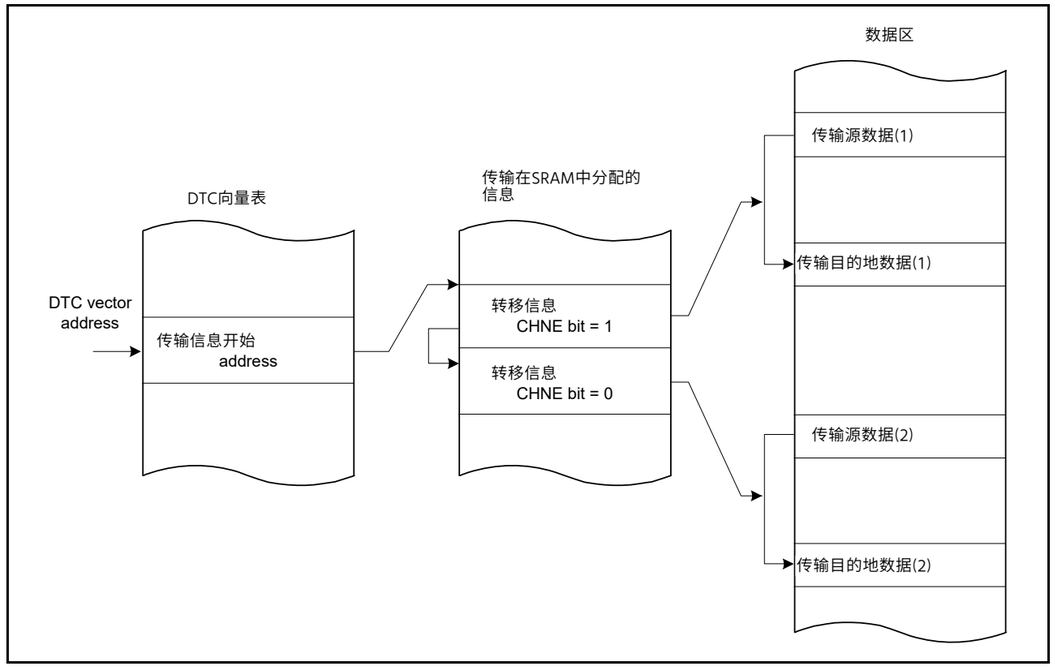


Figure 18.8 链转移操作

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 18.3, Chain transfer conditions.

18.4.7 Operation Timing

Figure 18.9 to Figure 18.12 are timing diagrams that show the minimum number of execution cycles.

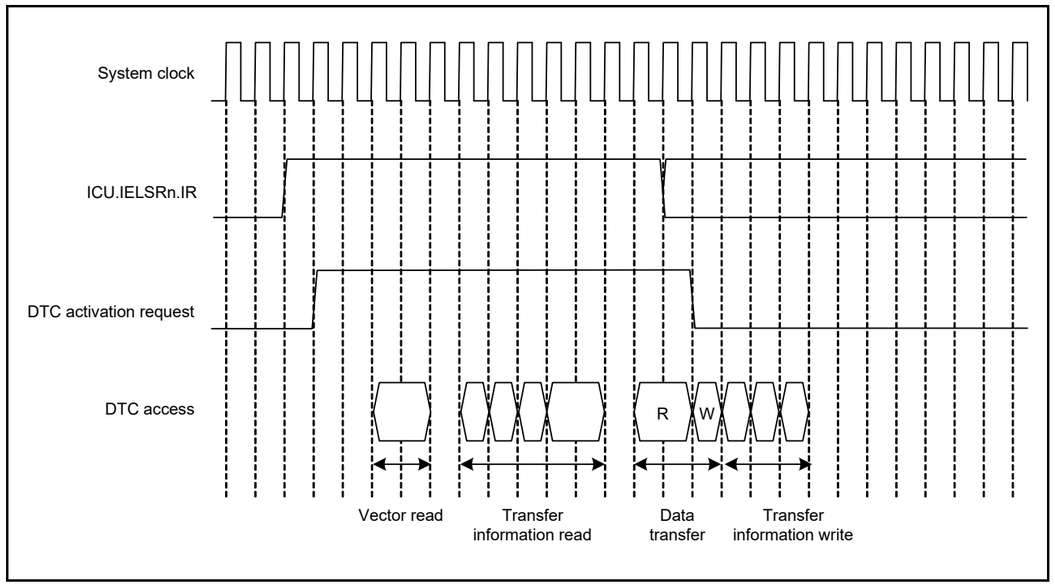


Figure 18.9 Example 1 of DTC operation timing in normal transfer mode and repeat transfer mode

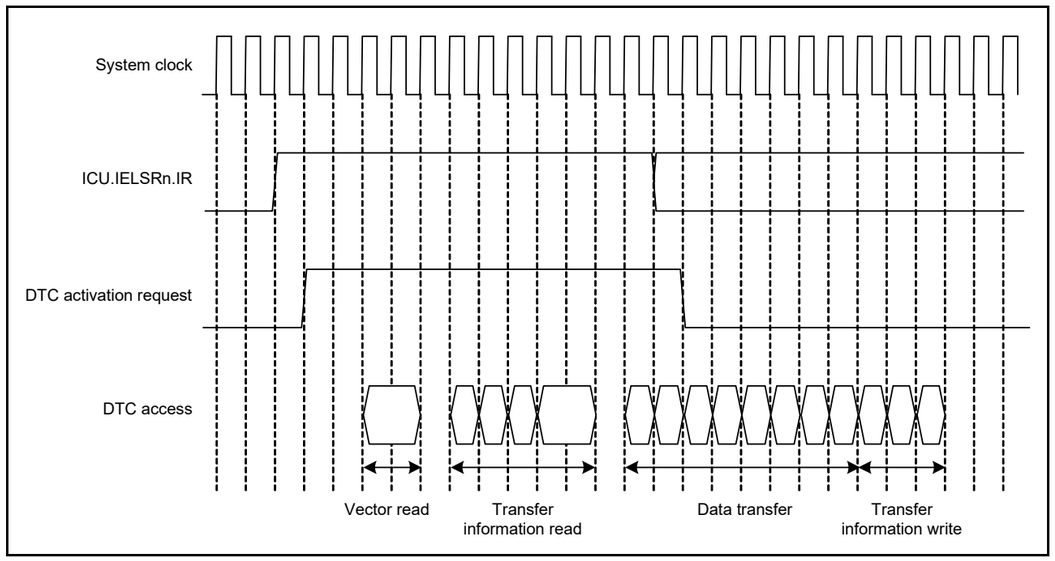


Figure 18.10 Example 2 of DTC operation timing in block transfer mode when block size = 4

将1写入MRB.CHNE和CHNS位可以使链式传输仅在完成指定的数据传输后执行。在重复传输模式下，在完成指定的数据传输后执行链式传输。有关链转移条件的详细信息，请参见表18.3，链转移条件。

18.4.7 操作时间

图18.9至图18.12是显示最小执行周期数的时序图。

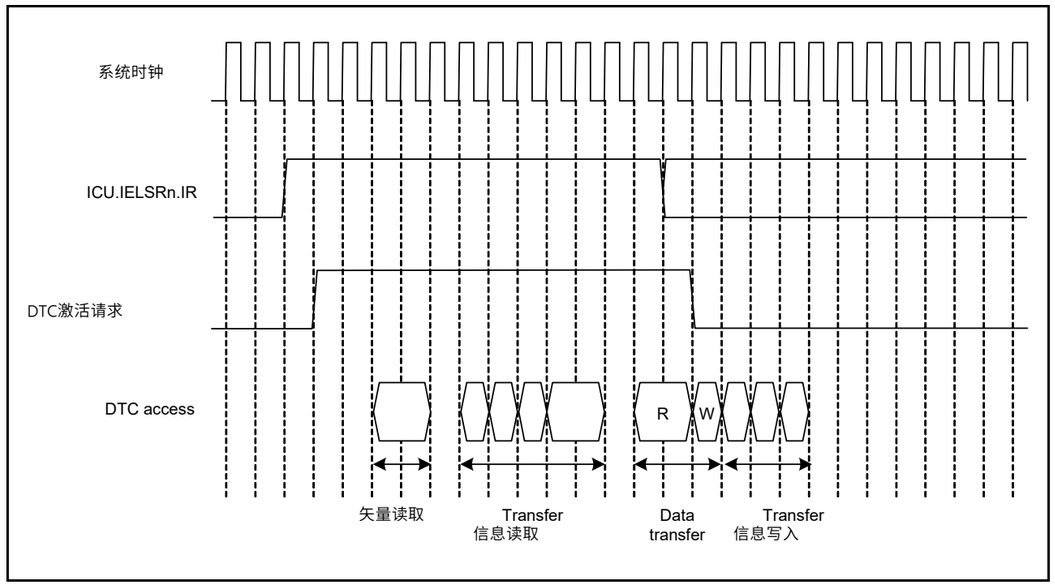


Figure 18.9 正常传输模式和重复传输模式下的DTC操作时序示例1

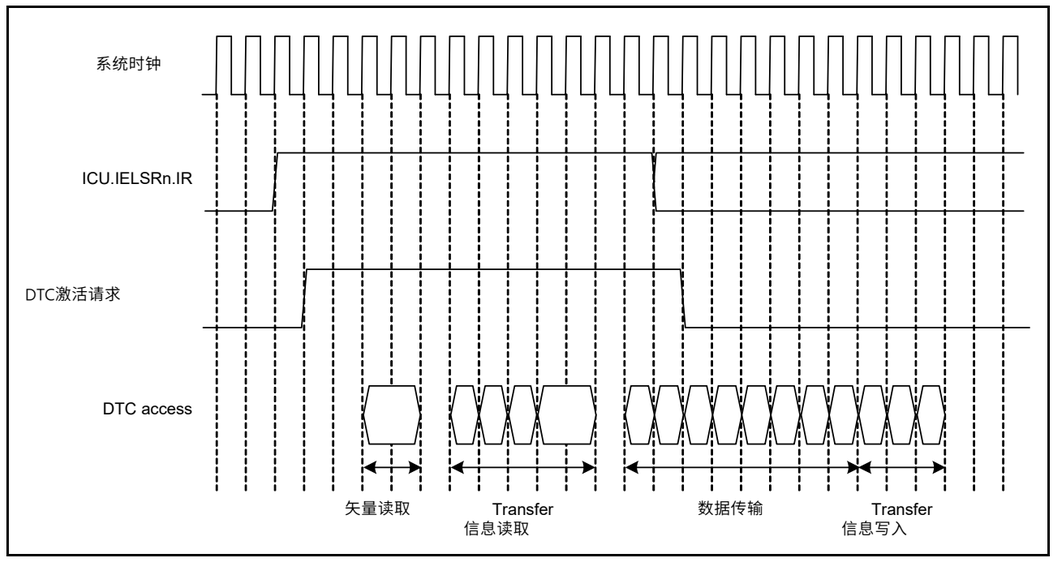


Figure 18.10 块大小=4时块传输模式下的DTC操作时序示例2

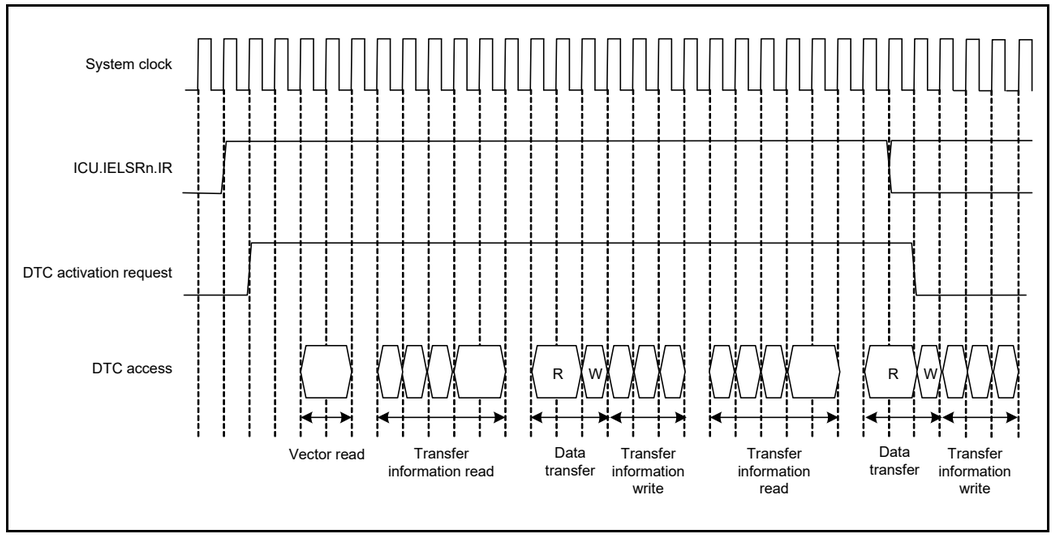
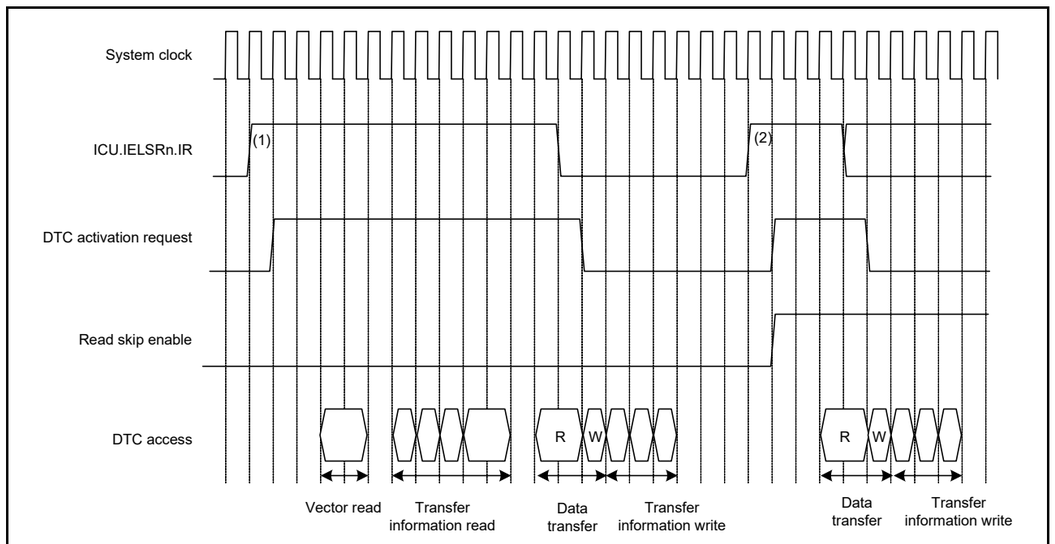


Figure 18.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS bit = 1, the transfer information read for request (2) is skipped.

Figure 18.12 Example of operation when a transfer information read is skipped, with the vector, transfer information, transfer destination data on the SRAM, and the transfer source data on the peripheral module

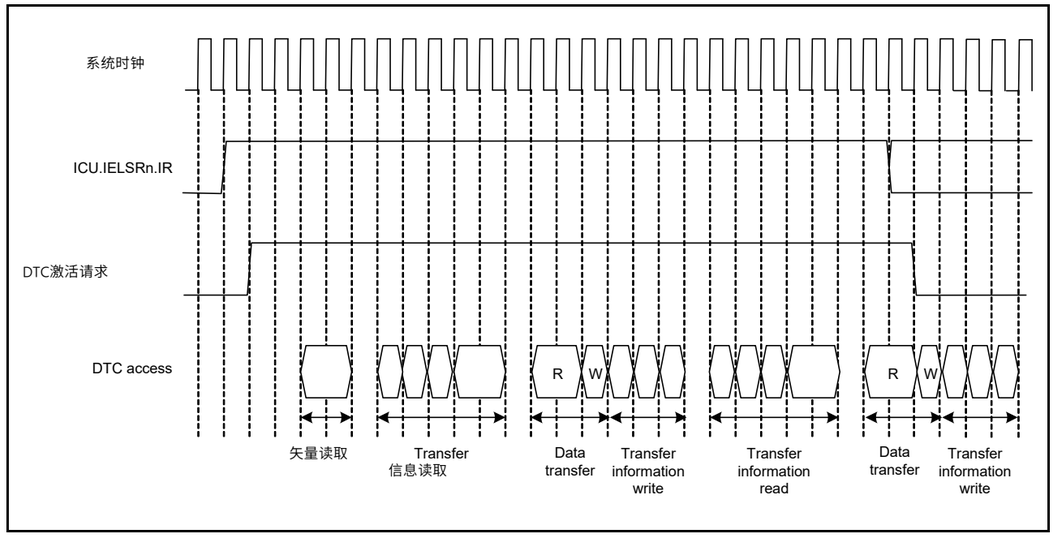
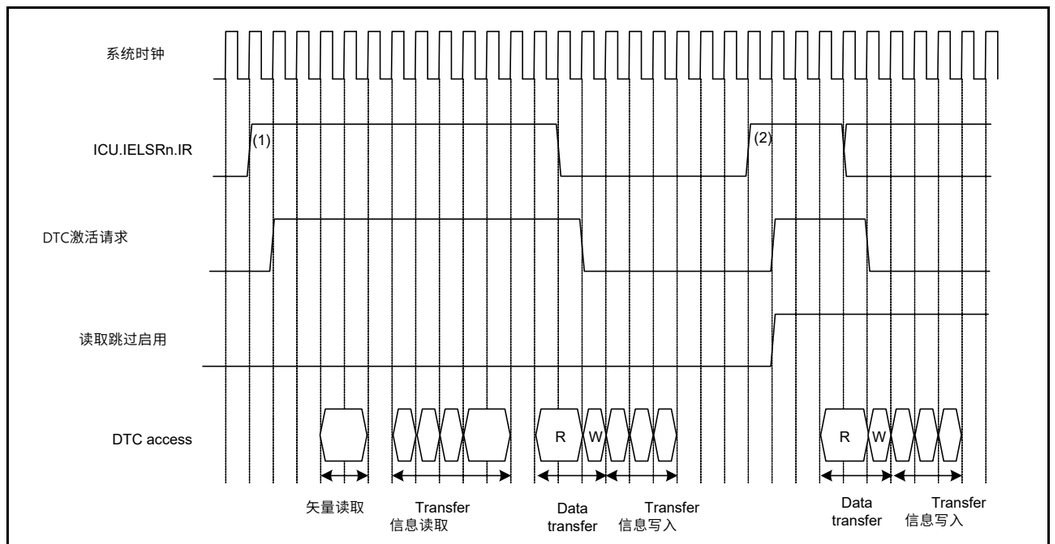


Figure 18.11 链转移的DTC操作时序示例3



Note: 当(1)和(2)的激活源(向量号)相同且RRS比特=1时，跳过请求(2)读取的传输信息。

Figure 18.12 跳过传输信息读取时的操作示例，包含向量、传输信息、SRAM上的传输目标数据和外围模块上的传输源数据

18.4.8 Execution Cycles of DTC

Table 18.8 lists the execution cycles of single data transfer of the DTC.

For the order of the execution states, see section 18.4.7, Operation Timing.

Table 18.8 Execution cycles of DTC

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci+1*2	2 × Ci+1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer is applied.

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
The unit is system clocks (ICLK) for + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 42, SRAM, section 43, Flash Memory, and section 15, Buses.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
This table does not include the time until DTC data transfer starts after the DTC activation source becomes active.

18.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 15, Buses.

18.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Figure 18.13 shows the procedure for setting the DTC.

18.4.8 DTC的执行周期

表18.8列出了DTC单次数据传输的执行周期。

有关执行状态的顺序，请参阅第18.4.7节，操作时序。

Table 18.8 DTC的执行周期

传输模式	矢量读取		传输信息读取		传输信息写入			数据传输		内部运作	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci+1*2	2 × Ci+1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

Note 1. 跳过传输信息读取时。
Note 2. 当SAR和DAR均未设置为地址固定模式时。
Note 3. 当SAR或DAR设置为地址固定模式时。
Note 4. 当SAR和DAR设置为地址固定模式时。
Note 5. 当块大小为2或更大时。如果块大小为1，则应用正常传输的周期数。

P：块大小（CRAH和CRAL的初始设置）
Cv：访问向量传输信息存储目标的周期Ci：访问传输信息存储目标地址的周期
Cr：访问数据读取目标的周期Cw：访问数据写入目标的周期
单位是系统时钟(ICLK)，用于向量读取、传输信息读取和数据传输读取列中的+1和2内部操作栏。
Cv、Ci、Cr和Cw根据相应的访问目的地而变化。有关各个访问目标的周期数，请参阅第42节SRAM、第43节闪存和第15节总线。系统时钟和外设时钟的频率比也被考虑在内。

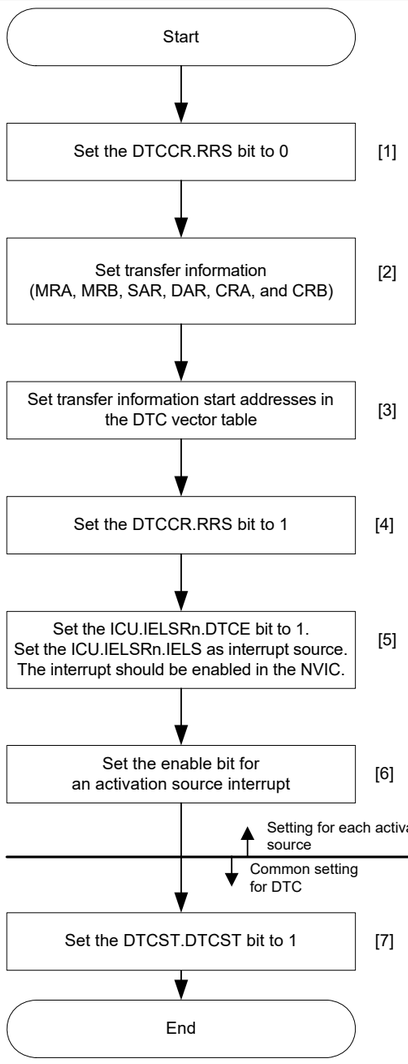
DTC响应时间是从检测到DTC激活源到DTC传输开始的时间。
此表不包括从DTC激活源激活到DTC数据传输开始的时间。

18.4.9 DTC总线主控释放时序

在传输信息读取期间，DTC不会释放总线主控权。在读取或写入传输信息之前，根据总线主仲裁器确定的优先级对总线进行仲裁。对于总线仲裁，请参见第15节，总线。

18.5 DTC设置程序

在使用DTC之前，请设置DTC向量基址寄存器(DTCVBR)。图18.13显示了设置DTC.



Set the ICU.IELSRn.IELS[7:0] bit to 0 to disable the interrupt in the NVIC and provide the following settings:

[1] Set the DTCCR.RRS bit to 0 to reset the transfer information read skip flag. After that, transfer information read is not skipped while the DTC is activated. Be sure to specify this setting when transfer information is updated.

[2] Allocate the transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) in the data area. To set transfer information, see section 18.2, Register Descriptions. To allocate transfer information, see section 18.3.1, Allocating Transfer Information and DTC Vector Table.

[3] Set the transfer information start addresses in the DTC vector table. To set the DTC vector table, see section 18.3.1, Allocating Transfer Information and DTC Vector Table.

[4] Set the DTCCR.RRS bit to 1 to enable skipping of the second and the subsequent transfer information read cycles for continuous DTC activation from the same interrupt source. The RRS bit can be set to 1, but if this is set during DTC transfer, it becomes valid from the next transfer.

[5] Set the ICU.IELSRn.DTCE bit to 1. Set ICU.IELSRn.IELS as the interrupt sources that trigger DTC. The interrupt must be enabled in the NVIC. See Table 14.4, Event table.

[6] Set the enable bit for an activation source interrupt to 1. When a source interrupt is generated, the DTC is activated. To set the interrupt source enable bit, see the settings for the modules that are to be the activation sources.

[7] Set the DTC Module Start bit (DTCST.DTCST) to 1.

Note: The DTCST.DTCST bit can be set even if the setting for the activation source is not complete.

Figure 18.13 DTC setting procedure

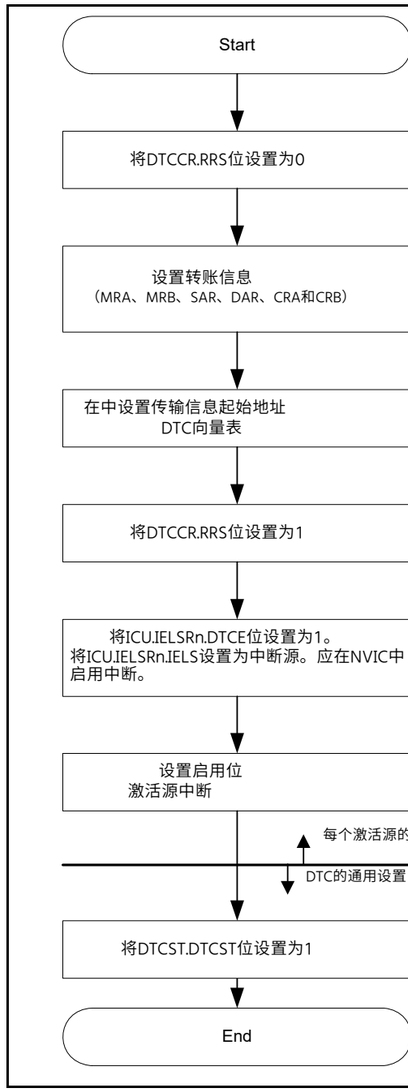
18.6 Examples of DTC Usage

18.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] bits = 00b), normal transfer mode (MRA.MD[1:0] bits = 00b), and byte-sized transfer (MRA.SZ[1:0] bits = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] bits = 10b) and single data transfer by a single interrupt (MRB.CHNE bit = 0 and MRB.DISEL bit = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the SRAM area for data storage in the DAR register, and 128 (0080h) in the CRA register. The CRB register can be set to any value.



将ICU.IELSRn.IELS[7:0]位设置为0以禁用NVIC中的中断并提供以下设置：

[1] 将DTCCR.RRS位设置为0以重置传输信息读取跳过标志。之后，在激活DTC时不会跳过读取的传输信息。请务必在传输信息更新时指定此设置。

[2] 分配传输信息（MRA、MRB、SAR、DAR、CRA和CRB）在数据区。要设置传输信息，请参阅第18.2节，寄存器说明。要分配传输信息，请参阅第18.3.1节，分配传输信息和DTC向量表。

[3] 在DTC向量表中设置传输信息起始地址。要设置DTC向量表，请参阅第18.3.1节，分配传输信息和DTC向量表。

[4] 将DTCCR.RRS位设置为1以允许跳过第二个和后续传输信息读取周期，以便从同一中断源连续激活DTC。RRS位可以设置为1，但如果在DTC传输期间设置，则从下一次传输开始生效。

[5] 将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS设置为触发DTC的中断源。必须在NVIC中启用中断。请参见表14.4，事件表。

[6] 将激活源中断的使能位设置为1。
当产生源中断时，DTC被激活。
要设置中断源使能位，请参见要成为激活源的模块的设置。

[7] 将DTC模块起始位(DTCST.DTCST)设置为1。

Note: 即使激活源的设置未完成，也可以设置DTCST.DTCST位。

Figure 18.13 DTC设置程序

18.6 DTC使用示例

18.6.1 正常转移

本节提供从SCI接收128字节数据时的DTC用法及其应用示例。

(1) 传输信息设置

在MRA寄存器中，选择固定源地址（MRA.SM[1:0]位=00b）、正常传输模式（MRA.MD[1:0]位=00b）和字节大小传输（MRA.SZ[1:0]位=00b)。在MRB寄存器中，指定目标地址的递增（MRB.DM[1:0]位=10b）和单个中断的单个数据传输（MRB.CHNE位=0和MRB.DISEL位=0）。MRB.DTS位可以设置为任何值。在SAR寄存器中设置SCI的RDR寄存器地址，在DAR寄存器中设置用于数据存储的SRAM区域的起始地址，在CRA寄存器中设置128（0080h）。CRB寄存器可以设置为任何值。

(2) DTC vector table settings

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allows the CPU to accept receive error interrupts.

(5) DTC transfer

Each time a reception of 1 byte by the SCI completes, an RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

18.6.2 Chain Transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfers to transfer PWM timer compare data and change the period of the PWM timer for the GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPTm.GTCCRC register (m = 320 to 323, 164 to 169). For the second transfer, normal transfer mode is specified for transfer to the GPTm.GTCCRE register. For the third transfer, normal transfer mode is specified for transfer to the GPTm.GTPBR register. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE bit = 0.

The following example shows how to use the counter overflow interrupt with a GPT320.GTPR register as an activating source for the DTC.

(1) First transfer information setting

Set up transfer to the GPT320.GTCCRC register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] bits = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] bits = 00b) and word-sized transfer (MRA.SZ[1:0] bits = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] bits = 00b) and set up chain transfer (MRB.CHNE bit = 1 and MRB.CHNS bit = 0).
4. Set the SAR to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information setting

Set up transfer to the GPT320.GTCCRE register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] bits = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] bits = 00b) and word-sized transfer (MRA.SZ[1:0] bits = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] bits = 00b) and set up chain transfer (MRB.CHNE bit = 1 and MRB.CHNS bit = 0).

(2) DTC向量表设置

RXI中断的传输信息的起始地址在DTC的向量表中设置。

(3) ICU设置和DTC模块激活

将ICU.IELSRn.DTCE位设置为1，并将ICU.IELSRn.IELS设置为SCI中断。中断必须在启用
英伟达。将DTCST.DTCST位设置为1。

(4) SCI设置

通过将SCI中的SCR.RIE位设置为1来启用RXI中断。如果在SCI接收操作期间发生接收错误，则接收停止。要管理此问题，请使用允许CPU接受接收错误中断的设置。

(5) DTC transfer

每次SCI完成1个字节的接收，就会产生一个RXI中断来激活DTC。DTC将接收到的字节从SCI的RDR传输到SRAM，之后DAR寄存器递增，CRA寄存器递减。

(6) 中断处理

在128轮数据传输完成后，CRA寄存器中的值变为0，产生一个RXI中断请求给CPU。完成该中断处理程序中的处理。

18.6.2 链转移

本节提供了DTC链传输的示例，并描述了其在DTC输出脉冲中的使用
通用PWM定时器(GPT)。您可以使用链式传输来传输PWM定时器比较数据并更改GPT的PWM定时器的周期。

对于第一个链传输，指定正常传输模式以传输到GPTm.GTCCRC寄存器（m=320到323、164到169）。对于第二次传输，指定正常传输模式以传输到GPTm.GTCCRE寄存器。对于第三次传输，指定正常传输模式以传输到GPTm.GTPBR寄存器。这是因为在完成指定数量的传输时清除激活源和产生中断仅限于链传输的第三个，即在MRB.CHNE位=0时传输。

以下示例显示了如何使用带有GPT320.GTPR寄存器的计数器溢出中断作为DTC的激活源。

(1) 首次转账信息设置

设置传输到GPT320.GTCCRC寄存器：

1. 在MRA寄存器中，选择源地址的增量（MRA.SM[1:0]位=10b）。
2. 将传输设置为正常传输模式（MRA.MD[1:0]位=00b）和字长传输（MRA.SZ[1:0]位=10b）。
3. 在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]位=00b）并设置链式传输（MRB.CHNE位=1和MRB.CHNS位=0）。
4. 将SAR设置为数据表的首地址。
5. 将DAR寄存器设置为GPT320.GTCCRC寄存器的地址。
6. 将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(2) 二转信息设置

设置传输到GPT320.GTCCRE寄存器：

1. 在MRA寄存器中，选择源地址的增量（MRA.SM[1:0]位=10b）。
2. 将传输设置为正常传输模式（MRA.MD[1:0]位=00b）和字长传输（MRA.SZ[1:0]位=10b）。
3. 在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]位=00b）并设置链式传输（MRB.CHNE位=1和MRB.CHNS位=0）。

4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information set

Set up transfer to the GPT320.GTPBR register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] bits = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] bits = 00b) and word-sized transfer (MRA.SZ[1:0] bits = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] bits = 00b) and set up single data transfer per interrupt (MRB.CHNE bit = 0, MRB.DISEL bit = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(4) Transfer information assignment

Place the transfer information for use in the transfer to the GPT320.GTPBR immediately after the transfer control information for use in the GPT320.GTCCRC and GPT320.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT320.GTCCRC and GPT320.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT320 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[7:0] to 97 (61h) for the GPT320 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT320.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT320.GTCCRA and GPT320.GTCCRB registers and the next PWM timer compare values in the GPT320.GTCCRC and GPT320.GTCCRE registers.
3. Set the default PWM timer period values in the GPT320.GTPR register and the next PWM timer period values in the GPT320.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the Peripheral Select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT320.GTSTR.CSTRT bits to 1 to start the GPT320.GTCNT counter.

(9) DTC transfer

Each time a GPT320 counter overflow is generated with the GPT320.GTPR register, the next PWM timer compare values are transferred to the GPT320.GTCCRC and GPT320.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT320.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT320 counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

4. 将SAR寄存器设置为数据表的首地址。
5. 将DAR寄存器设置为GPT320.GTCCRE寄存器的地址。
6. 将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(3) 三转信息集

设置传输到GPT320.GTPBR寄存器：

1. 在MRA寄存器中，选择源地址的增量（MRA.SM[1:0]位=10b）。
2. 将传输设置为正常传输模式（MRA.MD[1:0]位=00b）和字长传输（MRA.SZ[1:0]位=10b）。
3. 在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]位=00b）并设置每次中断的单次数据传输（MRB.CHNE位=0，MRB.DISEL位=0）。MRB.DTS位可以设置为任何值。
4. 将SAR寄存器设置为数据表的首地址。
5. 将DAR寄存器设置为GPT320.GTPBR寄存器的地址。
6. 将CRA寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(4) 转移信息分配

将用于传输到GPT320.GTPBR的传输信息放置在GPT320.GTCCRC和GPT320.GTCCRE寄存器中使用的传输控制信息之后。

(5) DTC向量表

在DTC向量表中，设置传输控制信息的地址，用于传输到GPT320.GTCCRC和GPT320.GTCCRE寄存器启动。

(6) ICU设置和DTC模块激活

1. 设置与GPT320计数器溢出中断相关的ICU.IELSRn.DTCE位。
2. 将ICU.IELSRn.IELS[7:0]设置为97(61h)用于GPT320计数器溢出。
3. 将DTCST.DTCST位设置为1。

(7) GPT settings

1. 设置GPT320.GTIOR寄存器，使GTCCRA和GTCCRB寄存器作为输出比较寄存器运行。
2. 在GPT320.GTCCRA和GPT320.GTCCRB寄存器中设置默认PWM定时器比较值，然后下一个PWM定时器比较GPT320.GTCCRC和GPT320.GTCCRE寄存器中的值。
3. 在GPT320.GTPR寄存器中设置默认PWM定时器周期值，在GPT320.GTPBR寄存器中设置下一个PWM定时器周期值。
4. 将PmnPFS.PDR中的输出位设置为1，并将PmnPFS.PSEL[4:0]中的外设选择位设置为00011b。

(8) GPT activation

将GPT320.GTSTR.CSTRT位设置为1以启动GPT320.GTCNT计数器。

(9) DTC transfer

每次使用GPT320.GTPR寄存器产生GPT320计数器溢出时，下一个PWM定时器比较值被传送到GPT320.GTCCRC和GPT320.GTCCRE寄存器。下一个PWM定时器周期的设置被传送到GPT320.GTPBR寄存器。

(10)中断处理

在指定轮次的数据传输完成后，例如当GPT传输的CRA寄存器中的值变为0时，会向CPU发出GPT320计数器溢出中断请求。在处理例程中完成该中断的处理。

18.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 128-KB input buffer, where the input buffer is set so that its lower address starts with 0000h. Figure 18.14 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   a. Transfer source address = fixed.
   b. CRA register = 0000h (65536) times.
   c. MRB.CHNE bit = 1 (chain transfer is enabled).
   d. MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   e. MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 65,536 times of the transfer destination address for the first data transfer in a different area such as the flash. For example, when setting the input buffer to 20 0000h to 21 FFFFh, prepare 21h and 20h.
3. For the second data transfer:
   f. Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   g. Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   h. Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   i. Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   j. When setting the input buffer to 20 0000h to 21 FFFFh, also set the transfer counter to 2.
4. The first data transfer is performed by an interrupt 65,536 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 21h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer is 0000h.
5. In succession, the first data transfer is performed by an interrupt 65,536 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 20h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer is 0000h.
6. Steps 4 and 5 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

18.6.3 Counter=0时的链式转移

仅当在第一次数据传输中将传输计数器设置为0时才执行第二次数据传输，并且在第二次传输中重复改变第一数据传输信息。链式转移使转移可以重复256次或更多。

以下过程显示了配置128KB输入缓冲区的示例，其中输入缓冲区设置为使其低地址以0000h开头。图18.14显示了当计数器=0时的链式传输。

1. 将正常传输模式设置为第一次数据传输的输入数据。设置以下内容：
   一个。传输源地址=固定。
   湾。CRA寄存器=0000h(65536)次。
   C。MRB.CHNE位=1（启用链式传输）。
   d。MRB.CHNS位=1（仅当传输计数器为0时才执行链式传输）。
   e.MRB.DISEL位=0（指定数据传输完成时向CPU产生中断请求）。
2. 在闪存等不同区域的第一次数据传输中，每65 536次传输目标地址准备起始地址的高8位地址。例如，将输入缓冲区设置为200000h到21FFFFh时，准备21h和20h。
3. 对于第二次数据传输：
   F。设置重复传输模式（以源为重复区域）重置第一次数据传输的传输目标地址。
   G。在传输目标的第一个传输信息区域中指定DAR寄存器的高8位。
   H。设置MRB.CHNE位=0（禁用链传输）。
   一世。设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   j.将输入缓冲区设置为200000h至21FFFFh时，还要将传输计数器设置为2。
4. 第一次数据传输由中断执行65 536次。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输目标地址的高8位设置为21h。第一次数据传输的传输目标地址和传输计数器的低16位为0000h。
5. 随后，第一次数据传输由中断执行65 536次，如为第一次数据传输指定的那样。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输目标地址的高8位设置为20h。第一次数据传输的传输目标地址和传输计数器的低16位为0000h。
6. 步骤4和5无限重复。因为第二次数据传输是重复传输模式，所以不会产生对CPU的中断请求。

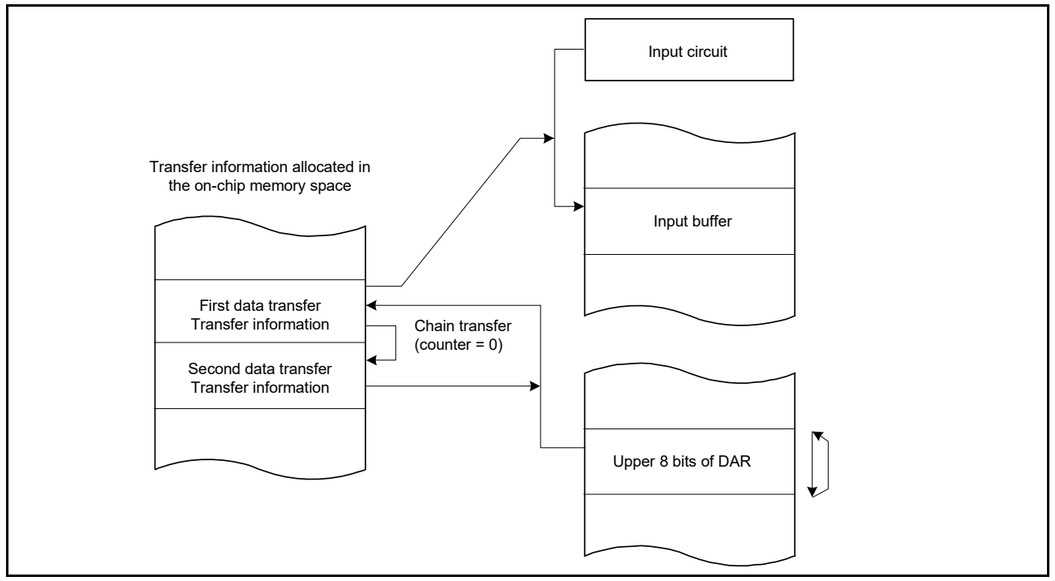


Figure 18.14 Chain transfer when counter = 0

18.7 Interrupt Source

When the DTC completes data transfer of the specified count or when data transfer with MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Interrupts to the CPU are controlled according to the settings in the NVIC and ICU.IELSRn.IELS[7:0]. See section 14, Interrupt Controller Unit (ICU).

The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

18.8 Event Link

The DTC can produce an event link request on completion of one transfer request.

18.9 Snooze Control Interface

To return to Software Standby mode from Snooze mode through the DTC, set SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 11.8.3, Return to Software Standby Mode.

SYSTEM.SNZEDCR.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion of CRA and CRB are 0.

SYSTEM.SNZEDCR.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion (CRA and CRB are not 0), detected on DTC transmission completion of CRA and CRB are not 0.

18.10 Module-Stop Function

Before transitioning to the module-stop function, Software Standby mode without Snooze mode transition, set the DTCST.DTCST bit to 0, and then perform the operations described in the following sections. The DTC is available in Snooze mode by setting SYSTEM.SNZCR.SNZDTCEN to 1. See section 11, Low Power Modes.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If the DTC transfer is in progress at the time, 1 is written to the MSTPCRA.MSTPA22 bit. The transition to the module-stop state proceeds after DTC transfer ends. While the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited. Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

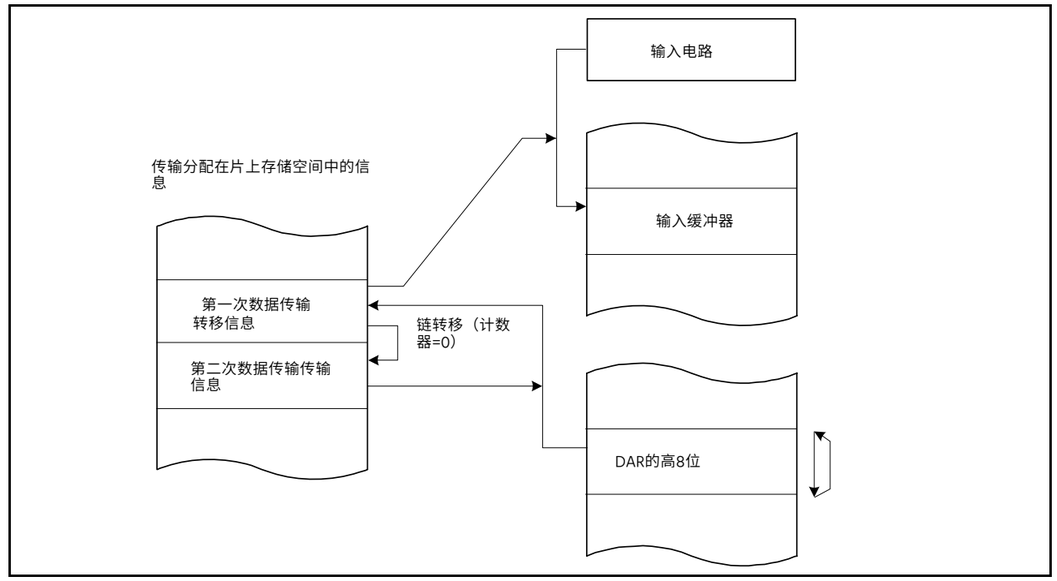


Figure 18.14 counter=0时的链转移

18.7 中断源

当DTC完成指定计数的数据传输或MRB.DISEL设置为1的数据传输完成时，DTC激活源向CPU生成中断。根据NVIC和ICU.IELSRn.IELS[7:0]中的设置控制对CPU的中断。参见第14节，中断控制器单元(ICU)。

DTC通过授予较小的中断向量编号较高的优先级来确定激活源的优先级。CPU中断的优先级由NVIC优先级决定。

18.8 活动链接

DTC可以在一个传输请求完成时产生一个事件链接请求。

18.9 贪睡控制界面

要通过DTC从贪睡模式返回到软件待机模式，请设置SYSTEM.SNZEDCR.DTCZRED或SYSTEM.SNZEDCR.DTCNZRED为1。请参见第11.8.3节，返回软件待机模式。

SYSTEM.SNZEDCR.DTCZRED在最后一次DTC传输完成时启用或禁用贪睡结束请求，在CRA和CRB的DTC传输完成时检测为0。

SYSTEM.SNZEDCR.DTCNZRED在非最后一个DTC传输完成（CRA和CRB不为0）时启用或禁用贪睡结束请求，在CRA和CRB不为0的DTC传输完成时检测到。

18.10 Module-Stop Function

在转换到模块停止功能之前，软件待机模式没有贪睡模式转换，设置DTCST.DTCST位为0，然后执行以下章节中描述的操作。DTC可用于通过将SYSTEM.SNZCR.SNZDTCEN设置为1来暂停模式。请参阅第11节，低功耗模式。

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DTC的模块停止功能。如果此时DTC传输正在进行，则将1写入MSTPCRA.MSTPA22位。在DTC传输结束后继续向模块停止状态的转换。当MSTPCRA.MSTPA22位为1时，禁止访问DTC寄存器。将0写入

MSTPCRA.MSTPA22位从模块停止状态释放DTC。

(2) Software Standby mode

Use the settings described in section 11.7.1, Transition to Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode follows the completion of the DTC transfer.

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 11.8.1, Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through the DTC, set the SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 11.8.3, Return to Software Standby Mode. The DTC activation request from the ICU is stopped during Software Standby mode but not during Snooze mode.

(3) Notes on the module-stop function

For the WFI instruction and the register setting procedure, see section 11, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 14.4.2, Selecting Interrupt Request Destinations, and then execute a WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

18.11 Usage Notes

18.11.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

(2) 软件待机模式

使用第11.7.1节，转换到软件待机模式中描述的设置。

如果在执行WFI指令时DTC传输操作正在进行，则在DTC传输完成之后转换到软件待机模式。

当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转入贪睡模式。请参阅第11.8.1节，过渡到贪睡模式。可以在SYSTEM.SNZCR.SNZDTCEN位中选择贪睡模式下的DTC操作。如果在贪睡模式下启用了DTC操作，则在转换到软件之前

待机模式，将DTCST.DTCST位设置为1。要通过DTC返回软件待机模式，请将SYSTEM.SNZEDCR.DTCZRED或SYSTEM.SNZEDCR.DTCNZRED为1。请参阅第11.8.3节，返回软件待机模式。来自ICU的DTC激活请求在软件待机模式期间停止，但在贪睡模式。

(3) 关于模块停止功能的注意事项

关于WFI指令和寄存器设置过程，请参见第11节，低功耗模式。

要在从低功耗模式返回后执行DTC传输而没有贪睡模式转换，请设置DTCST.DTCST位再次为1。

要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DTC激活请求，请按照第14.4.2节，选择中断请求目标中的说明将CPU指定为中断请求目标，然后执行WFI指令。如果在贪睡模式下启用DTC操作，请勿使用DTC的模块停止功能。

18.11 使用说明

18.11.1 传输信息起始地址

您必须为向量表中的传输信息起始地址设置4的倍数。否则，这些地址的最低2位被视为00b。

19. Event Link Controller (ELC)

19.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 19.1 lists the ELC specifications and Figure 19.1 shows a block diagram.

Table 19.1 ELC specifications

Parameter	Description
Event link function	135 types of event signals can be directly connected to modules.The ELC can generate an ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set

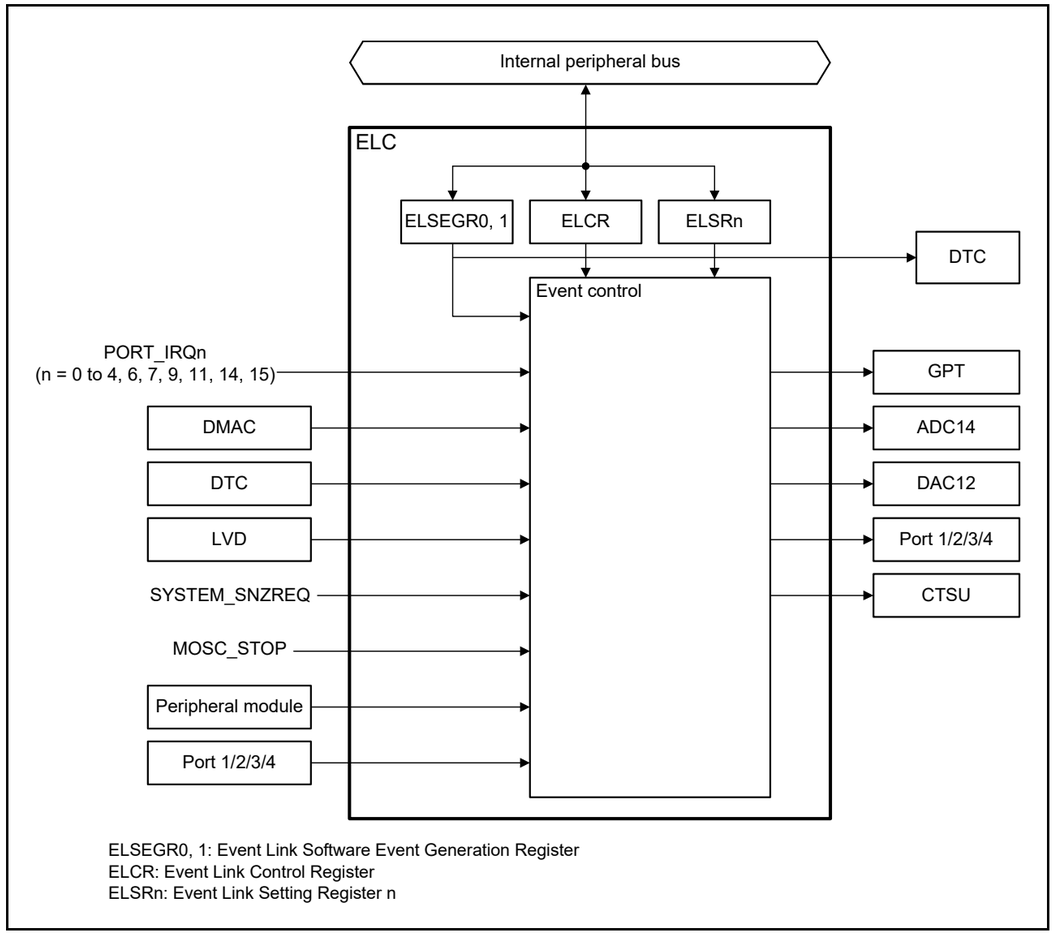


Figure 19.1 ELC block diagram (n = 0 to 9, 12, 14 to 18)

19. 事件链接控制器(ELC)

19.1 Overview

EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。

表19.1列出了ELC规范，图19.1显示了框图。

Table 19.1 ELC specifications

Parameter	Description
事件链接功能	135种事件信号可以直接连接到模块。ELC可以产生ELC事件信号，以及激活DTC的事件。
Module-stop function	模块停止状态可设置

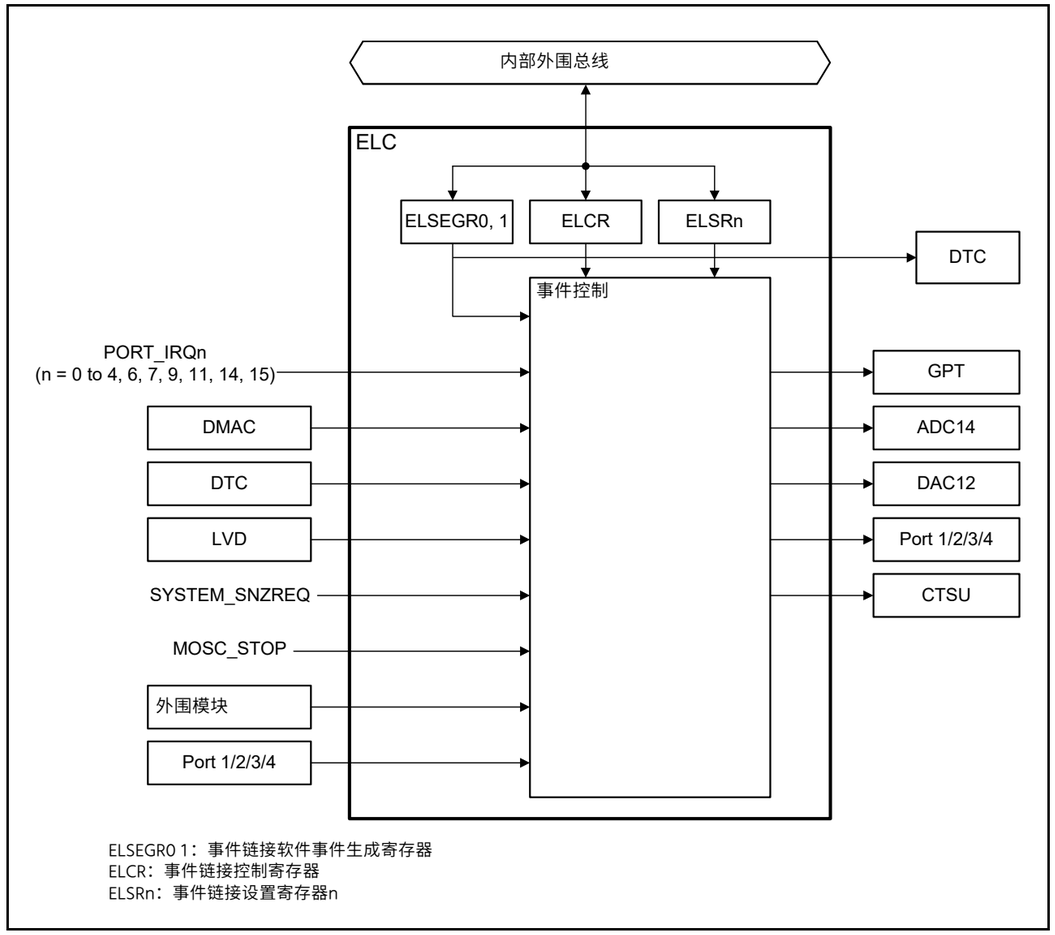


Figure 19.1 ELC框图（n=0到9、12、14到18）

19.2 Register Descriptions

19.2.1 Event Link Controller Register (ELCR)

Address(es): ELC.ELCR 4004 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ELCON	All Event Link Enable	0: ELC function disabled 1: ELC function enabled.	R/W

The ELCR register controls the ELC operation.

19.2.2 Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1)

Address(es): ELC.ELSEGR0 4004 1002h, ELC.ELSEGR1 4004 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEG	Software Event Generation	0: Normal operation 1: Software event is generated.	W
b5 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	WE	SEG Bit Write Enable	0: Write to SEG bit disabled 1: Write to SEG bit enabled.	R/W
b7	WI	ELSEGR Register Write Disable	0: Write to ELSEGR register enabled 1: Write to ELSEGR register disabled.	W

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

19.2 注册说明

19.2.1 事件链接控制器寄存器(ELCR)

Address(es): ELC.ELCR 4004 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	ELCON	所有事件链接启用	0：ELC功能禁用1：ELC 功能启用。	R/W

ELCR寄存器控制ELC操作。

19.2.2 事件链接软件事件生成寄存器n(ELSEGRn)(n=0 1)

Address(es): ELC.ELSEGR0 4004 1002h, ELC.ELSEGR1 4004 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SEG	软件事件生成	0：正常操作1：产生软件事件 。	W
b5 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	WE	SEG位写使能	0：禁止写入SEG位1：允许 写入SEG位。	R/W
b7	WI	ELSEGR寄存器写入禁用	0：允许写入ELSEGR寄存器1：禁止写 入ELSEGR寄存器。	W

SEG位（软件事件生成）

当WE位为1时向SEG位写入1时，将产生软件事件。该位被读取为0。即使向该位写入1，也不存储数据。在写入该位之前，WE位必须设置为1。

软件事件可以触发链接的DTC事件。

WE位（SEG位写使能）

SEG位只能在WE位为1时写入。在写入该位之前将WI位清零。

[Setting condition]

- 如果在WI位为0时向该位写入1，则该位变为1。

[Clearing condition]

- 如果在WI位为0时向该位写入0，则该位变为0。

WI位（ELSEGR寄存器写禁止）

只有当WI位的写入值为0时，才能写入ELSEGR寄存器。该位读为1。在设置WE或SEG位之前，必须将WI位设置为0。

19.2.3 Event Link Setting Register n (ELSRn) (n = 0 to 9, 12, 14 to 18)

Address(es): ELC.ELSR0 4004 1010h, ELC.ELSR1 4004 1014h, ELC.ELSR2 4004 1018h, ELC.ELSR3 4004 101Ch, ELC.ELSR4 4004 1020h, ELC.ELSR5 4004 1024h, ELC.ELSR6 4004 1028h, ELC.ELSR7 4004 102Ch, ELC.ELSR8 4004 1030h, ELC.ELSR9 4004 1034h, ELC.ELSR12 4004 1040h, ELC.ELSR14 4004 1048h, ELC.ELSR15 4004 104Ch, ELC.ELSR16 4004 1050h, ELC.ELSR17 4004 1054h, ELC.ELSR18 4004 1058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ELS[7:0]	Event Link Select	b7 b0 00000000:Event output disabled for the associated peripheral module 00000001 to 11010100: Number setting for the event signal to be linked. Other settings are prohibited.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 19.2 shows the association between the ELSRn registers and the peripheral modules. Table 19.3 shows the association between the event signal names set in the ELSRn registers and the signal numbers.

Table 19.2 Association between the ELSRn registers and peripheral functions

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC14A	ELC_AD00
ELSR9	ADC14B	ELC_AD01
ELSR12	DAC12	ELC_DA0
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4
ELSR18	CTSU	ELC_CTSU

19.2.3 事件链接设置寄存器n(ELSRn)(n=0到9、12、14到18)

Address(es): ELC.ELSR0 4004 1010h, ELC.ELSR1 4004 1014h, ELC.ELSR2 4004 1018h, ELC.ELSR3 4004 101Ch, ELC.ELSR4 4004 1020h, ELC.ELSR5 4004 1024h, ELC.ELSR6 4004 1028h, ELC.ELSR7 4004 102Ch, ELC.ELSR8 4004 1030h, ELC.ELSR9 4004 1034h, ELC.ELSR12 4004 1040h, ELC.ELSR14 4004 1048h, ELC.ELSR15 4004 104Ch, ELC.ELSR16 4004 1050h, ELC.ELSR17 4004 1054h, ELC.ELSR18 4004 1058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ELS[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ELS[7:0]	活动链接选择	b7b000000000：相关外围模块的事件输出禁用00000001至11010100：要链接的事件信号的编号设置。禁止其他设置。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ELSRn寄存器指定要链接到每个外围模块的事件信号。表19.2显示了ELSRn寄存器和外设模块之间的关联。表19.3显示了在ELSRn寄存器中设置的事件信号名称和信号编号之间的关联。

Table 19.2 ELSRn寄存器和外设功能之间的关联

注册名称	外设功能（模块）	活动名称
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC14A	ELC_AD00
ELSR9	ADC14B	ELC_AD01
ELSR12	DAC12	ELC_DA0
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4
ELSR18	CTSU	ELC_CTSU

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (1 of 4)

Event number	Interrupt request source	Name	Description
001h	Port	PORT_IRQ0*1	External pin interrupt 0
002h		PORT_IRQ1*1	External pin interrupt 1
003h		PORT_IRQ2*1	External pin interrupt 2
004h		PORT_IRQ3*1	External pin interrupt 3
005h		PORT_IRQ4*1	External pin interrupt 4
007h		PORT_IRQ6*1	External pin interrupt 6
008h		PORT_IRQ7*1	External pin interrupt 7
00Ah		PORT_IRQ9*1	External pin interrupt 9
00Ch		PORT_IRQ11*1	External pin interrupt 11
00Fh		PORT_IRQ14*1	External pin interrupt 14
010h		PORT_IRQ15*1	External pin interrupt 15
011h	DMAC0	DMAC0_INT	DMAC transfer end 0
012h	DMAC1	DMAC1_INT	DMAC transfer end 1
013h	DMAC2	DMAC2_INT	DMAC transfer end 2
014h	DMAC3	DMAC3_INT	DMAC transfer end 3
016h	DTC	DTC_DTCEND*3	DTC transfer end
019h	LVD	LVD_LVD1	Voltage monitor 1 interrupt
01Ch	MOSC	MOSC_STOP	Main clock oscillation stop
01Dh	Low power mode	SYSTEM_SNZREQ*2, *3	Snooze entry
01Eh	AGT0	AGT0_AGTI	AGT interrupt
01Fh		AGT0_AGTCMAI	Compare match A
020h		AGT0_AGTCMBI	Compare match B
021h	AGT1	AGT1_AGTI	AGT interrupt
022h		AGT1_AGTCMAI	Compare match A
023h		AGT1_AGTCMBI	Compare match B
024h	IWDT	IWDT_NMIUNDF	IWDT underflow
025h	WDT	WDT_NMIUNDF	WDT underflow
027h	RTC	RTC_PRD	Periodic interrupt
029h	ADC140	ADC140_ADI	A/D scan end interrupt
02Dh		ADC140_WCMPM*3	Compare match
02Eh		ADC140_WCMPUM*3	Compare mismatch
02Fh	ACMPLP	ACMP_LP0	Low-power analog comparator interrupt 0
030h		ACMP_LP1	Low-power analog comparator interrupt 1
035h	IIC0	IIC0_RXI	Receive data full
036h		IIC0_TXI	Transmit data empty
037h		IIC0_TEI	Transmit end
038h		IIC0_EEI	Transfer error
03Ah	IIC1	IIC1_RXI	Receive data full
03Bh		IIC1_TXI	Transmit data empty
03Ch		IIC1_TEI	Transmit end
03Dh		IIC1_EEI	Transfer error
04Ah	DOC	DOC_DOPCI*3	Data operation circuit interrupt

Table 19.3 在ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（1of4）

事件编号	中断请求源	Name	Description
001h	Port	PORT_IRQ0*1	外部引脚中断0
002h		PORT_IRQ1*1	外部引脚中断1
003h		PORT_IRQ2*1	外部引脚中断2
004h		PORT_IRQ3*1	外部引脚中断3
005h		PORT_IRQ4*1	外部引脚中断4
007h		PORT_IRQ6*1	外部引脚中断6
008h		PORT_IRQ7*1	外部引脚中断7
00Ah		PORT_IRQ9*1	外部引脚中断9
00Ch		PORT_IRQ11*1	外部引脚中断11
00Fh		PORT_IRQ14*1	外部引脚中断14
010h		PORT_IRQ15*1	外部引脚中断15
011h	DMAC0	DMAC0_INT	DMAC传输结束0
012h	DMAC1	DMAC1_INT	DMAC传输结束1
013h	DMAC2	DMAC2_INT	DMAC传输结束2
014h	DMAC3	DMAC3_INT	DMAC传输结束3
016h	DTC	DTC_DTCEND*3	DTC传输结束
019h	LVD	LVD_LVD1	电压监视器1中断
01Ch	MOSC	MOSC_STOP	主时钟振荡停止
01Dh	低功耗模式	SYSTEM_SNZREQ*2, *3	贪睡进入
01Eh	AGT0	AGT0_AGTI	AGT interrupt
01Fh		AGT0_AGTCMAI	比较匹配A
020h		AGT0_AGTCMBI	比较匹配B
021h	AGT1	AGT1_AGTI	AGT interrupt
022h		AGT1_AGTCMAI	比较匹配A
023h		AGT1_AGTCMBI	比较匹配B
024h	IWDT	IWDT_NMIUNDF	IWDT underflow
025h	WDT	WDT_NMIUNDF	WDT underflow
027h	RTC	RTC_PRD	周期性中断
029h	ADC140	ADC140_ADI	AD扫描结束中断
02Dh		ADC140_WCMPM*3	比较匹配
02Eh		ADC140_WCMPUM*3	比较不匹配
02Fh	ACMPLP	ACMP_LP0	低功耗模拟比较器中断0
030h		ACMP_LP1	低功耗模拟比较器中断1
035h	IIC0	IIC0_RXI	接收数据已满
036h		IIC0_TXI	传输数据为空
037h		IIC0_TEI	发射端
038h		IIC0_EEI	传输错误
03Ah	IIC1	IIC1_RXI	接收数据已满
03Bh		IIC1_TXI	传输数据为空
03Ch		IIC1_TEI	发射端
03Dh		IIC1_EEI	传输错误
04Ah	DOC	DOC_DOPCI*3	数据运算电路中断

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (2 of 4)

Event number	Interrupt request source	Name	Description
053h	I/O port	IOPORT_GROUP1	Port 1 event
054h		IOPORT_GROUP2	Port 2 event
055h		IOPORT_GROUP3	Port 3 event
056h		IOPORT_GROUP4	Port 4 event
057h	ELC	ELC_SWEVT0	Software event 0
058h		ELC_SWEVT1	Software event 1
05Bh	GPT320	GPT0_CCMPA	Compare match A
05Ch		GPT0_CCMPB	Compare match B
05Dh		GPT0_CMPC	Compare match C
05Eh		GPT0_CMPD	Compare match D
05Fh		GPT0_CMPE	Compare match E
060h		GPT0_CMPF	Compare match F
061h		GPT0_OVF	Overflow
062h		GPT0_UDF	Underflow
063h	GPT321	GPT1_CCMPA	Compare match A
064h		GPT1_CCMPB	Compare match B
065h		GPT1_CMPC	Compare match C
066h		GPT1_CMPD	Compare match D
067h		GPT1_CMPE	Compare match E
068h		GPT1_CMPF	Compare match F
069h		GPT1_OVF	Overflow
06Ah		GPT1_UDF	Underflow
06Bh	GPT322	GPT2_CCMPA	Compare match A
06Ch		GPT2_CCMPB	Compare match B
06Dh		GPT2_CMPC	Compare match C
06Eh		GPT2_CMPD	Compare match D
06Fh		GPT2_CMPE	Compare match E
070h		GPT2_CMPF	Compare match F
071h		GPT2_OVF	Overflow
072h		GPT2_UDF	Underflow
073h	GPT323	GPT3_CCMPA	Compare match A
074h		GPT3_CCMPB	Compare match B
075h		GPT3_CMPC	Compare match C
076h		GPT3_CMPD	Compare match D
077h		GPT3_CMPE	Compare match E
078h		GPT3_CMPF	Compare match F
079h		GPT3_OVF	Overflow
07Ah		GPT3_UDF	Underflow

Table 19.3 在ELSRn.ELS位中设置的事件信号名称和信号编号之间的关联（2of4）

事件编号	中断请求源	Name	Description
053h	I/O port	IOPORT_GROUP1	端口1事件
054h		IOPORT_GROUP2	端口2事件
055h		IOPORT_GROUP3	端口3事件
056h		IOPORT_GROUP4	端口4事件
057h	ELC	ELC_SWEVT0	软件事件0
058h		ELC_SWEVT1	软件事件1
05Bh	GPT320	GPT0_CCMPA	比较匹配A
05Ch		GPT0_CCMPB	比较匹配B
05Dh		GPT0_CMPC	比较匹配C
05Eh		GPT0_CMPD	比较匹配D
05Fh		GPT0_CMPE	比较匹配E
060h		GPT0_CMPF	比较匹配F
061h		GPT0_OVF	Overflow
062h		GPT0_UDF	Underflow
063h	GPT321	GPT1_CCMPA	比较匹配A
064h		GPT1_CCMPB	比较匹配B
065h		GPT1_CMPC	比较匹配C
066h		GPT1_CMPD	比较匹配D
067h		GPT1_CMPE	比较匹配E
068h		GPT1_CMPF	比较匹配F
069h		GPT1_OVF	Overflow
06Ah		GPT1_UDF	Underflow
06Bh	GPT322	GPT2_CCMPA	比较匹配A
06Ch		GPT2_CCMPB	比较匹配B
06Dh		GPT2_CMPC	比较匹配C
06Eh		GPT2_CMPD	比较匹配D
06Fh		GPT2_CMPE	比较匹配E
070h		GPT2_CMPF	比较匹配F
071h		GPT2_OVF	Overflow
072h		GPT2_UDF	Underflow
073h	GPT323	GPT3_CCMPA	比较匹配A
074h		GPT3_CCMPB	比较匹配B
075h		GPT3_CMPC	比较匹配C
076h		GPT3_CMPD	比较匹配D
077h		GPT3_CMPE	比较匹配E
078h		GPT3_CMPF	比较匹配F
079h		GPT3_OVF	Overflow
07Ah		GPT3_UDF	Underflow

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (3 of 4)

Event number	Interrupt request source	Name	Description
07Bh	GPT164	GPT4_CCMPA	Compare match A
07Ch		GPT4_CCMPB	Compare match B
07Dh		GPT4_CMPC	Compare match C
07Eh		GPT4_CMPD	Compare match D
07Fh		GPT4_CMPE	Compare match E
080h		GPT4_CMPF	Compare match F
081h		GPT4_OVF	Overflow
082h		GPT4_UDF	Underflow
083h	GPT165	GPT5_CCMPA	Compare match A
084h		GPT5_CCMPB	Compare match B
085h		GPT5_CMPC	Compare match C
086h		GPT5_CMPD	Compare match D
087h		GPT5_CMPE	Compare match E
088h		GPT5_CMPF	Compare match F
089h		GPT5_OVF	Overflow
08Ah		GPT5_UDF	Underflow
09Bh	GPT168	GPT8_CCMPA	Compare match A
09Ch		GPT8_CCMPB	Compare match B
09Dh		GPT8_CMPC	Compare match C
09Eh		GPT8_CMPD	Compare match D
09Fh		GPT8_CMPE	Compare match E
0A0h		GPT8_CMPF	Compare match F
0A1h		GPT8_OVF	Overflow
0A2h		GPT8_UDF	Underflow
0ABh	GPT	GPT_UVWEDGE	UVW edge event
0ACh	SCI0	SCI0_RXI*4	Receive data full
0ADh		SCI0_TXI*4	Transmit data empty
0AEh		SCI0_TEI	Transmit end
0AFh		SCI0_ERI*4	Receive error
0B0h		SCI0_AM	Address match event
0B2h	SCI1	SCI1_RXI*4	Receive data full
0B3h		SCI1_TXI*4	Transmit data empty
0B4h		SCI1_TEI	Transmit end
0B5h		SCI1_ERI*4	Receive error
0B6h		SCI1_AM	Address match event
0C1h	SCI4	SCI4_RXI*4	Receive data full
0C2h		SCI4_TXI*4	Transmit data empty
0C3h		SCI4_TEI	Transmit end
0C4h		SCI4_ERI*4	Receive error
0C5h		SCI4_AM	Address match event
0C6h	SCI9	SCI9_RXI*4	Receive data full
0C7h		SCI9_TXI*4	Transmit data empty
0C8h		SCI9_TEI	Transmit end
0C9h		SCI9_ERI*4	Receive error
0CAh		SCI9_AM	Address match event

Table 19.3 ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（3of4）

事件编号	中断请求源	Name	Description
07Bh	GPT164	GPT4_CCMPA	比较匹配A
07Ch		GPT4_CCMPB	比较匹配B
07Dh		GPT4_CMPC	比较匹配C
07Eh		GPT4_CMPD	比较匹配D
07Fh		GPT4_CMPE	比较匹配E
080h		GPT4_CMPF	比较匹配F
081h		GPT4_OVF	Overflow
082h		GPT4_UDF	Underflow
083h	GPT165	GPT5_CCMPA	比较匹配A
084h		GPT5_CCMPB	比较匹配B
085h		GPT5_CMPC	比较匹配C
086h		GPT5_CMPD	比较匹配D
087h		GPT5_CMPE	比较匹配E
088h		GPT5_CMPF	比较匹配F
089h		GPT5_OVF	Overflow
08Ah		GPT5_UDF	Underflow
09Bh	GPT168	GPT8_CCMPA	比较匹配A
09Ch		GPT8_CCMPB	比较匹配B
09Dh		GPT8_CMPC	比较匹配C
09Eh		GPT8_CMPD	比较匹配D
09Fh		GPT8_CMPE	比较匹配E
0A0h		GPT8_CMPF	比较匹配F
0A1h		GPT8_OVF	Overflow
0A2h		GPT8_UDF	Underflow
0ABh	GPT	GPT_UVWEDGE	UVW边缘事件
0ACh	SCI0	SCI0_RXI*4	接收数据已满
0ADh		SCI0_TXI*4	传输数据为空
0AEh		SCI0_TEI	发射端
0AFh		SCI0_ERI*4	接收错误
0B0h		SCI0_AM	地址匹配事件
0B2h	SCI1	SCI1_RXI*4	接收数据已满
0B3h		SCI1_TXI*4	传输数据为空
0B4h		SCI1_TEI	发射端
0B5h		SCI1_ERI*4	接收错误
0B6h		SCI1_AM	地址匹配事件
0C1h	SCI4	SCI4_RXI*4	接收数据已满
0C2h		SCI4_TXI*4	传输数据为空
0C3h		SCI4_TEI	发射端
0C4h		SCI4_ERI*4	接收错误
0C5h		SCI4_AM	地址匹配事件
0C6h	SCI9	SCI9_RXI*4	接收数据已满
0C7h		SCI9_TXI*4	传输数据为空
0C8h		SCI9_TEI	发射端
0C9h		SCI9_ERI*4	接收错误
0CAh		SCI9_AM	地址匹配事件

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (4 of 4)

Event number	Interrupt request source	Name	Description
0CBh	SPI0	SPI0_SPRI	Receive buffer full
0CCh		SPI0_SPTI	Transmit buffer empty
0CDh		SPI0_SPII	Idle
0CEh		SPI0_SPEI	Error
0CFh		SPI0_SPTEND	Transmission completed event
0D0h	SPI1	SPI1_SPRI	Receive buffer full
0D1h		SPI1_SPTI	Transmit buffer empty
0D2h		SPI1_SPII	Idle
0D3h		SPI1_SPEI	Error
0D4h		SPI1_SPTEND	Transmission completed event

Note 1. Only pulse (edge detection) is supported.
Note 2. ELSR8, 9, and ELSR14 to ELSR18 can select this event.
Note 3. This event can occur in Snooze Mode.
Note 4. This event is not supported in FIFO mode.

19.3 Operation

19.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

19.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 19.4 lists the operations of modules when an event occurs.

Table 19.4 Module operations when event occurs

Module	Operations when event occurs
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture.
ADC14	Starts A/D conversion
DAC12	Starts D/A conversion
I/O ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT 1 PORT 2 PORT 3 PORT 4.
CTSU	Starts measurement operation
DTC	Starts DTC data transfer

19.3.3 Example of Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn register for the module to be linked.

Table 19.3 在ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（4个，共4个）

事件编号	中断请求源	Name	Description
0CBh	SPI0	SPI0_SPRI	接收缓冲区已满
0CCh		SPI0_SPTI	发送缓冲区为空
0CDh		SPI0_SPII	Idle
0CEh		SPI0_SPEI	Error
0CFh		SPI0_SPTEND	传输完成事件
0D0h	SPI1	SPI1_SPRI	接收缓冲区已满
0D1h		SPI1_SPTI	发送缓冲区为空
0D2h		SPI1_SPII	Idle
0D3h		SPI1_SPEI	Error
0D4h		SPI1_SPTEND	传输完成事件

Note 1. 仅支持脉冲（边缘检测）。
Note 2. ELSR8、9和ELSR14到ELSR18可以选择此事件。
Note 3. 此事件可能在贪睡模式下发生。
Note 4. FIFO模式不支持此事件。

19.3 Operation

19.3.1 中断处理和事件链接的关系

事件链接的事件编号与关联中断源的事件编号相同。有关生成事件信号的信息，请参阅每个事件源模块的章节中的说明。

19.3.2 链接事件

当事件发生并且该事件已在事件链接设置寄存器(ELSRn)中设置为触发器时，将激活相关模块。模块的操作必须提前设置好。表19.4列出了事件发生时模块的操作。

Table 19.4 事件发生时的模块操作

Module	事件发生时的操作
GPT	开始计数 停止计数 清除计数 递增计数 递减计数 输入捕获。
ADC14	开始AD转换
DAC12	开始DA转换
I/O ports	根据EORR（复位）或EOSR（设置）更改引脚输出 将引脚状态锁定为EIDR 以下端口可用于ELC：PORT1PORT2PORT3PORT4。
CTSU	开始测量操作
DTC	开始DTC数据传输

19.3.3 链接事件的过程示例

链接事件：

1. 设置要链接事件的模块的操作。
2. 为要链接的模块设置适当的ELSRn寄存器。

3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 000000000b in the ELSRn.ELS[7:0] bits associated with the modules. To stop linkage of all events, set the ELCR.ELCON bit to 0.

If the event link output from the RTC is to be used, set the ELC after the RTC, for example, initialization and time setting. Unintended events can be generated if the RTC settings are made after the ELC settings.

19.4 Usage Notes

19.4.1 Linking DMAC or DTC Transfer End Signals as Events

When linking the DMAC or DTC transfer end signals as events, do not set the same peripheral module as the DMAC or DTC transfer destination and event link destination. If set, the peripheral module might be started before DMAC or DTC transfer to the peripheral module is complete.

19.4.2 Setting Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in low power modes in which the module is stopped (Software Standby mode). Some modules can perform in Snooze mode. For more information, see Table 19.3 and section 11, Low Power Modes.

19.4.3 Module-Stop Function Setting

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register. For more information, see section 11, Low Power Modes.

19.4.4 ELC Delay Time

In Figure 19.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. The ELC delay time is shown in Table 19.5.

If the clock domains on both module A and B are the same, the delay time is 0. But, if the clock domains on modules A and B are different, the ELC module has some delays. The time delay is defined by the slower clock frequency between module A and module B clocks.

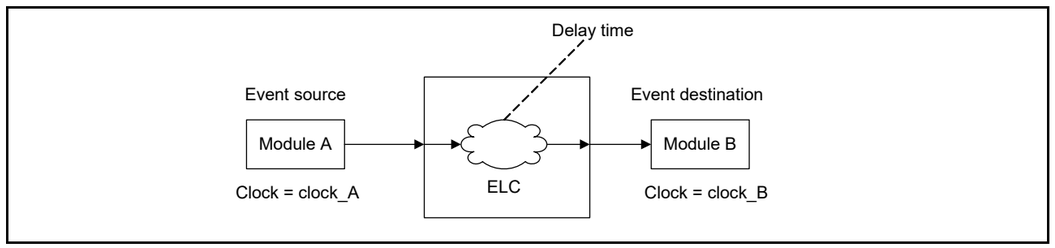


Figure 19.2 ELC delay time

Table 19.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of B
	clock_A < clock_B	1 cycle to 2 cycles of A

3. 将ELCR.ELCON位设置为1以启用所有事件的链接。
4. 配置输出事件的模块并激活该模块。两个模块之间的链接现在处于活动状态。
5. 要单独停止模块的事件链接，请在与模块关联的ELSRn.ELS[7:0]位中设置000000000b。要停止所有事件的链接，请将ELCR.ELCON位设置为0。

如果要使用RTC的事件链接输出，请在RTC之后设置ELC，例如初始化和时间设置。如果在ELC设置之后进行RTC设置，则可能会生成意外事件。

19.4 使用说明

19.4.1 将DMAC或DTC传输结束信号作为事件链接

将DMAC或DTC传输结束信号作为事件链接时，请勿将外设模块设置为DMAC或DTC传输目标和事件链接目标。如果设置，则外围模块可能会在DMAC或DTC传输到外围模块完成之前启动。

19.4.2 设置时钟

要链接事件，您必须启用ELC和相关模块。如果相关模块处于模块停止状态或模块停止的低功耗模式（软件待机模式），则模块无法运行。某些模块可以在贪睡模式下执行。有关详细信息，请参阅表19.3和第11节，低功耗模式。

19.4.3 模块停止功能设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用ELC操作。ELC在复位后最初停止。释放模块停止状态可以访问寄存器。在使用模块停止控制寄存器禁用ELC操作之前，必须将ELCON位设置为0。有关详细信息，请参阅第11节，低功耗模式。

19.4.4 ELC延迟时间

在图19.2中，模块A通过ELC访问模块B。模块A和模块B之间的ELC存在延迟时间。ELC延迟时间如表19.5所示。

如果模块A和B上的时钟域相同，则延迟时间为0。但是，如果模块A和B上的时钟域不同，则ELC模块有一些延迟。时间延迟由模块A和模块B时钟之间较慢的时钟频率定义。

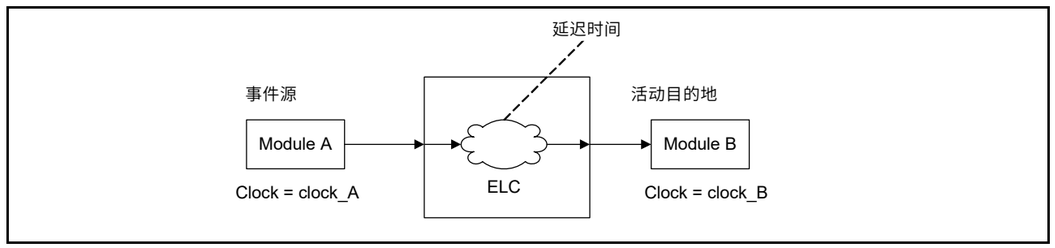


Figure 19.2 ELC延迟时间

Table 19.5 ELC延迟时间

时钟域	时钟频率	ELC延迟时间
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1个周期到2个周期
	clock_A > clock_B	B的1个周期到2个周期
	clock_A < clock_B	A的1个周期到2个周期

20. I/O Ports

20.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for ELC, or bus control pins. All pins operate as input pins immediately after a reset, and pin functions are switched by register settings. The I/O ports and peripheral modules for each pin are specified in the associated registers.

Figure 20.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs depending on the package. Table 20.1 shows the I/O port specifications, and Table 20.2 lists the port functions.

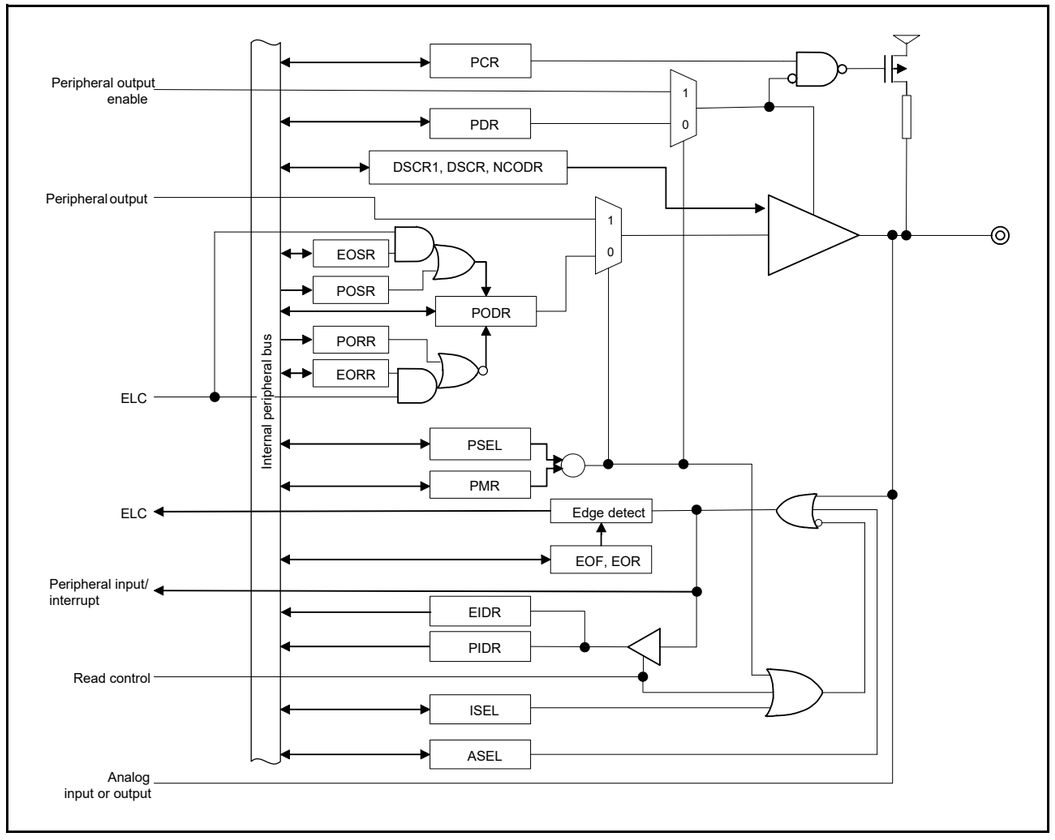


Figure 20.1 Connection diagram for I/O port registers

Note: Figure 20.1 shows a basic port configuration. The configuration differs depending on the ports.

Table 20.1 I/O port specifications (1 of 2)

Port	Port name	Number of pins
PORT0	P004, P010, P011, P014, P015	5
PORT1	P100 to P111	12
PORT2	P200, P201, P204 to P206, P212 to P215	9
PORT3	P300	1
PORT4	P402, P404, P407, P409, P414	5

20. I/O Ports

20.1 Overview

IO端口引脚用作通用IO端口引脚、外围模块的IO引脚、中断输入引脚、模拟IO、ELC的端口组功能或总线控制引脚。所有引脚在复位后立即作为输入引脚工作，引脚功能通过寄存器设置进行切换。每个引脚的IO端口和外围模块在相关寄存器中指定。

图20.1显示了IO端口寄存器的连接图。IO端口的配置因封装而异。表20.1显示了IO端口规格，表20.2列出了端口功能。

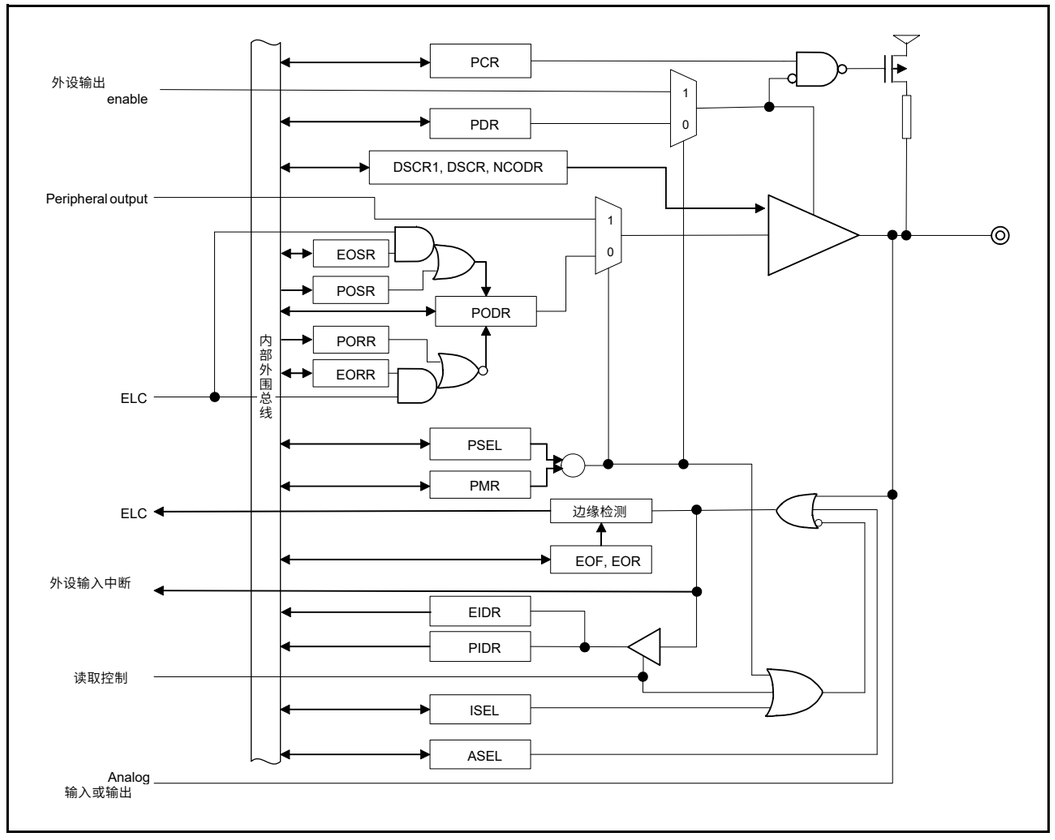


Figure 20.1 IO端口寄存器的连接图

Note: 图20.1显示了一个基本的端口配置。配置因端口而异。

Table 20.1 IO端口规格(1of2)

Port	端口名称	引脚数
PORT0	P004, P010, P011, P014, P015	5
PORT1	P100 to P111	12
PORT2	P200, P201, P204 to P206, P212 to P215	9
PORT3	P300	1
PORT4	P402, P404, P407, P409, P414	5

Table 20.1 I/O port specifications (2 of 2)

Port	Port name	Number of pins
PORT5	P501	1
PORT9	P914, P915	2

✓: available

Table 20.2 I/O port functions

Port	Port name	Input pull-up	Open-drain output	Drive capacity switch	5 V tolerant
PORT0	P004, P010, P011, P014, P015	✓	-	Low, middle	-
PORT1	P100 to P111	✓	✓	Low, middle	-
PORT2	P200, P214, P215	-	-	-	-
	P201, P204	✓	✓	Low, middle	-
	P205, P206	✓	✓	Low, middle	✓
	P212, P213	✓	✓	-	-
PORT3	P300	✓	✓	Low, middle	-
PORT4	P402, P407	✓	✓	Low, middle	✓
	P404, P409, P414	✓	✓	Low, middle	-
PORT5	P501	✓	✓	Low, middle	-
PORT9	P914, P915	-	-	-	-

✓: available

20.2 Register Descriptions

20.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

Address(es): PORT0.PCNTR1 4004 0000h, PORT1.PCNTR1 4004 0020h, PORT2.PCNTR1 4004 0040h, PORT3.PCNTR1 4004 0060h, PORT4.PCNTR1 4004 0080h, PORT5.PCNTR1 4004 00A0h, PORT9.PCNTR1 4004 0120h,

PORT0.PODR 4004 0000h, PORT1.PODR 4004 0020h, PORT2.PODR 4004 0040h, PORT3.PODR 4004 0060h, PORT4.PODR 4004 0080h, PORT5.PODR 4004 00A0h, PORT9.PODR 4004 0120h,

PORT0.PDR 4004 0002h, PORT1.PDR 4004 0022h, PORT2.PDR 4004 0042h, PORT3.PDR 4004 0062h, PORT4.PDR 4004 0082h, PORT5.PDR 4004 00A2h, PORT9.PDR 4004 0122h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PODR 15	PODR 14	PODR 13	PODR 12	PODR 11	PODR 10	PODR 09	PODR 08	PODR 07	PODR 06	PODR 05	PODR 04	PODR 03	PODR 02	PODR 01	PODR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PDRn	Pmn Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b31 to b16	PODRn	Pmn Output Data	0: Low output 1: High output.	R/W

m = 0 to 5, 9
n = 00 to 15

Table 20.1 IO端口规格(2of2)

Port	端口名称	引脚数
PORT5	P501	1
PORT9	P914, P915	2

✓: available

Table 20.2 IO口功能

Port	端口名称	Input pull-up	Open-drain output	驱动容量开关	5 V tolerant
PORT0	P004, P010, P011, P014, P015	✓	-	低、中	-
PORT1	P100 to P111	✓	✓	低、中	-
PORT2	P200, P214, P215	-	-	-	-
	P201, P204	✓	✓	低、中	-
	P205, P206	✓	✓	低、中	✓
	P212, P213	✓	✓	-	-
PORT3	P300	✓	✓	低、中	-
PORT4	P402, P407	✓	✓	低、中	✓
	P404, P409, P414	✓	✓	低、中	-
PORT5	P501	✓	✓	低、中	-
PORT9	P914, P915	-	-	-	-

✓: available

20.2 注册说明

20.2.1 端口控制寄存器1(PCNTR1PODRPDR)

Address(es): PORT0.PCNTR1 4004 0000h, PORT1.PCNTR1 4004 0020h, PORT2.PCNTR1 4004 0040h, PORT3.PCNTR1 4004 0060h, PORT4.PCNTR1 4004 0080h, PORT5.PCNTR1 4004 00A0h, PORT9.PCNTR1 4004 0120h,

PORT0.PODR 4004 0000h, PORT1.PODR 4004 0020h, PORT2.PODR 4004 0040h, PORT3.PODR 4004 0060h, PORT4.PODR 4004 0080h, PORT5.PODR 4004 00A0h, PORT9.PODR 4004 0120h,

PORT0.PDR 4004 0002h, PORT1.PDR 4004 0022h, PORT2.PDR 4004 0042h, PORT3.PDR 4004 0062h, PORT4.PDR 4004 0082h, PORT5.PDR 4004 00A2h, PORT9.PDR 4004 0122h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PODR 15	PODR 14	PODR 13	PODR 12	PODR 11	PODR 10	PODR 09	PODR 08	PODR 07	PODR 06	PODR 05	PODR 04	PODR 03	PODR 02	PODR 01	PODR 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	PDRn	Pmn Direction	0：输入（用作输入引脚）1：输出（用作输出引脚）。	R/W
b31 to b16	PODRn	Pmn输出数据	0：低输出1：高输出。	R/W

m = 0 to 5, 9
n = 00 to 15

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit and 16-bit read/write register that controls the port direction and port output data.

The PCNTR1 specifies the port direction and output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0. P200, P214, and P215 are input only, so PORT2.PCNTR1.PDR00, PORT2.PCNTR1.PDR14, and PORT2.PCNTR1.PDR15 are reserved. The PDRn bit in the PORTm.PCNTR1 register serve the same function as the PDR bit in the PFS.PmnPFS register.

The PODRn bits hold data to be output from the general I/O pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0. P200, P214, P215 are input only, so PORT2.PCNTR1.PODR00, PORT2.PCNTR1.PODR14, and PORT2.PCNTR1.PODR15 bits are reserved. A reserved bit is read as 0. The write value should be 0. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

20.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

Address(es): PORT0.PCNTR2 4004 0004h, PORT1.PCNTR2 4004 0024h, PORT2.PCNTR2 4004 0044h, PORT3.PCNTR2 4004 0064h, PORT4.PCNTR2 4004 0084h, PORT5.PCNTR2 4004 00A4h, PORT9.PCNTR2 4004 0124h,

PORT1.EIDR 4004 0024h, PORT2.EIDR 4004 0044h, PORT3.EIDR 4004 0064h, PORT4.EIDR 4004 0084h,

PORT0.PIDR 4004 0006h, PORT1.PIDR 4004 0026h, PORT2.PIDR 4004 0046h, PORT3.PIDR 4004 0066h, PORT4.PIDR 4004 0086h, PORT5.PIDR 4004 00A6h, PORT9.PIDR 4004 0126h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PIDRn	Pmn state	0: Low level 1: High level.	R
b31 to b16	EIDRn	Port Event Input Data*1	When the ELC_PORTx occurs: 0: Low input 1: High input.	R

m = 0 to 5, 9
n = 00 to 15
x = 1 to 4
Note 1. Supported for PORT1 to PORT4.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and the port event input data, and is accessed in 32-bit units. The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bit is read as undefined.

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PmnPFS.PDR. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

端口控制寄存器1(PCNTR1PODRPDR)是一个32位和16位读写寄存器，用于控制端口方向和端口输出数据。

PCNTR1指定端口方向和输出数据，并以32位为单位进行访问。PDRn（位[15:0]在PCNTR1)和PODRn（PCNTR1中的位[31:16]）分别以16位为单位进行访问。

当引脚配置为通用IO引脚时，PDRn位选择相关端口上各个引脚的输入或输出方向。端口m上的每个引脚都与一个PORTm.PCNTR1.PDRn位相关联。可以以1位为单位指定IO方向。与不存在的引脚相关的位被保留。保留位读为0。写入值应为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR1.PDR00、PORT2.PCNTR1.PDR14和PORT2.PCNTR1.PDR15。PORTm.PCNTR1寄存器中的PDRn位与

PFS.PmnPFS寄存器中的PDR位。

PODRn位保存要从通用IO引脚输出的数据。与不存在的引脚相关的位被保留。
保留位读为0。写入值应为0。P200、P214、P215仅为输入，因此保留PORT2.PCNTR1.PODR00、PORT2.PCNTR1.PODR14和PORT2.PCNTR1.PODR15位。保留位读取为0。写入值应为0。PORTm.PCNTR1寄存器中的PODRn位与PFS.PmnPFS寄存器中的PODR位具有相同的功能。

20.2.2 端口控制寄存器2(PCNTR2EIDRPIDR)

Address(es): PORT0.PCNTR2 4004 0004h, PORT1.PCNTR2 4004 0024h, PORT2.PCNTR2 4004 0044h, PORT3.PCNTR2 4004 0064h, PORT4.PCNTR2 4004 0084h, PORT5.PCNTR2 4004 00A4h, PORT9.PCNTR2 4004 0124h,

PORT1.EIDR 4004 0024h, PORT2.EIDR 4004 0044h, PORT3.EIDR 4004 0064h, PORT4.EIDR 4004 0084h,

PORT0.PIDR 4004 0006h, PORT1.PIDR 4004 0026h, PORT2.PIDR 4004 0046h, PORT3.PIDR 4004 0066h, PORT4.PIDR 4004 0086h, PORT5.PIDR 4004 00A6h, PORT9.PIDR 4004 0126h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b15 to b0	PIDRn	Pmn state	0：低电平1 ：高电平。	R
b31 to b16	EIDRn	端口事件输入数据*1	当ELC_PORTx发生时：0：低输入1：高输入。	R

m=0到5 9n=
00到15x=1
到4注1。

支持PORT1到PORT4。

端口控制寄存器2(PCNTR2EIDRPIDR)允许使用32位或16位访问对Pmn状态和端口事件输入数据进行读取访问。

PCNTR2指定Pmn状态和端口事件输入数据，并以32位为单位进行访问。PIDRn（PCNTR2中的位[15:0]）和EIDRn（PCNTR2中的位[31:16]）分别以16位为单位进行访问。与不存在的引脚相关的位被保留。保留位被读取为未定义。

PIDRn位反映端口的各个引脚状态，与PmnPFS.PMR和PmnPFS.PDR。PORTm.PCNTR2寄存器中的PIDRn位与PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)
- CS area controller (CSC)
- Analog function (ASEL = 1)
- Capacitive Touch Sensing Unit (CTSU)
- Segment LCD Controller (SLCDC)
- USB 2.0 Full-Speed Module (USBFS).

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PmnPFS.PDR are 0. When PmnPFS.ASEL is set to 1, the associated pin state is not reflected in EIDRn.

20.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

Address(es): PORT0.PCNTR3 4004 0008h, PORT1.PCNTR3 4004 0028h, PORT2.PCNTR3 4004 0048h, PORT3.PCNTR3 4004 0068h, PORT4.PCNTR3 4004 0088h, PORT5.PCNTR3 4004 00A8h, PORT9.PCNTR3 4004 0128h,

PORT0.PORR 4004 0008h, PORT1.PORR 4004 0028h, PORT2.PORR 4004 0048h, PORT3.PORR 4004 0068h, PORT4.PORR 4004 0088h, PORT5.PORR 4004 00A8h, PORT9.PORR 4004 0128h,

PORT0.POSR 4004 000Ah, PORT1.POSR 4004 002Ah, PORT2.POSR 4004 004Ah, PORT3.POSR 4004 006Ah, PORT4.POSR 4004 008Ah, PORT5.POSR 4004 00AAh, PORT9.POSR 4004 012Ah

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORR 15	PORR 14	PORR 13	PORR 12	PORR 11	PORR 10	PORR 09	PORR 08	PORR 07	PORR 06	PORR 05	PORR 04	PORR 03	PORR 02	PORR 01	PORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	POSR 15	POSR 14	POSR 13	POSR 12	POSR 11	POSR 10	POSR 09	POSR 08	POSR 07	POSR 06	POSR 05	POSR 04	POSR 03	POSR 02	POSR 01	POSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	POSRn	Pmn Output Set	0: No effect on output 1: High output.	W
b31 to b16	PORRn	Pmn Output Reset	0: No effect on output 1: Low output.	W

m = 0 to 5, 9
n = 00 to 15

Note: When EORRn or EOSRn is set, writing to PODRn, PORRn, and POSRn is prohibited.
Note: PORRn and POSRn should not be set at the same time.

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32- and 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units. The POSRn (bits [15:0] in PCNTR3) and PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 is 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.POSR00, PORT2.PCNTR3.POSR14, and PORT2.PCNTR3.POSR15 are reserved.

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.PORR00 is 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always

当启用以下功能之一时，引脚状态无法反映在PIDRn中：

- 主时钟振荡器(MOSC)
- Sub-clock oscillator (SOSC)
- CS区域控制器(CSC)
- 模拟功能(ASEL=1)
- 电容式触控感应单元(CTSU)
- 段式LCD控制器(SLCDC)
- USB2.0全速模块(USBFS)。

当ELC_PORTx信号出现时，EIDRn位锁存引脚状态。引脚状态只能输入到EIDRn时PmnPFS.PMR和PmnPFS.PDR为0。当PmnPFS.ASEL设置为1时，关联的引脚状态不会反映在EIDRn.

20.2.3 端口控制寄存器3(PCNTR3PORRPOSR)

Address(es): PORT0.PCNTR3 4004 0008h, PORT1.PCNTR3 4004 0028h, PORT2.PCNTR3 4004 0048h, PORT3.PCNTR3 4004 0068h, PORT4.PCNTR3 4004 0088h, PORT5.PCNTR3 4004 00A8h, PORT9.PCNTR3 4004 0128h,

PORT0.PORR 4004 0008h, PORT1.PORR 4004 0028h, PORT2.PORR 4004 0048h, PORT3.PORR 4004 0068h, PORT4.PORR 4004 0088h, PORT5.PORR 4004 00A8h, PORT9.PORR 4004 0128h,

PORT0.POSR 4004 000Ah, PORT1.POSR 4004 002Ah, PORT2.POSR 4004 004Ah, PORT3.POSR 4004 006Ah, PORT4.POSR 4004 008Ah, PORT5.POSR 4004 00AAh, PORT9.POSR 4004 012Ah

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORR 15	PORR 14	PORR 13	PORR 12	PORR 11	PORR 10	PORR 09	PORR 08	PORR 07	PORR 06	PORR 05	PORR 04	PORR 03	PORR 02	PORR 01	PORR 00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	POSR 15	POSR 14	POSR 13	POSR 12	POSR 11	POSR 10	POSR 09	POSR 08	POSR 07	POSR 06	POSR 05	POSR 04	POSR 03	POSR 02	POSR 01	POSR 00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	POSRn	Pmn输出设置	0：对输出无影响1： 高输出。	W
b31 to b16	PORRn	Pmn输出复位	0：对输出无影响1： 低输出。	W

m = 0 to 5, 9
n = 00 to 15

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: PORRn和POSRn不应同时设置。

端口控制寄存器3(PCNTR3PORRPOSR)是一个32位和16位的写寄存器，用于控制端口输出数据的设置或复位。

PCNTR3控制端口输出数据的设置或复位，并以32位为单位进行访问。POSRn（PCNTR3中的位[15:0]）和PORRn（PCNTR3中的位[31:16]）分别以16位为单位进行访问。

POSR在通过软件写入设置时改变PODR。例如，对于P100，当PORT1.PCNTR3.POSR00为1时，PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR3.POSR00、PORT2.PCNTR3.POSR14和PORT2.PCNTR3.POSR15。

PORR在通过软件写入复位时改变PODR。例如，对于P100，当PORT1.PCNTR3.PORR00为1时，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终

be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.PORR00, PORT2.PCNTR3.PORR14, and PORT2.PCNTR3.PORR15 are reserved.

20.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

Address(es): PORT1.PCNTR4 4004 002Ch, PORT2.PCNTR4 4004 004Ch, PORT3.PCNTR4 4004 006Ch, PORT4.PCNTR4 4004 008Ch,

PORT1.EORR 4004 002Ch, PORT2.EORR 4004 004Ch, PORT3.EORR 4004 006Ch, PORT4.EORR 4004 008Ch,

PORT1.EOSR 4004 002Eh, PORT2.EOSR 4004 004Eh, PORT3.EOSR 4004 006Eh, PORT4.EOSR 4004 008Eh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EORR 15	EORR 14	EORR 13	EORR 12	EORR 11	EORR 10	EORR 09	EORR 08	EORR 07	EORR 06	EORR 05	EORR 04	EORR 03	EORR 02	EORR 01	EORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EOSR 15	EOSR 14	EOSR 13	EOSR 12	EOSR 11	EOSR 10	EOSR 09	EOSR 08	EOSR 07	EOSR 06	EOSR 05	EOSR 04	EOSR 03	EOSR 02	EOSR 01	EOSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	EOSRn	Pmn Event Output Set	When an ELC_PORTx occurs: 0: No effect on output 1: High output.	R/W
b31 to b16	EORRn	Pmn Event Output Reset	When an ELC_PORTx occurs: 0: No effect on output 1: Low output.	R/W

m = 1 to 4
n = 00 to 15
x = 1 to 4

Note: When EORRn or EOSRn is set, writing to PODRn, PORRn, and POSRn is prohibited.
Note: EORRn and EOSRn should not be set at the same time.

The Port Control Register 4 is a 32-bit and 16-bit read/write register that controls the setting or resetting of the port output data by an event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units. The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR4.EOSR00, PORT2.PCNTR4.EOSR14, and PORT2.PCNTR4.EOSR15 are reserved.

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EORR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR4.EORR00, PORT2.PCNTR4.EORR14, and PORT2.PCNTR4.EORR15 bits are reserved.

为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR3.PORR00、PORT2.PCNTR3.PORR14和PORT2.PCNTR3.PORR15。

20.2.4 端口控制寄存器4(PCNTR4EORREOSR)

Address(es): PORT1.PCNTR4 4004 002Ch, PORT2.PCNTR4 4004 004Ch, PORT3.PCNTR4 4004 006Ch, PORT4.PCNTR4 4004 008Ch,

PORT1.EORR 4004 002Ch, PORT2.EORR 4004 004Ch, PORT3.EORR 4004 006Ch, PORT4.EORR 4004 008Ch,

PORT1.EOSR 4004 002Eh, PORT2.EOSR 4004 004Eh, PORT3.EOSR 4004 006Eh, PORT4.EOSR 4004 008Eh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EORR 15	EORR 14	EORR 13	EORR 12	EORR 11	EORR 10	EORR 09	EORR 08	EORR 07	EORR 06	EORR 05	EORR 04	EORR 03	EORR 02	EORR 01	EORR 00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EOSR 15	EOSR 14	EOSR 13	EOSR 12	EOSR 11	EOSR 10	EOSR 09	EOSR 08	EOSR 07	EOSR 06	EOSR 05	EOSR 04	EOSR 03	EOSR 02	EOSR 01	EOSR 00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	EOSRn	Pmn事件输出集	当发生ELC_PORTx时：0：对输出没有影响1：高输出。	R/W
b31 to b16	EORRn	Pmn事件输出复位	当ELC_PORTx发生时：0：对输出没有影响1：低输出。	R/W

m = 1 to 4
n = 00 to 15
x = 1 to 4

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: EORRn和EOSRn不应同时设置。

端口控制寄存器4是一个32位和16位读写寄存器，通过来自ELC的事件输入来控制端口输出数据的设置或复位。

PCNTR4通过来自ELC的事件输入来控制端口输出数据的设置或复位，并以32位为单位进行访问。分别以16位为单位访问EOSRn（PCNTR4中的位[15:0]）和EORRn（PCNTR4中的位[31:16]）。

EOSR在设置时会更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果当ELC_PORTx发生时，PORT1.PCNTR4.EOSR00设置为1，PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR4.EOSR00、PORT2.PCNTR4.EOSR14和PORT2.PCNTR4.EOSR15。

EORR会在复位时更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果当ELC_PORTx发生时，PORT1.PCNTR4.EORR00设置为1，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR4.EORR00、PORT2.PCNTR4.EORR14和PORT2.PCNTR4.EORR15位。

20.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15)

Address(es): PFS.P004PFS 4004 0810h, PFS.P010PFS 4004 0828h, PFS.P011PFS 4004 082Ch, PFS.P014PFS 4004 0838h, PFS.P015PFS 4004 083Ch, PFS.P100PFS 4004 0840h to PFS.P111PFS 4004 086Ch, PFS.P200PFS 4004 0880h, PFS.P201PFS 4004 0884h, PFS.P204PFS 4004 0890h to PFS.P206PFS 4004 0898h, PFS.P212PFS 4004 08B0h to PFS.P215PFS 4004 08BCh, PFS.P300PFS 4004 08C0h, PFS.P402PFS 4004 0908h, PFS.P404PFS 4004 0910h, PFS.P407PFS 4004 091Ch, PFS.P409PFS 4004 0924h, PFS.P414PFS 4004 0938h, PFS.P501PFS 4004 0944h, PFS.P914PFS 4004 0A78h, PFS.P915PFS 4004 0A7Ch,

PFS.P004PFS_HA 4004 0812h, PFS.P010PFS_HA 4004 082Ah, PFS.P011PFS_HA 4004 082Eh, PFS.P014PFS 4004 083Ah, PFS.P015PFS_HA 4004 083Eh, PFS.P100PFS_HA 4004 0842h to PFS.P111PFS_HA 4004 086Eh, PFS.P200PFS_HA 4004 0882h, PFS.P201PFS_HA 4004 0886h, PFS.P204PFS_HA 4004 0892h to PFS.P206PFS_HA 4004 089Ah, PFS.P212PFS_HA 4004 08B2h to PFS.P215PFS_HA 4004 08BEh, PFS.P300PFS_HA 4004 08C2h, PFS.P402PFS_HA 4004 090Ah, PFS.P404PFS_HA 4004 0912h, PFS.P407PFS_HA 4004 091Eh, PFS.P409PFS_HA 4004 0926h, PFS.P414PFS_HA 4004 093Ah, PFS.P501PFS_HA 4004 0946h, PFS.P914PFS_HA 4004 0A7Ah, PFS.P915PFS_HA 4004 0A7Eh

PFS.P004PFS_BY 4004 0813h, PFS.P010PFS_BY 4004 082Bh, PFS.P011PFS_BY 4004 082Fh, PFS.P014PFS_BY 4004 083Bh, PFS.P015PFS_BY 4004 083Fh, PFS.P100PFS_BY 4004 0843h to PFS.P111PFS_BY 4004 086Fh, PFS.P200PFS_BY 4004 0883h, PFS.P201PFS_BY 4004 0887h, PFS.P204PFS_BY 4004 0893h to PFS.P206PFS_BY 4004 089Bh, PFS.P212PFS_BY 4004 08B3h to PFS.P215PFS_BY 4004 08BFh, PFS.P300PFS_BY 4004 08C3h, PFS.P402PFS_BY 4004 090Bh, PFS.P404PFS_BY 4004 0913h, PFS.P407PFS_BY 4004 091Fh, PFS.P409PFS_BY 4004 0927h, PFS.P414PFS_BY 4004 093Bh, PFS.P501PFS_BY 4004 0947h, PFS.P914PFS_BY 4004 0A7Bh, PFS.P915PFS_BY 4004 0A7Fh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*2

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	EOF	EOR	DSCR1	DSCR	—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0	0	0	0	0	0*2	0	0	0	0	0	0*2	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PODR	Port Output Data	0: Low output 1: High output.	R/W
b1	PIDR	Pmn state	0: Low level 1: High level.	R
b2	PDR	Port Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	PCR	Pull-up Control	0: Disable an input pull-up 1: Enable an input pull-up	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	NCODR	N-Channel Open Drain Control	0: CMOS output 1: NMOS open-drain output.	R/W
b9 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10	DSCR	Port Drive Capability	0: Low drive 1: Middle drive.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	EOF/EOR	Event on Falling/Event on Rising*1	b13 b12 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges.	R/W
b14	ISEL	IRQ Input Enable	0: Not used as an IRQn input pin 1: Used as an IRQn input pin.	R/W
b15	ASEL	Analog Input Enable	0: Not used as an analog pin 1: Used as an analog pin.	R/W
b16	PMR	Port Mode Control	0: Used as a general I/O pin 1: Used as an I/O port for peripheral functions.	R/W

20.2.5 端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)(m=0to5 9;n=00to15)

Address(es): PFS.P004PFS 4004 0810h, PFS.P010PFS 4004 0828h, PFS.P011PFS 4004 082Ch, PFS.P014PFS 4004 0838h, PFS.P015PFS 4004 083Ch, PFS.P100PFS 4004 0840h to PFS.P111PFS 4004 086Ch, PFS.P200PFS 4004 0880h, PFS.P201PFS 4004 0884h, PFS.P204PFS 4004 0890h to PFS.P206PFS 4004 0898h, PFS.P212PFS 4004 08B0h to PFS.P215PFS 4004 08BCh, PFS.P300PFS 4004 08C0h, PFS.P402PFS 4004 0908h, PFS.P404PFS 4004 0910h, PFS.P407PFS 4004 091Ch, PFS.P409PFS 4004 0924h, PFS.P414PFS 4004 0938h, PFS.P501PFS 4004 0944h, PFS.P914PFS 4004 0A78h, PFS.P915PFS 4004 0A7Ch,

PFS.P004PFS_HA 4004 0812h, PFS.P010PFS_HA 4004 082Ah, PFS.P011PFS_HA 4004 082Eh, PFS.P014PFS 4004 083Ah, PFS.P015PFS_HA 4004 083Eh, PFS.P100PFS_HA 4004 0842h to PFS.P111PFS_HA 4004 086Eh, PFS.P200PFS_HA 4004 0882h, PFS.P201PFS_HA 4004 0886h, PFS.P204PFS_HA 4004 0892h to PFS.P206PFS_HA 4004 089Ah, PFS.P212PFS_HA 4004 08B2h to PFS.P215PFS_HA 4004 08BEh, PFS.P300PFS_HA 4004 08C2h, PFS.P402PFS_HA 4004 090Ah, PFS.P404PFS_HA 4004 0912h, PFS.P407PFS_HA 4004 091Eh, PFS.P409PFS_HA 4004 0926h, PFS.P414PFS_HA 4004 093Ah, PFS.P501PFS_HA 4004 0946h, PFS.P914PFS_HA 4004 0A7Ah, PFS.P915PFS_HA 4004 0A7Eh

PFS.P004PFS_BY 4004 0813h, PFS.P010PFS_BY 4004 082Bh, PFS.P011PFS_BY 4004 082Fh, PFS.P014PFS_BY 4004 083Bh, PFS.P015PFS_BY 4004 083Fh, PFS.P100PFS_BY 4004 0843h to PFS.P111PFS_BY 4004 086Fh, PFS.P200PFS_BY 4004 0883h, PFS.P201PFS_BY 4004 0887h, PFS.P204PFS_BY 4004 0893h to PFS.P206PFS_BY 4004 089Bh, PFS.P212PFS_BY 4004 08B3h to PFS.P215PFS_BY 4004 08BFh, PFS.P300PFS_BY 4004 08C3h, PFS.P402PFS_BY 4004 090Bh, PFS.P404PFS_BY 4004 0913h, PFS.P407PFS_BY 4004 091Fh, PFS.P409PFS_BY 4004 0927h, PFS.P414PFS_BY 4004 093Bh, PFS.P501PFS_BY 4004 0947h, PFS.P914PFS_BY 4004 0A7Bh, PFS.P915PFS_BY 4004 0A7Fh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*2

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	EOF	EOR	DSCR1	DSCR	—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值:	0	0	0	0	0	0*2	0	0	0	0	0	0*2	0	0	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PODR	端口输出数据	0：低输出1： 高输出。	R/W
b1	PIDR	Pmn state	0：低电平1 ：高电平。	R
b2	PDR	港口方向	0：输入（用作输入引脚）1：输出（ 用作输出引脚）。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	PCR	Pull-up Control	0：禁用输入上拉1：启用 输入上拉	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	NCODR	N沟道开漏控制	0: CMOS output 1: NMOS open-drain output.	R/W
b9 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10	DSCR	端口驱动能力	0：低驱动1： 中驱动。	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b13, b12	EOF/EOR	坠落事件 Rising*1	b13b1200：无关01：检 测上升沿10：检测下降沿 11：检测两个沿。	R/W
b14	ISEL	IRQ输入使能	0：不用作IRQn输入引脚1：用作 IRQn输入引脚。	R/W
b15	ASEL	模拟输入使能	0：不用作模拟引脚1：用作 模拟引脚。	R/W
b16	PMR	端口模式控制	0：用作通用IO引脚1：用作外围功能的IO端口 。	R/W

Bit	Symbol	Bit name	Description	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28 to b24	PSEL[4:0]	Peripheral Select	These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Supported for PORT1 to PORT4.
Note 2. The initial value of P108, P109, P110, P201, P300, P914 and P915 is not 0000 0000h.
P108 is 0001 0010h, P109 is 0001 0000h, P110 is 0001 0010h, P201 is 0000 0010h, P300 is 0001 0010h,P914 is 0001 0000h, and P915 is 0001 0000h.
The Port mn Pin Function Select register (PmnPFS) selects the pin function.

The Port mn Pin Function Select register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, and 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (bits [15:0] in PmnPFS) is accessed in 16-bit units. PmnPFS_BY (bits [7:0]) is accessed in 8-bit units.

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as an external bus pin, a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

The DSCR1 and DSCR bits switch the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is read/write, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

The EOR and EOF bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOR/EOF bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

The ISEL bit specifies IRQ input pins. This setting can be used in combination with the peripheral functions, although an IRQn (external pin interrupt) of the same number must only be enabled for one pin.

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port with the Port Mode Control bit (PmnPFS.PMR).
2. Disable the pull-up resistor with the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input with the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

The ISEL bit for an unspecified IRQn is reserved. The ASEL bit for an unspecified analog input/output is reserved.

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

The PSEL[4:0] bits assign the peripheral function.

For details of the peripheral settings for each product, see section 20.6, Peripheral Select Settings for each Product.

Bit	Symbol	位名称	Description	R/W
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28 to b24	PSEL[4:0]	外设选择	这些位选择外设功能。对于各个引脚功能，请参见本章中的相关表格。	R/W
b31 to b29	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 支持PORT1到PORT4。
Note 2. P108、P109、P110、P201、P300、P914、P915的初始值不是00000000h。
P108为00010010h，P109为00010000h，P110为00010010h，P201为00000010h，P300为00010010h，P914为00010000h，P915为00010000h。端口mn引脚功能选择寄存器(PmnPFS)选择引脚功能。

端口mn引脚功能选择寄存器（PmnPFSPmnPFS_HAPmnPFS_BY）是选择端口mn引脚功能的32位、16位和8位读写控制寄存器，以32位为单位进行访问。PmnPFS_HA（PmnPFS中的位[15:0]）以16位为单位进行访问。PmnPFS_BY（位[7:0]）以8位为单位进行访问。

PDRPIDRPODR位的功能与PCNTR相同。读取这些位时，将读取PCNTR值。

PCR位启用或禁用各个端口引脚上的输入上拉电阻。当引脚处于输入状态且PmnPFS.PCR中的相关位设置为1时，连接到该引脚的上拉电阻被启用。当引脚设置为外部总线引脚、通用端口输出引脚或外围功能输出引脚时，无论PCR设置如何，该引脚的上拉电阻都被禁用。上拉电阻在复位状态下也被禁用。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

NCODR位指定端口引脚的输出类型。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

DSCR1和DSCR位切换端口的驱动能力。如果某个管脚的驱动能力是固定的，则对应的位是读写，但驱动能力不能改变。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

EOR和EOF位选择端口组输入信号的边沿检测方法。这些位支持上升沿、下降沿或两个边沿检测。当EOREOF位设置为01b、10b或11b时，IO单元的输入使能有效。随后，事件脉冲从外部引脚输入，GPIO将事件脉冲输出到ELC。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

ISEL位指定IRQ输入引脚。此设置可以与外围功能结合使用，尽管
相同编号的IRQn（外部引脚中断）只能为一个引脚启用。

ASEL位指定模拟引脚。当一个引脚被该位设置为模拟引脚时：

1. 通过端口模式控制位(PmnPFS.PMR)将其指定为通用IO端口。
2. 使用上拉控制位(PmnPFS.PCR)禁用上拉电阻。
3. 使用端口方向位(PmnPFS.PDR)指定输入。此时无法读取引脚状态。这
PmnPFS寄存器受写保护寄存器(PWPR)保护。在修改寄存器之前释放写保护。

未指定的IRQn的ISEL位被保留。未指定模拟输入输出的ASEL位被保留。

PMR位指定端口引脚功能。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

PSEL[4:0]位分配外设功能。

有关每个产品的外设设置的详细信息，请参阅第20.6节，每个产品的外设选择设置。

20.2.6 Write-Protect Register (PWPR)

Address(es): PMISC.PWPR 4004 0D03h

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PmnPFS Register Write Enable	0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled.	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled.	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

20.3 Operation

20.3.1 General I/O Ports

All pins except P108, P109, P110, P300, P914, and P915 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or by individual pins with the Pin Function Select Registers. For details on these registers, see section 20.2, Register Descriptions.

Each port has the following bits:

- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin state
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORT1, 2, 3, or 4 signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORT1, 2, 3, or 4 signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORT1, 2, 3, or 4 signal occurs.

20.3.2 Port Function Select

The following port functions are available for configuring each pin:

- I/O configuration: Complementary or open-drain output, pull-up control, and drive strength
- General I/O: Port direction, output data setting, and read input data
- Alternate functions: Configured function mapping to the pin.

Each pin is associated with a Pin Function Select Register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes the following:

20.2.6 Write-Protect Register (PWPR)

Address(es): PMISC.PWPR 4004 0D03h

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	PFSWE	PmnPFS寄存器写入Enable	0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器。	R/W
b7	B0WI	PFSWE位写入禁用	0：允许写入PFSWE位1：禁止写入PFSWE位。	R/W

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时才允许写入PmnPFS寄存器。您必须先将0写入B0WI位，然后再将PFSWE设置为1。

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

20.3 Operation

20.3.1 通用IO端口

除P108、P109、P110、P300、P914和P915外的所有引脚在复位后都作为通用IO端口工作。通用IO端口组织为每个端口16位，可以通过端口控制寄存器（PCNTRn，其中n=1到4）通过端口访问，或者通过引脚功能选择寄存器通过单个引脚访问。有关这些寄存器的详细信息，请参见第20.2节，寄存器说明。

每个端口都有以下位：

- 端口方向位(PDRn)，用于选择输入或输出方向
- 端口输出数据位(PODRn)，用于保存输出数据
- 端口输入数据位(PIDRn)，指示引脚状态
- 事件输入数据位(EIDRn)，指示发生ELC_PORT1、2、3或4信号时的引脚状态
- 端口输出设置位(POSRn)，表示发生软件写入时的输出值
- 端口输出复位位(PORRn)，指示发生软件写入时的输出值
- 事件输出设置位(EOSRn)，指示ELC_PORT1、2、3或4信号发生时的输出值
- 事件输出复位位(EORRn)，指示发生ELC_PORT1、2、3或4信号时的输出值。

20.3.2 端口功能选择

以下端口功能可用于配置每个引脚：

- IO配置：互补或开漏输出、上拉控制和驱动强度
- 通用IO：端口方向、输出数据设置、读取输入数据
- 备用功能：配置的功能映射到引脚。

每个引脚都与一个引脚功能选择寄存器(PmnPFS)相关联，其中包括相关的PODR、PIDR和PDR位。此外，PmnPFS寄存器包括以下内容：

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR1, DSCR: Drive capacity control bit that selects the drive capacity
- EOR: Event on rising bit used to detect rising edges on the port input
- EOF: Event on falling bit used to detect falling edges on the port input
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode control bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Pin Function Select Register. For details, see section 20, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15).

20.3.3 Port Group Function for the ELC

In the MCU, PORT1 to PORT4 are assigned for the port group function.

20.3.3.1 Behavior when ELC_PORT1, 2, 3, or 4 is input from the ELC

The MCU supports the two functions described in this section when an ELC_PORT1, 2, 3, or 4 signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORT1, 2, 3, or 4 signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins are read into the EIDR bit.

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

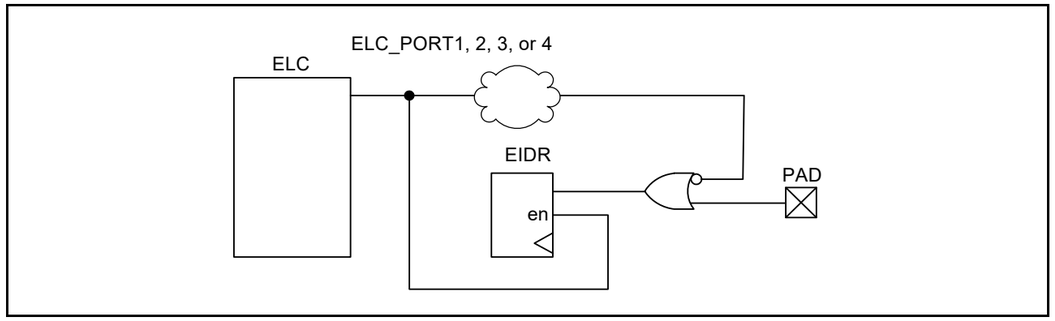


Figure 20.2 Event ports input data

(2) Output from PODR by EOSR/EORR

When an ELC_PORT1, 2, 3, or 4 signal occurs, the data is output from the PODR to the external pin based on the EOSR/EORR bit settings as follows:

- If EOSR is set to 1, when an ELC_PORT1, 2, 3, or 4 signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is kept.
- If EORR is set to 1, when an ELC_PORT1, 2, 3, or 4 signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is kept.

See Figure 20.3.

- PCR：上拉电阻控制位，用于打开或关闭输入上拉MOS
- NCODR：为每个引脚选择输出类型的N通道开漏控制位
- DSCR1、DSCR：选择驱动器容量的驱动器容量控制位
- EOR：上升位事件，用于检测端口输入的上升沿
- EOF：下降位事件，用于检测端口输入的下降沿
- ISEL：IRQ输入使能位，用于指定IRQ输入引脚
- ASEL：模拟输入使能位，用于指定模拟引脚
- PMR：端口模式控制位，指定每个端口的引脚功能
- PSEL[4:0]：端口功能选择位，用于选择相关的外设功能。

这些配置可以通过单个寄存器访问引脚功能选择寄存器来进行。有关详细信息，请参见第20节，端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)(m=0到5、9；n=00到15)。

20.3.3 ELC的端口组功能

在MCU中，为端口组功能分配了PORT1到PORT4。

20.3.3.1 从ELC输入ELC_PORT1、2、3或4时的行为

当ELC_PORT1、2、3或4信号来自
ELC.

(1) 输入到EIDR

对于GPI功能（PmnPFS寄存器中的PDR=0和PMR=0），当ELC_PORT1、2、3或4信号来自ELC时，IO单元的输入使能有效，并且来自外部引脚的数据被读入EIDR位。

对于GPO功能(PDR=1)或外设模式(PMR=1)，0从外部引脚输入到EIDR位。

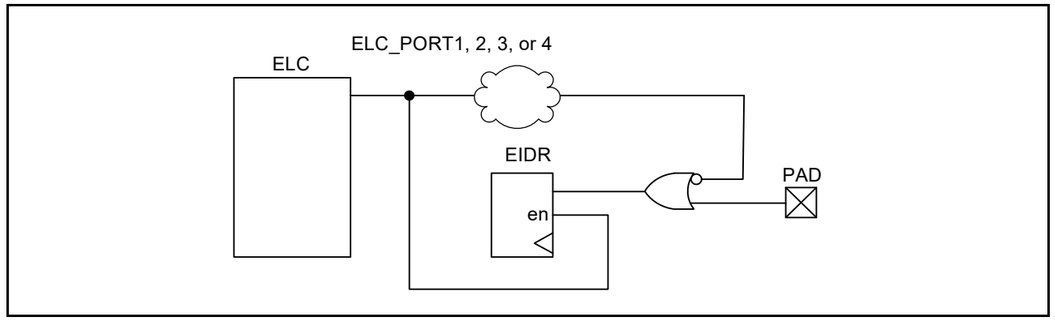


Figure 20.2 事件端口输入数据

(2) EOSREORR从PODR输出

当ELC_PORT1、2、3或4信号发生时，数据从PODR输出到基于EOSR的外部引脚
EORR位设置如下：

- 如果EOSR设置为1，当ELC_PORT1、2、3或4信号发生时，PODR寄存器输出1到外部引脚。
  否则，当EOSR=0时，保持PODR值。
- 如果EORR设置为1，则当ELC_PORT1、2、3或4信号发生时，PODR寄存器向外部引脚输出0。
  否则，当EORR=0时，保持PODR值。

请参见图20.3。

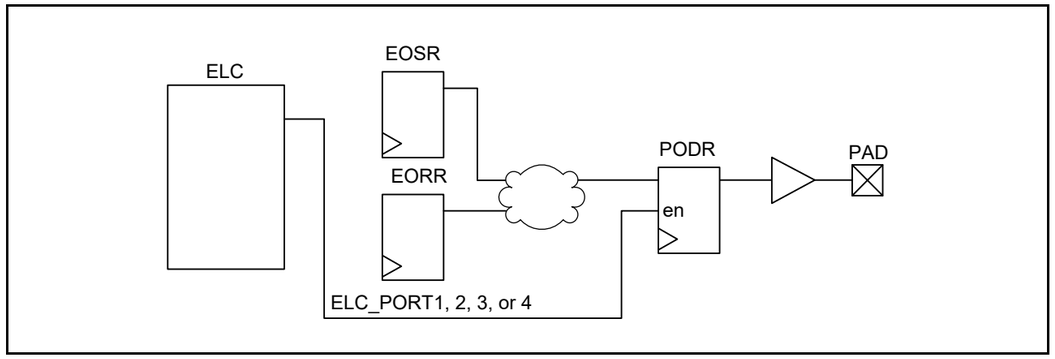


Figure 20.3 Event ports output data

20.3.3.2 Behavior when an event pulse is output to the ELC

To output the event pulse from the external pins to the ELC, set the EOR/EOF bits in the PmnPFS register. For details, see section 20.2.5, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5, 9; n = 00 to 15). When the EOR/EOF bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for PORT1, when the data is input from P100 to P111, the data of those 12 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORT2 to PORT4 is the same. See Figure 20.4.

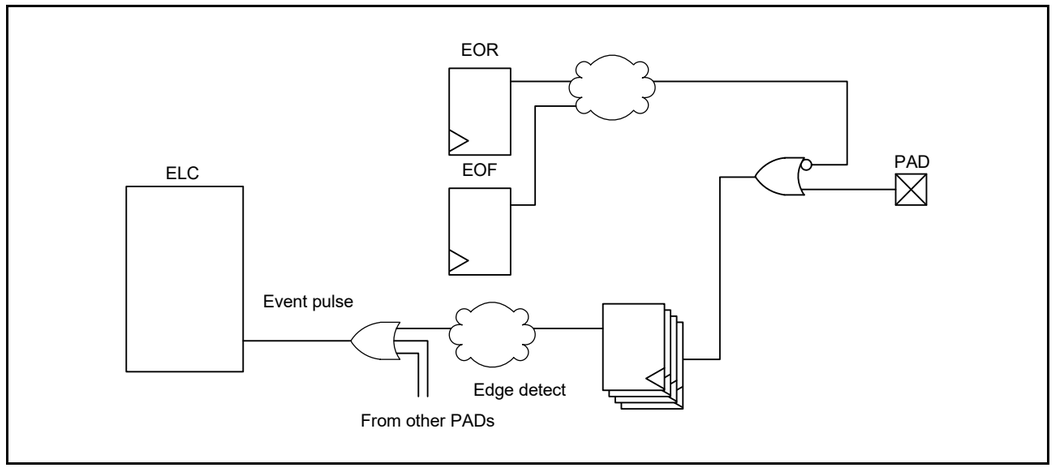


Figure 20.4 Generation of event pulse

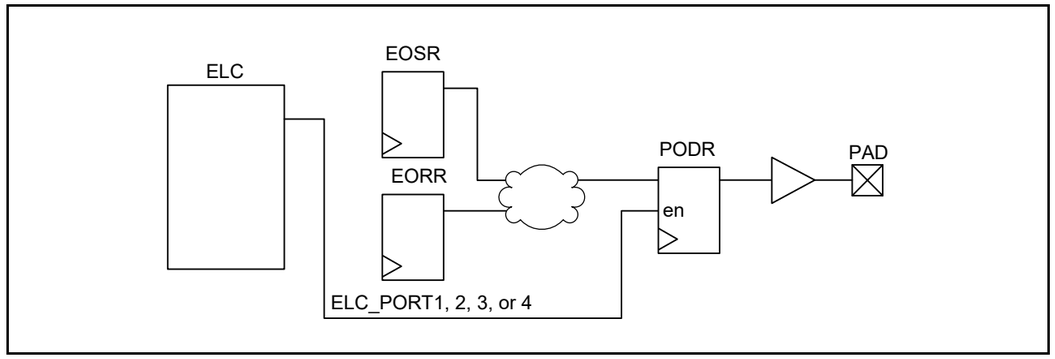


Figure 20.3 事件端口输出数据

20.3.3.2 事件脉冲输出到ELC时的行为

要将事件脉冲从外部引脚输出到ELC，请设置PmnPFS寄存器中的EOREOF位。有关详细信息，请参见第20.2.5节，端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)(m=0to5 9;n=00to15)。当EOREOF位被置位时，IO单元的输入使能被断言。

来自外部引脚的数据是输入。例如，对于PORT1，当数据从P100输入到P111时，这12个引脚的数据由OR逻辑组织。该数据形成一个单次脉冲，该脉冲进入ELC。PORT2到PORT4的操作是一样的。请参见图20.4。

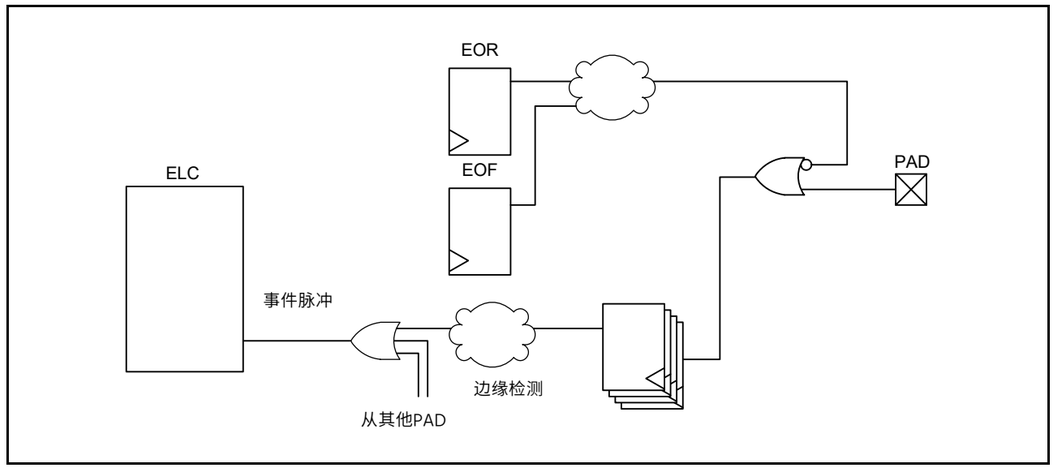


Figure 20.4 事件脉冲的产生

20.4 Handling of Unused Pins

Table 20.3 shows how to handle unused pins.

Table 20.3 Handling of unused pins

Pin name	Description
P201/MD	Use as a mode pin
RES	Connect to VCC through a resistor (pulling up)
USB_DP, USB_DM	When both P914PFS.PMR and P915PFS.PMR bits are set to 1, keep these pins open. When P914PFS.PMR or P915PFS.PMR bit is set to 0, configure it in the same way as ports 1 to 9.
P200/NMI	Connect to VCC through a resistor (pulling up)
P212/EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports 1 to 9.
P213/XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When this pin is not used as port P213, configure it in the same way as ports 1 to 9. When the external clock is input to the EXTAL pin, leave this pin open.
P215/XCIN	When the sub-clock oscillator is not used, set the SOSCCR.SOSTP bit to 1 (general port P215). When this pin is not used as port P215, configure it in the same way as ports 1 to 9.
P214/XCOUT	When the sub-clock oscillator is not used, set the SOSCCR.SOSTP bit to 1 (general port P214). When this pin is not used as port P214, configure it in the same way as ports 1 to 9.
P004, P010, P011, P014, P015	If the direction setting is for input (PCNTR1.PDRn = 0), connect the associated pin to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor.*1
P1x to P9x other than P200, P201 and P212 to P215	• If the direction setting is for input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor*1,*2 • If the direction setting is for output (PCNTR1.PDRn = 1), release the pin.*1,*3

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108, P110, and P300 are recommended for pull up VCC (pulled up) through a resistor, because these pins are input pull-up enabled from the initial value (PmnPFS.PCR=1).
Note 3. P109 is recommended to be set as an output (PCNTR1.PDRn = 1), because this pin is output from the initial value.

20.5 Usage Notes

20.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.
3. Clear the Port Mode Control bit in the PMR for the target pin to select the general I/O port.
4. Specify the input/output function for the pin through the PSEL[4:0] bit settings in the PmnPFS register.
5. Set the PMR to 1 as required to switch to the selected input/output function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.

20.5.2 Procedure for Using Port Group Input

To use the port group input (PORT1 to PORT4):

1. Set the ELSRx.ELS[7:0] bits to 0000 0000b to ignore unexpected pulses. For more information, see section 19, Event Link Controller (ELC).
2. Set the EOF/EOR bit of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[8:0] bits to enable the event signals.

20.4 未使用引脚的处理

表20.3显示了如何处理未使用的引脚。

Table 20.3 处理未使用的引脚

引脚名称	Description
P201/MD	用作模式引脚
RES	通过一个电阻连接到VCC（上拉）
USB_DP, USB_DM	当P914PFS.PMR和P915PFS.PMR位都设置为1时，保持这些引脚开路。 当P914PFS.PMR或P915PFS.PMR位设置为0时，按照与端口1到9相同的方式进行配置。
P200/NMI	通过一个电阻连接到VCC（上拉）
P212/EXTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P212）。 当该管脚不作为端口P212使用时，配置方式与端口1到9相同。
P213/XTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P213）。 当该管脚不作为端口P213使用时，配置方式与端口1到9相同。 当外部时钟输入到EXTAL引脚时，使该引脚保持打开状态。
P215/XCIN	当不使用副时钟振荡器时，将SOSCCR.SOSTP位设置为1（通用端口P215）。 该管脚不作为端口P215使用时，与端口1～9一样配置。
P214/XCOUT	当不使用副时钟振荡器时，将SOSCCR.SOSTP位设置为1（通用端口P214）。 当该管脚不作为端口P214使用时，按照与端口1到9相同的方式进行配置。
P004, P010, P011, P014, P015	如果方向设置为输入(PCNTR1.PDRn=0)，则通过电阻将相关引脚连接到AVCC0（上拉）或通过电阻连接到AVSS0（下拉）。*1
P1x到P9x，除了P200、P201和P212到P215	如果方向设置为输入(PCNTR1.PDRn=0)，则将相关引脚通过电阻连接到VCC（上拉）或通过电阻连接到VSS（下拉）*1、*2 如果方向设置为对于输出(PCNTR1.PDRn=1)，释放引脚。*1 *3

Note 1. 将PmnPFS.PMR、PmnPFS.ISEL、PmnPFS.PCR和PmnPFS.ASEL位清除为0。
Note 2. 推荐P108、P110和P300通过电阻上拉VCC（上拉），因为这些引脚从初始值（PmnPFS.PCR=1）开始输入上拉使能。
Note 3. 建议将P109设置为输出（PCNTR1.PDRn=1），因为该引脚是从初始值输出的。

20.5 使用说明

20.5.1 指定引脚功能的步骤

要指定IO引脚功能：

1. 将PWPR寄存器中的B0WI位清零。这允许写入PWPR寄存器中的PFSWE位。
2. 将PWPR寄存器中的PFSWE位设置为1。这允许写入PmnPFS寄存器。
3. 清除目标引脚的PMR中的端口模式控制位以选择通用IO端口。
4. 通过PmnPFS寄存器中的PSEL[4:0]位设置指定引脚的输入输出功能。
5. 根据需要将PMR设置为1，以切换到引脚的选定输入输出功能。
6. 将PWPR寄存器中的PFSWE位清零。这将禁止写入PmnPFS寄存器。
7. 将PWPR寄存器中的B0WI位设置为1。这将禁止写入PWPR寄存器中的PFSWE位。

20.5.2 使用端口组输入的过程

要使用端口组输入（PORT1到PORT4）：

1. 将ELSRx.ELS[7:0]位设置为00000000b以忽略意外脉冲。有关详细信息，请参阅第19节，事件链接控制器（ELC）。
2. 设置PmnPFS寄存器的EOFEOR位以指定上升沿、下降沿或两个边沿检测。
3. 执行虚拟读取或等待一小段时间，例如100ns。忽略意外脉冲取决于外部引脚的初始值。
4. 设置ELSRx.ELS[8:0]位以启用事件信号。

20.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Output 0 if PCNTR4.EORRn is set to 1 when an ELC_PORT1, 2, 3, or 4 signal occurs.
2. Output 1 if the PCNTR4.EOSRn is set to 1 when an ELC_PORT1, 2, 3, or 4 signal occurs.
3. Output 0 if PCNTR3.PORRn is set to 1.
4. Output 1 if PCNTR3.POSRn is set to 1.
5. Output 0 or 1 because PCNTR1.PODRn is set.
6. Output 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing to the PODR. For example, if 1. and 3. from the list occur at the same time, the higher priority 1. is executed.

20.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and Port Direction bit (PDR) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select register (PmnPFS.ASEL) to 1.

20.5.5 I/O Buffer Specification

When the P402 pin is configured as output or input with the internal pull-up resistor, set the VBTCR1.BPWSWSTP bit to 1 before setting the I/O registers regardless of whether or not the battery backup function is used. This setting is needed only one time after a power-on reset. Clear the VBTCR1.BPWSWSTP bit to 0 again after setting registers associated with the battery backup function, when using the battery backup function.

The setting flow of the VBTCR1.BPWSWSTP bit is shown in Figure 12.2.

The P402 pin can be used as the RTC input pin RTCIC0. When this input pin is enabled by the VBTICTLR register, the output function of this pin is forced to disable. Therefore, the VBTICTLR register must be set to 0 to use the port function.

Note: The VBTICTLR register is not initialized on reset. For more information, see section 12, Battery Backup Function.

20.5.6 Selecting the USB_DP and USB_DM Pins

The USB_DP pin is shared with pin P914. The USB_DM pin is shared with pin P915. USB_DP and P914 pins can be set with the PFS.P914PFS.PMR bit, and USB_DM and P915 pins can be set with the PFS.P915PFS.PMR bit. Table 20.4 shows the setting values of bits PFS.P914PFS.PMR and PFS.P915PFS.PMR with each selected pin.

Table 20.4 Selecting the USB/PORT pins

PMR bit settings		Pins selected	
P914PFS.PMR bit	**P915PFS.PMR bit**	**P914/USB_DP pin**	**P915/USB_DM pin**
0	0	P914	P915
0	1	P914	P915
1	0	P914	P915
1	1	USB_DP	USB_DM

Note: When using P914/USB_DP and P915/USB_DM as GPIO pins (P914 and P915), use the USB registers with their initial values.

Note: When using P914/USB_DP and P915/USB_DM as USB pins (USB_DP and USB_DM), use the GPIO registers for P914 and P915 with their initial values.

Note: When using P914/USB_DP and P915/USB_DM as GPIO pins or USB pins, set these pins only once after a reset.

20.5.3 端口输出数据寄存器(PODR)摘要

该寄存器输出数据如下：

1. 当ELC_PORT1、2、3或4信号出现时，如果PCNTR4.EORRn设置为1，则输出0。
2. 当ELC_PORT1、2、3或4信号出现时，如果PCNTR4.EOSRn设置为1，则输出1。
3. 如果PCNTR3.PORRn设置为1，则输出0。
4. 如果PCNTR3.POSRn设置为1，则输出1。
5. 输出0或1，因为PCNTR1.PODRn已设置。
6. 输出0或1，因为PmnPFS.PODRn已设置。

此列表中的数字对应于写入PODR的优先级。例如，如果列表中的1.和3.同时出现，则执行优先级较高的1.。

20.5.4 使用模拟功能的注意事项

要使用模拟功能，请将端口模式控制位(PMR)和端口方向位(PDR)设置为0，以便引脚用作通用输入端口。接下来，将端口mn引脚功能选择寄存器(PmnPFS.ASEL)中的模拟输入使能位(ASEL)设置为1。

20.5.5 IO缓冲器规格

当P402引脚通过内部上拉电阻配置为输出或输入时，无论是否使用电池备份功能，在设置IO寄存器之前将VBTCR1.BPWSWSTP位设置为1。此设置仅在上电复位后需要一次。使用电池备份功能时，在设置与电池备份功能相关的寄存器后，再次将VBTCR1.BPWSWSTP位清零。

VBTCR1.BPWSWSTP位的设置流程如图12.2所示。

P402引脚可用作RTC输入引脚RTCIC0。当该输入引脚由VBTICTLR寄存器使能时，该引脚的输出功能被强制禁用。因此，必须将VBTICTLR寄存器设置为0才能使用端口功能。

Note: VBTICTLR寄存器在复位时未初始化。有关详细信息，请参阅第12节，备用电池Function.

20.5.6 选择USB_DP和USB_DM引脚

USB_DP引脚与引脚P914共享。USB_DM引脚与引脚P915共享。USB_DP和P914引脚可以通过PFS.P914PFS.PMR位设置，USB_DM和P915引脚可以通过PFS.P915PFS.PMR位设置。表20.4显示了每个选定引脚的PFS.P914PFS.PMR和PFS.P915PFS.PMR位的设置值。

Table 20.4 选择USB端口引脚

PMR位设置		选择的引脚	
P914PFS.PMR bit	**P915PFS.PMR bit**	**P914/USB_DP pin**	**P915/USB_DM pin**
0	0	P914	P915
0	1	P914	P915
1	0	P914	P915
1	1	USB_DP	USB_DM

Note: 当使用P914USB_DP和P915USB_DM作为GPIO引脚（P914和P915）时，使用带有初始值的USB寄存器。

Note: 当使用P914USB_DP和P915USB_DM作为USB引脚（USB_DP和USB_DM）时，使用P914和P915的GPIO寄存器及其初始值。

Note: 当使用P914USB_DP和P915USB_DM作为GPIO管脚或USB管脚时，复位后这些管脚只设置一次。

20.5.7 Pull-up/Pull-down Setting for P914 and P915 using USBFS/GPIO Function

When P914 and P915 are used as GPIO pins, their operation is affected by the pull-up/pull-down function of the USBFS registers.

Therefore, before using the GPIO function, disable the pull-up and pull-down control of the USBFS registers using the SYSCFG.DMRPU, SYSCFG.DPRPU, and SYSCFG.DRPD bits.

20.6 Peripheral Select Settings for each Product

This section describes the pin function select configuration by the PmnPFS register. Assigning the same function to two or more pins simultaneously is prohibited.

Table 20.5 Register settings for I/O pin functions (PORT0)

PSEL[4:0] bit settings	Function	Pin				
		P004	P010	P011	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
01100b	CTSU	—	TS30	TS31	—	TS28
ASEL bit		AN004/ AMP2O	AN005/ VREFH0/ AMP2-	AN006/ VREFL0/ AMP2+	AN009/ DA0	AN010
ISEL bit		IRQ3	IRQ14	IRQ15	—	IRQ7
PCR bit		✓	✓	✓	✓	✓
DSCR bit		L/M	L/M	L/M	L/M	L/M

✓: Available
—: Setting prohibited

20.5.7 使用USBFSGPIO功能的P914和P915的上拉下拉设置

当P914和P915用作GPIO引脚时，它们的操作受USBFS寄存器的上拉下拉功能影响。

因此，在使用GPIO功能之前，请使用以下命令禁用USBFS寄存器的上拉和下拉控制SYSCFG.DMRPU、SYSCFG.DPRPU和SYSCFG.DRPD位。

20.6 每个产品的外设选择设置

本节介绍PmnPFS寄存器的引脚功能选择配置。禁止将相同的功能同时分配给两个或多个引脚。

Table 20.5 IO引脚功能的寄存器设置(PORT0)

PSEL[4:0]位设置	Function	Pin				
		P004	P010	P011	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
01100b	CTSU	—	TS30	TS31	—	TS28
ASEL bit		AN004/ AMP2O	AN005/ VREFH0/ AMP2-	AN006/ VREFL0/ AMP2+	AN009/ DA0	AN010
ISEL bit		IRQ3	IRQ14	IRQ15	—	IRQ7
PCR bit		✓	✓	✓	✓	✓
DSCR bit		L/M	L/M	L/M	L/M	L/M

:可用—:禁止设置

Table 20.6 Register settings for I/O pin functions (PORT1) (1)

PSEL[4:0] bit settings	Function	Pin P100	P101	P102	P103	P104	P105	P106	P107
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO0	AGTEE0	AGTO0	—	—	—	—	—
00010b	GPT	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—
00011b	GPT	GTIOC5B	GTIOC5A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A
00100b	SCI	RXD0/ MISO0/ SCL0	TXD0/ MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	RXD0/ MISO0/ SCL0	—	—	—
00101b	SCI	SCK1	CTS1_RTS1/ SS1	TXD2/ MOSI2/ SDA2	—	—	—	—	—
00110b	SPI	MISOA	MOSIA	RSPCKA	SSLA0	SSLA1	SSLA2	SSLA3	—
00111b	IIC	SCL1	SDA1	—	—	—	—	—	—
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT/ ACMPLP/ RTC	—	—	—	—	—	—	—	—
01010b	CAC/ADC14	—	—	ADTRG0	—	—	—	—	—
01100b	CTSU	—	—	—	—	TS13	TS34	—	—
01101b	SLCDC	VL1	VL2	—	VL4	COM0	COM1	COM2	COM3
10000h	CAN	—	—	CRX0	CTX0	—	—	—	—
ASEL bit		CMPIN0	CMPREF0	AN020/ CMPIN1	AN019/ CMPREF1	—	—	—	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—
NCODR bit		✓	✓	✓	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓
DSCR bit		L/M	L/M	L/M	L/M	L/M	L/M	L/M	L/M

✓: Available
—: Setting prohibited

Table 20.6 IO引脚功能的寄存器设置(PORT1)(1)

PSEL[4:0]位设置	Function	Pin P100	P101	P102	P103	P104	P105	P106	P107
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO0	AGTEE0	AGTO0	—	—	—	—	—
00010b	GPT	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—
00011b	GPT	GTIOC5B	GTIOC5A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A
00100b	SCI	RXD0/ MISO0/ SCL0	TXD0/ MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	RXD0/ MISO0/ SCL0	—	—	—
00101b	SCI	SCK1	CTS1_RTS1/ SS1	TXD2/ MOSI2/ SDA2	—	—	—	—	—
00110b	SPI	MISOA	MOSIA	RSPCKA	SSLA0	SSLA1	SSLA2	SSLA3	—
00111b	IIC	SCL1	SDA1	—	—	—	—	—	—
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT/ ACMPLP/ RTC	—	—	—	—	—	—	—	—
01010b	CAC/ADC14	—	—	ADTRG0	—	—	—	—	—
01100b	CTSU	—	—	—	—	TS13	TS34	—	—
01101b	SLCDC	VL1	VL2	—	VL4	COM0	COM1	COM2	COM3
10000h	CAN	—	—	CRX0	CTX0	—	—	—	—
ASEL bit		CMPIN0	CMPREF0	AN020/ CMPIN1	AN019/ CMPREF1	—	—	—	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—
NCODR bit		✓	✓	✓	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓
DSCR bit		L/M	L/M	L/M	L/M	L/M	L/M	L/M	L/M

:可用—:禁止设置

Table 20.7 Register settings for I/O pin functions (PORT1) (2)

PSEL[4:0] bit settings	Function	Pin P108	P109	P110	P111
00000b (value after reset)	Hi-Z/JTAG/SWD	TMS/ SWDIO	TDO/ TRACESWO	TDI	Hi-Z
00001b	AGT	—	—	—	—
00010b	GPT	GTOULO	GTOVUP	GTOVLO	—
00011b	GPT	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC3A
00100b	SCI	—	SCK1	CTS2_RTS2/ SS2	SCK2
00101b	SCI	CTS9_RTS9/ SS9	TXD9/ MOSI9/ SDA9	RXD9/ MISO9/ SCL9	SCK9
00110b	SPI	SSLB0	MOSIB	MISOB	RSPCKB
00111b	IIC	—	—	—	—
01000b	KINT	—	—	—	—
01001b	CLKOUT/ ACMPLP/ RTC	—	CLKOUT	VCOUT	—
01010b	CAC/ADC14	—	—	—	—
01100b	CTSU	—	TS10	—	TS12
01101b	SLCDC	—	SEG52	SEG53	—
10000b	CAN	—	CTX0	CRX0	—
ASEL bit		—	—	—	—
ISEL bit		—	—	IRQ3	IRQ4
NCODR bit		✓	✓	✓	✓
PCR bit		✓	✓	✓	✓
DSCR bit		L/M	L/M	L/M	L/M

✓: Available
—: Setting prohibited

Table 20.7 IO引脚功能的寄存器设置(PORT1)(2)

PSEL[4:0]位设置	Function	Pin P108	P109	P110	P111
00000b (value after reset)	Hi-Z/JTAG/SWD	TMS/ SWDIO	TDO/ TRACESWO	TDI	Hi-Z
00001b	AGT	—	—	—	—
00010b	GPT	GTOULO	GTOVUP	GTOVLO	—
00011b	GPT	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC3A
00100b	SCI	—	SCK1	CTS2_RTS2/ SS2	SCK2
00101b	SCI	CTS9_RTS9/ SS9	TXD9/ MOSI9/ SDA9	RXD9/ MISO9/ SCL9	SCK9
00110b	SPI	SSLB0	MOSIB	MISOB	RSPCKB
00111b	IIC	—	—	—	—
01000b	KINT	—	—	—	—
01001b	CLKOUT/ ACMPLP/ RTC	—	CLKOUT	VCOUT	—
01010b	CAC/ADC14	—	—	—	—
01100b	CTSU	—	TS10	—	TS12
01101b	SLCDC	—	SEG52	SEG53	—
10000b	CAN	—	CTX0	CRX0	—
ASEL bit		—	—	—	—
ISEL bit		—	—	IRQ3	IRQ4
NCODR bit		✓	✓	✓	✓
PCR bit		✓	✓	✓	✓
DSCR bit		L/M	L/M	L/M	L/M

:可用—:禁止设置

Table 20.8 Register settings for I/O pin functions (PORT2) (1)

PSEL[4:0] bit settings	Function	Pin P200	P201	P204	P205	P206
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00001b	AGT	—	—	AGTIO1	AGTO1	—
00010b	GPT	—	—	GTIW	GTIV	GTIU
00011b	GPT	—	—	GTIOC4B	GTIOC4A	—
00100b	SCI	—	—	SCK4	TXD4/ MOSI4/ SDA4	RXD4/ MISO4/ SCL4
00101b	SCI	—	—	SCK9	CTS9_RTS9/ SS9	—
00110b	SPI	—	—	RSPCKB	SSLB0	SSLB1
00111b	IIC	—	—	SCL0	SCL1	SDA1
01001b	CLKOUT/ ACMPLP/ RTC	—	—	—	CLKOUT	—
01010b	CAC/ADC14	—	—	CACREF	—	—
01100b	CTSU	—	—	TS00	TSCAP	TS01
01101b	SLCDC	—	—	SEG23	SEG20	SEG12
10011b	USBFS	—	—	USB_OVRCURB	USB_OVRCURA	USB_VBUSEN A
ISEL bit		NMI	—	—	IRQ1	IRQ0
NCODR bit		—	✓	✓	✓	✓
PCR bit		—	✓	✓	✓	✓
DSCR bit		—	L/M	L/M	L/M	L/M

✓: Available
—: Setting prohibited

Table 20.8 IO引脚功能的寄存器设置(PORT2)(1)

PSEL[4:0]位设置	Function	Pin P200	P201	P204	P205	P206
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00001b	AGT	—	—	AGTIO1	AGTO1	—
00010b	GPT	—	—	GTIW	GTIV	GTIU
00011b	GPT	—	—	GTIOC4B	GTIOC4A	—
00100b	SCI	—	—	SCK4	TXD4/ MOSI4/ SDA4	RXD4/ MISO4/ SCL4
00101b	SCI	—	—	SCK9	CTS9_RTS9/ SS9	—
00110b	SPI	—	—	RSPCKB	SSLB0	SSLB1
00111b	IIC	—	—	SCL0	SCL1	SDA1
01001b	CLKOUT/ ACMPLP/ RTC	—	—	—	CLKOUT	—
01010b	CAC/ADC14	—	—	CACREF	—	—
01100b	CTSU	—	—	TS00	TSCAP	TS01
01101b	SLCDC	—	—	SEG23	SEG20	SEG12
10011b	USBFS	—	—	USB_OVRCURB	USB_OVRCURA	USB_VBUSEN A
ISEL bit		NMI	—	—	IRQ1	IRQ0
NCODR bit		—	✓	✓	✓	✓
PCR bit		—	✓	✓	✓	✓
DSCR bit		—	L/M	L/M	L/M	L/M

:可用—:禁止设置

Table 20.9 Register settings for I/O pin functions (PORT2) (2)

PSEL[4:0] bit settings	Function	Pin P212	P213	P214	P215
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z			
00001b	AGT	AGTEE1	—	—	—
00010b	GPT	GTETRGB	GTETRGA	—	—
00011b	GPT	GTIOC0B	GTIOC0A	—	—
00100b	SCI	—	—	—	—
00101b	SCI	RXD1/ MISO1/ SCL1	TXD1/ MOSI1/ SDA1	—	—
00110b	SPI	—	—	—	—
00111b	IIC	—	—	—	—
01001b	CLKOUT/ ACMPLP/ RTC	—	—	—	—
01010b	CAC/ADC14	—	—	—	—
01100b	CTSU	—	—	—	—
01101b	SLCDC	—	—	—	—
10011b	USBFS	—	—	—	—
ISEL bit		IRQ3	IRQ2	—	—
NCODR bit		✓	✓	—	—
PCR bit		✓	✓	—	—
DSCR bit		—	—	—	—

✓: Available
—: Setting prohibited

Table 20.9 IO引脚功能的寄存器设置(PORT2)(2)

PSEL[4:0]位设置	Function	Pin P212	P213	P214	P215
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z			
00001b	AGT	AGTEE1	—	—	—
00010b	GPT	GTETRGB	GTETRGA	—	—
00011b	GPT	GTIOC0B	GTIOC0A	—	—
00100b	SCI	—	—	—	—
00101b	SCI	RXD1/ MISO1/ SCL1	TXD1/ MOSI1/ SDA1	—	—
00110b	SPI	—	—	—	—
00111b	IIC	—	—	—	—
01001b	CLKOUT/ ACMPLP/ RTC	—	—	—	—
01010b	CAC/ADC14	—	—	—	—
01100b	CTSU	—	—	—	—
01101b	SLCDC	—	—	—	—
10011b	USBFS	—	—	—	—
ISEL bit		IRQ3	IRQ2	—	—
NCODR bit		✓	✓	—	—
PCR bit		✓	✓	—	—
DSCR bit		—	—	—	—

:可用—:禁止设置

Table 20.10 Register settings for I/O pin functions (PORT3)

PSEL[4:0] bit settings	Function	Pin P300
00000b (value after reset)	Hi-Z/JTAG/SWD	TCK/ SWCLK
00001b	AGT	—
00010b	GPT	GTOUUP
00011b	GPT	GTIOC0A
00110b	SPI	SSLB1
ISEL bit		—
NCODR bit		✓
PCR bit		✓
DSCR bit		L/M

✓: Available
—: Setting prohibited

Table 20.11 Register settings for I/O pin functions (PORT4) (1)

PSEL[4:0] bit settings	Function	Pin P402	P404	P407
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
00001b	AGT	AGTIO0*2/ AGTIO1*2	—	AGTIO0
00010b	GPT	—	—	—
00011b	GPT	—	GTIOC3B	—
00100b	SCI	—	—	CTS4_RTS4/ SS4
00101b	SCI	RXD1/ MISO1/ SCL1	—	—
00110b	SPI	—	—	SSLB3
00111b	IIC	—	—	SDA0
01001b	CLKOUT/ ACMPLP/ RTC	—	—	RTCOUT
01010b	CAC/ADC14	—	—	ADTRG0
01100b	CTSU	TS18	—	TS03
01101b	SLCDC	SEG06	—	SEG11
10000b	CAN	CRX0	—	—
10011b	USBFS	—	—	USB_VBUS
Don't care		RTCIC0*1	—	—
ISEL bit		IRQ4	—	—
NCODR bit		✓	✓	✓
PCR bit		✓	✓	✓
DSCR bit		L/M	L/M	L/M

✓: Available
—: Setting prohibited

Note 1. To use this pin function, set the corresponding pin as general input (set the PmnPFS.PDR and PmnPFS.PMR bits to 0).
Note 2. To use this pin function, set the PmnPFS.PSEL[4:0] bits and the AGTIOSEL.SEL[1:0] bits (described in section 24, AGT Pin Select Register (AGTIOSEL)).

Table 20.10 IO引脚功能的寄存器设置(PORT3)

PSEL[4:0]位设置	Function	Pin P300
00000b (value after reset)	Hi-Z/JTAG/SWD	TCK/ SWCLK
00001b	AGT	—
00010b	GPT	GTOUUP
00011b	GPT	GTIOC0A
00110b	SPI	SSLB1
ISEL bit		—
NCODR bit		✓
PCR bit		✓
DSCR bit		L/M

:可用—:禁止设置

Table 20.11 IO引脚功能的寄存器设置(PORT4)(1)

PSEL[4:0]位设置	Function	Pin P402	P404	P407
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
00001b	AGT	AGTIO0*2/ AGTIO1*2	—	AGTIO0
00010b	GPT	—	—	—
00011b	GPT	—	GTIOC3B	—
00100b	SCI	—	—	CTS4_RTS4/ SS4
00101b	SCI	RXD1/ MISO1/ SCL1	—	—
00110b	SPI	—	—	SSLB3
00111b	IIC	—	—	SDA0
01001b	CLKOUT/ ACMPLP/ RTC	—	—	RTCOUT
01010b	CAC/ADC14	—	—	ADTRG0
01100b	CTSU	TS18	—	TS03
01101b	SLCDC	SEG06	—	SEG11
10000b	CAN	CRX0	—	—
10011b	USBFS	—	—	USB_VBUS
Don't care		RTCIC0*1	—	—
ISEL bit		IRQ4	—	—
NCODR bit		✓	✓	✓
PCR bit		✓	✓	✓
DSCR bit		L/M	L/M	L/M

:可用—:禁止设置

Note 1. 要使用此引脚功能，请将相应引脚设置为通用输入（将PmnPFS.PDR和PmnPFS.PMR位设置为0）。
Note 2. 要使用此引脚功能，请设置PmnPFS.PSEL[4:0]位和AGTIOSEL.SEL[1:0]位（在第24节，AGT引脚中描述选择注册(AGTISEL)）。

Table 20.12 Register settings for I/O pin functions (PORT4) (2)

PSEL[4:0] bit settings	Function	Pin	
		P409	P414
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00001b	AGT	—	—
00010b	GPT	GTOWUP	—
00011b	GPT	GTIOC5A	GTIOC0B
00100b	SCI	—	—
00101b	SCI	—	—
00110b	SPI	—	SSLA1
00111b	IIC	—	—
01001b	CLKOUT/ ACMPLP/ RTC	—	—
01010b	CAC/ADC14	—	—
01100b	CTSU	—	—
01101b	SLCDC	SEG09	—
10000b	CAN	—	—
10011b	USBFS	—	—
Don't care		—	—
ISEL bit		IRQ6	IRQ9
NCODR bit		✓	✓
PCR bit		✓	✓
DSCR bit		L/M	L/M

✓: Available
—: Setting prohibited

Note: To use this pin function, set the corresponding pin as general input (set the PmnPFS.PDR and PmnPFS.PMR bits to 0).
Note: To use this pin function, set the PmnPFS.PSEL[4:0] bits and the AGTIOSEL.SEL[1:0] bits (described in section 24, AGT Pin Select Register (AGTIOSEL)).

Table 20.12 IO引脚功能的寄存器设置(PORT4)(2)

PSEL[4:0]位设置	Function	Pin	
		P409	P414
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00001b	AGT	—	—
00010b	GPT	GTOWUP	—
00011b	GPT	GTIOC5A	GTIOC0B
00100b	SCI	—	—
00101b	SCI	—	—
00110b	SPI	—	SSLA1
00111b	IIC	—	—
01001b	CLKOUT/ ACMPLP/ RTC	—	—
01010b	CAC/ADC14	—	—
01100b	CTSU	—	—
01101b	SLCDC	SEG09	—
10000b	CAN	—	—
10011b	USBFS	—	—
Don't care		—	—
ISEL bit		IRQ6	IRQ9
NCODR bit		✓	✓
PCR bit		✓	✓
DSCR bit		L/M	L/M

:可用一:禁止设置

Note: 要使用此引脚功能，请将相应引脚设置为通用输入（将PmnPFS.PDR和PmnPFS.PMR位设置为0）。
Note: 要使用此引脚功能，请设置PmnPFS.PSEL[4:0]位和AGTIOSEL.SEL[1:0]位（在第24节，AGT引脚中描述选择注册(AGTISEL))。

Table 20.13 Register settings for I/O pin functions (PORT5)

PSEL[4:0] bit settings	Function	Pin P501
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z
00001b	AGT	AGTOB0
00010b	GPT	GTIV
00011b	GPT	GTIOC2B
01101b	SLCDC	SEG49
10011b	USBFS	USB_OVRCURA
ASEL bit		AN017/ CMPIN1
ISEL bit		IRQ11
NCODR bit		✓
PCR bit		✓
DSCR bit		L/M

✓: Available
—: Setting prohibited

Table 20.14 Register settings for I/O pin functions (PORT9)

PSEL[4:0] bit settings	Function	Pin P914	P915
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00001b	AGT	—	—
00100b	SCI	—	—
01011b	BUS	—	—
Don't care		(USB_DP)	(USB_DM)
NCODR bit		—	—
PCR bit		—	—
DSCR bit		—	—

✓: Available
—: Setting prohibited

Table 20.13 IO引脚功能的寄存器设置(PORT5)

PSEL[4:0]位设置	Function	Pin P501
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z
00001b	AGT	AGTOB0
00010b	GPT	GTIV
00011b	GPT	GTIOC2B
01101b	SLCDC	SEG49
10011b	USBFS	USB_OVRCURA
ASEL bit		AN017/ CMPIN1
ISEL bit		IRQ11
NCODR bit		✓
PCR bit		✓
DSCR bit		L/M

:可用—:禁止设置

Table 20.14 IO引脚功能的寄存器设置(PORT9)

PSEL[4:0]位设置	Function	Pin P914	P915
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00001b	AGT	—	—
00100b	SCI	—	—
01011b	BUS	—	—
Don't care		(USB_DP)	(USB_DM)
NCODR bit		—	—
PCR bit		—	—
DSCR bit		—	—

:可用—:禁止设置

21. Key Interrupt Function (KINT)

21.1 Overview

A key interrupt (KEY_INTKR) can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins, KR00 to KR07.

Table 21.1 shows the assignment for key interrupt detection, Table 21.2 shows the function configuration, and Figure 21.1 shows a block diagram.

Table 21.1 Assignment of key interrupt detection pins

Flag	Description
KRM0	Controls KR00 signal in 1-bit units
KRM1	Controls KR01 signal in 1-bit units
KRM2	Controls KR02 signal in 1-bit units
KRM3	Controls KR03 signal in 1-bit units
KRM4	Controls KR04 signal in 1-bit units
KRM5	Controls KR05 signal in 1-bit units
KRM6	Controls KR06 signal in 1-bit units
KRM7	Controls KR07 signal in 1-bit units

Table 21.2 Configuration of key interrupt function

Parameter	Configuration
Input	KR00 to KR07
Control registers	Key Return Control register (KRCTL) Key Return Mode register (KRM) Key Return Flag register (KRF)

21. 按键中断功能(KINT)

21.1 Overview

按键中断(KEY_INTKR)可通过设置按键返回模式寄存器(KRM)并向按键中断输入引脚KR00至KR07输入上升沿或下降沿来产生。

表21.1显示按键中断检测的分配，表21.2显示功能配置，图21.1显示框图。

Table 21.1 按键中断检测引脚的分配

Flag	Description
KRM0	以1位为单位控制KR00信号
KRM1	以1位为单位控制KR01信号
KRM2	以1位为单位控制KR02信号
KRM3	以1位为单位控制KR03信号
KRM4	以1位为单位控制KR04信号
KRM5	以1位为单位控制KR05信号
KRM6	以1位为单位控制KR06信号
KRM7	以1位为单位控制KR07信号

Table 21.2 按键中断功能配置

Parameter	Configuration
Input	KR00 to KR07
控制寄存器	密钥返回控制寄存器(KRCTL) 密钥返回模式寄存器(KRM) 键返回标志寄存器(KRF)

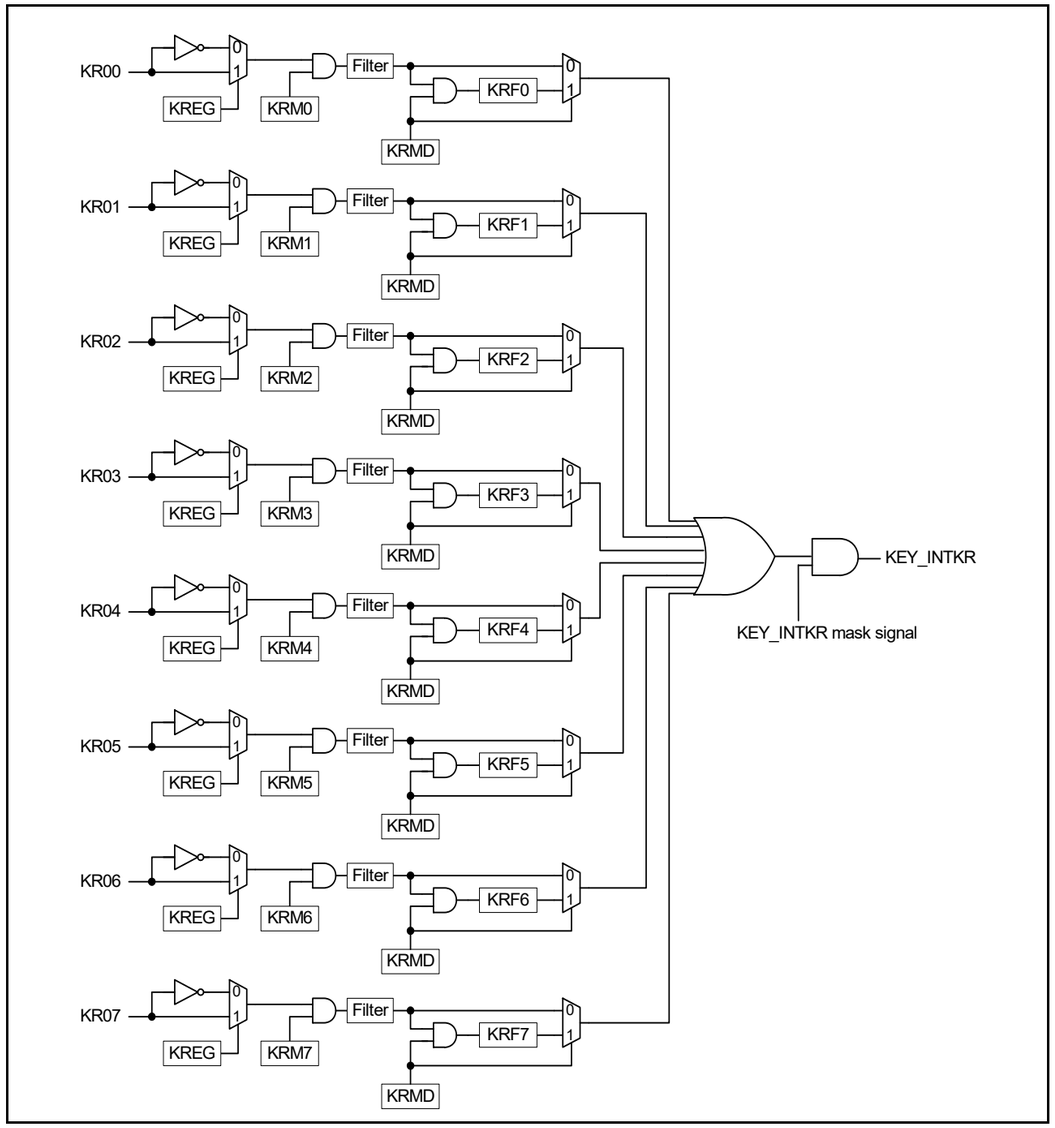


Figure 21.1 Key interrupt function block diagram

In Figure 21.1, all key return factors are merged by an OR gate, and the key interrupt (KEY_INTKR) is the output of the AND gate to mask the merged key return factor by the KEY_INTKR mask signal. When using KRFn (KRMD = 1), the KEY_INTKR mask signal is used as the output mask that is asserted by clearing KRFn.

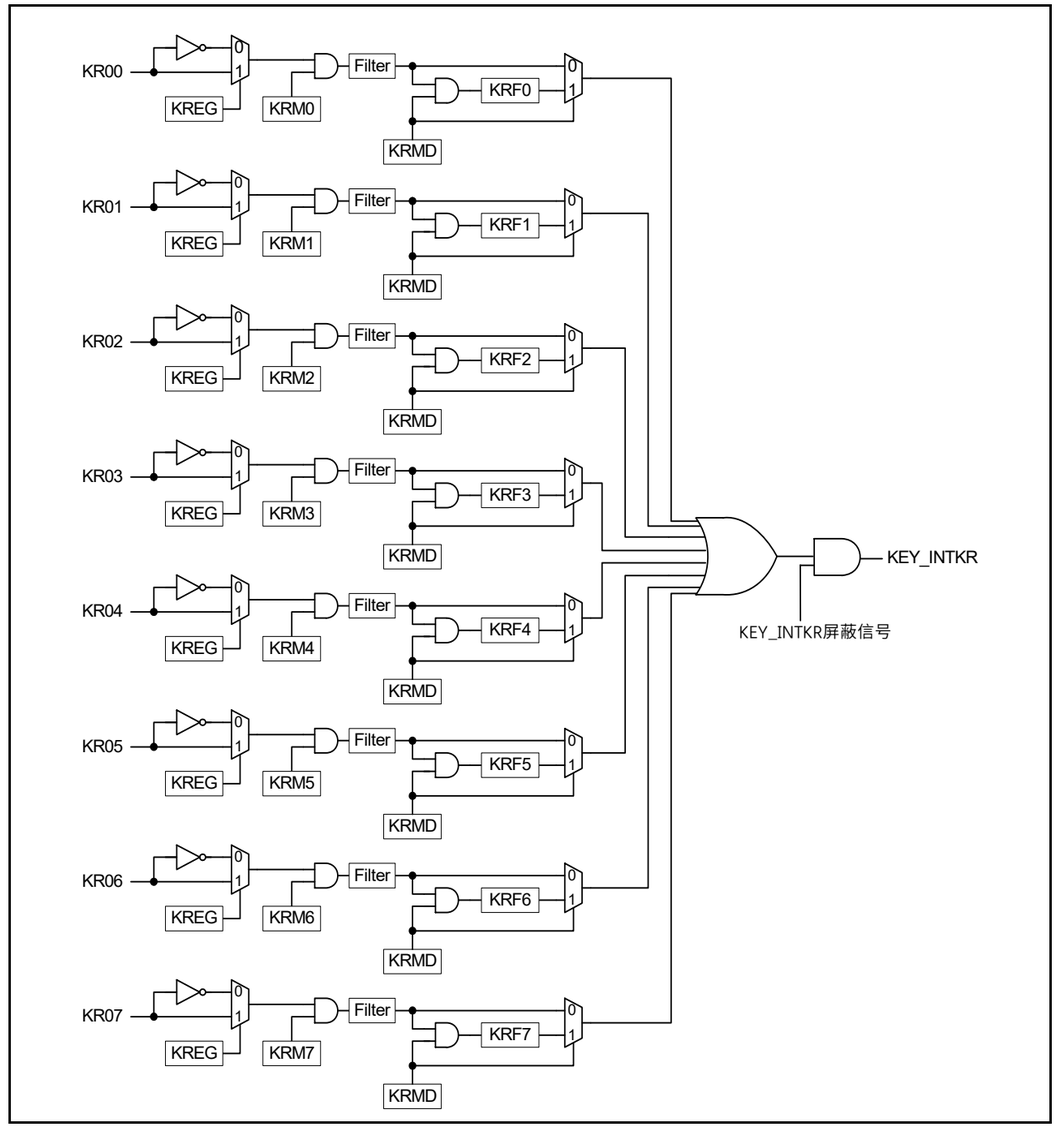


Figure 21.1 按键中断功能框图

在图21.1中，所有的键返回因子由一个或门合并，键中断（KEY_INTKR）是与门的输出，用于通过KEY_INTKR屏蔽信号屏蔽合并的键返回因子。当使用KRFn(KRMD=1)时，
KEY_INTKR掩码信号用作通过清除KRFn断言的输出掩码。

21.2 Register Descriptions

21.2.1 Key Return Control Register (KRCTL)

Address(es): KINT.KRCTL 4008 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRMD	—	—	—	—	—	—	KREG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	KREG	Selection of Detection Edge (KR00 to KR07)	0: Falling edge 1: Rising edge.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	KRMD	Usage of Key Interrupt Flags (KRF0 to KRF7)	0: Do not use key interrupt flags 1: Use key interrupt flags.	R/W

The KRCTL register controls the usage of the key interrupt flags, KRF0 to KRF7, and sets the detection edge.

21.2.2 Key Return Flag Register (KRF)

Address(es): KINT.KRF 4008 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRFn	Key Interrupt Flag n	0: No key interrupt detected 1: Key interrupt detected.	R/W

n = 0 to 7

Note: When KRMD = 0, setting the KRFn bit to 1 is prohibited.
When setting the KRFn bit to 1, the KRFn value does not change. To clear the KRFn bit, confirm that the target bit is 1 before writing 0 to the bit, then write 1 to the other bits.

The KRF register controls the key interrupt flags, KRF0 to KRF7.

21.2.3 Key Return Mode Register (KRM)

Address(es): KINT.KRM 4008 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRMn	Key Interrupt Mode Control n	0: No key interrupt signal detected 1: Key interrupt signal detected.	R/W

n = 0 to 7

21.2 注册说明

21.2.1 密钥返回控制寄存器(KRCTL)

Address(es): KINT.KRCTL 4008 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRMD	—	—	—	—	—	—	KREG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	KREG	检测边缘的选择（KR00至KR07）	0：下降沿1： 上升沿。	R/W
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	KRMD	按键中断标志（KRF0到KRF7）的使用	0：不使用按键中断标志1：使 用按键中断标志。	R/W

KRCTL寄存器控制按键中断标志KRF0到KRF7的使用，并设置检测沿。

21.2.2 密钥返回标志寄存器(KRF)

Address(es): KINT.KRF 4008 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	KRFn	按键中断标志n	0：未检测到按键中断1：检 测到按键中断。	R/W

n = 0 to 7

Note: 当KRMD=0时，禁止将KRFn位设置为1。
将KRFn位设置为1时，KRFn值不变。要清除KRFn位，在向该位写入0之前确认目标位为1，然后向其他位写入1。

KRF寄存器控制关键中断标志，KRF0到KRF7。

21.2.3 密钥返回模式寄存器(KRM)

Address(es): KINT.KRM 4008 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	KRMn	按键中断模式控制n	0：未检测到按键中断信号1：检 测到按键中断信号。	R/W

n = 0 to 7

Note: The on-chip pull-up resistors can be applied by setting the associated key interrupt input pin in the pull-up resistor. For details, see section 20, I/O Ports.
Key interrupts can be assigned in the PmnPFS.PSEL bits. For more information, see section 20, I/O Ports.
An interrupt is generated when the target bit in the KRM register is set while a low level (KREG is set to 0) or a high level (KREG is set to 1) is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling the interrupt handling.

The KRM register sets the key interrupt mode.

21.3 Operation

21.3.1 Operation When Not Using Key Interrupt Flag (KRMD = 0)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channel to which the valid edge is input, read the port register and check the port level after the key interrupt (KEY_INTKR) is generated.

The KEY_INTKR signal changes based on the input level of the key interrupt input pin, KR00 to KR07.

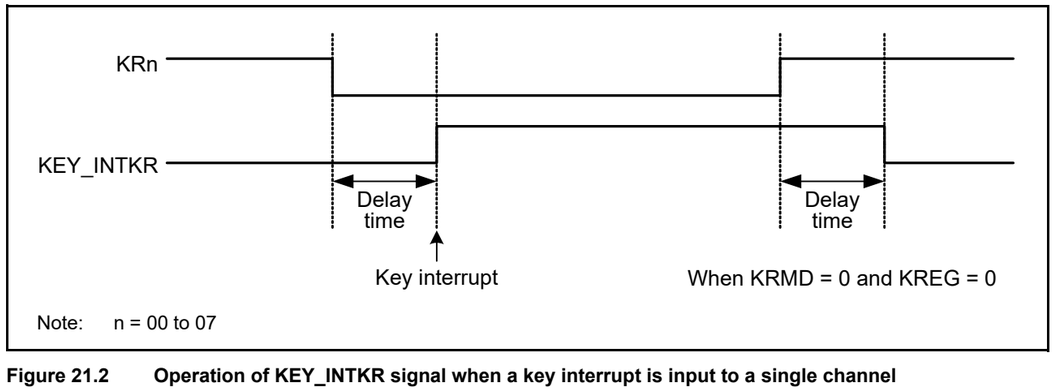


Figure 21.2 Operation of KEY_INTKR signal when a key interrupt is input to a single channel

Figure 21.3 shows the operation when a valid edge is input to multiple key interrupt input pins. The KEY_INTKR signal is set while a low level is being input to one pin, that is, when KREG is set to 0. Therefore, even if a falling edge is input to another pin in this period, a key interrupt (KEY_INTKR) is not generated again. See [1] in Figure 21.3.

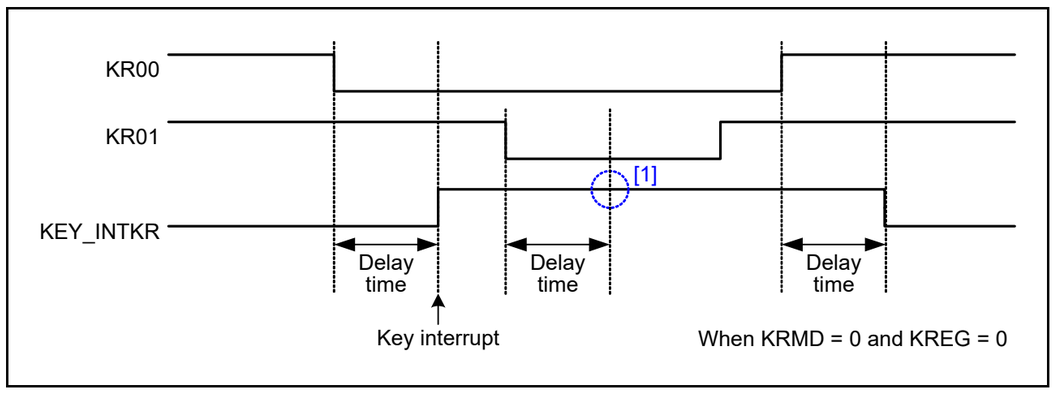


Figure 21.3 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

21.3.2 Operation When Using Key Interrupt Flag (KRMD = 1)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channels to which the valid edge is input, read the Key Return Flag register (KRF) after

Note: 可以通过设置上拉电阻中的相关按键中断输入引脚来应用片上上拉电阻。有关详细信息，请参阅第20节，IO端口。可以在PmnPFS.PSEL位中分配键中断。有关详细信息，请参阅第20节，IO端口。

当低电平（KREG设置为0）或高电平（KREG设置为1）输入到按键中断输入引脚时，如果KRM寄存器中的目标位被置位，则会产生中断。要忽略此中断，请在禁用中断处理后设置KRM寄存器。

KRM寄存器设置按键中断模式。

21.3 Operation

21.3.1 不使用按键中断标志(KRMD=0)时的操作

当KREG位中指定的有效边沿输入到按键中断引脚时，将产生按键中断(KEY_INTKR)，KR00至KR07。要识别输入有效边沿的通道，读取端口寄存器并在按键中断（KEY_INTKR）产生后检查端口电平。

KEY_INTKR信号根据按键中断输入引脚KR00至KR07的输入电平而变化。

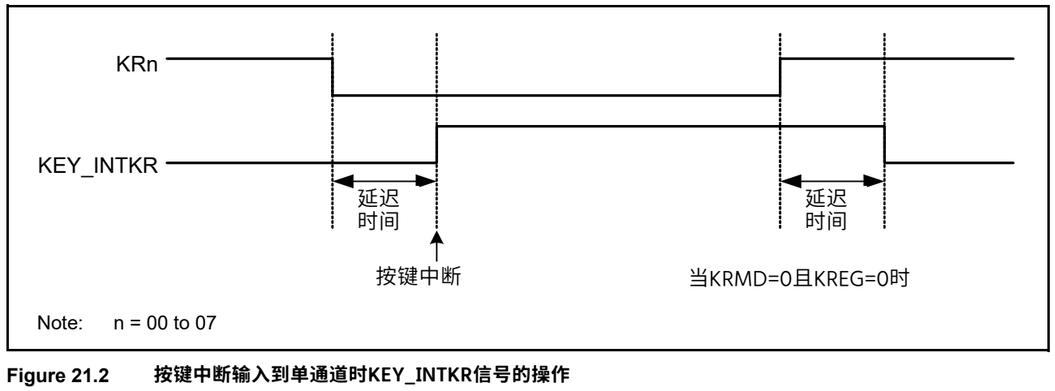


Figure 21.2 按键中断输入到单通道时KEY_INTKR信号的操作

图21.3显示了向多个按键中断输入引脚输入有效边沿时的操作。KEY_INTKR信号在一个引脚输入低电平时置位，即当KREG设置为0时。因此，即使在此期间向另一个引脚输入下降沿，按键中断(KEY_INTKR)也不会发生。再次生成。参见图21.3中的[1]。

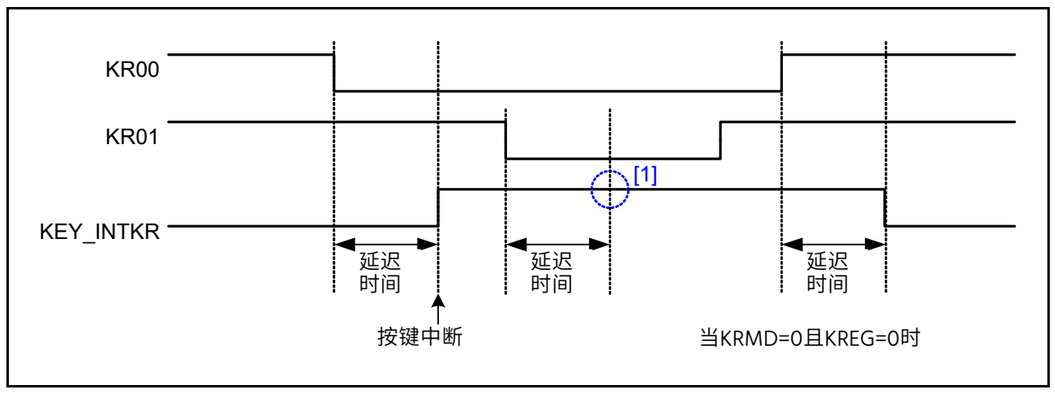


Figure 21.3 按键中断输入到多个通道时KEY_INTKR信号的操作

21.3.2 使用按键中断标志(KRMD=1)时的操作

当KREG位中指定的有效边沿输入到按键中断引脚KR00至KR07时，将产生按键中断(KEY_INTKR)。要识别输入有效边沿的通道，请在之后读取密钥返回标志寄存器(KRF)

the key interrupt (KEY_INTKR) is generated. If the KRMD bit is set to 1, clear the KEY_INTKR signal by clearing the associated bit in the KRF register.

As Figure 21.4 shows, only one interrupt is generated each time a falling edge is input to one channel, that is, when KREG = 0, regardless of whether the KRFn bit is cleared before or after a rising edge is input.

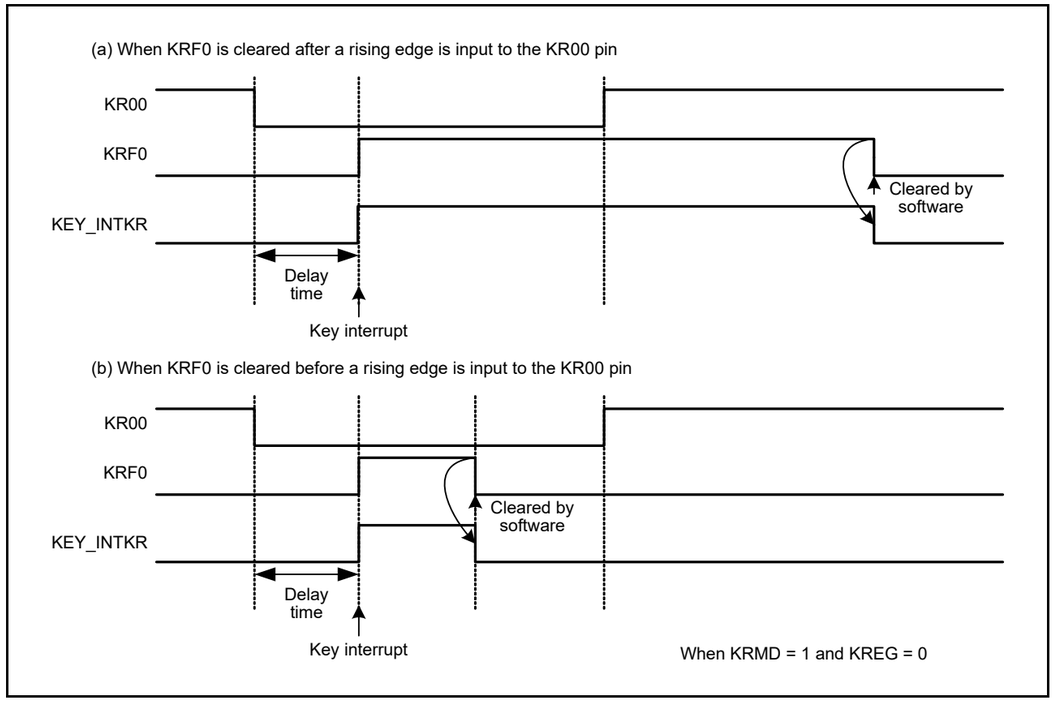


Figure 21.4 Basic operation of KEY_INTKR signal when key interrupt flag is used

Figure 21.5 shows the operation when a valid edge is input to multiple key interrupt input pins. A falling edge is also input to the KR01 and KR05 pins after a falling edge is input to the KR00 pin, that is, when KREG = 0. The KRF1 bit is set when the KRF0 bit is cleared. A key interrupt generates 1 PCLKB clock cycle, after the KRF0 bit is cleared. See [1] in Figure 21.5. Also, after a falling edge is input to the KR05 pin, the KRF5 bit is set. See [2] in the figure when the KRF1 bit is cleared. A key interrupt generates 1 PCLKB clock cycle, after the KRF1 bit is cleared. See [3] in the figure. It is therefore possible to generate a key interrupt when a valid edge is input to multiple channels.

生成密钥中断（KEY_INTKR）。如果KRMD位设置为1，则通过清除KRF寄存器中的相关位来清除KEY_INTKR信号。

如图21.4所示，每次下降沿输入到一个通道时，只产生一个中断，即当KREG=0，无论KRFn位是在输入上升沿之前还是之后清零。

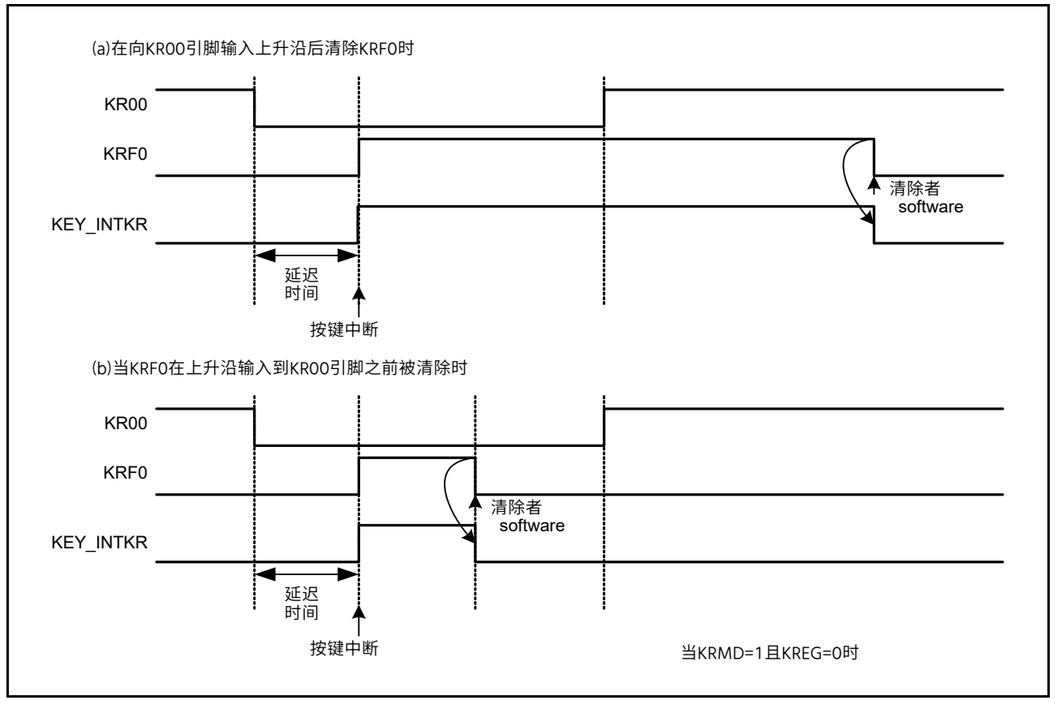


Figure 21.4 使用按键中断标志时KEY_INTKR信号的基本操作

图21.5显示了有效边沿输入到多个按键中断输入引脚时的操作。在KR00引脚输入下降沿后，即KREG=0时，KR01和KR05引脚也输入一个下降沿。当KRF0位清零时，KRF1位被置位。在KRF0位清零后，按键中断产生1个PCLKB时钟周期。请参见图21.5中的[1]。此外，在向KR05引脚输入下降沿后，KRF5位被置位。当KRF1位清零时，请参见图中的[2]。在KRF1位清零后，按键中断产生1个PCLKB时钟周期。见图[3]。

因此，当有效边沿输入到多个通道时，可能会产生按键中断。

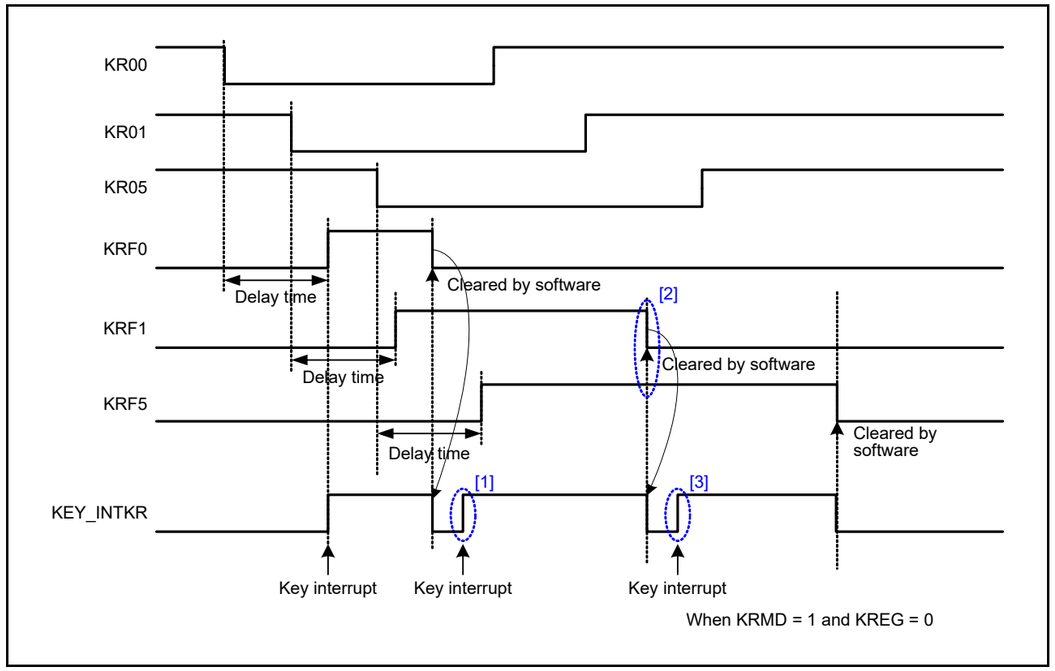


Figure 21.5 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

21.4 Usage Notes

- If KEY_INTKR is used as the snooze request, the KRMD bit must be set to 0.
- If KEY_INTKR is used as the interrupt source for returning to Normal mode from Snooze and Software Standby modes, the KRMD bit must be set to 1.
- When the key interrupt function is assigned to a pin, this pin input is always enabled in Software Standby mode, and if this pin level changes, the associated KRFn can be set. Therefore, a key interrupt might occur on canceling Software Standby mode.

To ignore changes to the key interrupt pin during a software standby, clear the associated KRM bit before entering Software Standby mode. After canceling Software Standby mode, clear KRFn before the associated KRM bit is set.

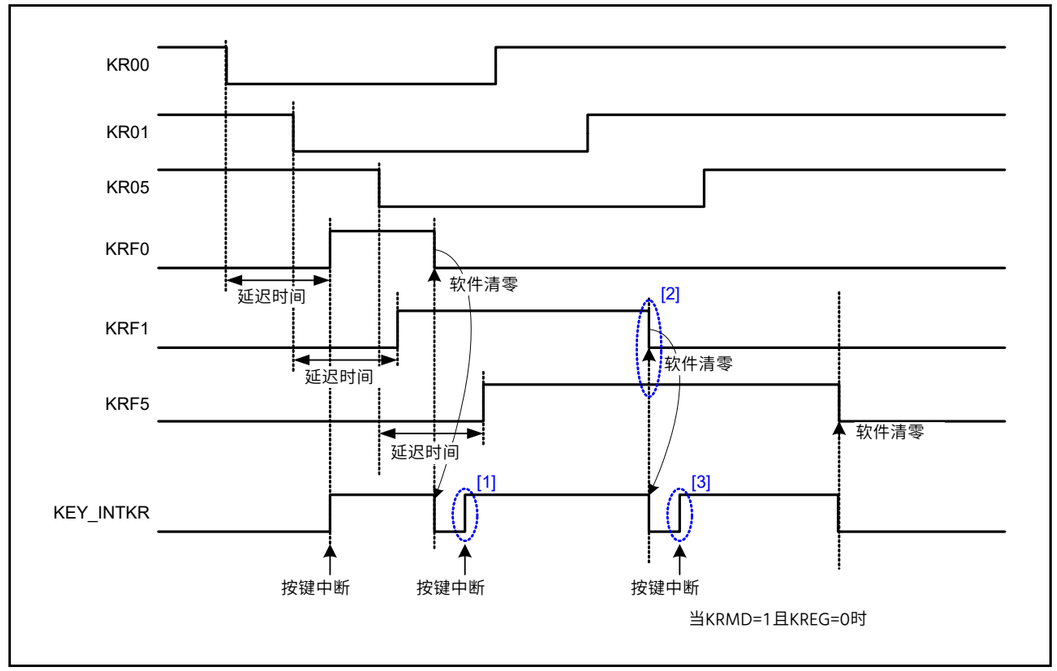


Figure 21.5 按键中断输入到多个通道时KEY_INTKR信号的操作

21.4 使用说明

- 如果KEY_INTKR用作贪睡请求，则KRMD位必须设置为0。
- 如果KEY_INTKR用作从贪睡和软件待机模式返回正常模式的中断源，则KRMD位必须设置为1。
- 当按键中断功能分配给某个引脚时，该引脚输入在软件待机模式下始终使能，如果该引脚电平发生变化，可以设置相关的KRFn。因此，取消软件待机模式时可能会发生按键中断。

要在软件待机期间忽略对按键中断引脚的更改，请在进入软件待机模式之前清除相关的KRM位。取消软件待机模式后，在设置相关KRM位之前清除KRFn。

22. Port Output Enable for GPT (POEG)

22.1 Overview

The Port Output Enable (POEG) can place the General PWM Timer (GPT) output pins in the output-disable state in one of the following ways:

- Input level detection of the GTETRGn (n = A, B) pins
- Output-disable request from the GPT
- Comparator interrupt request detection
- Oscillation stop detection of the clock generation circuit
- Register settings.

The GTETRGn (n = A, B) pins can also be used as GPT external trigger input pins.

Table 22.1 lists the POEG specifications, Figure 22.1 shows a block diagram, and Table 22.2 lists the input pins.

Table 22.1 POEG specifications

Parameter	Description
Output-disable control through input level detection	The GPT output pins can be disabled when a GTETRGn rising edge or high level is sampled after polarity and filter selection
Output-disable request from the GPT	When the GTIOCA pin and the GTIOCB pin are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG. Through reception of these requests, the POEG can control whether the GTIOCA and GTIOCB pins are output-disabled.
Output-disable control through oscillation stop detection	The GPT output pins can be disabled when oscillation of the clock generation circuit stops
Output-disable control by software (registers)	The GPT output pins can be disabled by modifying the register settings
Interrupts	• Allows output-disable control by the input level detection • Allows output-disable requests from the GPT.
External trigger output function to GPT (count start, count stop, count clear, up-count, down-count, or input capture function)	The GTETRGn signals can be output to the GPT after polarity and filter selection
Noise filtering	• Three times sampling for every PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be set for each input pin GTETRGn • Positive or negative polarity can be selected for each input pin, GTETRGn • The signal state after polarity and filter selection can be monitored.

22. GPT(POEG)的端口输出使能

22.1 Overview

端口输出使能(POEG)可以通过以下方式之一将通用PWM定时器(GPT)输出引脚置于输出禁用状态：

- GTETRn(n=A B)引脚的输入电平检测
- 来自GPT的输出禁用请求
- 比较器中断请求检测
- 时钟发生电路的振荡停止检测
- 注册设置。

GTETRn(n=A B)引脚也可用作GPT外部触发输入引脚。

表22.1列出了POEG规范，图22.1显示了框图，表22.2列出了输入引脚。

Table 22.1 POEG specifications

Parameter	Description
通过输入电平检测进行输出禁用控制	在极性和滤波器选择后采样GTETRn上升沿或高电平时，可以禁用GPT输出引脚
来自GPT的输出禁用请求	当GTIOCA引脚和GTIOCB引脚同时被驱动到有效电平时，GPT向POEG产生一个输出禁用请求。通过接收这些请求，POEG可以控制GTIOCA和GTIOCB引脚是否输出禁用。
通过振荡停止检测进行输出禁用控制	当时钟生成电路的振荡停止时，可以禁用GPT输出引脚
通过软件（寄存器）进行输出禁用控制	可以通过修改寄存器设置来禁用GPT输出引脚
Interrupts	允许通过输入电平检测进行输出禁用控制 允许来自GPT的输出禁用请求。
到GPT的外部触发输出功能（计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉功能）	GTETRn信号可在极性和滤波器选择后输出到GPT
噪声过滤	每个输入引脚GTETRn可以设置每个PCLKB1、PCLKB8、PCLKB32或PCLKB128的3次采样 每个输入引脚GTETRn可以选择正极性或负极性 极性和滤波器选择后的信号状态可以被监控。

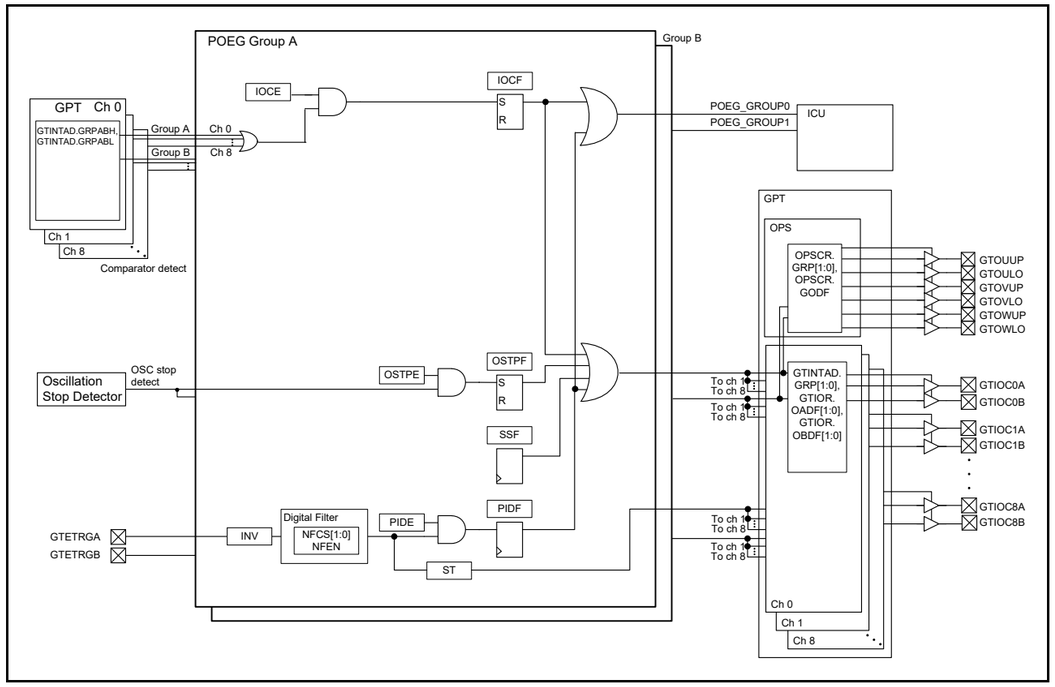


Figure 22.1 POEG block diagram

Table 22.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal and GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal and GPT external trigger input pin B

22.2 Register Descriptions

22.2.1 POEG Group n Setting Register (POEGGn) (n = A, B)

Address(es): POEG.POEGGA 4004 2000h, POEG.POEGGB 4004 2100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIDF	Port Input Detection Flag	0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R(/W)*1

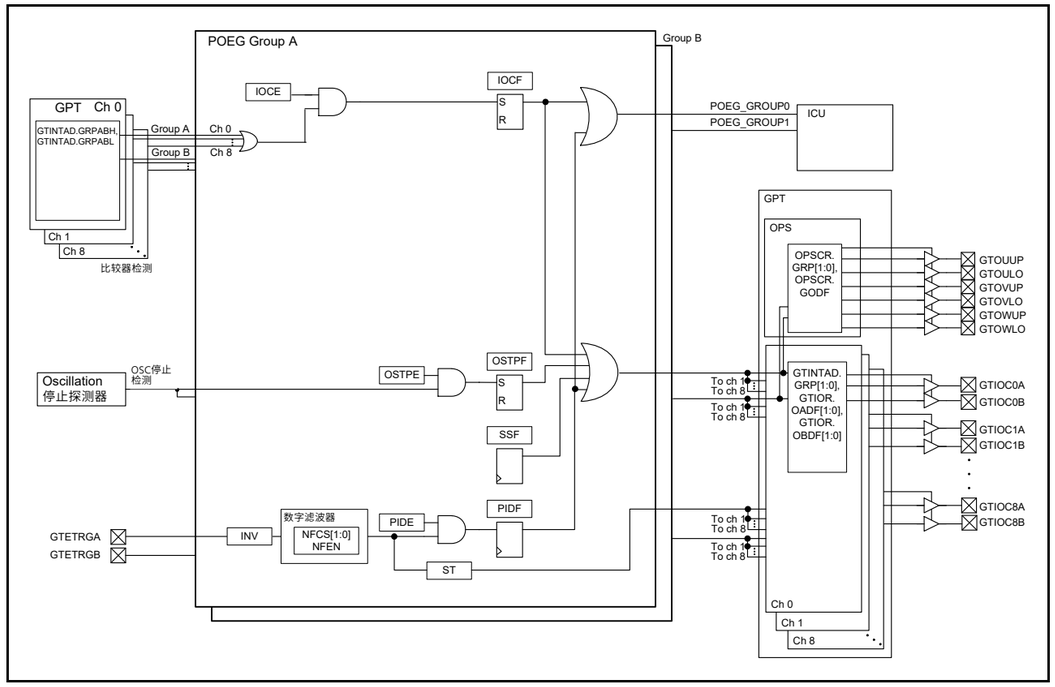


Figure 22.1 POEG框图

Table 22.2 POEG输入引脚

引脚名称	I/O	Description
GTETRGA	Input	GPT输出引脚输出禁止请求信号和GPT外部触发输入引脚A
GTETRGB	Input	GPT输出引脚输出禁止请求信号和GPT外部触发输入引脚B

22.2 注册说明

22.2.1 POEG组n设置寄存器(POEGGn)(n=A B)

Address(es): POEG.POEGGA 4004 2000h, POEG.POEGGB 4004 2100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIDF	端口输入检测标志	0：未发生来自GTETRn引脚的输出禁止请求1：发生了来自GTETRn引脚的输出禁止请求。	R(/W)*1

Bit	Symbol	Bit name	Description	R/W
b1	IOCF	Output-disable Request Detection Flag from GPT	0: No output-disable request from the GPT disable request occurred 1: Output-disable request from the GPT disable request occurred.	R(/W)*1
b2	OSTPF	Oscillation Stop Detection Flag	0: No output-disable request from oscillation stop detection occurred 1: Output-disable request from oscillation stop detection occurred.	R(/W)*1
b3	SSF	Software Stop Flag	0: No output-disable request from software occurred 1: Output-disable request from software occurred.	R/W
b4	PIDE	Port Input Detection Enable	0: Output-disable request from the GTETRGn pins disabled 1: Output-disable request from the GTETRGn pins enabled.	R/W*2
b5	IOCE	Output-disable Request Enable from GPT	0: Output-disable request from the GPT disable request disabled 1: Output-disable request from the GPT disable request enabled.	R/W*2
b6	OSTPE	Oscillation Stop Detection Enable	0: Output-disable request from the oscillation stop detection disabled 1: Output-disable request from the oscillation stop detection enabled.	R/W*2
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	ST	GTETRGn Input Status Flag	0: GTETRGn input after filtering is 0 1: GTETRGn input after filtering is 1.	R
b27 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	INV	GTETRGn Input Reverse	0: GTETRGn input as-is 1: GTETRGn input reversed.	R/W
b29	NFEN	Noise Filter Enable	0: Noise filtering disabled 1: Noise filtering enabled.	R/W
b31, b30	NFCS[1:0]	Noise Filter Clock Select	b1 b0 0 0: GTETRGn pin input level sampled three times every PCLKB 0 1: GTETRGn pin input level sampled three times every PCLKB/8 1 0: GTETRGn pin input level sampled three times every PCLKB/32 1 1: GTETRGn pin input level sampled three times every PCLKB/128.	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGA to POEGGD registers control the output-disable state of the GPT pins, interrupts, and the external trigger input to GPT. In the descriptions, POEGGn represents all the POEGGA to POEGGD registers.

22.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output disable:

- Input level or edge detection of the GTETRGn pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request enabled in the GTINTAD.GRPABH, or GTINTAD.GRPABL applies to the group selected in the GPT registers GTINTAD.GRP[1:0] and OPSCR.GRP[1:0].
- Oscillation stop detection for the clock generation circuit
  When POEGGn.OSTPE is 1, the POEGGn.OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the PWM output is disabled.

The output-disable state is controlled in the GPT. The output disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in the GPT. The output disable of the 3-phase PWM output for the BLDC motor control pins is set in the OPSCR.GRP[1:0] and OPSCR.GODF bits in GPT_OPS.

Bit	Symbol	位名称	Description	R/W
b1	IOCF	来自GPT的输出禁用请求检测标志	0：未发生来自GPT禁用请求的输出禁用请求1：发生了来自GPT禁用请求的输出禁用请求。	R(/W)*1
b2	OSTPF	振荡停止检测 Flag	0：未发生振荡停止检测的输出禁止请求1：发生了振荡停止检测的输出禁止请求。	R(/W)*1
b3	SSF	软件停止标志	0：没有来自软件的输出禁止请求1：有来自软件的输出禁止请求。	R/W
b4	PIDE	端口输入检测启用	0：禁止来自GTETRn引脚的输出禁止请求1：允许来自GTETRn引脚的输出禁止请求。	R/W*2
b5	IOCE	Output-disable Request 从GPT启用	0：禁用来自GPT禁用请求的输出禁用请求1：启用来自GPT禁用请求的输出禁用请求。	R/W*2
b6	OSTPE	振荡停止检测 Enable	0：禁止来自振荡停止检测的输出禁止请求1：允许来自振荡停止检测的输出禁止请求。	R/W*2
b15 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	ST	GTETRn输入状态标志	0：GTETRn滤波后输入为01：GTETRn滤波后输入为1。	R
b27 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	INV	GTETRn输入反向	0：GTETRn输入原样1：GTETRn输入反转。	R/W
b29	NFEN	噪声过滤器启用	0：禁用噪声过滤1：启用噪声过滤。	R/W
b31, b30	NFCS[1:0]	噪声滤波器时钟选择	b1b000：GTETRn引脚输入电平每PCLKB采样3次01：GTETRn引脚输入电平每PCLKB采样3次810：GTETRn引脚输入电平每PCLKB采样3次3211：GTETRn引脚输入电平采样3次每个PCLKB128。	R/W

Note 1. 只能写入0来清除标志。
Note 2. 重置后只能修改一次。

POEGGA到POEGGD寄存器控制GPT引脚的输出禁用状态、中断和GPT的外部触发输入。在描述中，POEGGn代表所有的POEGGA到POEGGD寄存器。

22.3 输出禁用控制操作

如果满足以下任一条件，GTIOCxA、GTIOCxB和BLDC电机控制引脚的3相PWM输出可设置为输出禁用：

- GTETRn引脚的输入电平或边沿检测
  当POEGGn.PIDE为1时，POEGGn.PIDF标志设置为1。
- 来自GPT的输出禁用请求
  当POEGGn.IOCE为1时，如果在GTINTAD.GRPABH中启用的禁用请求或GTINTAD.GRPABL适用于在GPT寄存器中选择的组，则POEGGn.IOCF标志设置为1
  GTINTAD.GRP[1:0] and OPSCR.GRP[1:0].
- 时钟发生电路的振荡停止检测
  当POEGGn.OSTPE为1时，POEGGn.OSTPF标志设置为1。
- SSF位设置
  当POEGGn.SSF设置为1时，PWM输出被禁用。

输出禁用状态由GPT控制。GTIOCxA和GTIOCxB引脚的输出禁用在GPT中的GTINTAD.GRP[1:0]、GTIOR.OADF[1:0]和GTIOR.OBDF[1:0]位中设置。三相输出禁用
BLDC电机控制引脚的PWM输出在GPT_OPS中的OPSCR.GRP[1:0]和OPSCR.GODF位中设置。

22.3.1 Pin Input Level Detection Operation

If the input conditions set by POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN, and POEGGn.INV occur on the GTETRGn pins, the GPT output pins are output-disabled.

22.3.1.1 Digital filter

Figure 22.2 shows high level detection by the digital filter. When a high level associated with the POEGGn.INV polarity setting is detected three times consecutively with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, the detected level is recognized as high, and the GPT output pins are output-disabled. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not being output, changes of the levels on the GTETRGn pins are ignored.

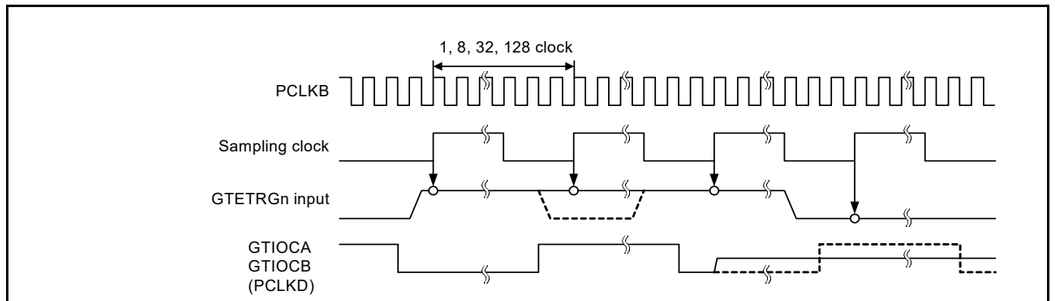


Figure 22.2 Example of digital filter operation

22.3.2 Output-Disable Request from GPT

For details on the operation, see GTIOC Pin Output Negate Control in section 23, General PWM Timer (GPT).

22.3.3 Output-Disable Control on Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are output-disabled for each group.

22.3.4 Output-Disable Control Using Registers

The GPT output pins can be directly controlled by writing to the Software Stop Flag, POEGGn.SSF.

22.3.5 Release from Output Disable

To release the GPT output pins in the output-disable state, either return them to their initial state with a reset or clear all of the following flags:

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF.

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins, GTETRGn, are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.OABHF, and GTST.OABLF

22.3.1 引脚输入电平检测操作

如果POEGGn.PIDE、POEGGn.NFCS[1:0]、POEGGn.NFEN和POEGGn.INV设置的输入条件发生在GTETRn引脚，GPT输出引脚输出禁用。

22.3.1.1 数字滤波器

图22.2显示了数字滤波器的高电平检测。当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续3次检测到与POEGGn.INV极性设置相关的高电平时，检测到的电平被识别为高电平，并且GPT输出引脚为输出禁用。如果在此间隔期间甚至检测到一个低电平，则检测到的电平不会被识别为高电平。此外，在不输出采样时钟的时间间隔内，GTETRn引脚上的电平变化将被忽略。

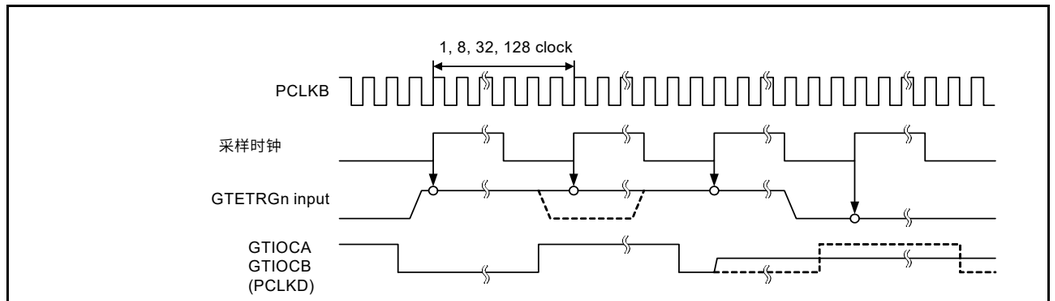


Figure 22.2 数字滤波器操作示例

22.3.2 来自GPT的输出禁用请求

有关操作的详细信息，请参阅第23节通用PWM定时器(GPT)中的GTIOC引脚输出取反控制。

22.3.3 停止振荡检测的输出禁用控制

当时钟发生电路中的振荡停止检测功能检测到停止振荡时POEGGn.OSTPE为1，每组的GPT输出引脚输出禁用。

22.3.4 使用寄存器的输出禁用控制

GPT输出引脚可以通过写入软件停止标志POEGGn.SSF来直接控制。

22.3.5 从输出禁用释放

要释放处于输出禁用状态的GPT输出引脚，可以通过复位将它们返回到初始状态，或者清除以下所有标志：

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF.

如果外部输入引脚GTETRn未禁用且POEGGn.ST位未设置为0，则忽略向POEGGn.PIDF标志写入0（该标志未清除）。

只有当所有的GTST.OABHF和GTST.OABLF都写入0到POEGGn.IOCF标志时才有效（标志被清除）

flags in GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the flag set takes precedence.

Figure 22.3 shows the released timing for output disable. The output disable is released at the beginning of the next count cycle of the GPT after the flag is cleared.

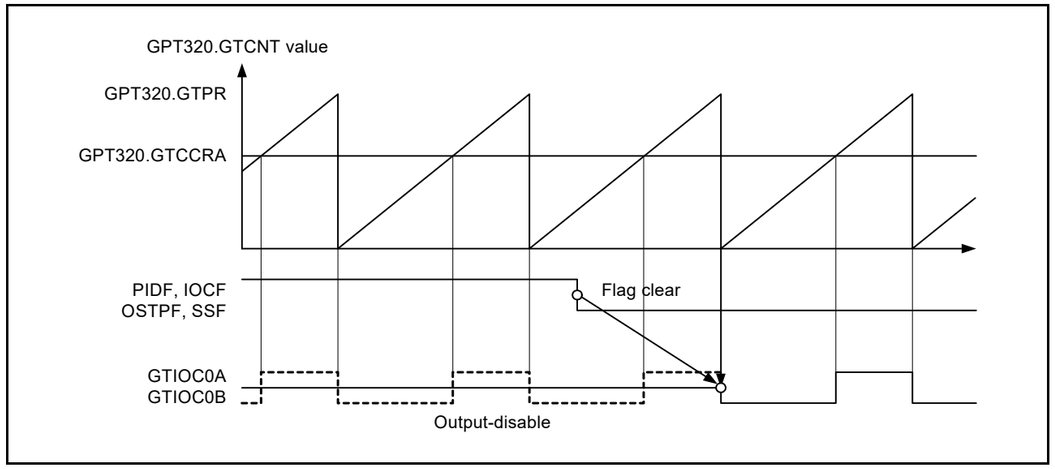


Figure 22.3 Output-disable release timing for GPT pin outputs

22.4 Interrupt Sources

The POEG generates an interrupt request when triggered by these sources:

- Output-disable control by the input level detection
- Output-disable request from the GPT.

Table 22.3 lists the conditions for interrupt requests.

Table 22.3 Interrupt sources and conditions

Interrupt source	Symbol	Associated flag	Trigger conditions
POEG group A interrupt	POEG_GROUP0	POEGGA.IOCF	An output-disable request from a GPT disable request occurred
		POEGGA.PIDF	An output-disable request from the GTETRGA pin occurred
POEG group B interrupt	POEG_GROUP1	POEGGB.IOCF	An output-disable request from a GPT disable request occurred
		POEGGB.PIDF	An output-disable request from the GTETRGB pin occurred

22.5 External Trigger Output to GPT

The POEG outputs the GTETRGn signals as the GPT operation trigger signal for the following:

- Count start
- Count stop
- Count clear
- Up-count

GPT中的标志设置为0。

如果时钟生成电路中的OSTDSR.OSTDF标志未设置为0，则忽略向POEGGn.OSTPF标志写入0（该标志不被清除）。此外，当标志设置和释放同时发生时，标志集优先。

图22.3显示了输出禁用的释放时序。清除标志后，在GPT的下一个计数周期开始时释放输出禁用。

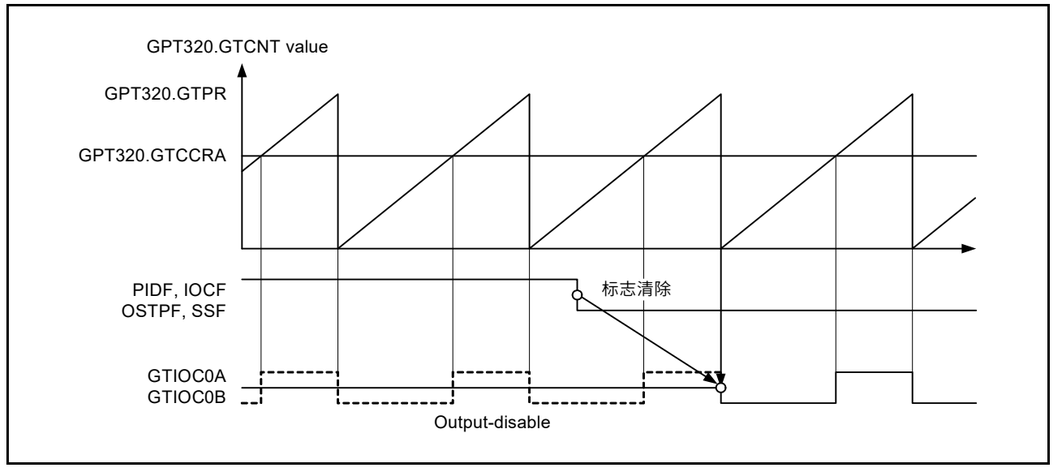


Figure 22.3 GPT引脚输出的输出禁用释放时序

22.4 中断源

当这些源触发时，POEG会产生一个中断请求：

- 通过输入电平检测进行输出禁用控制
- 来自GPT的输出禁用请求。

表22.3列出了中断请求的条件。

Table 22.3 中断源和条件

中断源	Symbol	相关标志	触发条件
POEGA组中断	POEG_GROUP0	POEGGA.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGA.PIDF	发生了来自GTETRGA引脚的输出禁用请求
POEGB组中断	POEG_GROUP1	POEGGB.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGB.PIDF	发生来自GTETRGB引脚的输出禁用请求

22.5 外部触发输出到GPT

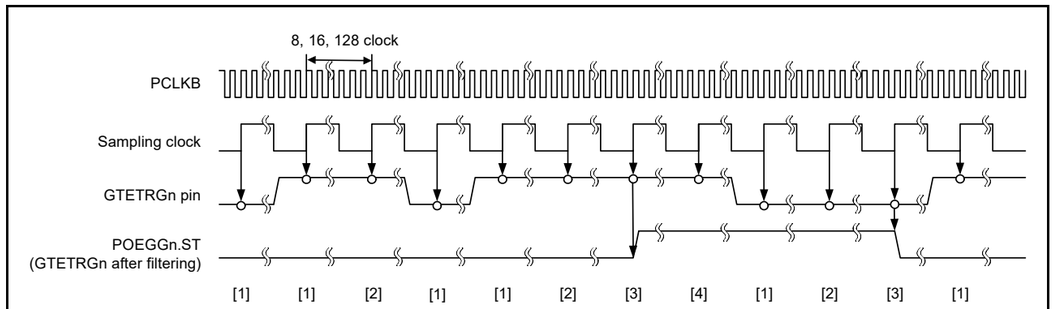
POEG输出GTETRn信号作为GPT操作触发信号，用于以下用途：

- 计数开始
- 计数停止
- 清点数
- Up-count

- Down-count
- Input capture.

For the POEGG.INV polarity setting signal, when the same level is input three times continuously with the sampling clock selected in the POEGGn.NFCS[1:0] and POEGGn.NFEN bits, that value is output. Set the control registers the same as for the input level detection operation described in section 22.3.1, Pin Input Level Detection Operation. The state after filtering can be monitored in POEGGn.ST.

Figure 22.4 shows the output timing of an external trigger to the GPT.



Note 1. Each channel output can be set in the GPT setting.
Polarity can be reversed in the POEGGn.INV setting.

Figure 22.4 Output timing of external trigger to GPT

22.6 Usage Notes

22.6.1 Transition to Software Standby Mode

When using the POEG, do not invoke Software Standby mode. In this mode, the POEG stops and therefore output disable of the pins cannot be controlled.

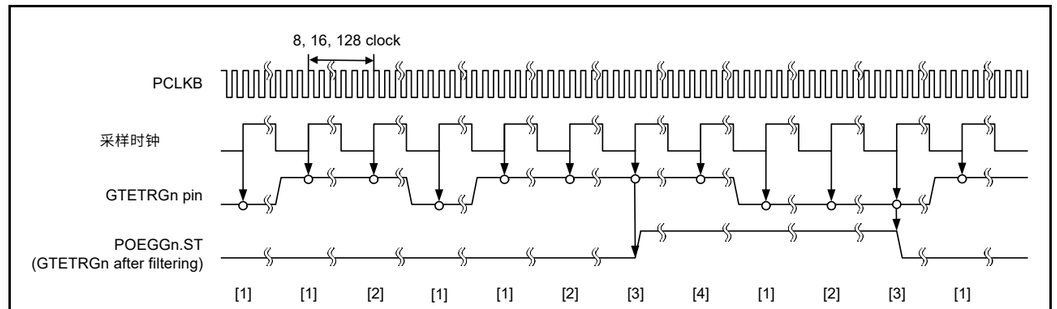
22.6.2 Specifying Pins Associated with the GPT

The POEG controls output disable only when a pin is associated with the GPT in the PmnPFS.PMR and PmnPFS.PSEL settings. When the pin is specified as a general I/O pin, the POEG does not perform output-disable control.

- Down-count
- 输入捕获。

对于POEGG.INV极性设置信号，当使用POEGGn.NFCS[1:0]和POEGGn.NFEN位中选择的采样时钟连续输入相同电平3次时，输出该值。将控制寄存器设置为与第22.3.1节"引脚输入电平检测操作"中描述的输入电平检测操作相同。过滤后的状态可以在POEGGn.ST中监控。

图22.4显示了外部触发到GPT的输出时序。



Note 1. 每个通道输出都可以在GPT设置中进行设置。
在POEGGn.INV设置中可以反转极性。

Figure 22.4 外部触发到GPT的输出时序

22.6 使用说明

22.6.1 过渡到软件待机模式

使用POEG时，请勿调用软件待机模式。在此模式下，POEG停止，因此无法控制引脚的输出禁用。

22.6.2 指定与GPT关联的引脚

仅当引脚与PmnPFS.PMR和PmnPFS.PSEL设置中的GPT关联时，POEG才控制输出禁用。当引脚指定为通用IO引脚时，POEG不执行输出禁用控制。

23. General PWM Timer (GPT)

23.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with four GPT32 channels, and a 16-bit timer with three GPT16 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

Table 23.1 lists the GPT specifications, Table 23.2 shows the GPT functions, Figure 23.1 shows a block diagram, Figure 23.2 shows the correspondence between the GPT channels and module names, and Table 23.3 lists the I/O pins.

Table 23.1 GPT specifications

Parameter	Description
Functions	• 32 bits × 4 channels • 16 bits × 3 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Starting, stopping, clearing and up/down counters in response to a maximum of eight ELC events • Starting, stopping, clearing and up/down counters in response to input level comparison • Starting, clearing, stopping and up/down counters in response to a maximum of four external triggers • Output pin disable function by detected short-circuits between output pins • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW • Bus clock: PCLKA • Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64).

23. 通用PWM定时器(GPT)

23.1 Overview

通用PWM定时器(GPT)是一个具有四个GPT32通道的32位定时器和一个具有三个GPT16通道的16位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。

表23.1列出了GPT规格，表23.2列出了GPT功能，图23.1给出了框图，图23.2给出了GPT通道和模块名称的对应关系，表23.3列出了IO引脚。

Table 23.1 GPT specifications

Parameter	Description
Functions	32位×4通道 16位×3通道 每个计数器的递增计数或递减计数（锯齿波）或递增递减计数（三角波） 每条通道可独立选择时钟源 每个通道有两个输入输出引脚通道 每个通道两个输出比较输入捕捉寄存器 对于每个通道的两个输出比较输入捕捉寄存器，提供了四个寄存器作为缓冲寄存器，并且在不使用缓冲时能够作为比较寄存器运行 在输出比较操作中，缓冲器切换可以在波峰或波谷，从而产生横向不对称的PWM波形 用于在每个通道中设置帧周期的寄存器，能够在上溢或下溢时产生中断 在PWM操作中生成死区 同步启动、停止和清除任意通道的计数器 响应最多8个ELC前夕的启动、停止、清除和递增计数器nts 响应输入电平比较启动、停止、清除和递增递减计数器 响应最多四个外部触发启动、清除、停止和递增递减计数器 通过检测到输出引脚之间的短路来禁用输出引脚 可以生成用于控制无刷直流电机的PWM波形比较匹配A到F事件、上溢下溢事件和输入UVW边缘事件可以输出到ELC启用用于输入捕获和输入UVW的噪声滤波器总线时钟：PCLKA内核时钟：PCLKD 频率比：PCLKA:PCLKD=1:N(N=1248163264)。

Table 23.2 GPT functions

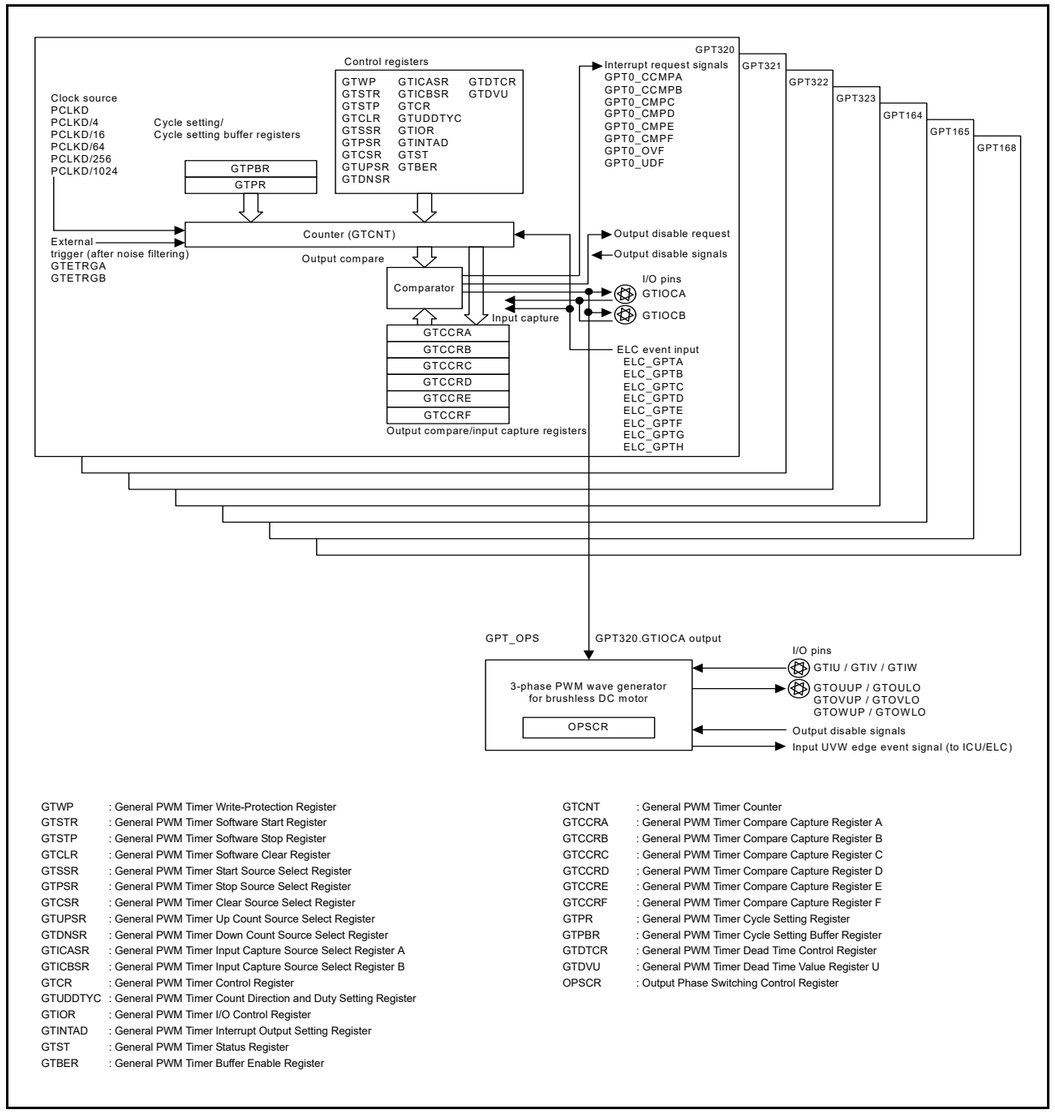
Parameter		GPT32, GPT16
Count clock		PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
Output compare/input capture registers (GTCCR)		GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register		GTPR
Cycle setting buffer registers		GTPBR
I/O pins		GTIOCA GTIOCB
External trigger input pin*1		GTETRGA GTETRGB
Counter clear sources		GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n = A, B) pin input
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available (no dead time buffer)
PWM mode		Available
Phase count function		Available
Buffer operation		Double buffer
One-shot operation		Available
DTC activation		All the interrupt sources
Brushless DC motor control function		Available
Interrupt sources		8 sources: • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCCRE compare match (GPTn_CMPE) • GTCCRF compare match (GPTn_CMPF) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF). Note: n = 0 to 5, 8
Event linking (ELC) function		Available
Noise filtering function		Available

Note 1. GTRETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPD14 bit.

Table 23.2 GPT functions

Parameter		GPT32, GPT16
计数时钟		PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
输出比较输入捕捉寄存器(GTCCR)		GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF
周期设定寄存器		GTPR
循环设置缓冲寄存器		GTPBR
I/O pins		GTIOCA GTIOCB
外部触发输入引脚*1		GTETRGA GTETRGB
反清源		GTPR寄存器比较匹配、输入捕捉、输入引脚状态、ELC事件输入和GTETRn (n=A B)引脚输入
比较匹配输出	低输出	Available
	高输出	Available
	切换输出	Available
输入捕捉功能		Available
自动添加死区时间		可用（无死区时间缓冲区）
PWM mode		Available
相位计数功能		Available
缓冲操作		双缓冲
One-shot operation		Available
DTC activation		所有中断源
直流无刷电机控制功能		Available
中断源		8个来源： GTCCRA比较匹配输入捕获(GPTn_CCMPA) GTCCRB比较匹配输入捕获(GPTn_CCMPB) GTCCRC比较匹配(GPTn_CMPC) GTCCRD比较匹配(GPTn_CMPD) GTCCRE比较匹配(GPTn_CMPE) GTCCRF比较匹配(GPTn_CMPF) GTCNT上溢（GTPR比较匹配）（GPTn_OVF） GTCNT下溢（GPTn_UDF）。注：n=0至5、8
事件链接(ELC)功能		Available
噪音过滤功能		Available

注1.GTRETRGn通过POEG模块连接到GPT。因此，要使用GPT功能，通过清除MSTPD14位来提供POEG时钟。



GTWP : General PWM Timer Write-Protection Register
GTSTR : General PWM Timer Software Start Register
GTSTP : General PWM Timer Software Stop Register
GTCLR : General PWM Timer Software Clear Register
GTSSR : General PWM Timer Start Source Select Register
GTPSR : General PWM Timer Stop Source Select Register
GTCSR : General PWM Timer Clear Source Select Register
GTUPSR : General PWM Timer Up Count Source Select Register
GTDNSR : General PWM Timer Down Count Source Select Register
GTICASR : General PWM Timer Input Capture Source Select Register A
GTICBSR : General PWM Timer Input Capture Source Select Register B
GTCR : General PWM Timer Control Register
GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register
GTIOR : General PWM Timer I/O Control Register
GTINTAD : General PWM Timer Interrupt Output Setting Register
GTST : General PWM Timer Status Register
GTBER : General PWM Timer Buffer Enable Register

GTCNT : General PWM Timer Counter
GTCCRA : General PWM Timer Compare Capture Register A
GTCCRB : General PWM Timer Compare Capture Register B
GTCCRC : General PWM Timer Compare Capture Register C
GTCCRD : General PWM Timer Compare Capture Register D
GTCCRE : General PWM Timer Compare Capture Register E
GTCCRF : General PWM Timer Compare Capture Register F
GTPR : General PWM Timer Cycle Setting Register
GTPBR : General PWM Timer Cycle Setting Buffer Register
GTDTCR : General PWM Timer Dead Time Control Register
GTDVU : General PWM Timer Dead Time Value Register U
OPSCR : Output Phase Switching Control Register

Figure 23.1 GPT block diagram

Figure 23.2 shows an example using multiple GPTs.

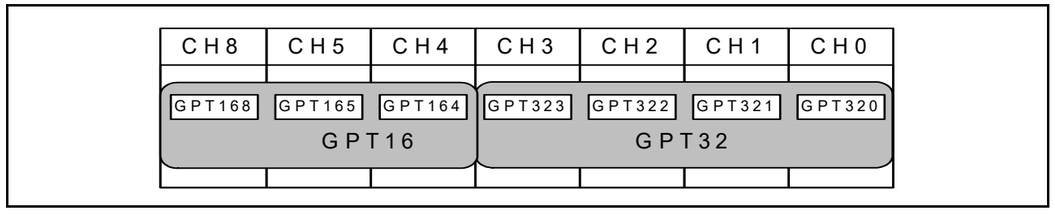
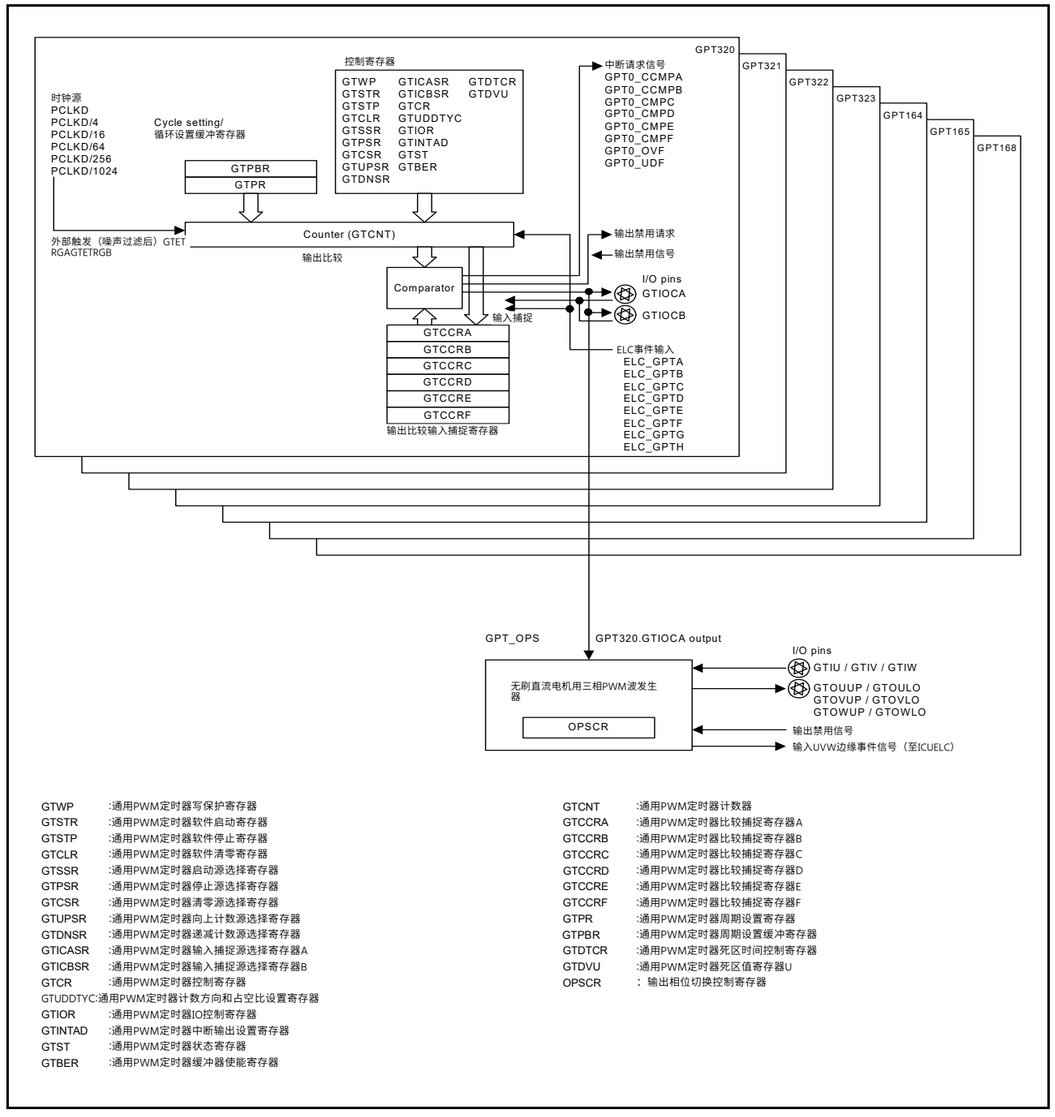


Figure 23.2 Association between GPT channels and module names



GTWP :通用PWM定时器写保护寄存器
GTSTR :通用PWM定时器软件启动寄存器
GTSTP :通用PWM定时器软件停止寄存器
GTCLR :通用PWM定时器软件清零寄存器
GTSSR :通用PWM定时器启动源选择寄存器
GTPSR :通用PWM定时器停止源选择寄存器
GTCSR :通用PWM定时器清零源选择寄存器
GTUPSR :通用PWM定时器向上计数源选择寄存器
GTDNSR :通用PWM定时器递减计数源选择寄存器
GTICASR :通用PWM定时器输入捕捉源选择寄存器A
GTICBSR :通用PWM定时器输入捕捉源选择寄存器B
GTCR :通用PWM定时器控制寄存器
GTUDDTYC:通用PWM定时器计数方向和占空比设置寄存器
GTIOR :通用PWM定时器IO控制寄存器
GTINTAD :通用PWM定时器中断输出设置寄存器
GTST :通用PWM定时器状态寄存器
GTBER :通用PWM定时器缓冲器使能寄存器

GTCNT :通用PWM定时器计数器
GTCCRA :通用PWM定时器比较捕捉寄存器A
GTCCRB :通用PWM定时器比较捕捉寄存器B
GTCCRC :通用PWM定时器比较捕捉寄存器C
GTCCRD :通用PWM定时器比较捕捉寄存器D
GTCCRE :通用PWM定时器比较捕捉寄存器E
GTCCRF :通用PWM定时器比较捕捉寄存器F
GTPR :通用PWM定时器周期设置寄存器
GTPBR :通用PWM定时器周期设置缓冲寄存器
GTDTCR :通用PWM定时器死区时间控制寄存器
GTDVU :通用PWM定时器死区值寄存器U
OPSCR : 输出相位切换控制寄存器

Figure 23.1 GPT框图

图23.2显示了使用多个GPT的示例。

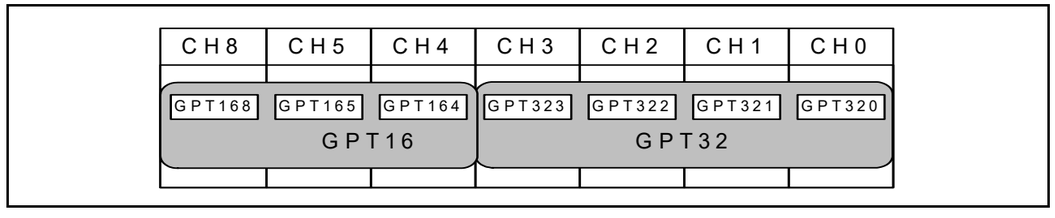


Figure 23.2 GPT通道和模块名称之间的关联

Table 23.3 lists the I/O pins used in the GPT.

Table 23.3 GPT I/O pins

Channel	Pin name	I/O	Function
Shared	GTETRGA	Input	External trigger input pin A (after noise filtering)
	GTETRGB	Input	External trigger input pin B (after noise filtering)
GPT320	GTIOC0A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT321	GTIOC1A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT322	GTIOC2A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT323	GTIOC3A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT164	GTIOC4A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC4B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT165	GTIOC5A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC5B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT168	GTIOC8A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC8B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

表23.3列出了GPT中使用的IO引脚。

Table 23.3 GPT I/O pins

Channel	引脚名称	I/O	Function
Shared	GTETRGA	Input	外部触发输入引脚A（噪声过滤后）
	GTETRGB	Input	外部触发输入引脚B（噪声过滤后）
GPT320	GTIOC0A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC0B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT321	GTIOC1A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC1B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT322	GTIOC2A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC2B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT323	GTIOC3A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC3B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT164	GTIOC4A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC4B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT165	GTIOC5A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC5B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT168	GTIOC8A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC8B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT_OPS	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）

23.2 Register Descriptions

Table 23.4 lists the registers in the GPT.

Table 23.4 GPT registers

Module symbol	Register name	Register symbol	Reset value	Address	Access size
GPT32m*1 GPT16m*2	General PWM Timer Write Protection Register	GTWP	00000000h	4007 8000h + 0100h × m	32
	General PWM Timer Software Start Register	GTSTR	00000000h	4007 8004h + 0100h × m	32
	General PWM Timer Software Stop Register	GTSTP	FFFFFFFFh	4007 8008h + 0100h × m	32
	General PWM Timer Software Clear Register	GTCLR	00000000h	4007 800Ch + 0100h × m	32
	General PWM Timer Start Source Select Register	GTSSR	00000000h	4007 8010h + 0100h × m	32
	General PWM Timer Stop Source Select Register	GTPSR	00000000h	4007 8014h + 0100h × m	32
	General PWM Timer Clear Source Select Register	GTCSR	00000000h	4007 8018h + 0100h × m	32
	General PWM Timer Up Count Source Select Register	GTUPSR	00000000h	4007 801Ch + 0100h × m	32
	General PWM Timer Down Count Source Select Register	GTDNSR	00000000h	4007 8020h + 0100h × m	32
	General PWM Timer Input Capture Source Select Register A	GTICASR	00000000h	4007 8024h + 0100h × m	32
	General PWM Timer Input Capture Source Select Register B	GTICBSR	00000000h	4007 8028h + 0100h × m	32
	General PWM Timer Control Register	GTCR	00000000h	4007 802Ch + 0100h × m	32
	General PWM Timer Count Direction and Duty Setting Register	GTUDDTYC	00000001h	4007 8030h + 0100h × m	32
	General PWM Timer I/O Control Register	GTIOR	00000000h	4007 8034h + 0100h × m	32
	General PWM Timer Interrupt Output Setting Register	GTINTAD	00000000h	4007 8038h + 0100h × m	32
	General PWM Timer Status Register	GTST	00008000h	4007 803Ch + 0100h × m	32
	General PWM Timer Buffer Enable Register	GTBER	00000000h	4007 8040h + 0100h × m	32
	General PWM Timer Counter	GTCNT	00000000h	4007 8048h + 0100h × m	32
	General PWM Timer Compare Capture Register A	GTCCRA	FFFFFFFFh*3	4007 804Ch + 0100h × m	32
	General PWM Timer Compare Capture Register B	GTCCRB	FFFFFFFFh*3	4007 8050h + 0100h × m	32
	General PWM Timer Compare Capture Register C	GTCCRC	FFFFFFFFh*3	4007 8054h + 0100h × m	32
	General PWM Timer Compare Capture Register E	GTCCRE	FFFFFFFFh*3	4007 8058h + 0100h × m	32
	General PWM Timer Compare Capture Register D	GTCCRD	FFFFFFFFh*3	4007 805Ch + 0100h × m	32
	General PWM Timer Compare Capture Register F	GTCCRF	FFFFFFFFh*3	4007 8060h + 0100h × m	32
	General PWM Timer Cycle Setting Register	GTPR	FFFFFFFFh*3	4007 8064h + 0100h × m	32
	General PWM Timer Cycle Setting Buffer Register	GTPBR	FFFFFFFFh*3	4007 8068h + 0100h × m	32
	General PWM Timer Dead Time Control Register	GTDTCR	00000000h	4007 8088h + 0100h × m	32
	General PWM Timer Dead Time Value Register U	GTDVU	FFFFFFFFh*3	4007 808Ch + 0100h × m	32
GPT_OPS	Output Phase Switching Control Register	OPSCR	00000000h	4007 8FF0h	32

Note 1. GPT32m (m = 0 to 3)
Note 2. GPT16m (m = 4, 5, 8)
Note 3. The reset value of GPT16m is 0000FFFFh.

23.2 注册说明

表23.4列出了GPT中的寄存器。

Table 23.4 GPT registers

模块符号	注册名称	注册符号	重置值	Address	访问大小
GPT32m*1 GPT16m*2	通用PWM定时器写保护寄存器	GTWP	00000000h	4007 8000h + 0100h × m	32
	通用PWM定时器软件启动寄存器	GTSTR	00000000h	4007 8004h + 0100h × m	32
	通用PWM定时器软件停止寄存器	GTSTP	FFFFFFFFh	4007 8008h + 0100h × m	32
	通用PWM定时器软件清零寄存器	GTCLR	00000000h	4007 800Ch + 0100h × m	32
	通用PWM定时器启动源选择寄存器	GTSSR	00000000h	4007 8010h + 0100h × m	32
	通用PWM定时器停止源选择寄存器	GTPSR	00000000h	4007 8014h + 0100h × m	32
	通用PWM定时器清零源选择寄存器	GTCSR	00000000h	4007 8018h + 0100h × m	32
	通用PWM定时器向上计数源选择寄存器	GTUPSR	00000000h	4007 801Ch + 0100h × m	32
	通用PWM定时器递减计数源选择寄存器	GTDNSR	00000000h	4007 8020h + 0100h × m	32
	通用PWM定时器输入捕捉源选择寄存器A	GTICASR	00000000h	4007 8024h + 0100h × m	32
	通用PWM定时器输入捕捉源选择寄存器B	GTICBSR	00000000h	4007 8028h + 0100h × m	32
	通用PWM定时器控制寄存器	GTCR	00000000h	4007 802Ch + 0100h × m	32
	通用PWM定时器计数方向和占空比设置 Register	GTUDDTYC	00000001h	4007 8030h + 0100h × m	32
	通用PWM定时器IO控制寄存器	GTIOR	00000000h	4007 8034h + 0100h × m	32
	通用PWM定时器中断输出设置寄存器	GTINTAD	00000000h	4007 8038h + 0100h × m	32
	通用PWM定时器状态寄存器	GTST	00008000h	4007 803Ch + 0100h × m	32
	通用PWM定时器缓冲器使能寄存器	GTBER	00000000h	4007 8040h + 0100h × m	32
	通用PWM定时器计数器	GTCNT	00000000h	4007 8048h + 0100h × m	32
	通用PWM定时器比较捕捉寄存器A	GTCCRA	FFFFFFFFh*3	4007 804Ch + 0100h × m	32
	通用PWM定时器比较捕捉寄存器B	GTCCRB	FFFFFFFFh*3	4007 8050h + 0100h × m	32
	通用PWM定时器比较捕捉寄存器C	GTCCRC	FFFFFFFFh*3	4007 8054h + 0100h × m	32
	通用PWM定时器比较捕捉寄存器E	GTCCRE	FFFFFFFFh*3	4007 8058h + 0100h × m	32
	通用PWM定时器比较捕捉寄存器D	GTCCRD	FFFFFFFFh*3	4007 805Ch + 0100h × m	32
	通用PWM定时器比较捕捉寄存器F	GTCCRF	FFFFFFFFh*3	4007 8060h + 0100h × m	32
	通用PWM定时器周期设置寄存器	GTPR	FFFFFFFFh*3	4007 8064h + 0100h × m	32
	通用PWM定时器周期设置缓冲寄存器	GTPBR	FFFFFFFFh*3	4007 8068h + 0100h × m	32
	通用PWM定时器死区时间控制寄存器	GTDTCR	00000000h	4007 8088h + 0100h × m	32
	通用PWM定时器死区值寄存器U	GTDVU	FFFFFFFFh*3	4007 808Ch + 0100h × m	32
GPT_OPS	输出相位切换控制寄存器	OPSCR	00000000h	4007 8FF0h	32

Note 1. GPT32m (m = 0 to 3)
Note 2. GPT16m (m = 4, 5, 8)
Note 3. GPT16m的复位值为0000FFFFh。

23.2.1 General PWM Timer Write-Protection Register (GTWP)

Address(es): GPT32m.GTWP 4007 8000h + 0100h × m (m = 0 to 3),
GPT16m.GTWP 4007 8000h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	—	—	—	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WP	Register Write Disable	0: Write to the register enabled 1: Write to the register disabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	GTWP Key Code	When A5h is written to these bits, writing to the WP bits is permitted. These bits are read as 0.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

To prevent accidental modification, the GTWP enables or disables writing to registers. The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

23.2.2 General PWM Timer Software Start Register (GTSTR)

Address(es): GPT32m.GTSTR 4007 8004h + 0100h × m (m = 0 to 3),
GPT16m.GTSTR 4007 8004h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CSTRT8	—	—	CSTRT5	CSTRT4	CSTRT3	CSTRT2	CSTRT1	CSTRT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 5, 8.

The GTSTR bit number represents the channel number. The GTSTR register is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

For the association between GTSTR bit number and a channel number, see Figure 23.2.

CSTRT[9:0] bits (Channel n GTCNT Count Start) (n = 0 to 5, 8)

The CSTRT[9:0] bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 5, 8) has no effect unless GPTm.GTSSR.CSTRTn bit is set to 1 (m = 320 to 323, 164, 165, 168).

The read data shows the counter status of each channel (GTCR.CST bit). Zero means the counter is stopped and 1 means the counter is running.

23.2.1 通用PWM定时器写保护寄存器(GTWP)

Address(es): GPT32m.GTWP 4007 8000h + 0100h × m (m = 0 to 3),
GPT16m.GTWP 4007 8000h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	—	—	—	WP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	WP	寄存器写禁用	0：允许写入寄存器1：禁止写入寄存器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	PRKEY[7:0]	GTWP密钥代码	当A5h写入这些位时，允许写入WP位。这些位读为0。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

为防止意外修改，GTWP启用或禁用对寄存器的写入。以下是写启用或禁用寄存器的列表：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

23.2.2 通用PWM定时器软件启动寄存器(GTSTR)

Address(es): GPT32m.GTSTR 4007 8004h + 0100h × m (m = 0 to 3),
GPT16m.GTSTR 4007 8004h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CSTRT8	—	—	CSTRT5	CSTRT4	CSTRT3	CSTRT2	CSTRT1	CSTRT0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTSTR启动每个通道n的GTCNT计数器操作，其中n=0到5、8。

GTSTR位号代表通道号。GTSTR寄存器由所有通道共享。这
GTCNT计数器针对与写入1的GTSTR位号相关的通道启动。写0对GTCNT计数器的状态和GTSTR寄存器的值没有影响。

GTSTR位号与通道号的关系见图23.2。

CSTRT[9:0]位（通道nGTCNT计数开始）（n=0到5、8）

CSTRT[9:0]位启动GTCNT计数器操作的通道n。除非GPTm.GTSSR.CSTRTn位设置为1（m=320到323、164、165、168），否则写入GTSTR.CSTRTn位（n=0到5、8）无效。

读取的数据显示每个通道的计数器状态（GTCR.CST位）。零表示计数器停止，1表示计数器正在运行。

23.2.3 General PWM Timer Software Stop Register (GTSTP)

Address(es): GPT32m.GTSTP 4007 8008h + 0100h × m (m = 0 to 3),
GPT16m.GTSTP 4007 8008h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CSTOP 8	—	—	CSTOP 5	CSTOP 4	CSTOP 3	CSTOP 2	CSTOP 1	CSTOP 0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0 to 5, 8.

The GTSTP bit number represents the channel number. Each channel of the GTSTP register is shared by all the channels. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTP register.

For the association between the GTSTP bit number and a channel number, see Figure 23.2.

CSTOP[9:0] bits (Channel n GTCNT Count Stop) (n = 0 to 5, 8)

The CSTOP[9:0] bits stop channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 5, 8) has no effect unless the GPT32m.GTPSR.CSTOPn bit is set to 1 (m = 320 to 323, 164, 165, 168). The read data shows the counter status of each channel (invert of GTCR.CST bit). Zero means the counter is running and 1 means the counter stops.

23.2.4 General PWM Timer Software Clear Register (GTCLR)

Address(es): GPT32m.GTCLR 4007 800Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCLR 4007 800Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CCLR 8	—	—	CCLR 5	CCLR 4	CCLR 3	CCLR 2	CCLR 1	CCLR 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 5, 8.

The GTCLR bit number represents the channel number. Each channel of the GTCLR register is shared by all the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter.

For the association between the GTCLR bit number and a channel number, see Figure 23.2.

CCLR[9:0] bits (Channel n GTCNT Count Clear) (n = 0 to 5, 8)

Channel n of the GTCNT counter value is cleared on writing 1 to the CCLR[9:0] bit. This bit is read as 0.

23.2.3 通用PWM定时器软件停止寄存器(GTSTP)

Address(es): GPT32m.GTSTP 4007 8008h + 0100h × m (m = 0 to 3),
GPT16m.GTSTP 4007 8008h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CSTOP 8	—	—	CSTOP 5	CSTOP 4	CSTOP 3	CSTOP 2	CSTOP 1	CSTOP 0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTSTP停止每个通道n的GTCNT计数器操作，其中n=0到5、8。

GTSTP位号代表通道号。GTSTP寄存器的每个通道由所有通道共享。
对于与写入1的GTSTP位号相关的通道，GTCNT计数器停止。写0对GTCNT计数器的状态和GTSTP寄存器的值没有影响。

GTSTP比特编号与通道编号的关系见图23.2。

CSTOP[9:0]位（通道nGTCNT计数停止）（n=0到5、8）

CSTOP[9:0]位停止GTCNT计数器操作的通道n。除非GPT32m.GTPSR.CSTOPn位设置为1（m=320到323、164、165、168），否则写入GTSTP.CSTOPn位（n=0到5、8）无效。读取的数据显示每个通道的计数器状态（GTCR.CST位的反转）。零表示计数器正在运行，1表示计数器停止。

23.2.4 通用PWM定时器软件清零寄存器(GTCLR)

Address(es): GPT32m.GTCLR 4007 800Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCLR 4007 800Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CCLR 8	—	—	CCLR 5	CCLR 4	CCLR 3	CCLR 2	CCLR 1	CCLR 0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCLR是一个只写寄存器，用于清除每个通道n的GTCNT计数器操作，其中n=0到5、8。

GTCLR位号代表通道号。GTCLR寄存器的每个通道由所有通道共享。与写入1的GTCLR位号关联的通道的GTCNT计数器清零。写0对GTCNT计数器的状态没有影响。

GTCLR位号和通道号之间的关联，见图23.2。

CCLR[9:0]位（通道nGTCNT计数清除）（n=0到5、8）

GTCNT计数器值的通道n在向CCLR[9:0]位写入1时被清除。该位读为0。

23.2.5 General PWM Timer Start Source Select Register (GTSSR)

Address(es): GPT32m.GTSSR 4007 8010h + 0100h × m (m = 0 to 3),
GPT16m.GTSSR 4007 8010h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	—	—	—	—	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable	0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input.	R/W
b1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable	0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input.	R/W
b2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable	0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input.	R/W
b3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable	0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	SSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter start enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	SSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter start enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	SSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter start enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	SSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter start enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	SSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter start enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	SSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable	0: Counter start disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter start enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

23.2.5 通用PWM定时器启动源选择寄存器(GTSSR)

Address(es): GPT32m.GTSSR 4007 8010h + 0100h × m (m = 0 to 3),
GPT16m.GTSSR 4007 8010h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	—	—	—	—	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SSGTRGAR	GTETRGA引脚上升输入源计数器启动启用	0：在GTETRGA输入的上升沿禁止计数器启动1：在GTETRGA输入的上升沿使能计数器启动。	R/W
b1	SSGTRGAF	GTETRGA引脚下降输入源计数器启动启用	0：在GTETRGA输入的下降沿禁止计数器启动1：在GTETRGA输入的下降沿使能计数器启动。	R/W
b2	SSGTRGBR	GTETRGB引脚上升输入源计数器启动启用	0：在GTETRGB输入的上升沿禁止计数器启动1：在GTETRGB输入的上升沿使能计数器启动。	R/W
b3	SSGTRGBF	GTETRGB引脚下降输入源计数器启动启用	0：在GTETRGB输入的下降沿禁用计数器启动1：在GTETRGB输入的下降沿启用计数器启动。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	SSCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器启动启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器启动1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器启动。	R/W
b9	SSCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器启动启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器启动1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器启动。	R/W
b10	SSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器启动启用	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁止计数器启动1：当GTIOCB输入为0时，在GTIOCA输入的下降沿使能计数器启动。	R/W
b11	SSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器启动启用	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁止计数器启动1：当GTIOCB输入为1时，在GTIOCA输入的下降沿使能计数器启动。	R/W
b12	SSCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器启动启用	0：当GTIOCA输入为0时，在GTIOCB输入的上升沿禁止计数器启动1：当GTIOCA输入为0时，在GTIOCB输入的上升沿使能计数器启动。	R/W
b13	SSCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器启动启用	0：当GTIOCA输入为1时，在GTIOCB输入的上升沿禁止计数器启动1：当GTIOCA输入为1时，在GTIOCB输入的上升沿使能计数器启动。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	SSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter start enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	SSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable	0: Counter start disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter start enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	SSELCA	ELC_GPTA Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTA input 1: Counter start enabled at the ELC_GPTA input.	R/W
b17	SSELCB	ELC_GPTB Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTB input 1: Counter start enabled at the ELC_GPTB input.	R/W
b18	SSELCC	ELC_GPTC Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTC input 1: Counter start enabled at the ELC_GPTC input.	R/W
b19	SSELCD	ELC_GPTD Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTD input 1: Counter start enabled at the ELC_GPTD input.	R/W
b20	SSELCE	ELC_GPTE Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTE input 1: Counter start enabled at the ELC_GPTE input.	R/W
b21	SSELCF	ELC_GPTF Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTF input 1: Counter start enabled at the ELC_GPTF input.	R/W
b22	SSELCG	ELC_GPTG Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTG input 1: Counter start enabled at the ELC_GPTG input.	R/W
b23	SSELCH	ELC_GPTH Event Source Counter Start Enable	0: Counter start disabled at the ELC_GPTH input 1: Counter start enabled at the ELC_GPTH input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTRT	Software Source Counter Start Enable	0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register.	R/W

The GTSSR sets the source to start the GTCNT counter.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of GTETRGB pin input.

SSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

SSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

SSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

Bit	Symbol	位名称	Description	R/W
b14	SSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器启动启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器启动1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器启动。	R/W
b15	SSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器启动启用	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁止计数器启动1：当GTIOCA输入为1时，在GTIOCB输入的下降沿使能计数器启动。	R/W
b16	SSELCA	ELC_GPTA事件源计数器启动启用	0：在ELC_GPTA输入处禁用计数器启动1：在ELC_GPTA输入处启用计数器启动。	R/W
b17	SSELCB	ELC_GPTB事件源计数器启动启用	0：在ELC_GPTB输入处禁用计数器启动1：在ELC_GPTB输入处启用计数器启动。	R/W
b18	SSELCC	ELC_GPTC事件源计数器启动启用	0：在ELC_GPTC输入处禁用计数器启动1：在ELC_GPTC输入处启用计数器启动。	R/W
b19	SSELCD	ELC_GPTD事件源计数器启动启用	0：在ELC_GPTD输入处禁用计数器启动1：在ELC_GPTD输入处启用计数器启动。	R/W
b20	SSELCE	ELC_GPTE事件源计数器启动启用	0：在ELC_GPTE输入处禁用计数器启动1：在ELC_GPTE输入处启用计数器启动。	R/W
b21	SSELCF	ELC_GPTF事件源计数器启动启用	0：在ELC_GPTF输入处禁用计数器启动1：在ELC_GPTF输入处启用计数器启动。	R/W
b22	SSELCG	ELC_GPTG事件源计数器启动启用	0：在ELC_GPTG输入处禁用计数器启动1：在ELC_GPTG输入处启用计数器启动。	R/W
b23	SSELCH	ELC_GPTH事件源计数器启动启用	0：在ELC_GPTH输入处禁用计数器启动1：在ELC_GPTH输入处启用计数器启动。	R/W
b30 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	CSTRT	软件源计数器启动Enable	0：由GTSTR寄存器禁止计数器启动1：由GTSTR寄存器使能计数器启动。	R/W

GTSSR设置启动GTCNT计数器的源。

SSGTRGAR位（GTETRGA引脚上升沿输入源计数器启动使能）

SSGTRGAR位启用或禁用GTCNT计数器在GTETRGA引脚输入的上升沿启动。

SSGTRGAF位（GTETRGA引脚下降输入源计数器启动使能）

SSGTRGAF位启用或禁用GTCNT计数器在GTETRGA引脚输入的下降沿启动。

SSGTRGBR位（GTETRGB引脚上升输入源计数器启动使能）

SSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSGTRGBF位（GTETRGB引脚下降输入源计数器启动使能）

SSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器启动。

SSCARBL位（GTIOCB值低电平期间的GTIOCA引脚上升沿输入源计数器启动使能）

当GTIOCB输入为0时，SSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSCARBH位（GTIOCB值高源计数器启动启用期间GTIOCA引脚上升沿输入）

SSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器启动，当GTIOCB输入为1。

SSCAFBL位（GTIOCB值低源计数器启动启用期间的GTIOCA引脚下降输入）

SSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器，当GTIOCB输入为0。

SSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

SSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

SSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

SSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

SSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by GTSTR register.

23.2.6 General PWM Timer Stop Source Select Register (GTPSR)

Address(es): GPT32m.GTPSR 4007 8014h + 0100h × m (m = 0 to 3),
GPT16m.GTPSR 4007 8014h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	—	—	—	—	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input.	R/W
b1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input.	R/W
b2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input.	R/W

SSCAFBH位（GTIOCB值高源计数器启动启用期间GTIOCA引脚下降输入）

SSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器启动，当GTIOCB输入为1。

SSCBRAL位（GTIOCA值低源计数器启动启用期间GTIOCB引脚上升沿输入）

当GTIOCA输入为0时，SSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSCBRAH位（GTIOCA值高源计数器启动启用期间的GTIOCB引脚上升沿输入）

SSCBRAH位启用或禁用GTCNT计数器在GTIOCB引脚输入的上升沿启动，当GTIOCA输入为1。

SSCBFAL位（GTIOCA值低源计数器启动启用期间的GTIOCB引脚下降输入）

SSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器，当GTIOCA输入为0。

SSCBFAH位（GTIOCA值高源计数器启动启用期间GTIOCB引脚下降输入）

SSCBFAH位启用或禁用GTCNT计数器在GTIOCB引脚输入的下降沿启动，当GTIOCA输入为1。

SSELCm位（ELC_GPTm事件源计数器启动启用）（m=A到H）

SSELCm位启用或禁用在ELC_GPTm事件输入时启动的GTCNT计数器。

CSTRT位（软件源计数器启动使能）

CSTRT位启用或禁用由GTSTR寄存器启动的GTCNT计数器。

23.2.6 通用PWM定时器停止源选择寄存器(GTPSR)

Address(es): GPT32m.GTPSR 4007 8014h + 0100h × m (m = 0 to 3),
GPT16m.GTPSR 4007 8014h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	—	—	—	—	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PSGTRGAR	GTETRGA引脚上升输入源计数器停止启用	0：在GTETRGA输入的上升沿禁止计数器停止1：在GTETRGA输入的上升沿使能计数器停止。	R/W
b1	PSGTRGAF	GTETRGA引脚下降输入源计数器停止启用	0：在GTETRGA输入的下降沿禁止计数器停止1：在GTETRGA输入的下降沿使能计数器停止。	R/W
b2	PSGTRGBR	GTETRGB引脚上升输入源计数器停止启用	0：在GTETRGB输入的上升沿禁止计数器停止1：在GTETRGB输入的上升沿使能计数器停止。	R/W

Bit	Symbol	Bit name	Description	R/W
b3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter stop enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	PSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter stop enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	PSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter stop enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	PSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter stop enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	PSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter stop enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	PSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable	0: Counter stop disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter stop enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	PSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter stop enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	PSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable	0: Counter stop disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter stop enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	PSELCA	ELC_GPTA Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTA input 1: Counter stop enabled at the ELC_GPTA input.	R/W
b17	PSELCB	ELC_GPTB Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTB input 1: Counter stop enabled at the ELC_GPTB input.	R/W
b18	PSELCC	ELC_GPTC Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTC input 1: Counter stop enabled at the ELC_GPTC input.	R/W
b19	PSELCD	ELC_GPTD Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTD input 1: Counter stop enabled at the ELC_GPTD input.	R/W
b20	PSELCE	ELC_GPTE Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTE input 1: Counter stop enabled at the ELC_GPTE input.	R/W
b21	PSELCF	ELC_GPTF Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTF input 1: Counter stop enabled at the ELC_GPTF input.	R/W
b22	PSELCG	ELC_GPTG Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTG input 1: Counter stop enabled at the ELC_GPTG input.	R/W
b23	PSELCH	ELC_GPTH Event Source Counter Stop Enable	0: Counter stop disabled at the ELC_GPTH input 1: Counter stop enabled at the ELC_GPTH input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTOP	Software Source Counter Stop Enable	0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register.	R/W

The GTPSR sets the source to stop the GTCNT counter.

Bit	Symbol	位名称	Description	R/W
b3	PSGTRGBF	GTETRGB引脚下降输入源计数器停止启用	0：在GTETRGB输入的下降沿禁用计数器停止1：在GTETRGB输入的下降沿启用计数器停止。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	PSCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器停止启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器停止1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器停止。	R/W
b9	PSCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器停止启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器停止1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器停止。	R/W
b10	PSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器停止启用	0：当GTIOCB输入为0时，在GTIOCA输入下降沿禁止计数器停止1：当GTIOCB输入为0时，在GTIOCA输入下降沿使能计数器停止。	R/W
b11	PSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器停止启用	0：当GTIOCB输入为1时，在GTIOCA输入下降沿禁止计数器停止1：当GTIOCB输入为1时，在GTIOCA输入下降沿使能计数器停止。	R/W
b12	PSCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器停止启用	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止计数器停止1：当GTIOCA输入为0时，在GTIOCB输入上升沿使能计数器停止。	R/W
b13	PSCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器停止启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器停止1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器停止。	R/W
b14	PSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器停止启用	0：当GTIOCA输入为0时，在GTIOCB输入下降沿禁止计数器停止1：当GTIOCA输入为0时，在GTIOCB输入下降沿使能计数器停止。	R/W
b15	PSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器停止启用	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁止计数器停止1：当GTIOCA输入为1时，在GTIOCB输入的下降沿使能计数器停止。	R/W
b16	PSELCA	ELC_GPTA事件源计数器停止启用	0：在ELC_GPTA输入处禁用计数器停止1：在ELC_GPTA输入处启用计数器停止。	R/W
b17	PSELCB	ELC_GPTB事件源计数器停止启用	0：在ELC_GPTB输入处禁用计数器停止1：在ELC_GPTB输入处启用计数器停止。	R/W
b18	PSELCC	ELC_GPTC事件源计数器停止启用	0：在ELC_GPTC输入处禁用计数器停止1：在ELC_GPTC输入处启用计数器停止。	R/W
b19	PSELCD	ELC_GPTD事件源计数器停止启用	0：在ELC_GPTD输入处禁用计数器停止1：在ELC_GPTD输入处启用计数器停止。	R/W
b20	PSELCE	ELC_GPTE事件源计数器停止启用	0：在ELC_GPTE输入处禁用计数器停止1：在ELC_GPTE输入处启用计数器停止。	R/W
b21	PSELCF	ELC_GPTF事件源计数器停止启用	0：在ELC_GPTF输入处禁用计数器停止1：在ELC_GPTF输入处启用计数器停止。	R/W
b22	PSELCG	ELC_GPTG事件源计数器停止启用	0：在ELC_GPTG输入处禁用计数器停止1：在ELC_GPTG输入处启用计数器停止。	R/W
b23	PSELCH	ELC_GPTH事件源计数器停止启用	0：在ELC_GPTH输入处禁用计数器停止1：在ELC_GPTH输入处启用计数器停止。	R/W
b30 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	CSTOP	软件源计数器停止Enable	0：GTSTP寄存器禁止计数器停止1：GTSTP寄存器使能计数器停止。	R/W

GTPSR设置源以停止GTCNT计数器。

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

The PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of GTETRGB pin input.

PSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

PSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables the GTCNT counter stop on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

PSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

PSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

PSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

PSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

PSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

PSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

PSELCm bit (ELC_GPTm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by GTSTP register.

PSGTRGAR位（GTETRGA引脚上升沿输入源计数器停止使能）

PSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGAF位（GTETRGA引脚下降输入源计数器停止使能）

PSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGBR位（GTETRGB引脚上升输入源计数器停止使能）

PSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGBF位（GTETRGB引脚下降输入源计数器停止使能）

PSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSCARBL位（GTIOCB值低源计数器停止使能期间GTIOCA引脚上升沿输入）

当GTIOCB输入为0时，PSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSCARBH位（GTIOCB值高源计数器停止使能期间GTIOCA引脚上升沿输入）

当GTIOCB输入为1时，PSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSCAFBL位（GTIOCB值低源计数器停止使能期间GTIOCA引脚下降输入）

PSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCB输入为0。

PSCAFBH位（GTIOCB值高源计数器停止使能期间GTIOCA引脚下降输入）

PSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCB输入为1。

PSCBRAL位（GTIOCA值低源计数器停止使能期间GTIOCB引脚上升沿输入）

当GTIOCA输入为0时，PSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSCBRAH位（GTIOCA值高源计数器停止使能期间GTIOCB引脚上升沿输入）

当GTIOCA输入为1时，PSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSCBFAL位（GTIOCA值低源计数器停止使能期间GTIOCB引脚下降输入）

PSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCA输入为0。

PSCBFAH位（GTIOCA值高源计数器停止使能期间GTIOCB引脚下降输入）

PSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCA输入为1。

PSELCm位（ELC_GPTm事件源计数器停止使能）（m=A到H）

PSELCm位启用或禁用GTCNT计数器在ELC_GPTm事件输入处停止。

CSTOP位（软件源计数器停止使能）

CSTOP位通过GTSTP寄存器启用或禁用GTCNT计数器停止。

23.2.7 General PWM Timer Clear Source Select Register (GTCSR)

Address(es): GPT32m.GTCSR 4007 8018h + 0100h × m (m = 0 to 3),
GPT16m.GTCSR 4007 8018h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	—	—	—	—	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input.	R/W
b1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input.	R/W
b2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTETRGB input 1: Counter clear enabled on the rising edge of GTETRGB input.	R/W
b3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter clear enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	CSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter clear enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	CSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter clear enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	CSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter clear enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	CSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter clear enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	CSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable	0: Counter clear disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter clear enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

23.2.7 通用PWM定时器清零源选择寄存器(GTCSR)

Address(es): GPT32m.GTCSR 4007 8018h + 0100h × m (m = 0 to 3),
GPT16m.GTCSR 4007 8018h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	—	—	—	—	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CSGTRGAR	GTETRGA引脚上升输入源计数器清除启用	0：在GTETRGA输入的上升沿禁止计数器清除1：在GTETRGA输入的上升沿使能计数器清除。	R/W
b1	CSGTRGAF	GTETRGA引脚下降输入源计数器清除启用	0：在GTETRGA输入的下降沿禁止计数器清除1：在GTETRGA输入的下降沿使能计数器清除。	R/W
b2	CSGTRGBR	GTETRGB引脚上升输入源计数器清除启用	0：在GTETRGB输入的上升沿禁止计数器清除1：在GTETRGB输入的上升沿使能计数器清除。	R/W
b3	CSGTRGBF	GTETRGB引脚下降输入源计数器清除启用	0：在GTETRGB输入的下降沿禁用计数器清除1：在GTETRGB输入的下降沿启用计数器清除。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	CSCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器清除启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器清除1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器清除。	R/W
b9	CSCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器清除启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器清除1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器清除。	R/W
b10	CSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器清除启用	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁止计数器清除1：当GTIOCB输入为0时，在GTIOCA输入的下降沿使能计数器清除。	R/W
b11	CSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器清除启用	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁止计数器清零1：当GTIOCB输入为1时，在GTIOCA输入的下降沿使能计数器清零。	R/W
b12	CSCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器清除启用	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止计数器清除1：当GTIOCA输入为0时，在GTIOCB输入上升沿使能计数器清除。	R/W
b13	CSCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器清除启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器清除1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器清除。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	CSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter clear enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	CSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable	0: Counter clear disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter clear enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	CSELCA	ELC_GPTA Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTA input 1: Counter clear enabled at the ELC_GPTA input.	R/W
b17	CSELCB	ELC_GPTB Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTB input 1: Counter clear enabled at the ELC_GPTB input.	R/W
b18	CSELCC	ELC_GPTC Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTC input 1: Counter clear enabled at the ELC_GPTC input.	R/W
b19	CSELCD	ELC_GPTD Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTD input 1: Counter clear enabled at the ELC_GPTD input.	R/W
b20	CSELCE	ELC_GPTE Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTE input 1: Counter clear enabled at the ELC_GPTE input.	R/W
b21	CSELCF	ELC_GPTF Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTF input 1: Counter clear enabled at the ELC_GPTF input.	R/W
b22	CSELCG	ELC_GPTG Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTG input 1: Counter clear enabled at the ELC_GPTG input.	R/W
b23	CSELCH	ELC_GPTH Event Source Counter Clear Enable	0: Counter clear disabled at the ELC_GPTH input 1: Counter clear enabled at the ELC_GPTH input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CCLR	Software Source Counter Clear Enable	0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register.	R/W

The GTCSR sets the source to clear the GTCNT counter.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of GTETRGB pin input.

CSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

CSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

CSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

Bit	Symbol	位名称	Description	R/W
b14	CSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器清除启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器清零1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器清零。	R/W
b15	CSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器清除启用	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁止计数器清除1：当GTIOCA输入为1时，在GTIOCB输入的下降沿使能计数器清除。	R/W
b16	CSELCA	ELC_GPTA事件源计数器清除启用	0：在ELC_GPTA输入处禁用计数器清除1：在ELC_GPTA输入处启用计数器清除。	R/W
b17	CSELCB	ELC_GPTB事件源计数器清除启用	0：在ELC_GPTB输入处禁用计数器清除1：在ELC_GPTB输入处启用计数器清除。	R/W
b18	CSELCC	ELC_GPTC事件源计数器清除启用	0：在ELC_GPTC输入处禁用计数器清除1：在ELC_GPTC输入处启用计数器清除。	R/W
b19	CSELCD	ELC_GPTD事件源计数器清除启用	0：在ELC_GPTD输入处禁用计数器清除1：在ELC_GPTD输入处启用计数器清除。	R/W
b20	CSELCE	ELC_GPTE事件源计数器清除启用	0：在ELC_GPTE输入处禁用计数器清除1：在ELC_GPTE输入处启用计数器清除。	R/W
b21	CSELCF	ELC_GPTF事件源计数器清除启用	0：在ELC_GPTF输入处禁用计数器清除1：在ELC_GPTF输入处启用计数器清除。	R/W
b22	CSELCG	ELC_GPTG事件源计数器清除启用	0：在ELC_GPTG输入处禁用计数器清除1：在ELC_GPTG输入处启用计数器清除。	R/W
b23	CSELCH	ELC_GPTH事件源计数器清除启用	0：在ELC_GPTH输入处禁用计数器清除1：在ELC_GPTH输入处启用计数器清除。	R/W
b30 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	CCLR	软件源计数器清零Enable	0：GTCLR寄存器禁止计数器清零1：GTCLR寄存器使能计数器清零。	R/W

GTCSR设置源以清除GTCNT计数器。

CSGTRGAR位（GTETRGA引脚上升沿输入源计数器清零使能）

CSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGAF位（GTETRGA引脚下降输入源计数器清零使能）

CSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGBR位（GTETRGB引脚上升沿输入源计数器清零使能）

CSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGBF位（GTETRGB引脚下降输入源计数器清零使能）

CSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCARBL位（在GTIOCB值低源计数器清除启用期间GTIOCA引脚上升输入）

CSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCB输入为0。

CSCARBH位（GTIOCB值高电平期间的GTIOCA引脚上升沿输入源计数器清零使能）

CSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCB输入为1。

CSCAFBL位（GTIOCB值低源计数器清除启用期间GTIOCA引脚下降输入）

CSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCB输入为0。

CSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables GTCNT counter clear on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

CSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables GTCNT counter clear on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

CSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables GTCNT counter clear on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

CSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables GTCNT counter clear on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

CSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables GTCNT counter clear on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

CSELCm bit (ELC_GPTm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables GTCNT counter clear at the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables GTCNT counter clear by GTCLR register.

23.2.8 General PWM Timer Up Count Source Select Register (GTUPSR)

Address(es): GPT32m.GTUPSR 4007 801Ch + 0100h × m (m = 0 to 3),
GPT16m.GTUPSR 4007 801Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	—	—	—	—	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input.	R/W
b1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input.	R/W
b2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input.	R/W

CSCAFBH位（在GTIOCB值高源计数器清除启用期间GTIOCA引脚下降输入）

当GTIOCB输入为1时，CSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCBRAL位（GTIOCA值低源计数器清除启用期间GTIOCB引脚上升沿输入）

当GTIOCA输入为0时，CSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSCBRAH位（GTIOCA值高源计数器清除启用期间GTIOCB引脚上升沿输入）

当GTIOCA输入为1时，CSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSCBFAL位（GTIOCA值低源计数器清除启用期间GTIOCB引脚下降输入）

当GTIOCA输入为0时，CSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCBFAH位（GTIOCA值高源计数器清零启用期间的GTIOCB引脚下降输入）

当GTIOCA输入为1时，CSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSELCm位（ELC_GPTm事件源计数器清除启用）（m=A到H）

CSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器清零。

CCLR位（软件源计数器清除使能）

CCLR位启用或禁用由GTCLR寄存器清除的GTCNT计数器。

23.2.8 通用PWM定时器向上计数源选择寄存器(GTUPSR)

Address(es): GPT32m.GTUPSR 4007 801Ch + 0100h × m (m = 0 to 3),
GPT16m.GTUPSR 4007 801Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	—	—	—	—	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	USGTRGAR	GTETRGA引脚上升输入源计数器计数启用	0：在GTETRGA输入的上升沿禁止向上计数1：在GTETRGA输入的上升沿使能向上计数。	R/W
b1	USGTRGAF	GTETRGA引脚下降输入源计数器计数启用	0：在GTETRGA输入的下降沿禁止向上计数1：在GTETRGA输入的下降沿使能向上计数。	R/W
b2	USGTRGBR	GTETRGB引脚上升输入源计数器计数启用	0：在GTETRGB输入的上升沿禁止计数器向上计数1：在GTETRGB输入的上升沿使能计数器向上计数。	R/W

Bit	Symbol	Bit name	Description	R/W
b3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	USCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter count up enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	USCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter count up enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	USCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter count up enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	USCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter count up enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	USCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter count up enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	USCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable	0: Counter count up disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter count up enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	USCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter count up enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	USCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable	0: Counter count up disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter count up enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	USELCA	ELC_GPTA Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTA input 1: Counter count up enabled at the ELC_GPTA input.	R/W
b17	USELCB	ELC_GPTB Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTB input 1: Counter count up enabled at the ELC_GPTB input.	R/W
b18	USELCC	ELC_GPTC Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTC input 1: Counter count up enabled at the ELC_GPTC input.	R/W
b19	USELCD	ELC_GPTD Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTD input 1: Counter count up enabled at the ELC_GPTD input.	R/W
b20	USELCE	ELC_GPTE Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTE input 1: Counter count up enabled at the ELC_GPTE input.	R/W
b21	USELCF	ELC_GPTF Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTF input 1: Counter count up is enabled at the ELC_GPTF input	R/W
b22	USELCG	ELC_GPTG Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTG input 1: Counter count up is enabled at the ELC_GPTG input	R/W
b23	USELCH	ELC_GPTH Event Source Counter Count Up Enable	0: Counter count up disabled at the ELC_GPTH input 1: Counter count up enabled at the ELC_GPTH input	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Bit	Symbol	位名称	Description	R/W
b3	USGTRGBF	GTETRGB引脚下降输入源计数器计数启用	0：在GTETRGB输入的下降沿禁止向上计数1：在GTETRGB输入的下降沿使能向上计数。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	USCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器计数启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器向上计数1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器向上计数。	R/W
b9	USCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器计数启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器加计数1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器加计数。	R/W
b10	USCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器计数启用	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁止计数器向上计数1：当GTIOCB输入为0时，在GTIOCA输入的下降沿使能计数器向上计数。	R/W
b11	USCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器计数启用	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁止计数器向上计数1：当GTIOCB输入为1时，在GTIOCA输入的下降沿使能计数器向上计数。	R/W
b12	USCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器计数启用	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止计数器向上计数1：当GTIOCA输入为0时，在GTIOCB输入上升沿使能计数器向上计数。	R/W
b13	USCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器计数启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器向上计数1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器向上计数。	R/W
b14	USCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器计数启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器向上计数1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器向上计数。	R/W
b15	USCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器计数启用	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁止计数器向上计数1：当GTIOCA输入为1时，在GTIOCB输入的下降沿使能计数器向上计数。	R/W
b16	USELCA	ELC_GPTA事件源计数器计数启用	0：在ELC_GPTA输入处禁用计数器向上计数1：在ELC_GPTA输入处启用计数器向上计数。	R/W
b17	USELCB	ELC_GPTB事件源计数器计数启用	0：在ELC_GPTB输入处禁用计数器向上计数1：在ELC_GPTB输入处启用计数器向上计数。	R/W
b18	USELCC	ELC_GPTC事件源计数器计数启用	0：在ELC_GPTC输入处禁用计数器向上计数1：在ELC_GPTC输入处启用计数器向上计数。	R/W
b19	USELCD	ELC_GPTD事件源计数器计数启用	0：在ELC_GPTD输入处禁用计数器向上计数1：在ELC_GPTD输入处启用计数器向上计数。	R/W
b20	USELCE	ELC_GPTE事件源计数器计数启用	0：在ELC_GPTE输入处禁用计数器向上计数1：在ELC_GPTE输入处启用计数器向上计数。	R/W
b21	USELCF	ELC_GPTF事件源计数器计数启用	0：在ELC_GPTF输入处禁用计数器向上计数1：在ELC_GPTF输入处启用计数器向上计数	R/W
b22	USELCG	ELC_GPTG事件源计数器计数启用	0：在ELC_GPTG输入处禁用计数器向上计数1：在ELC_GPTG输入处启用计数器向上计数	R/W
b23	USELCH	ELC_GPTH事件源计数器计数启用	0：在ELC_GPTH输入处禁用计数器向上计数1：在ELC_GPTH输入处启用计数器向上计数	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTUPSR将源设置为对GTCNT计数器进行计数。

当GTUPSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行计数。在这种情况下，GTCR.TPCS无效。

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of GTETRGB pin input.

USCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables the GTCNT counter count up on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

USCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

USCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

USCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

USCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

USCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

USCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

USCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

USGTRGAR位（GTETRGA引脚上升沿输入源计数器向上计数使能）

USGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGAF位（GTETRGA引脚下降输入源计数器向上计数使能）

USGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGBR位（GTETRGB引脚上升输入源计数器向上计数使能）

USGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGBF位（GTETRGB引脚下降输入源计数器向上计数使能）

USGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCARBL位（GTIOCB值低源计数器向上计数启用期间的GTIOCA引脚上升沿输入）

USCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为0。

USCARBH位（GTIOCB值高电平源计数器向上计数启用期间的GTIOCA引脚上升沿输入）

USCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为1。

USCAFBL位（GTIOCB值低源计数器向上计数启用期间的GTIOCA引脚下降输入）

USCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为0。

USCAFBH位（GTIOCB值高源计数器向上计数启用期间的GTIOCA引脚下降输入）

USCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为1。

USCBRAL位（GTIOCA值低源计数器向上计数启用期间的GTIOCB引脚上升输入）

USCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为0。

USCBRAH位（GTIOCA值高源计数器向上计数启用期间的GTIOCB引脚上升沿输入）

USCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为1。

USCBFAL位（GTIOCA值低源计数器向上计数启用期间的GTIOCB引脚下降输入）

USCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为0。

USCBFAH位（GTIOCA值高源计数器向上计数启用期间GTIOCB引脚下降输入）

USCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为1。

USELCm位（ELC_GPTm事件源计数器向上计数启用）（m=A到H）

USELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器向上计数。

23.2.9 General PWM Timer Down Count Source Select Register (GTDNSR)

Address(es): GPT32m.GTDNSR 4007 8020h + 0100h × m (m = 0 to 3),
GPT16m.GTDNSR 4007 8020h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	—	—	—	—	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input.	R/W
b1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input.	R/W
b2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input.	R/W
b3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: Counter count down enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	DSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: Counter count down enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	DSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: Counter count down enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	DSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: Counter count down enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	DSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: Counter count down enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	DSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable	0: Counter count down disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: Counter count down enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

23.2.9 通用PWM定时器递减计数源选择寄存器(GTDNSR)

Address(es): GPT32m.GTDNSR 4007 8020h + 0100h × m (m = 0 to 3),
GPT16m.GTDNSR 4007 8020h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	—	—	—	—	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DSGTRGAR	GTETRGA引脚上升输入源计数器倒计时启用	0：在GTETRGA输入的上升沿禁用计数器递减计数1：在GTETRGA输入的上升沿启用计数器递减计数。	R/W
b1	DSGTRGAF	GTETRGA引脚下降输入源计数器倒计时启用	0：在GTETRGA输入的下降沿禁止计数器减计数1：在GTETRGA输入的下降沿使能计数器减计数。	R/W
b2	DSGTRGBR	GTETRGB引脚上升输入源计数器倒计时启用	0：在GTETRGB输入的上升沿禁用计数器减计数1：在GTETRGB输入的上升沿启用计数器减计数。	R/W
b3	DSGTRGBF	GTETRGB引脚下降输入源计数器倒计时启用	0：在GTETRGB输入的下降沿禁用计数器递减计数1：在GTETRGB输入的下降沿启用计数器递减计数。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	DSCARBL	GTIOCA引脚上升期间输入GTIOCB值低源计数器倒计时启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器减计数1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器减计数。	R/W
b9	DSCARBH	GTIOCA引脚上升期间输入GTIOCB值高源计数器倒计时启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器减计数1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器减计数。	R/W
b10	DSCAFBL	GTIOCA引脚下降期间输入GTIOCB值低源计数器倒计时启用	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁止计数器减计数1：当GTIOCB输入为0时，在GTIOCA输入的下降沿使能计数器减计数。	R/W
b11	DSCAFBH	GTIOCA引脚下降期间输入GTIOCB值高源计数器倒计时启用	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁止计数器减计数1：当GTIOCB输入为1时，在GTIOCA输入的下降沿使能计数器减计数。	R/W
b12	DSCBRAL	GTIOCB引脚上升期间输入GTIOCA值低源计数器倒计时启用	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止计数器减计数1：当GTIOCA输入为0时，在GTIOCB输入上升沿使能计数器减计数。	R/W
b13	DSCBRAH	GTIOCB引脚上升期间输入GTIOCA值高源计数器倒计时启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器减计数1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器减计数。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	DSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: Counter count down enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	DSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable	0: Counter count down disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: Counter count down enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTA input 1: Counter count down enabled at the ELC_GPTA input.	R/W
b17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTB input 1: Counter count down enabled at the ELC_GPTB input.	R/W
b18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTC input 1: Counter count down enabled at the ELC_GPTC input.	R/W
b19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTD input 1: Counter count down enabled at the ELC_GPTD input.	R/W
b20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTE input 1: Counter count down enabled at the ELC_GPTE input.	R/W
b21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input.	R/W
b22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTG input 1: Counter count down enabled at the ELC_GPTG input.	R/W
b23	DSELCH	ELC_GPTH Event Source Counter Count Down Enable	0: Counter count down disabled at the ELC_GPTH input 1: Counter count down enabled at the ELC_GPTH input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register, but the GTCNT counter set by GTCR.TPCS does not perform the count.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of GTETRGB pin input.

DSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

DSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

DSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of GTIOCA pin input, when

Bit	Symbol	位名称	Description	R/W
b14	DSCBFAL	在GTIOCB引脚下降输入GTIOCA值低源计数器倒计时启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器减计数1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器减计数。	R/W
b15	DSCBFAH	在GTIOCB引脚下降输入GTIOCA值高源计数器倒计时启用	0：当GTIOCA输入为1时，在GTIOCB输入下降沿禁止计数器减计数1：当GTIOCA输入为1时，在GTIOCB输入下降沿使能计数器减计数。	R/W
b16	DSELCA	ELC_GPTA事件源计数器倒计时启用	0：在ELC_GPTA输入处禁用计数器递减计数1：在ELC_GPTA输入处启用计数器递减计数。	R/W
b17	DSELCB	ELC_GPTB事件源计数器倒计时启用	0：在ELC_GPTB输入处禁用计数器递减计数1：在ELC_GPTB输入处启用计数器递减计数。	R/W
b18	DSELCC	ELC_GPTC事件源计数器倒计时启用	0：在ELC_GPTC输入处禁用计数器递减计数1：在ELC_GPTC输入处启用计数器递减计数。	R/W
b19	DSELCD	ELC_GPTD事件源计数器倒计时启用	0：在ELC_GPTD输入处禁用计数器递减计数1：在ELC_GPTD输入处启用计数器递减计数。	R/W
b20	DSELCE	ELC_GPTE事件源计数器倒计时启用	0：在ELC_GPTE输入处禁用计数器递减计数1：在ELC_GPTE输入处启用计数器递减计数。	R/W
b21	DSELCF	ELC_GPTF事件源计数器倒计时启用	0：在ELC_GPTF输入处禁用计数器递减计数1：在ELC_GPTF输入处启用计数器递减计数。	R/W
b22	DSELCG	ELC_GPTG事件源计数器倒计时启用	0：在ELC_GPTG输入处禁用计数器递减计数1：在ELC_GPTG输入处启用计数器递减计数。	R/W
b23	DSELCH	ELC_GPTH事件源计数器倒计时启用	0：在ELC_GPTH输入处禁用计数器递减计数1：在ELC_GPTH输入处启用计数器递减计数。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDNSR将源设置为对GTCNT计数器进行倒计时。

当GTDNSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源递减计数，但由GTCR.TPCS设置的GTCNT计数器不执行计数。

DSGTRGAR位（GTETRGA引脚上升沿输入源计数器倒计时使能）

DSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGAF位（GTETRGA引脚下降输入源计数器倒计时使能）

DSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGBR位（GTETRGB引脚上升输入源计数器倒计时使能）

DSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGBF位（GTETRGB引脚下降输入源计数器倒计时使能）

DSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCARBL位（GTIOCB值低源计数器倒计时期间GTIOCA引脚上升沿输入Enable）

DSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCB输入为0。

DSCARBH位（GTIOCB值高电平期间的GTIOCA引脚上升沿输入源计数器向下计数Enable）

DSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCB输入为1。

DSCAFBL位（GTIOCB值低源计数器向下计数期间GTIOCA引脚下降输入Enable）

DSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当

GTIOCB input is 0.

DSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

DSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

DSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

DSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

DSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

23.2.10 General PWM Timer Input Capture Source Select Register A(GTICASR)

Address(es): GPT32m.GTICASR 4007 8024h + 0100h × m (m = 0 to 3),
GPT16m.GTICASR 4007 8024h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	—	—	—	—	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input.	R/W
b1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input.	R/W

GTIOCB输入为0。

DSCAFBH位（GTIOCB值高源计数器倒计时期间GTIOCA引脚下降输入Enable）

DSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当GTIOCB输入为1。

DSCBRAL位（GTIOCA值低源计数器向下计数期间GTIOCB引脚上升沿输入Enable）

DSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCA输入为0。

DSCBRAH位（GTIOCA值高源计数器倒计时期间GTIOCB引脚上升沿输入Enable）

DSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCA输入为1。

DSCBFAL位（GTIOCA值低源计数器倒计时期间GTIOCB引脚下降输入Enable）

DSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当GTIOCA输入为0。

DSCBFAH位（GTIOCA值高源计数器倒计时期间GTIOCB引脚下降输入Enable）

DSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当GTIOCA输入为1。

DSELCm位（ELC_GPTm事件源计数器倒计时启用）（m=A到H）

DSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器倒计时。

23.2.10 通用PWM定时器输入捕捉源选择寄存器A(GTICASR)

Address(es): GPT32m.GTICASR 4007 8024h + 0100h × m (m = 0 to 3),
GPT16m.GTICASR 4007 8024h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	—	—	—	—	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ASGTRGAR	GTETRGA引脚上升输入源GTCCRA输入捕捉使能	0：在GTETRGA输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGA输入的上升沿启用GTCCRA输入捕捉。	R/W
b1	ASGTRGAF	GTETRGA引脚下降输入源GTCCRA输入捕捉使能	0：在GTETRGA输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGA输入的下降沿启用GTCCRA输入捕捉。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input.	R/W
b3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ASCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	ASCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	ASCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	ASCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	ASCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	ASCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	ASCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	ASCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTA input 1: GTCCRA input capture enabled at the ELC_GPTA input.	R/W
b17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTB input 1: GTCCRA input capture enabled at the ELC_GPTB input.	R/W
b18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTC input 1: GTCCRA input capture enabled at the ELC_GPTC input.	R/W
b19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTD input 1: GTCCRA input capture enabled at the ELC_GPTD input.	R/W
b20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTE input 1: GTCCRA input capture enabled at the ELC_GPTE input.	R/W
b21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTF input 1: GTCCRA input capture enabled at the ELC_GPTF input.	R/W
b22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTG input 1: GTCCRA input capture enabled at the ELC_GPTG input.	R/W
b23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable	0: GTCCRA input capture disabled at the ELC_GPTH input 1: GTCCRA input capture enabled at the ELC_GPTH input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	位名称	Description	R/W
b2	ASGTRGBR	GTETRGB引脚上升输入源 GTCCRA输入捕捉使能	0：在GTETRGB输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGB输入的上升沿启用GTCCRA输入捕捉。	R/W
b3	ASGTRGBF	GTETRGB引脚下降输入源 GTCCRA输入捕捉使能	0：在GTETRGB输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGB输入的下降沿启用GTCCRA输入捕捉。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	ASCARBL	GTIOCB值低源期间的GTIOCA引脚上升输入 GTCCRA输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入的上升沿禁用GTCCRA输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入的上升沿启用GTCCRA输入捕捉。	R/W
b9	ASCARBH	GTIOCB值高源期间的GTIOCA引脚上升输入 GTCCRA输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁用GTCCRA输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入上升沿启用GTCCRA输入捕捉。	R/W
b10	ASCAFBL	GTIOCA引脚下降期间输入 GTIOCB价值低来源 GTCCRA输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁用GTCCRA输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入的下降沿启用GTCCRA输入捕捉。	R/W
b11	ASCAFBH	GTIOCA引脚下降期间输入 GTIOCB价值高来源 GTCCRA输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁用GTCCRA输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入的下降沿启用GTCCRA输入捕捉。	R/W
b12	ASCBRAL	GTIOCA值低源期间的GTIOCB引脚上升输入 GTCCRA输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入的上升沿禁用GTCCRA输入捕捉1：当GTIOCA输入为0时，在GTIOCB输入的上升沿启用GTCCRA输入捕捉。	R/W
b13	ASCBRAH	GTIOCA值高源期间的GTIOCB引脚上升输入 GTCCRA输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入的上升沿禁用GTCCRA输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入的上升沿启用GTCCRA输入捕捉。	R/W
b14	ASCBFAL	在GTIOCB引脚下降输入 GTIOCA价值低来源 GTCCRA输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁用GTCCRA输入捕捉1：当GTIOCA输入为0时，在GTIOCB输入的下降沿启用GTCCRA输入捕捉。	R/W
b15	ASCBFAH	在GTIOCB引脚下降输入 GTIOCA价值高来源 GTCCRA输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁用GTCCRA输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入的下降沿启用GTCCRA输入捕捉。	R/W
b16	ASELCA	ELC_GPTA事件源 GTCCRA输入捕捉使能	0：在ELC_GPTA输入处禁用GTCCRA输入捕捉1：在ELC_GPTA输入处启用GTCCRA输入捕捉。	R/W
b17	ASELCB	ELC_GPTB事件源 GTCCRA输入捕捉使能	0：在ELC_GPTB输入处禁用GTCCRA输入捕捉1：在ELC_GPTB输入处启用GTCCRA输入捕捉。	R/W
b18	ASELCC	ELC_GPTC事件源 GTCCRA输入捕捉使能	0：在ELC_GPTC输入处禁用GTCCRA输入捕捉1：在ELC_GPTC输入处启用GTCCRA输入捕捉。	R/W
b19	ASELCD	ELC_GPTD事件源 GTCCRA输入捕捉使能	0：在ELC_GPTD输入处禁用GTCCRA输入捕捉1：在ELC_GPTD输入处启用GTCCRA输入捕捉。	R/W
b20	ASELCE	ELC_GPTE事件源 GTCCRA输入捕捉使能	0：在ELC_GPTE输入处禁用GTCCRA输入捕捉1：在ELC_GPTE输入处启用GTCCRA输入捕捉。	R/W
b21	ASELCF	ELC_GPTF事件源 GTCCRA输入捕捉使能	0：在ELC_GPTF输入处禁用GTCCRA输入捕捉1：在ELC_GPTF输入处启用GTCCRA输入捕捉。	R/W
b22	ASELCG	ELC_GPTG事件源 GTCCRA输入捕捉使能	0：在ELC_GPTG输入处禁用GTCCRA输入捕捉1：在ELC_GPTG输入处启用GTCCRA输入捕捉。	R/W
b23	ASELCH	ELC_GPTH事件源 GTCCRA输入捕捉使能	0：在ELC_GPTH输入处禁用GTCCRA输入捕捉1：在ELC_GPTH输入处启用GTCCRA输入捕捉。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

The GTICASR sets the source of input capture for GTCCRA.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables input capture for GTCCRA on the rising edge of GTETRGA pin input.

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables input capture for GTCCRA on the falling edge of GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables input capture for GTCCRA on the rising edge of GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables input capture for GTCCRA on the falling edge of GTETRGB pin input.

ASCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables input capture for GTCCRA on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

ASCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables input capture for GTCCRA on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

ASCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables input capture for GTCCRA on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

ASCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables input capture for GTCCRA on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

ASCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables input capture for GTCCRA on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

ASCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables input capture for GTCCRA on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

ASCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables input capture for GTCCRA on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

ASCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables input capture for GTCCRA on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables input capture for GTCCRA at the ELC_GPTm event input.

GTICASR设置GTCCRA的输入捕获源。

ASGTRGAR位（GTETRGA引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGAF位（GTETRGA引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBR位（GTETRGB引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBF位（GTETRGB引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCARBL位（GTIOCB值低电平期间GTIOCA引脚上升沿输入源GTCCRA输入捕捉Enable）

ASCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为0。

ASCARBH位（GTIOCB值高电平期间GTIOCA引脚的上升沿输入源GTCCRA输入捕捉Enable）

ASCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为1。

ASCAFBL位（GTIOCB值低电平期间GTIOCA引脚下降输入源GTCCRA输入捕捉Enable）

ASCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为0。

ASCAFBH位（GTIOCB值高电平期间GTIOCA引脚下降输入源GTCCRA输入捕捉Enable）

ASCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为1。

ASCBRAL位（GTIOCA值低电平期间GTIOCB引脚上升沿输入源GTCCRA输入捕捉Enable）

ASCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为0。

ASCBRAH位（GTIOCA值高电平期间GTIOCB引脚的上升沿输入源GTCCRA输入捕捉Enable）

ASCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为1。

ASCBFAL位（GTIOCA值低电平期间GTIOCB引脚下降输入源GTCCRA输入捕捉Enable）

ASCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为0。

ASCBFAH位（GTIOCA值高电平期间GTIOCB引脚下降输入源GTCCRA输入捕捉Enable）

ASCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为1。

ASELCm位（ELC_GPTm事件源计数器GTCCRA输入捕捉使能）（m=A到H）

ASELCm位在ELC_GPTm事件输入处启用或禁用GTCCRA的输入捕捉。

23.2.11 General PWM Timer Input Capture Source Select Register B(GTICBSR)

Address(es): GPT32m.GTICBSR 4007 8028h + 0100h × m (m = 0 to 3),
GPT16m.GTICBSR 4007 8028h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	—	—	—	—	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input.	R/W
b1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input.	R/W
b2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input.	R/W
b3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	BSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCA input when GTIOCB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	BSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	BSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCA input when GTIOCB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	BSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	BSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the rising edge of GTIOCB input when GTIOCA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W

23.2.11 通用PWM定时器输入捕捉源选择寄存器B(GTICBSR)

Address(es): GPT32m.GTICBSR 4007 8028h + 0100h × m (m = 0 to 3),
GPT16m.GTICBSR 4007 8028h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	—	—	—	—	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BSGTRGAR	GTETRGA引脚上升输入源GTCCRB输入捕捉使能	0：在GTETRGA输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGA输入的上升沿启用GTCCRB输入捕捉。	R/W
b1	BSGTRGAF	GTETRGA引脚下降输入源GTCCRB输入捕捉使能	0：在GTETRGA输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGA输入的下降沿启用GTCCRB输入捕捉。	R/W
b2	BSGTRGBR	GTETRGB引脚上升输入源GTCCRB输入捕捉使能	0：在GTETRGB输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGB输入的上升沿启用GTCCRB输入捕捉。	R/W
b3	BSGTRGBF	GTETRGB引脚下降输入源GTCCRB输入捕捉使能	0：在GTETRGB输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGB输入的下降沿启用GTCCRB输入捕捉。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	BSCARBL	GTIOCB值低源期间的GTIOCA引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁用GTCCRB输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入上升沿启用GTCCRB输入捕捉。	R/W
b9	BSCARBH	GTIOCB值高源期间的GTIOCA引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁用GTCCRB输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入上升沿启用GTCCRB输入捕捉。	R/W
b10	BSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源 GTCCRB输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁用GTCCRB输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入的下降沿启用GTCCRB输入捕捉。	R/W
b11	BSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源 GTCCRB输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁用GTCCRB输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入的下降沿启用GTCCRB输入捕捉。	R/W
b12	BSCBRAL	GTIOCA值低源期间的GTIOCB引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入的上升沿禁用GTCCRB输入捕捉1：当GTIOCA输入为0时，在GTIOCB输入的上升沿启用GTCCRB输入捕捉。	R/W
b13	BSCBRAH	GTIOCA值高源期间的GTIOCB引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入的上升沿禁用GTCCRB输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入的上升沿启用GTCCRB输入捕捉。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	BSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	BSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled on the falling edge of GTIOCB input when GTIOCA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTA input 1: GTCCRB input capture enabled at the ELC_GPTA input.	R/W
b17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTB input 1: GTCCRB input capture enabled at the ELC_GPTB input.	R/W
b18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTC input 1: GTCCRB input capture enabled at the ELC_GPTC input.	R/W
b19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTD input 1: GTCCRB input capture enabled at the ELC_GPTD input.	R/W
b20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTE input 1: GTCCRB input capture enabled at the ELC_GPTE input.	R/W
b21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTF input 1: GTCCRB input capture enabled at the ELC_GPTF input.	R/W
b22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTG input 1: GTCCRB input capture enabled at the ELC_GPTG input.	R/W
b23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable	0: GTCCRB input capture disabled at the ELC_GPTH input 1: GTCCRB input capture enabled at the ELC_GPTH input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTICBSR sets the source of input capture for GTCCRB.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables input capture for GTCCRB on the rising edge of GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables input capture for GTCCRB on the falling edge of GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables input capture for GTCCRB on the falling edge of GTETRGB pin input.

BSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables input capture for GTCCRB on the rising edge of GTIOCA pin input, when GTIOCB input is 0.

BSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables input capture for GTCCRB on the rising edge of GTIOCA pin input, when GTIOCB input is 1.

BSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables input capture for GTCCRB on the falling edge of GTIOCA pin input, when GTIOCB input is 0.

Bit	Symbol	位名称	Description	R/W
b14	BSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源GTCCRB输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁用GTCCRB输入捕捉1：当GTIOCA输入为0时，在GTIOCB输入的下降沿启用GTCCRB输入捕捉。	R/W
b15	BSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源GTCCRB输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁用GTCCRB输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入的下降沿启用GTCCRB输入捕捉。	R/W
b16	BSELCA	ELC_GPTA事件源GTCCRB输入捕捉使能	0：在ELC_GPTA输入处禁用GTCCRB输入捕捉1：在ELC_GPTA输入处启用GTCCRB输入捕捉。	R/W
b17	BSELCB	ELC_GPTB事件源GTCCRB输入捕捉使能	0：在ELC_GPTB输入处禁用GTCCRB输入捕捉1：在ELC_GPTB输入处启用GTCCRB输入捕捉。	R/W
b18	BSELCC	ELC_GPTC事件源GTCCRB输入捕捉使能	0：在ELC_GPTC输入处禁用GTCCRB输入捕捉1：在ELC_GPTC输入处启用GTCCRB输入捕捉。	R/W
b19	BSELCD	ELC_GPTD事件源GTCCRB输入捕捉使能	0：在ELC_GPTD输入处禁用GTCCRB输入捕捉1：在ELC_GPTD输入处启用GTCCRB输入捕捉。	R/W
b20	BSELCE	ELC_GPTE事件源GTCCRB输入捕捉使能	0：在ELC_GPTE输入处禁用GTCCRB输入捕捉1：在ELC_GPTE输入处启用GTCCRB输入捕捉。	R/W
b21	BSELCF	ELC_GPTF事件源GTCCRB输入捕捉使能	0：在ELC_GPTF输入处禁用GTCCRB输入捕捉1：在ELC_GPTF输入处启用GTCCRB输入捕捉。	R/W
b22	BSELCG	ELC_GPTG事件源GTCCRB输入捕捉使能	0：在ELC_GPTG输入处禁用GTCCRB输入捕捉1：在ELC_GPTG输入处启用GTCCRB输入捕捉。	R/W
b23	BSELCH	ELC_GPTH事件源GTCCRB输入捕捉使能	0：在ELC_GPTH输入处禁用GTCCRB输入捕捉1：在ELC_GPTH输入处启用GTCCRB输入捕捉。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTICBSR设置GTCCRB的输入捕获源。

BSGTRGAR位（GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGAF位（GTETRGA引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBR位（GTETRGB引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBF位（GTETRGB引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSCARBL位（GTIOCB值低电平期间GTIOCA引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为0。

BSCARBH位（GTIOCB值高电平期间GTIOCA引脚的上升沿输入源GTCCRB输入捕捉Enable)

BSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为1。

BSCAFBL位（GTIOCB值低电平期间GTIOCA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为0。

BSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables input capture for GTCCRB on the falling edge of GTIOCA pin input, when GTIOCB input is 1.

BSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables input capture for GTCCRB on the rising edge of GTIOCB pin input, when GTIOCA input is 0.

BSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables input capture for GTCCRB on the rising edge of GTIOCB pin input, when GTIOCA input is 1.

BSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables input capture for GTCCRB on the falling edge of GTIOCB pin input, when GTIOCA input is 0.

BSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables input capture for GTCCRB on the falling edge of GTIOCB pin input, when GTIOCA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables input capture for GTCCRB at the ELC_GPTm event input.

23.2.12 General PWM Timer Control Register (GTCR)

Address(es): GPT32m.GTCR 4007 802Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCR 4007 802Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CST	Count Start	0: Count operation is stopped 1: Count operation is performed.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

BSCAFBH位（GTIOCB值高电平期间GTIOCA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为1。

BSCBRAL位（GTIOCA值低电平期间GTIOCB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为0。

BSCBRAH位（GTIOCA值高电平期间GTIOCB引脚的上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为1。

BSCBFAL位（GTIOCA值低电平期间GTIOCB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为0。

BSCBFAH位（GTIOCA值高电平期间GTIOCB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为1。

BSELCm位（ELC_GPTm事件源计数器GTCCRB输入捕捉使能）（m=A到H）

BSELCm位在ELC_GPTm事件输入处启用或禁用GTCCRB的输入捕捉。

23.2.12 通用PWM定时器控制寄存器(GTCR)

Address(es): GPT32m.GTCR 4007 802Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCR 4007 802Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CST	计数开始	0：停止计数1：进行计数。	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b18 to b16	MD[2:0]	Mode Select	b18 b16 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	TPCS[2:0]	Timer Prescaler Select	b26 b24 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTCR controls the GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input enabled by GTSSR as the counter start source, occurs
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTOP bit at 1
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input enabled by GTSSR as the counter stop source, occurs
- 0 is written by software directly.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

TPCS[2:0] bits (Timer Prescaler Select)

The TPCS[2:0] bits select the clock for the GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[2:0] bits must be set while the GTCNT operation is stopped.

Bit	Symbol	位名称	Description	R/W
b18 to b16	MD[2:0]	模式选择	b18b16000：Saw-wavePWM模式（单缓冲或双缓冲均可）001：Saw-waveone-shot脉冲模式（固定缓冲操作）010：设置禁止011：设置禁止100：三角波PWM模式1（波谷32位传输）（可单缓冲器或双缓冲器）101：三角波PWM模式2（波峰和波谷32位传输）（单缓冲器或双缓冲器可能）110：三角波PWM模式3（波谷64位传输）（固定缓冲操作）111：禁止设置。	R/W
b23 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b24	TPCS[2:0]	定时器预分频器选择	b26 b24 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024.	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTCR控制GTCNT。

CST位（计数开始）

CST位控制GTCNT计数器的启动和停止。

[Setting conditions]

- GTSTR值，其中与位号关联的通道号设置为1，GTSSR.CSTRT位为1
- 发生由GTSSR作为计数器启动源启用的ELC事件输入或GTIOCAGTIOCBGTETRn端口输入
- 1由软件直接编写。

[Clearing conditions]

- GTSTP值，其中与位号关联的通道号设置为1，且GTSSR.CSTOP位为1
- 发生由GTSSR作为计数器停止源启用的ELC事件输入或GTIOCAGTIOCBGTETRn端口输入
- 0由软件直接写入。

MD[2:0]位（模式选择）

MD[2:0]位选择GPT操作模式。当GTCNT操作停止时，必须设置MD[2:0]位。

TPCS[2:0]位（定时器预分频器选择）

TPCS[2:0]位选择GTCNT的时钟。可为每个通道独立选择时钟预分频器。
当GTCNT操作停止时，必须设置TPCS[2:0]位。

23.2.13 General PWM Timer Count Direction and Duty Setting Register (GTUDDTYC)

Address(es): GPT32m.GTUDDTYC 4007 8030h + 0100h × m (m = 0 to 3),
GPT16m.GTUDDTYC 4007 8030h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	UD	Count Direction Setting	0: GTCNT counts down 1: GTCNT counts up.	R/W
b1	UDF	Forcible Count Direction Setting	0: Not forcibly set 1: Forcibly set.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, 16	OADTY[1:0]	GTIOCA Output Duty Setting	b17 b16 0 x: GTIOCA pin duty depends on compare match 1 0: GTIOCA pin duty 0% 1 1: GTIOCA pin duty 100%.	R/W
b18	OADTYF	Forcible GTIOCA Output Duty Setting	0: Not forcibly set 1: Forcibly set.	R/W
b19	OADTYR	GTIOCA Output Value Selecting after Releasing 0% or 100% Duty Setting	0: Apply output value set in 0% or 100% duty to GTIOA[3:2] function after releasing 0% or 100% duty setting 1: Apply masked compare match output value to GTIOA[3:2] function after releasing 0% or 100% duty setting.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	OBDTY[1:0]	GTIOCB Output Duty Setting	b25 b24 0 x: GTIOCB pin duty is depend on compare match 1 0: GTIOCB pin duty 0% 1 1: GTIOCB pin duty 100%.	R/W
b26	OBDTYF	Forcible GTIOCB Output Duty Setting	0: Not forcibly set 1: Forcibly set.	R/W
b27	OBDTYR	GTIOCB Output Value Selecting after Releasing 0% or 100% Duty Setting	0: Apply output value set in 0% or 100% duty to GTIOB[3:2] function after releasing 0% or 100% duty setting 1: Apply masked compare match output value to GTIOB[3:2] function after releasing 0% or 100% duty setting.	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

The GTUDDTYC sets the direction in which GTCNT counts (up-counting or down-counting), and sets the duty of the GTIOCA/GTIOCB pin output.

Count Direction:

- In saw-wave mode

When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after GTCNT value becomes 0).

When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after GTCNT value

23.2.13 通用PWM定时器计数方向和占空比设置寄存器(GTUDDTYC)

Address(es): GPT32m.GTUDDTYC 4007 8030h + 0100h × m (m = 0 to 3),
GPT16m.GTUDDTYC 4007 8030h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	UD	计数方向设置	0：GTCNT向下计数1： GTCNT向上计数。	R/W
b1	UDF	强制计数方向 Setting	0：不强制设置1 ：强制设置。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, 16	OADTY[1:0]	GTIOCA输出占空比设置	b17b160x：GTIOCA引脚占空比取决于比较匹配10： GTIOCA引脚占空比0%11：GTIOCA引脚占空比100% 。	R/W
b18	OADTYF	强制GTIOCA输出占空比 Setting	0：不强制设置1 ：强制设置。	R/W
b19	OADTYR	GTIOCA输出值 释放0%或100%占空比设置后选择	0：释放0%或100%占空比设置后，将设置为0%或100%占空比的输出值应用到GTIOA[3:2]功能1：释放0%后，将屏蔽比较匹配输出值应用到GTIOA[3:2]功能或100%占空比设置。	R/W
b23 to b20	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	OBDTY[1:0]	GTIOCB输出占空比设置	b25b240x：GTIOCB引脚占空比取决于比较匹配10：G TIOCB引脚占空比0%11：GTIOCB引脚占空比100%。	R/W
b26	OBDTYF	强制GTIOCB输出占空比 Setting	0：不强制设置1 ：强制设置。	R/W
b27	OBDTYR	GTIOCB输出值 释放0%或100%占空比设置后选择	0：释放0%或100%占空比设置后，将设置为0%或100%占空比的输出值应用到GTIOB[3:2]功能1：释放0%后，将屏蔽比较匹配输出值应用到GTIOB[3:2]功能或100%占空比设置。	R/W
b31 to b28	—	Reserved	这些位被读取为0。写入值应为0。	R/W

x: Don't care

GTUDDTYC设置GTCNT计数的方向（向上计数或向下计数），并设置
GTIOCAGTIOCB引脚输出。

Count Direction:

- 在锯齿波模式下

如果在向上计数期间将UD值设置为0，则计数方向会在溢出时发生变化（GTCNT值变为GTPR值后与计数时钟同步的时序）。当在递减计数期间将UD值设置为1时，计数方向会在下溢（GTCNT值变为0后与计数时钟同步的时序）下发生变化。

当UD值从1变为0且UDF位为0且计数停止时，计数器开始向上计数，并且计数方向在溢出时改变（与GTCNT值之后的计数时钟同步的时序）

becomes GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after GTCNT value becomes 0).

When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.

- In triangle-wave mode

When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.

When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, this bit must be returned to 0 before counting starts.

Output duty

- In saw-wave mode

When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR). When the OADTY/OBDTY value changes during down-counting, the duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0). When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting is stopped, the output duty is reflected at the starting counter operation.

- In triangle-wave mode

When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow.

When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow. When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at the starting counter operation.

OmDTY[1:0] bits (GTIOCm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty (0%, 100% or compare match control) of the GTIOCm pin.

OmDTYF bit (ForcibleGTIOCm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. This bit must be set to 0 during counter operation. When this bit is set to 1 while counting stops, this bit must be returned to 0 until the first period ends after the counter starts.

OmDTYR bit (GTIOCm Output Value Selecting after Releasing 0% or 100% Duty Setting) (m = A, B)

The OmDTYR bit selects the value that is the object of output retained or toggled at cycle end, when the control changes from 0% or 100% duty setting to compare match for GTIOCm pin and GTIOR. The GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

While the duty 0%/100% setting operation is running, compare match operation is continued inside the GPT32. When the OmDTYR bit is set to 1, the GTIOCm pin is in the output state selected by the GTIOR.GTIOm [3:2] bit at the end of the cycle in this compare match operation.

变为GTPR值）。当UDF位为0时UD值从0变为1并且在计数停止时，计数器开始递减计数并且计数方向在下溢时改变（GTCNT值变为0后与计数时钟同步的时序）。

当计数停止时UDF位设置为1时，UD位值在计数开始时反映在计数方向上。

- 在三角波模式

计数过程中UD值变化时，计数方向不变。当UD值改变而
UDF位为0且计数停止，计数开始时变化不反映在计数方向上。

当计数停止时UDF位设置为1时，UD值在计数开始时反映在计数方向上。

UD位（计数方向设置）

UD位设置GTCNT的计数方向（向上计数或向下计数）。

UDF位（强制计数方向设置）

当GTCNT开始操作时，UDF位将计数方向强制设置为UD值。在计数器操作期间，只能将0写入该位。当计数停止时向该位写入1时，该位必须在计数开始前返回0。

输出占空比

- 在锯齿波模式下

当OADTYOBDTY值在递增计数期间发生变化时，占空比反映在溢出处(GTCNT=GTPR)。
当向下计数期间OADTYOBDTY值发生变化时，占空比反映为下溢(GTCNT=0)。

当OADTYFOBDTYF位为0且OADTYOBDTY值变为1且计数停止时，输出占空比不会反映在开始计数器操作中。当计数方向向上时，输出占空比反映在溢出处(GTCNT=GTPR)。当计数方向向下时，输出占空比反映为下溢(GTCNT=0)。当OADTYOBDTY值变为0且OADTYFOBDTYF位为1且计数停止时，输出占空比反映在开始计数器操作中。

- 在三角波模式

当计数期间OADTYOBDTY值发生变化时，占空比反映为下溢。

当OADTYFOBDTYF位为0且OADTYOBDTY值变为1且计数停止时，输出占空比不会反映在开始计数器操作中。输出占空比反映在下溢处。当OADTYOBDTY值变为0且OADTYFOBDTYF位为1且计数停止时，输出占空比反映在开始计数器操作中。

OmDTY[1:0]位（GTIOCm输出占空比设置）（m=A，B）

OmDTY[1:0]位设置GTIOCm引脚的输出占空比（0%、100%或比较匹配控制）。

OmDTYF位(ForcibleGTIOCm输出占空比设置)(m=A B)

OmDTYF位强制将输出占空比设置为OmDTY设置。在计数器操作期间，该位必须设置为0。当计数停止时该位设置为1时，该位必须返回0，直到计数器开始后第一个周期结束。

OmDTYR位（释放0%或100%占空比设置后选择GTIOCm输出值）（m=A、B）

当控制从0%或100%占空比设置更改为GTIOCm引脚和GTIOR比较匹配时，OmDTYR位选择作为输出对象在周期结束时保持或切换的值。GTIOm[3:2]位设置为00b（输出在循环结束时保留）或GTIOR.GTIOm[3:2]位设置为11b（输出在循环结束时切换）。

在运行占空比0%100%设置操作时，GPT32内部继续进行比较匹配操作。当OmDTYR位设置为1时，GTIOCm引脚在此比较匹配操作的周期结束时处于由GTIOR.GTIOm[3:2]位选择的输出状态。

23.2.14 General PWM Timer I/O Control Register (GTIOR)

Address(es): GPT32m.GTIOR 4007 8034h + 0100h × m (m = 0 to 3),
GPT16m.GTIOR 4007 8034h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	GTIOA[4:0]	GTIOCA Pin Function Select	See Table 23.5.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	OADFLT	GTIOCA Pin Output Value Setting at the Count Stop	0: The GTIOCA pin outputs low when counting stops 1: The GTIOCA pin outputs high when counting stops.	R/W
b7	OAHLD	GTIOCA Pin Output Setting at the Start/Stop Count	0: The GTIOCA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCA pin output level is retained at the start or stop of counting.	R/W
b8	OAE	GTIOCA Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b10, b9	OADF[1:0]	GTIOCA Pin Disable Value Setting	b10 b9 0 0: Output disable is prohibited 0 1: GTIOCA pin is set to Hi-Z on output disable 1 0: GTIOCA pin is set to 0 on output disable 1 1: GTIOCA pin is set to 1 on output disable.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	NFAEN	Noise Filter A Enable	0: The noise filter for the GTIOCA pin is disabled 1: The noise filter for the GTIOCA pin is enabled.	R/W
b15, b14	NFCSA[1:0]	Noise Filter A Sampling Clock Select	b15 b14 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W
b20 to b16	GTIOB[4:0]	GTIOCB Pin Function Select	See Table 23.5.	R/W
b21	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b22	OBDFLT	GTIOCB Pin Output Value Setting at the Count Stop	0: The GTIOCB pin outputs low when counting stops 1: The GTIOCB pin outputs high when counting stops.	R/W
b23	OBHLD	GTIOCB Pin Output Setting at the Start/Stop Count	0: The GTIOCB pin output level at the start/stop of counting depends on the register setting 1: The GTIOCB pin output level is retained at the start/stop of counting.	R/W
b24	OBE	GTIOCB Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b26, b25	OBDF[1:0]	GTIOCB Pin Disable Value Setting	b26 b25 0 0: Output disable is prohibited 0 1: GTIOCB pin is set to Hi-Z on output disable 1 0: GTIOCB pin is set to 0 on output disable 1 1: GTIOCB pin is set to 1 on output disable.	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	NFBEN	Noise Filter B Enable	0: The noise filter for the GTIOCB pin is disabled 1: The noise filter for the GTIOCB pin is enabled.	R/W

23.2.14 通用PWM定时器IO控制寄存器(GTIOR)

Address(es): GPT32m.GTIOR 4007 8034h + 0100h × m (m = 0 to 3),
GPT16m.GTIOR 4007 8034h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	GTIOA[4:0]	GTIOCA引脚功能选择	见表23.5。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	OADFLT	GTIOCA引脚输出值 在计数停止处设置	0：计数停止时GTIOCA引脚输出低电平1：计数停止时GTIOCA引脚输出高电平。	R/W
b7	OAHLD	开始停止计数时的GTIOCA引脚输出设置	0：计数开始或停止时GTIOCA引脚输出电平取决于寄存器设置 1：计数开始或停止时GTIOCA引脚输出电平保持不变。	R/W
b8	OAE	GTIOCA引脚输出使能	0：禁用输出1：启用输出。	R/W
b10, b9	OADF[1:0]	GTIOCA引脚禁用值 Setting	b10b900：禁止输出禁用01：GTIOCA引脚设置为Hi-Z，输出禁用10：GTIOCA引脚设置为0，输出禁用11：GTIOCA引脚设置为1，输出禁用。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	NFAEN	噪声滤波器A启用	0：GTIOCA引脚的噪声滤波器禁用1：GTIOCA引脚的噪声滤波器启用。	R/W
b15, b14	NFCSA[1:0]	噪声滤波器A采样时钟 Select	b15 b14 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W
b20 to b16	GTIOB[4:0]	GTIOCB引脚功能选择	见表23.5。	R/W
b21	—	Reserved	该位读取为0。写入值应为0。	R/W
b22	OBDFLT	GTIOCB引脚输出值 在计数停止处设置	0：计数停止时GTIOCB引脚输出低电平1：计数停止时GTIOCB引脚输出高电平。	R/W
b23	OBHLD	开始停止计数时的GTIOCB引脚输出设置	0：计数开始停止时GTIOCB引脚输出电平取决于寄存器设置1：计数开始停止时GTIOCB引脚输出电平保持不变。	R/W
b24	OBE	GTIOCB引脚输出使能	0：禁用输出1：启用输出。	R/W
b26, b25	OBDF[1:0]	GTIOCB引脚禁用值 Setting	b26b2500：禁止输出禁用01：GTIOCB引脚在输出禁用时设置为Hi-Z10：GTIOCB引脚在输出禁用时设置为011：GTIOCB引脚在输出禁用时设置为1。	R/W
b28, b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b29	NFBEN	噪声滤波器B启用	0：GTIOCB引脚的噪声滤波器禁用1：GTIOCB引脚的噪声滤波器启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b31, b30	NFCSB[1:0]	Noise Filter B Sampling Clock Select	b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

The GTIOR sets the functions of the GTIOCA and GTIOCB pins.

GTIOA[4:0] bits (GTIOCA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCA pin function. For details, see Table 23.5.

OADFLT bit (GTIOCA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCA pin outputs high or low when counting stops.

OAHLD bit (GTIOCA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCA pin output level is retained or the level at the start/stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCA Pin Output Enable)

The OAE bit disables or enables the GTIOCA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of GTIOCA pin when an output disable request occurs.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCA pin. Because changing the value of the bit might lead to internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCB pin function. For details, see Table 23.5.

OBDFLT bit (GTIOCB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCB pin outputs high or low when counting stops.

OBHLD bit (GTIOCB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether the GTIOCB pin output level is retained or the level at the start/stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

Bit	Symbol	位名称	Description	R/W
b31, b30	NFCSB[1:0]	噪声滤波器B采样时钟 Select	b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

GTIOR设置GTIOCA和GTIOCB引脚的功能。

GTIOA[4:0]位（GTIOCA引脚功能选择）

GTIOA[4:0]位选择GTIOCA引脚功能。详见表23.5。

OADFLT位（计数停止时GTIOCA引脚输出值设置）

OADFLT位设置当计数停止时GTIOCA引脚输出高电平还是低电平。

OAHLD位（开始停止计数时GTIOCA引脚输出设置）

OAHLD位指定是保留GTIOCA引脚输出电平还是计数开始停止时的电平取决于寄存器设置。

当OAHLD位设置为0时：

- 计数开始时输出GTIOA[4:0]位的位[4]中指定的值
- 计数停止时输出OADFLT位中指定的值
- 如果在计数停止时修改OADFLT位，则新值会立即反映在输出中。

当OAHLD位设置为1时：

- 当计数开始或停止时，输出保持不变。

OAE位（GTIOCA引脚输出使能）

OAE位禁用或启用GTIOCA引脚输出。

当GTCCRA寄存器用作输入捕捉寄存器时（GTICASR寄存器中至少有一位设置为1），
无论OAE位值如何，GTIOCA引脚都不输出。

OADF[1:0]位（GTIOCA引脚禁用值设置）

当输出禁用请求发生时，OADF[1:0]位选择GTIOCA引脚的输出值。

NFAEN位（噪声滤波器A使能）

NFAEN位禁用或启用来自GTIOCA引脚的输入的噪声滤波器。由于更改该位的值可能会导致内部产生意外边沿，因此在执行此操作之前，请在GTIOR寄存器中为相关引脚选择输出比较功能。

NFCSA[1:0]位（噪声滤波器A采样时钟选择）

NFCSA[1:0]位设置GTIOCA引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

GTIOB[4:0]位（GTIOCB引脚功能选择）

GTIOB[4:0]位选择GTIOCB引脚功能。详见表23.5。

OBDFLT位（计数停止时GTIOCB引脚输出值设置）

OBDFLT位设置当计数停止时GTIOCB引脚输出高电平还是低电平。

OBHLD位（开始停止计数时GTIOCB引脚输出设置）

OBHLD位指定是保留GTIOCB引脚输出电平还是计数开始停止时的电平取决于寄存器设置。

当OBHLD位设置为0时：

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCB Pin Output Enable)

The OBE bit disables or enables the GTIOCB pin output.

When GTCCRB register is used as the input capture register (at least one bit in GTICBSR register is set to 1), the GTIOCB pin does not output independently of the OBE bit value.

OBDF[1:0] bits (GTIOCB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of GTIOCB pin when an output disable request occurs.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

Table 23.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits (1 of 2)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1,*2,*3	b1, b0*2
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

- 计数开始时输出GTIOB[4:0]位的位[4]中指定的值
- 计数停止时输出OBDFLT位中指定的值
- 如果在计数停止时修改了OBDFLT位，则新值会立即反映在输出中。

当OBHLD位设置为1时：

- 当计数开始或停止时，输出保持不变。

OBE位（GTIOCB引脚输出使能）

OBE位禁用或启用GTIOCB引脚输出。

当GTCCRB寄存器用作输入捕捉寄存器时（GTICBSR寄存器中至少有一位设置为1），GTIOCB引脚不独立于OBE位值输出。

OBDF[1:0]位（GTIOCB引脚禁用值设置）

当输出禁用请求发生时，OBDF[1:0]位选择GTIOCB引脚的输出值。

NFBEN位（噪声滤波器B启用）

NFBEN位禁用或启用来自GTIOCB引脚的输入的噪声滤波器。因为更改位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSB[1:0]位（噪声滤波器B采样时钟选择）

NFCSB[1:0]位设置GTIOCB引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

Table 23.5 GTIOA[4:0]和GTIOB[4:0]位的设置(1of2)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1,*2,*3	b1, b0*2
0	0	0	0	0	初始输出低	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
0	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
0	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
0	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
0	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出

Table 23.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits (2 of 2)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1,*2,*3	b1, b0*2
1	0	0	0	0	Initial output is high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting) or underflow (GTCNT changes from 0 to GTPR in down-counting). The GTCNT counter is cleared for saw waves and for the trough (GTCNT changes from 0 to 1) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

23.2.15 General PWM Timer Interrupt Output Setting Register (GTINTAD)

Address(es): GPT32m.GTINTAD 4007 8038h + 0100h × m (m = 0 to 3),
GPT16m.GTINTAD 4007 8038h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disable Source Select	b25 b24 0 0: Group A output disable request 0 1: Group B output disable request 1 x: Setting prohibited.	R/W
b28 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 23.5 GTIOA[4:0]和GTIOB[4:0]位的设置(2of2)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1,*2,*3	b1, b0*2
1	0	0	0	0	初始输出高	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
1	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
1	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
1	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
1	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出

注1.循环结束意味着上溢（GTCNT在递增计数时从GTPR变为0）或下溢（GTCNT向下计数时从0变为GTPR）。锯齿波和波谷（GTCNT从0变为1）的三角波清除GTCNT计数器。注2.当一个循环结束的时间和一个GTCCRAGTCCRB比较匹配的时间在一个

比较匹配操作时，b3和b2设置在锯齿波PWM模式下优先，而b1和b0设置在任何其他模式下优先。注3.在GTUPSR或GTDNSR中至少一位设置为1的事件计数操作中，忽略b3和b2的设置。

23.2.15 通用PWM定时器中断输出设置寄存器(GTINTAD)

Address(es): GPT32m.GTINTAD 4007 8038h + 0100h × m (m = 0 to 3),
GPT16m.GTINTAD 4007 8038h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	GRP[1:0]	输出禁用源选择	b25b2400：A组输出禁止请求01：B组输出禁止请求1x：设置禁止。	R/W
b28 to b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b29	GRPABH	Same Time Output Level High Disable Request Enable	0: Same time output level high disable request disabled 1: Same time output level high disable request enabled.	R/W
b30	GRPABL	Same Time Output Level Low Disable Request Enable	0: Same time output level low disable request disabled 1: Same time output level low disable request enabled.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The GTINTAD enables or disables interrupt requests and output disable requests.

GRP[1:0] bits (Output Disable Source Select)

The GRP[1:0] bits select the GTIOCA or GTIOCB pin output disable sources.

The output disable request to POEG outputs to the group which is selected by GRP[1:0] bits when same time output level high or same time output level low occurs based on the output disable request enable bit.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. GRP[1:0] bits should be set when both GTIOR.OAE and GTIOR.OBE bits are 0.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCA and GTIOCB pins output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCA and GTIOCB pins output 0 at the same time.

23.2.16 General PWM Timer Status Register (GTST)

Address(es): GPT32m.GTST 4007 803Ch + 0100h × m (m = 0 to 3),
GPT16m.GTST 4007 803Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	TCFA	Input Capture/Compare Match Flag A	0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated.	R/(W)*1
b1	TCFB	Input Capture/Compare Match Flag B	0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated.	R/(W)*1
b2	TCFC	Input Compare Match Flag C	0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated.	R/(W)*1
b3	TCFD	Input Compare Match Flag D	0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated.	R/(W)*1
b4	TCFE	Input Compare Match Flag E	0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated.	R/(W)*1

Bit	Symbol	位名称	Description	R/W
b29	GRPABH	同时输出电平高禁用请求启用	0：禁止同时输出电平高禁止请求1：允许同时输出电平高禁止请求。	R/W
b30	GRPABL	同时输出电平低禁用请求启用	0：禁止同时输出电平低禁止请求1：允许同时输出电平低禁止请求。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

GTINTAD启用或禁用中断请求和输出禁用请求。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择GTIOCA或GTIOCB引脚输出禁用源。

当基于输出禁用请求使能位发生同时输出电平高或同时输出电平低时，对POEG的输出禁用请求输出到由GRP[1:0]位选择的组。

GTST.ODF显示了使用GRP[1:0]位选择的输出禁用源组的请求。当GTIOR.OAE和GTIOR.OBE位均为0时，应设置GRP[1:0]位。

GRPABH位（同时输出电平高禁用请求启用）

当GTIOCA和GTIOCB引脚同时输出1时，GRPABH位启用或禁用输出禁用请求。

GRPABL位（同时输出电平低禁用请求启用）

当GTIOCA和GTIOCB引脚同时输出0时，GRPABL位启用或禁用输出禁用请求。

23.2.16 通用PWM定时器状态寄存器(GTST)

Address(es): GPT32m.GTST 4007 803Ch + 0100h × m (m = 0 to 3),
GPT16m.GTST 4007 803Ch + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值：	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	TCFA	输入捕捉比较匹配 Flag A	0：不生成GTCCRA的输入捕捉比较匹配1：生成GTCCRA的输入捕捉比较匹配。	R/(W)*1
b1	TCFB	输入捕捉比较匹配 Flag B	0：不生成GTCCRB的输入捕捉比较匹配1：生成GTCCRB的输入捕捉比较匹配。	R/(W)*1
b2	TCFC	输入比较匹配标志C	0：没有生成GTCCRC的比较匹配1：生成了GTC CRC的比较匹配。	R/(W)*1
b3	TCFD	输入比较匹配标志D	0：不产生GTCCRD的比较匹配1：产生GTCCRD 的比较匹配。	R/(W)*1
b4	TCFE	输入比较匹配标志E	0：不产生GTCCRE的比较匹配1：产生GTCCRE 的比较匹配。	R/(W)*1

Bit	Symbol	Bit name	Description	R/W
b5	TCFF	Input Compare Match Flag F	0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated.	R/(W)*1
b6	TCFPO	Overflow Flag	0: No overflow (crest) occurred 1: An overflow (crest) occurred.	R/(W)*1
b7	TCFPU	Underflow Flag	0: No underflow (trough) occurred 1: An underflow (trough) occurred.	R/(W)*1
b14 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	TUCF	Count Direction Flag	0: GTCNT counter counts downward 1: GTCNT counter counts upward.	R
b23 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	ODF	Output Disable Flag	0: No output disable request is generated 1: An output disable request is generated.	R
b28 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	OABHF	Same Time Output Level High Flag	0: GTIOCA and GTIOCB pins do not output 1 at the same time 1: GTIOCA and GTIOCB pins output 1 at the same time.	R
b30	OABLF	Same Time Output Level Low Flag	0: GTIOCA and GTIOCB pins do not output 0 at the same time 1: GTIOCA and GTIOCB pins output 0 at the same time.	R
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit. Do not write 1.

The GTST indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

TCFA is the status flag for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

TCFB is the status flag for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

TCFC is the status flag for the compare match of GTCCRC.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

Bit	Symbol	位名称	Description	R/W
b5	TCFF	输入比较匹配标志F	0：不产生GTCCRF的比较匹配1：产生GTCCRF的比较匹配。	R/(W)*1
b6	TCFPO	溢出标志	0：未发生溢出（波峰）1：发生溢出（波峰）。	R/(W)*1
b7	TCFPU	Underflow Flag	0：未发生下溢（谷）1：发生下溢（谷）。	R/(W)*1
b14 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	TUCF	计数方向标志	0：GTCNT计数器向下计数1：GTCNT计数器向上计数。	R
b23 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	ODF	输出禁用标志	0：不产生输出禁止请求1：产生输出禁止请求。	R
b28 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b29	OABHF	同时输出电平高Flag	0：GTIOCA和GTIOCB引脚不同时输出11：GTIOCA和GTIOCB引脚同时输出1。	R
b30	OABLF	同时输出电平低Flag	0：GTIOCA和GTIOCB引脚不同时输出01：GTIOCA和GTIOCB引脚同时输出0。	R
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 该位只能写入0。不要写1。

GTST指示GPT的状态。

TCFA标志（输入捕捉比较匹配标志A）

TCFA是GTCCRA的输入捕获或比较匹配的状态标志。

[Setting conditions]

- 当GTCCRA寄存器用作比较匹配寄存器时GTCNT=GTCCRA
- 当GTCCRA寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRA。

[Clearing condition]

- 0写入该标志。

TCFB标志（输入捕捉比较匹配标志B）

TCFB是GTCCRB的输入捕获或比较匹配的状态标志。

[Setting conditions]

- GTCNT=GTCCRB，当GTCCRB寄存器用作比较匹配寄存器时
- 当GTCCRB寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRB。

[Clearing condition]

- 0写入该标志。

TCFC标志（输入比较匹配标志C）

TCFC是GTCCRC比较匹配的状态标志。

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

TCFD is the status flag for the compare match of GTCCRD.

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE is the status flag for the compare match of GTCCRE.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

TCFF is the status flag for the compare match of GTCCRF.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or a crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR-1) has occurred

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=01b 10b 11b（GTCCRC执行缓冲操作）。

TCFD标志（输入比较匹配标志D）

TCFD是GTCCRD比较匹配的状态标志。

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=10b 11b（GTCCRD执行缓冲操作）。

TCFE标志（输入比较匹配标志E）

TCFE是GTCCRE比较匹配的状态标志。

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=01b 10b 11b（GTCCRE执行缓冲操作）。

TCFF标志（输入比较匹配标志F）

TCFF是GTCCRF比较匹配的状态标志。

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=10b 11b（GTCCRF执行缓冲操作）。

TCFPO标志（溢出标志）

TCFPO标志指示何时发生溢出或波峰。

[Setting conditions]

- 在锯齿波模式下，发生了溢出（GTCNT在递增计数中从GTPR变为0）
- 在三角波模式下，出现波峰（GTCNT从GTPR变为GTPR-1）

- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or a trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a trough (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and is set to 0 in down-counting.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits.

When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCA and GTIOCB pins output 1 at the same time.

When GTIOCA or GTIOCB pin outputs 0, this flag is returned to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to the POEG as the output disable request.

[Setting condition]

- The GTIOCA and GTIOCB pins output 1 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCA pin output value is different from the GTIOCB pin output value when both OAE and OBE bits are set to 1
- The GTIOCA and GTIOCB pins output 0 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCA and GTIOCB pins output 0 at the same time.

When the GTIOCA pin or GTIOCB pin outputs 1, this flag is returned to 0. This flag is read only. Writing 0 to clear the flag is prohibited. When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to the POEG as the output disable request.

[Setting condition]

- The GTIOCA and GTIOCB pins output 0 at the same time when both the OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCA pin output value is different from the GTIOCB pin output value when both OAE and OBE bits are set to 1

- 在硬件源的计数中，发生了溢出（GTCNT在递增计数中从GTPR变为0）。

[Clearing condition]

- 0写入该标志。

TCFPU flag (Underflow Flag)

TCFPU标志指示何时发生下溢或波谷。

[Setting conditions]

- 在锯齿波模式下，发生下溢（向下计数时GTCNT从0变为GTPR）
- 在三角波模式下，出现了一个波谷（GTCNT从0变为1）
- 在硬件源的计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

[Clearing condition]

- 0写入该标志。

TUCF标志（计数方向标志）

TUCF标志表示GTCNT的计数方向。在事件计数操作中，该标志在向上计数时设置为1，在向下计数时设置为0。

ODF标志（输出禁用标志）

ODF标志显示在GRP[1:0]位中选择的输出禁用源组的请求。

当输出禁用时，输出禁用控制不会在输出禁用请求被否定的同一周期内释放。它在下一个周期中发布。

OABHF标志（同时输出电平高标志）

OABHF标志表示GTIOCA和GTIOCB管脚同时输出1。

当GTIOCA或GTIOCB引脚输出0时，该标志返回0。该标志为只读。禁止写入0清除标志。

当启用OABHF标志的中断时(GTINTAD.GRPABH=1)，OABHF标志作为输出禁用请求输出到POEG。

[Setting condition]

- 当OAE和OBE位都设置为1时，GTIOCA和GTIOCB引脚同时输出1。

[Clearing conditions]

- 当OAE和OBE位都设置为1时，GTIOCA引脚输出值与GTIOCB引脚输出值不同
- 当OAE和OBE位都设置为1时，GTIOCA和GTIOCB引脚同时输出0
- OAE位或OBE位设置为0。

OABLF标志（同时输出电平低标志）

OABLF标志表示GTIOCA和GTIOCB管脚同时输出0。

当GTIOCA引脚或GTIOCB引脚输出1时，该标志返回0。该标志为只读。禁止写入0清除标志。当启用OABLF标志的中断时(GTINTAD.GRPABL=1)，OABLF标志作为输出禁用请求输出到POEG。

[Setting condition]

- 当OAE和OBE位都设置为1时，GTIOCA和GTIOCB引脚同时输出0。

[Clearing conditions]

- 当OAE和OBE位都设置为1时，GTIOCA引脚输出值与GTIOCB引脚输出值不同

- The GTIOCA and GTIOCB pins output 1 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or the OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. When the output disable state is active, a compare match is performed continuously in the GPT and the OABHF/OABLF flag is updated in association with the result of the compared value.

23.2.17 General PWM Timer Buffer Enable Register (GTBER)

Address(es): GPT32m.GTBER 4007 8040h + 0100h × m (m = 0 to 3),
GPT16m.GTBER 4007 8040h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—		—	—	—		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD[1]	BD[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BD[0]	GTCCR Buffer Operation Disable	0: Buffer operation is enabled 1: Buffer operation is disabled.	R/W
b1	BD[1]	GTPR Buffer Operation Disable		R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, b16	CCRA[1:0]	GTCCRA Buffer Operation	b17 b16 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD).	R/W
b19, b18	CCRB[1:0]	GTCCRB Buffer Operation	b19 b18 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF).	R/W
b21, b20	PR[1:0]	GTPR Buffer Operation	b21 b20 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Setting prohibited.	R/W
b22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation	Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	R/W
b31 to b23	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTBER register provides settings for the buffer operation and must be set while the GTCNT operation stops.

BD[0] bit (GTCCR Buffer Operation Disable)

The BD[0] bit disables buffer operation using GTCCRA, GTCCRC, and GTCCRD combined and the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD[0] is set to 0, GTCCRB does not perform buffer operation and the GTCCRB register is automatically set to a compare match value for a negative-phase waveform with dead time.

BD[1] bit (GTPR Buffer Operation Disable)

The BD[1] bit disables buffer operation using GTPR and GTPBR combined.

- 当OAE和OBE位都设置为1时，GTIOCA和GTIOCB管脚同时输出1
- OAE位或OBE位设置为0。

生成OABHFOABLF标志的比较目标信号是比较匹配输出（PWM输出）信号，在它们被输出禁用功能屏蔽之前。当输出禁用状态激活时，在GPT中连续执行比较匹配，并根据比较值的结果更新OABHFOABLF标志。

23.2.17 通用PWM定时器缓冲器使能寄存器(GTBER)

Address(es): GPT32m.GTBER 4007 8040h + 0100h × m (m = 0 to 3),
GPT16m.GTBER 4007 8040h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—		—	—	—		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD[1]	BD[0]
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BD[0]	GTCCR缓冲区操作禁用	0：启用缓冲操作1：禁用缓冲操作。	R/W
b1	BD[1]	GTPR缓冲区操作禁用		R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, b16	CCRA[1:0]	GTCCRA缓冲区操作	b17b1600：无缓存操作01：单缓存操作（GTCCRA↔GTCCRC）1x：双缓存操作（GTCCRA↔GTCCRC↔GTCCRD）。	R/W
b19, b18	CCRB[1:0]	GTCCRB缓冲区操作	b19b1800：无缓冲操作01：单缓冲操作（GTCCRB↔GTCCRE）1x：双缓冲操作（GTCCRB↔GTCCRE↔GTCCRF）。	R/W
b21, b20	PR[1:0]	GTPR缓冲区操作	b21b2000：无缓冲操作01：单缓冲操作（GTPBR→GTPR）1x：禁止设置。	R/W
b22	CCRSWT	GTCCRA和GTCCRB强制缓冲操作	向该位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0。	R/W
b31 to b23	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTBER寄存器为缓冲区操作提供设置，并且必须在GTCNT操作停止时设置。

BD[0]位（GTCCR缓冲区操作禁用）

BD[0]位禁用使用GTCCRA、GTCCRC和GTCCRD组合的缓冲器操作以及使用GTCCRB、GTCCRE和GTCCRF组合的缓冲器操作。

当GTDTCR.TDE为1且BD[0]设置为0时，GTCCRB不执行缓冲操作，并且GTCCRB寄存器自动设置为具有死区时间的反相波形的比较匹配值。

BD[1]位（GTPR缓冲区操作禁用）

BD[1]位禁用使用GTPR和GTPBR组合的缓冲区操作。

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set buffer operation using GTCCRA, GTCCRC, and GTCCRD combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set buffer operation using GTPR and GTPBR combined.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0 and is valid only when counting is stopped with a specified compare match operation.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode, or triangle-wave PWM mode 3 (64-bit transfer at trough).

23.2.18 General PWM Timer Counter (GTCNT)

Address(es): GPT32m.GTCNT 4007 8048h + 0100h × m (m = 0 to 3),
GPT16m.GTCNT 4007 8048h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT is a 32-bit read/write counter for GPT32m (m = 0 to 3). For GPT16m (m = 4, 5, 8), GTCNT is a 16-bit register. GTCNT can only be written to after counting stops. GTCNT must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited.

For GPT16m (m = 4, 5, 8) the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.

CCRA[1:0]位（GTCCRA缓冲区操作）

CCRA[1:0]位使用GTCCRA、GTCCRC和GTCCRD组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。*1

CCRB[1:0]位（GTCCRB缓冲区操作）

CCRB[1:0]位使用GTCCRB、GTCCRE和GTCCRF组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。*1

PR[1:0]位（GTPR缓冲区操作）

PR[1:0]位使用GTPR和GTPBR组合设置缓冲区操作。

CCRSWT位（GTCCRA和GTCCRB强制缓冲操作）

向CCRSWT位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0，仅在使用指定的比较匹配操作停止计数时有效。

注1.缓冲器操作模式固定为锯齿波单次脉冲模式，或三角波PWM模式3（64位低谷传输）。

23.2.18 通用PWM定时器计数器(GTCNT)

Address(es): GPT32m.GTCNT 4007 8048h + 0100h × m (m = 0 to 3),
GPT16m.GTCNT 4007 8048h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT是GPT32m（m=0到3）的32位读写计数器。对于GPT16m(m=4 5 8)，GTCNT是一个16位寄存器。GTCNT只能在计数停止后写入。GTCNT必须以32位单元访问。禁止以8位16位为单位进行访问。

对于GPT16m(m=4 5 8)，用于访问32位单元的高16位始终被读取为0000h，并且忽略写入这些位。

GTCNT必须设置在0≤GTCNT≤GTPR的范围内。

23.2.19 General PWM Timer Compare Capture Register n (GTCCRn) (n = A to F)

Address(es): GPT32m.GTCCRA 4007 804Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCCRA 4007 804Ch + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRB 4007 8050h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRB 4007 8050h + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRC 4007 8054h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRC 4007 8054h + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRD 4007 805Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCCRD 4007 805Ch + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRE 4007 8058h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRE 4007 8058h + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRF 4007 8060h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRF 4007 8060h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16m (m = 4, 5, 8), the value of the upper 16 bits after reset is 0000h.

GTCCRn registers are read/write registers. The effective size of GTCCRn is the same as GTCNT (16- or 32-bit). If the effective size of GTCCRn is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

GTCCRA and GTCCRB are registers used for both output compare and input capture. GTCCRC and GTCCRE are comparison match registers that can also function as buffer registers for GTCCRA and GTCCRB.

GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).

23.2.20 General PWM Timer Cycle Setting Register (GTPR)

Address(es): GPT32m.GTPR 4007 8064h + 0100h × m (m = 0 to 3),
GPT16m.GTPR 4007 8064h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16m (m = 4, 5, 8), value of the upper 16 bits after reset is 0000h.

GTPR is a read/write register that sets the maximum count value of GTCNT. The effective size of GTPR is the same as GTCNT (16- or 32-bit). If the effective size of GTPR is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.

23.2.19 通用PWM定时器比较捕捉寄存器n(GTCCRn)(n=AtoF)

Address(es): GPT32m.GTCCRA 4007 804Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCCRA 4007 804Ch + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRB 4007 8050h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRB 4007 8050h + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRC 4007 8054h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRC 4007 8054h + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRD 4007 805Ch + 0100h × m (m = 0 to 3),
GPT16m.GTCCRD 4007 805Ch + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRE 4007 8058h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRE 4007 8058h + 0100h × m (m = 4, 5, 8),
GPT32m.GTCCRF 4007 8060h + 0100h × m (m = 0 to 3),
GPT16m.GTCCRF 4007 8060h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. 对于GPT16m(m=4 5 8)，复位后高16位的值为0000h。

GTCCRn寄存器是读写寄存器。GTCCRn的有效大小与GTCNT（16位或32位）相同。如果GTCCRn的有效大小为16位，则在32位单元中访问的高16位始终被读取为0000h，并且忽略写入这些位。

GTCCRA和GTCCRB是用于输出比较和输入捕捉的寄存器。GTCCRC和GTCCRE是比较匹配寄存器，也可以用作GTCCRA和GTCCRB的缓冲寄存器。

GTCCRD和GTCCRF是比较匹配寄存器，也可以用作GTCCRC的缓冲寄存器和GTCCRE（GTCCRA和GTCCRB的双缓冲寄存器）。

23.2.20 通用PWM定时器周期设置寄存器(GTPR)

Address(es): GPT32m.GTPR 4007 8064h + 0100h × m (m = 0 to 3),
GPT16m.GTPR 4007 8064h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. 对于GPT16m(m=4 5 8)，复位后高16位的值为0000h。

GTPR是一个读写寄存器，设置GTCNT的最大计数值。GTPR的有效大小与GTCNT（16位或32位）。如果GTPR的有效大小为16位，则在32位单元中访问的高16位始终被读取为0000h，并且忽略写入这些位。

对于锯齿波，(GTPR+1)的值就是周期。对于三角波，（GTPR值 2）的值是周期。

23.2.21 General PWM Timer Cycle Setting Buffer Register (GTPBR)

Address(es): GPT32m.GTPBR 4007 8068h + 0100h × m (m = 0 to 3),
GPT16m.GTPBR 4007 8068h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16m (m = 4, 5, 8), the value of the upper 16 bits after reset is 0000h.

GTPBR is a read/write register that functions as a buffer register for GTPR. The effective size of GTPBR is the same as GTCNT (16- or 32-bit). If the effective size of GTPBR is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

23.2.22 General PWM Timer Dead Time Control Register (GTDTCR)

Address(es): GPT32m.GTDTCR 4007 8088h + 0100h × m (m = 0 to 3),
GPT16m.GTDTCR 4007 8088h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: GTCCRB is set without using GTDVU 1: GTDVU sets the compare match value for negative-phase waveform with automatic dead time in GTCCRB.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. GPT has a dead time control function and the GTDVU register is used for setting dead time value.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU. When GTDVU is used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU), is automatically set in GTCCRB. The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB.

- Triangle waves:
  Upper limit value: GTPR – 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR

23.2.21 通用PWM定时器周期设置缓冲寄存器(GTPBR)

Address(es): GPT32m.GTPBR 4007 8068h + 0100h × m (m = 0 to 3),
GPT16m.GTPBR 4007 8068h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. 对于GPT16m(m=4 5 8)，复位后高16位的值为0000h。

GTPBR是一个读写寄存器，用作GTPR的缓冲寄存器。GTPBR的有效大小与GTCNT（16位或32位）相同。如果GTPBR的有效大小为16位，则在32位单元中访问的高16位始终被读取为0000h，并且忽略写入这些位。

23.2.22 通用PWM定时器死区控制寄存器(GTDTCR)

Address(es): GPT32m.GTDTCR 4007 8088h + 0100h × m (m = 0 to 3),
GPT16m.GTDTCR 4007 8088h + 0100h × m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TDE	负相位波形设置	0：不使用GTDVU设置GTCCRB1：GTDVU在GTCCRB中设置带自动死区时间的反相波形的比较匹配值。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDTCR可以自动设置带死区时间的负相位波形的比较匹配值。GPT具有死区时间控制功能，GTDVU寄存器用于设置死区时间值。

TDE位（负相位波形设置）

TDE位指定是否使用GTDVU。使用GTDVU时，通过正相波形的比较匹配值(GTCCRA)和死区时间值(GTDVU)获得的带死区时间的负相波形的比较匹配值自动设置在GTCCRB中。TDE位设置在锯齿波PWM模式下被忽略，并且不会进行自动设置。

GTCCRB值是自动设置的，具有以下上下限值。如果获得的GTCCRB值不在上限或下限内，则在GTCCRB中设置以下限值。

- Triangle waves:
  上限值：GTPR　1
  下限值：加1，减0
- Saw-wave one-shot pulse mode:
  上限值：GTPR

Lower limit value: 0.

23.2.23 General PWM Timer Dead Time Value Register U (GTDVU)

Address(es): GPT32m.GTDVU 4007 808Ch + 0100h x m (m = 0 to 3),
GPT16m.GTDVU 4007 808Ch + 0100h x m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. For GPT16m (m = 4, 5, 8), the value of the upper 16 bits after reset is 0000h.

GTDVU is a read/write register that sets the dead time for generating PWM waveforms with dead time. The effective size of GTDVU is the same as GTCNT (16- or 32-bit). If the effective size of GTDVU is 16-bit, the upper 16 bits for access in a 32-bit unit are always read as 0000h, and writing to these bits is ignored.

Setting a dead time value that exceeds the cycle value is prohibited. The set value can be confirmed by reading from GTCCRB. When GTDVU is used, writing to GTCCRB is prohibited. When this register is set to 0, waveforms without dead time are output.

While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, stop the GPT with the CST bit in the GTCR register. GTDVU must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited.

23.2.24 Output Phase Switching Control Register (OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	—	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	UF	Input Phase Soft Setting	These bits set the input phase from software settings. Setting these bits is valid when the OPSCR.FB bit = 1.	R/W
b1	VF			R/W
b2	WF			R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	U	Input U-Phase Monitor	These bits monitor the state of the input phase: OPSCR.FB = 0: External input that are synchronized by PCLKD are monitored by these bits OPSCR.FB = 1: Software settings (UF/VF/WF).	R
b5	V	Input V-Phase Monitor		R
b6	W	Input W-Phase Monitor		R
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	EN	Enable-Phase Output Control	0: Do not output (Hi-Z external pin). 1: Output.*1	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

下限值：0。

23.2.23 通用PWM定时器死区值寄存器U(GTDVU)

Address(es): GPT32m.GTDVU 4007 808Ch + 0100h x m (m = 0 to 3),
GPT16m.GTDVU 4007 808Ch + 0100h x m (m = 4, 5, 8)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1	1*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. 对于GPT16m(m=4 5 8)，复位后高16位的值为0000h。

GTDVU是一个读写寄存器，用于设置死区时间，以生成带死区时间的PWM波形。GTDVU的有效大小与GTCNT相同（16位或32位）。如果GTDVU的有效大小为16位，则在32位单元中访问的高16位始终被读取为0000h，并且忽略写入这些位。

禁止设置超过周期值的死区时间值。设定值可以通过读取来确认GTCCRB。使用GTDVU时，禁止写入GTCCRB。当该寄存器设置为0时，输出无死区时间的波形。

在GPT运行时，禁止更改GTDVU值。要将GTDVU更改为新值，请使用GTCR寄存器中的CST位停止GPT。GTDVU必须以32位单元访问。禁止以8位16位为单位进行访问。

23.2.24 输出相位切换控制寄存器(OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	—	INV	N	P	FB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	UF	输入相位软设置	这些位通过软件设置设置输入相位。当OPSCR.FB位=1时，设置这些位有效。	R/W
b1	VF			R/W
b2	WF			R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	U	输入U相监视器	这些位监控输入相位的状态：OPSCR.FB=0:同步的外部输入PCLKD由这些位监控 OPSCR.FB=1：软件设置（UFVFWF）。	R
b5	V	输入V相监视器		R
b6	W	输入W相监视器		R
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	EN	使能相输出控制	0：不输出（Hi-Z外部引脚）。1：输出。*1	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b16	FB	External Feedback Signal Enable	This bit selects the input phase from software settings and external input: 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF).	R/W
b17	P	Positive-Phase Output (P) Control	0: Level signal output 1: PWM signal output (PWM of GPT320).	R/W
b18	N	Negative-Phase Output (N) Control	0: Level signal output 1: PWM signal output (PWM of GPT320).	R/W
b19	INV	Invert-Phase Output Control	0: Positive logic (active-high) output 1: Negative logic (active-low) output.	R/W
b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b21	ALIGN	Input Phase Alignment	0: Input phase aligned to PCLKD 1: Input phase aligned to PWM.	R/W
b23, b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disabled Source Selection	b25 b24 0 0: Select Group A output disable source 0 1: Select Group B output disable source 1 x: Setting Prohibited.	R/W
b26	GODF	Group Output Disable Function	0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit.*1	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	NFEN	External Input Noise Filter Enable	0: Do not use a noise filter on the external input 1: Use a noise filter on the external input.	R/W
b31, b30	NFCS[1:0]	External Input Noise Filter Clock Selection	Noise filter sampling clock setting of the external input: b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF, VF, WF bits (Input Phase Soft Setting)

The UF, VF, WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF/VF/WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by PCLKD are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF, OPSCR.VF, and OPSCR.WF bits.

EN bit (Enable-Phase Output Control)

The EN bit controls the output enable signal output phase (positive phase/reverse phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF/VF/WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.ALIGN, OPSCR.RV, OPSCR.GRP[1:0], OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS[1:0]. Then, set the EN bit to 1. Also when OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output (PWM of GPT320) or PWM signal output for the positive-phase output

Bit	Symbol	位名称	Description	R/W
b16	FB	外部反馈信号使能	该位从软件设置和外部输入中选择输入相位：0：选择外部输入1：选择软设置（OPSCR.UF、VF、WF）。	R/W
b17	P	正相输出(P)控制	0：电平信号输出1：PWM信号输出（GPT320的PWM）。	R/W
b18	N	负相输出(N)控制	0：电平信号输出1：PWM信号输出（GPT320的PWM）。	R/W
b19	INV	反相输出控制	0：正逻辑（高电平有效）输出1：负逻辑（低电平有效）输出。	R/W
b20	—	Reserved	该位读取为0。写入值应为0。	R/W
b21	ALIGN	输入相位对齐	0：输入相位与PCLKD对齐1：输入相位与PWM对齐。	R/W
b23, b22	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	GRP[1:0]	输出禁用源选择	b25b2400：选择A组输出禁用源01：选择B组输出禁用源1x：设置禁止。	R/W
b26	GODF	组输出禁用功能	0：忽略该位功能1：组禁用清除OPSCR.EN位。*1	R/W
b28, b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b29	NFEN	外部输入噪声滤波器启用	0：外部输入不使用噪声滤波器1：外部输入使用噪声滤波器。	R/W
b31, b30	NFCS[1:0]	外部输入噪声滤波器时钟Selection	外部输入的噪声滤波器采样时钟设置：b31b3000：PCLKD101：PCLKD410：PCLKD1611：PCLKD64。	R/W

Note 1. 当OPSCR.GODF=1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

OPSCR寄存器设置无刷直流电机控制所需的信号波形输出。

UF VF WF位（输入相位软设置）

UF、VF、WF位通过软件设置设置输入相位。当OPSCR.FB位为1时，这些位有效。UFVFWF的设定值代替了UVW外部输入。

U V W位（输入相位监视器）

当OPSCR.FB位为0时，由PCLKD同步的外部输入由这些位监控。当。。。的时候OPSCR.FB位为1，OPSCR.U、OPSCR.V和OPSCR.W位可以读取OPSCR.UF、OPSCR.VF和OPSCR.WF bits.

EN位（使能相位输出控制）

EN位控制输出使能信号的输出相位（正相反相）。

当OPSCR.EN位为1时，输出信号波形。

当OPSCR.EN位为0时，先设置OPSCR.FB、OPSCR.UFVFWF（选择软件设置）、OPSCR.PN、OPSCR.INV、OPSCR.ALIGN、OPSCR.RV、OPSCR.GRP[1:0]、OPSCR.GODF、OPSCR.NFEN、OPSCR.NFCS[1:0]。然后，将EN位设置为1。同样，当OPSCR.GODF为1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

FB位（外部反馈信号使能）

FB位从软件设置（OPSCR.UF、VF、WF）和霍尔元件等外部输入中选择输入相位。

P位（正相输出（P）控制）

P位选择电平信号输出（GPT320的PWM）或PWM信号输出之一为正相输出

(GTOUUP pin, GTOVUP pin, GTOWUP pin).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output (PWM of GPT320) or PWM signal output for the negative-phase output (GTOULO pin, GTOVLO pin, GTOWLO pin).

INV bit (Invert-Phase Output Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the PCLKD or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit).

When OPSCR.ALIGN bit is 0, input phase is aligned to PCLKD.

Note: When PWM output is selected (OPSCR.P/N is 1) and the PCLKD input phase is aligned, the PWM pulse can be short-pulsed.

Note: When OPSCR.ALIGN bit is 1, input phase is aligned with PWM output.

GRP[1:0] bits (Output Disabled Source Selection)

The GRP[1:0] bits select the output disable source (A, B).

GODF bit (Group Output Disable Function)

When the OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0. When the OPSCR.GODF bit is 0, this bit is ignored.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter for the external input is not used.

Note: When this bit is switched because of an unintentional internal edge, set the OPSCR.EN bit to 0.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

23.3 Operation

23.3.1 Basic Operation

Each channel has a 32-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR controls the count cycle. When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated pin GTIOCA or GTIOCB can be changed. GTCCRA or GTCCRB can be used as an input capture register with hardware resources. GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

23.3.1.1 Counter operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1. The GTCR.CST bit value is changed by the following sources:

(GTOUUP pin, GTOVUP pin, GTOWUP pin).

N位（负相输出（N）控制）

N位选择电平信号输出（GPT320的PWM）或负相输出（GTOULO引脚、GTOVLO引脚、GTOWLO引脚）的PWM信号输出之一。

INV位（反相输出控制）

INV位选择输出相位的正逻辑（高电平有效）输出或负逻辑（低电平有效）输出之一。

ALIGN位（输入相位对齐）

ALIGN位选择PCLKD或PWM用于输入相位的采样（输入相位在
OPSCR.FB bit).

当OPSCR.ALIGN位为0时，输入相位与PCLKD对齐。

Note: WhenPWMoutputisselected(OPSCR.PNis1)andthePCLKDinputphaseisaligned thePWMpulsecanbeshort-pulsed.

Note: 当OPSCR.ALIGN位为1时，输入相位与PWM输出对齐。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择输出禁用源（A，B）。

GODF位（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。当OPSCR.GODF位为0时，该位被忽略。

NFEN位（外部输入噪声滤波器使能）

NFEN位选择外部输入的噪声滤波器。当OPSCR.NFEN位为0时，不使用外部输入的噪声滤波器。

Note: 由于无意的内部边沿而切换该位时，将OPSCR.EN位设置为0。

NFCS[1:0]位（外部输入噪声滤波器时钟选择）

NFCS[1:0]位选择外部输入噪声滤波器的时钟。当OPSCR.NFEN位为1时，使能外部输入的噪声滤波器采样时钟设置。

1. 设置NFCS[1:0]。
2. 等待2个周期。
3. 将OPSCR.EN位设置为1。

23.3 Operation

23.3.1 基本操作

每个通道都有一个32位定时器，它使用计数时钟和硬件源执行周期性计数操作。
计数功能提供向上计数和向下计数。GTPR控制计数周期。当。。。的时候
GTCNT计数器值与GTCCRA或GTCCRB中的值匹配，相关引脚GTIOCA或GTIOCB的输出可以更改。GTCCRA或GTCCRB可用作具有硬件资源的输入捕捉寄存器。
GTCCRC和GTCCRD可以作为GTCCRA的缓冲寄存器。GTCCRE和GTCCRF可以作为GTCCRB的缓冲寄存器。

23.3.1.1 计数器操作

(1) 计数器启动和停止

当GTCR.CST设置为1时，每个通道的计数器开始计数操作。GTCR.CST位值由以下来源更改：

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit is set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit is set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 0000 0000h. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set to 1. After GTCNT overflows, up-counting resumes from 0000 0000h.

Figure 23.3 shows an example of a periodic count operation in up-counting.

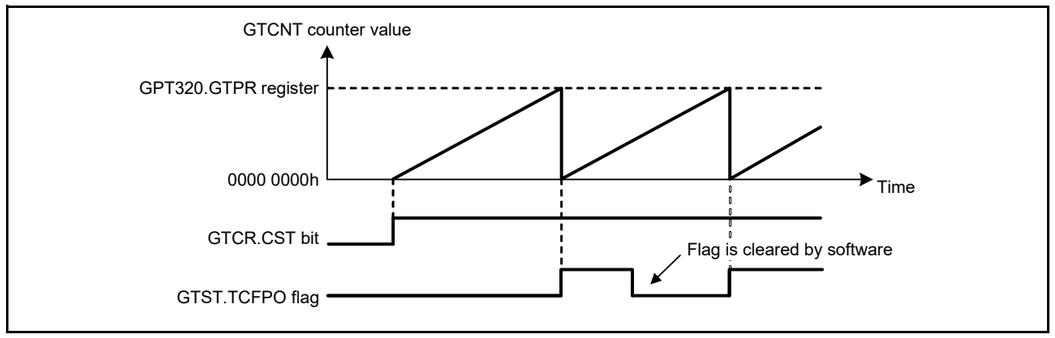


Figure 23.3 Example of periodic count operation in up-counting by the count clock

Figure 23.4 shows an example for setting periodic count operation in up-counting.

- 写入GTCR寄存器
- 当GTSSR.CSTRT位设置为1时，将1写入GTSTR中与GPT通道号相关的位
- 当GTPSR.CSTOP位设置为1时，将1写入GTSTP中与GPT通道号相关联的位
- GTSSR寄存器中选择的硬件源
- 在GTPSR寄存器中选择的硬件源。

(2) 计数时钟递增计数中的周期计数操作

当相关的GTCR.CST位设置为1且GTUPSR和GTDNSR寄存器设置为00000000h时，每个通道中的GTCNT计数器开始向上计数。当GTCNT值从GTPR值变为0（溢出）时，GTST.TCFPO标志设置为1。GTCNT溢出后，向上计数从00000000h恢复。

图23.3显示了递增计数中周期性计数操作的示例。

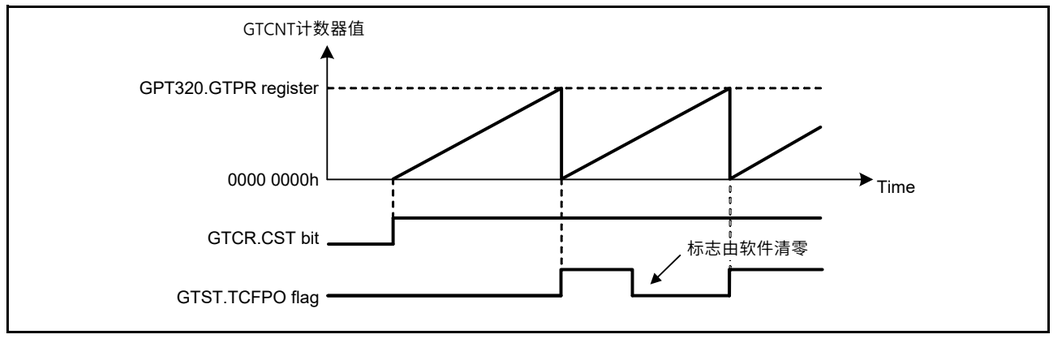


Figure 23.3 计数时钟递增计数中的周期计数操作示例

图23.4显示了在递增计数中设置周期性计数操作的示例。

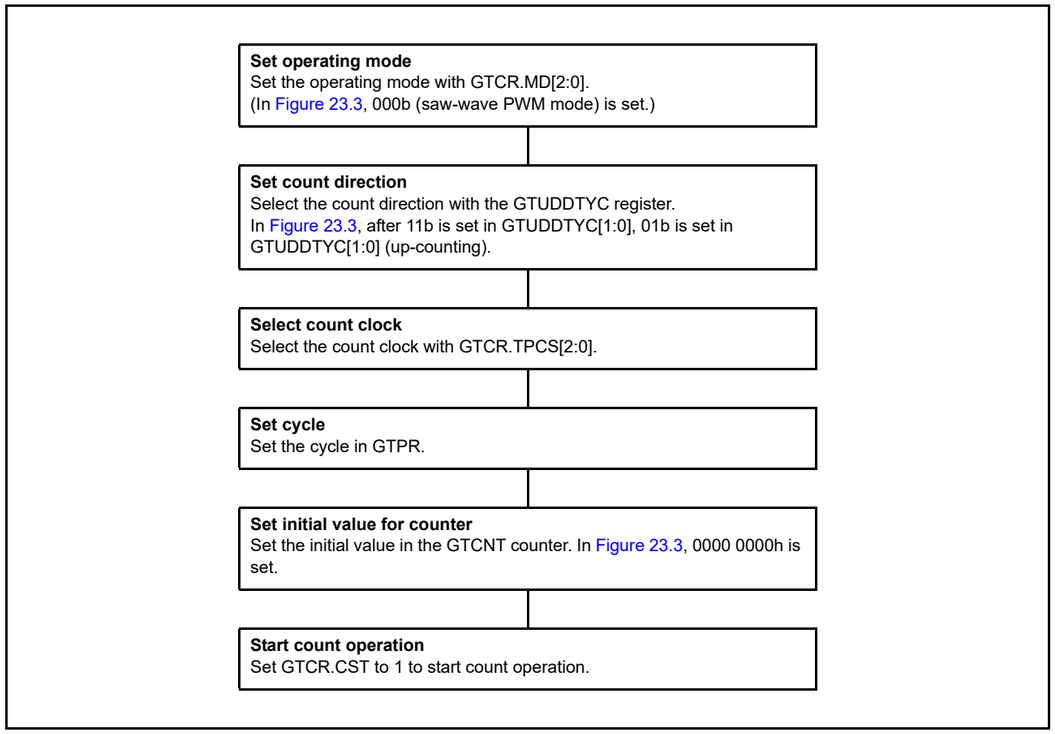


Figure 23.4 Example for setting a periodic count operation in up-counting by the count clock

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 0000 0000h. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1. When the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 23.5 shows an example of periodic count operation in down-counting by the count clock.

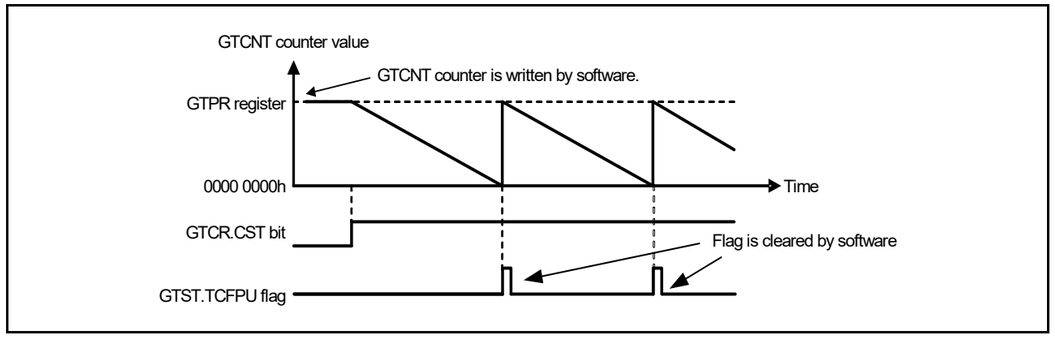


Figure 23.5 Example of periodic count operation in down-counting by the count clock

Figure 23.6 shows an example for setting periodic count operation in down-counting by the count clock.

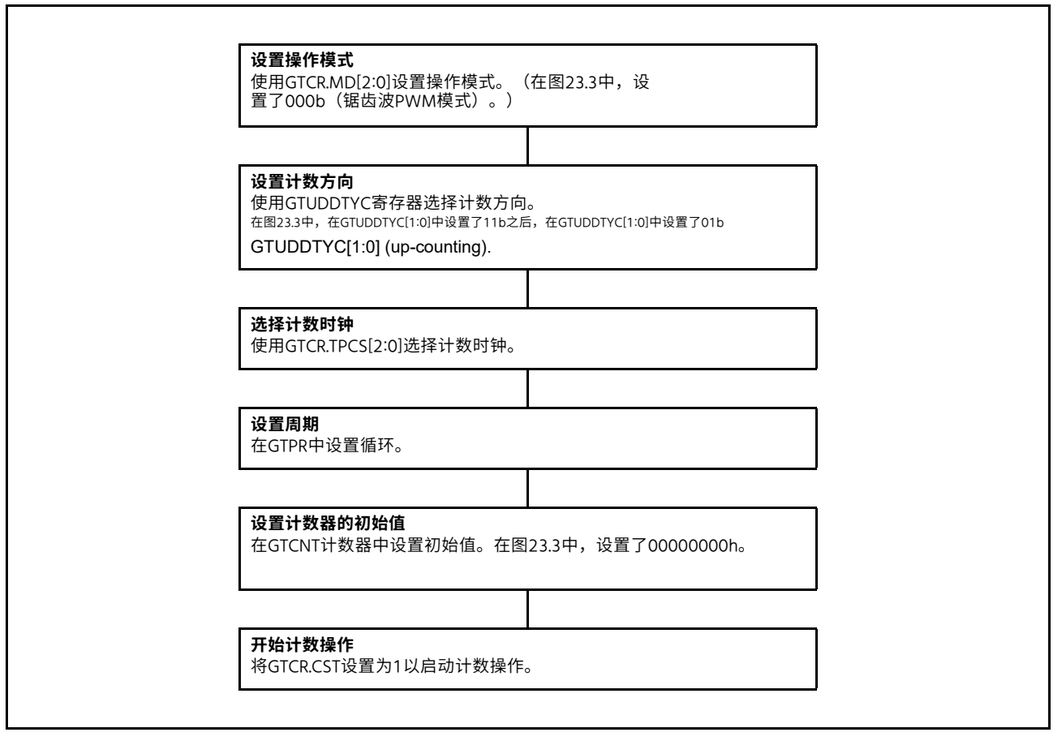


Figure 23.4 使用计数时钟在递增计数中设置周期性计数操作的示例

(3) 计数时钟递减计数中的周期计数操作

每个通道中的GTCNT计数器可以通过使用GTUPSR设置GTUDDTYC.UD和GTDNSR寄存器设置为00000000h。当GTCNT从0变为GTPR值（下溢）时，GTST.TCFPU设置为1。当GTCNT计数器下溢时，从GTPR值开始向下计数。

图23.5显示了计数时钟递减计数中周期性计数操作的示例。

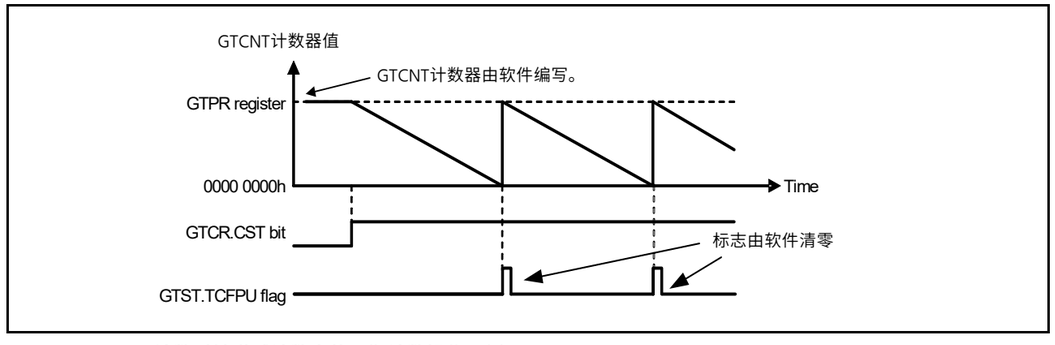


Figure 23.5 计数时钟递减计数中的周期计数操作示例

图23.6显示了在计数时钟递减计数中设置周期性计数操作的示例。

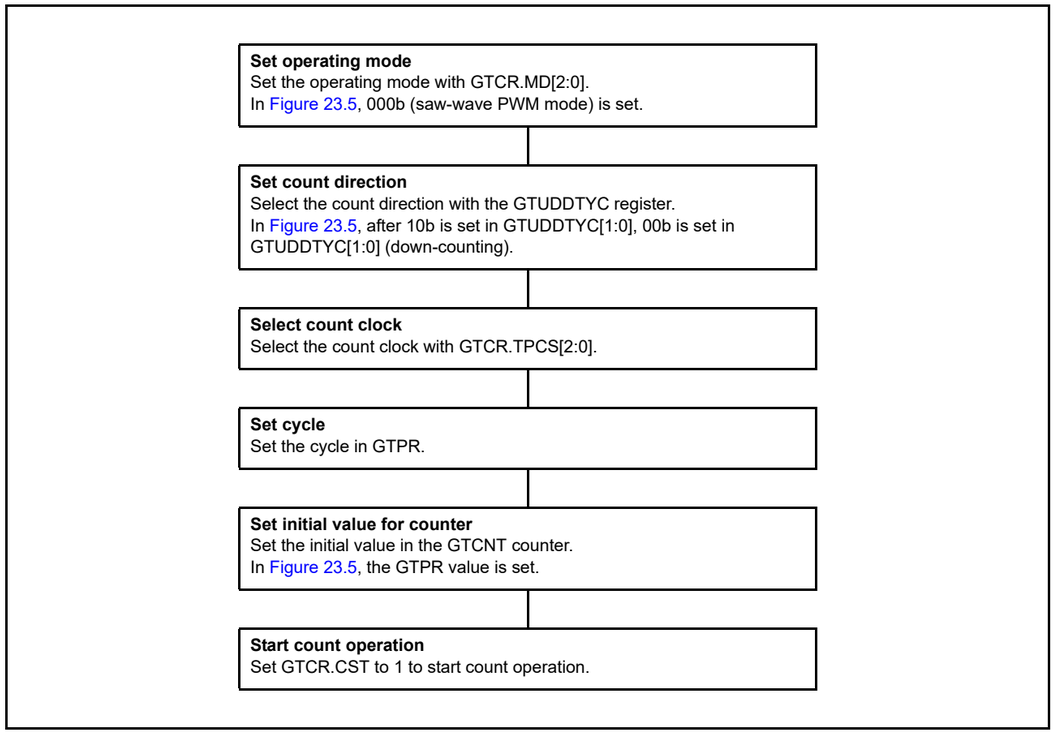


Figure 23.6 Example for setting periodic count operation in down-counting by count clock

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior for up-counting using hardware sources is the same as for up-counting by the count clock.

When GTCR.CST bit is set to 1 to count up using hardware sources, the count operation is enabled. When GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is synchronized by the count clock selected by GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count up with 1 PCLKD delay after GTCR.CST is set to 1.

Figure 23.7 shows an example of a periodic count operation in up-counting by a hardware resource (rising edge of GTETRGA pin).

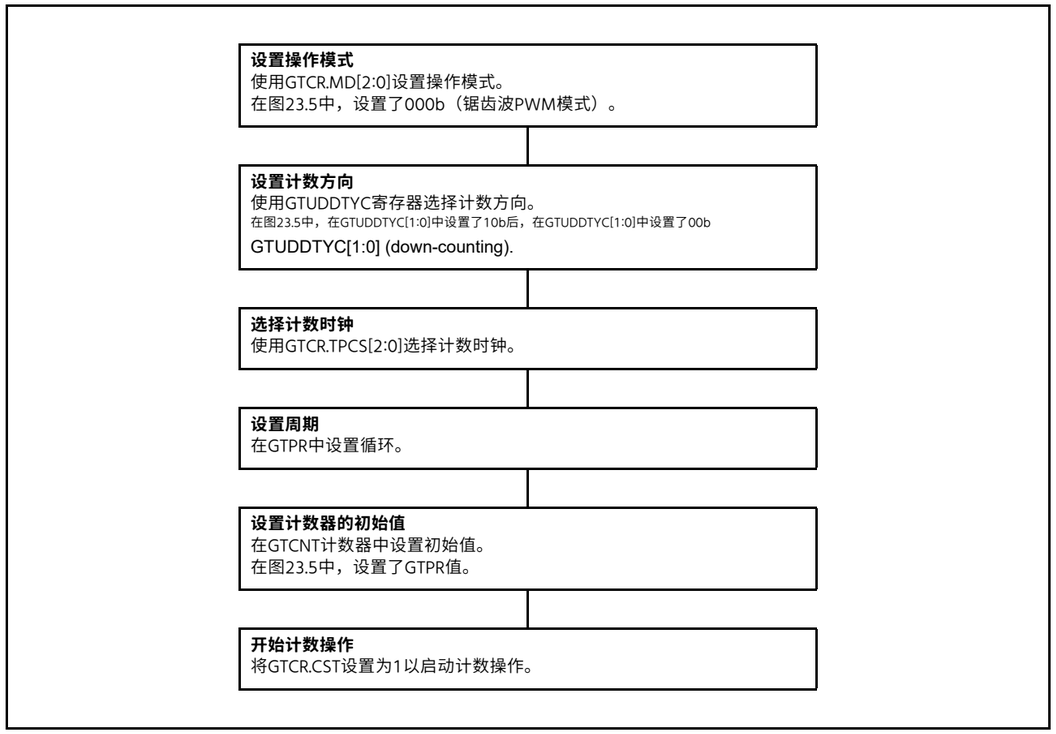


Figure 23.6 计数时钟递减计数中设置周期计数操作的示例

(4) 使用硬件源的递增计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTUPSR中设置的硬件源执行递增计数。

当GTUPSR设置为使能时，在GTCR.TPCS[2:0]中选择的计数时钟和在GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则GTCNT计数器值不会改变。使用硬件源进行向上计数的溢出行为与使用计数时钟进行向上计数的溢出行为相同。

当GTCR.CST位设置为1以使用硬件源进行计数时，计数操作被启用。当GTCR.CST设置为1时，计数器无法按GTCR.TPCS[2:0]中的规定向上计数1个时钟周期，因为计数操作与GTCR.TPCS[2:0]选择的计数时钟同步。将GTCR.TPCS[2:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟递增计数。

图23.7显示了硬件资源递增计数中的周期性计数操作的示例（上升沿GTETRGA pin).

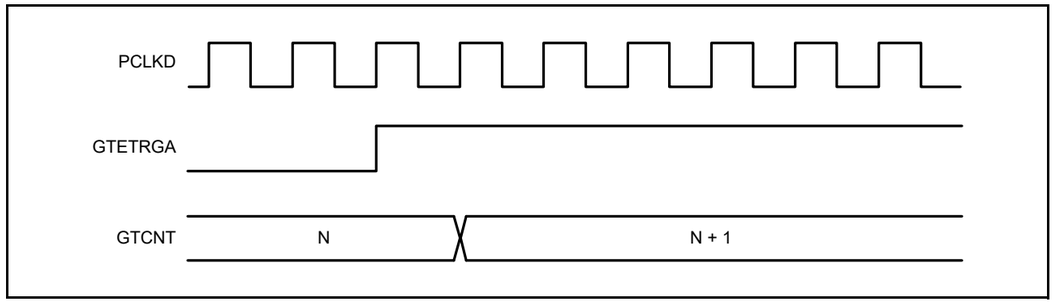


Figure 23.7 Example of periodic count operation in up-counting using hardware sources

Figure 23.8 shows an example for setting periodic count operation in down-counting by the count clock.

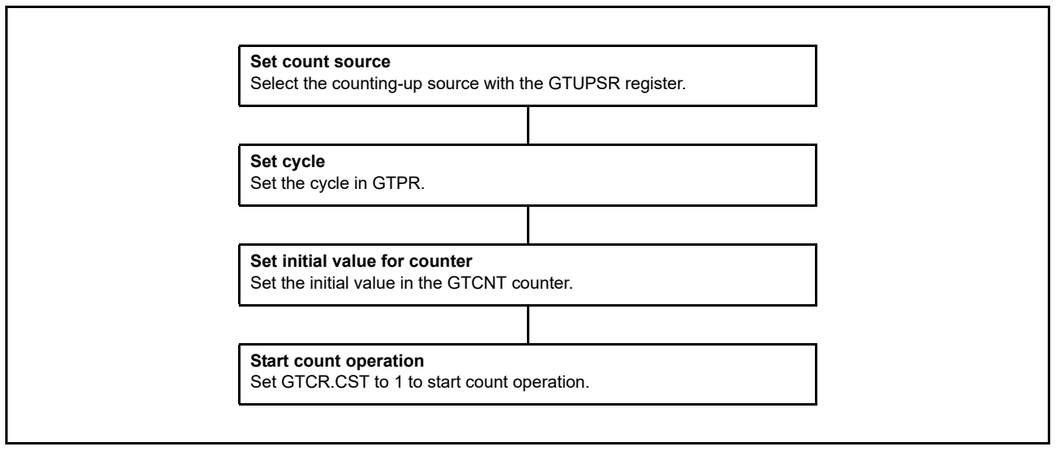


Figure 23.8 Example for setting an event count operation in up-counting using hardware sources

(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, GTCNT counter value does not change. The underflow behavior for down-counting using hardware sources is the same as for down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. When GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified by GTCR.TPCS[2:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count down with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 23.9 shows an example of a periodic count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).

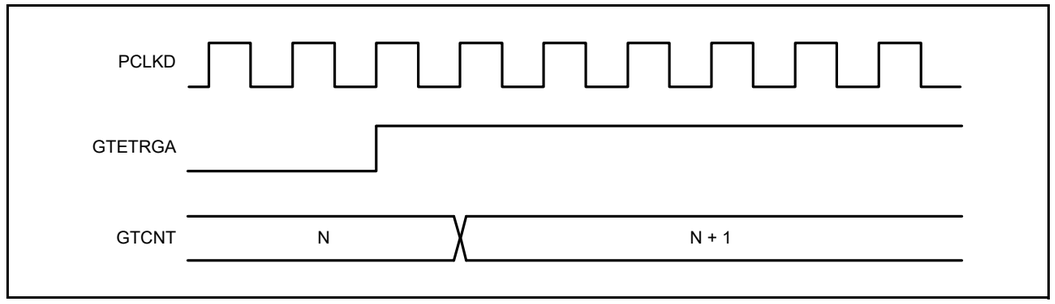


Figure 23.7 使用硬件源进行递增计数的周期性计数操作示例

图23.8显示了在计数时钟递减计数中设置周期性计数操作的示例。

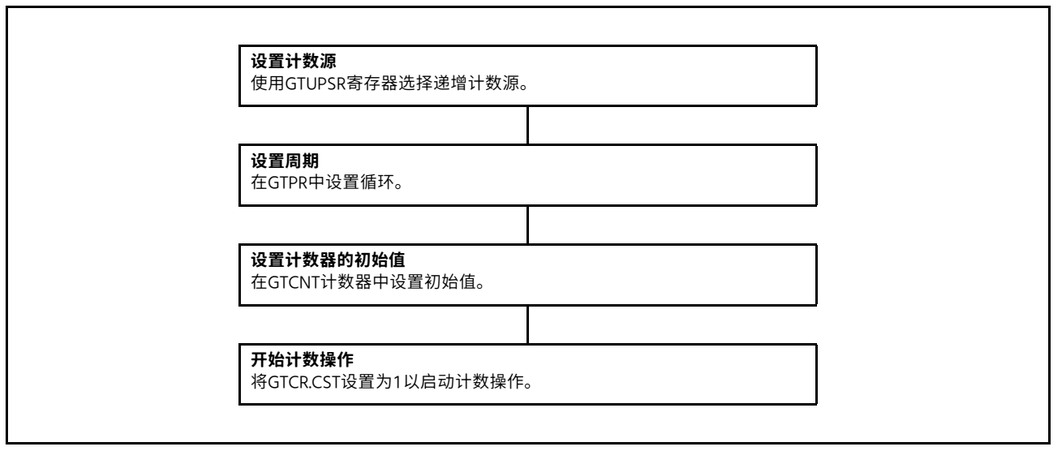


Figure 23.8 使用硬件源在递增计数中设置事件计数操作的示例

(5) 使用硬件源的递减计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTDNSR中设置的硬件源进行递减计数。

当GTDNSR设置为使能时，在GTCR.TPCS[2:0]中选择的计数时钟和在GTUDDTYC.UD中选择的计数方向被忽略。如果同时发生使用硬件源的递增计数和递减计数，
GTCNT计数器值不会改变。使用硬件源向下计数的下溢行为与使用计数时钟向下计数的相同。

当GTCR.CST位设置为1以使用硬件源进行递减计数时，启用计数操作。什么时候
GTCR.CST设置为1，计数器不能按GTCR.TPCS[2:0]指定的1个时钟周期递减计数，因为计数操作与GTCR.TPCS[2:0]中选择的计数时钟同步。将GTCR.TPCS[2:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟递减计数。

图23.9显示了通过硬件资源进行递减计数的周期性计数操作示例（上升沿
GTETRGA pin).

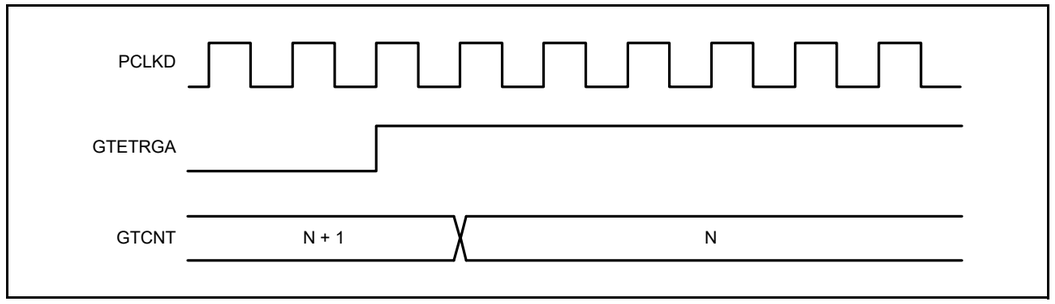


Figure 23.9 Example of event count operation in down-counting using hardware sources

Figure 23.10 shows an example for setting a periodic count operation in down-counting using a hardware resource.

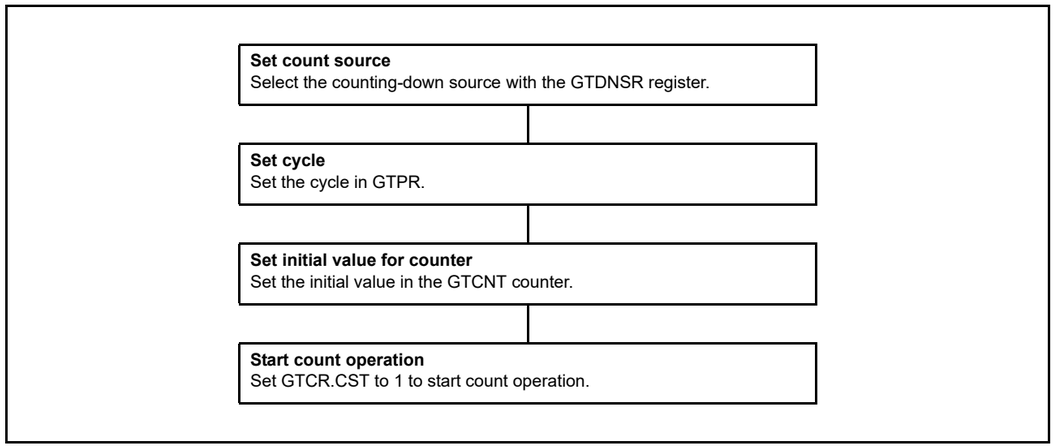


Figure 23.10 Example for setting an event count operation in down-counting using hardware sources

(6) Counter clear operation

The counter of each channel is cleared by the following sources.

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit is set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST = 1) or not (GTCR.CST = 0).

For saw waves selected by setting GTCR.MD[2:0] and the count direction flag showing down-counting (GTST.TUCF is 0), the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register or when clearing by hardware sources are performed. When not in saw-wave mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to the GTCLR register and clearing by hardware sources are performed immediately to synchronize with PCLKD. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[2:0].

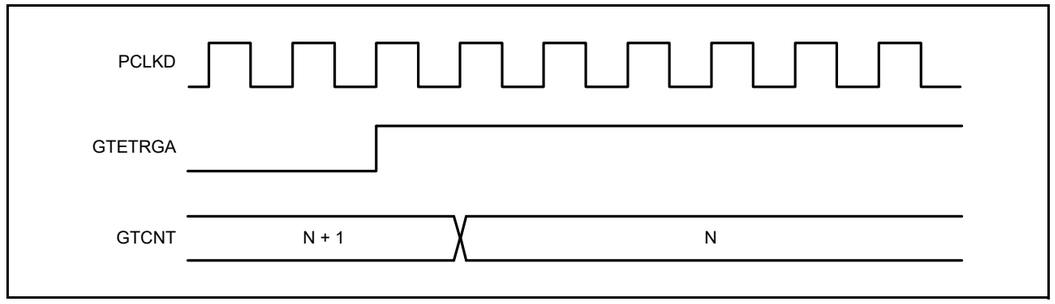


Figure 23.9 使用硬件源递减计数中的事件计数操作示例

图23.10显示了使用硬件资源在递减计数中设置周期性计数操作的示例。

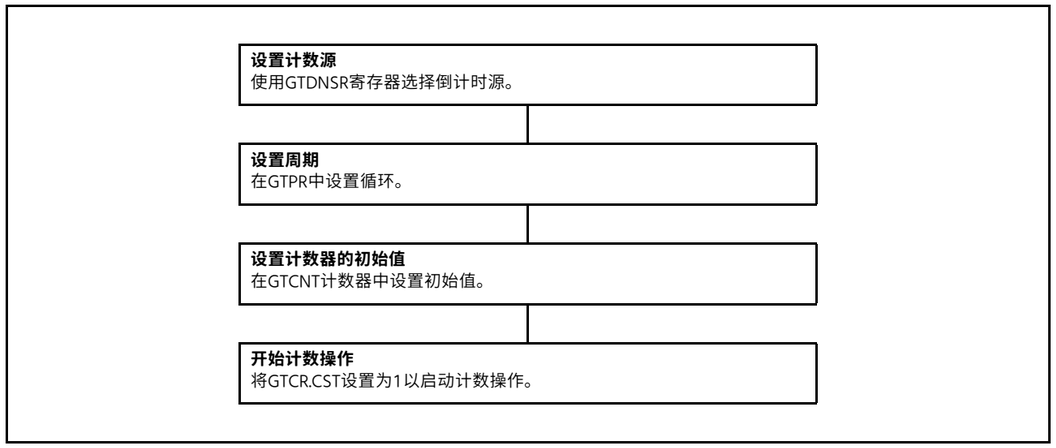


Figure 23.10 使用硬件源在递减计数中设置事件计数操作的示例

(6) 计数器清零操作

每个通道的计数器由以下源清除。

- 将0写入GTCNT寄存器
- 当GTCSR.CCLR位设置为1时，将1写入GTCLR中与GPT通道号相关的位
- 在GTCSR寄存器中选择的硬件源。

计数操作期间禁止写入GTCNT寄存器。GTCNT计数器可以通过向GTCLR写入1和硬件源的清除请求来清除，无论GTCNT正在计数（GTCR.CST=1）还是不计数（GTCR.CST=0）。

对于通过设置GTCR.MD[2:0]和显示递减计数的计数方向标志（GTST.TUCF为0）选择的锯齿波，当向GTCLR寄存器写入1时，GTCNT寄存器设置为GTPR寄存器的值或执行硬件源清除时。当不处于锯齿波模式和向下计数时，当向GTCLR寄存器写入1和执行硬件源清零时，GTCNT寄存器设置为0。

在GTUPSR或GTDNSR中至少有1位设置为1的事件计数操作中，在清除源发生后，立即执行写入GTCLR寄存器和通过硬件源清除以与PCLKD同步。如果使用其他设置，则清除与GTCR.TPCS[2:0]中选择的计数器时钟同步。

23.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock including the event count. At the same time the GPT can output low, high, or toggled output from the associated GTIOCA or GTIOCB output pin. In addition, the GTIOCA or GTIOCB pin output can be low, high, or toggled at the cycle end which is determined by GTPR.

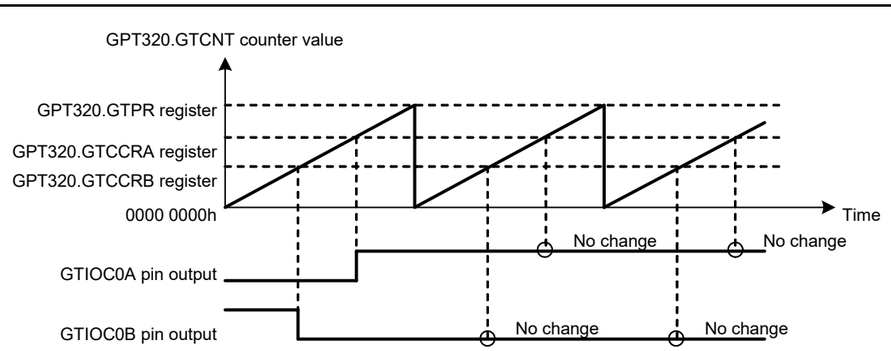
The cycle end is:

- For saw waves in up-counting – when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting – when GTCNT changes from 0 to GTPR value (underflow)
- For saw waves – when the GTCNT counter is cleared
- For triangle waves – when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 23.11 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GPT320.GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOC0A pin by a GPT320.GTCCRA compare match, and low is output from the GTOC0B pin by a GPT320.GTCCRB compare match. The pin level does not change when the specified level and pin level match.



[Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits: Initial output is low, high output at compare match, output retained at cycle end

GPT320.GTIOR.GTIOB[4:0] bits: Initial output is high, low output at compare match, output retained at cycle end

Figure 23.11 Example of low output and high output operation

23.3.1.2 比较匹配的波形输出

比较匹配意味着GTCNT计数器值与GTCCRA或GTCCRB的值匹配。当比较匹配发生时，比较匹配标志与包括事件计数的计数时钟同步生成。同时，GPT可以从相关的GTIOCA或GTIOCB输出引脚输出低、高或切换输出。此外，GTIOCA或GTIOCB引脚输出可以是低电平、高电平或在由GTPR确定的周期结束时切换。

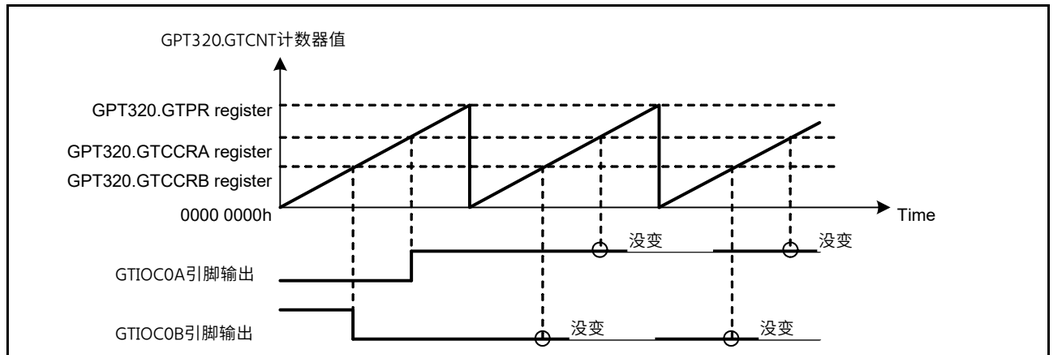
循环结束为：

- 对于向上计数中的锯齿波——当GTCNT从GTPR值变为0（溢出）时
- 对于向下计数中的锯波——当GTCNT从0变为GTPR值时（下溢）
- 对于锯齿波——当GTCNT计数器清零时
- 对于三角波——当GTCNT从0变为1（波谷）时。

(1) 低输出和高输出

图23.11显示了通过GTCCRA和比较匹配的低输出和高输出操作示例
GTCCRB.

在本例中，GPT320.GTCNT计数器进行递增计数，设置为通过GPT320.GTCCRA比较匹配从GTIOC0A引脚输出高电平，通过GPT320.GTCCRB比较匹配从GTOC0B引脚输出低电平.当指定电平和引脚电平匹配时，引脚电平不会改变。



[Setting examples]

GPT320.GTIOR.GTIOA[4:0]位：初始输出低，比较匹配时输出高，循环结束时保持输出

GPT320.GTIOR.GTIOB[4:0]位：初始输出为高电平，比较匹配时输出低电平，循环结束时保持输出

Figure 23.11 低输出和高输出操作示例

Figure 23.12 shows an example for setting low output and high output operation.

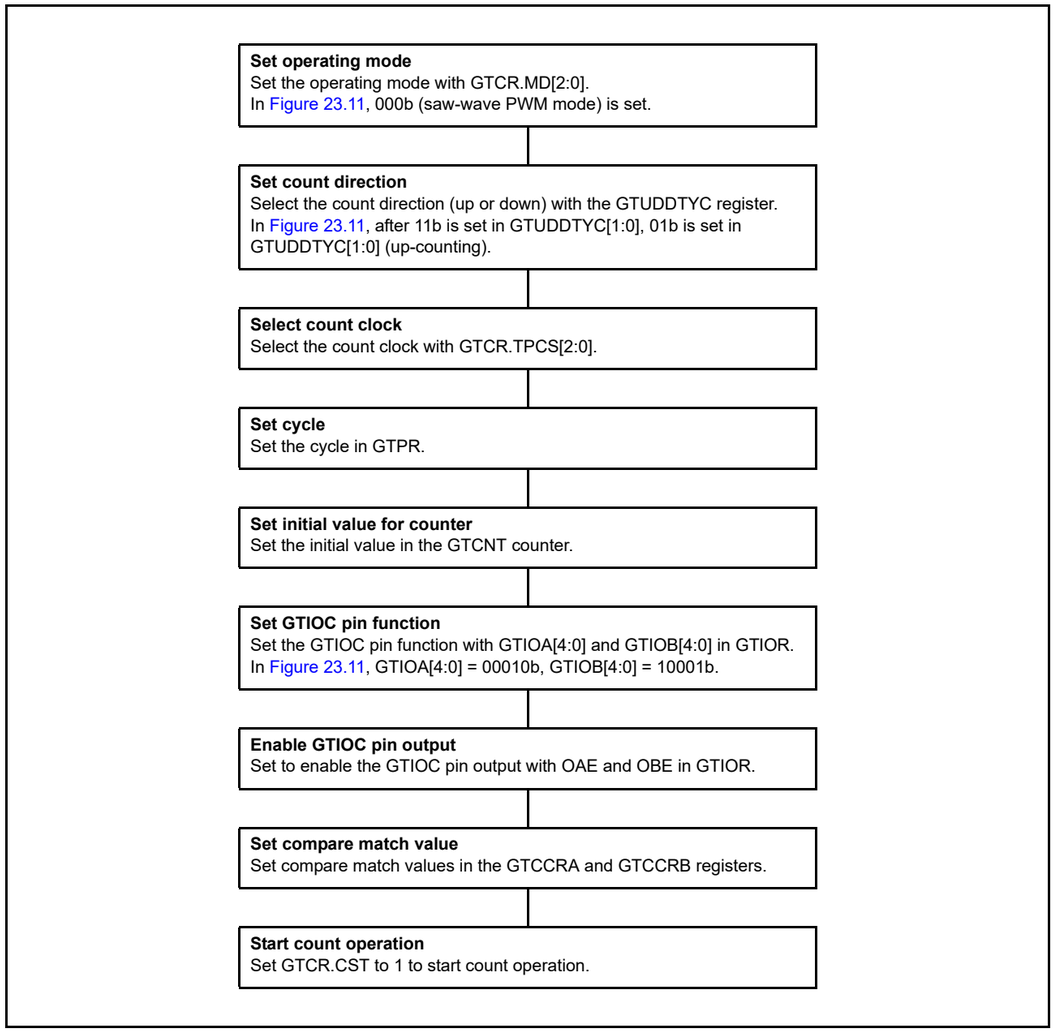


Figure 23.12 Example setting for low output and high output operation

(2) Toggled output

Figure 23.13 and Figure 23.14 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 23.13, the GPT320.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A pin output by a GPT320.GTCCRA compare match and GTIOC0B pin output by a GPT320.GTCCRB compare match are toggled.

In Figure 23.14, the GPT320.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A output is toggled by a compare match of GPT320.GTCCRA and the GTIOC0B output is toggled at the cycle end.

图23.12显示了设置低输出和高输出操作的示例。

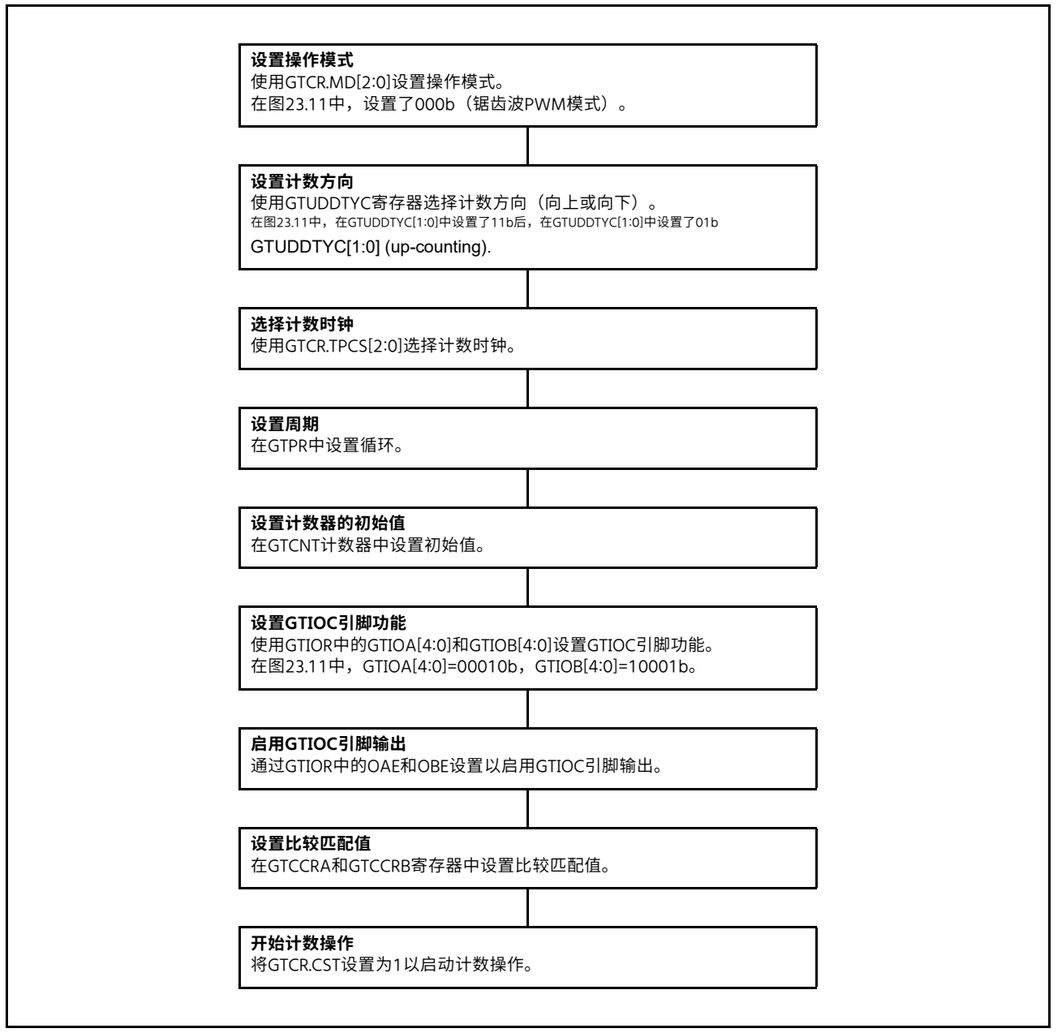


Figure 23.12 低输出和高输出操作的示例设置

(2) Toggled output

图23.13和图23.14通过GTCCRA和GTCCRB的比较匹配显示了切换输出操作的示例。在图23.13中，GPT320.GTCNT计数器执行递增计数，并进行设置，以使GPT320.GTCCRA比较匹配输出的GTIOC0A引脚和GPT320.GTCCRB比较匹配输出的GTIOC0B引脚切换。

在图23.14中，GPT320.GTCNT计数器执行向上计数，并进行设置，以使GTIOC0A输出通过GPT320.GTCCRA的比较匹配来切换，并且GTIOC0B输出在周期结束时切换。

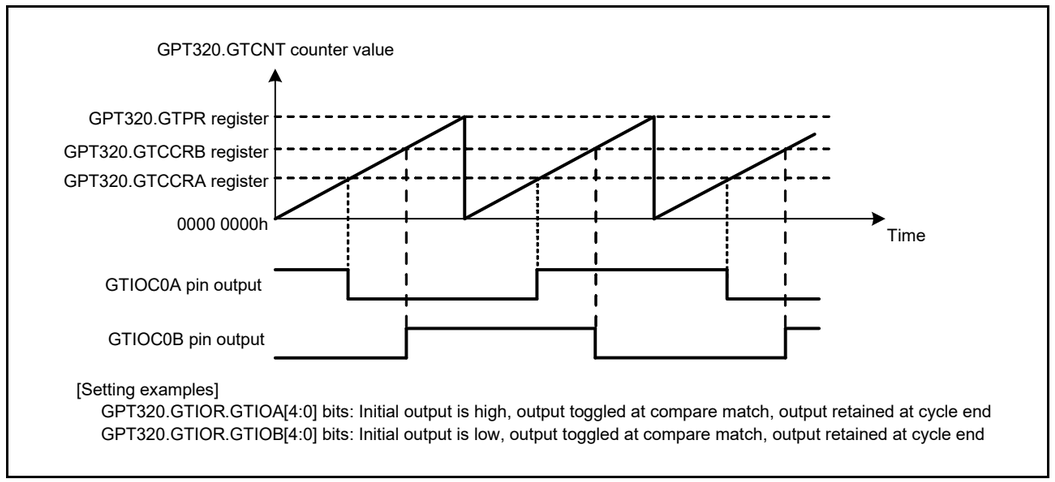


Figure 23.13 Example of toggled output operation (1)

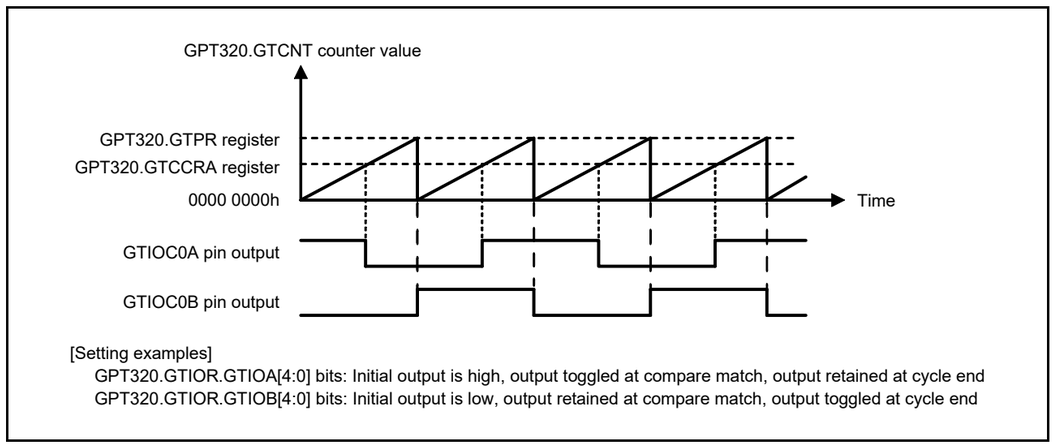


Figure 23.14 Example of toggled output operation (2)

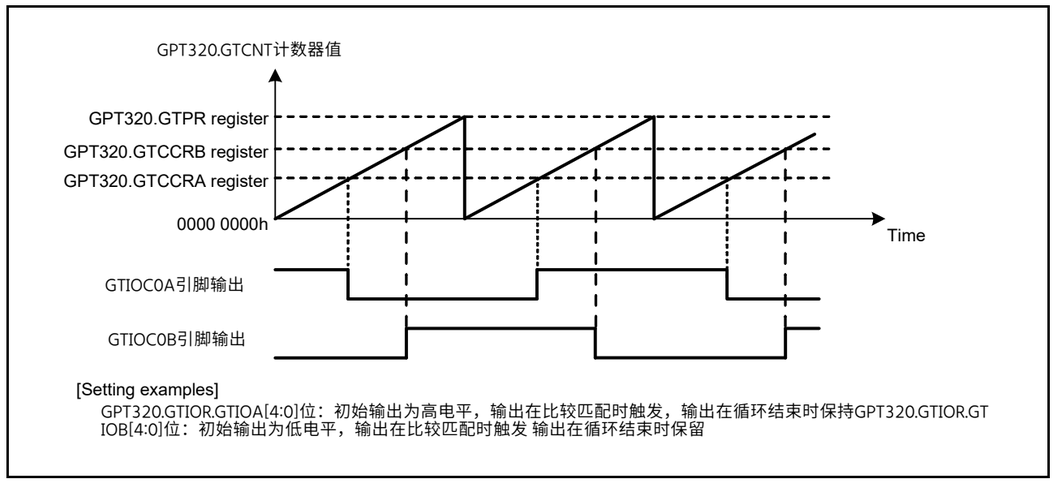


Figure 23.13 切换输出操作示例(1)

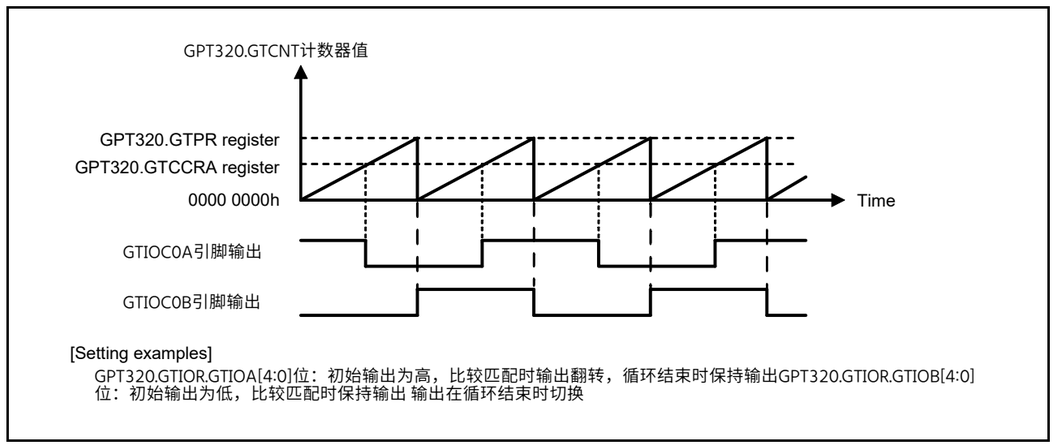


Figure 23.14 切换输出操作示例(2)

Figure 23.15 shows an example setting for toggled output operation.

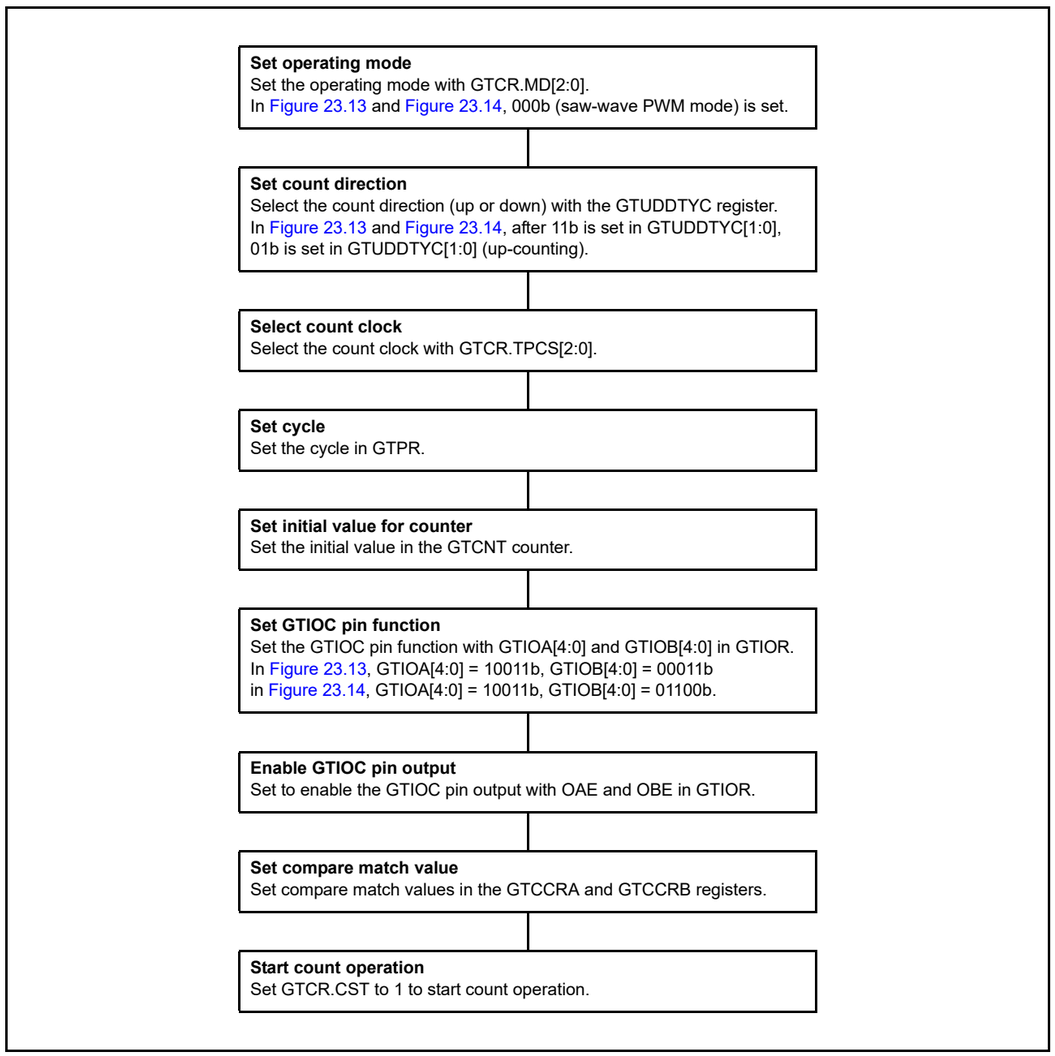


Figure 23.15 Example for setting toggled output operation

23.3.1.3 Input capture function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 23.16 shows an example of the input capture function.

In this example, the GPT320.GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTICCRA at both edges of the GTIOC0A input pin and to GTICCRB on the rising edge of the GTIOC0B input pin.

图23.15显示了切换输出操作的示例设置。

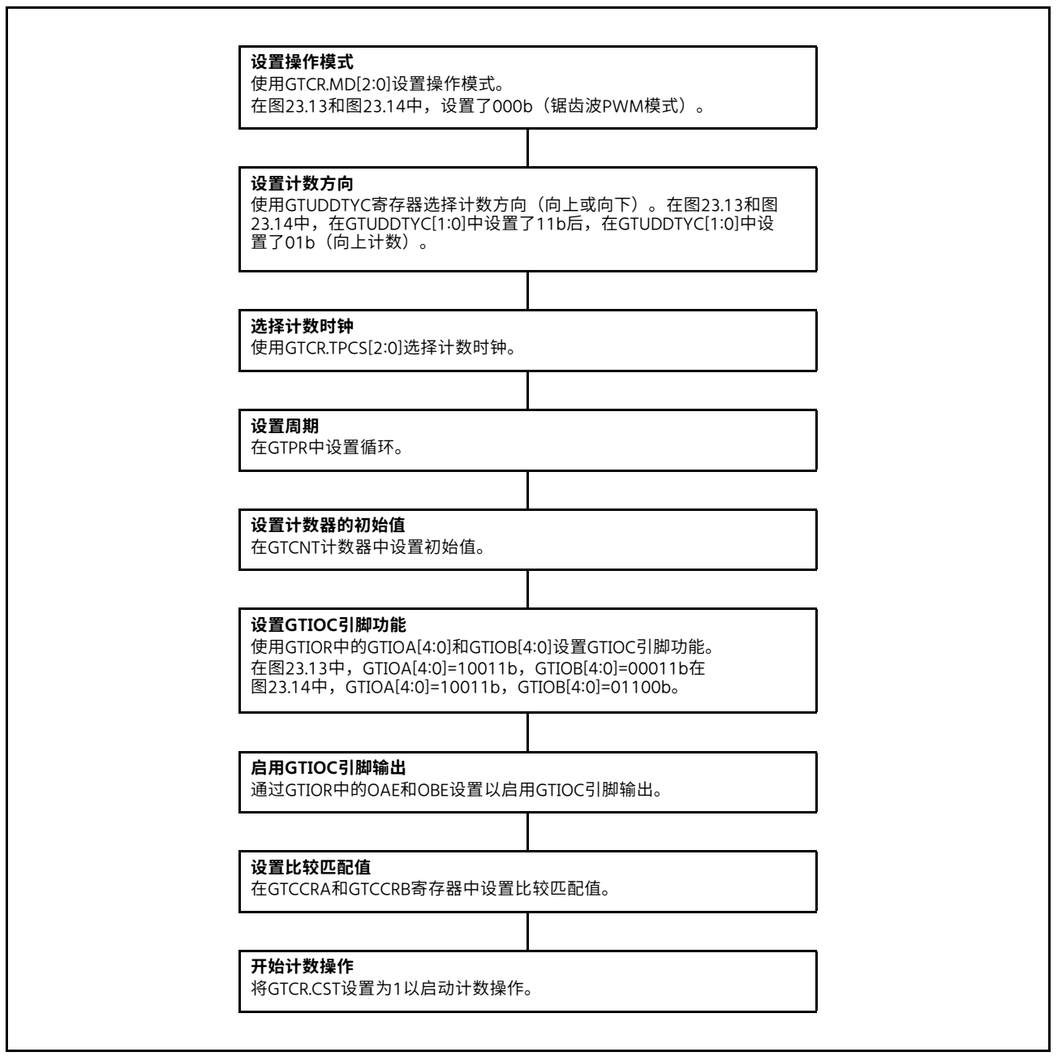


Figure 23.15 设置切换输出操作的示例

23.3.1.3 输入捕捉功能

在检测到在GTICASR和GTICBSR中设置的硬件源时，可以将GTCNT计数器值传输到GTCCRA或GTCCRB。

图23.16显示了输入捕获函数的示例。

在本例中，GPT320.GTCNT计数器通过计数时钟进行递增计数，并进行了设置，以便在GTIOC0A输入引脚的两个边沿对GTICCRA执行输入捕获，并在GTIOC0B输入的上升沿对GTICCRB执行输入捕获别针。

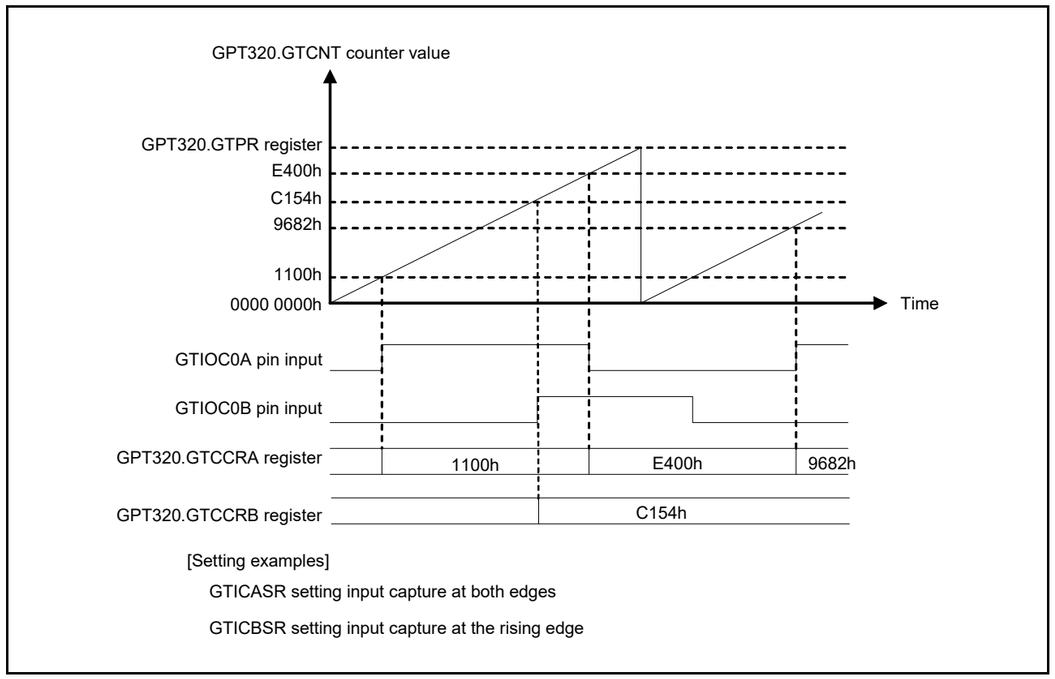


Figure 23.16 Example of input capture operation

Figure 23.17 shows an example for setting an input capture operation with count operation by the count clock.

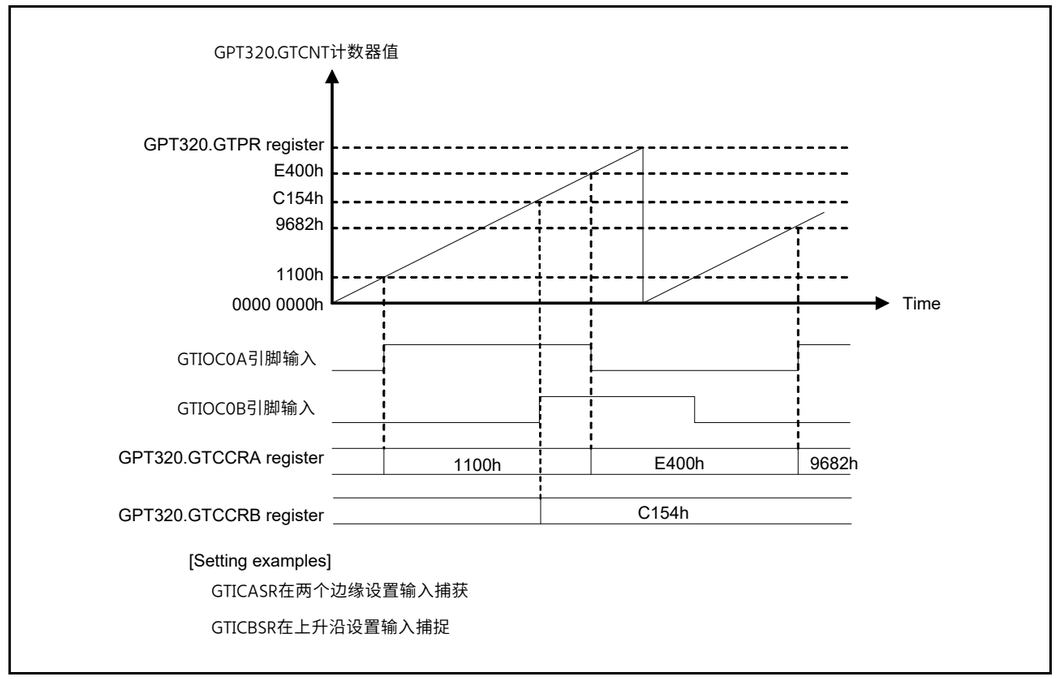


Figure 23.16 输入捕捉操作示例

图23.17显示了一个通过计数时钟设置计数操作的输入捕捉操作的示例。

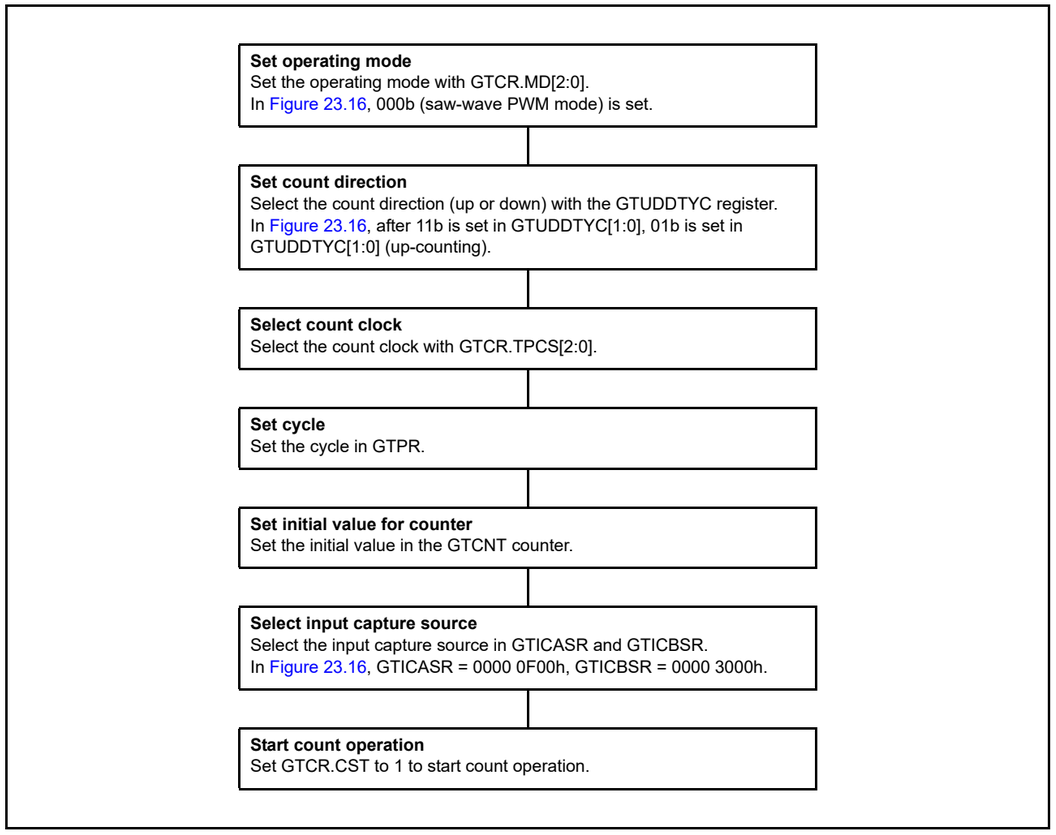


Figure 23.17 Example for setting input capture operation

23.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR and GTPBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF.

23.3.2.1 GTPR register buffer operation

GTPBR can function as a buffer register for GTPR. The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR[23:0])
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR[n] bit is set to 1, n = channel number).

Figure 23.18 to Figure 23.20 show examples of GTPR buffer operation, and Figure 23.21 shows an example setting for GTPR buffer operation.

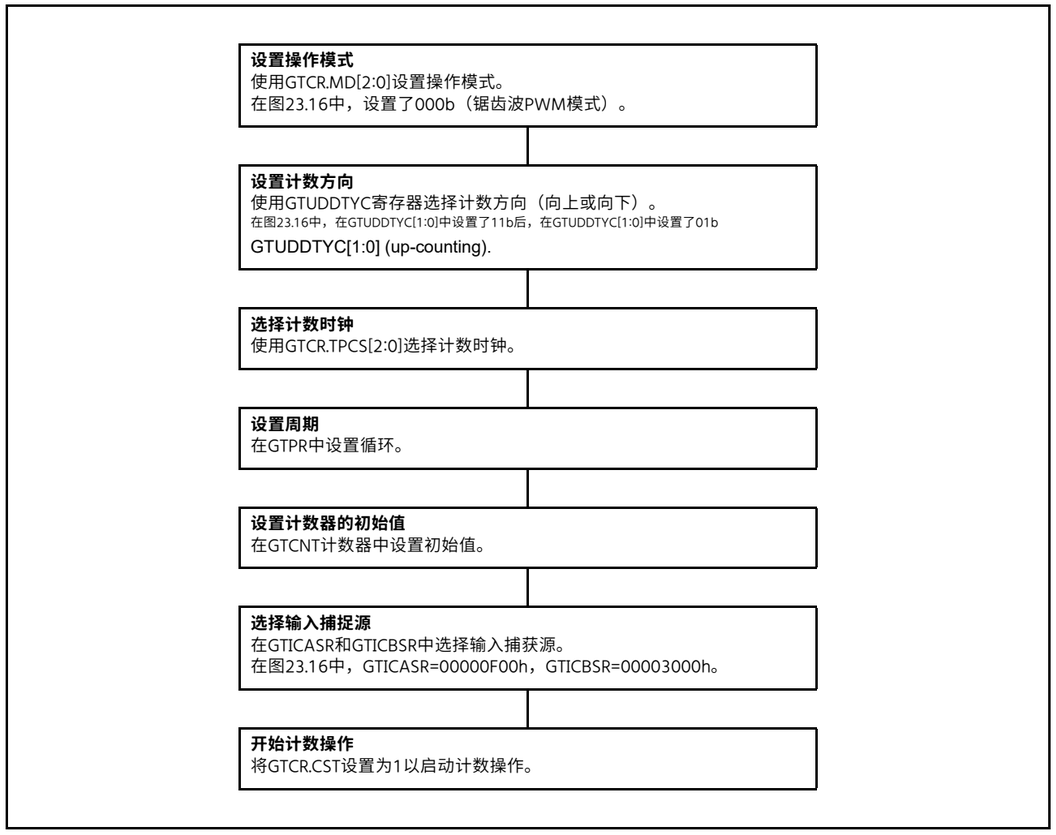


Figure 23.17 设置输入捕捉操作的示例

23.3.2 缓冲操作

可以使用GTBER设置以下缓冲区操作：

- GTPR and GTPBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF.

23.3.2.1 GTPR寄存器缓冲操作

GTPBR可以作为GTPR的缓冲寄存器。缓冲区传输在锯齿波模式或事件计数中的上溢（向上计数期间）或下溢（向下计数期间）以及三角波模式的波谷处执行。

在锯齿波模式或事件计数中，当计数期间发生以下计数器清零操作时，将执行缓冲区传输：

- 通过硬件源清除（清除源在GTCSR[23:0]中选择）
- 由软件清零（当GTCSR.CCLR位为1且GTCLR[n]位设置为1时，n=通道号）。

图23.18至图23.20显示了GTPR缓冲区操作的示例，图23.21显示了示例设置GTPR缓冲区操作。

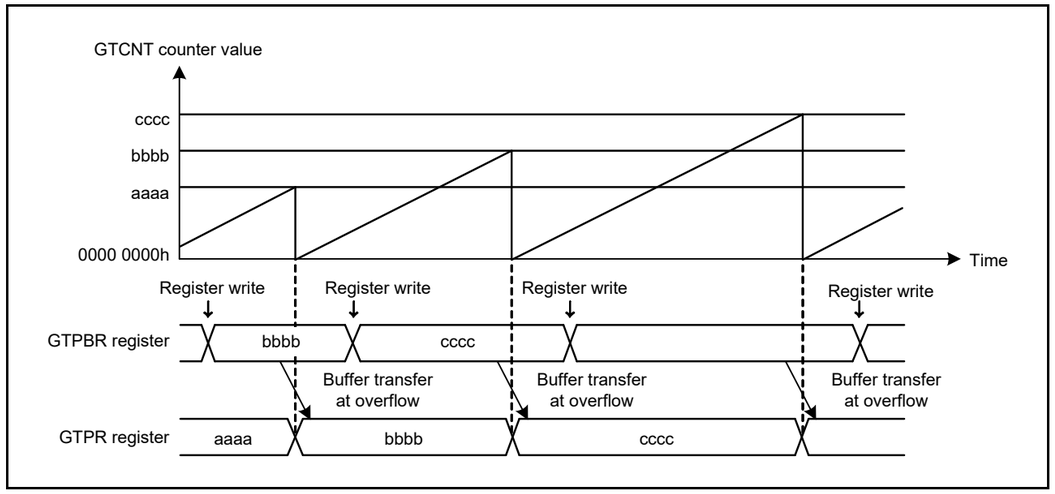


Figure 23.18 Example of GTPR buffer operation with saw waves in up-counting

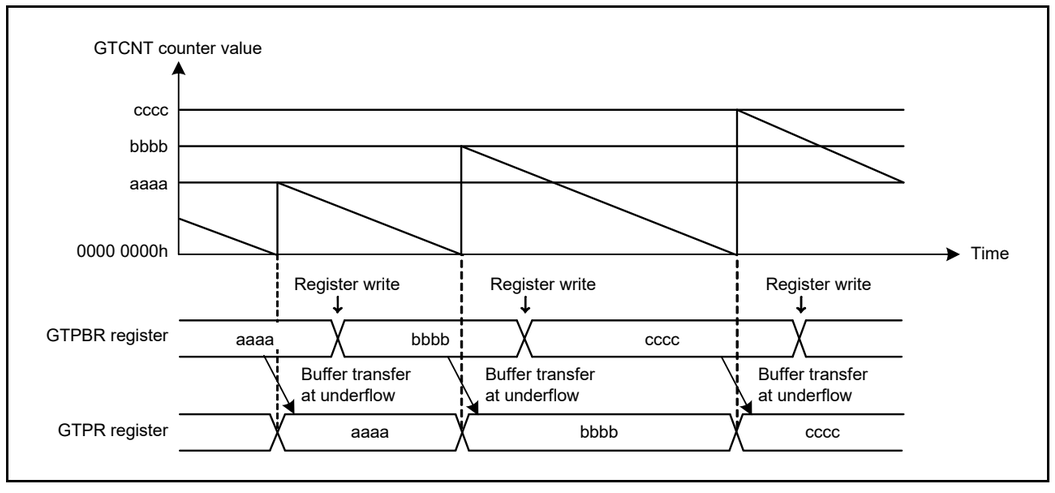


Figure 23.19 Example of GTPR buffer operation with saw waves in down-counting

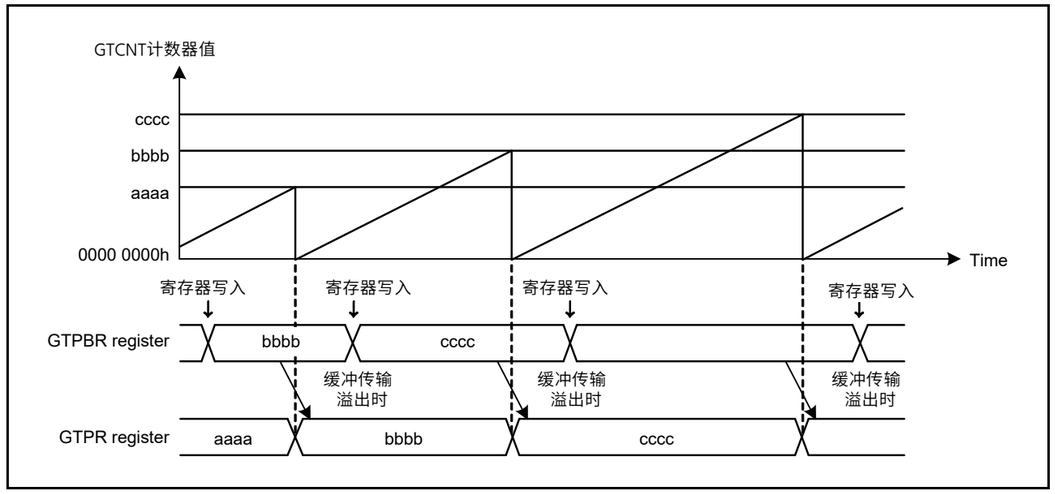


Figure 23.18 GTPR缓冲区操作示例，在向上计数中使用锯齿波

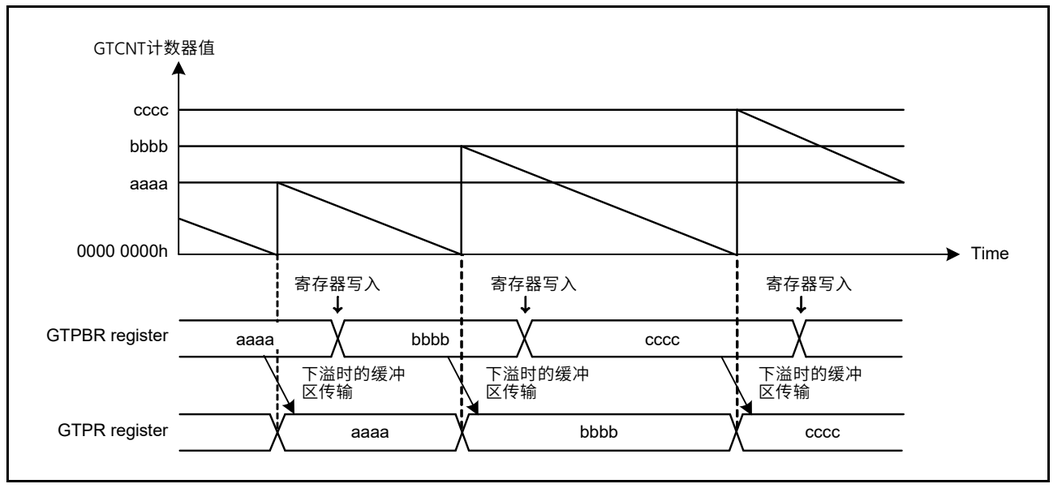


Figure 23.19 向下计数中锯波的GTPR缓冲区操作示例

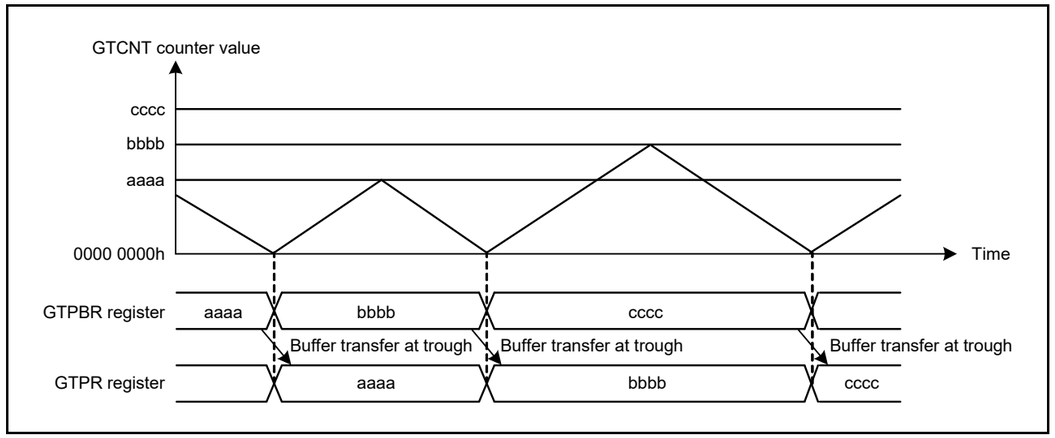


Figure 23.20 Example of GTPR buffer operation with triangle waves

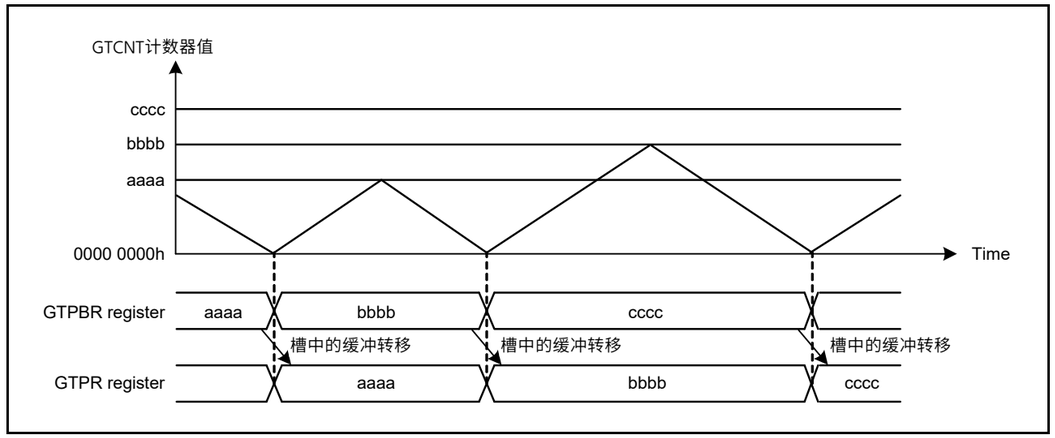


Figure 23.20 使用三角波的GTPR缓冲操作示例

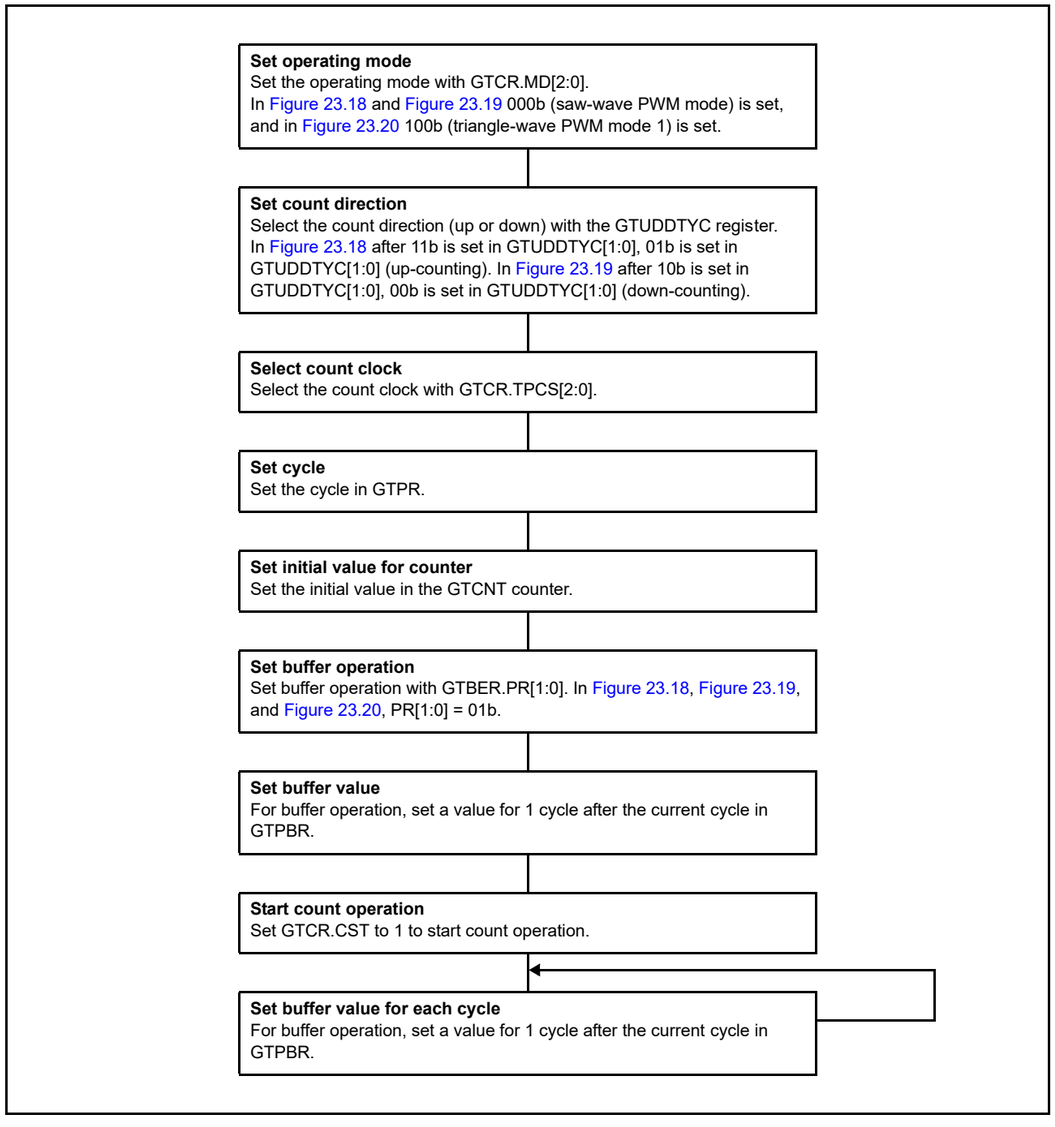


Figure 23.21 Example for setting GTPR buffer operation

23.3.2.2 Buffer operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For a single buffer operation, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 01b. To set GTCCRA or GTCCRB to not function as a buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 00b.

(1) When GTCCRA or GTCCRB functions as an output compare register

Buffer transfer occurs in the following situations:

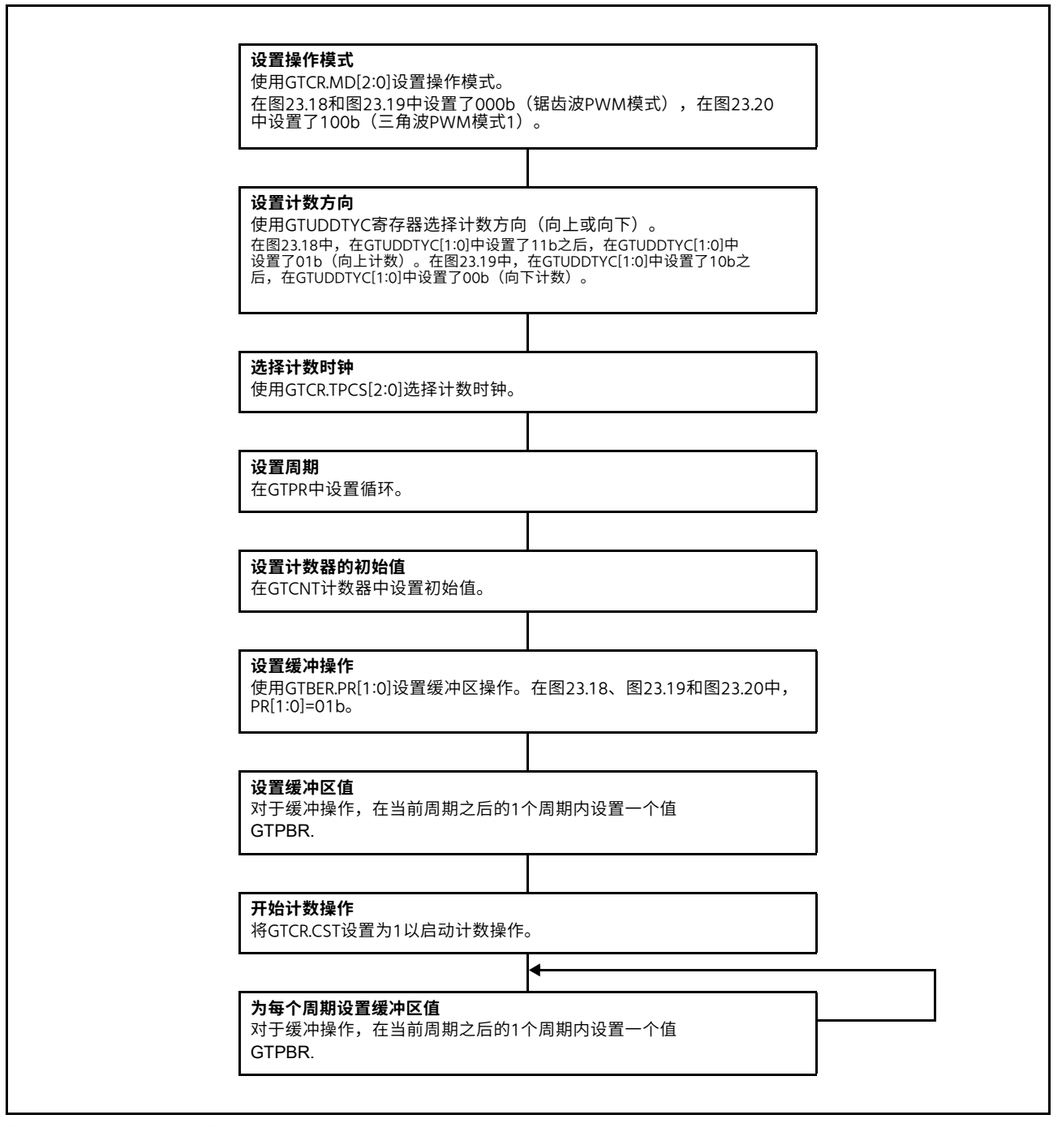


Figure 23.21 设置GTPR缓冲区操作的示例

23.3.2.2 GTCCRA和GTCCRB的缓冲操作

GTCCRC可以作为GTCCRA缓冲寄存器，GTCCRD可以作为GTCCRC缓冲寄存器（GTCCRA的双缓冲寄存器）。同样，GTCCRE可以作为GTCCRB缓冲寄存器，GTCCRF可以作为GTCCRE缓冲寄存器（GTCCRB的双缓冲寄存器）。

要将GTCCRA或GTCCRB设置为双缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为10b或11b。对于单个缓冲区操作，将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为01b。要将GTCCRA或GTCCRB设置为不用作缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为00b。

(1) 当GTCCRA或GTCCRB用作输出比较寄存器时

缓冲区传输发生在以下情况：

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources the same as in the case of section 23.3.2.1, GTPR register buffer operation. In triangle-wave mode, buffer transfer is not performed by the counter clear.
- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfers are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode. Additionally, buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave 1 shot pulse mode or triangle-wave PWM mode 3.

Figure 23.22 to Figure 23.24 show examples of GTCCRA and GTCCRB buffer operation and Figure 23.25 shows an example for setting GTCCRA and GTCCRB buffer operation.

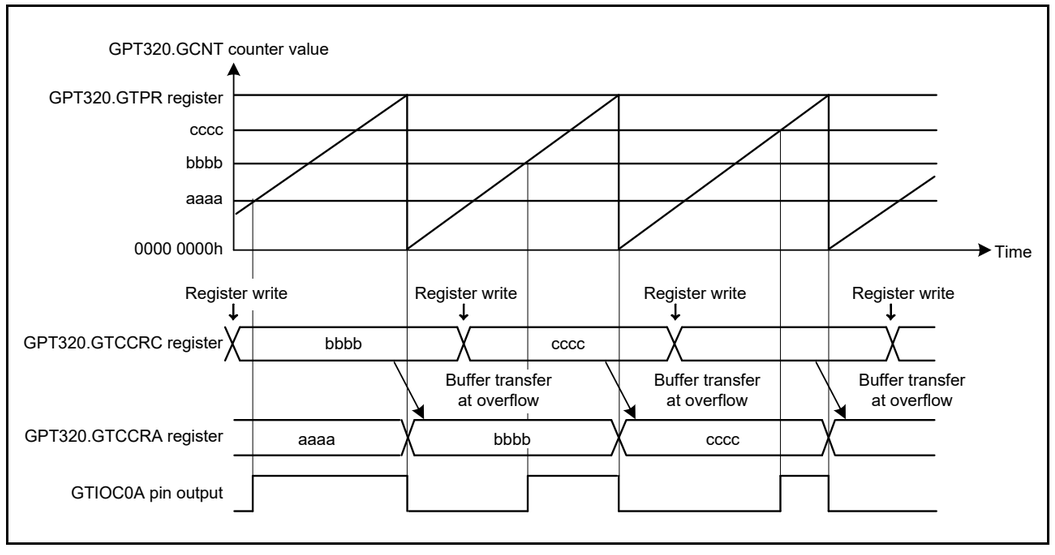


Figure 23.22 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, low output at cycle end

- 通过上溢或下溢进行缓冲区传输
  在锯齿波模式或事件计数操作中，在溢出（向上计数期间）或下溢（向下计数期间）时执行缓冲区传输。在三角波模式中，缓冲区传输在波谷（三角波PWM模式1）或波峰和波谷（三角波PWM模式2）处执行。
- 通过计数器清除缓冲区传输
  在锯齿波模式或事件计数操作中，在计数期间，缓冲区传输（与向上计数期间的溢出或向下计数期间的下溢相同）由计数器清除源执行，与第23.3.2.1节，GTPR寄存器缓冲区操作。在三角波模式下，计数器清零不执行缓冲区传输。
- 强制缓冲转移
  如果在计数操作停止时GTBER.CCRSWT位设置为1，则在锯齿波模式、事件计数操作和三角波模式下强制执行GTCCRA和GTCCRB寄存器缓冲传输。此外，从GTCCRD寄存器到临时寄存器A和从GTCCRF寄存器到临时寄存器B的缓冲区传输是在锯齿波1发射脉冲模式或三角波PWM模式3中执行的。

图23.22至图23.24显示了GTCCRA和GTCCRB缓冲操作的示例，图23.25显示了设置GTCCRA和GTCCRB缓冲操作的示例。

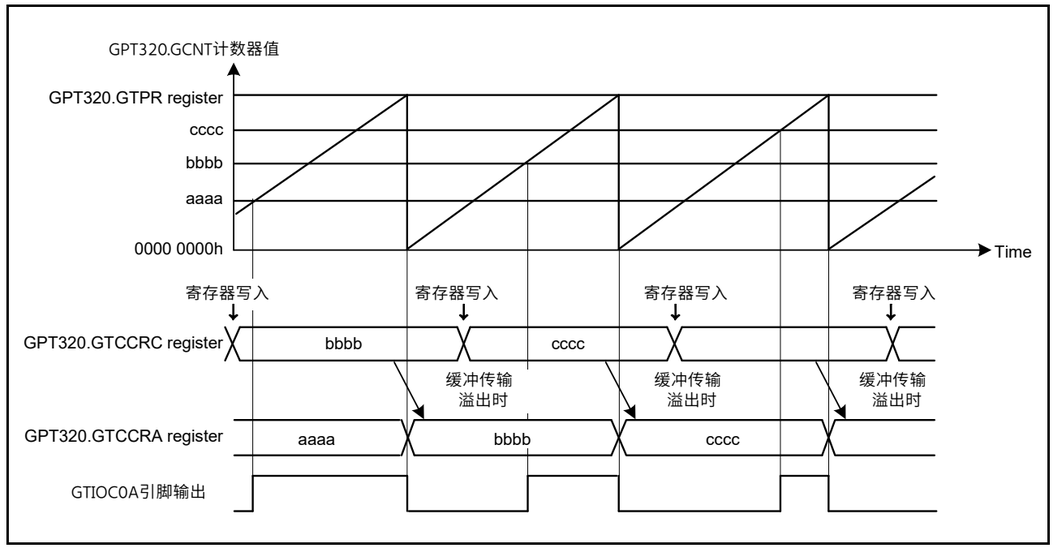


Figure 23.22 带输出比较的GTCCRA和GTCCRB缓冲器操作示例，递增计数时锯齿波，GTCCRA比较匹配时的高输出，循环结束时的低输出

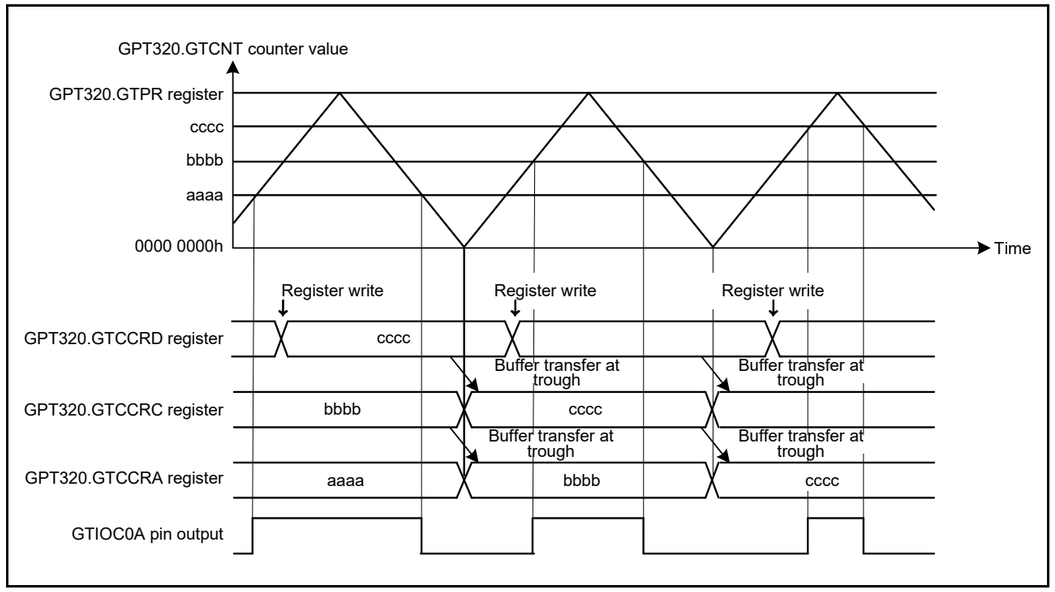


Figure 23.23 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end

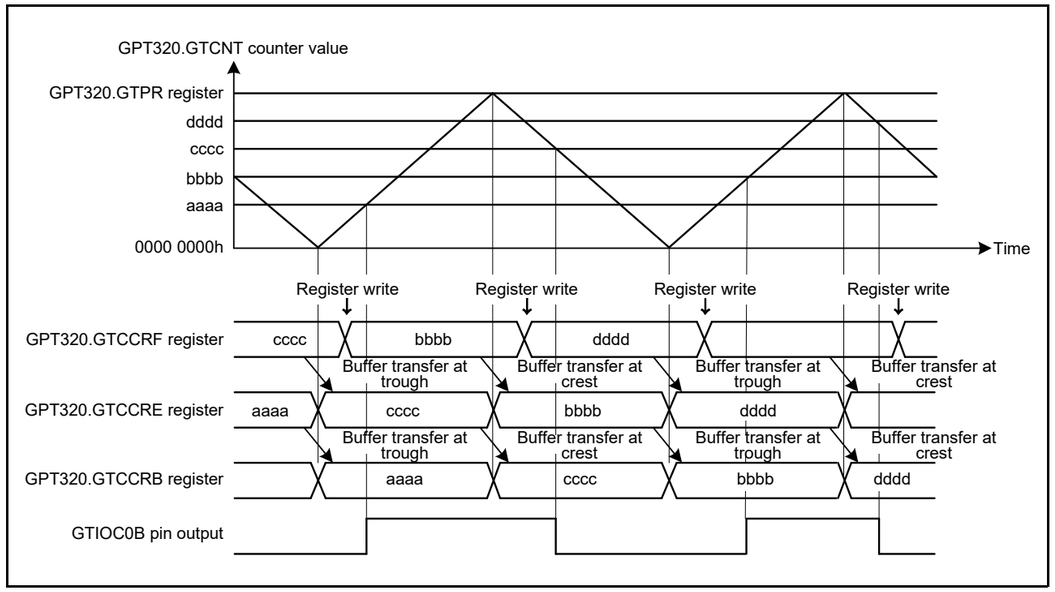


Figure 23.24 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end

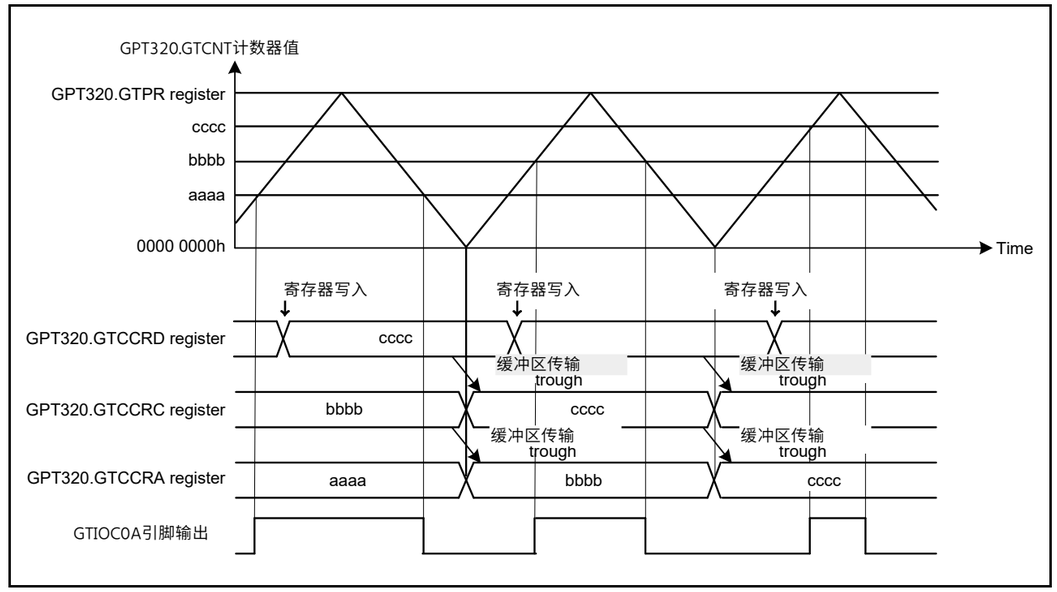


Figure 23.23 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷缓冲操作、GTCCRA比较匹配时切换输出、循环结束时保留输出

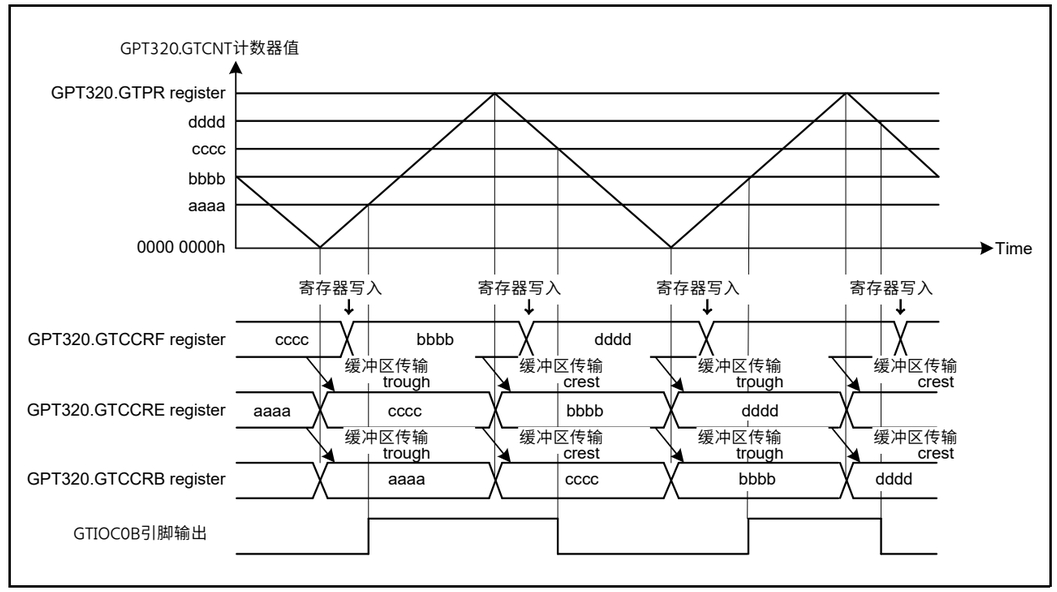


Figure 23.24 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷和波峰缓冲操作、在GTCCRB比较匹配时切换输出以及在周期结束时保留输出

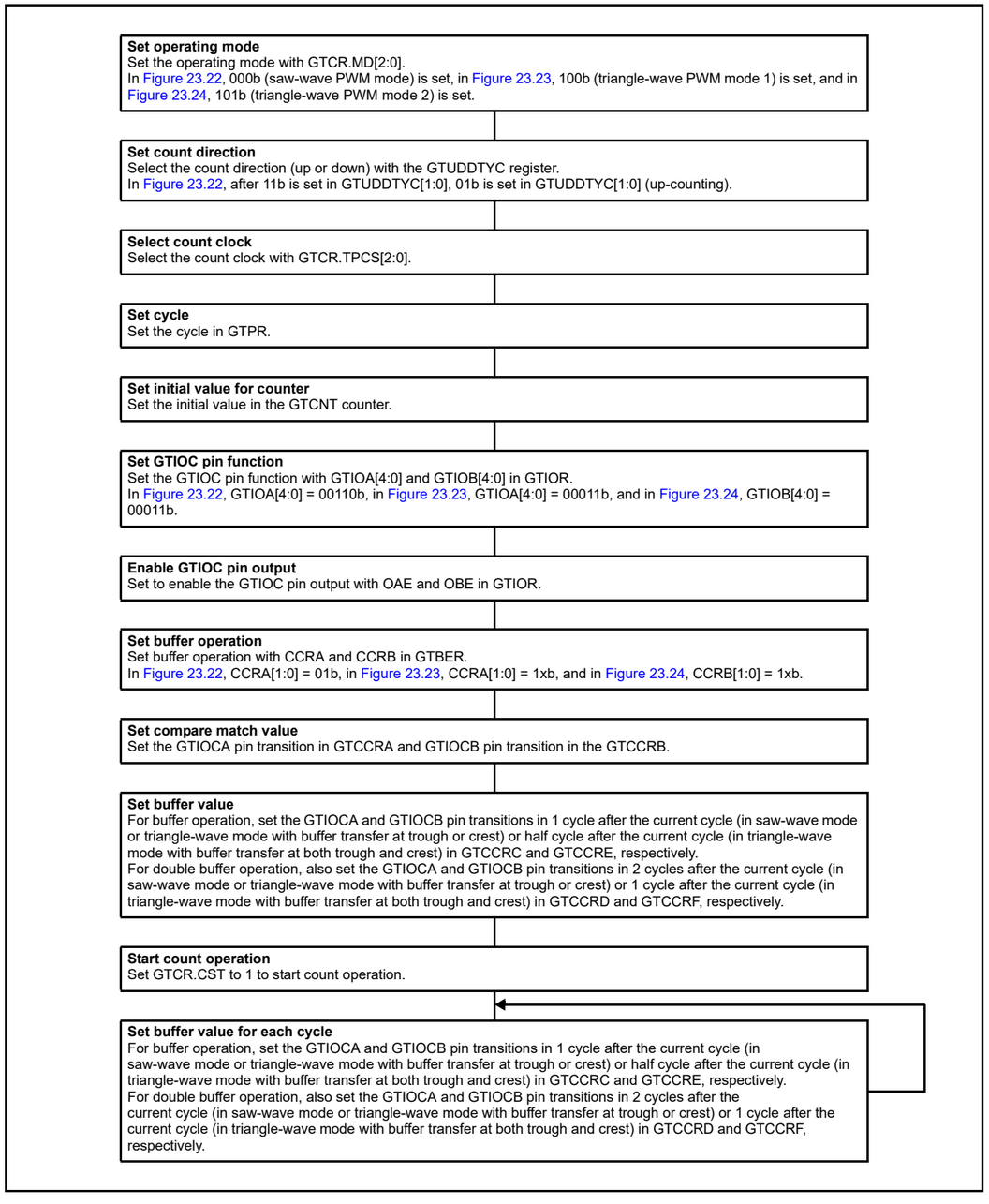


Figure 23.25 Example for setting GTCCRA and GTCCRB buffer operation for output compare

(2) When GTCCRA or GTCCRB functions as an input capture register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 23.25 为输出比较设置GTCCRA和GTCCRB缓冲操作的示例

(2) 当GTCCRA或GTCCRB用作输入捕捉寄存器时

当产生输入捕捉时，GTCNT计数器值被传送到GTCCRA和GTCCRB并存储GTCCRA和GTCCRB寄存器值被传送到缓冲寄存器。在输入捕捉操作中，缓冲区传输不是由计数器清零来执行的。

Figure 23.26 and Figure 23.27 show examples of GTCCRA and GTCCRB buffer operation and Figure 23.28 shows an example for setting the GTCCRA and GTCCRB buffer operation.

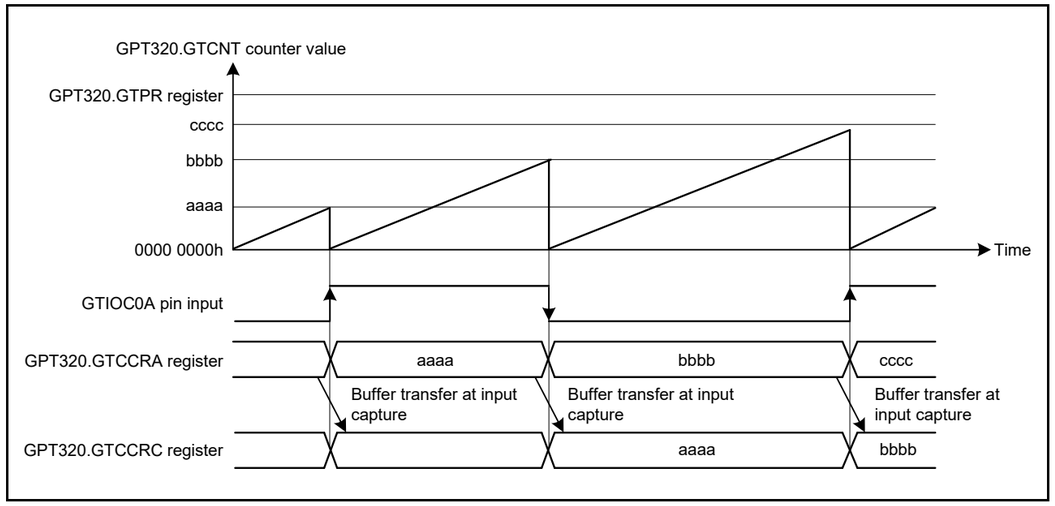


Figure 23.26 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOC0A input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0A input

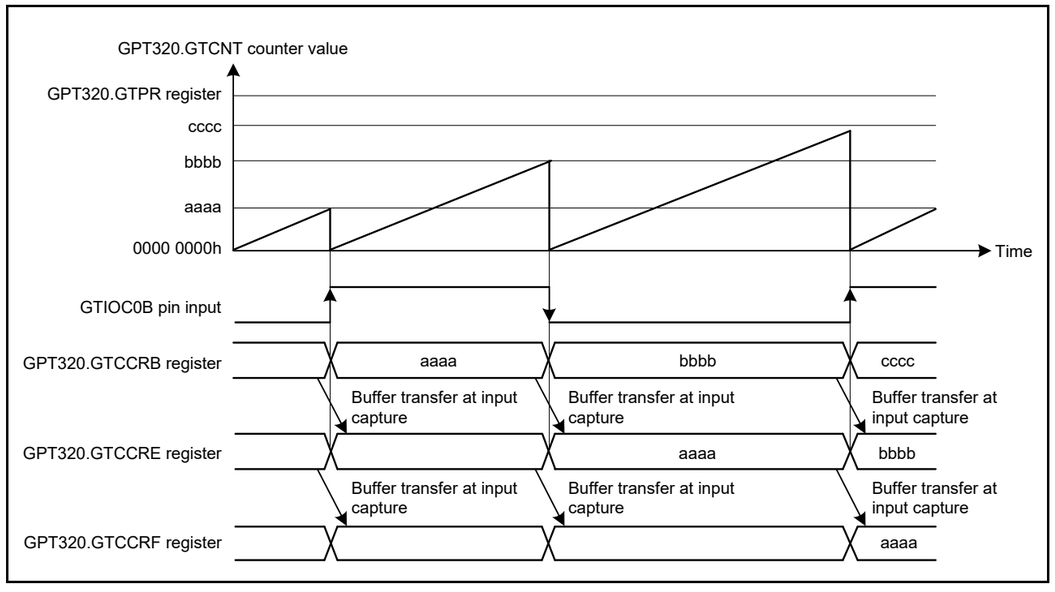


Figure 23.27 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOC0B input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0B input

图23.26和图23.27显示了GTCCRA和GTCCRB缓冲操作的示例，图23.28显示了设置GTCCRA和GTCCRB缓冲操作的示例。

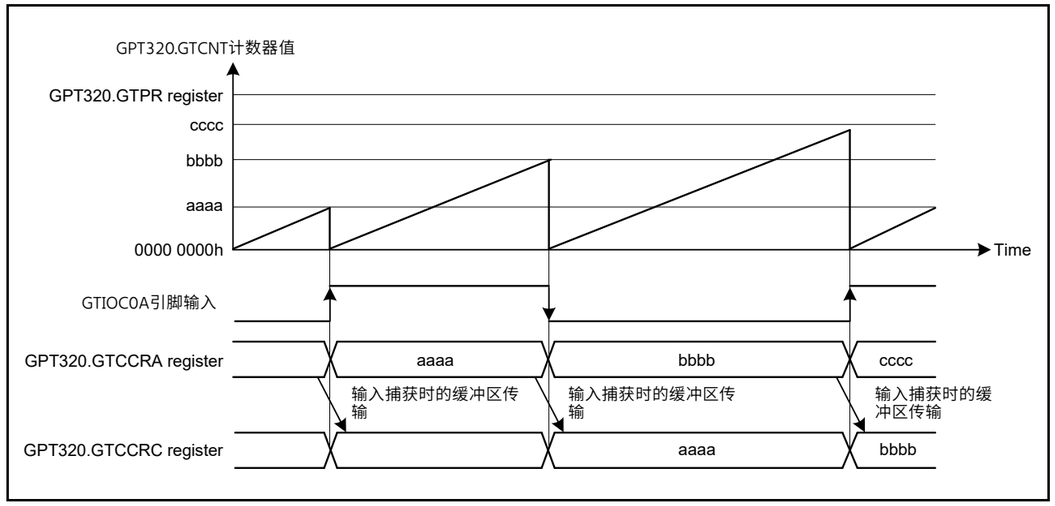


Figure 23.26 GTCCRA和GTCCRB缓冲器操作示例，在GTIOC0A输入的两个边沿进行输入捕获，在向上计数时看到锯齿波，并且在GTIOC0A输入的两个边沿清除GTCNT计数器

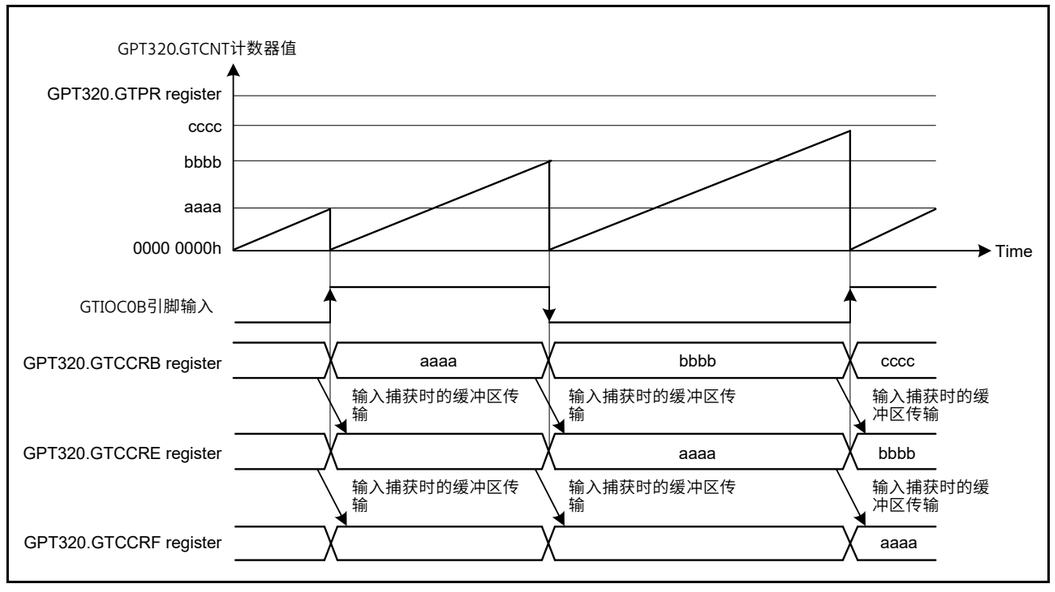


Figure 23.27 GTCCRA和GTCCRB双缓冲操作示例，在两个边沿进行输入捕获GTIOC0B输入，递增计数中的锯齿波，并且GTCNT计数器在GTIOC0B input

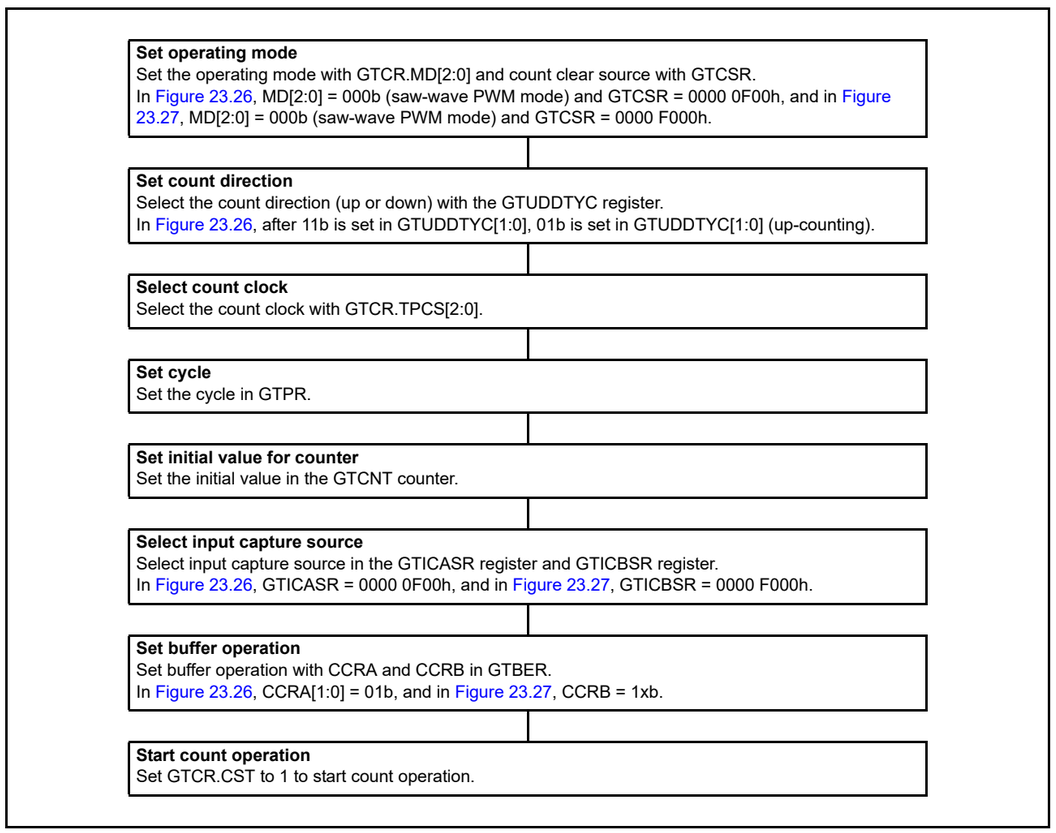


Figure 23.28 Example setting for GTCCRA and GTCCRB buffer operation with input capture

23.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCA or GTIOCB pin by a compare match between the GTCNT counter and GTCCRA or GTCCRB. By setting GTDTCR and GTDVU, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

23.3.3.1 Saw-wave PWM mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR. A PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting

Figure 23.29 shows an example of saw-wave PWM mode operation, and Figure 23.30 shows an example setting for saw-wave PWM mode.

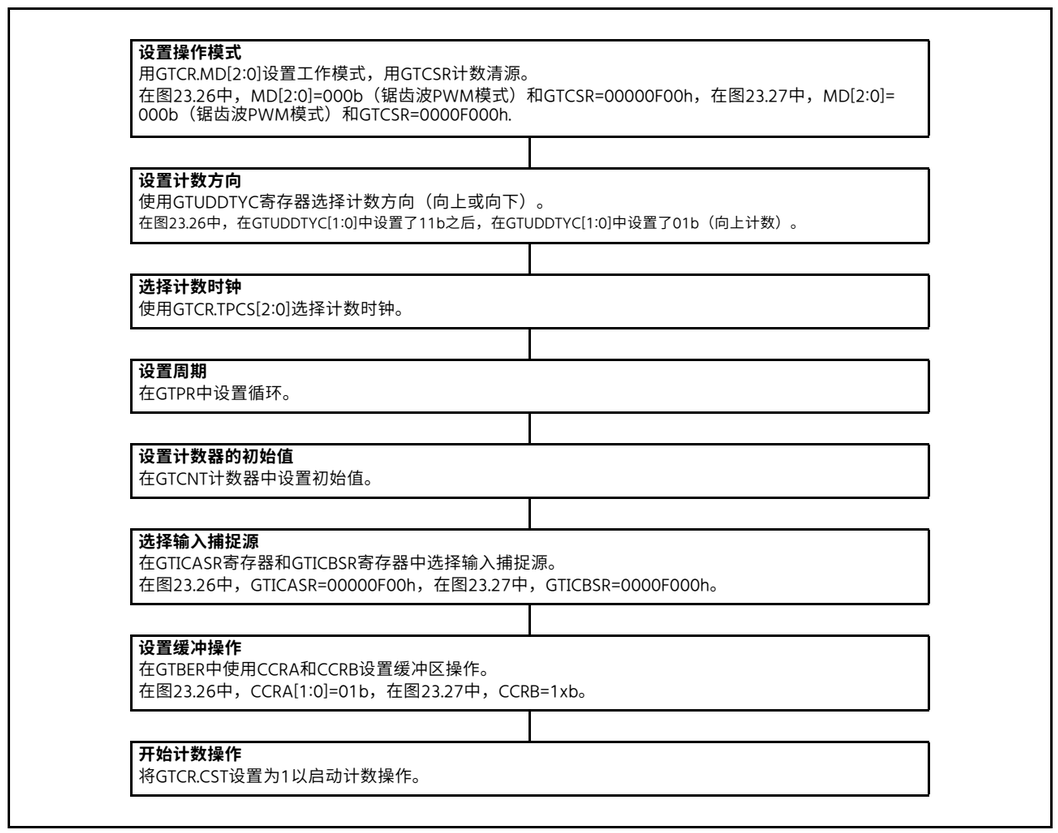


Figure 23.28 带输入捕获的GTCCRA和GTCCRB缓冲区操作设置示例

23.3.3 PWM输出工作模式

通过GTCNT计数器与GTCCRA或GTCCRB之间的比较匹配，GPT可以将PWM波形输出到GTIOCA或GTIOCB引脚。通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

23.3.3.1 Saw-wave PWM mode

在锯齿波PWM模式下，GTCNT通过在GTPR中设置周期来执行锯齿波（半波）操作。当GTCCRA或GTCCRB比较匹配发生时，PWM波形输出到GTIOCA或GTIOCB引脚。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，以进行比较匹配和循环结束

图23.29显示了锯波PWM模式操作的示例，图23.30显示了锯波PWM模式的示例设置。

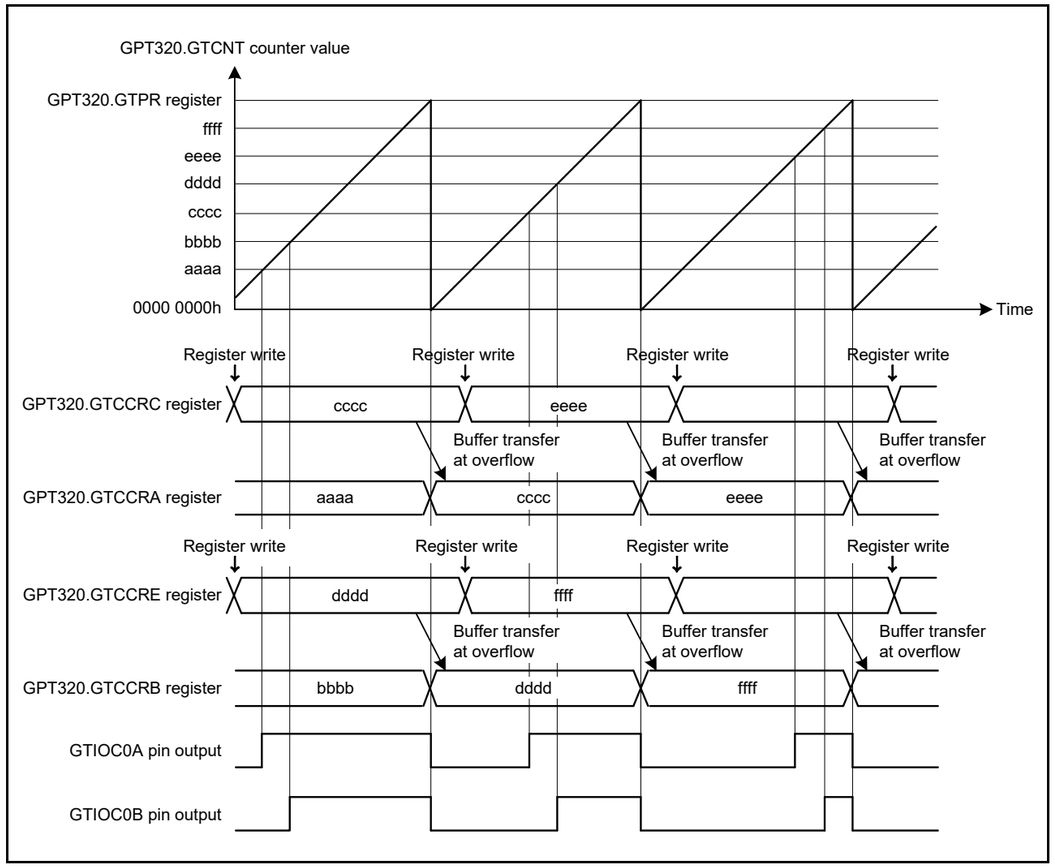


Figure 23.29 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end

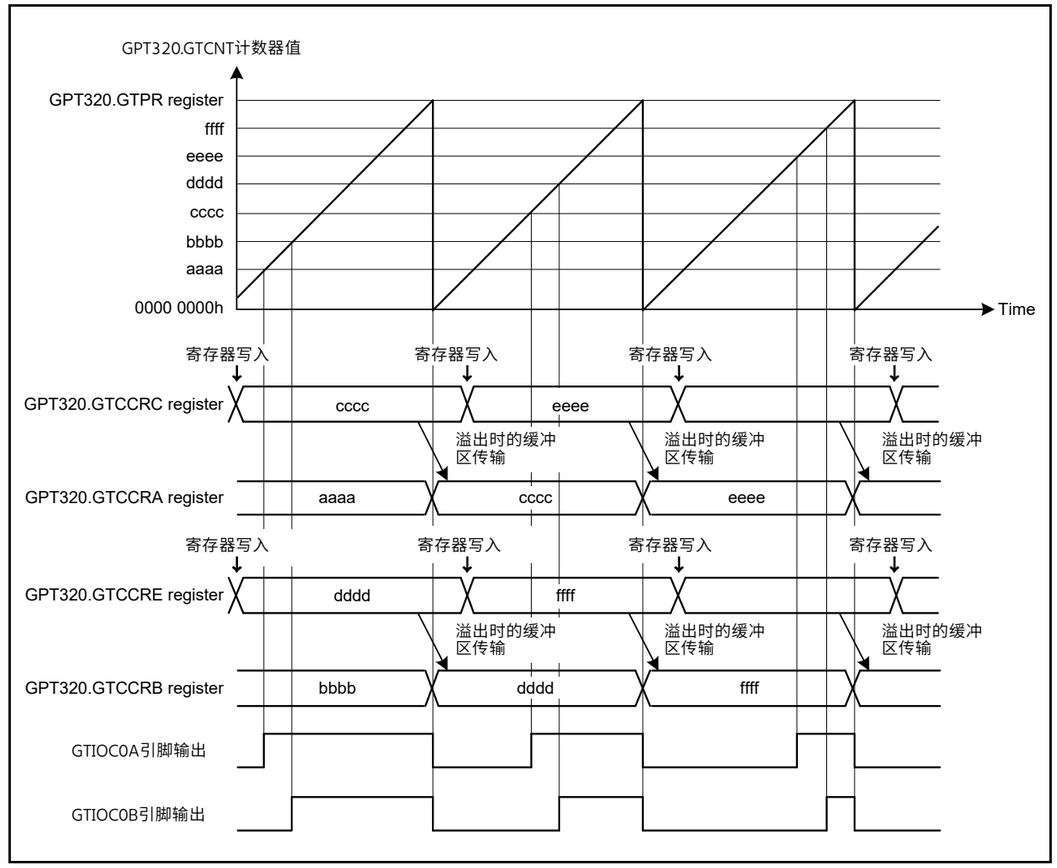


Figure 23.29 具有递增计数、缓冲操作、高输出的锯齿波PWM模式操作示例 GTCCRAGTCCRB比较匹配，循环结束时输出低

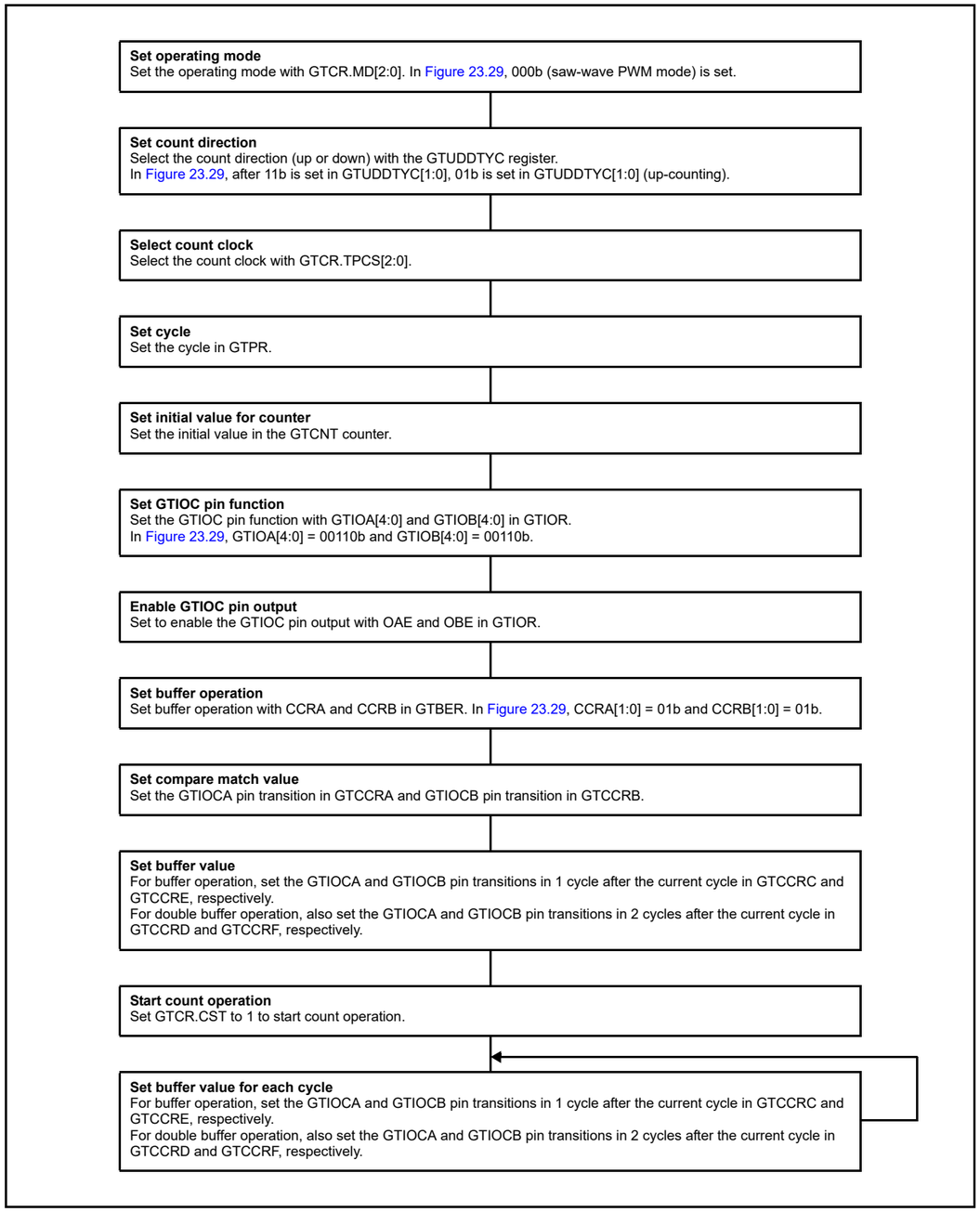


Figure 23.30 Example setting for saw-wave PWM mode

Figure 23.30 锯齿波PWM模式设置示例

23.3.3.2 Saw-wave one-shot pulse mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR. The GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.31 shows an example of saw-wave one-shot pulse mode operation, and Figure 23.32 shows an example setting for saw-wave one-shot pulse mode.

23.3.3.2 锯波单发脉冲模式

锯齿波单发脉冲模式是在GTPR中设置周期的模式。GTCNT计数器执行锯齿波（半波）操作，并且在GTCCRA或GTCCRB的比较匹配时将PWM波形输出到GTIOCA或GTIOCB引脚，且缓冲器操作固定。

锯波单次脉冲模式中的缓冲操作不同于通常的缓冲操作。缓冲区传输从以下位置执行：

- 循环结束时GTCCRC到GTCCRA
- 循环结束时GTCCRE到GTCCRB
- GTCCRD在循环结束时到临时寄存器A
- GTCCRF在循环结束时到临时寄存器B
- 在GTCCRA比较匹配时将临时寄存器A发送到GTCCRA
- 在GTCCRB比较匹配时，临时寄存器B到GTCCRB。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，以进行比较匹配和循环结束。当计数操作停止时GTBER.CCRSWT位设置为1时，缓冲区被强制从GTCCRD寄存器传送到临时寄存器A，并从GTCCRF寄存器传送到临时寄存器B。通过设置GTDTCR和GTDVU，比较匹配值对于带有死区时间的负相位波形，可以自动设置为GTCCRB。

图23.31显示了锯齿波单次脉冲模式操作的示例，图23.32显示了锯齿波单次脉冲模式设置的示例。

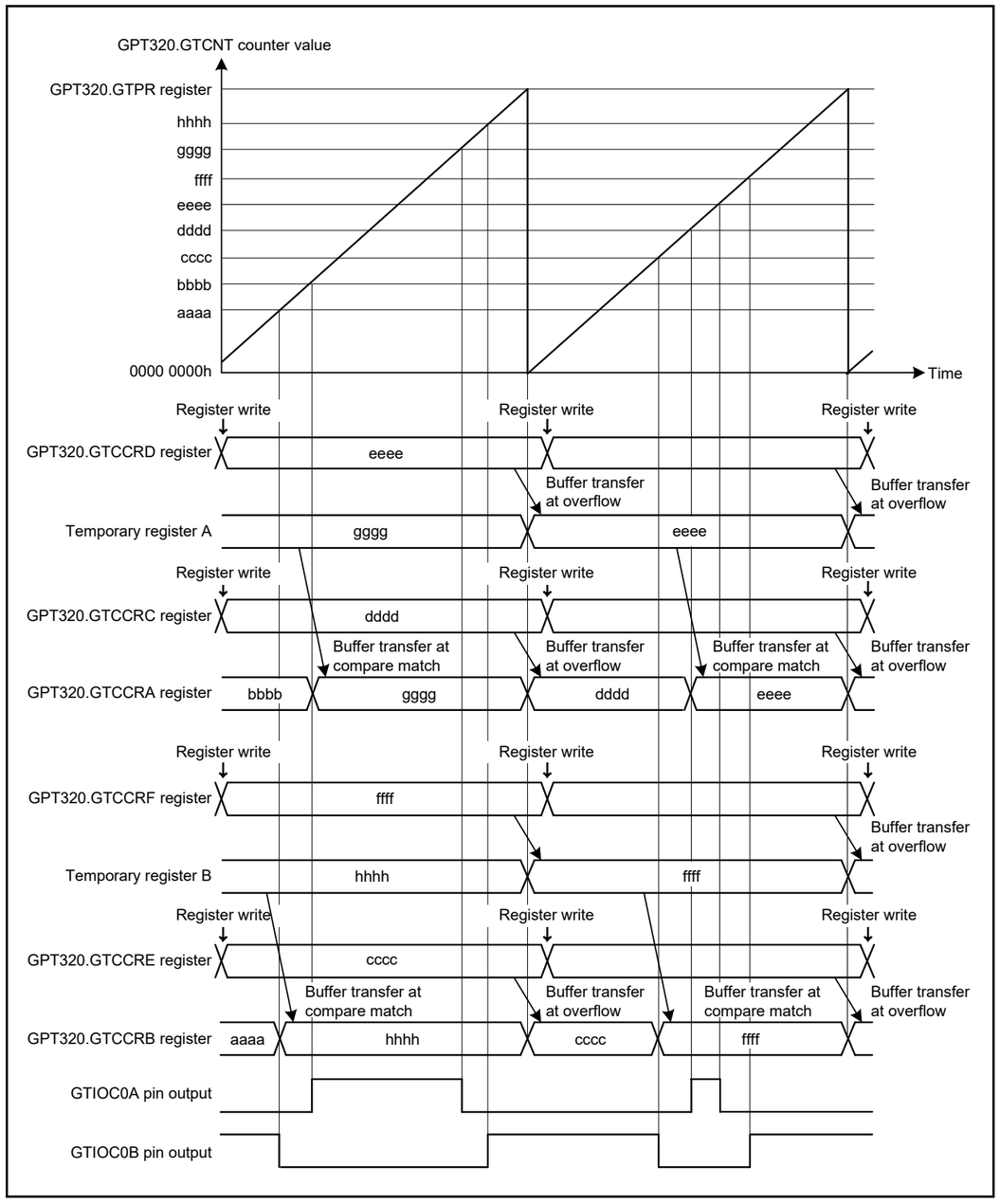


Figure 23.31 **Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end**

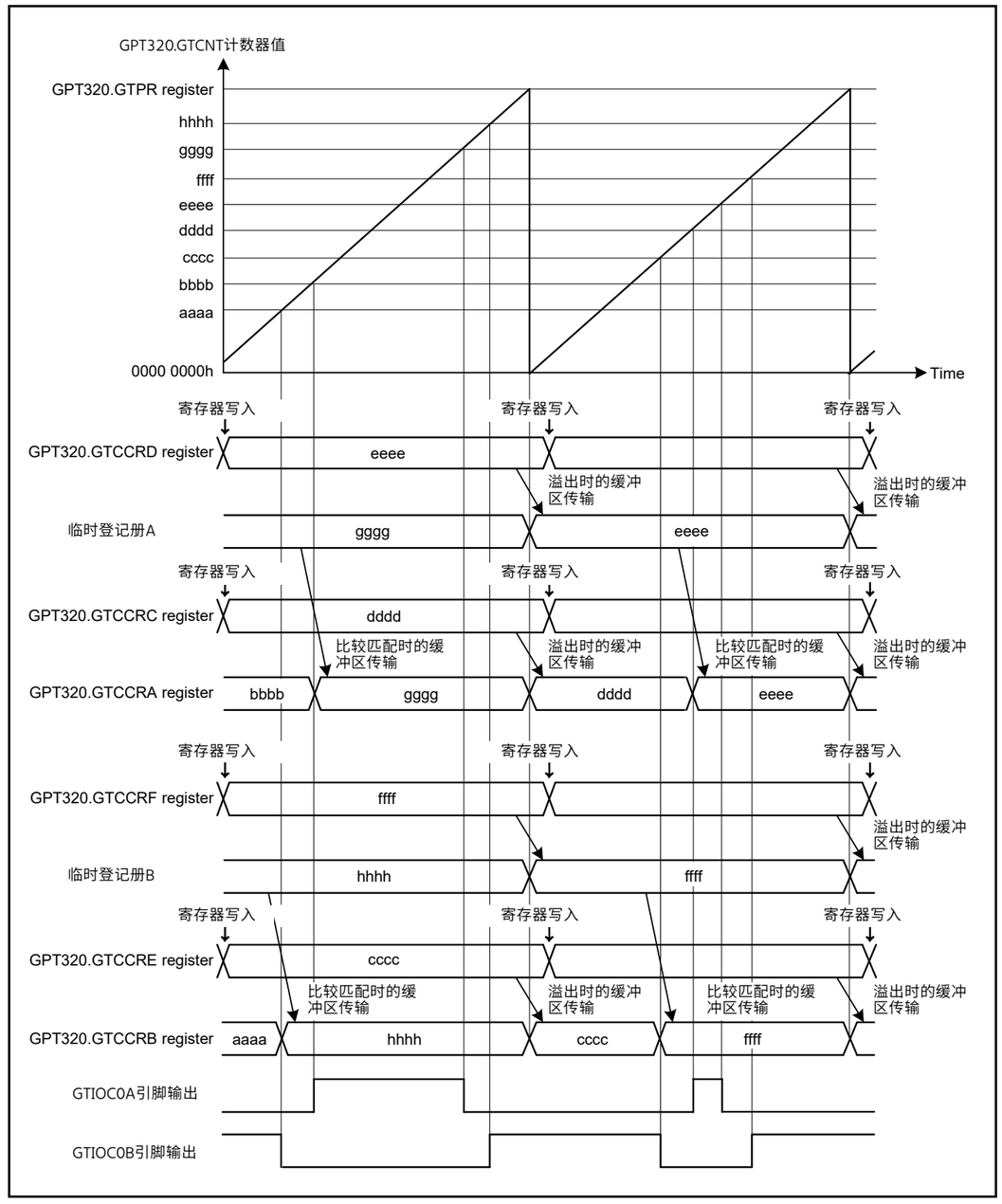


Figure 23.31 **具有递增计数、低输出的锯齿波单次脉冲模式操作示例 GTIOC0A引脚和GTIOC0B引脚在计数开始时的高电平输出，输出在GTCCRA切换 GTCCRB比较匹配，并在循环结束时保留输出**

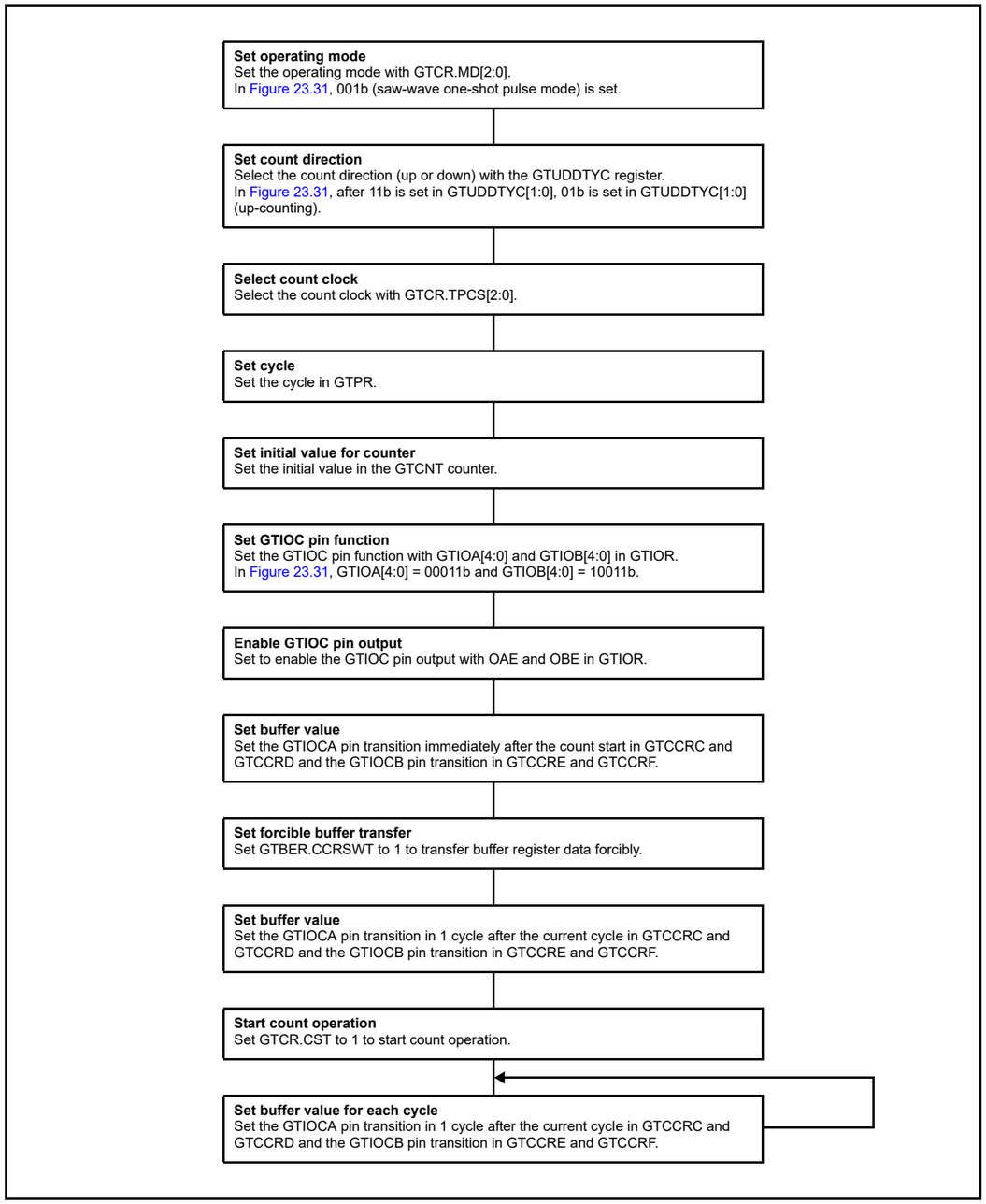


Figure 23.32 Example setting for saw-wave one-shot pulse mode

23.3.3.3 Triangle-wave PWM mode 1 (32-bit transfer at trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from

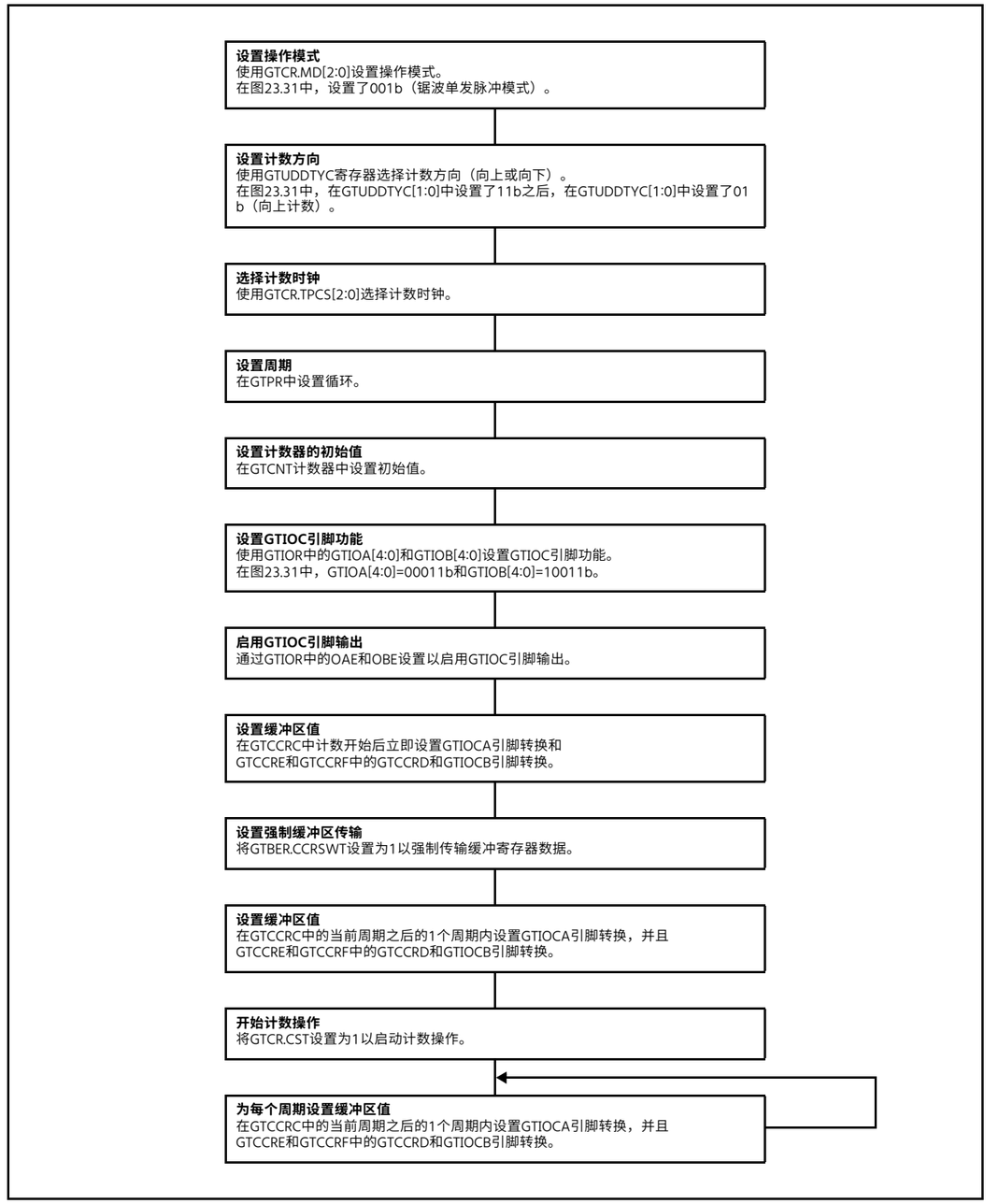


Figure 23.32 锯波单发脉冲模式设置示例

23.3.3.3 三角波PWM模式1（波谷32位传输）

三角波PWM模式1是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形将输出到GTIOCA或GTIOCB引脚。在槽中进行缓冲转移。引脚输出值可以从

low output, high output, or toggle output separately for a compare match and for the cycle end based on the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.33 shows an example of a triangle-wave PWM mode 1 operation, and Figure 23.34 shows an example setting for a triangle-wave PWM mode 1.

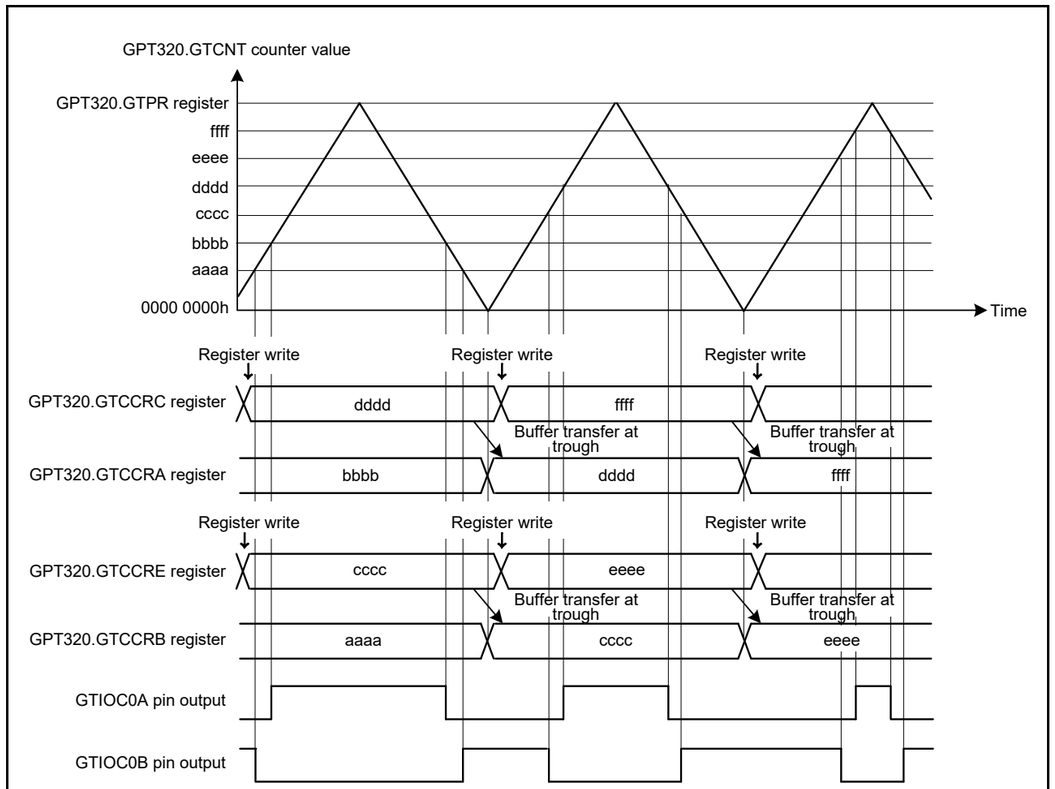


Figure 23.33 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, and output retained at cycle end

低输出、高输出或切换输出分别用于比较匹配和基于GTIOR设置的循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图23.33显示了三角波PWM模式1操作的示例，图23.34显示了三角波PWM模式1的示例设置。

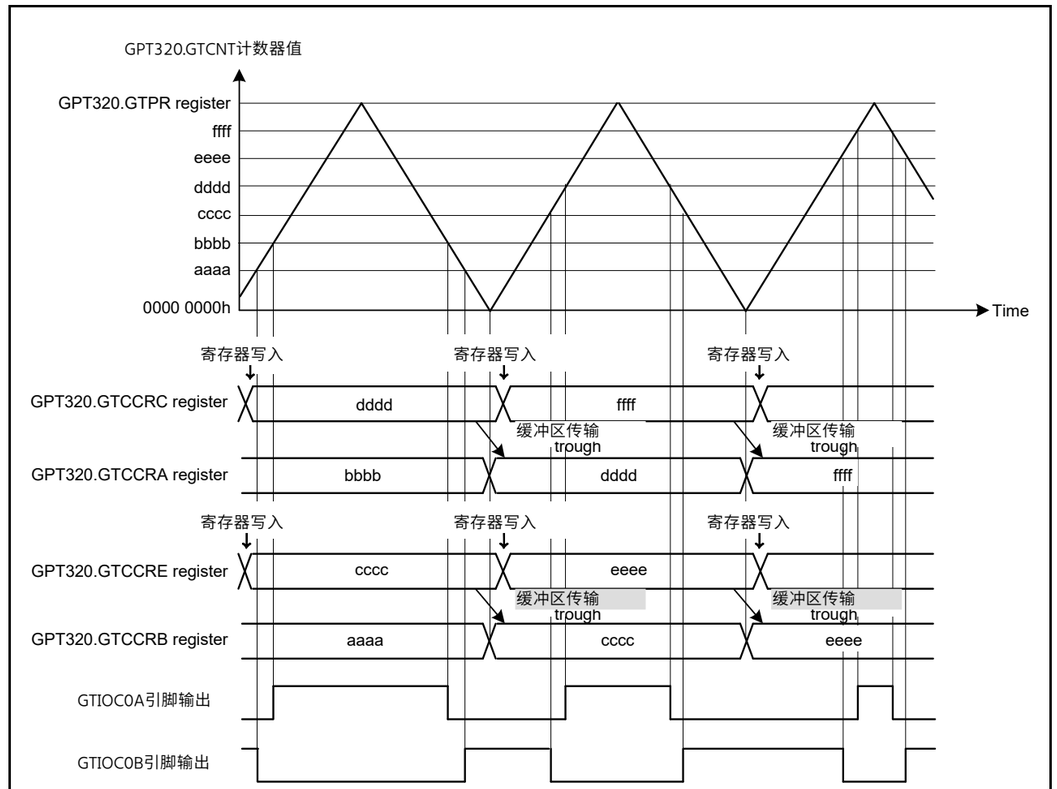


Figure 23.33 带缓冲操作的三角波PWM模式1操作示例，从GTIOC0A引脚和GTIOC0B引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB寄存器比较匹配，并在循环结束时保留输出

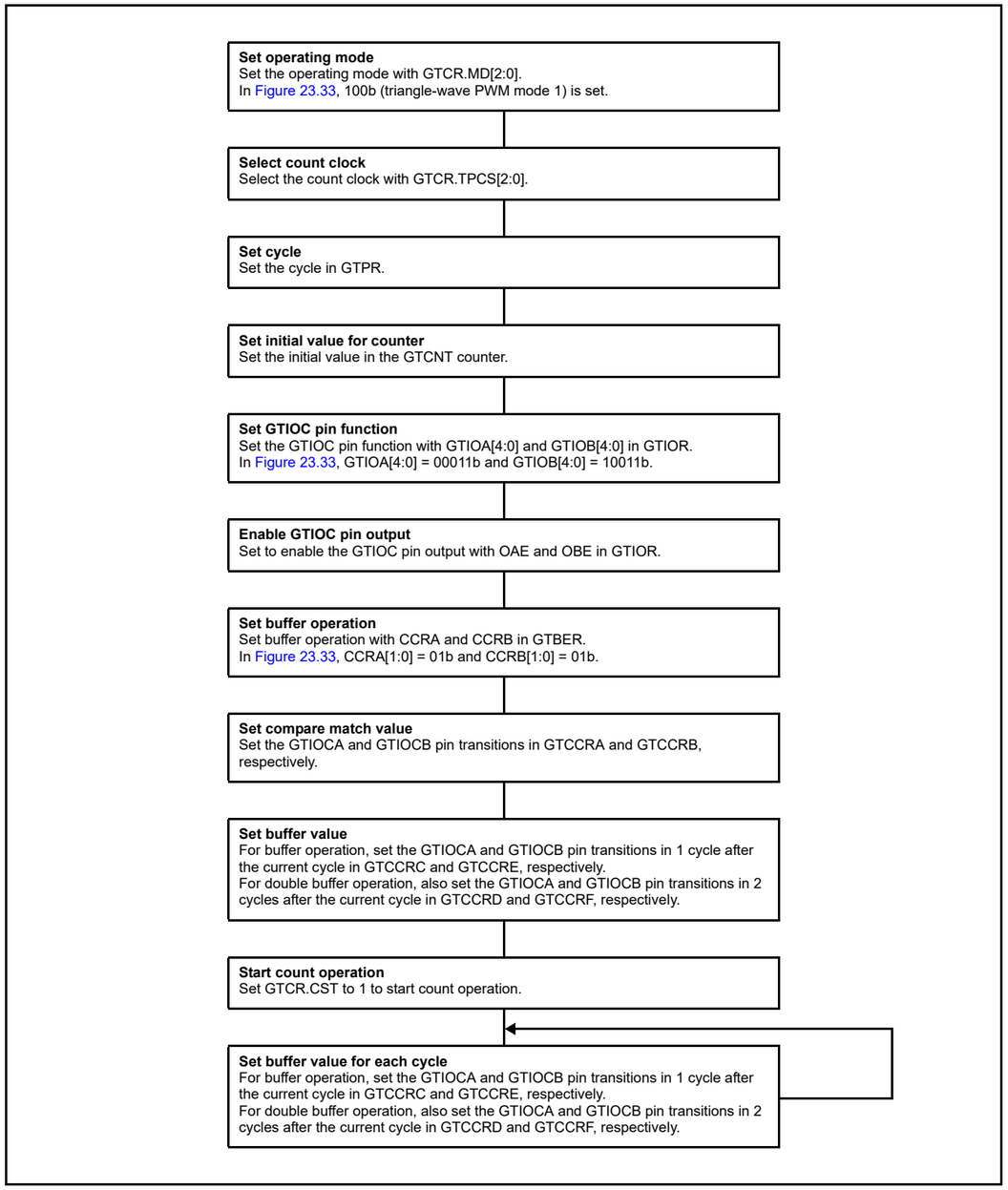


Figure 23.34 Example setting for triangle-wave PWM mode 1

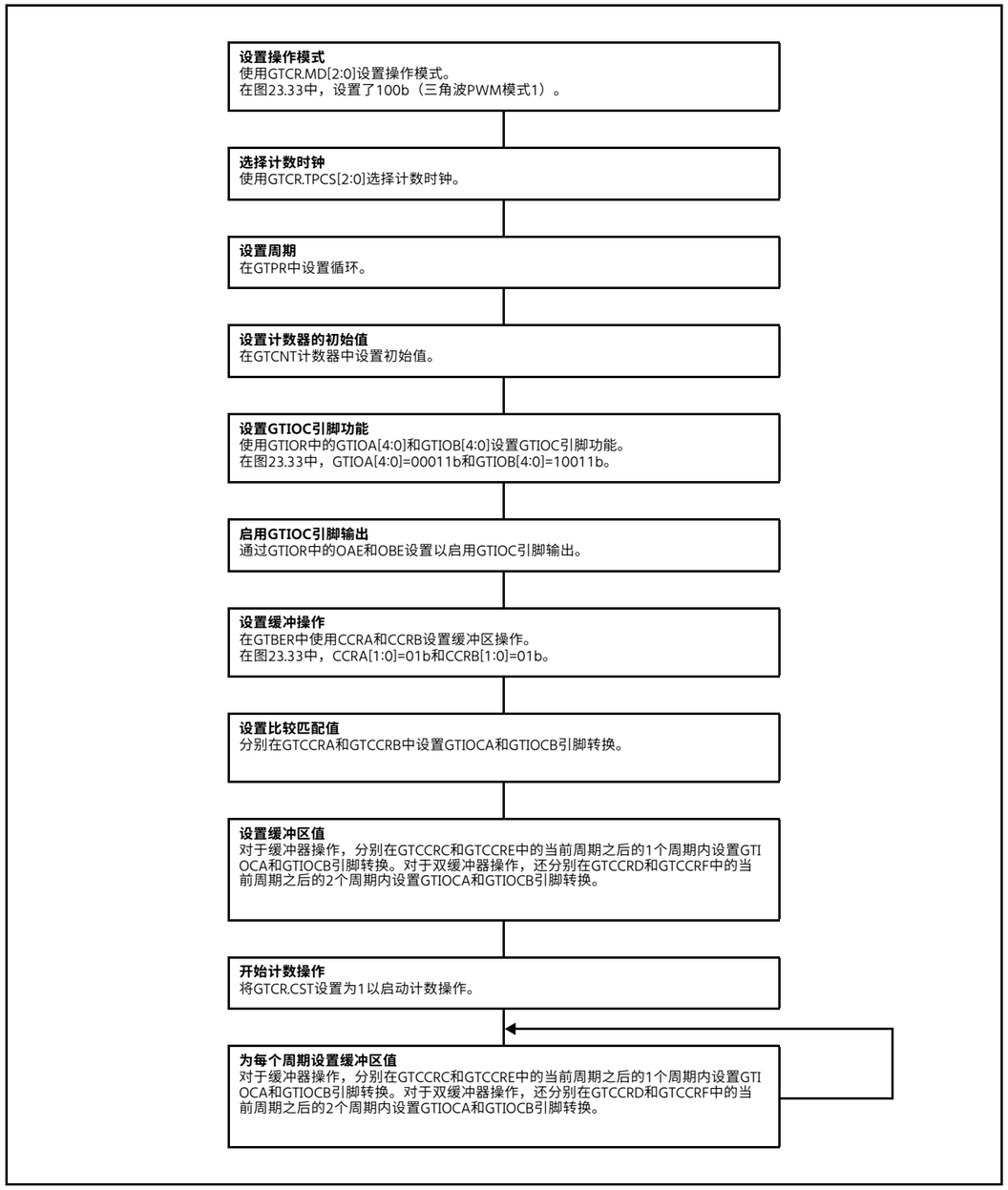


Figure 23.34 三角波PWM模式1的设置示例

23.3.3.4 Triangle-wave PWM mode 2 (32-bit transfer at crest and trough)

Similar to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end based on the GTIOR setting. By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.35 shows an example of triangle-wave PWM mode 2 operation, and Figure 23.36 shows an example setting for triangle-wave PWM mode 2.

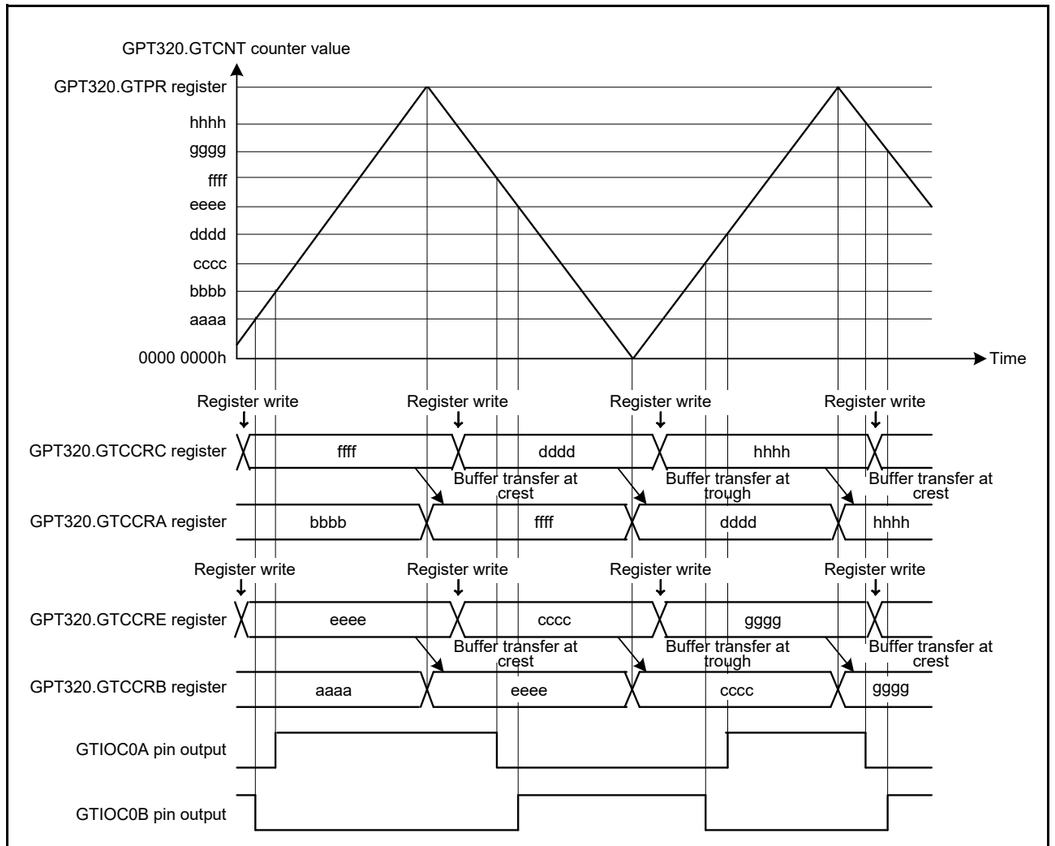


Figure 23.35 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end

23.3.3.4 三角波PWM模式2（波峰和波谷32位传输）

与三角波PWM模式1类似，在三角波PWM模式2中，周期在GTPR中设置。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形将输出到GTIOCA或GTIOCB引脚。缓冲转移在波峰和波谷进行。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图23.35显示了三角波PWM模式2操作的示例，图23.36显示了三角波PWM模式2的示例设置。

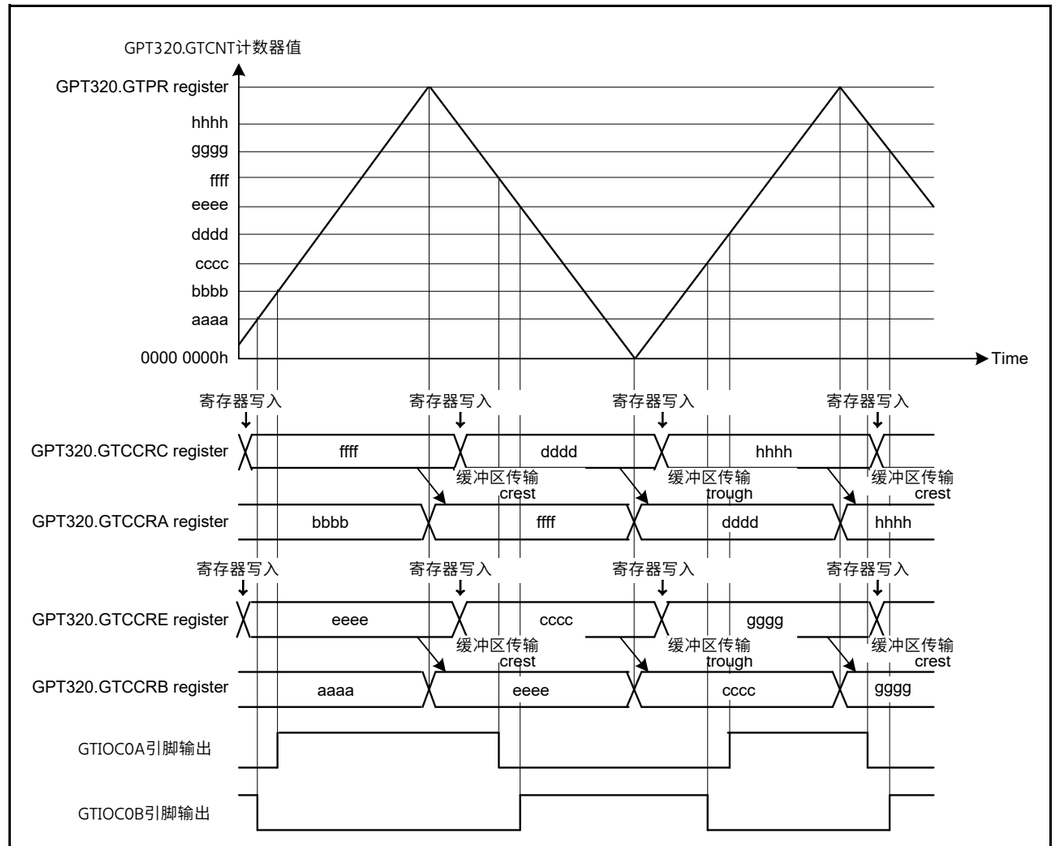


Figure 23.35 带缓冲操作的三角波PWM模式2操作示例，从GTIOC0A引脚和GTIOC0B引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB比较匹配，并在循环结束时保留输出

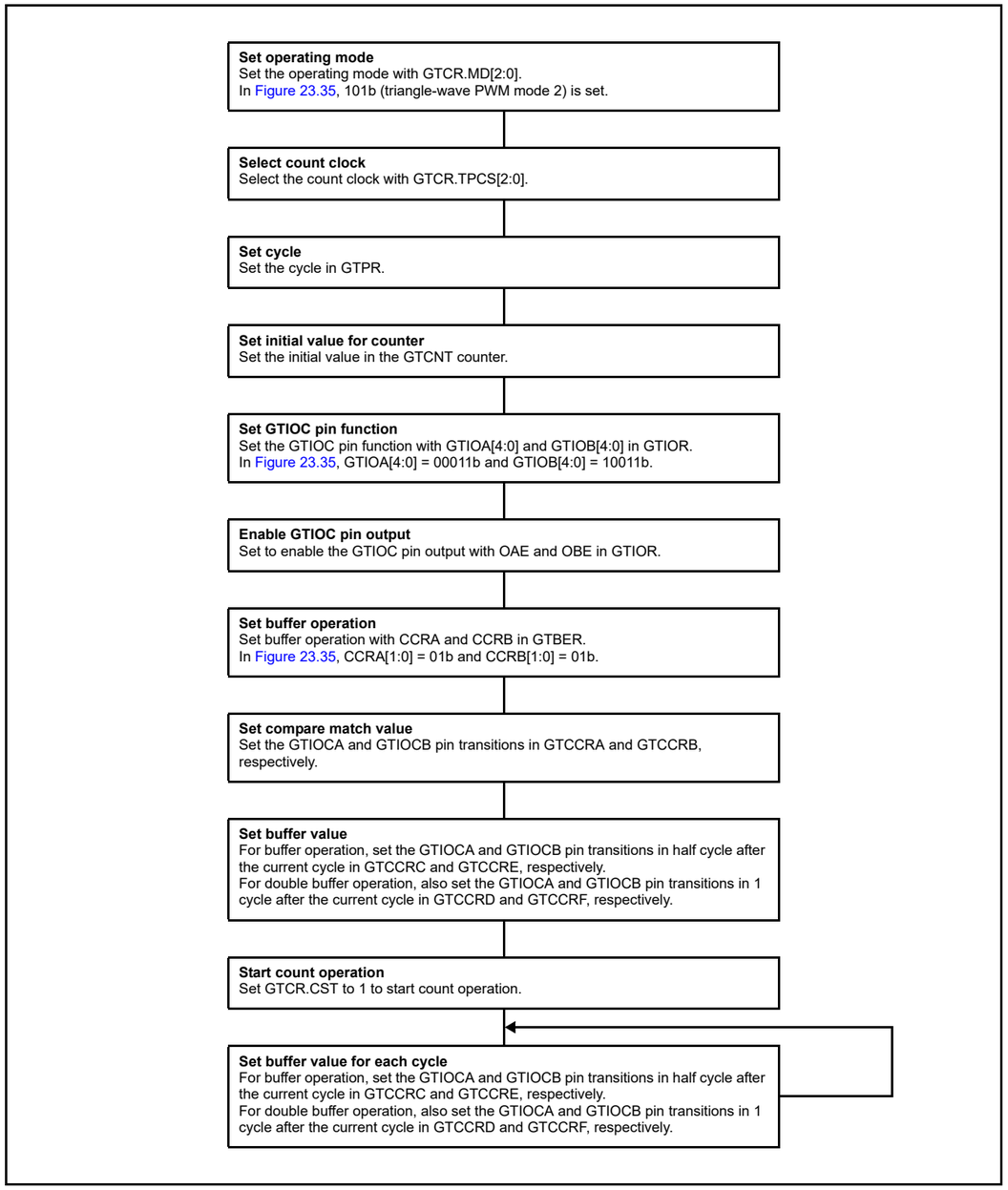


Figure 23.36 Example setting for triangle-wave PWM mode 2

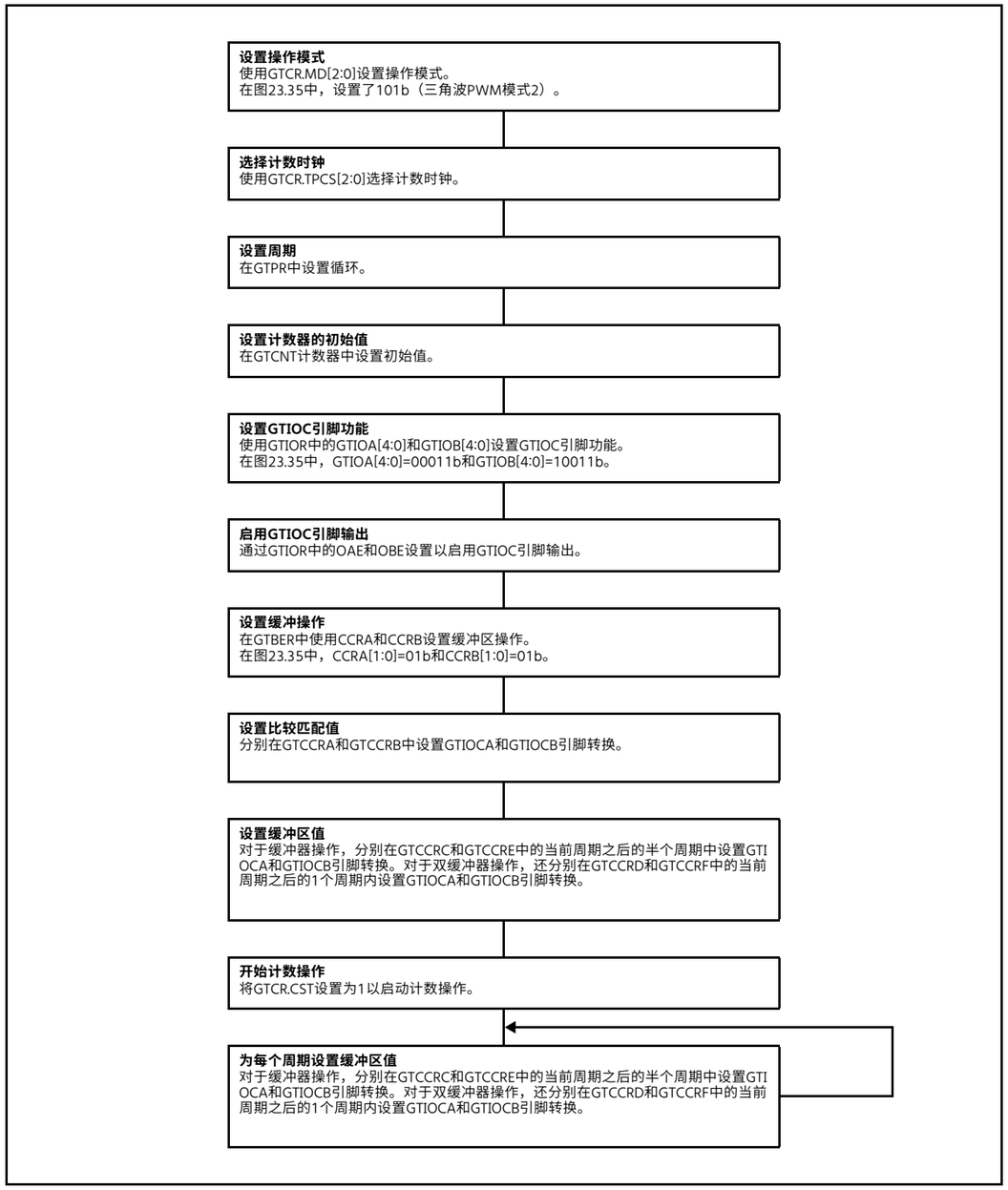


Figure 23.36 三角波PWM模式2的设置示例

23.3.3.5 Triangle-wave PWM mode 3 (64-bit transfer at trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting. By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.37 shows an example of triangle-wave PWM mode 3 operation, and Figure 23.38 shows an example setting for triangle-wave PWM mode 3.

23.3.3.5 三角波PWM模式3（波谷64位传输）

三角波PWM模式3是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，并且在GTCCRA或GTCCRB的比较匹配且缓冲器操作固定时，PWM波形输出到GTIOCA或GTIOCB引脚。三角波PWM模式3中的缓冲操作与通常的缓冲操作不同。缓冲区传输从以下位置执行：

- GTCCRC到GTCCRA在低谷
- GTCCRE到GTCCRB在低谷
- GTCCRD到谷底临时寄存器A
- GTCCRF到波谷临时寄存器B
- 顶部GTCCRA的临时注册A
- 在顶部的GTCCRB临时寄存器B。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图23.37显示了三角波PWM模式3操作的示例，图23.38显示了三角波PWM模式3的示例设置。

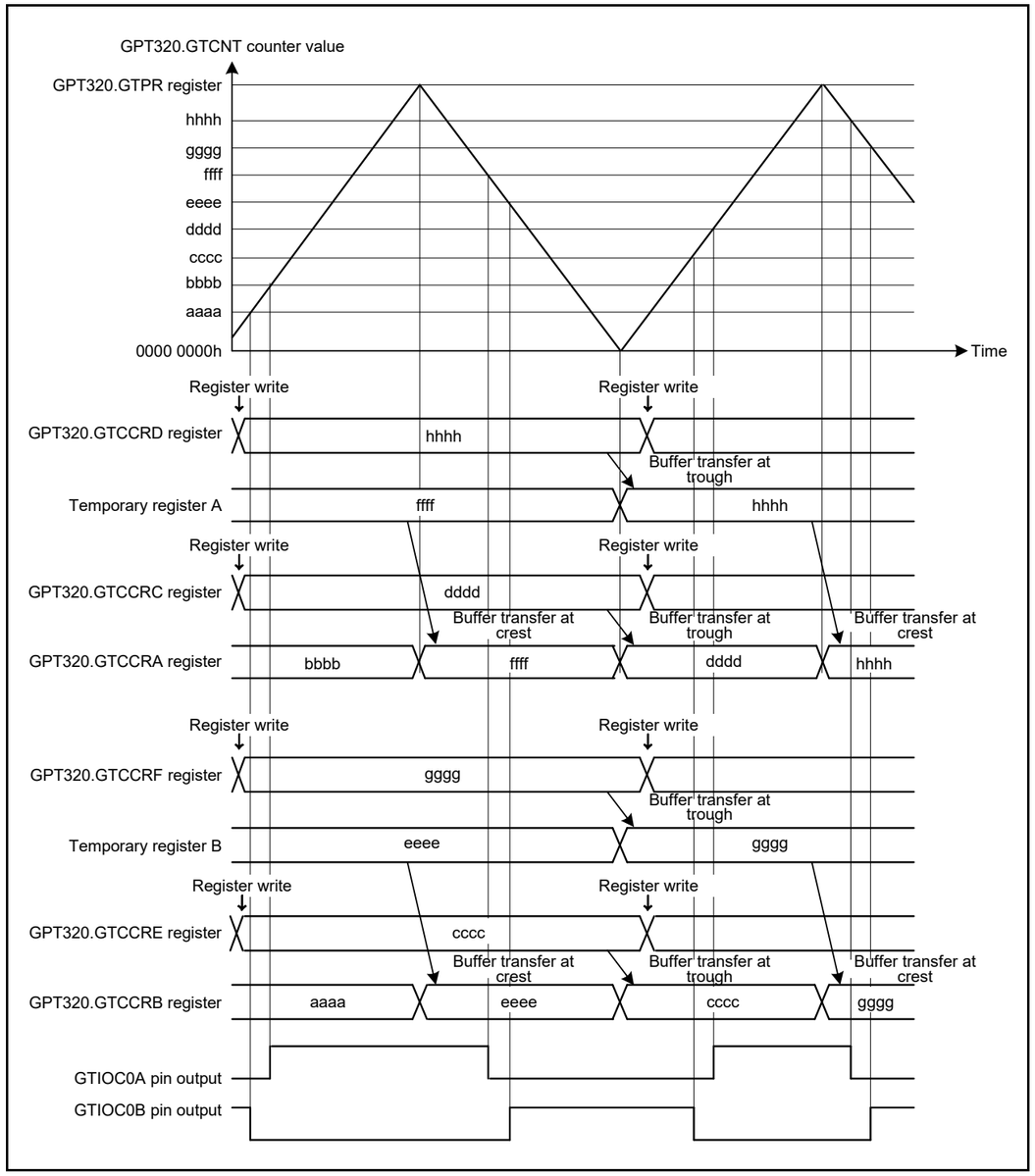


Figure 23.37 Example of triangle-wave PWM mode 3 operation with low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end

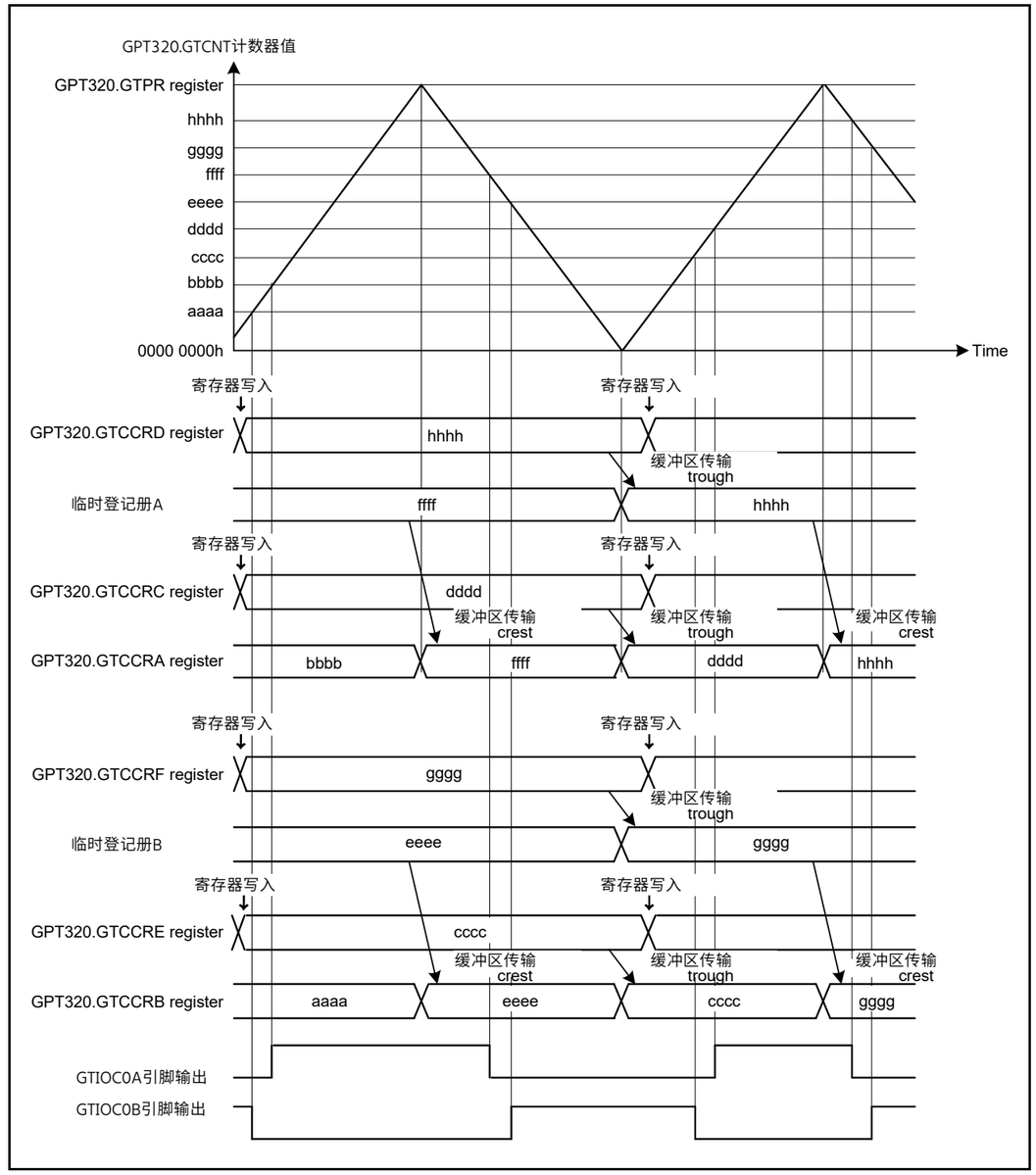


Figure 23.37 三角波PWM模式3操作示例，计数开始时GTIOC0A引脚输出低电平，GTIOC0B引脚输出高电平，在GTCCRAGTCCRB比较匹配时切换输出，在周期结束时保持输出

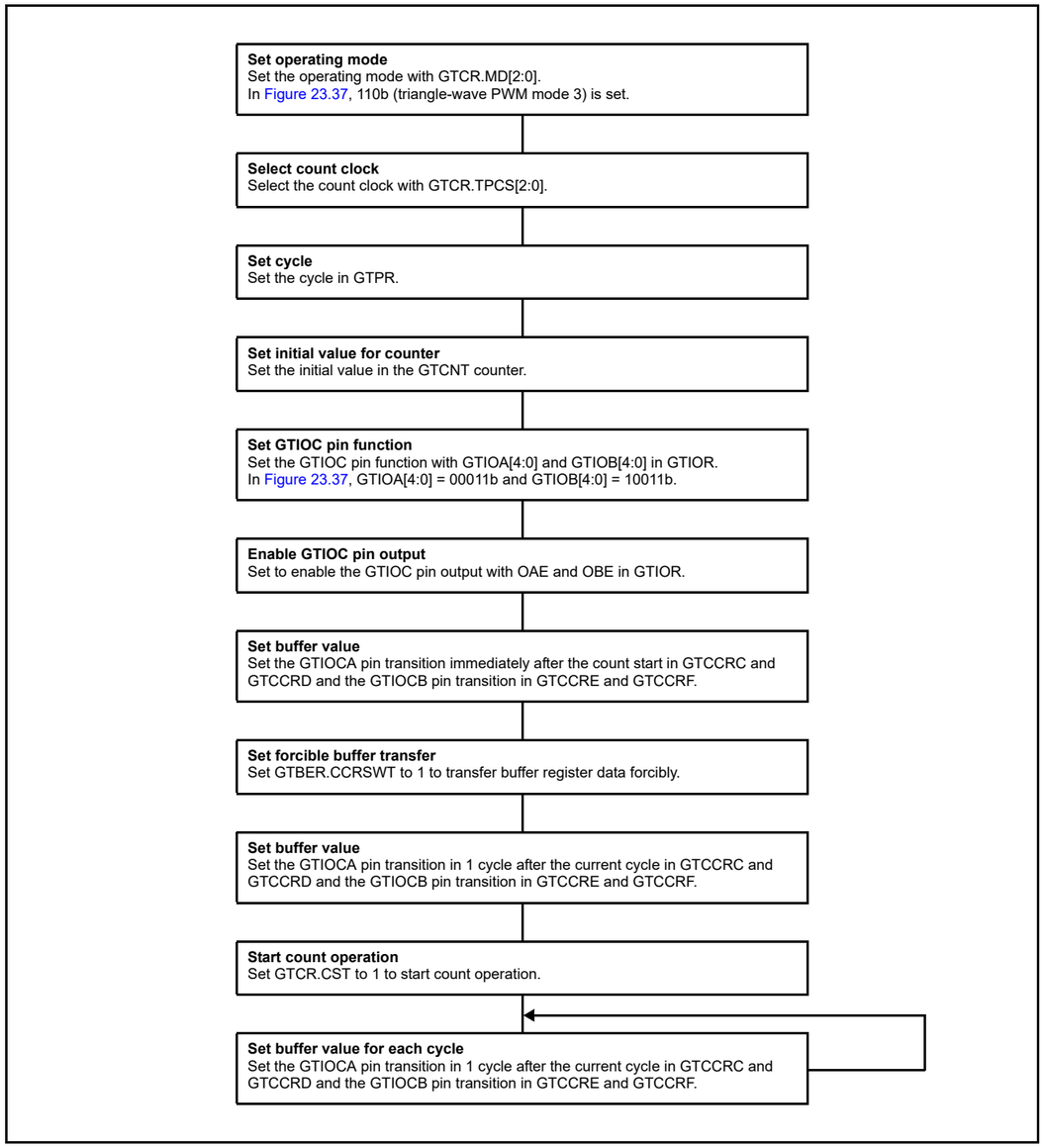


Figure 23.38 Example setting for triangle-wave PWM mode 3

23.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU value) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. The automatic dead time value setting to GTCCRB is performed at the next count clock cycle when registers that are used for calculating the automatic dead time value are updated.

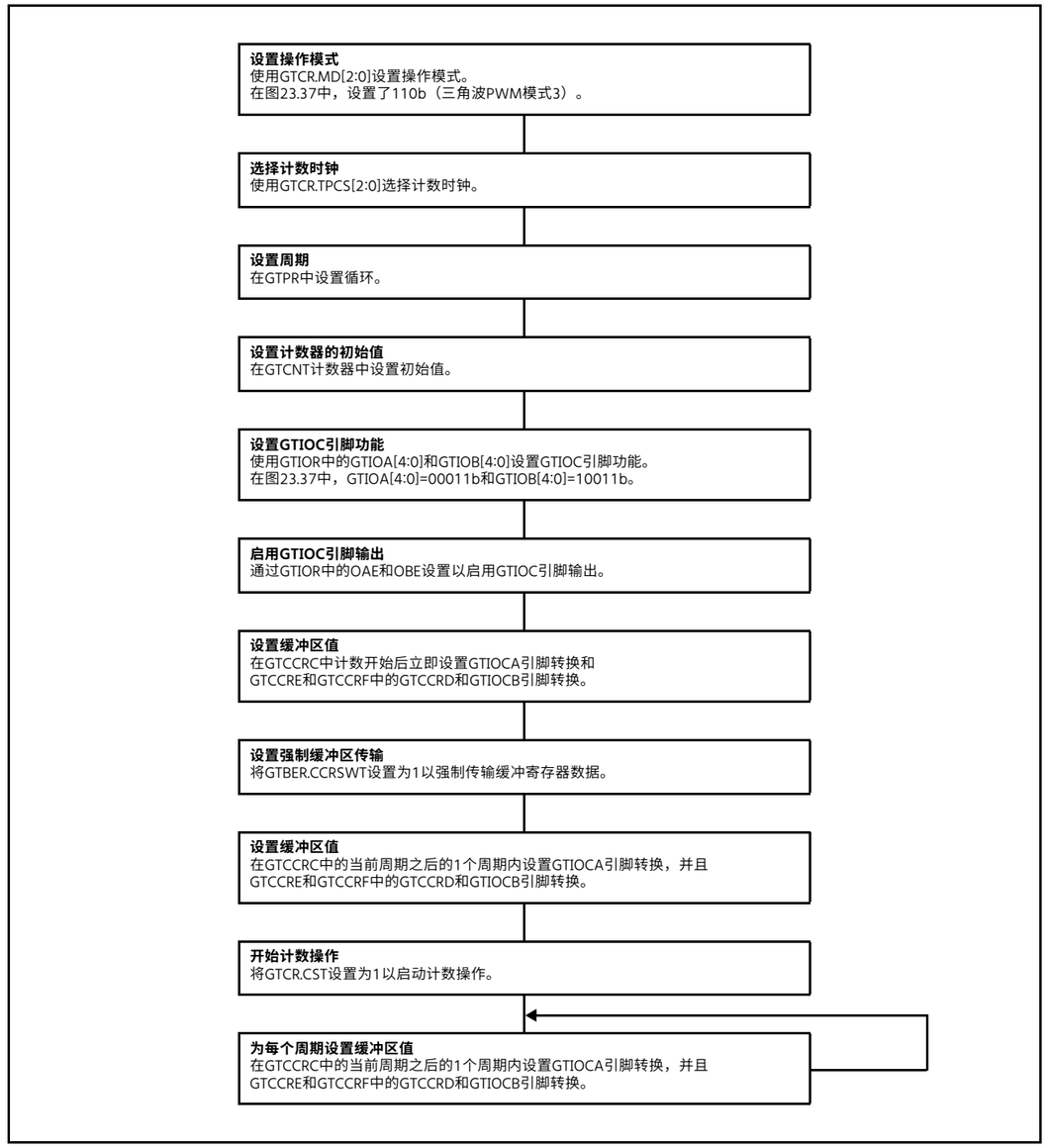


Figure 23.38 三角波PWM模式3的设置示例

23.3.4 自动死区时间设置功能

通过设置GTDTCR，可以自动将正波形的比较匹配值（GTCCRA值）和指定死区时间值（GTDVU值）得到的负波形与死区时间的比较匹配值设置为GTCCRB。自动死区时间设置功能可用于锯齿波一次性脉冲模式和所有三角PWM模式。

使用自动死区时间设置功能时，禁止写入GTCCRB。超出周期的死区时间设置也被禁止。自动死区时间设置的值可以从GTCCRB中读取。当用于计算自动死区时间值的寄存器被更新时，在下一个计数时钟周期执行GTCCRB的自动死区时间值设置。

Figure 23.39 to Figure 23.42 show examples of automatic dead time setting function operation. Figure 23.43 and Figure 23.44 show the setting examples.

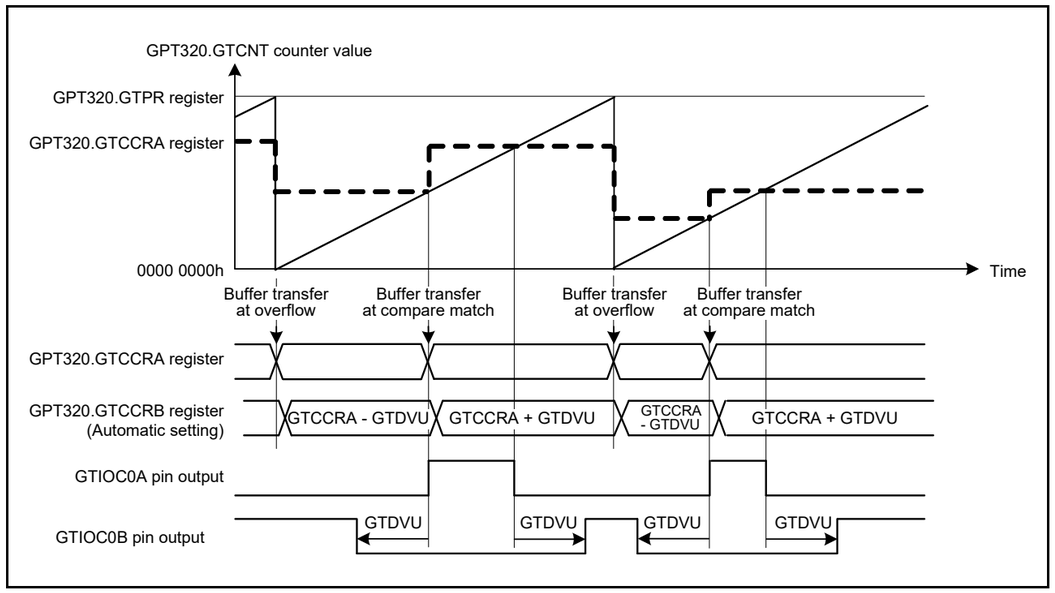


Figure 23.39 Example of automatic dead time setting function operation with saw-wave one-shot pulse mode, up-counting, and active-high

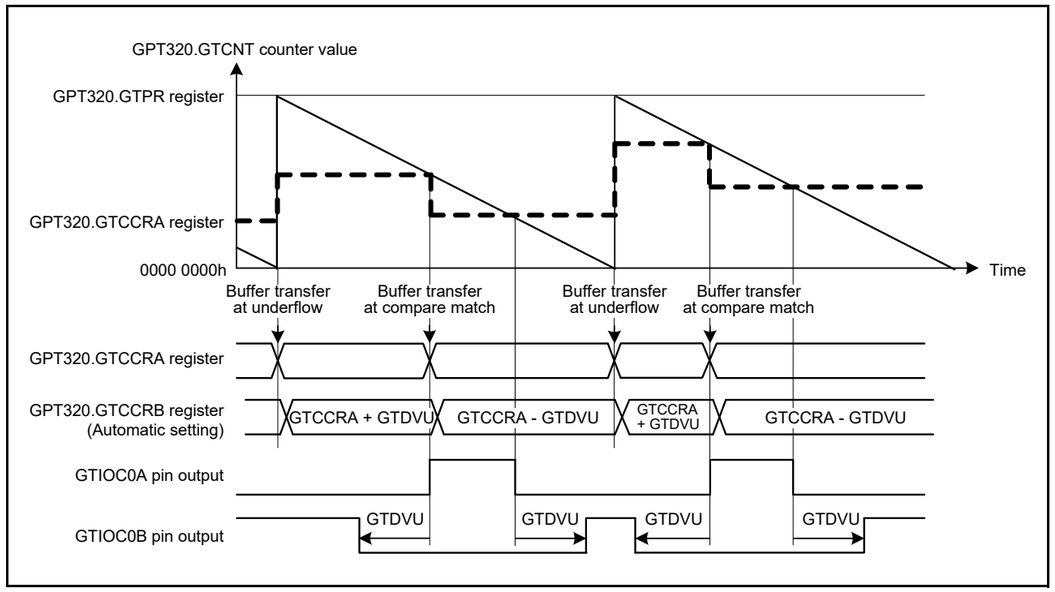


Figure 23.40 Example of automatic dead time setting function operation with saw-wave one-shot pulse mode, down-counting, and active-high

图23.39至图23.42显示了自动死区时间设置功能操作的示例。图23.43和图23.44显示了设置示例。

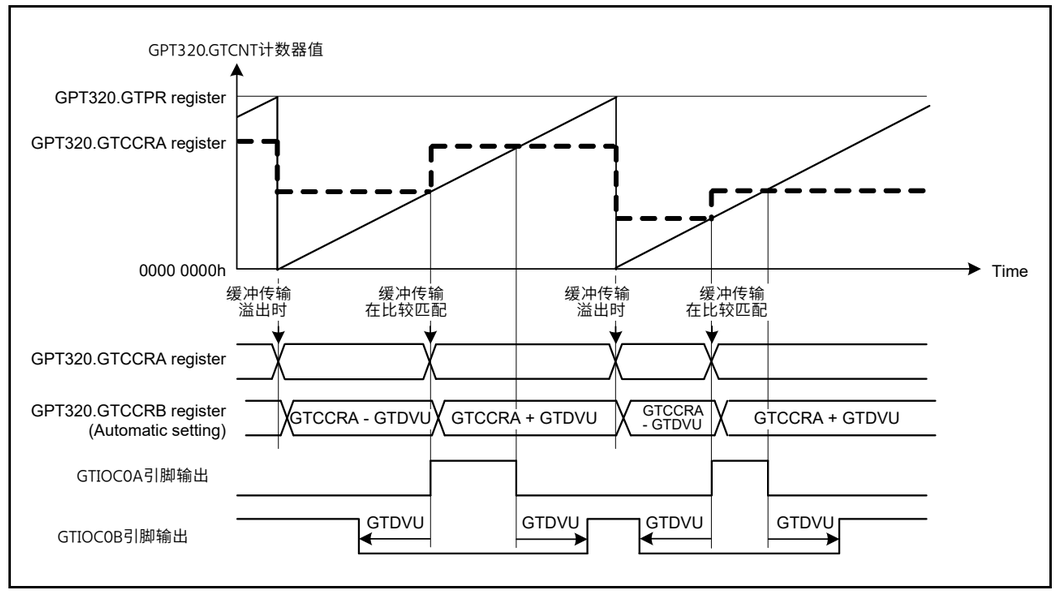


Figure 23.39 使用锯齿波单发脉冲模式、递增计数和高电平有效的自动死区时间设置功能操作示例

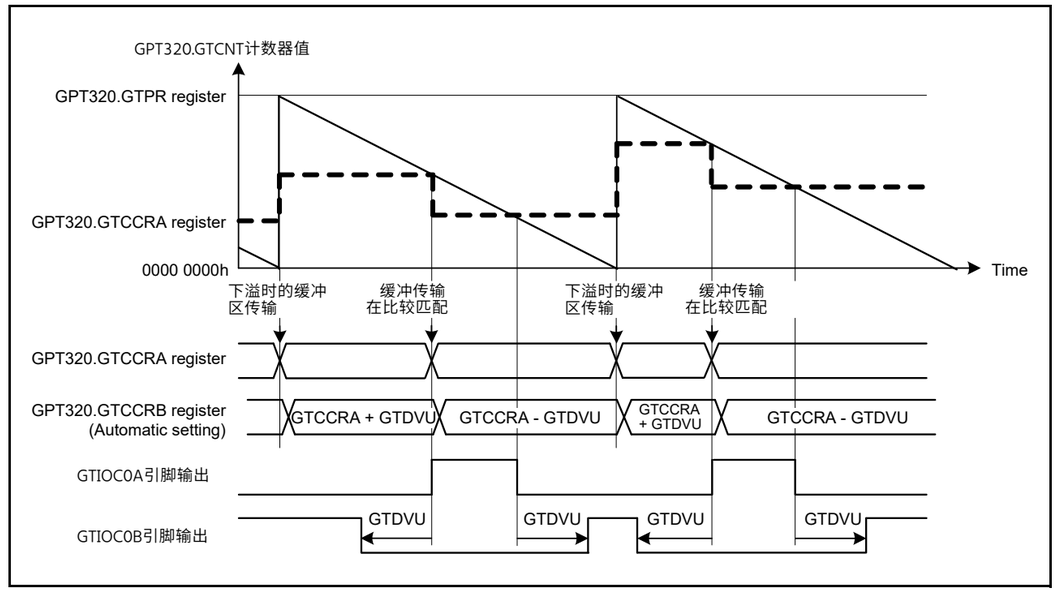


Figure 23.40 使用锯齿波一次性脉冲模式、递减计数和高电平有效的自动死区时间设置功能操作示例

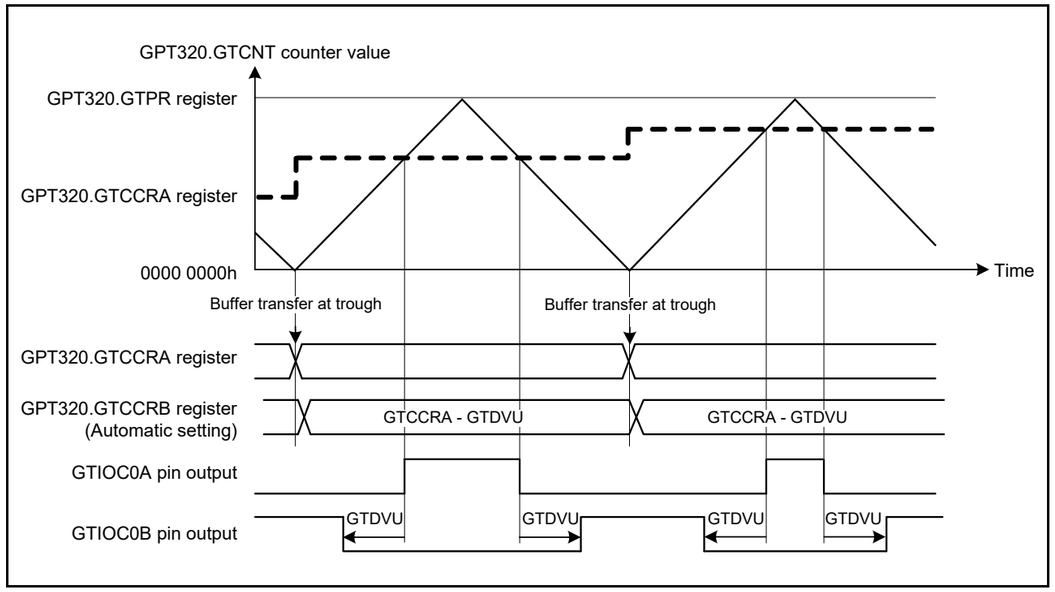


Figure 23.41 Example of automatic compare-match value setting function with dead time with triangle-wave PWM mode 1, and active-high

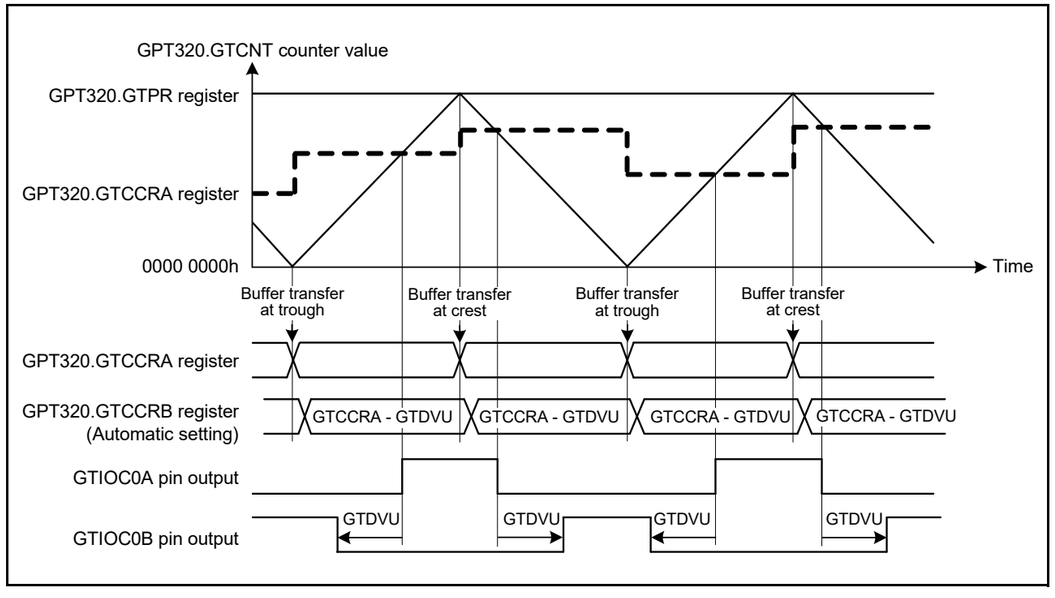


Figure 23.42 Example of automatic compare-match value setting function with dead time with triangle-wave PWM mode 2 or 3, and active-high

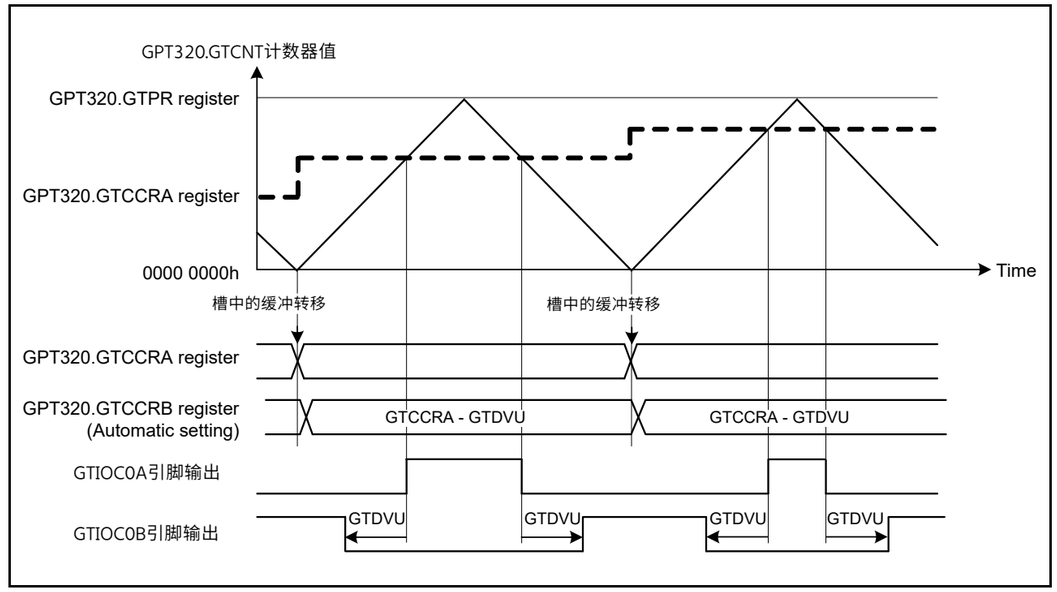


Figure 23.41 三角波带死区时间的自动比较匹配值设置功能示例 PWM模式1，高电平有效

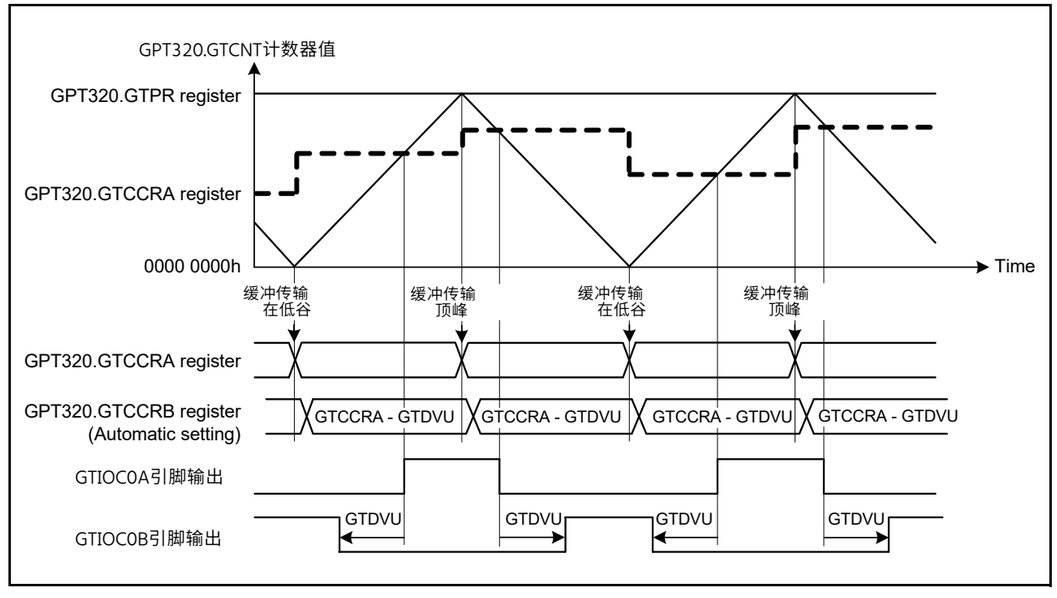


Figure 23.42 三角波带死区时间的自动比较匹配值设置功能示例 PWM模式2或3，高电平有效

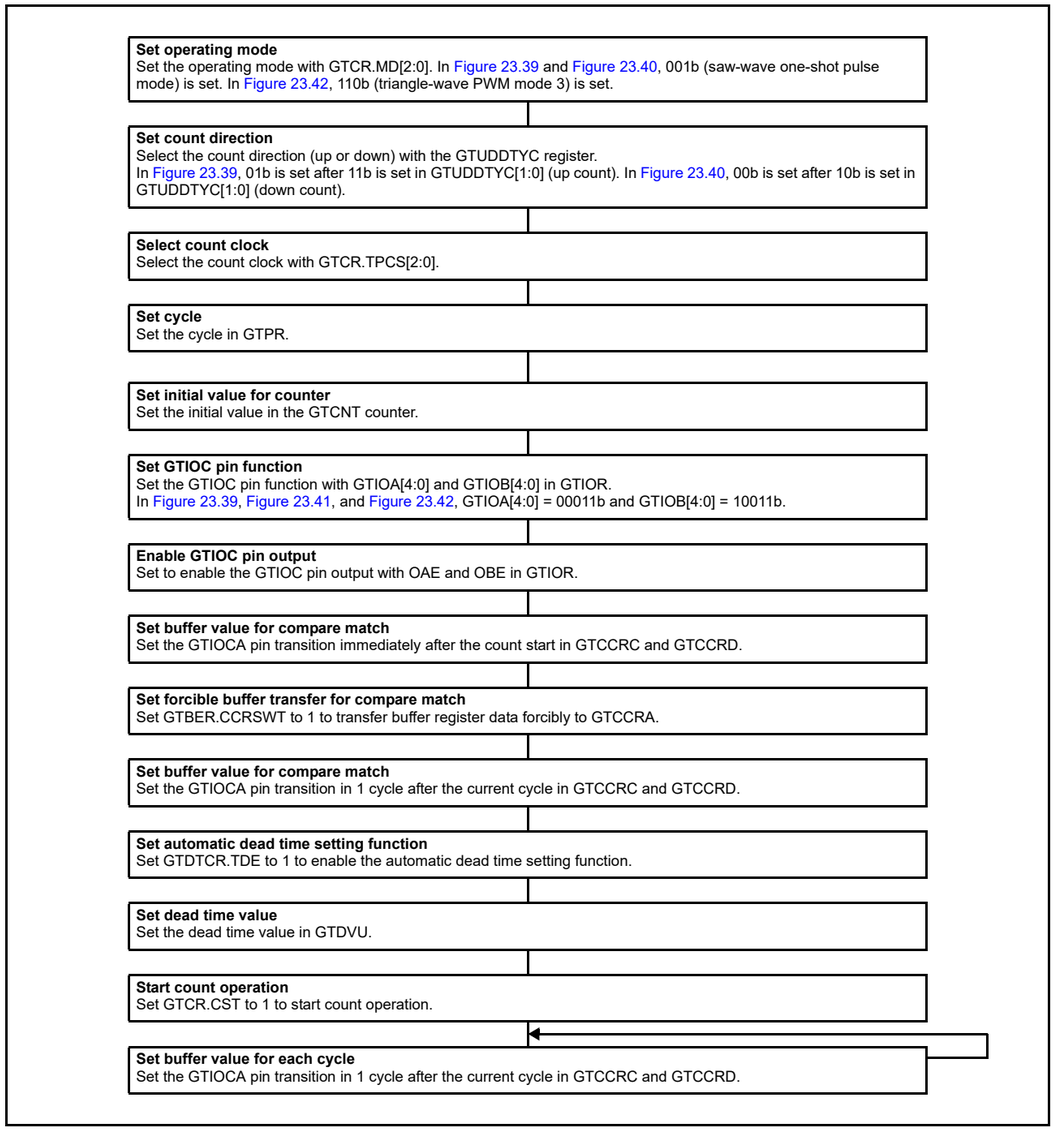


Figure 23.43 Example setting for automatic dead time setting function with saw-wave one-shot pulse mode, and triangle-wave PWM mode 3

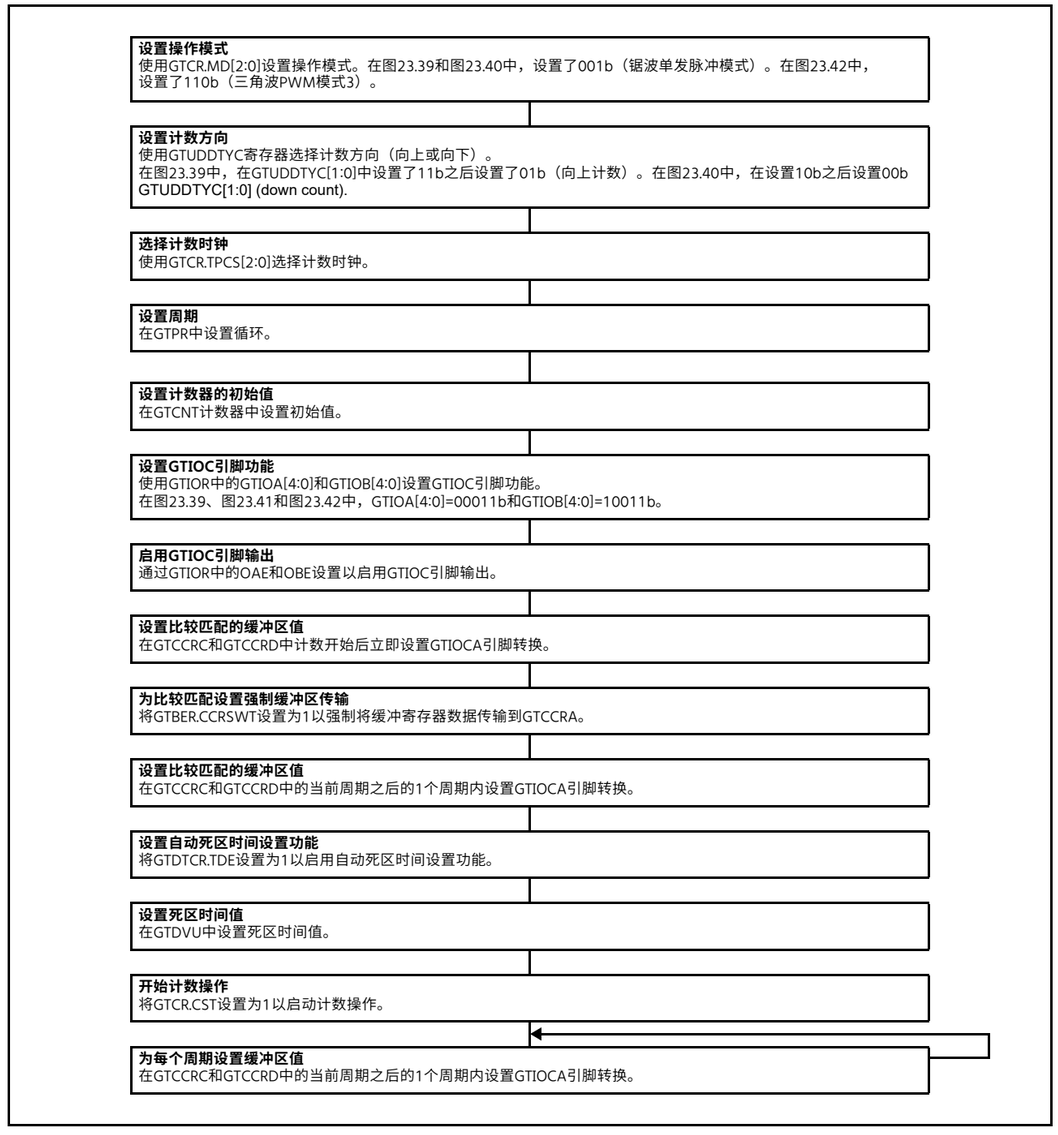


Figure 23.43 锯齿波一次性脉冲模式和三角波PWM模式的自动死区时间设置功能示例3

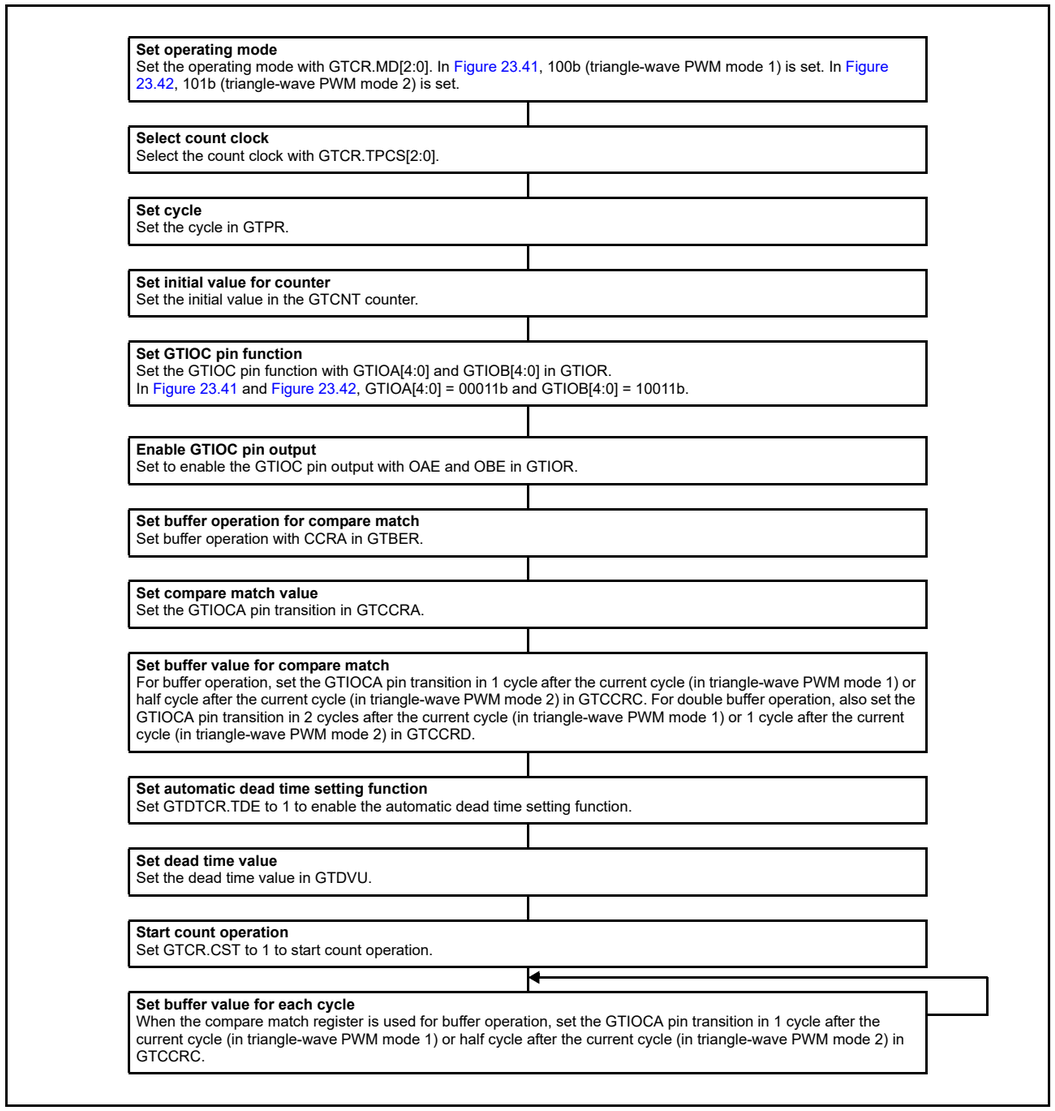


Figure 23.44 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2

23.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation is stopped and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction changes at an overflow or an underflow. If the UDF bit is set to 1 while the count operation is stopped the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation is stopped

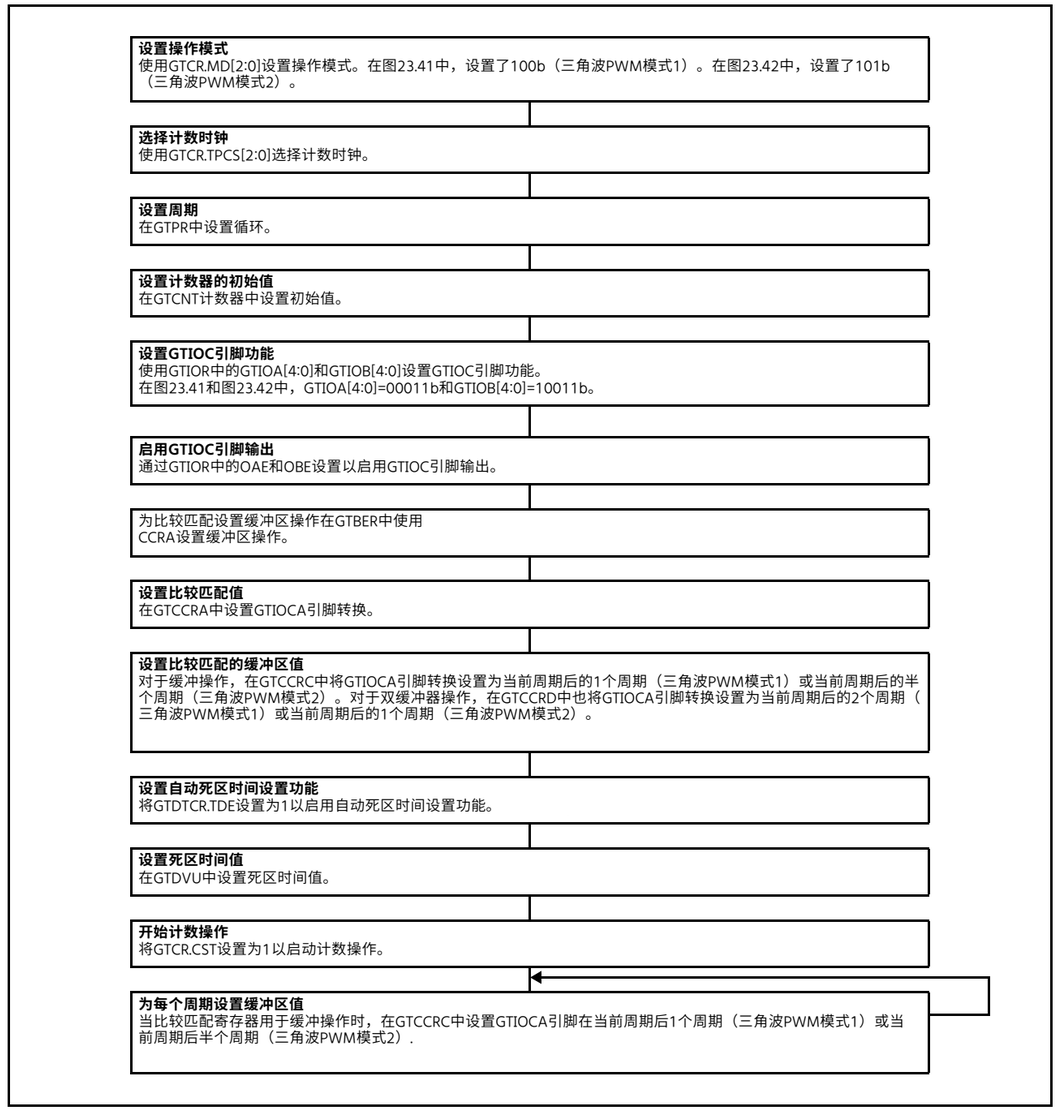


Figure 23.44 三角波PWM模式1或2中自动死区时间设置功能的设置示例

23.3.5 计数方向改变功能

GTCNT计数器的计数方向可以通过修改GTUDDTYC中的UD位来改变。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC中的UD位，则计数方向会在溢出（在向上计数期间修改时）或下溢（在向下计数期间修改时）改变。如果在计数操作停止且GTUDDTYC.UDF位为0时修改GTUDDTYC.UD位，则

GTUDDTYC.UD位修改不会反映在计数开始时，计数方向会在上溢或下溢时改变。如果在计数操作停止时UDF位设置为1，则此时GTUDDTYC.UD位的值将反映在计数开始时。

在三角波模式下，即使在计数操作期间修改GTUDDTYC中的UD位，计数方向也不会改变。同样，即使在计数操作停止时修改了GTUDDTYC.UD位

and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value before the start of down-counting is reflected during down-counting.

Figure 23.45 shows an example of count direction changing function operation.

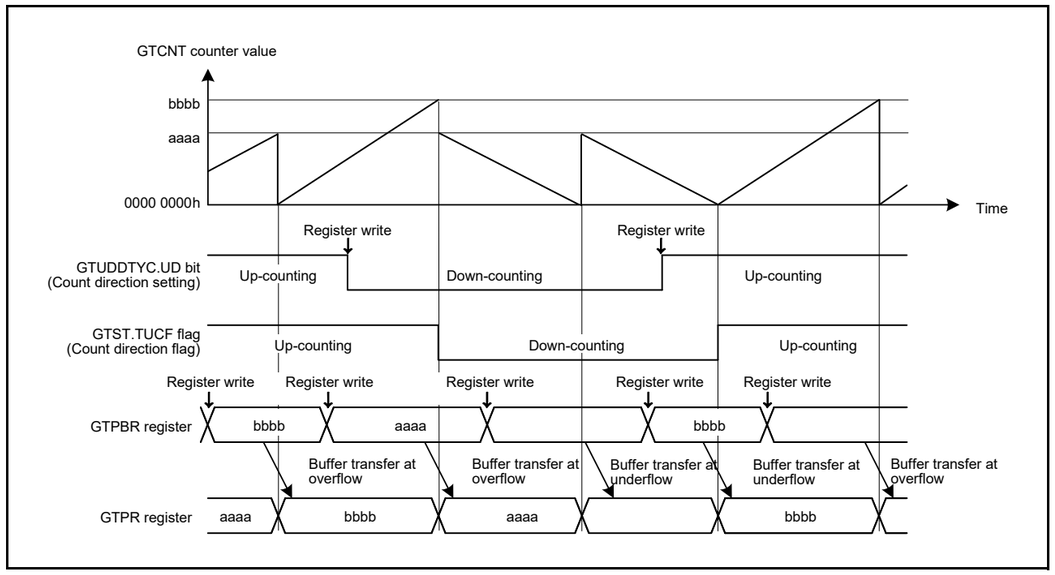


Figure 23.45 Example of a count direction changing function operation during buffer operation

23.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCA pin and the GTIOCB pin is set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is set to 1 while the count operation is stopped, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an underflow.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0% or 100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag

并且GTUDDTYC.UDF位为0，GTUDDTYC.UD位的值不反映到计数操作中。如果在计数操作停止时将GTUDDTYC.UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

如果在锯齿波计数操作期间计数方向发生变化，则加计数开始后的GTPR值反映在加计数期间的计数周期中，减计数开始前的GTPR值反映在减计数期间.

图23.45显示了计数方向改变功能操作的示例。

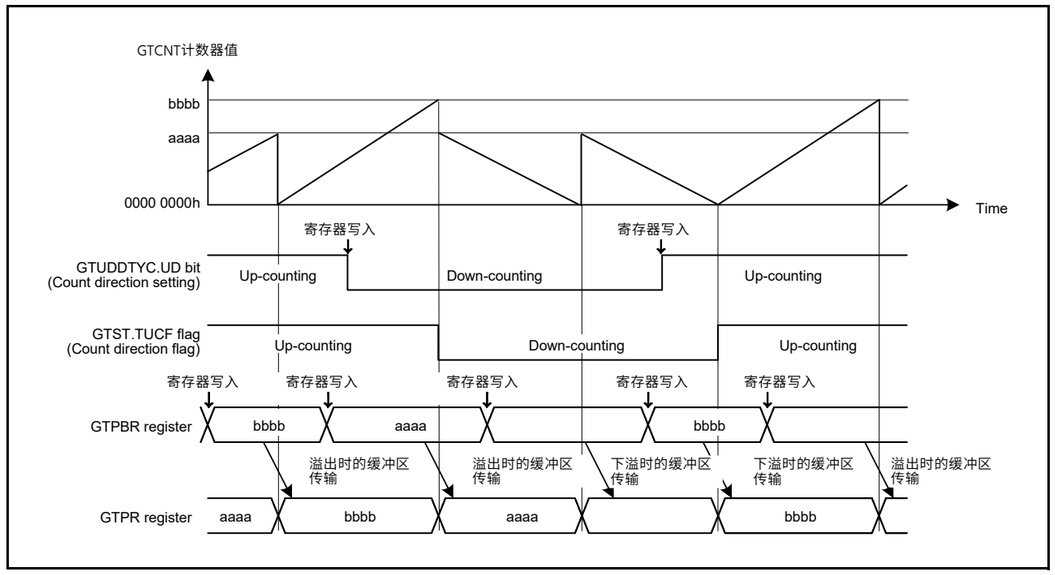


Figure 23.45 缓冲操作期间的计数方向改变功能操作示例

23.3.6 输出占空比0%和100%的功能

GTIOCA引脚和GTIOCB引脚的输出占空比通过更改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位设置为0%或100%。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映在溢出（在向上计数期间修改时）或下溢（在向下期间修改时-数数）。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在上溢或下溢时发生变化。如果在计数操作停止时GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位设置为1，则

GTUDDTYC.OADTY位或当时的GTUDDTYC.OBDTY位值反映在计数开始时。

在三角波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置会反映在下溢处。

如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在下溢时发生变化。如果GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位在计数操作停止且GTUDDTYC.OADTYF或

GTUDDTYC.OBDTYF位为1，输出占空比修改反映在计数开始。

在执行0%或100%占空比操作时，GPT在内部继续：

- 执行比较匹配操作
- 设置比较匹配标志

- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCA pin at cycle end is determined by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 23.6 shows the values of GTIOCA/GTIOCB pin output at cycle end.

Table 23.6 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	—	0	0	0	0
10 (high output at cycle end)	—	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 23.46 shows an example of output duty 0% and 100% function.

- 输出中断
- 执行缓冲操作。

当控制从0%或100%占空比设置更改为比较匹配时，循环结束时GTIOCA引脚的输出值由GTIOR.GTIOA[3:2]和GTUDDTYC.OADTYR确定。周期结束时GTIOCB引脚的输出值由GTIOR.GTIOB[3:2]和GTUDDTYC.OBDTYR决定。

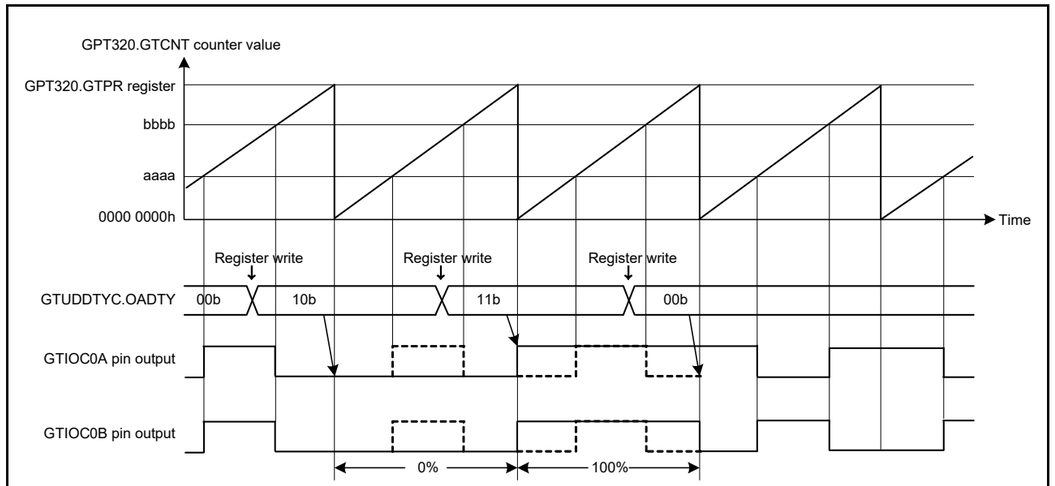
当GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为01b时，输出引脚在周期结束时输出低电平。什么时候GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为10b，输出引脚在周期结束时输出高电平。

GTUDDTYC.OADTYR选择在循环结束时作为输出保持切换的对象的值，当GTIOR.GTIOm[3:2]设置为00b（输出在循环结束时保留）或GTIOR.GTIOm[3:2]设置为11b（输出在循环结束时切换）。表23.6显示了循环结束时GTIOCAGTIOCB引脚输出的值。

Table 23.6 释放0%或100%占空比设置后的输出值(m=A B)

GTIOR.GTIOm[3:2]	比较被0%或100%占空比设置屏蔽的循环结束时的匹配值	GTUDDTYC.OmDTYR 在占空比0%设置		GTUDDTYC.OmDTYR 占空比100%设置	
		0	1	0	1
00（循环结束时保留输出）	0	0	0	1	0
	1	0	1	1	1
01（循环结束时输出低）	—	0	0	0	0
10（循环结束时的高输出）	—	1	1	1	1
11（循环结束时切换输出）	0	1	1	0	1
	1	1	0	0	0

图23.46显示了输出占空比0%和100%功能的示例。



[Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits: 00011b
Initial low output, output toggled at compare match, output retained at cycle end

GPT320.GTUDDTYC.OADTYR bit: 0b
Applied the value of duty 0% or 100% output to GTIOA[3:2] bits function after 0% or 100% duty setting is released

GPT320.GTIOR.GTIOB[4:0] bits: 00011b
Initial low output, output toggled at compare match, output retained at cycle end

GPT320.GTUDDTYC.OBDTYR bit: 1
Applied the value of masked compare match output to GTIOB[3:2] bits function after 0% or 100% duty setting is released

Figure 23.46 Example of output duty 0% and 100% function

23.3.7 Hardware Count Start/Count Stop and Clear Operation

The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCA/GTIOCB pin input.

23.3.7.1 Hardware start operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 23.47 shows an example of a count start operation by a hardware source. Figure 23.48 shows the setting example.

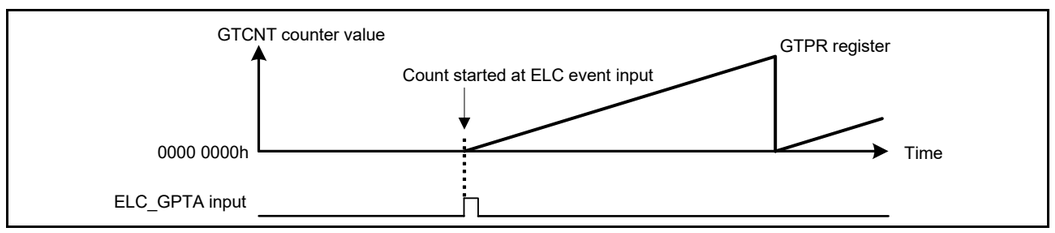
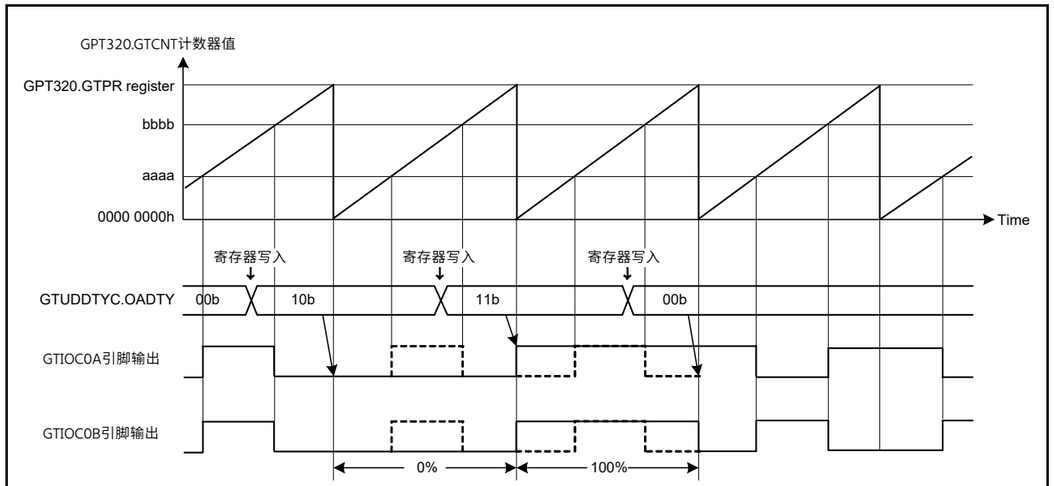


Figure 23.47 Example of count start operation by a hardware source started, at the input of the signal from the ELC_GPTA event



[Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits: 00011b初始低输出，在比较匹配时切换输出，在循环结束时保持输出

GPT320.GTUDDTYC.OADTYR bit: 0b
在释放0%或100%占空比设置后，将占空比0%或100%输出的值应用于GTIOA[3:2]位功能

GPT320.GTIOR.GTIOB[4:0] bits: 00011b初始低输出，在比较匹配时切换输出，在循环结束时保持输出

GPT320.GTUDDTYC.OBDTYR bit: 1
在释放0%或100%占空比设置后，将屏蔽比较匹配输出的值应用于GTIOB[3:2]位功能

Figure 23.46 输出占空比0%和100%功能示例

23.3.7 硬件计数开始计数停止和清除操作

GTCNT计数器可以由以下硬件源启动、停止或清除：

- 外部触发输入
- ELC事件输入
- GTIOCAGTIOCB引脚输入。

23.3.7.1 硬件启动操作

GTCNT计数器可以通过使用GTSSR选择硬件源来启动。

图23.47显示了一个硬件源的计数开始操作示例。图23.48显示了设置示例。

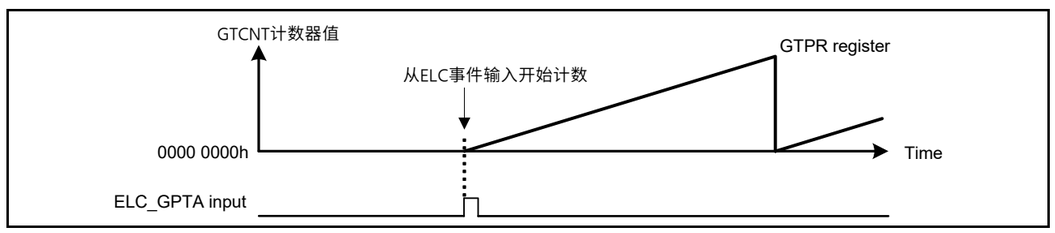


Figure 23.47 由硬件源启动的计数启动操作示例，在输入来自 ELC_GPTA event

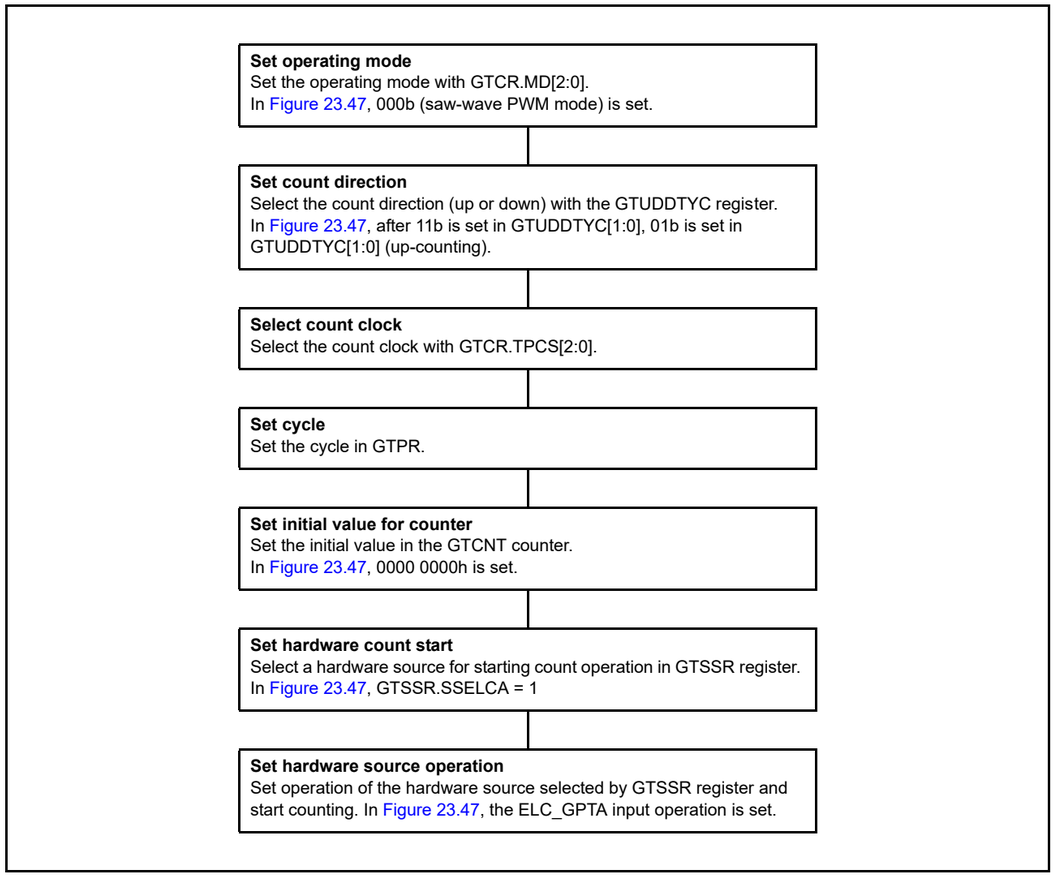


Figure 23.48 Example setting for count start operation by a hardware source

23.3.7.2 Hardware stop operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 23.49 shows an example of a count stop operation by a hardware source. Figure 23.50 shows the setting example. In this example, the count operation stops and restarts at the edge of the ELC event input.

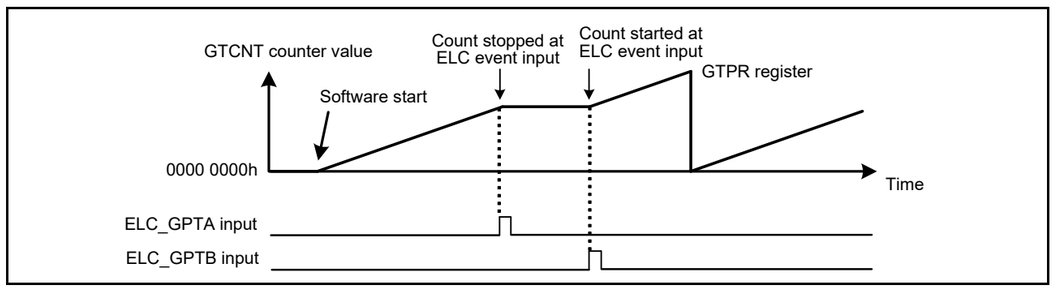


Figure 23.49 Example of count stop operation by a hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

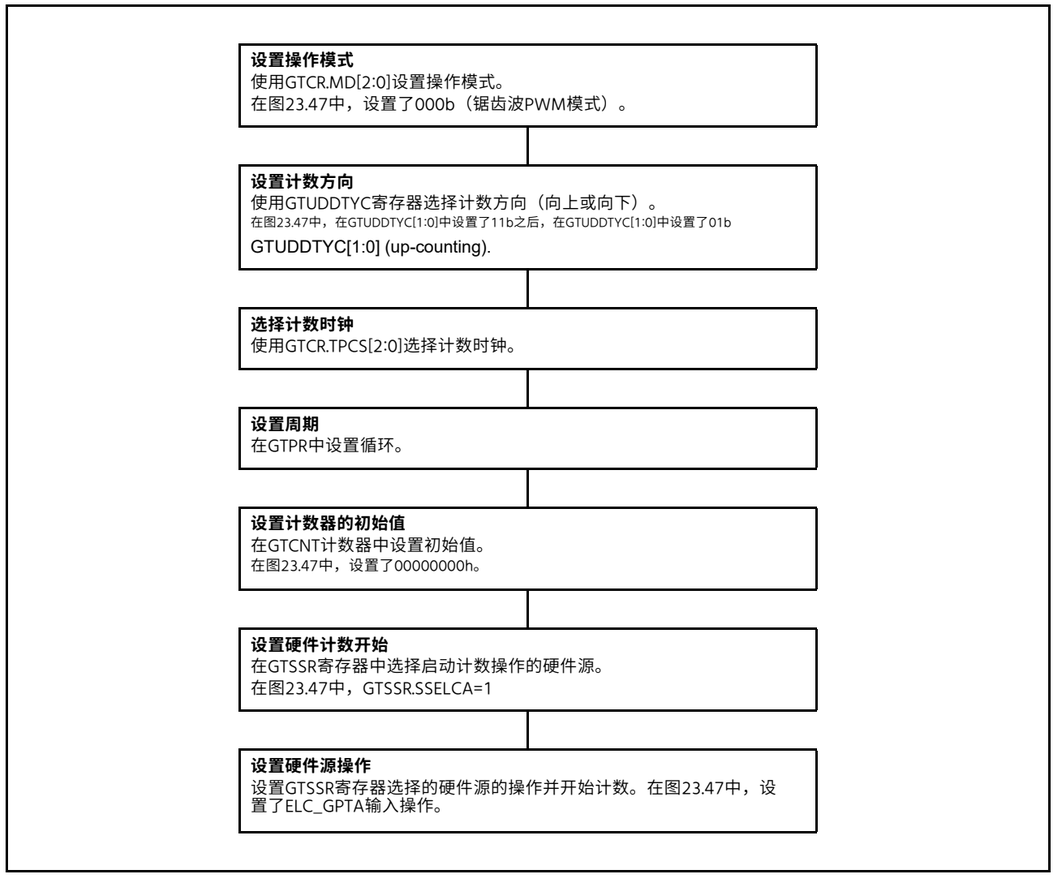


Figure 23.48 硬件源的计数开始操作设置示例

23.3.7.2 硬件停止操作

GTCNT计数器可以通过使用GTPSR选择硬件源来停止。

图23.49显示了一个硬件源的计数停止操作示例。图23.50显示了设置示例。
在本例中，计数操作在ELC事件输入的边沿停止并重新开始。

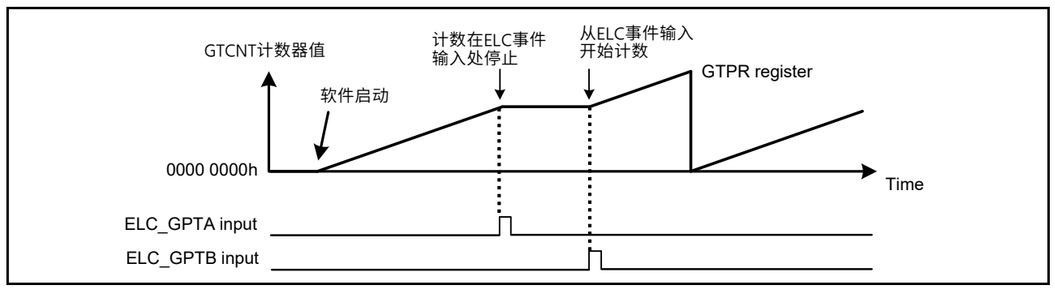


Figure 23.49 由软件启动的硬件源的计数停止操作示例，停止于ELC_GPTA输入，并在ELC_GPTB输入处重新启动

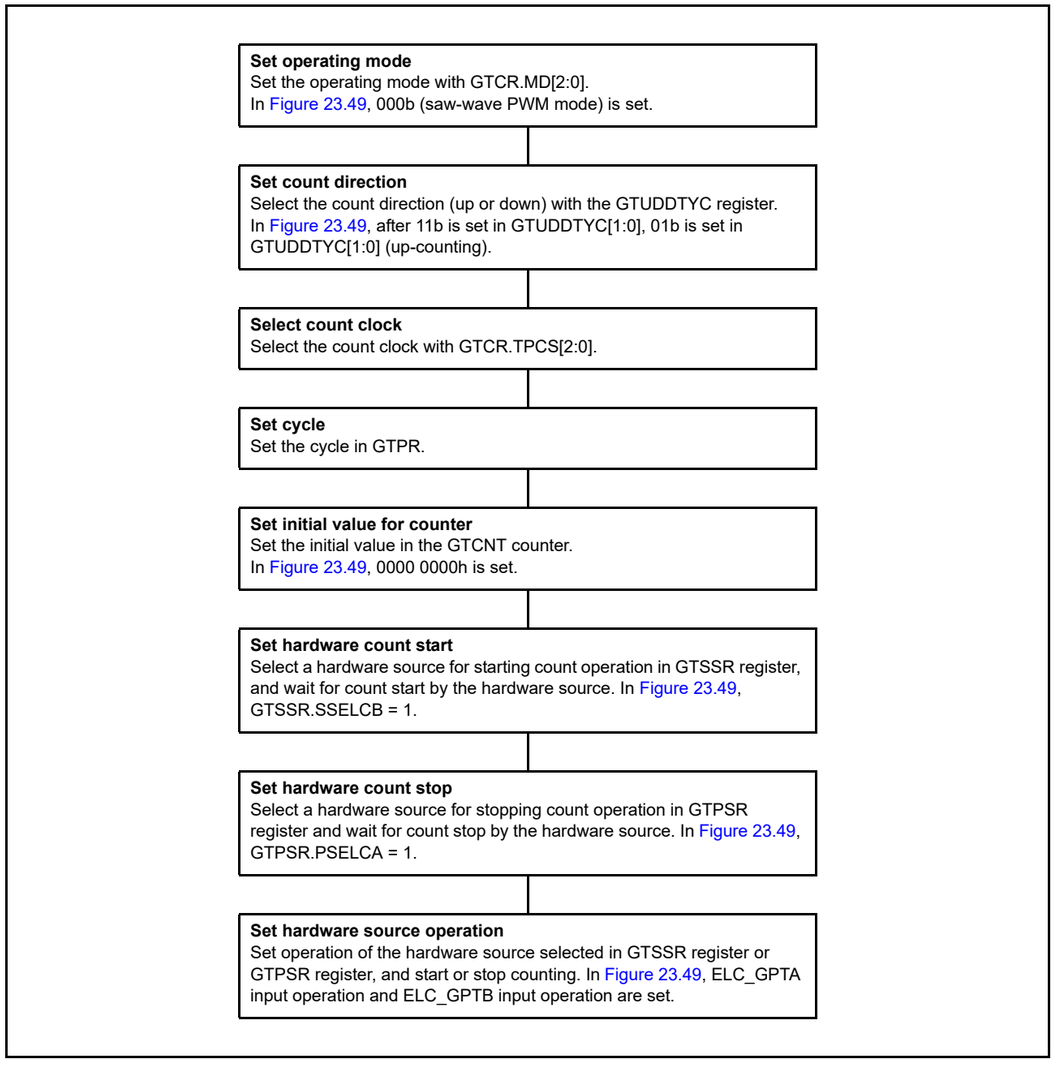


Figure 23.50 Example setting for count stop operation by a hardware source

Figure 23.51 shows an example of a count start/stop operation by a hardware source. Figure 23.52 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.

Figure 23.50 硬件源的计数停止操作设置示例

图23.51显示了一个硬件源的计数开始停止操作示例。图23.52显示了设置示例。在本例中，计数器在外部触发输入GTETRGA的高电平期间运行。

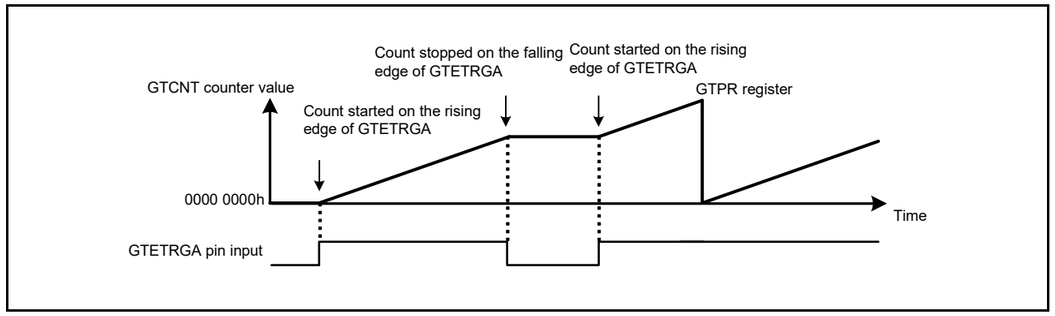


Figure 23.51 Example of count start/stop operation by a hardware source started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

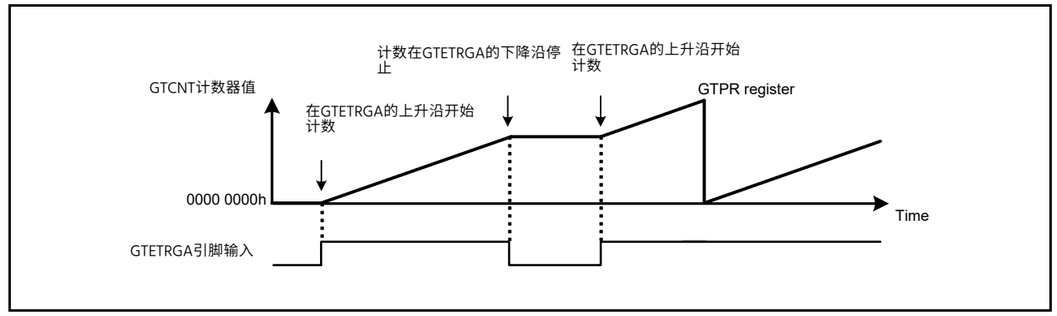


Figure 23.51 由硬件源在上升沿开始的计数开始停止操作示例 GTETRGA引脚输入，并在GTETRGA引脚输入的下降沿停止

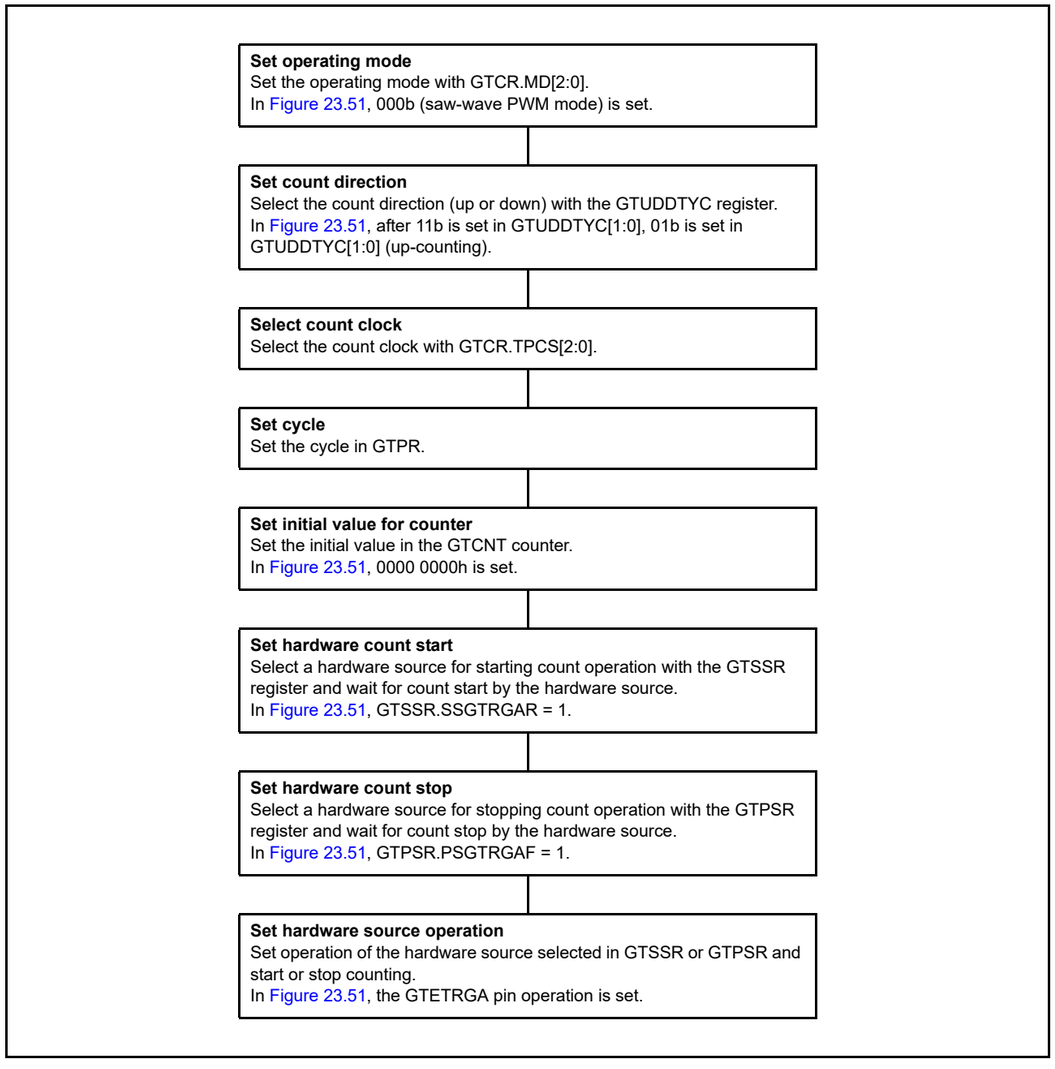


Figure 23.52 Example setting for count start/stop operation by a hardware source

23.3.7.3 Hardware clear operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 5, 8) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 23.53 and Figure 23.54 show examples of the GTCNT counter clearing operation by a hardware source. Figure 23.55 shows the setting example. In this example, the GTCNT counter starts at the edge of the ELC_GPTA input, and the counter stops and clears at the edge of the ELC_GPTB input.

Figure 23.52 硬件源的计数开始停止操作设置示例

23.3.7.3 硬件清除操作

GTCNT计数器可以通过使用GTCSR选择硬件源来清除。GPTn_OVFGPTn_UDF(n=0to5 8)中断（上溢下溢中断）不会在GTCNT计数器被硬件或软件清零时产生。

图23.53和图23.54显示了通过硬件源清除GTCNT计数器操作的示例。图23.55显示了设置示例。在本例中，GTCNT计数器在ELC_GPTA输入的边沿开始，计数器在ELC_GPTB输入的边沿停止并清零。

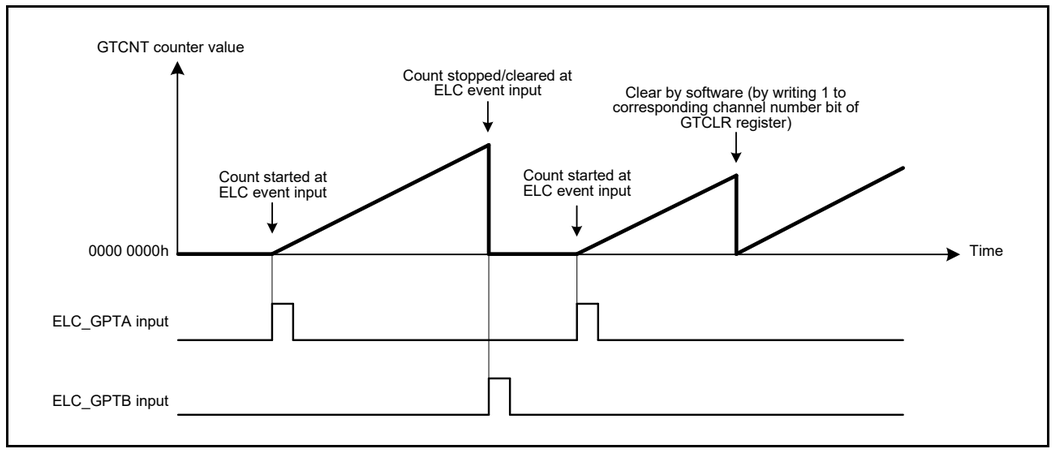


Figure 23.53 Examples of count clearing operation by hardware source with saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

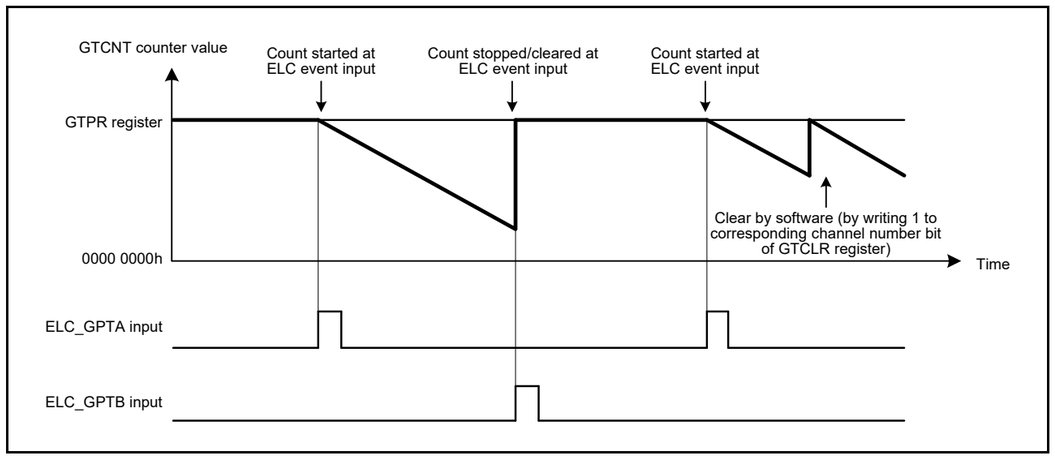


Figure 23.54 Examples of count clearing operation by hardware source with saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

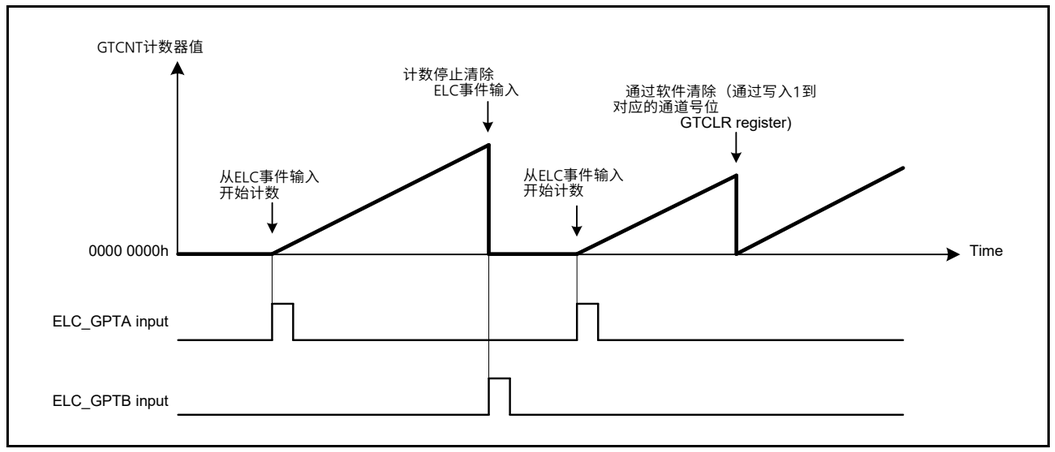


Figure 23.53 使用锯波递增计数的硬件源的计数清除操作示例，开始于ELC_GPTA输入，并在ELC_GPTB输入处停止清除

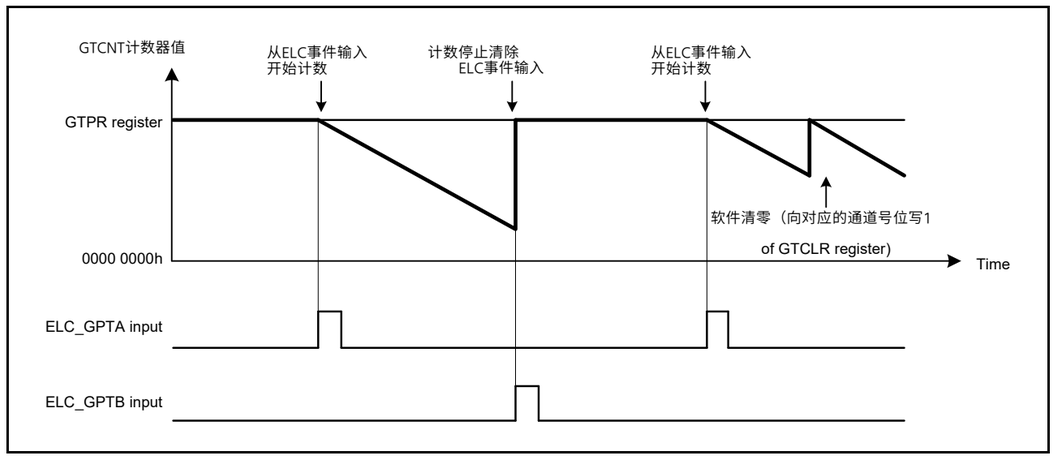


Figure 23.54 使用锯波递减计数的硬件源的计数清除操作示例，在ELC_GPTA输入处开始，在ELC_GPTB输入处停止清除

Set operating mode
Set the operating mode with GTCR.MD[2:0].
In Figure 23.53 and Figure 23.54, 000b (saw-wave PWM mode) is set.

Set count direction
Select the count direction (up or down) with the GTUDDTYC register.
In Figure 23.53, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting). In Figure 23.54, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).

Select count clock
Select the count clock with GTCR.TPCS[2:0].

Set cycle
Set the cycle in the GTPR register.

Set initial value for counter
Set the initial value in the GTCNT counter.
In Figure 23.53, 0000 0000h is set. In Figure 23.54, the GTPR value is set.

Set hardware count start
Select a hardware source for starting count operation in the GTSSR register and wait for count start by the hardware source. In Figure 23.53 and Figure 23.54, GTSSR.SSELCA = 1.

Set hardware count stop
Select a hardware source for stopping count operation in the GTPSR register and wait for count stop by the hardware source. In Figure 23.53 and Figure 23.54, GTPSR.PSELCB = 1.

Set hardware count clear
Select a hardware source for clearing count operation in the GTCSR register and wait for count clear by the hardware source. In Figure 23.53 and Figure 23.54, GTCSR.CSELCB = 1.

Set hardware source operation
Set operation of the hardware source selected in the GTSSR, GTPSR, or GTCSR register and start, stop, or clear counting.
In Figure 23.53 and Figure 23.54, the ELC_GPTA input and ELC_GPTB input are set.

Figure 23.55 Example for setting count clearing operation by a hardware source

The GPTn_OVF/GPTn_UDF (n = 0 to 5, 8) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 23.56 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 5, 8) interrupt.

设置操作模式
使用GTCR.MD[2:0]设置操作模式。
在图23.53和图23.54中，设置了000b（锯齿波PWM模式）。

设置计数方向
使用GTUDDTYC寄存器选择计数方向（向上或向下）。
在图23.53中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。在图23.54，在GTUDDTYC[1:0]中设置10b后，在GTUDDTYC[1:0]中设置00b（向下计数）。

选择计数时钟
使用GTCR.TPCS[2:0]选择计数时钟。

设置周期
在GTPR寄存器中设置周期。

设置计数器的初始值
在GTCNT计数器中设置初始值。
在图23.53中，设置了00000000h。在图23.54中，设置了GTPR值。

设置硬件计数开始
在GTSSR寄存器中选择一个开始计数操作的硬件源，等待硬件源开始计数。在图23.53和图23.54中，GTSSR.SSELCA=1。

设置硬件计数停止
在GTPSR寄存器中选择一个停止计数操作的硬件源，并等待硬件源停止计数。在图23.53和图23.54中，GTPSR.PSELCB=1。

设置硬件计数清除
在GTCSR寄存器中选择清除计数操作的硬件源，等待硬件源清除计数。在图23.53和图23.54中，GTCSR.CSELCB=1。

设置硬件源操作
设置在GTSSR、GTPSR或GTCSR寄存器中选择的硬件源的操作，并开始、停止或清除计数。在图23.53和图23.54中，设置了ELC_GPTA输入和ELC_GPTB输入。

Figure 23.55 通过硬件源设置计数清除操作的示例

GPTn_OVFGPTn_UDF(n=0to5 8)中断（上溢下溢中断）不会在计数器被硬件源或软件清零时产生。

图23.56显示了通过硬件源清除计数器和GPTn_OVF（n=0到5、8）中断之间的关系。

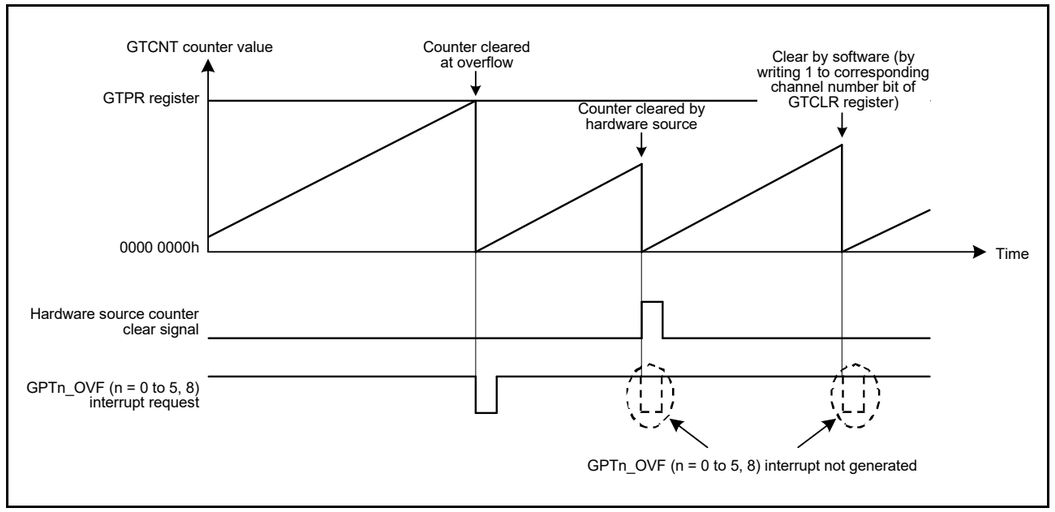


Figure 23.56 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 5, 8) interrupt

23.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

23.3.8.1 Synchronized operation by software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

Figure 23.57 shows an example of a simultaneous start, stop, and clear by software. Figure 23.58 shows an example of a phase start operation by software.

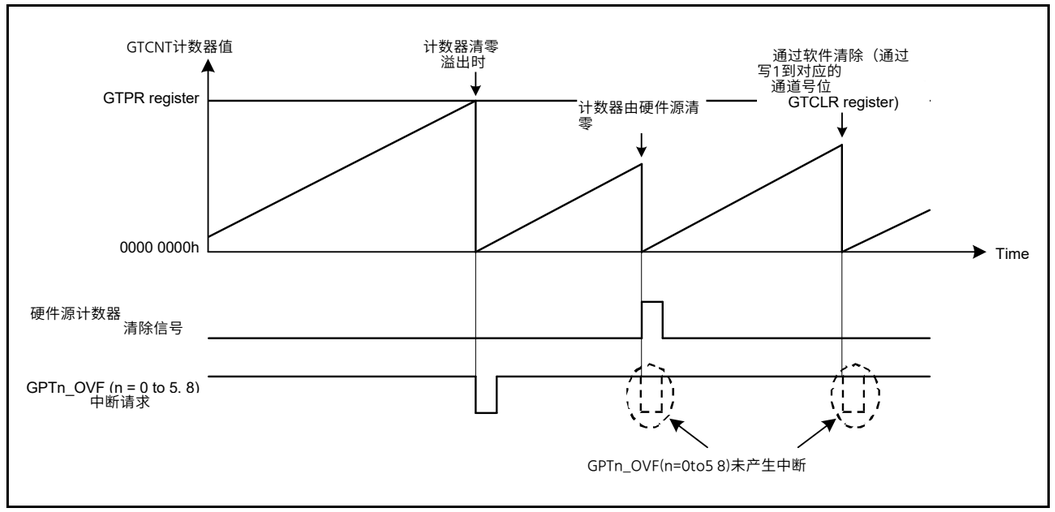


Figure 23.56 硬件源计数器清零与GPTn_OVF(n=0to5 8)中断的关系

23.3.8 同步操作

可以对通道进行同步操作，例如同步启动、停止和清除操作。

23.3.8.1 软件同步操作

通过设置相关的GTSTR，可以在多个通道上启动、停止和清除GTCNT计数器，
GTSTP或GTCLR位同时为1。

通过在GTCNT计数器中设置初始值并同时将相关的GTSTR位设置为1，可以从相位差开始计数。

图23.57显示了通过软件同时启动、停止和清除的示例。图23.58显示了通过软件进行相位启动操作的示例。

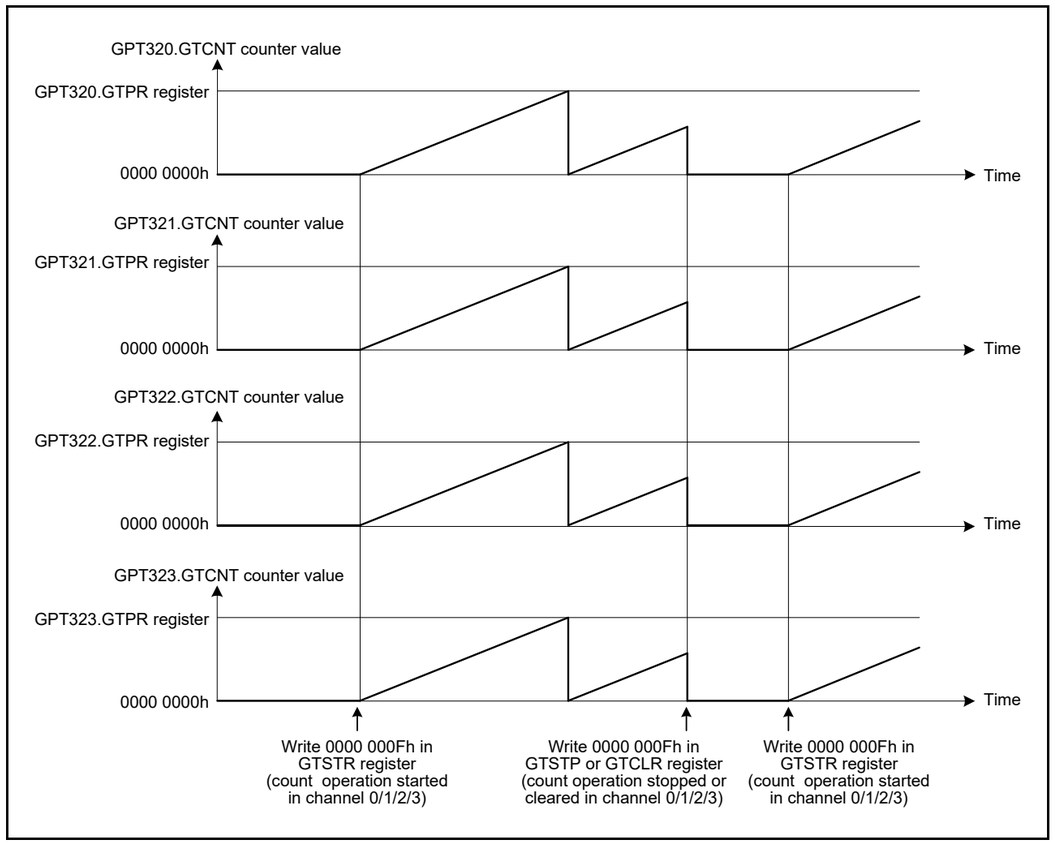


Figure 23.57 Example of a simultaneous start, stop, and clear by software with the same count cycle (GTPR register value)

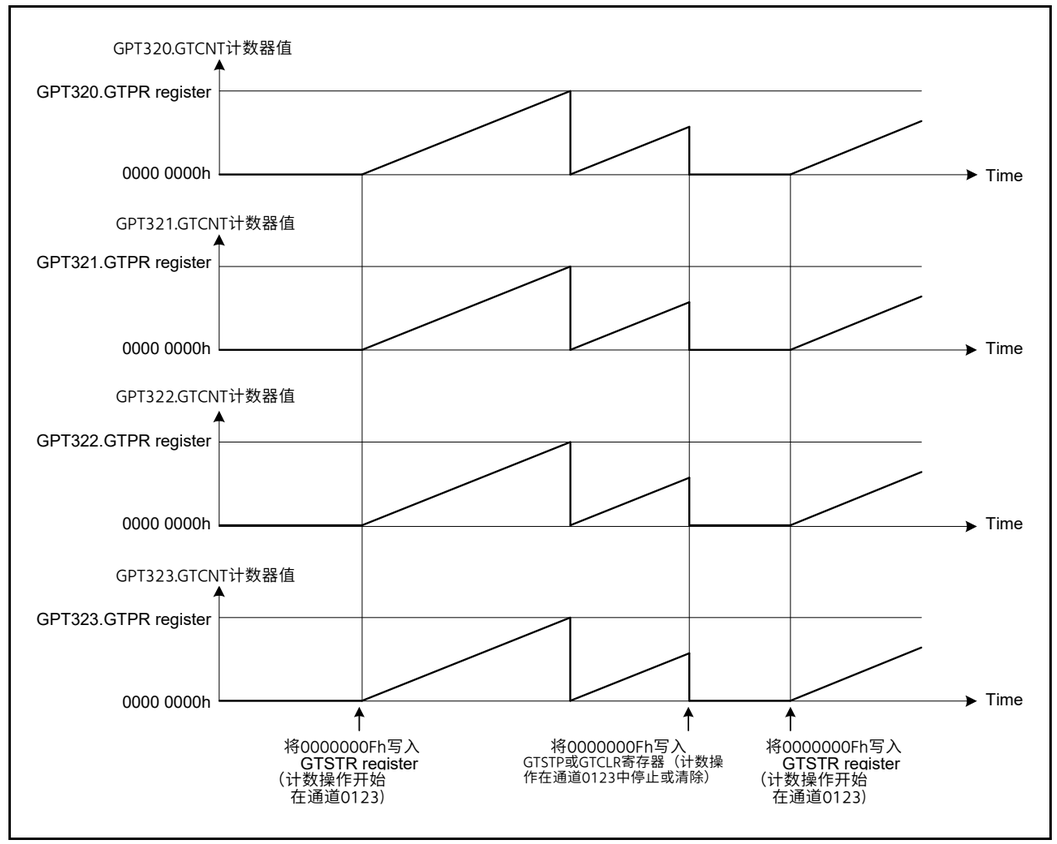


Figure 23.57 使用相同计数周期（GTPR寄存器值）的软件同时启动、停止和清除的示例

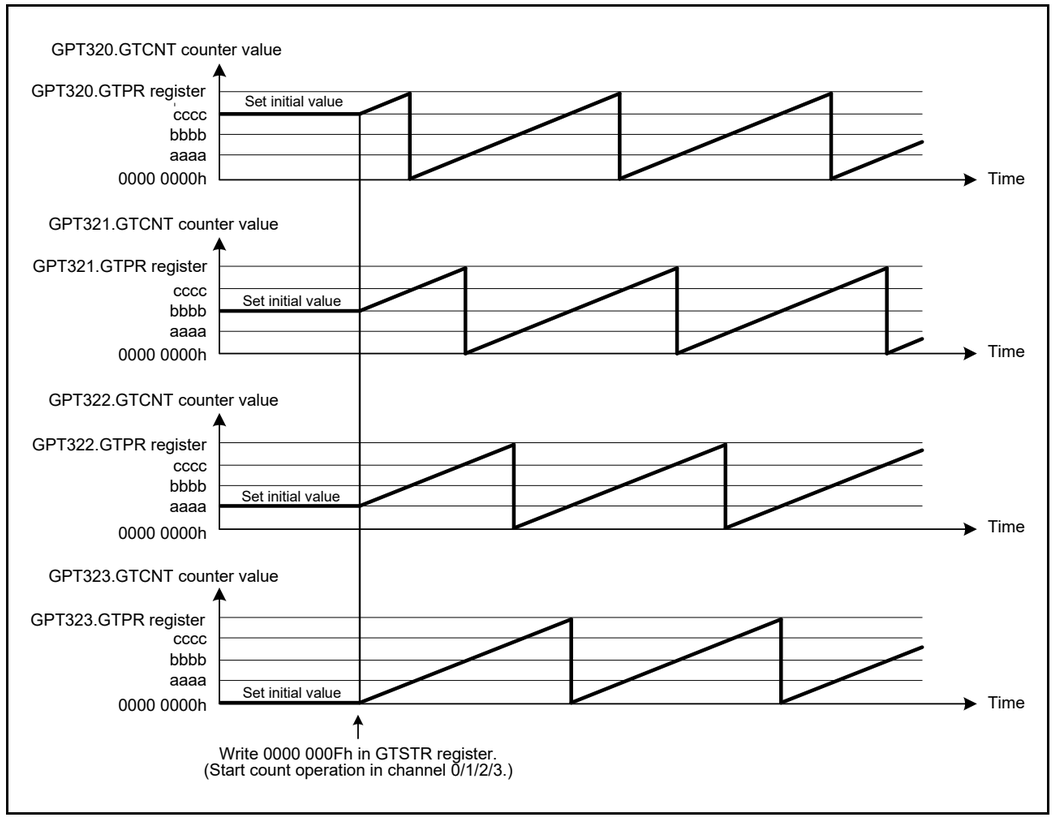


Figure 23.58 Example of software phase start with the same count cycle (GTPR register value)

23.3.8.2 Synchronized operation by hardware

The GTCNT counters can be started simultaneously by the following hardware sources:

- External trigger input
- ELC event input.

Figure 23.59 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Figure 23.60 shows the setting example.

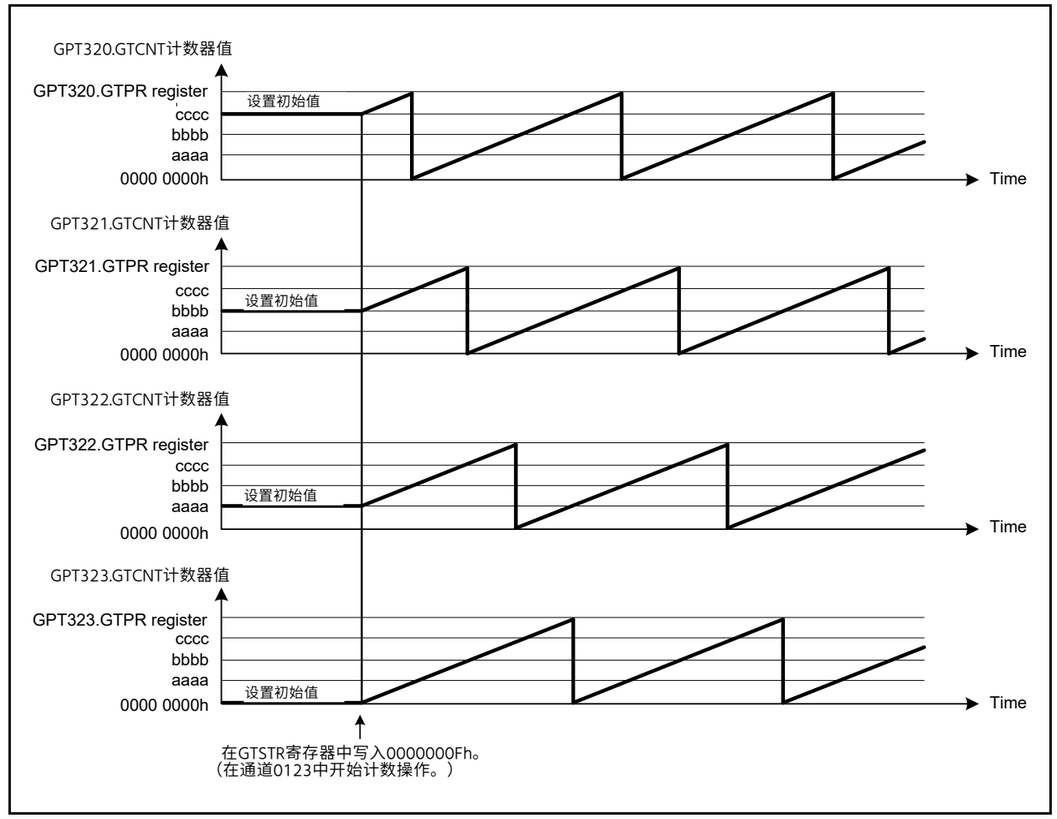


Figure 23.58 以相同计数周期开始的软件阶段示例（GTPR寄存器值）

23.3.8.2 硬件同步操作

GTCNT计数器可以由以下硬件源同时启动：

- 外部触发输入
- ELC事件输入。

图23.59显示了一个硬件源同时启动、停止和清除操作的示例。图23.60显示了设置示例。

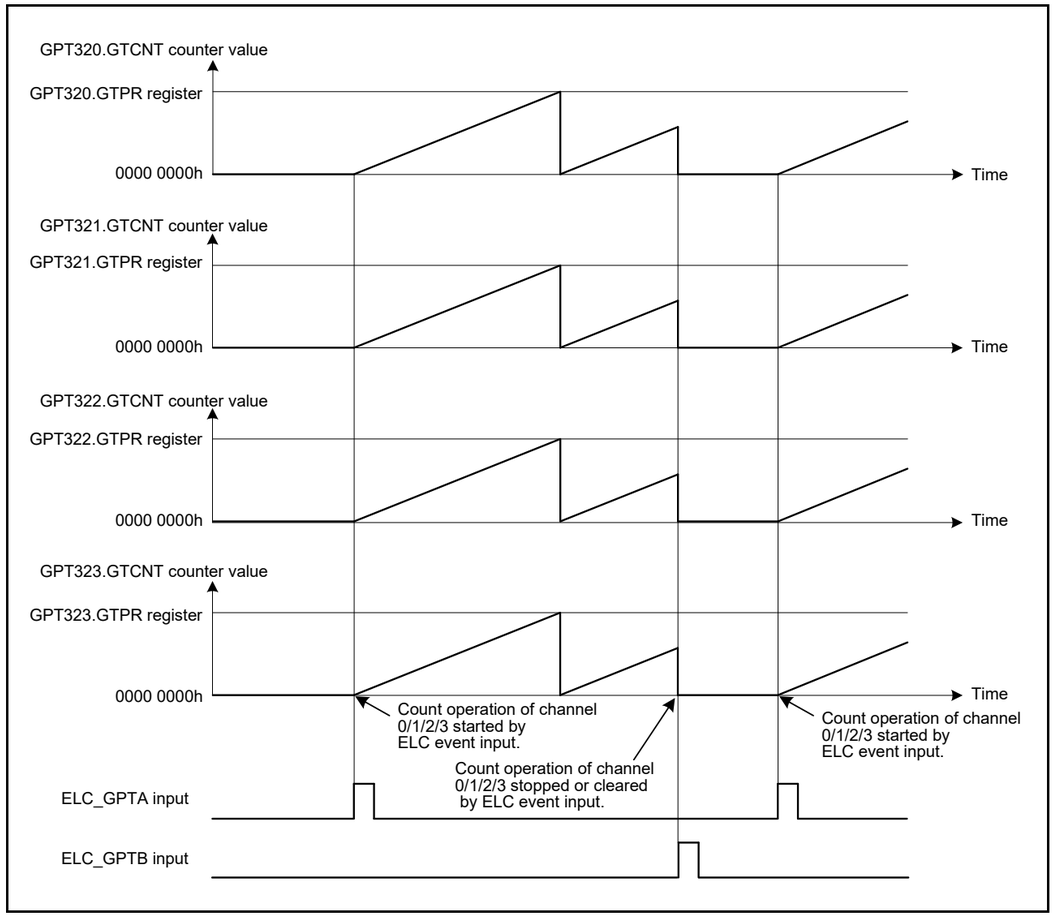


Figure 23.59 Example of a simultaneous start, stop, and clear by a hardware source with the same count cycle (GTPR register value)

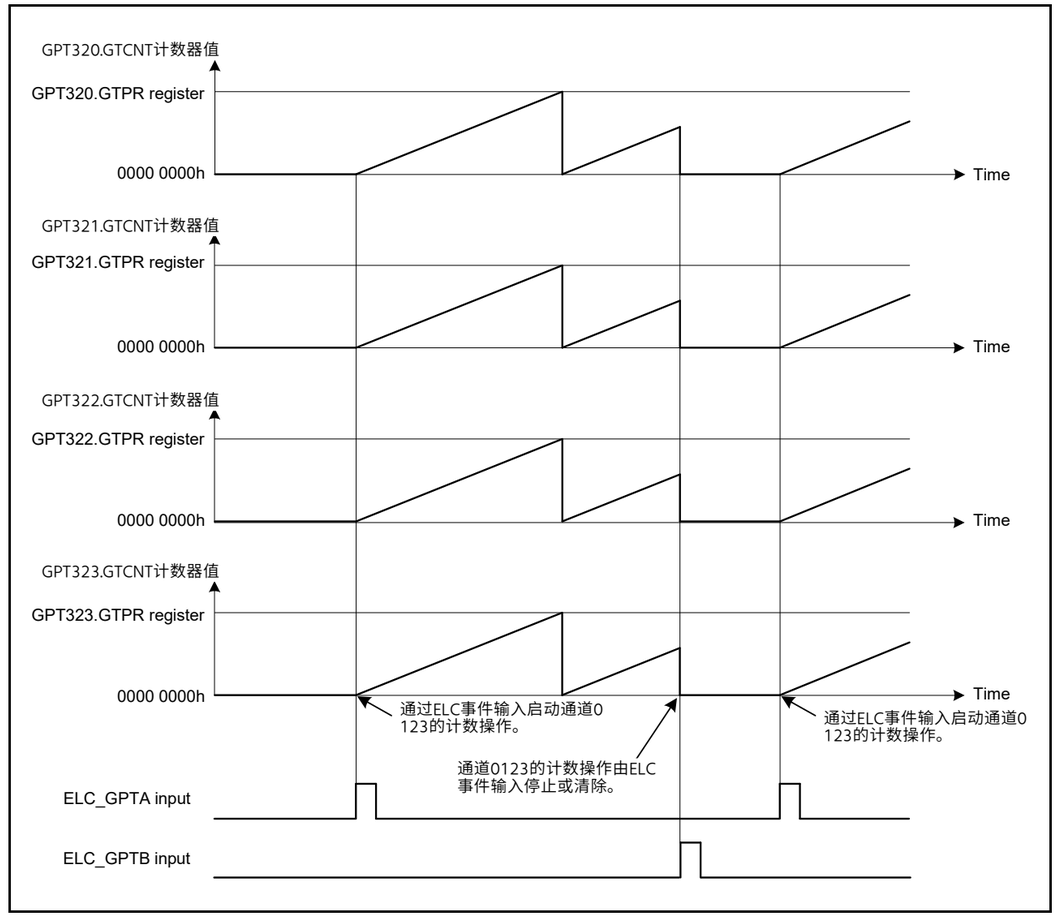


Figure 23.59 具有相同计数周期（GTPR寄存器值）的硬件源同时启动、停止和清除的示例

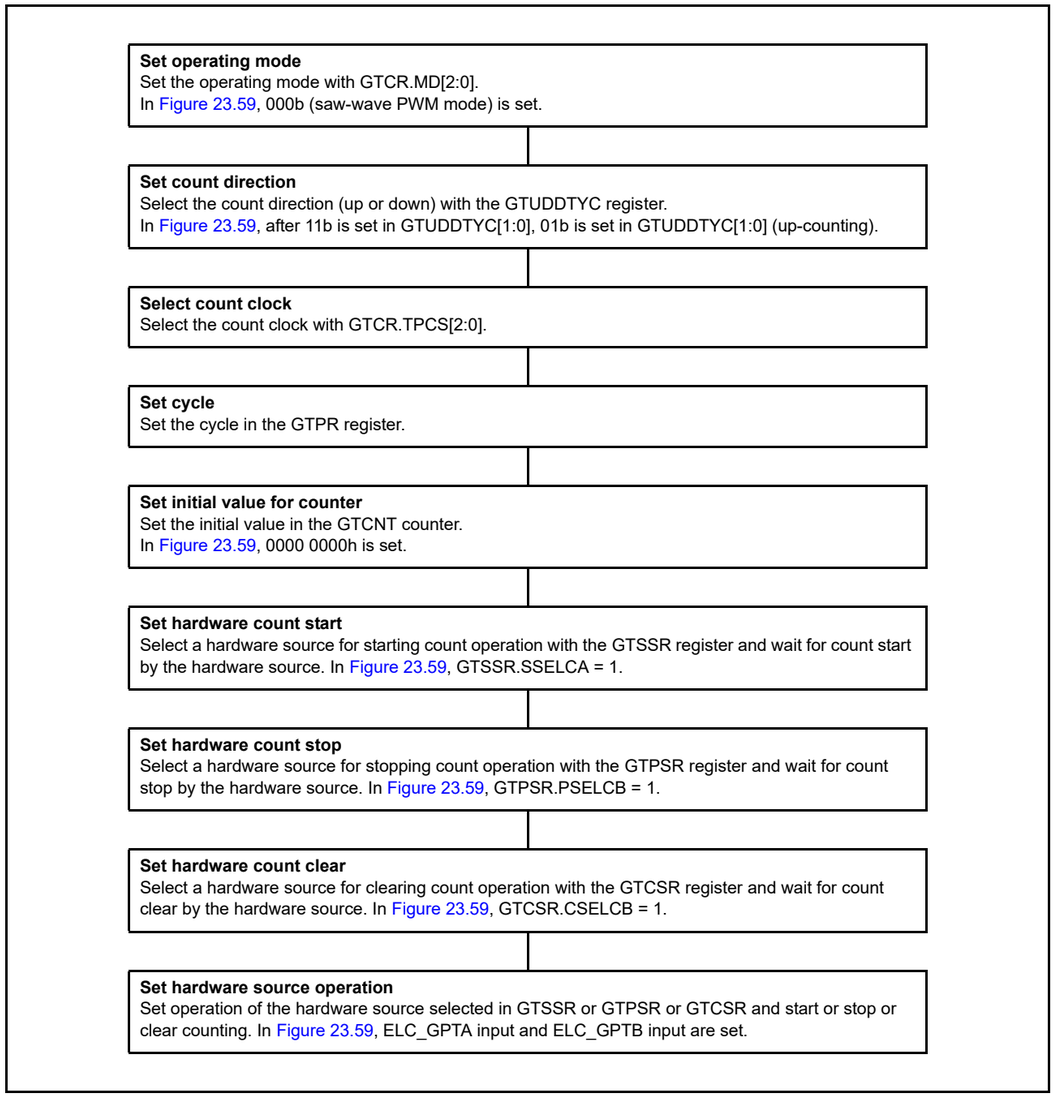


Figure 23.60 Example setting for simultaneous start by a hardware source

23.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 20 phases of linked PWM waveforms for a maximum of 10 channels by multiple GPTs.

Figure 23.61 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

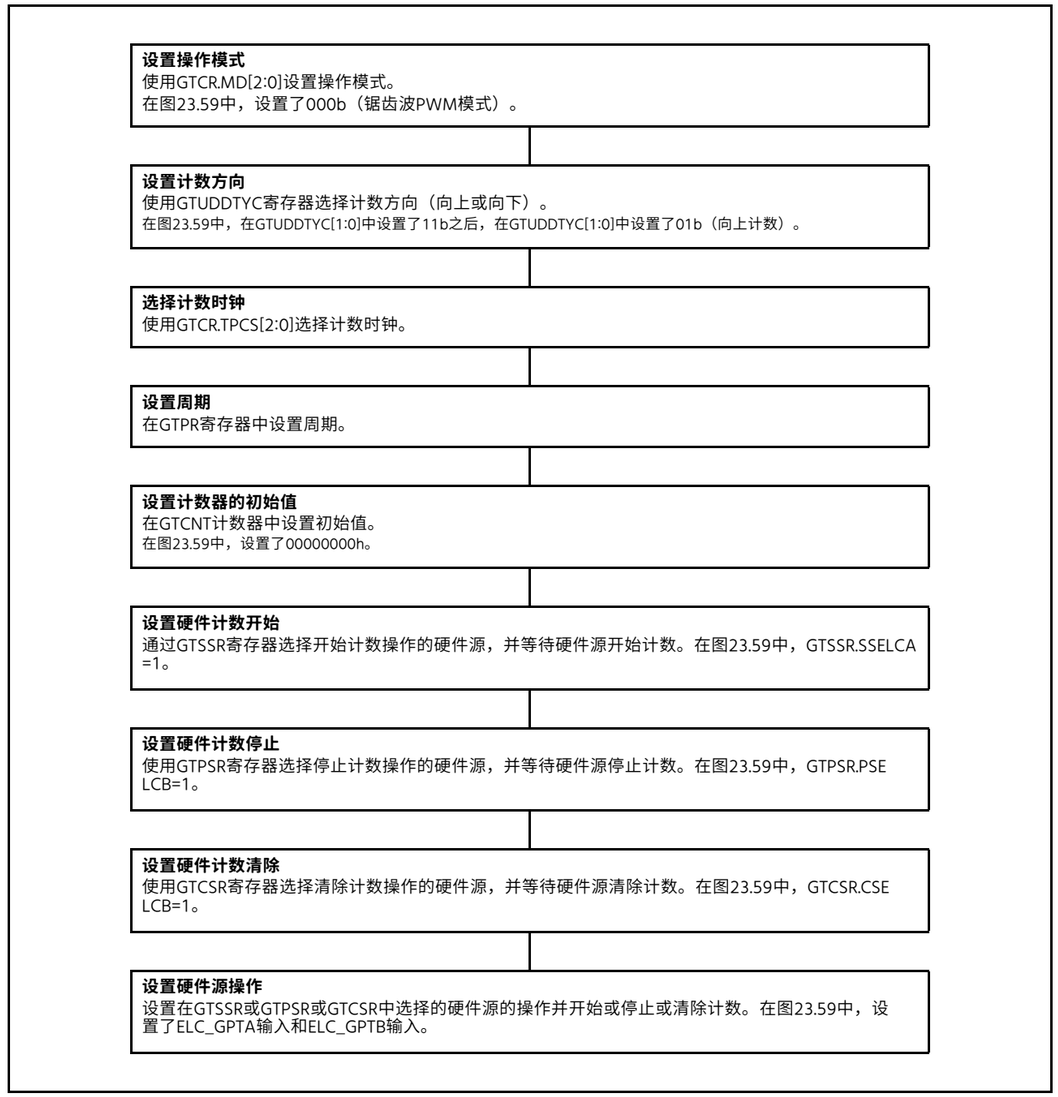


Figure 23.60 通过硬件源同时启动的示例设置

23.3.9 PWM输出操作示例

(1) 同步PWM输出

GPT通过多个GPT为最多10个通道输出20相链接的PWM波形。

图23.61显示了一个示例，其中4个通道在锯齿波PWM模式下执行同步操作并输出8相PWM波形。GTIOCA设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCB设置为输出低作为初始值，在GTCCRB比较匹配时输出高，在循环结束时输出低。

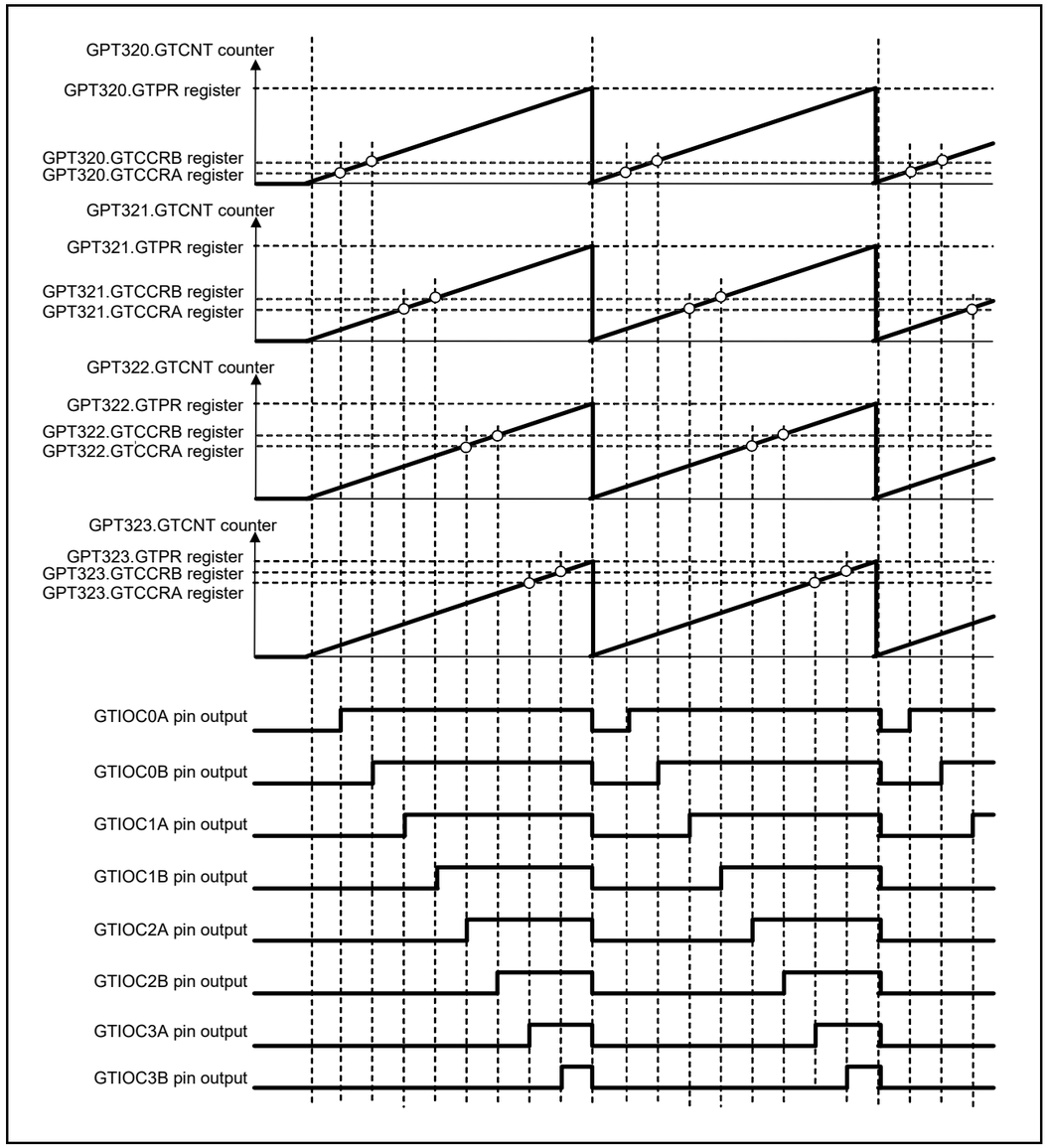


Figure 23.61 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 23.62 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

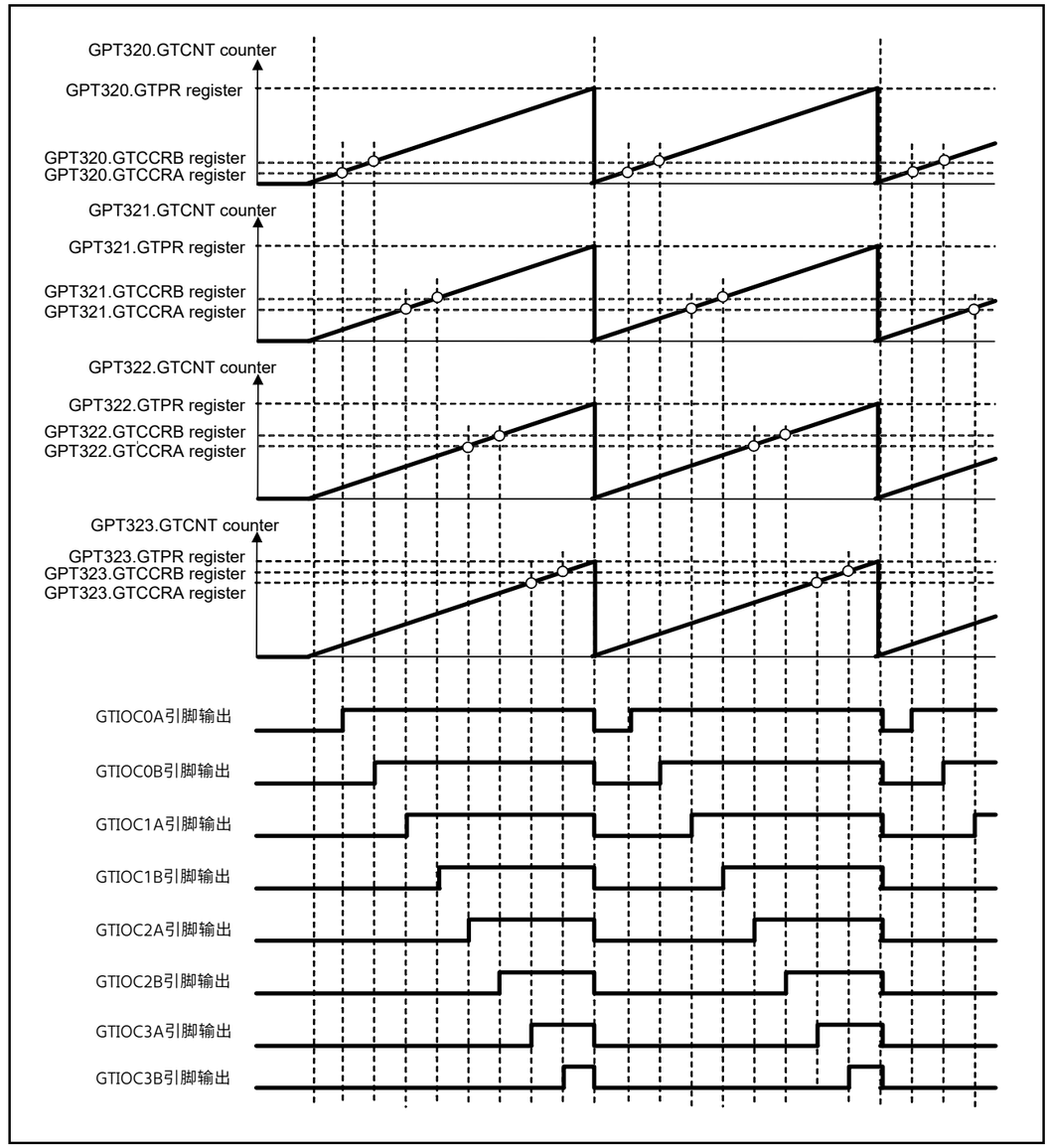


Figure 23.61 同步PWM输出示例

(2) 三相锯齿波互补PWM输出

图23.62显示了一个示例，其中三个通道在锯齿波PWM模式下执行同步操作并输出三相互补PWM波形。GTIOCA引脚设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCB引脚设置为输出高作为初始值，在GTCCRB比较匹配时输出低，在周期结束时输出高。

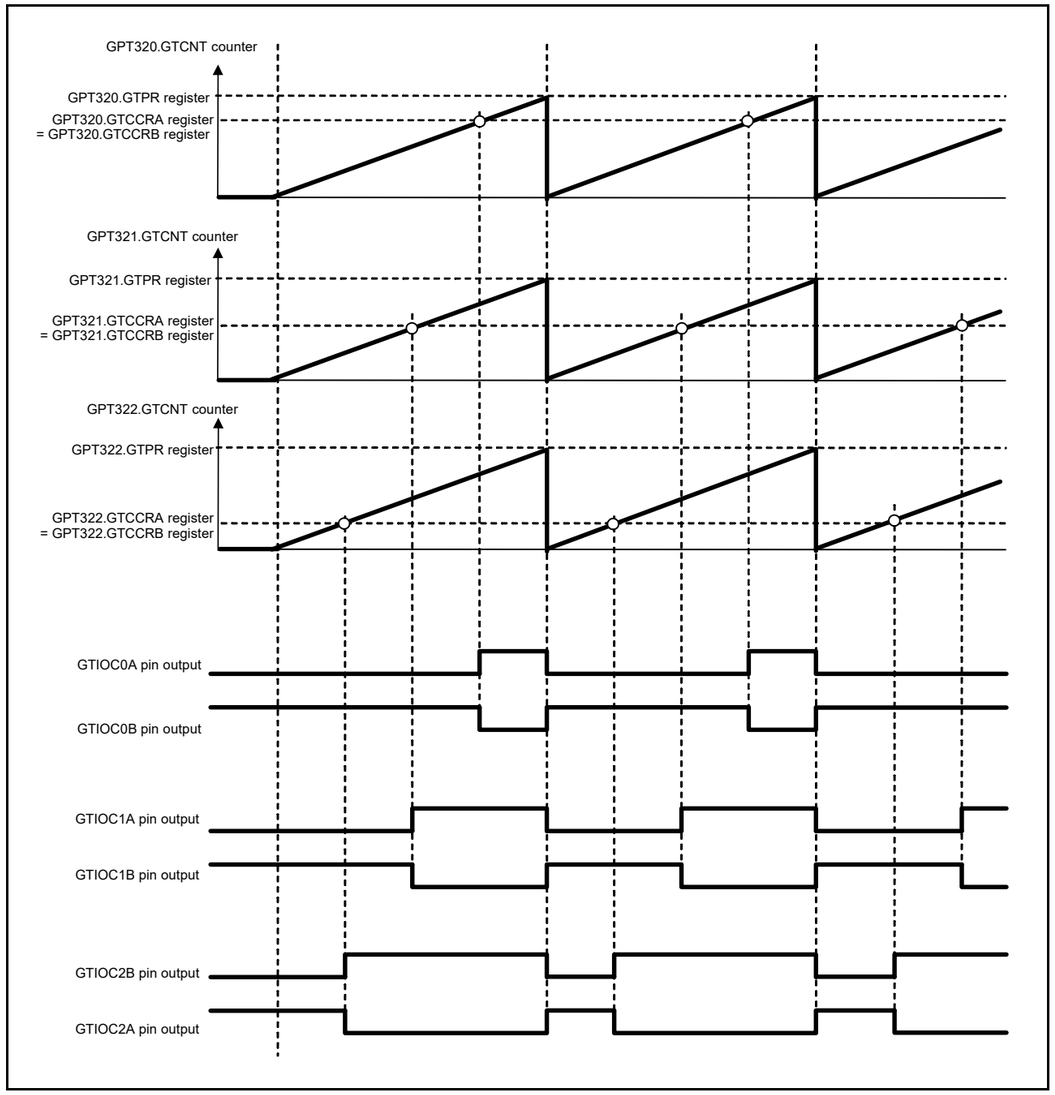


Figure 23.62 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 23.63 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

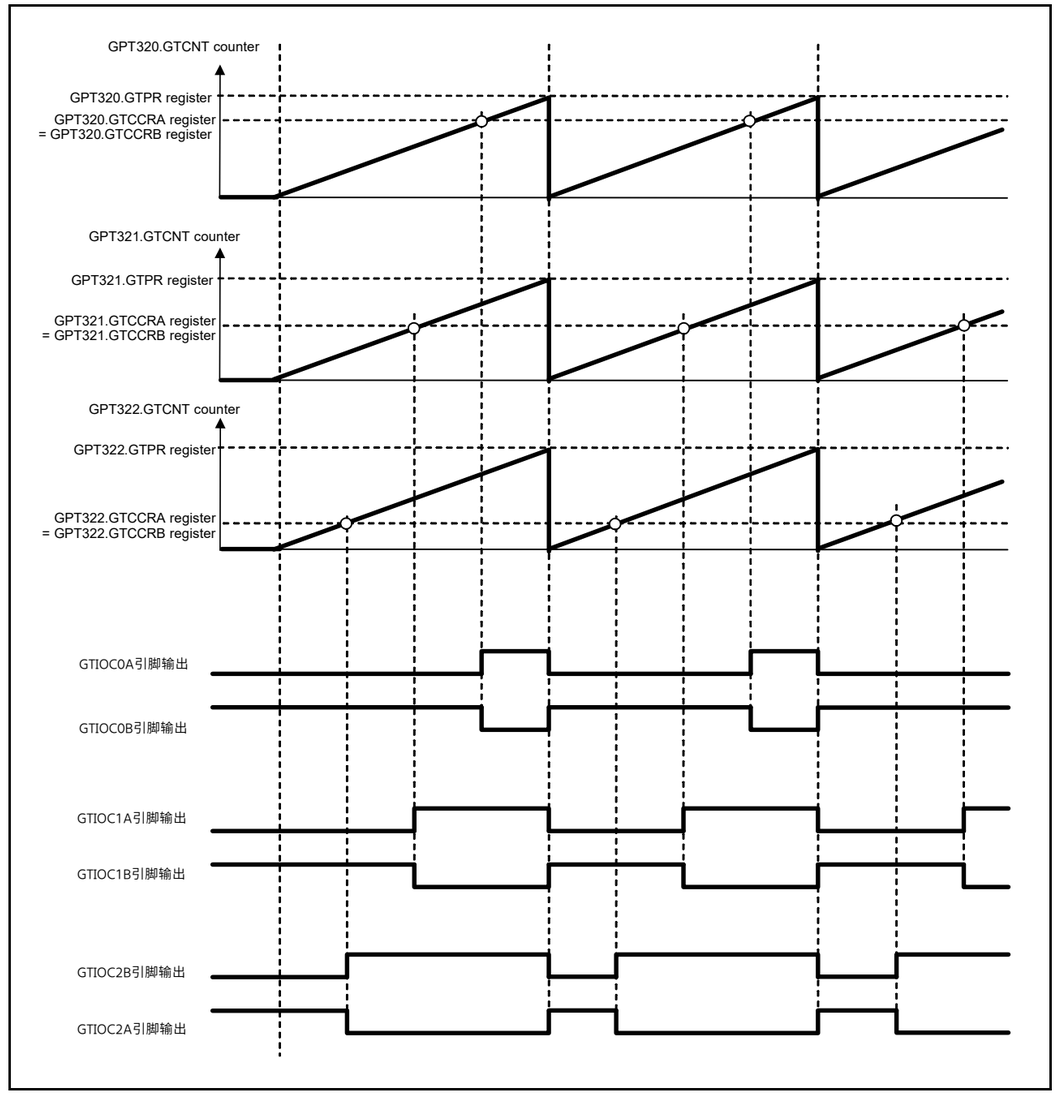


Figure 23.62 三相锯齿波互补PWM输出示例

(3) 具有自动死区时间设置的三相锯齿波互补PWM输出

图23.63显示了一个示例，其中三个通道在具有自动死区时间设置的锯齿波一次性脉冲模式下执行同步操作并输出三相互补PWM波形。GTIOCA引脚设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

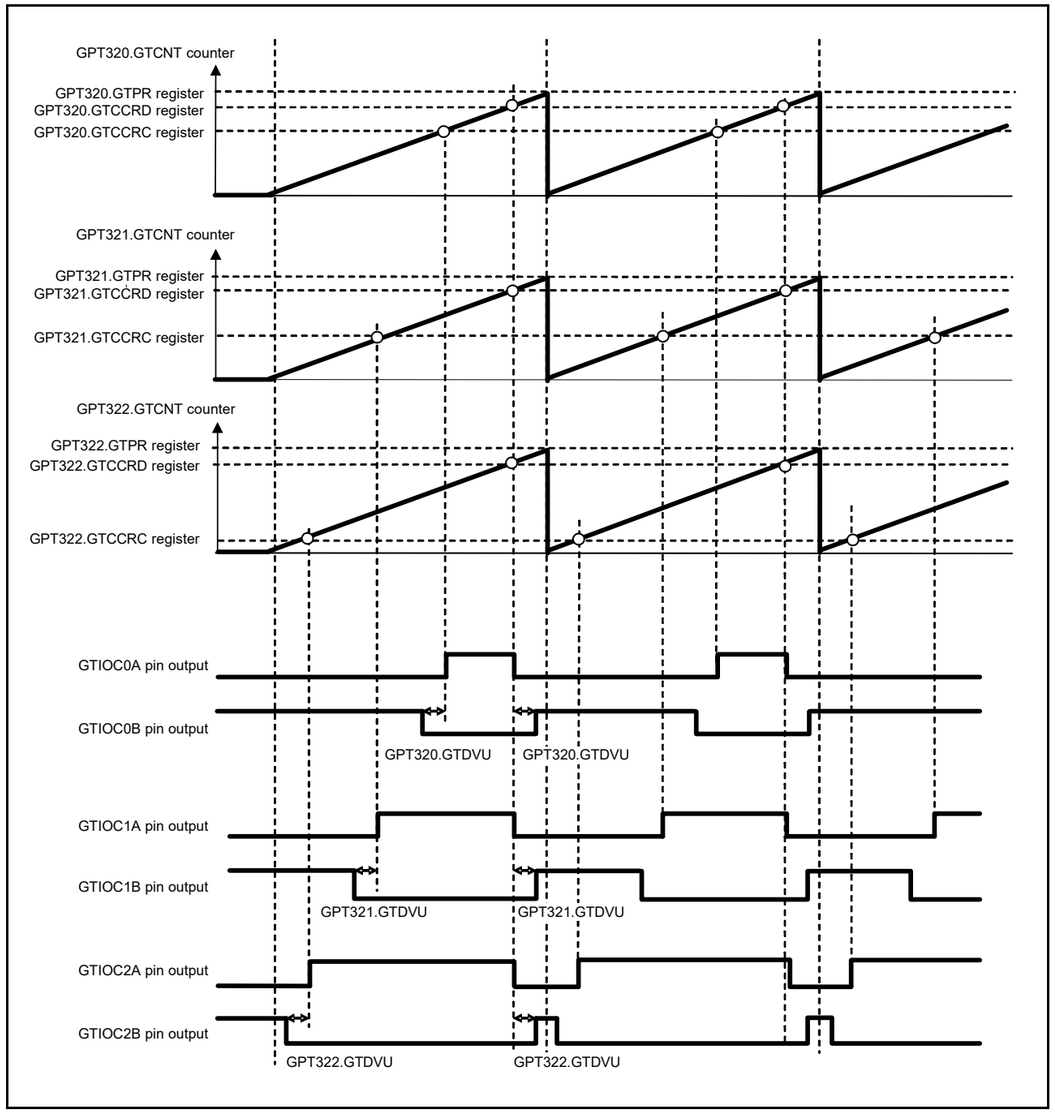


Figure 23.63 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 23.64 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

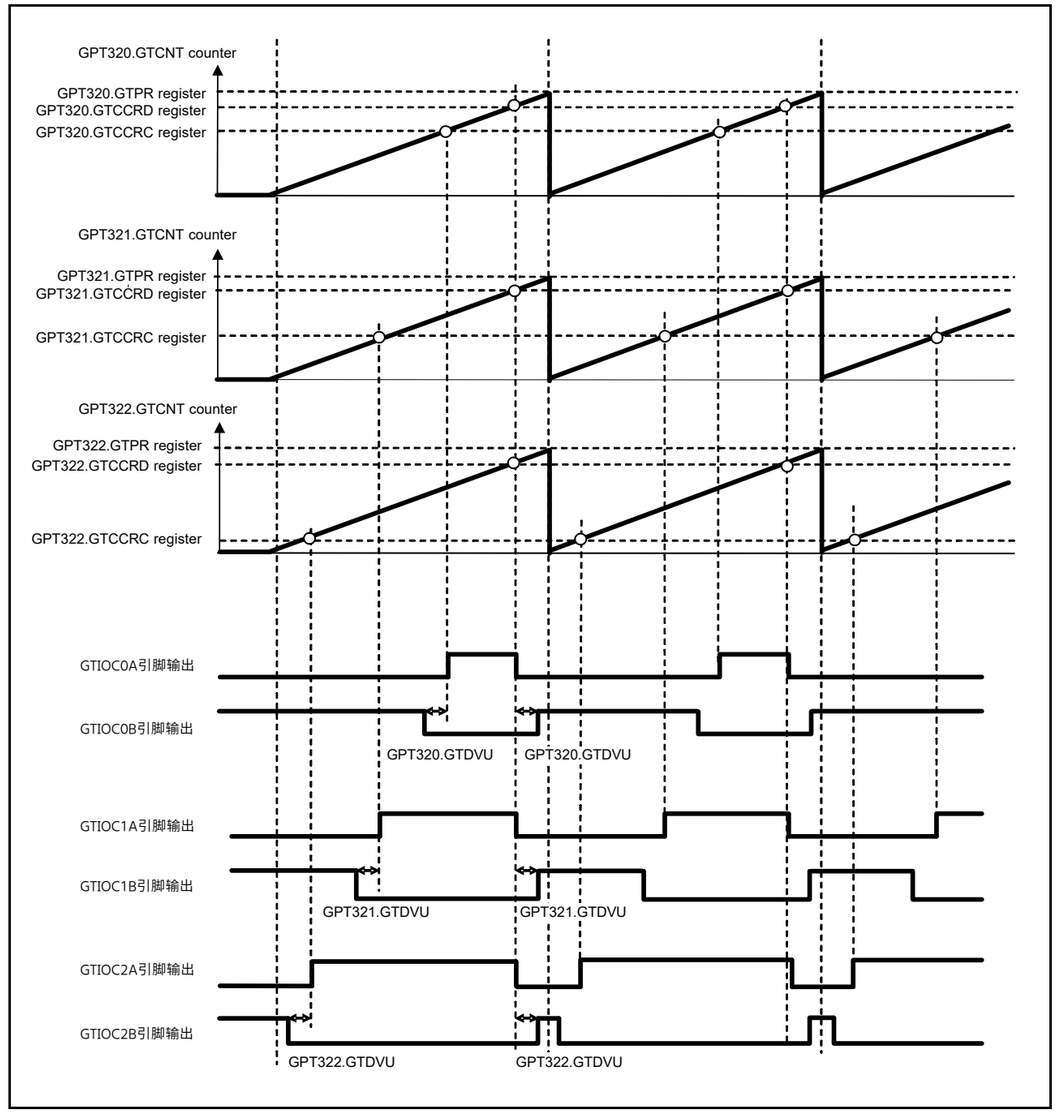


Figure 23.63 具有自动死区时间设置的三相锯齿波互补PWM输出示例

(4) 三相三角波互补PWM输出

图23.64显示了一个示例，其中三个通道在三角波PWM模式1中执行同步操作并输出三相互补PWM波形。GTIOCA引脚设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

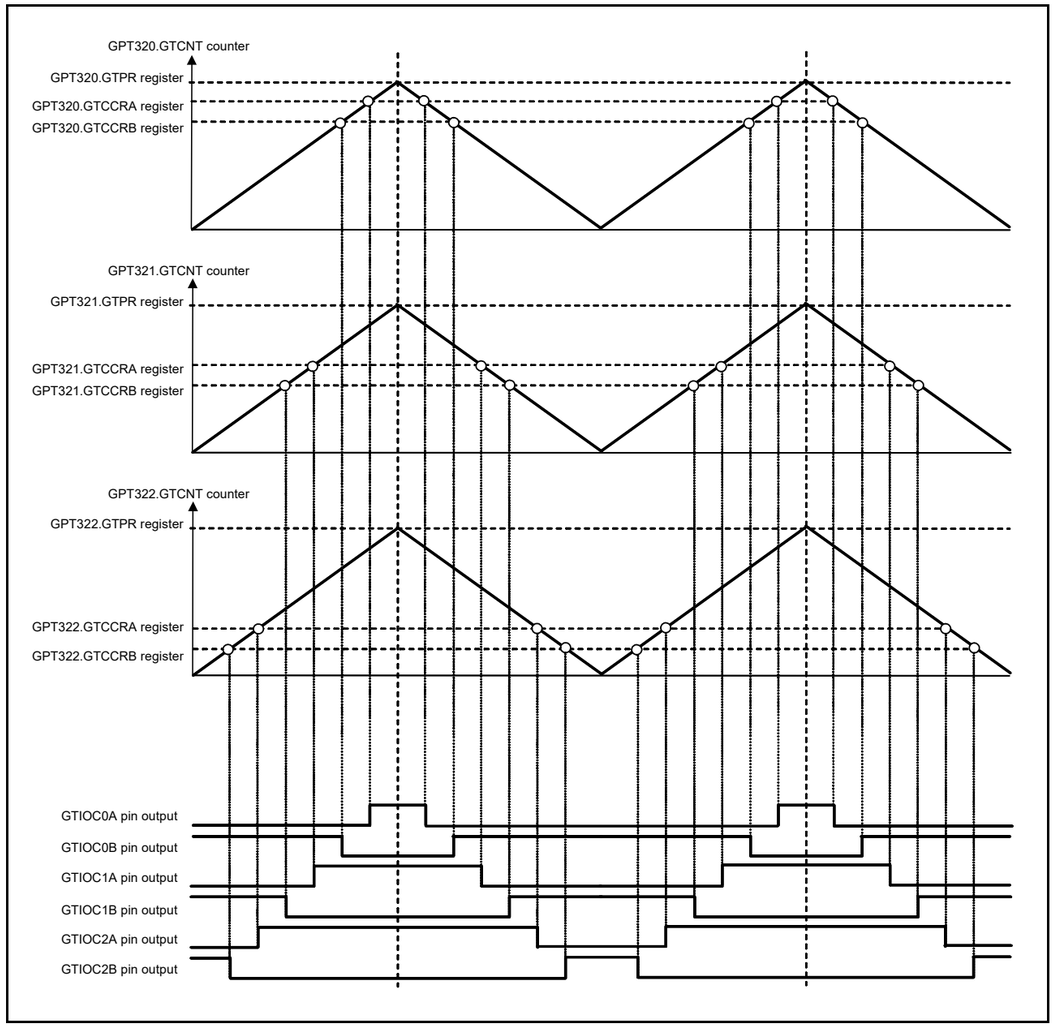


Figure 23.64 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 23.65 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

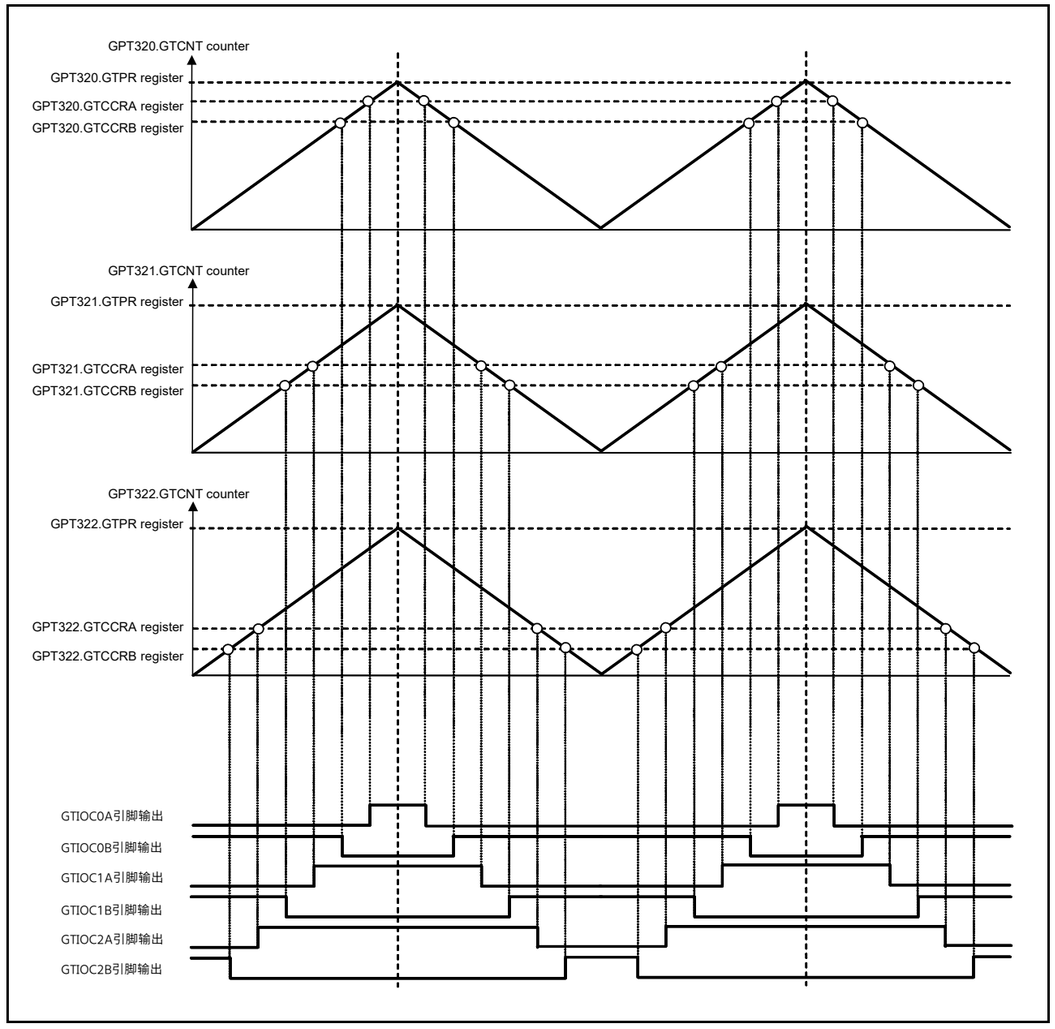


Figure 23.64 三相三角波互补PWM输出示例

(5) 具有自动死区时间设置的三相三角波互补PWM输出

图23.65显示了一个示例，其中三个通道在三角波PWM模式1下执行同步操作，自动设置死区时间并输出3相互补PWM波形。GTIOCA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

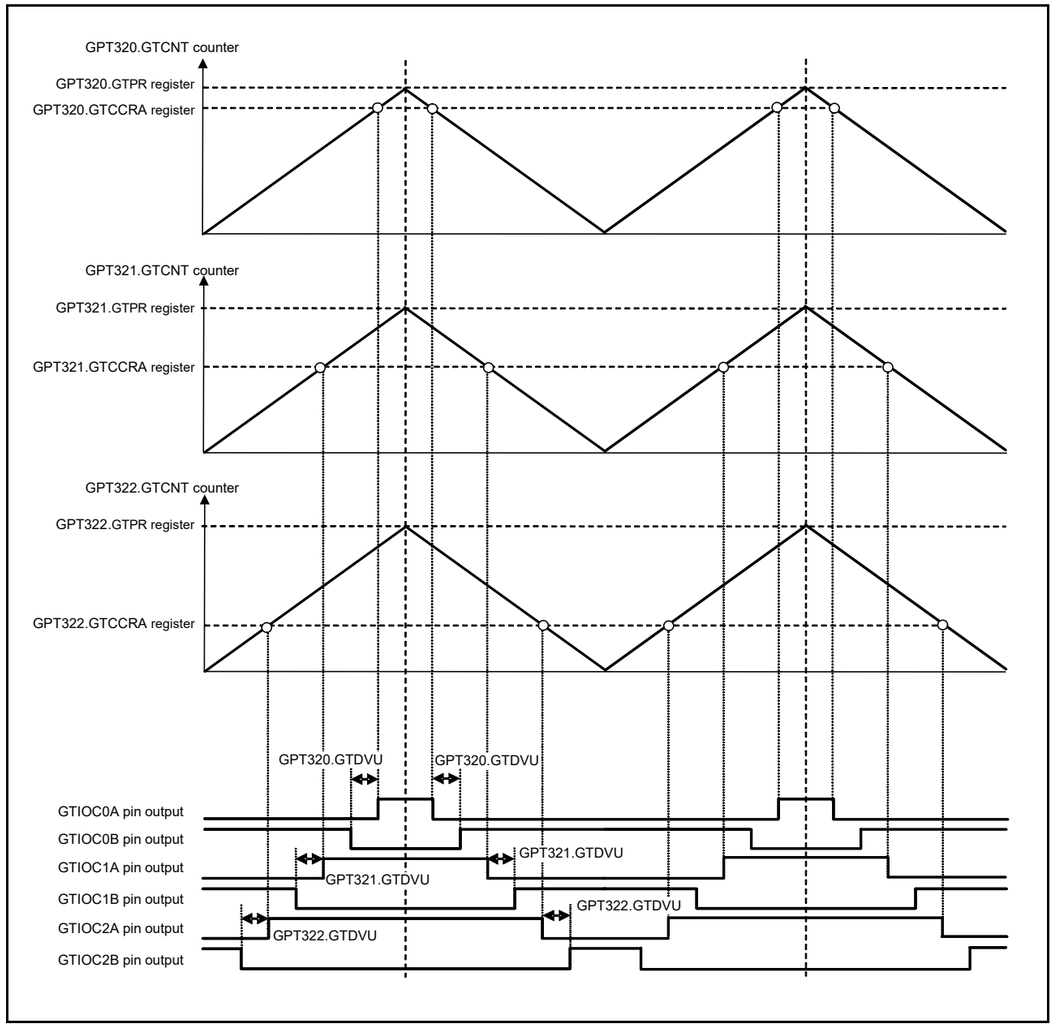


Figure 23.65 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 23.66 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

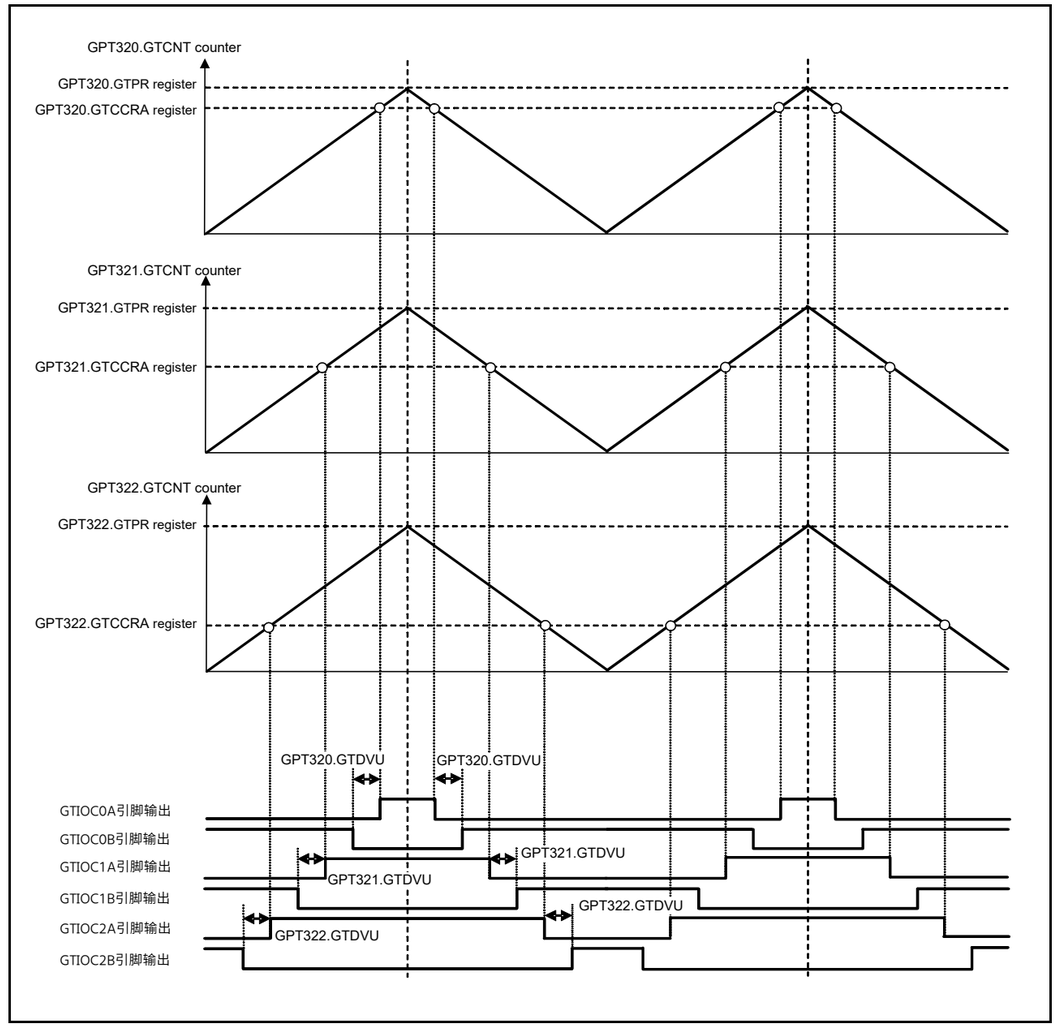


Figure 23.65 具有自动死区时间设置的三相三角波互补PWM输出示例

(6) 具有自动死区时间设置的三相不对称三角波互补PWM输出

图23.66显示了一个示例，其中三个通道在三角波PWM模式3下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCA设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在循环结束时保留输出。GTIOCB设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在循环结束时保留输出。

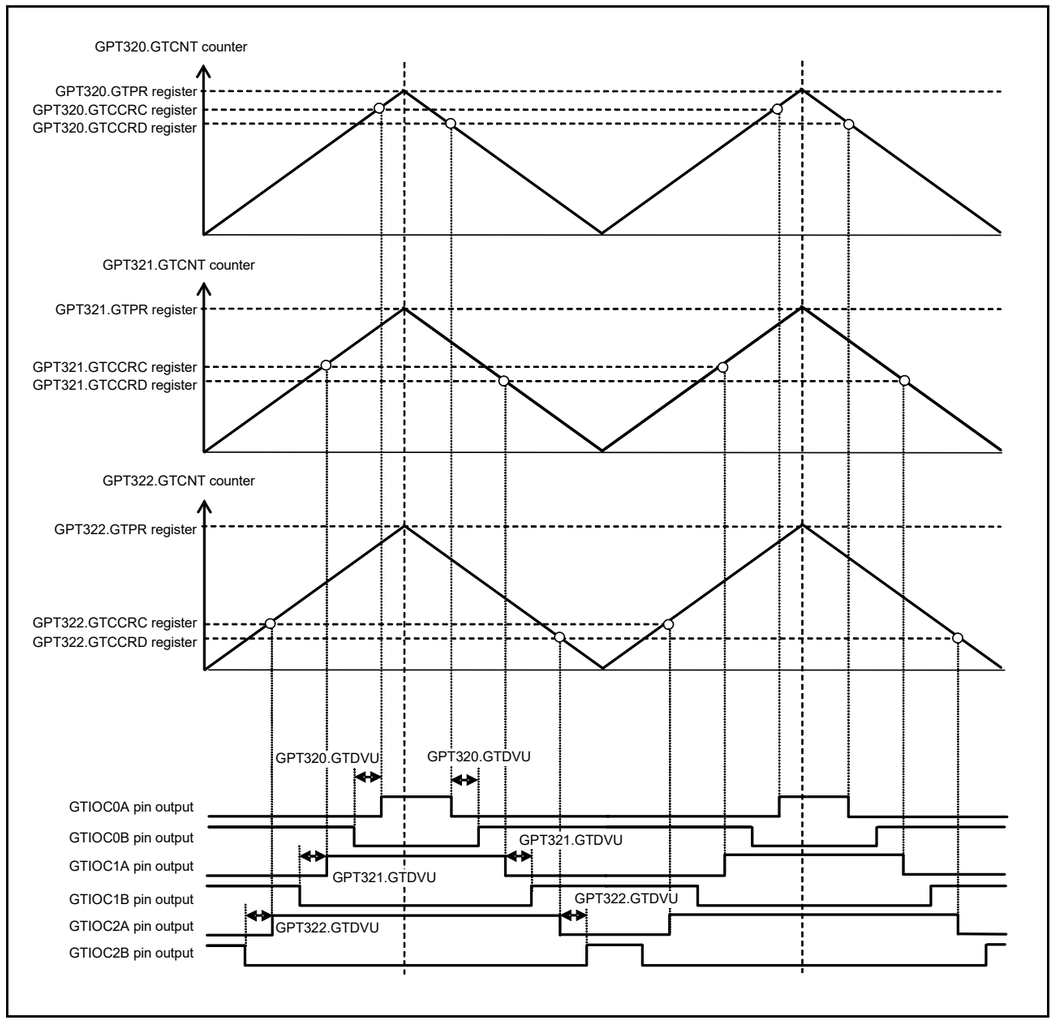


Figure 23.66 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

23.3.10 Phase Counting Function

The phase difference between the GTIOCA and GTIOCB pin inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCA and GTIOCB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 23.3.1.1, Counter operation.

Figure 23.67 to Figure 23.76 show phase counting modes 1 to 5. Table 23.7 to Table 23.16 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers.

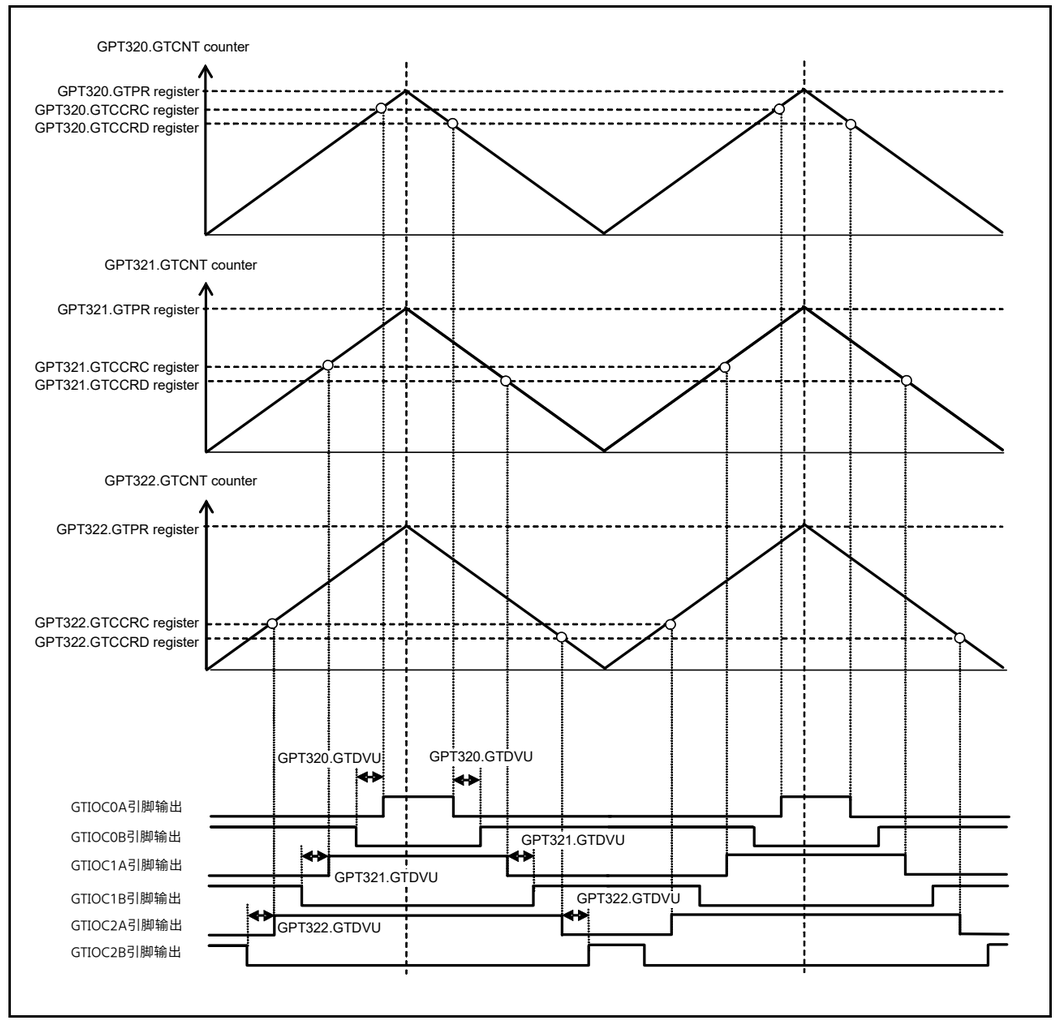


Figure 23.66 具有自动死区时间设置的三相不对称三角波互补PWM输出示例

23.3.10 相位计数功能

检测到GTIOCA和GTIOCB引脚输入之间的相位差，并且相关的GTCNT向上计数或向下计数。可检测的相位差可与在GTUPSR和GTDNSR寄存器中设置的GTIOCA和GTIOCB引脚输入的边沿和电平之间的关系任意组合。有关计数操作的详细信息，请参阅第23.3.1.1节，计数器操作。

图23.67至图23.76显示了相位计数模式1至5。表23.7至表23.16显示了向上计数或向下计数的条件以及GTUPSR和GTDNSR寄存器的列表设置。

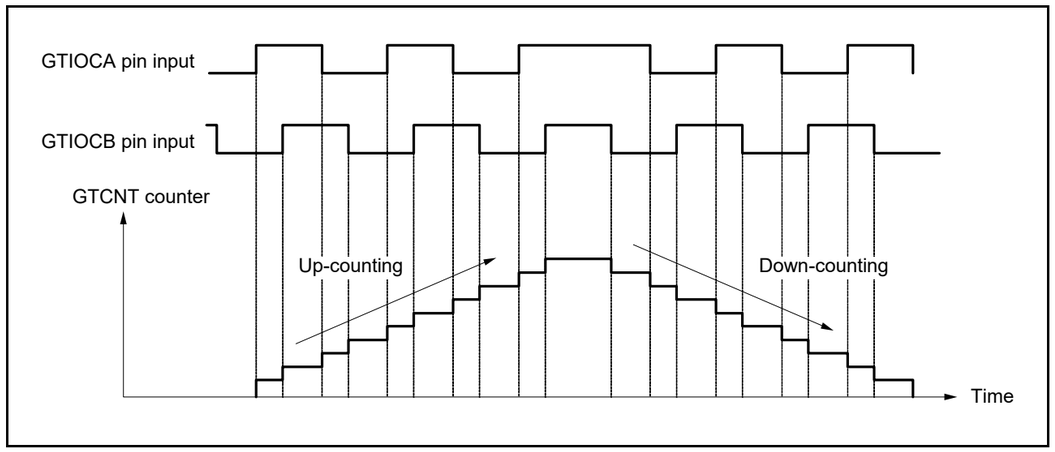


Figure 23.67 Example of phase counting mode 1

Table 23.7 Conditions of up-counting/down-counting in phase counting mode 1

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0000 6900h GTDNSR = 0000 9600h
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

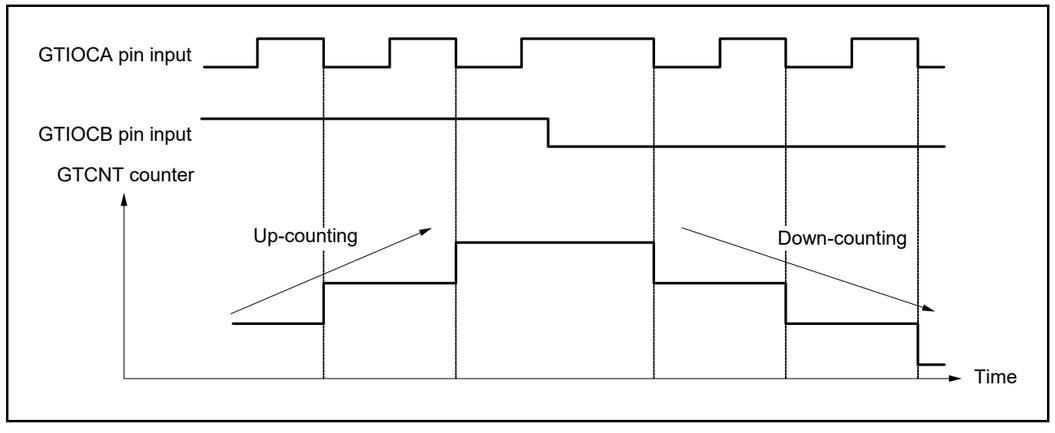


Figure 23.68 Example of phase counting mode 2 (A)

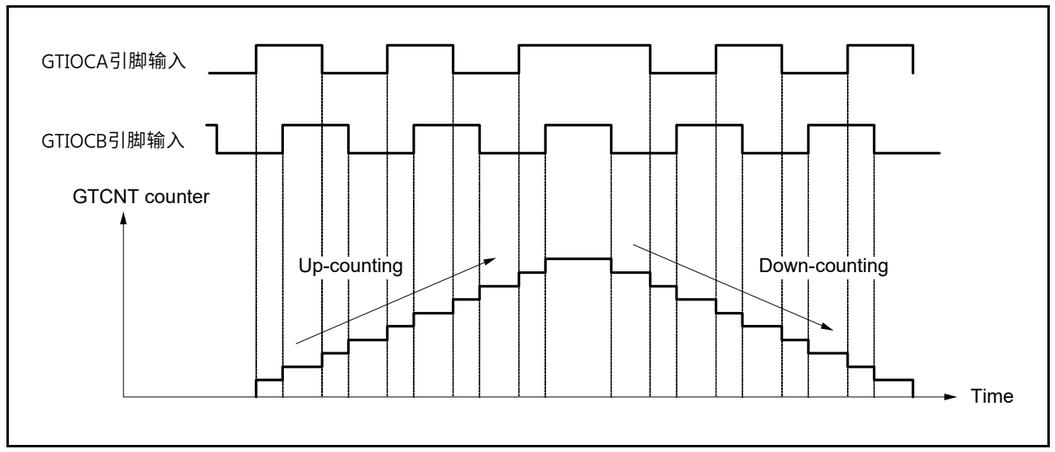


Figure 23.67 相位计数模式示例1

Table 23.7 相位计数模式加减计数条件1

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0000 6900h GTDNSR = 0000 9600h
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

↑ :上升沿

↓ :下降沿

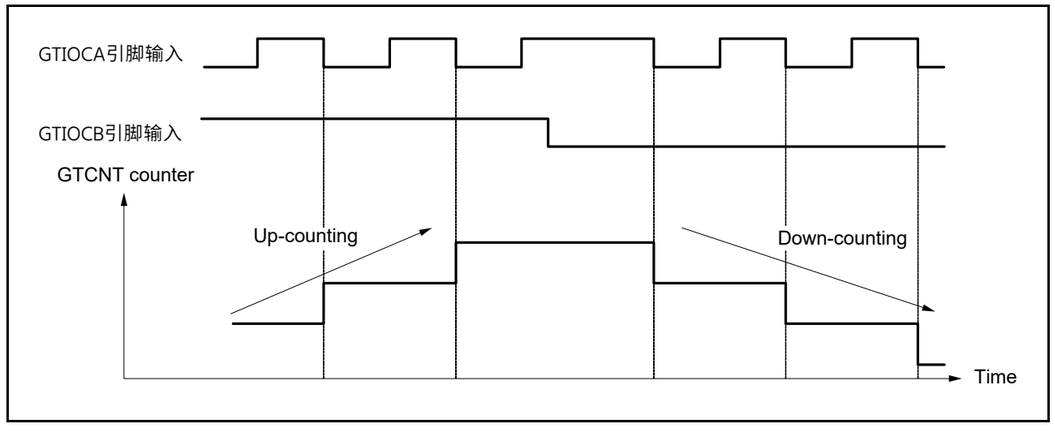


Figure 23.68 相位计数模式示例2(A)

Table 23.8 Conditions of up-counting/down-counting in phase counting mode 2 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 0400h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Down-counting	

↑ : Rising edge

↓ : Falling edge

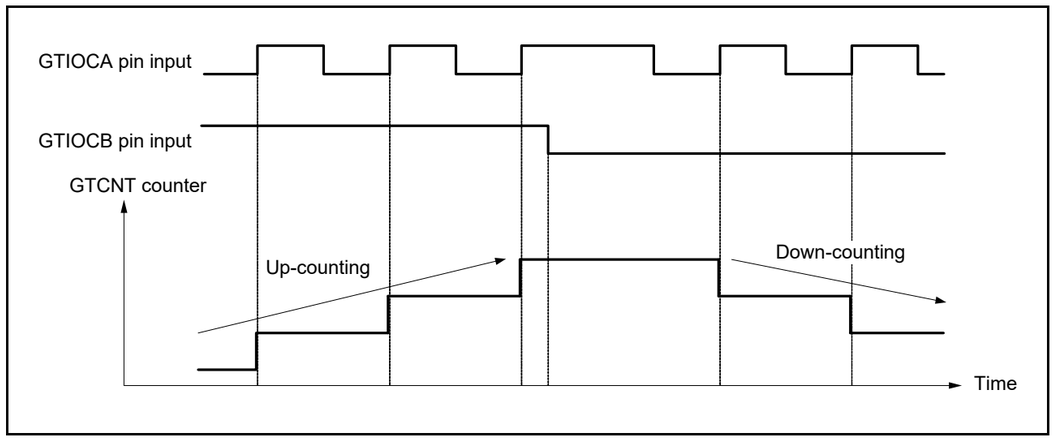


Figure 23.69 Example of phase counting mode 2 (B)

Table 23.9 Conditions of up-counting/down-counting in phase counting mode 2 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0200h GTDNSR = 0000 0100h
Low	↓		
↑	Low	Down-counting	
↓	High	Don't care	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

Table 23.8 相位计数模式2(A)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 0400h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Down-counting	

↑ :上升沿

↓ :下降沿

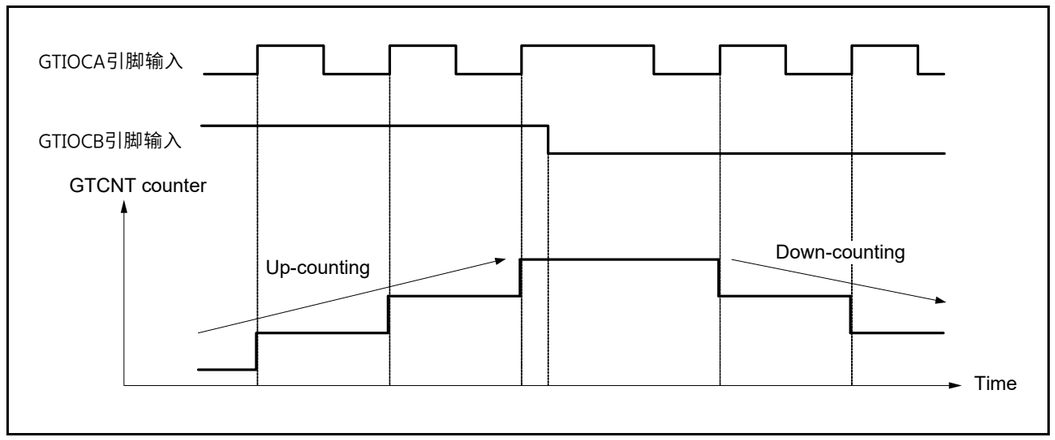


Figure 23.69 相位计数模式示例2(B)

Table 23.9 相位计数模式2(B)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Don't care	GTUPSR = 0000 0200h GTDNSR = 0000 0100h
Low	↓		
↑	Low	Down-counting	
↓	High	Don't care	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ :上升沿

↓ :下降沿

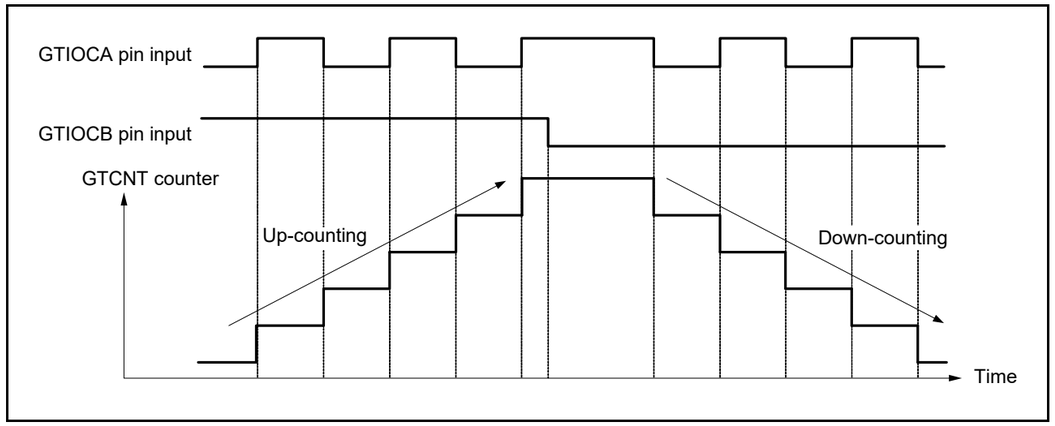


Figure 23.70 Example of phase counting mode 2 (C)

Table 23.10 Conditions of up-counting/down-counting in phase counting mode 2 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0A00h GTDNSR = 0000 0500h
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

↑ : Rising edge

↓ : Falling edge

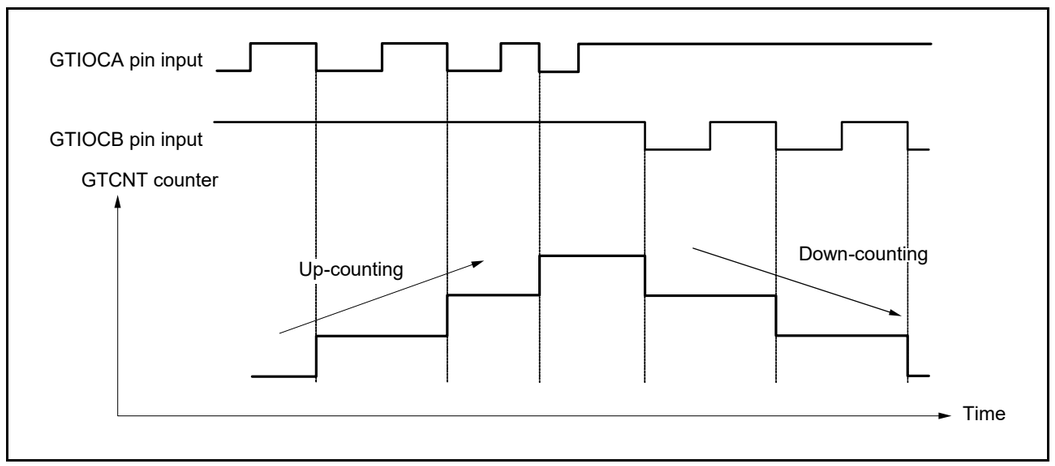


Figure 23.71 Example of phase counting mode 3 (A)

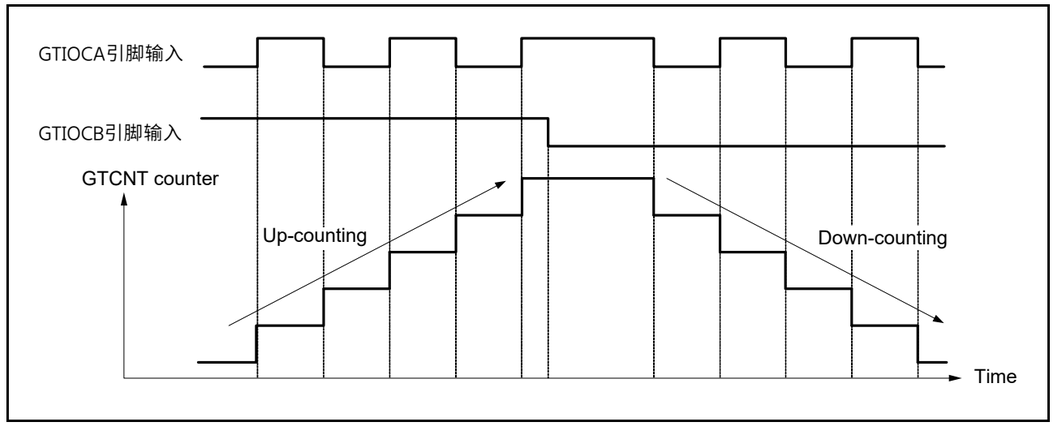


Figure 23.70 相位计数模式示例2(C)

Table 23.10 相位计数模式2(C)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Don't care	GTUPSR = 0000 0A00h GTDNSR = 0000 0500h
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	不在乎	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

↑ :上升沿

↓ :下降沿

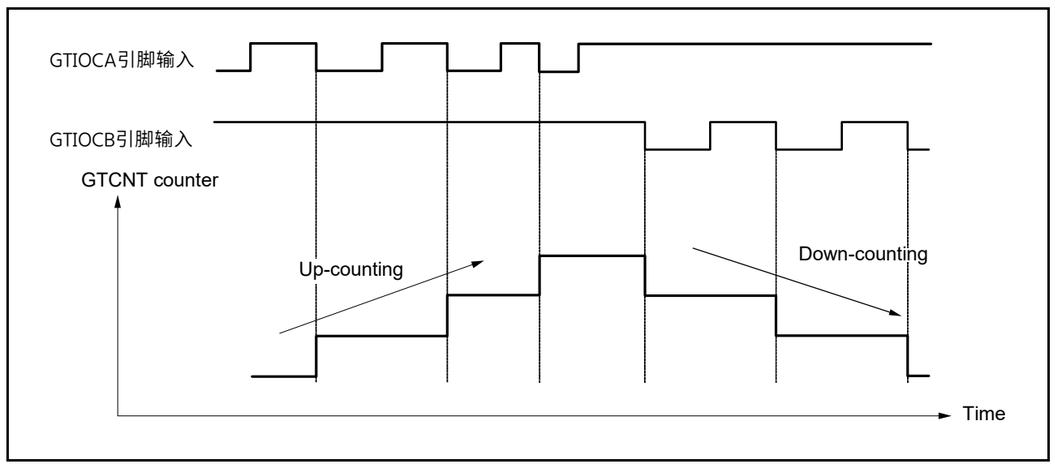


Figure 23.71 相位计数模式示例3(A)

Table 23.11 Conditions of up-counting/down-counting in phase counting mode 3 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 8000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

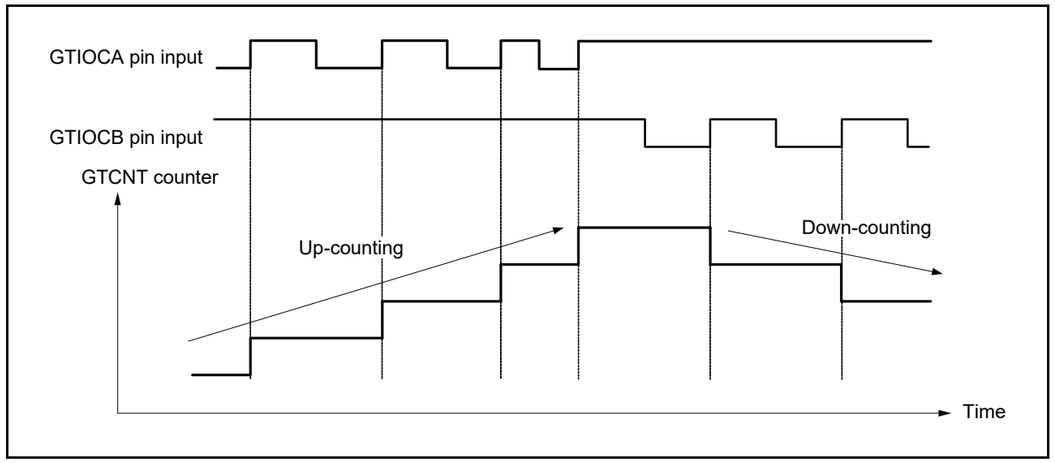


Figure 23.72 Example of phase counting mode 3 (B)

Table 23.12 Conditions of up-counting/down-counting in phase counting mode 3 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0000 0200h GTDNSR = 0000 2000h
Low	↓	Don't care	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

Table 23.11 相位计数模式3(A)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 8000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ :上升沿

↓ :下降沿

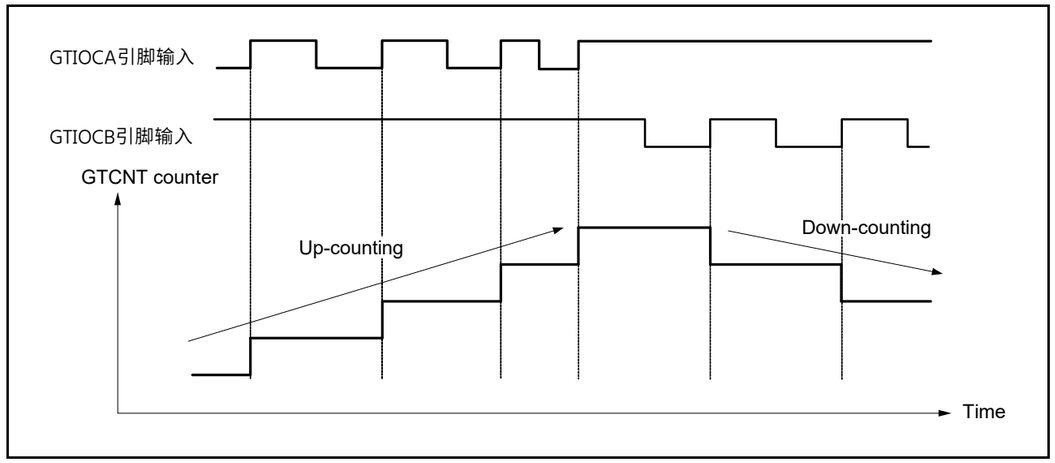


Figure 23.72 相位计数模式示例3(B)

Table 23.12 相位计数模式3(B)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0000 0200h GTDNSR = 0000 2000h
Low	↓	Don't care	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Don't care	

↑ :上升沿

↓ :下降沿

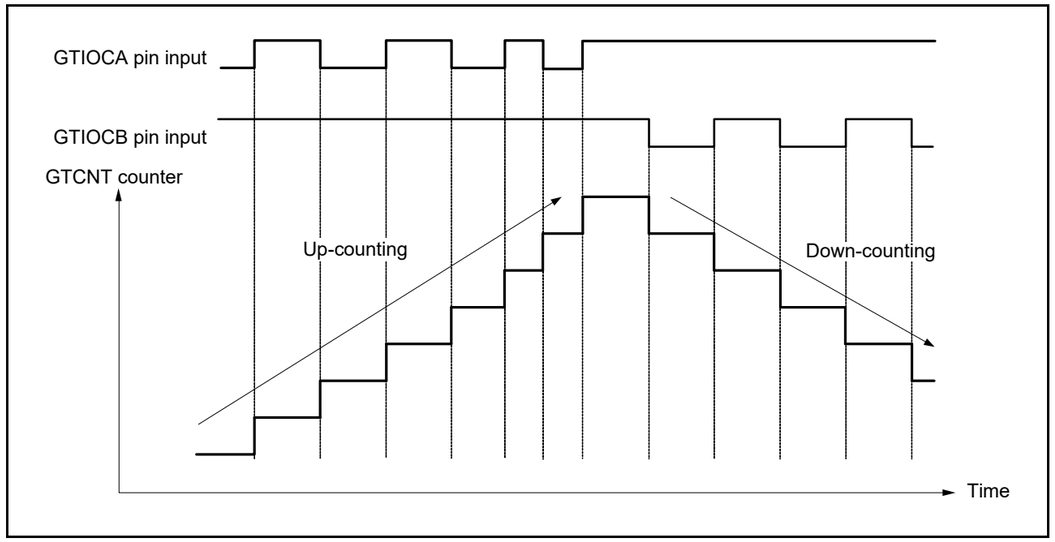


Figure 23.73 Example of phase counting mode 3 (C)

Table 23.13 Conditions of up-counting/down-counting in phase counting mode 3 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0000 0A00h GTDNSR = 0000 A000h
Low	↑	Don't care	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High	Up-counting	
↓	Low	Don't care	

↑ : Rising edge

↓ : Falling edge

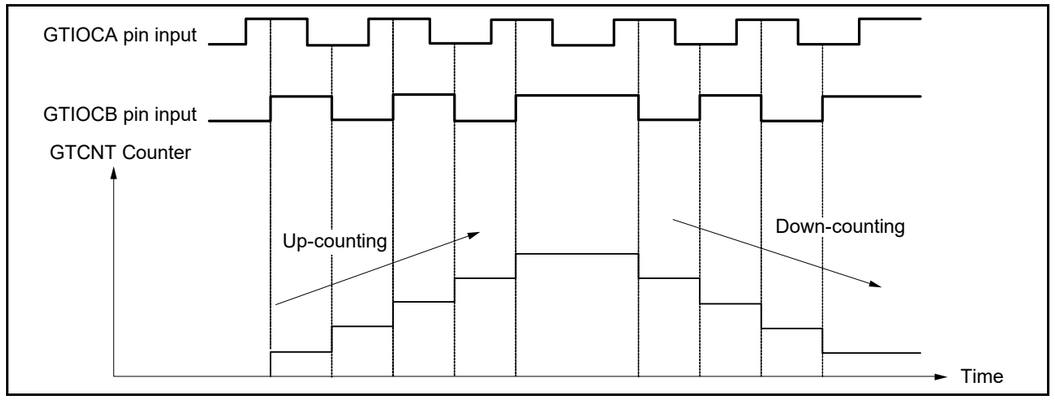


Figure 23.74 Example of phase counting mode 4

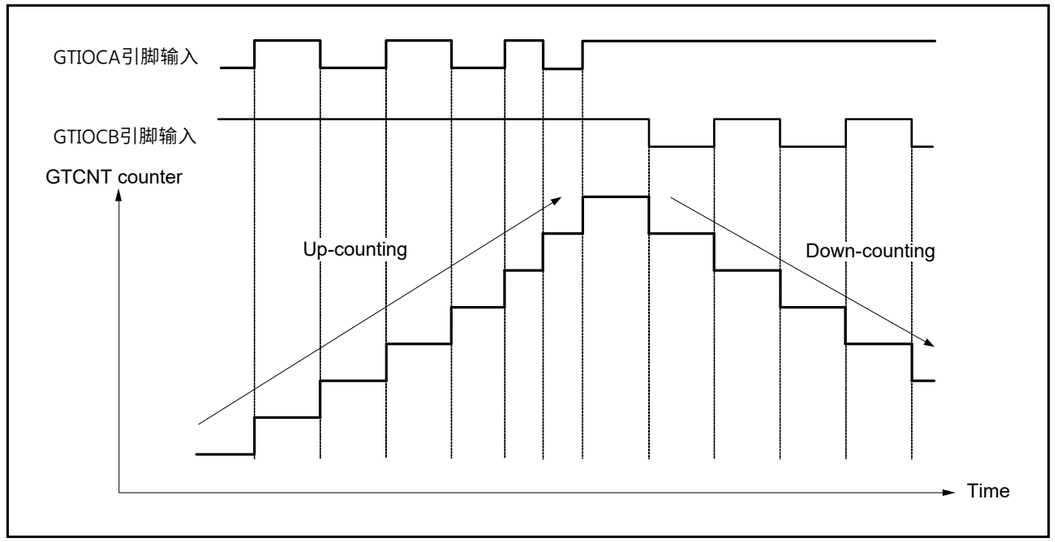


Figure 23.73 相位计数模式示例3(C)

Table 23.13 相位计数模式3(C)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0000 0A00h GTDNSR = 0000 A000h
Low	↑	Don't care	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Don't care	
↑	High	Up-counting	
↓	Low	Don't care	

↑ :上升沿

↓ :下降沿

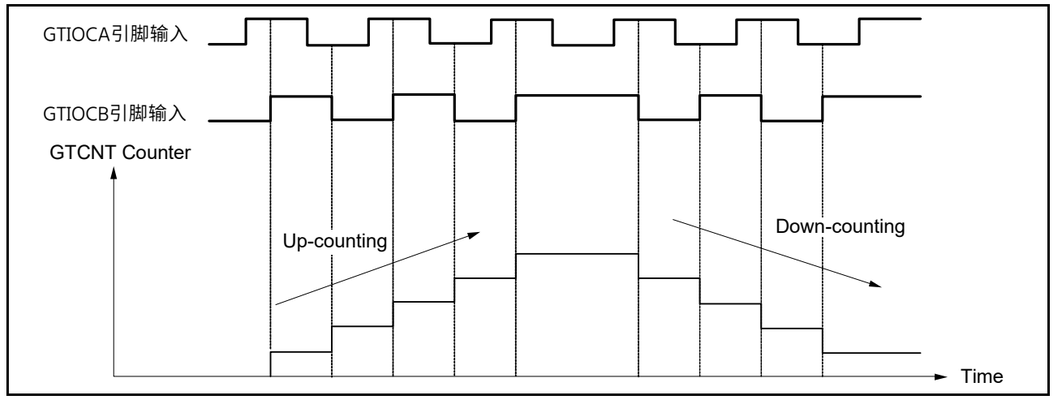


Figure 23.74 相位计数模式示例4

Table 23.14 Conditions of up-counting/down-counting in phase counting mode 4

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0000 6000h GTDNSR = 0000 9000h
Low	↓		
↑	Low	Don't care	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Don't care	
↓	Low		

↑ : Rising edge

↓ : Falling edge

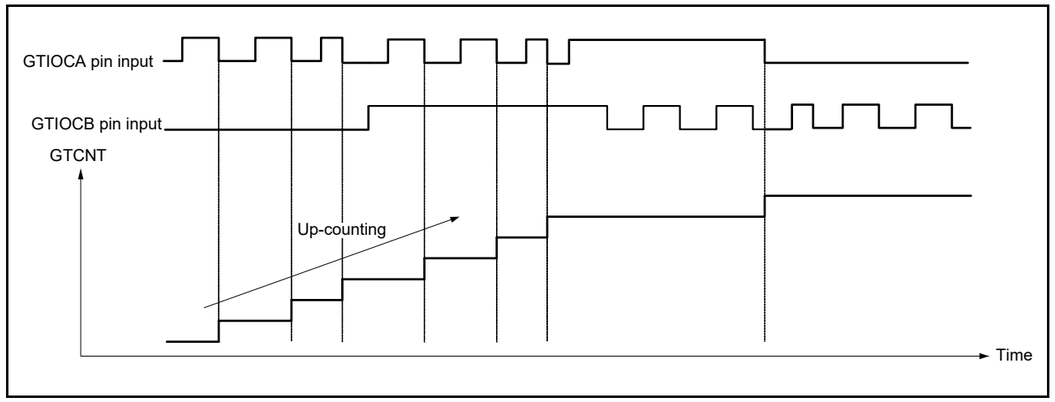


Figure 23.75 Example of phase counting mode 5 (A)

Table 23.15 Conditions of up-counting/down-counting in phase counting mode 5 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Up-counting	

↑ : Rising edge

↓ : Falling edge

Table 23.14 相位计数方式4加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0000 6000h GTDNSR = 0000 9000h
Low	↓		
↑	Low	Don't care	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Don't care	
↓	Low		

↑ :上升沿

↓ :下降沿

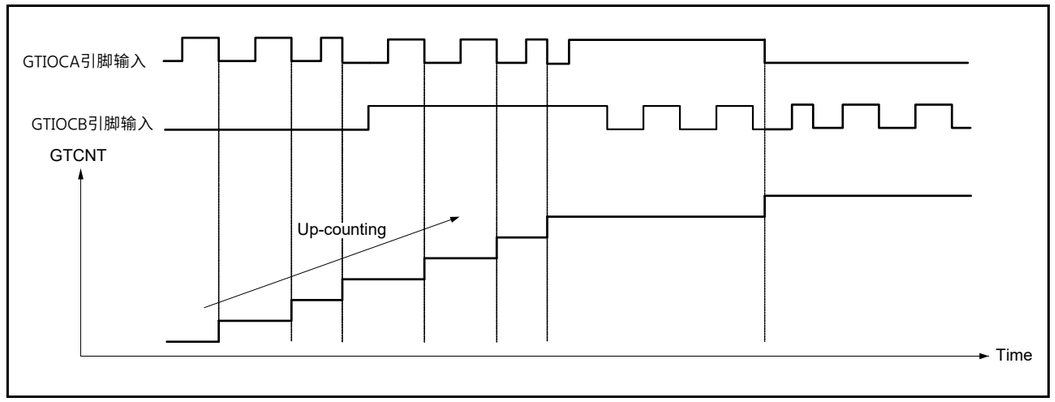


Figure 23.75 相位计数模式示例5(A)

Table 23.15 相位计数模式下加减计数条件5（A）

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Don't care	
Low	↑		
↑	High		
↓	Low	Up-counting	

↑ :上升沿

↓ :下降沿

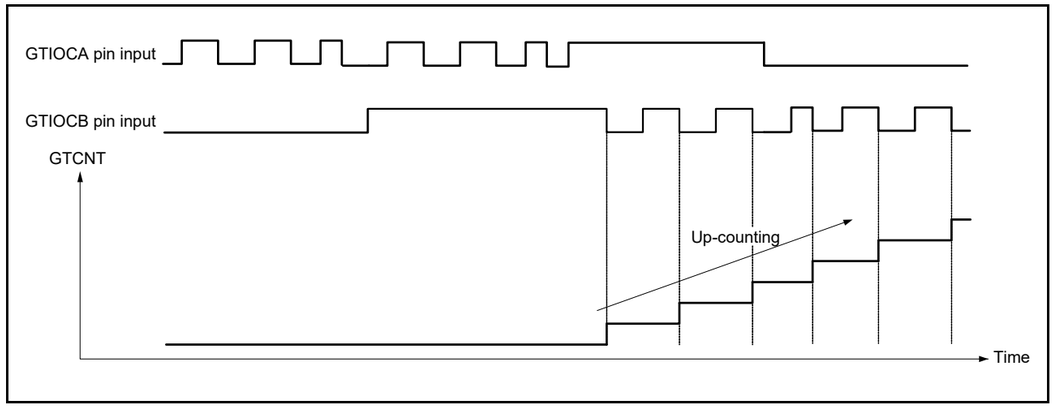


Figure 23.76 Example of phase counting mode 5 (B)

Table 23.16 Conditions of up-counting/down-counting in phase counting mode 5 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
High	↑	Don't care	GTUPSR = 0000 C000h GTDNSR = 0000 0000h
Low	↓	Up-counting	
↑	Low	Don't care	
↓	High		
High	↓	Up-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ : Rising edge

↓ : Falling edge

23.3.11 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT320.GTIOCA.

Figure 23.77 shows the GPT_OPS control flow conceptual diagram.

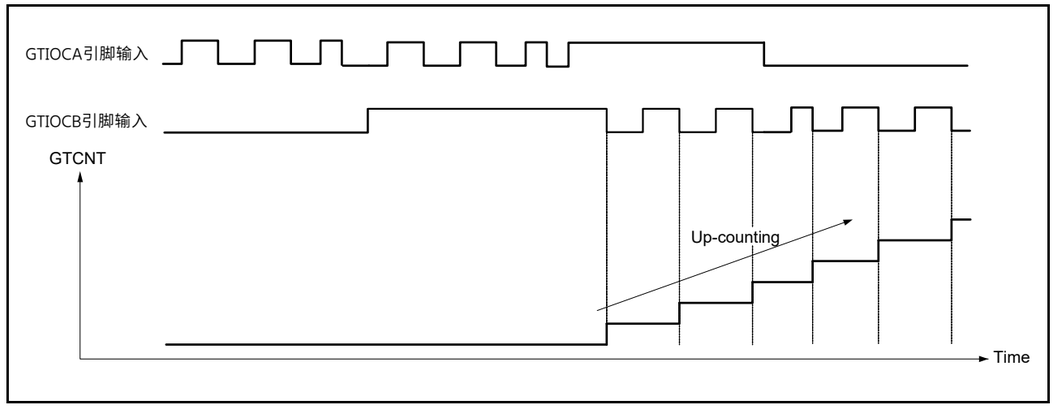


Figure 23.76 相位计数模式示例5(B)

Table 23.16 相位计数模式下加减计数条件5(B)

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
High	↑	Don't care	GTUPSR = 0000 C000h GTDNSR = 0000 0000h
Low	↓	Up-counting	
↑	Low	Don't care	
↓	High		
High	↓	Up-counting	
Low	↑	Don't care	
↑	High		
↓	Low		

↑ :上升沿

↓ :下降沿

23.3.11 输出相位切换(GPT_OPS)

GPT_OPS提供使用输出相位切换轻松控制无刷直流电机运行的功能
控制寄存器(OPSCR)。

GPT_OPS输出用于斩波控制的PWM信号或6相电机控制的每一相（U正相负相、V正相负相、W正相负相）的电平信号。该功能使用软件设置的软设置值（OPSCR.UF、VF、WF）或霍尔元件检测到的外部信号，GPT320.GTIOCA的PWM波形。

图23.77显示了GPT_OPS控制流概念图。

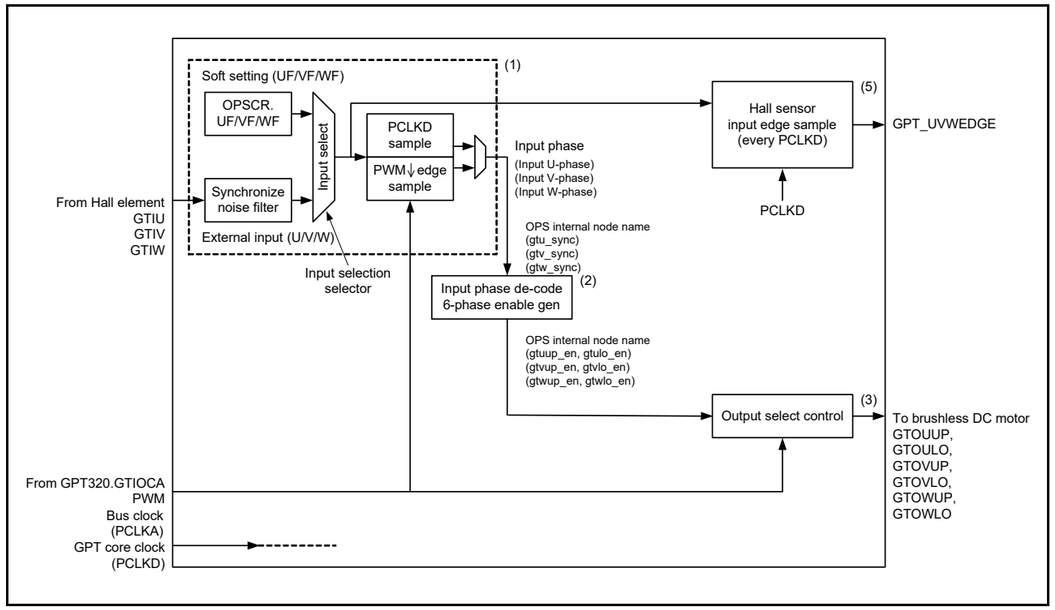


Figure 23.77 Conceptual diagram of GPT_OPS control flow

Figure 23.78 shows a 6-phase level signals output example of a GPT_OPS operation.

The GPT_UVWEDGE signal in Figure 23.78 is the Hall sensor input edge to ELC output.

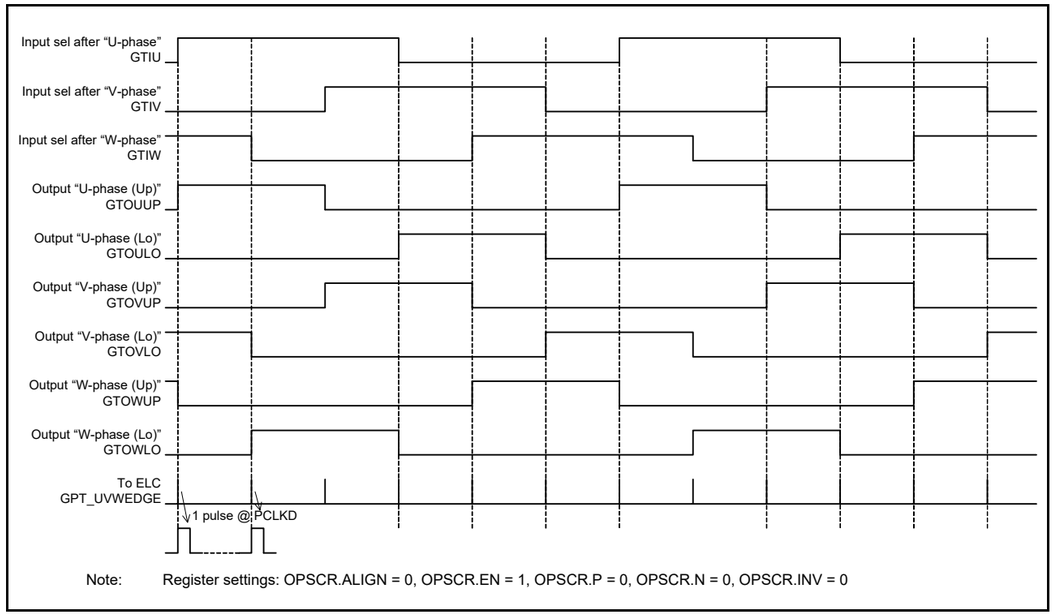


Figure 23.78 Example of 6-phase level output operation

Figure 23.79 shows a 6-phase PWM output example of a GPT_OPS operation with chopper control.

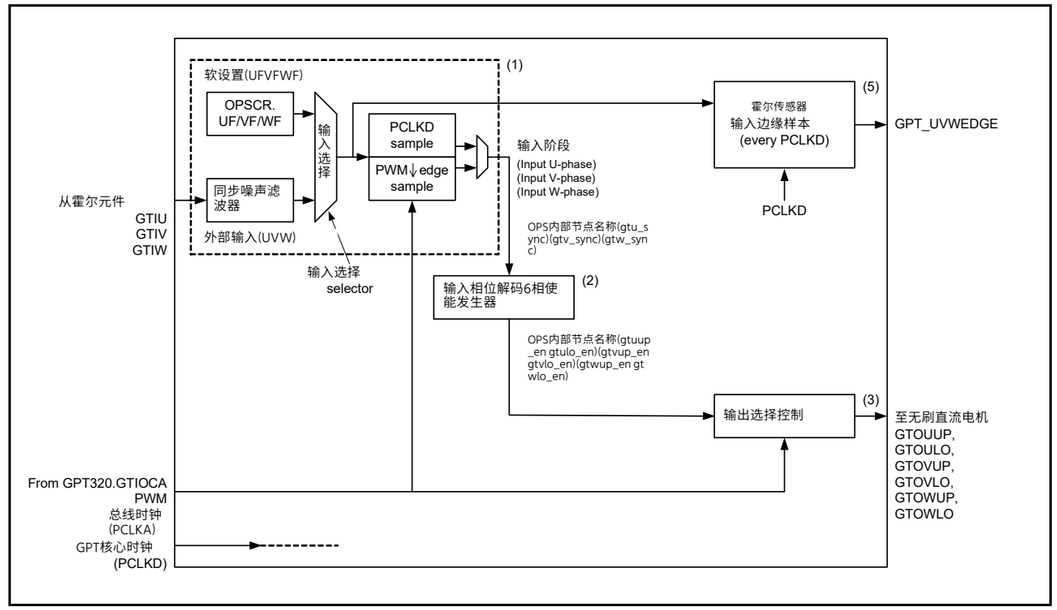


Figure 23.77 GPT_OPS控制流程概念图

图23.78显示了GPT_OPS操作的6相电平信号输出示例。

图23.78中的GPT_UVWEDGE信号是霍尔传感器输入边沿到ELC输出。

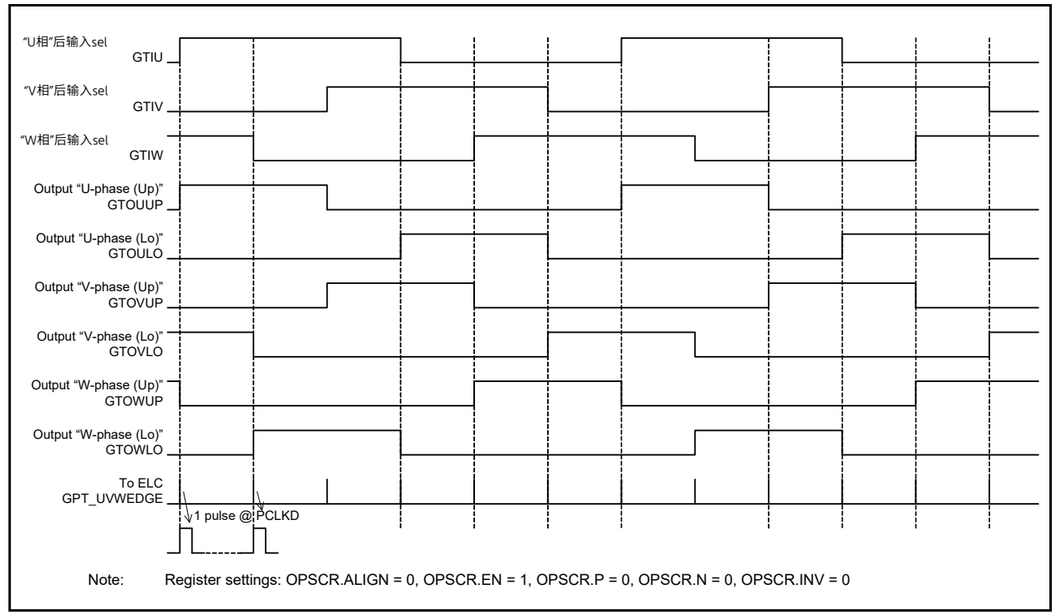


Figure 23.78 6相电平输出动作示例

图23.79显示了带斩波器控制的GPT_OPS操作的6相PWM输出示例。

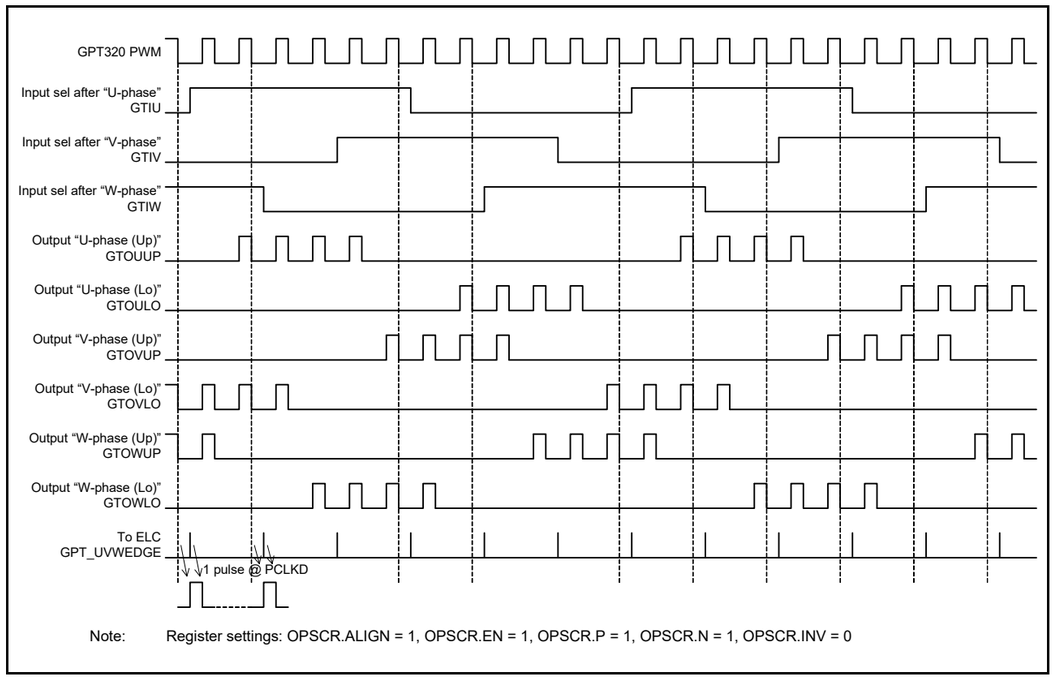


Figure 23.79 Example of 6-phase PWM output operation with chopper control

Figure 23.80 shows an example of output disable control (6-phase PWM output operation).

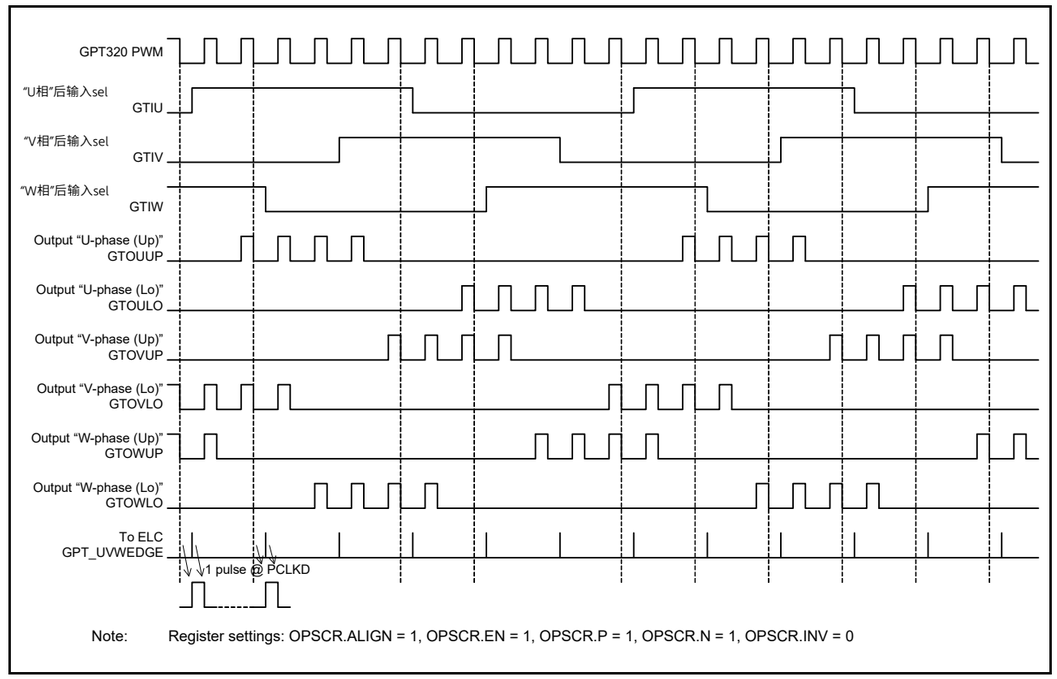


Figure 23.79 带斩波器控制的6相PWM输出操作示例

图23.80显示了输出禁用控制的示例（6相PWM输出操作）。

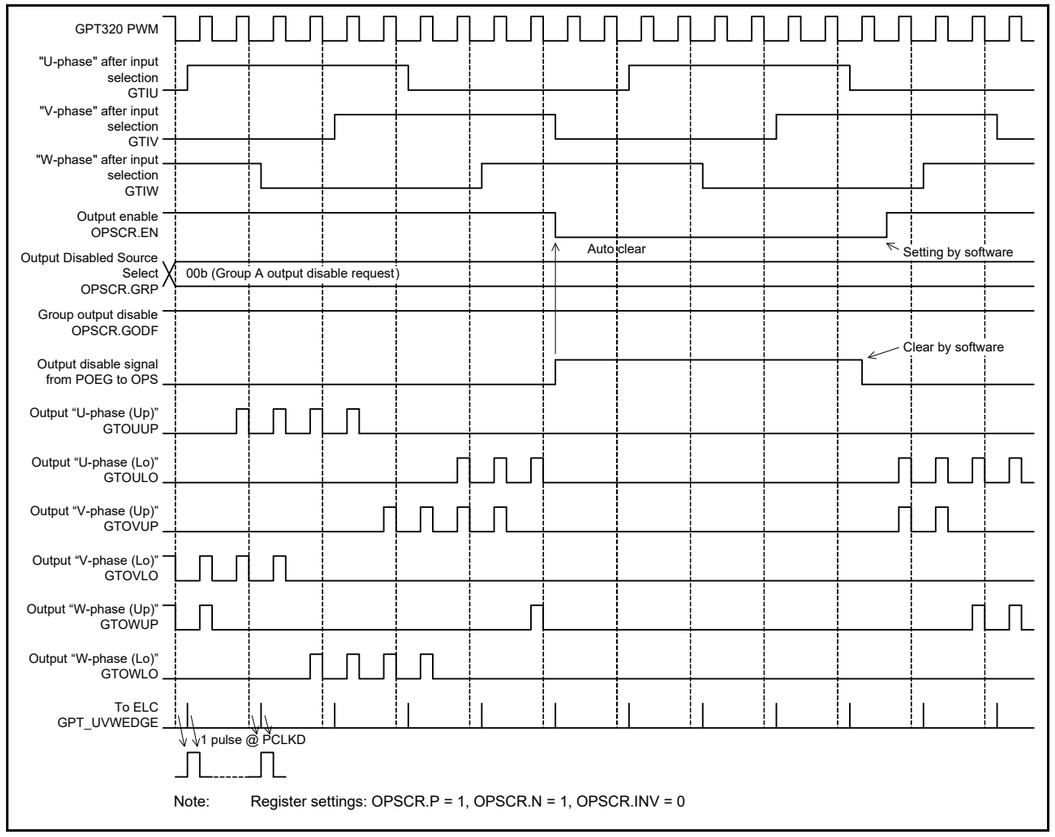


Figure 23.80 Example of group output disable control operation

23.3.11.1 Input selection and synchronization of external input signal

In the GPT_OPS control flow conceptual diagram shown in Figure 23.77, (1) is a selection of input phase from software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit is 0, select the external input. Enable the input signal after synchronization with the GPT core clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT320.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit is 1.

When OPSCR.FB bit is 1, select the soft setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT320.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit is 1.

When OPSCR.ALIGN bit is 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit is 0 or OPSCR.FB bit is 1. However, in some situations, the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before or just after) is shortened.

Table 23.17 shows the input selection process and setting of associated OPSCR bits.

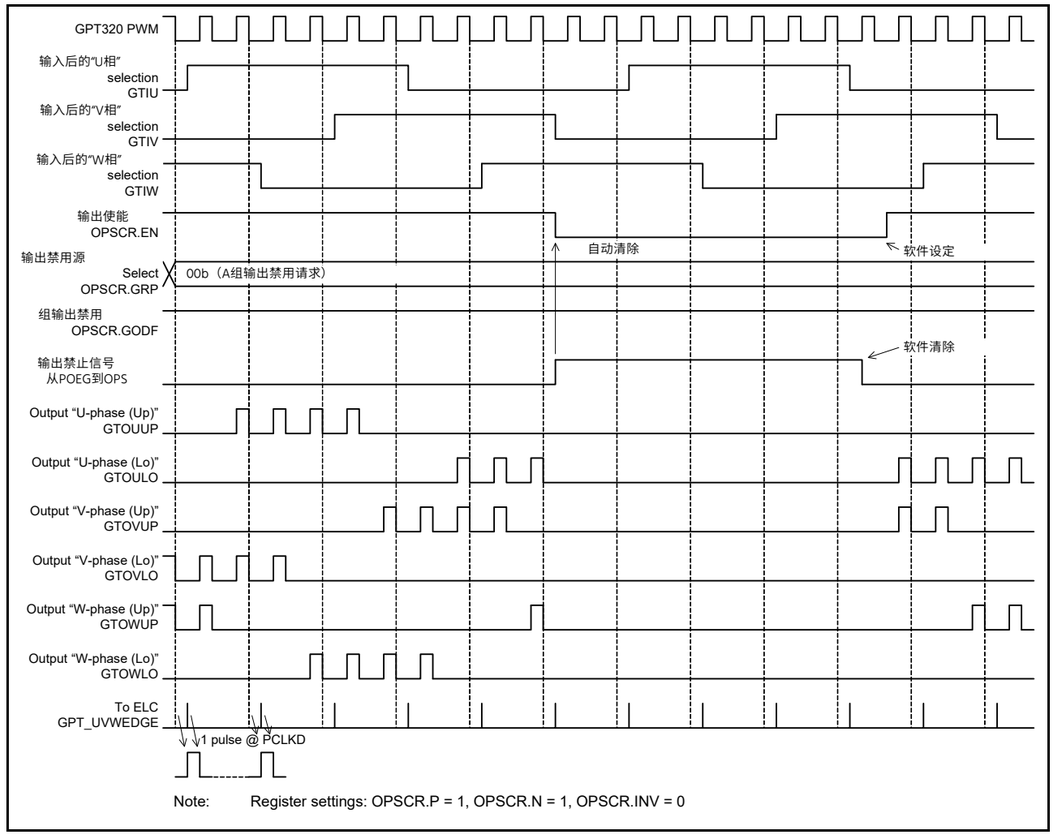


Figure 23.80 组输出禁用控制操作示例

23.3.11.1 外部输入信号的输入选择和同步

在图23.77所示的GPT_OPS控制流程概念图中，(1)是通过OPSCR.FB位从软件设置和外部输入中选择输入相位。

当OPSCR.FB位为0时，选择外部输入。与GPT内核时钟(PCLKD)同步后启用输入信号。进行噪声过滤（可选）后，将外部输入设置为PWM的输入相位（GPT320.GTIOCA的PWM）使用下降沿采样，且OPSCR.ALIGN位为1。

当OPSCR.FB位为1时，使用OPSCR.ALIGN位的下降沿采样的PWM（GPT320.GTIOCA的PWM）输入相位的值为1来选择软设置（OPSCR.UF、VF、WF）。

当OPSCR.ALIGN位为0时，GPT_OPS以PCLKD同步的输入相位与任一OPSCR.FB位为0或OPSCR.FB位为1。但是，在某些情况下，开关时序（恰好之前或之后）的输出UVW相位（PWM输出模式）的PWM脉冲宽度会缩短。

表23.17显示了输入选择过程和相关OPSCR位的设置。

Table 23.17 Input selection processing method

OPSCR register		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD synchronization + falling edge sample)	Input Phase Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD synchronization + through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of falling edge sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD synchronization)	

23.3.11.2 Input sampling

The OPSCR.U, V, W bits indicate the PCLKD sampling results of the input selected by the OPSCR.FB bit.

When OPSCR.FB bit is 0 and after synchronization with the GPT core clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits indicate the sampling results of the external input. When OPSCR.FB bit is 1, OPSCR.U, V, W bits have the value (OPSCR.UF, VF, WF) of the soft setting.

23.3.11.3 Input phase decode

In the GPT_OPS control flow conceptual diagram shown in Figure 23.77, (2) enables the 6-phase signals by decoding the input phase selected by the OPSCR.FB bit. The 6-phase enable signal is used for internal processing of GPT_OPS.

Table 23.18 shows the decode table of input phase.

Table 23.18 Decode table of input phase

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-phase	Input V-phase	Input W-phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

23.3.11.4 Output selection control

In the GPT_OPS control flow conceptual diagram in Figure 23.77, (3) represents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P and OPSCR.N bits can select from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to positive logic or negative logic by the OPSCR.INV bit.

Table 23.19 and Table 23.20 show the output selection control method using the OPSCR register bit.

Table 23.17 输入选择处理方法

OPSCR register		输入相位采样方式的选择（UVW−phase）	同步输入输出选择过程（GPT_OPS内部节点名）
FB bit	对齐位		
0	1	PWM下降沿采样的外部输入（PCLKD同步+下降沿采样）	输入相位 Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	PCLKD同步输出端的外部输入（PCLKD同步+直通模式）	
1	1	PWM下降沿采样的软件设置（下降沿采样的OPSCR.UF、VF、WF）	
	0	软件设置值选择（=OPSCR.UFVFWF值）（=PCLKD同步）	

23.3.11.2 输入采样

OPSCR.U、V、W位指示由OPSCR.FB位选择的输入的PCLKD采样结果。

当OPSCR.FB位为0并与GPT内核时钟(PCLKD)和噪声过滤（可选）同步后，
OPSCR.U、V、W位表示外部输入的采样结果。当OPSCR.FB位为1时，OPSCR.U、V、W位具有软设置的值（OPSCR.UF、VF、WF）。

23.3.11.3 输入相位解码

在图23.77所示的GPT_OPS控制流程概念图中，(2)通过解码OPSCR.FB位选择的输入相位来启用6相信号。6相使能信号用于GPT_OPS的内部处理。

表23.18显示了输入相位的解码表。

Table 23.18 输入相位解码表

输入相位(UVW)（GPT_OPS内部节点名称）			6−phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
输入U相	输入V相	输入W相	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

23.3.11.4 输出选择控制

在图23.77的GPT_OPS控制流程概念图中，(3)表示通过设置OPSCR寄存器位来选择输出波形。

对于输出选择，以下位是相关的：

- OPSCR.EN位控制是输出6相输出，还是停止
- OPSCR.P和OPSCR.N位可以选择输出相位的电平信号或PWM信号（斩波器输出）
- 输出相位的极性可通过OPSCR.INV位设置为正逻辑或负逻辑。

表23.19和表23.20显示了使用OPSCR寄存器位的输出选择控制方法。

Table 23.19 Output selection control method (positive phase)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtuup_en) (gtvup_en) (gtwup_en)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_en) (~gtvup_en) (~gtwup_en)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM Output Mode (Positive phase) (Negative logic)

Table 23.20 Output selection control method (negative phase)

Enable-phase output control	Negative-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtulo_en) (gtvlo_en) (gtwlo_en)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_en) (~gtvlo_en) (~gtwlo_en)	Level Output Mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM Output Mode (Negative phase) (Negative logic)

Table 23.19 输出选择控制方式（正相）

使能相位输出控制	正相输出(P)控制	反相输出控制	输出端口名称（正相=向上）（输出选择内部节点分配）	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS→0输出
1	0	0	电平信号(gtuup_en)(gtvup_en)(gtwup_en)	电平输出模式（正相）（正逻辑）
1	0	1	电平信号(~gtuup_en)(~gtvup_en)(~gtwup_en)	电平输出模式（正相）（负逻辑）
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM输出模式（正相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM输出模式（正相）（负逻辑）

Table 23.20 输出选择控制方式（负相）

使能相位输出控制	负相输出(N)控制	反相输出控制	输出端口名称（负相=Lo）（输出选择内部节点分配）	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS→0输出
1	0	0	电平信号(gtulo_en)(gtvlo_en)(gtwlo_en)	电平输出模式（负相）（正逻辑）
1	0	1	电平信号(~gtulo_en)(~gtvlo_en)(~gtwlo_en)	电平输出模式（负相）（负逻辑）
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM输出模式（负相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM输出模式（负相）（负逻辑）

23.3.11.5 Output selection control (group output disable function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high (output disable request), the GPT_OPS output pins are changed to Hi-Z asynchronously and the OPSCR.EN bit is set to 0 by the output disable request signal synchronized with PCLKD. For the return, set the OPSCR.EN to 1 after clearing the output disable request with software.

The timing of the OPSCR.EN bit cleared to 0 is 3 PCLKD cycles after generating the output disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated. For an example of the operation of group output disable control, see Figure 23.80.

23.3.11.6 Event Link Controller (ELC) output

In the GPT_OPS control flow conceptual diagram shown in Figure 23.77, (5) outputs the Hall sensor input signal edge to the ELC.

The Hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase of the input phase is short in duration, the Hall sensor edge input signal is not output at that time.

When the OPSCR.FB bit is 0, the Hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit is 1, the Hall sensor input edge signal is the logical OR of the edge of the soft setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 23.78 to Figure 23.80 for examples of the output signal to the ELC.

23.3.11.5 输出选择控制（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP[1:0]位选择的信号值为高（输出禁用请求）时，GPT_OPS输出引脚异步更改为Hi-Z并且OPSCR.EN位设置为0通过与PCLKD同步的输出禁用请求信号。对于返回，请在用软件清除输出禁用请求后将OPSCR.EN设置为1。

OPSCR.EN位清零的时序是在产生输出禁用请求后的3个PCLKD周期。为了可靠地执行输出禁用控制，在生成输出禁用请求后（通过清除POEG中的输出禁用请求标志）至少允许4个PCLKD周期，直到输出禁用请求终止。组输出禁用控制的操作示例见图23.80。

23.3.11.6 事件链接控制器(ELC)输出

在图23.77所示的GPT_OPS控制流程概念图中，(5)将霍尔传感器输入信号沿输出到ELC。

霍尔传感器输入边沿信号是在PCLKD采样的每个U相V相W相输入的上升沿和下降沿信号的逻辑或。也就是说，如果输入相的U相V相W相中的每一个的高电平时段持续时间短，则此时不输出霍尔传感器边沿输入信号。

当OPSCR.FB位为0时，霍尔传感器输入边沿信号为在PCLKD采样的外部输入相位边沿信号的逻辑或。

当OPSCR.FB位为1时，霍尔传感器输入边沿信号为软设置边沿的逻辑或（OPSCR.UF，VF，WF）在PCLKD采样。

有关ELC的输出信号示例，请参见图23.78至图23.80。

23.3.11.7 GPT_OPS start operation setting flow

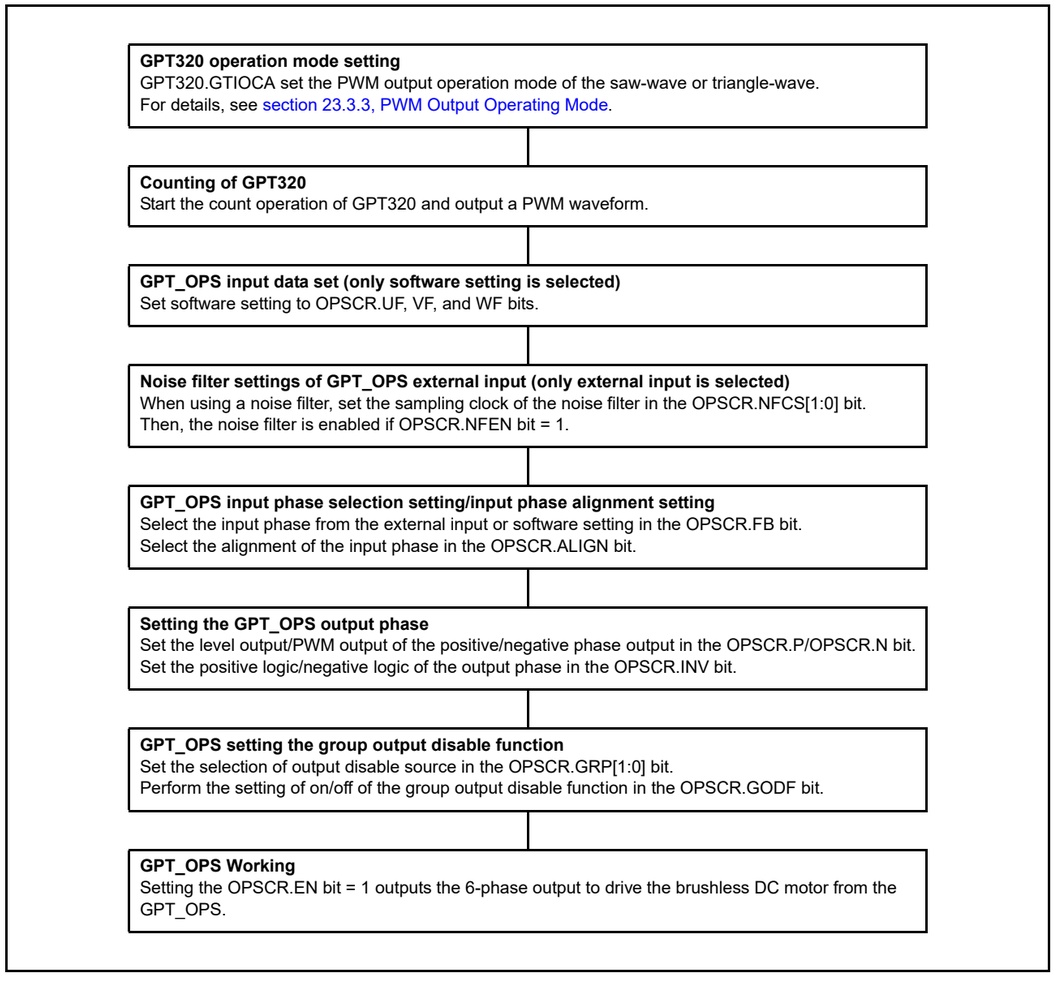


Figure 23.81 Example setting of GPT_OPS start operation

23.4 Interrupt Sources

23.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTCNT counter overflow (GTPR compare match)/underflow.

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. Table 23.21 lists the GPT interrupt sources.

23.3.11.7 GPT_OPS启动操作设置流程

Figure 23.81 GPT_OPS启动操作的示例设置

23.4 中断源

23.4.1 中断源

GPT提供以下中断源：

- GTCCR输入捕获比较匹配
- GTCNT计数器上溢（GTPR比较匹配）下溢。

每个中断源都有自己的状态标志。当产生中断源信号时，GTST中的相关状态标志设置为1。GTST中的相关状态标志可以通过写入0来清除。如果标志设置和标志清除同时发生，则标志清除优先于标志放。这些标志由内部状态自动更新。表23.21列出了GPT中断源。

Table 23.21 Interrupt sources (1 of 2)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
0	GPT0_CCMPA	GPT320.GTCCRA input capture/compare match	TCFA	Possible
	GPT0_CCMPB	GPT320.GTCCRB input capture/compare match	TCFB	Possible
	GPT0_CMPC	GPT320.GTCCRC compare match	TCFC	Possible
	GPT0_CMPD	GPT320.GTCCRD compare match	TCFD	Possible
	GPT0_CMPE	GPT320.GTCCRE compare match	TCFE	Possible
	GPT0_CMPF	GPT320.GTCCRF compare match	TCFF	Possible
	GPT0_OVF	GPT320.GTCNT overflow (GPT320.GTPR compare match)	TCFPO	Possible
	GPT0_UDF	GPT320.GTCNT underflow	TCFPU	Possible
1	GPT1_CCMPA	GPT321.GTCCRA input capture/compare match	TCFA	Possible
	GPT1_CCMPB	GPT321.GTCCRB input capture/compare match	TCFB	Possible
	GPT1_CMPC	GPT321.GTCCRC compare match	TCFC	Possible
	GPT1_CMPD	GPT321.GTCCRD compare match	TCFD	Possible
	GPT1_CMPE	GPT321.GTCCRE compare match	TCFE	Possible
	GPT1_CMPF	GPT321.GTCCRF compare match	TCFF	Possible
	GPT1_OVF	GPT321.GTCNT overflow (GPT321.GTPR compare match)	TCFPO	Possible
	GPT1_UDF	GPT321.GTCNT underflow	TCFPU	Possible
2	GPT2_CCMPA	GPT322.GTCCRA input capture/compare match	TCFA	Possible
	GPT2_CCMPB	GPT322.GTCCRB input capture/compare match	TCFB	Possible
	GPT2_CMPC	GPT322.GTCCRC compare match	TCFC	Possible
	GPT2_CMPD	GPT322.GTCCRD compare match	TCFD	Possible
	GPT2_CMPE	GPT322.GTCCRE compare match	TCFE	Possible
	GPT2_CMPF	GPT322.GTCCRF compare match	TCFF	Possible
	GPT2_OVF	GPT322.GTCNT overflow (GPT322.GTPR compare match)	TCFPO	Possible
	GPT2_UDF	GPT322.GTCNT underflow	TCFPU	Possible
3	GPT3_CCMPA	GPT323.GTCCRA input capture/compare match	TCFA	Possible
	GPT3_CCMPB	GPT323.GTCCRB input capture/compare match	TCFB	Possible
	GPT3_CMPC	GPT323.GTCCRC compare match	TCFC	Possible
	GPT3_CMPD	GPT323.GTCCRD compare match	TCFD	Possible
	GPT3_CMPE	GPT323.GTCCRE compare match	TCFE	Possible
	GPT3_CMPF	GPT323.GTCCRF compare match	TCFF	Possible
	GPT3_OVF	GPT323.GTCNT overflow (GPT323.GTPR compare match)	TCFPO	Possible
	GPT3_UDF	GPT323.GTCNT underflow	TCFPU	Possible
4	GPT4_CCMPA	GPT164.GTCCRA input capture/compare match	TCFA	Possible
	GPT4_CCMPB	GPT164.GTCCRB input capture/compare match	TCFB	Possible
	GPT4_CMPC	GPT164.GTCCRC compare match	TCFC	Possible
	GPT4_CMPD	GPT164.GTCCRD compare match	TCFD	Possible
	GPT4_CMPE	GPT164.GTCCRE compare match	TCFE	Possible
	GPT4_CMPF	GPT164.GTCCRF compare match	TCFF	Possible
	GPT4_OVF	GPT164.GTCNT overflow (GPT164.GTPR compare match)	TCFPO	Possible
	GPT4_UDF	GPT164.GTCNT underflow	TCFPU	Possible

Table 23.21 中断源(1of2)

Channel	Name	中断源	中断标志	DMAC/DTC activation
0	GPT0_CCMPA	GPT320.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT0_CCMPB	GPT320.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT0_CMPC	GPT320.GTCCRC比较匹配	TCFC	Possible
	GPT0_CMPD	GPT320.GTCCRD比较匹配	TCFD	Possible
	GPT0_CMPE	GPT320.GTCCRE比较匹配	TCFE	Possible
	GPT0_CMPF	GPT320.GTCCRF比较匹配	TCFF	Possible
	GPT0_OVF	GPT320.GTCNT溢出（GPT320.GTPR比较匹配）	TCFPO	Possible
	GPT0_UDF	GPT320.GTCNT underflow	TCFPU	Possible
1	GPT1_CCMPA	GPT321.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT1_CCMPB	GPT321.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT1_CMPC	GPT321.GTCCRC比较匹配	TCFC	Possible
	GPT1_CMPD	GPT321.GTCCRD比较匹配	TCFD	Possible
	GPT1_CMPE	GPT321.GTCCRE比较匹配	TCFE	Possible
	GPT1_CMPF	GPT321.GTCCRF比较匹配	TCFF	Possible
	GPT1_OVF	GPT321.GTCNT溢出（GPT321.GTPR比较匹配）	TCFPO	Possible
	GPT1_UDF	GPT321.GTCNT underflow	TCFPU	Possible
2	GPT2_CCMPA	GPT322.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT2_CCMPB	GPT322.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT2_CMPC	GPT322.GTCCRC比较匹配	TCFC	Possible
	GPT2_CMPD	GPT322.GTCCRD比较匹配	TCFD	Possible
	GPT2_CMPE	GPT322.GTCCRE比较匹配	TCFE	Possible
	GPT2_CMPF	GPT322.GTCCRF比较匹配	TCFF	Possible
	GPT2_OVF	GPT322.GTCNT溢出（GPT322.GTPR比较匹配）	TCFPO	Possible
	GPT2_UDF	GPT322.GTCNT underflow	TCFPU	Possible
3	GPT3_CCMPA	GPT323.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT3_CCMPB	GPT323.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT3_CMPC	GPT323.GTCCRC比较匹配	TCFC	Possible
	GPT3_CMPD	GPT323.GTCCRD比较匹配	TCFD	Possible
	GPT3_CMPE	GPT323.GTCCRE比较匹配	TCFE	Possible
	GPT3_CMPF	GPT323.GTCCRF比较匹配	TCFF	Possible
	GPT3_OVF	GPT323.GTCNT溢出（GPT323.GTPR比较匹配）	TCFPO	Possible
	GPT3_UDF	GPT323.GTCNT underflow	TCFPU	Possible
4	GPT4_CCMPA	GPT164.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT4_CCMPB	GPT164.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT4_CMPC	GPT164.GTCCRC比较匹配	TCFC	Possible
	GPT4_CMPD	GPT164.GTCCRD比较匹配	TCFD	Possible
	GPT4_CMPE	GPT164.GTCCRE比较匹配	TCFE	Possible
	GPT4_CMPF	GPT164.GTCCRF比较匹配	TCFF	Possible
	GPT4_OVF	GPT164.GTCNT溢出（GPT164.GTPR比较匹配）	TCFPO	Possible
	GPT4_UDF	GPT164.GTCNT underflow	TCFPU	Possible

Table 23.21 Interrupt sources (2 of 2)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
5	GPT5_CCMPA	GPT165.GTCCRA input capture/compare match	TCFA	Possible
	GPT5_CCMPB	GPT165.GTCCRB input capture/compare match	TCFB	Possible
	GPT5_CMPC	GPT165.GTCCRC compare match	TCFC	Possible
	GPT5_CMPD	GPT165.GTCCRD compare match	TCFD	Possible
	GPT5_CMPE	GPT165.GTCCRE compare match	TCFE	Possible
	GPT5_CMPF	GPT165.GTCCRF compare match	TCFF	Possible
	GPT5_OVF	GPT165.GTCNT overflow (GPT165.GTPR compare match)	TCFPO	Possible
	GPT5_UDF	GPT165.GTCNT underflow	TCFPU	Possible
8	GPT8_CCMPA	GPT168.GTCCRA input capture/compare match	TCFA	Possible
	GPT8_CCMPB	GPT168.GTCCRB input capture/compare match	TCFB	Possible
	GPT8_CMPC	GPT168.GTCCRC compare match	TCFC	Possible
	GPT8_CMPD	GPT168.GTCCRD compare match	TCFD	Possible
	GPT8_CMPE	GPT168.GTCCRE compare match	TCFE	Possible
	GPT8_CMPF	GPT168.GTCCRF compare match	TCFF	Possible
	GPT8_OVF	GPT168.GTCNT overflow (GPT168.GTPR compare match)	TCFPO	Possible
	GPT8_UDF	GPT168.GTCNT underflow	TCFPU	Possible

(1) GPTn_CCMPA interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register.

(2) GPTn_CCMPB interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register
- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register.

(3) GPTn_CMPC interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and thus interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(4) GPTn_CMPD interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and thus interrupt is not requested under the following conditions:

Table 23.21 中断源（2个中的2个）

Channel	Name	中断源	中断标志	DMAC/DTC activation
5	GPT5_CCMPA	GPT165.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT5_CCMPB	GPT165.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT5_CMPC	GPT165.GTCCRC比较匹配	TCFC	Possible
	GPT5_CMPD	GPT165.GTCCRD比较匹配	TCFD	Possible
	GPT5_CMPE	GPT165.GTCCRE比较匹配	TCFE	Possible
	GPT5_CMPF	GPT165.GTCCRF比较匹配	TCFF	Possible
	GPT5_OVF	GPT165.GTCNT溢出（GPT165.GTPR比较匹配）	TCFPO	Possible
	GPT5_UDF	GPT165.GTCNT underflow	TCFPU	Possible
8	GPT8_CCMPA	GPT168.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT8_CCMPB	GPT168.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT8_CMPC	GPT168.GTCCRC比较匹配	TCFC	Possible
	GPT8_CMPD	GPT168.GTCCRD比较匹配	TCFD	Possible
	GPT8_CMPE	GPT168.GTCCRE比较匹配	TCFE	Possible
	GPT8_CMPF	GPT168.GTCCRF比较匹配	TCFF	Possible
	GPT8_OVF	GPT168.GTCNT溢出（GPT168.GTPR比较匹配）	TCFPO	Possible
	GPT8_UDF	GPT168.GTCNT underflow	TCFPU	Possible

(1) GPTn_CCMPA中断（n=0到5、8）

在以下情况下会产生中断请求：

- 当GTCCRA寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRA register
- 当GTCCRA寄存器用作输入捕捉寄存器时，输入捕捉信号会导致传输GTCNT计数器值到GTCCRA寄存器。

(2) GPTn_CCMPB中断（n=0到5、8）

在以下情况下会产生中断请求：

- 当GTCCRB寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRB register
- 当GTCCRB寄存器用作输入捕捉寄存器时，输入捕捉信号会导致GTCNT计数器值到GTCCRB寄存器。

(3) GPTn_CMPC中断（n=0到5、8）

在以下情况下会产生中断请求：

- 当GTCCRC寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRC register.

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=01b 10b 11b（使用GTCCRC寄存器进行缓冲操作）。

(4) GPTn_CMPD中断（n=0到5、8）

在以下情况下会产生中断请求：

- 当GTCCRD寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRD register.

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(5) GPTn_CMPE interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following condition:

- When the GTCCRE register functions as a compare match register, the GTCNT counter value matches with the GTCCRE register.

A compare match is not performed and therefore interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register).

(6) GPTn_CMPF interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value matches with the GTCCRF register.

A compare match is not performed and therefore interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register).

(7) GPTn_OVF interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (GTCNT changes from GTPR to GTPR-1)
- In counting by hardware sources, overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(8) GPTn_UDF interrupt (n = 0 to 5, 8)

An interrupt request is generated under the following conditions:

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (GTCNT changes from 0 to 1)
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

Table 23.22 Interrupt signals and interrupt status flags (1 of 2)

Interrupt signal	Interrupt status flag
GPTn_UDF	GTST[7] (TCFPU)
GPTn_OVF	GTST[6] (TCFPO)
GPTn_CMPF	GTST[5] (TCFF)
GPTn_CMPE	GTST[4] (TCFE)
GPTn_CMPD	GTST[3] (TCFD)
GPTn_CMPC	GTST[2] (TCFC)
GPTn_CCMPB	GTST[1] (TCFB)

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=10b 11b（使用GTCCRD寄存器进行缓冲操作）。

(5) GPTn_CMPE中断（n=0到5、8）

在以下情况下会产生中断请求：

- 当GTCCRE寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRE register.

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=01b 10b 11b（使用GTCCRE寄存器进行缓冲操作）。

(6) GPTn_CMPF中断（n=0到5、8）

在以下情况下会产生中断请求：

- 当GTCCRF寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRF register.

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=10b 11b（使用GTCCRF寄存器进行缓冲操作）。

(7) GPTn_OVF中断（n=0到5、8）

在以下情况下会产生中断请求：

- 在锯齿波模式下，中断请求在溢出时启用（当GTCNT计数器值从向上计数期间GTPR为0）
- 在三角波模式下，在波峰处启用中断请求（GTCNT从GTPR变为GTPR-1）
- 在硬件源的计数中，发生了溢出（GTCNT在向上计数中从GTPR变为0）。

(8) GPTn_UDF中断（n=0到5、8）

在以下情况下会产生中断请求：

- 在锯齿波模式下，中断请求在下溢时启用（当GTCNT计数器值从0变为GTPR during down-counting)
- 在三角波模式下，在波谷处启用中断请求（GTCNT从0变为1）
- 在硬件源的计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

Table 23.22 中断信号和中断状态标志（1of2）

中断信号	中断状态标志
GPTn_UDF	GTST[7] (TCFPU)
GPTn_OVF	GTST[6] (TCFPO)
GPTn_CMPF	GTST[5] (TCFF)
GPTn_CMPE	GTST[4] (TCFE)
GPTn_CMPD	GTST[3] (TCFD)
GPTn_CMPC	GTST[2] (TCFC)
GPTn_CCMPB	GTST[1] (TCFB)

Table 23.22 Interrupt signals and interrupt status flags (2 of 2)

Interrupt signal	Interrupt status flag
GPTn_CCMPA	GTST[0] (TCFA)

Note: n = 0 to 5, 8

23.4.2 DMAC/DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 14, Interrupt Controller Unit (ICU), section 17, DMA Controller (DMAC), and section 18, Data Transfer Controller (DTC).

23.5 Operations Linked by ELC

23.5.1 Event Signal Output to ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

The GPT has the following ELC event signals:

- Generation of compare match A interrupt (GPTn_CCMPA)
- Generation of compare match B interrupt (GPTn_CCMPB)
- Generation of compare match C interrupt (GPTn_CMPC)
- Generation of compare match D interrupt (GPTn_CMPD)
- Generation of compare match E interrupt (GPTn_CMPE)
- Generation of compare match F interrupt (GPTn_CMPF)
- Generation of overflow interrupt (GPTn_OVF)
- Generation of underflow interrupt (GPTn_UDF).

Note: n = 0 to 5, 8

23.5.2 Event Signal Inputs from ELC

The GPT can perform the following operations in response to a maximum of eight events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down-counting
- Input capture.

See section 23.3, Operation for details on hardware resources.

23.6 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 23.82 shows the timing of noise filtering.

Table 23.22 中断信号和中断状态标志(2of2)

中断信号	中断状态标志
GPTn_CCMPA	GTST[0] (TCFA)

Note: n = 0 to 5, 8

23.4.2 DMAC/DTC Activation

DMAC和DTC可以通过每个通道中的中断来激活。有关详细信息，请参见第14节，中断控制器单元(ICU)，第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

23.5 由ELC链接的操作

23.5.1 事件信号输出到ELC

当GPT的中断请求信号被事件链接控制器(ELC)用作事件信号时，GPT可以执行与预先设置的另一个模块链接的操作。

GPT具有以下ELC事件信号：

- 产生比较匹配A中断(GPTn_CCMPA)
- 产生比较匹配B中断(GPTn_CCMPB)
- 产生比较匹配C中断(GPTn_CMPC)
- 产生比较匹配D中断(GPTn_CMPD)
- 产生比较匹配E中断(GPTn_CMPE)
- 产生比较匹配F中断(GPTn_CMPF)
- 产生溢出中断(GPTn_OVF)
- 产生下溢中断(GPTn_UDF)。

Note: n = 0 to 5, 8

23.5.2 来自ELC的事件信号输入

GPT最多可以执行以下操作以响应来自ELC的八个事件：

- 开始计数，停止计数，清除计数
- Up-counting, down-counting
- 输入捕获。

有关硬件资源的详细信息，请参见第23.3节，操作。

23.6 噪音过滤功能

用于GPT的输入捕捉和霍尔传感器输入的每个引脚都配备了噪声滤波器。噪声滤波器以采样时钟对输入信号进行采样，并去除长度小于3个采样周期的脉冲。

噪声过滤器功能包括为每个引脚启用和禁用噪声过滤器以及为每个通道设置采样时钟。

图23.82显示了噪声过滤的时序。

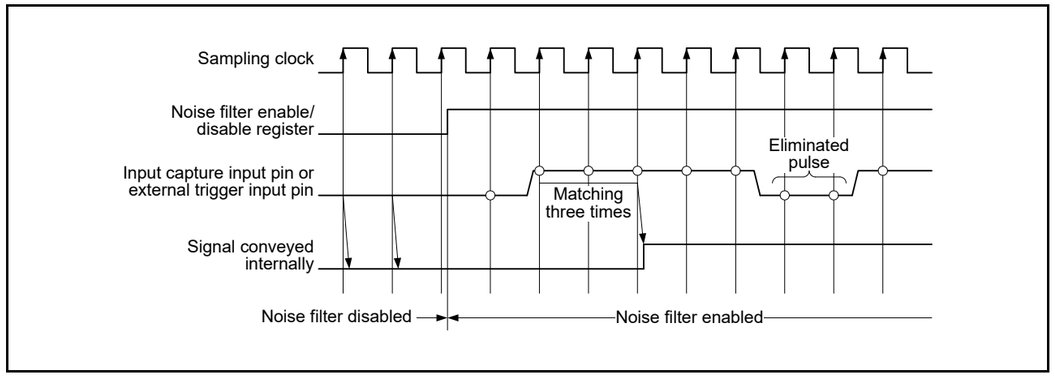


Figure 23.82 Timing of noise filtering

If noise filtering is enabled, the input capture operation or external trigger operation is performed on the edges of the noise filtered signal after a delay of a sampling interval × 3 + PCLKD. This is caused by the noise filtering for the input capture input or external trigger operation.

23.7 Protection Function

23.7.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

23.7.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD setting. Buffer transfer can be temporarily disabled even though a buffer transfer condition is generated during a buffer register write. This can be done by setting the associated GTBER.BD bit to 1 (buffer operation disabled) before buffer register write and clearing the bit to 0 (buffer operation enabled) after completion of writing to all buffer registers.

Figure 23.83 shows an example of operation for disabling buffer operation.

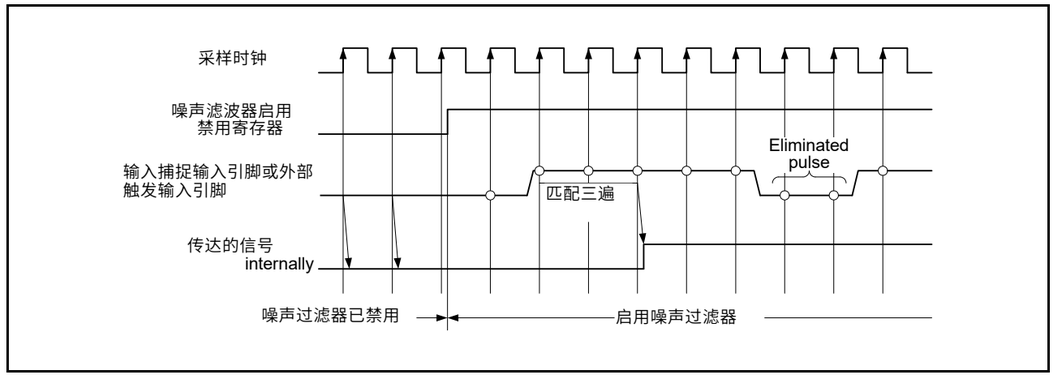


Figure 23.82 噪声过滤的时序

如果噪声过滤使能，输入捕捉操作或外部触发操作在经过一个采样间隔×3+PCLKD的延迟后，在噪声过滤信号的边沿上执行。这是由输入捕捉输入或外部触发操作的噪声过滤引起的。

23.7 保护功能

23.7.1 寄存器的写保护

为了防止寄存器被意外修改，可以通过设置以通道为单位对寄存器进行写保护 GTWP.WP。可以为以下寄存器设置写保护：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

23.7.2 禁用缓冲区操作

如果缓冲寄存器写入的时序相对于缓冲传输的时序延迟，则可以通过GTBER.BD设置暂停缓冲操作。即使在缓冲寄存器写入期间产生了缓冲传输条件，也可以暂时禁用缓冲传输。这可以通过在写入缓冲寄存器之前将相关的GTBER.BD位设置为1（禁用缓冲操作）并在完成对所有缓冲寄存器的写入后将该位清除为0（启用缓冲操作）来完成。

图23.83显示了禁用缓冲区操作的操作示例。

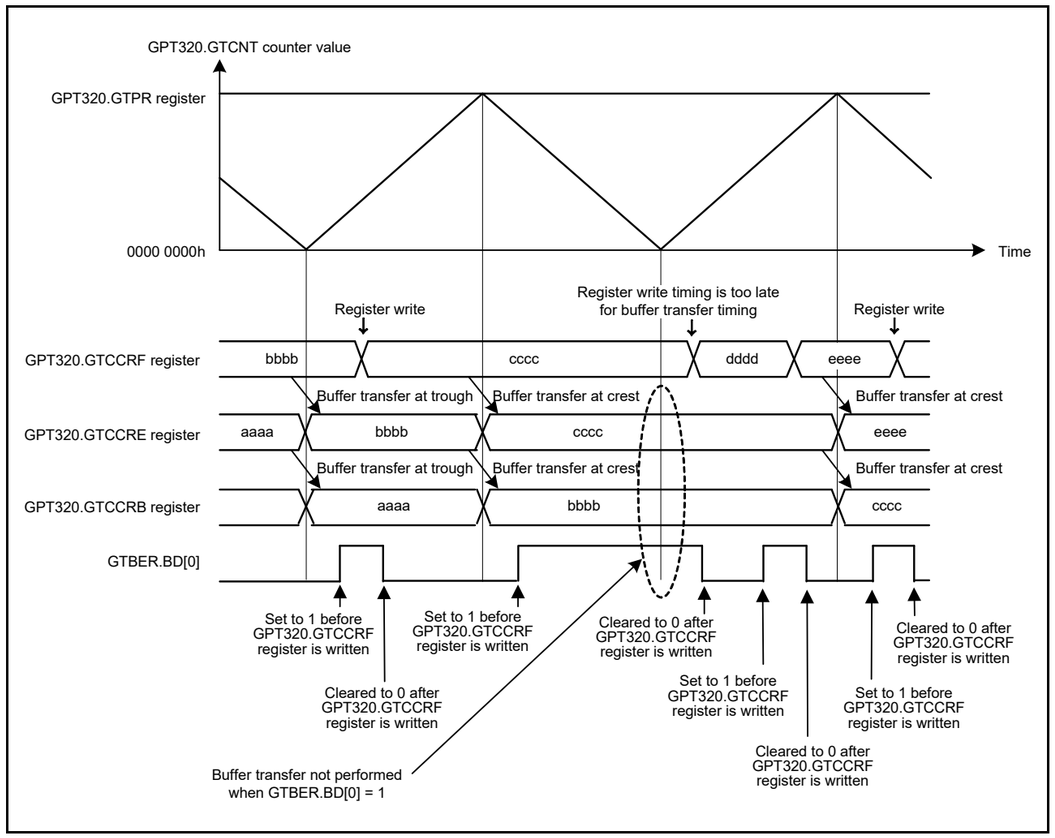


Figure 23.83 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

23.7.3 GTIOC Pin Output Negate Control

For protection from system failure, the output disable control that changes the GTIOC pin output value forcibly is provided for GTIOC pin output by the request of output disable from POEG.

When the GTIOCA pin output value is the same as the GTIOCB pin output value, output protection is required. GPT detects such a case and generates output disable requests to POEG based on the settings in the output disable request permission bits, such as GTINTAD.GRPABH, GTINTAD.GRPABL. When the POEG receives output disable requests from each channel and calculates external input using an OR operation, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCA pin and the GTIOCB pin) out of four output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set based on the GTIOR.OADF[1:0] setting for the GTIOCA pin and the GTIOR.OBDF[1:0] setting for the GTIOCB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. The timing of release of the output disable state is a minimum of 3 PCLKD cycles after terminating the output disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated.

When event count is performed or when the output disable state should be released immediately without waiting for the

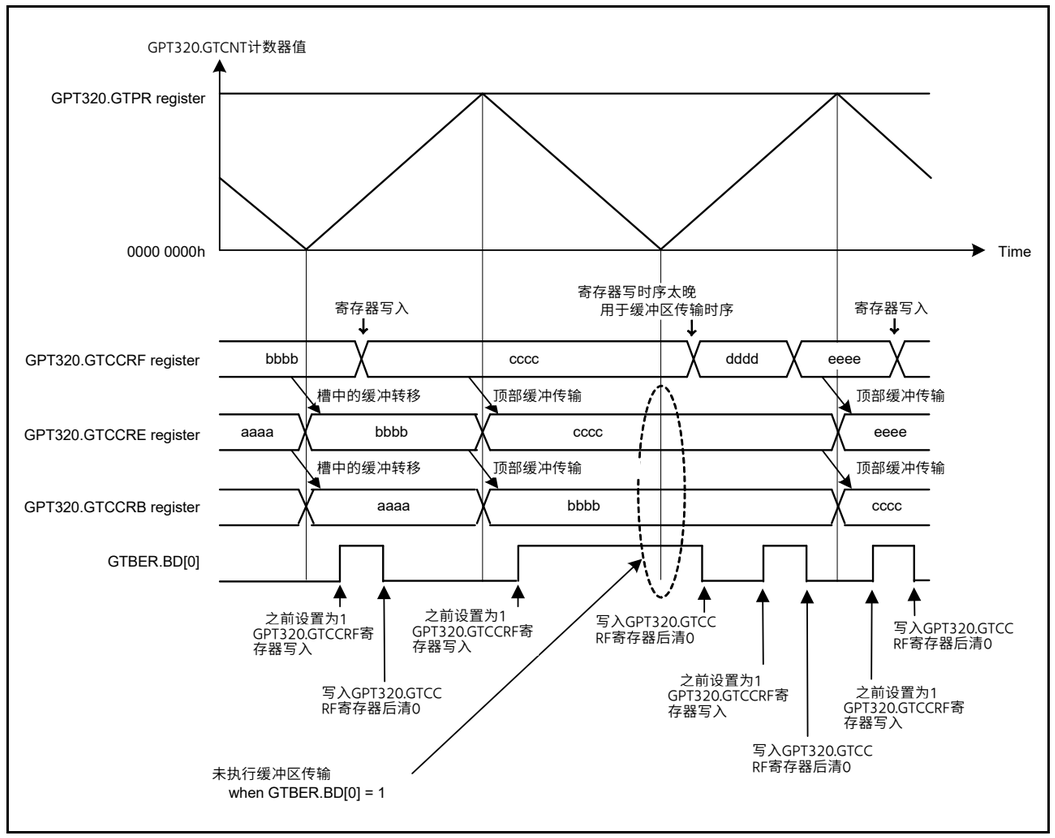


Figure 23.83 三角波缓冲操作、双缓冲操作、波谷和波峰缓冲转移的禁用操作示例

23.7.3 GTIOC引脚输出负控制

为防止系统故障，根据POEG的输出禁用请求，为GTIOC引脚输出提供强制改变GTIOC引脚输出值的输出禁用控制。

当GTIOCA引脚输出值与GTIOCB引脚输出值相同时，需要输出保护。GPT检测到这种情况并根据输出禁用请求权限位中的设置（例如GTINTAD.GRPABH、GTINTAD.GRPABL）向POEG生成输出禁用请求。当POEG接收到来自每个通道的输出禁用请求并使用OR运算计算外部输入时，POEG向GPT生成输出禁用请求。

通过设置GTINTAD.GRP[1:0]，从POEG产生的四个输出禁止请求中选择一个输出禁止信号（代表GTIOCA引脚和GTIOCB引脚的共享输出禁止请求信号）。通过读取GTST.ODF位来监控所选禁用输出请求的状态。输出禁用期间的输出电平根据GTIOCA引脚的GTIOR.OADF[1:0]设置和GTIOCB引脚的GTIOR.OBDF[1:0]设置进行设置。

对输出禁用状态的更改是通过从
POEG。通过终止输出禁用请求，在循环结束时执行输出禁用状态的释放。输出禁用状态的释放时间是在终止输出禁用请求后至少3个PCLKD周期。为了可靠地执行输出禁用控制，在生成输出禁用请求后（通过清除POEG中的输出禁用请求标志）至少允许4个PCLKD周期，直到输出禁用请求终止。

当执行事件计数或输出禁用状态应立即释放而无需等待

end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCA pin) or GTIOR.OBDF[1:0] should be set to 00b (for GTIOCB pin).

Figure 23.84 shows an example of the GTIOC pin output disable control operation.

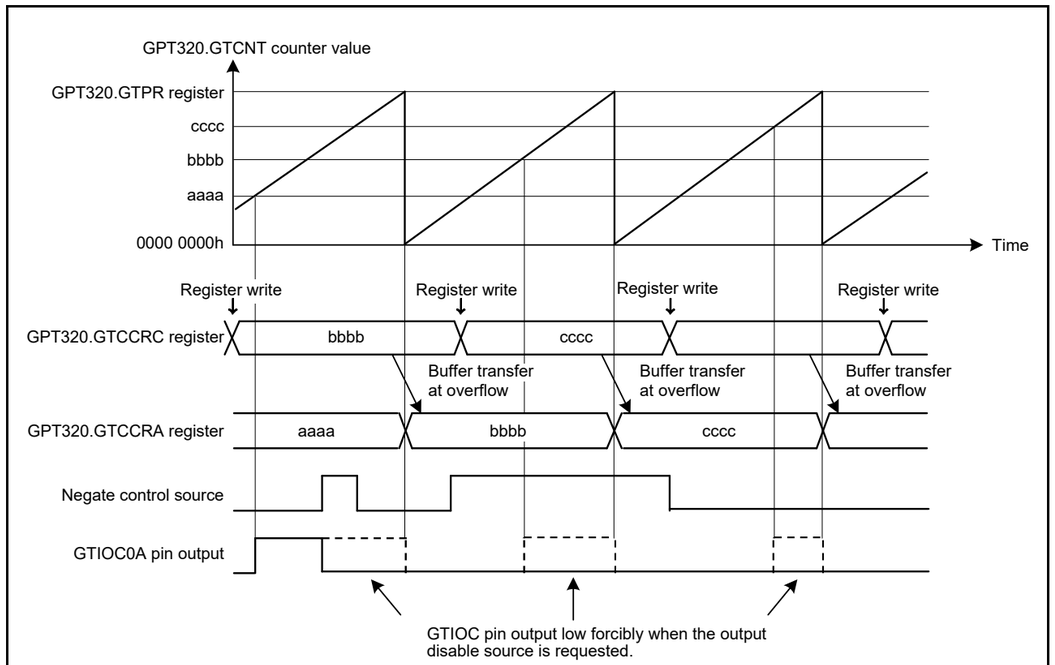


Figure 23.84 Example of GTIOC pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable

23.8 Initialization Method of Output Pins

23.8.1 Pin Settings after Reset

The GPT registers are initialized at reset. Start counting after selecting the port pin function by PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.

周期结束时，GTIOR.OADF[1:0]应设置为00b（对于GTIOCA引脚）或GTIOR.OBDF[1:0]应设置为00b（对于GTIOCB引脚）。

图23.84显示了GTIOC引脚输出禁用控制操作的示例。

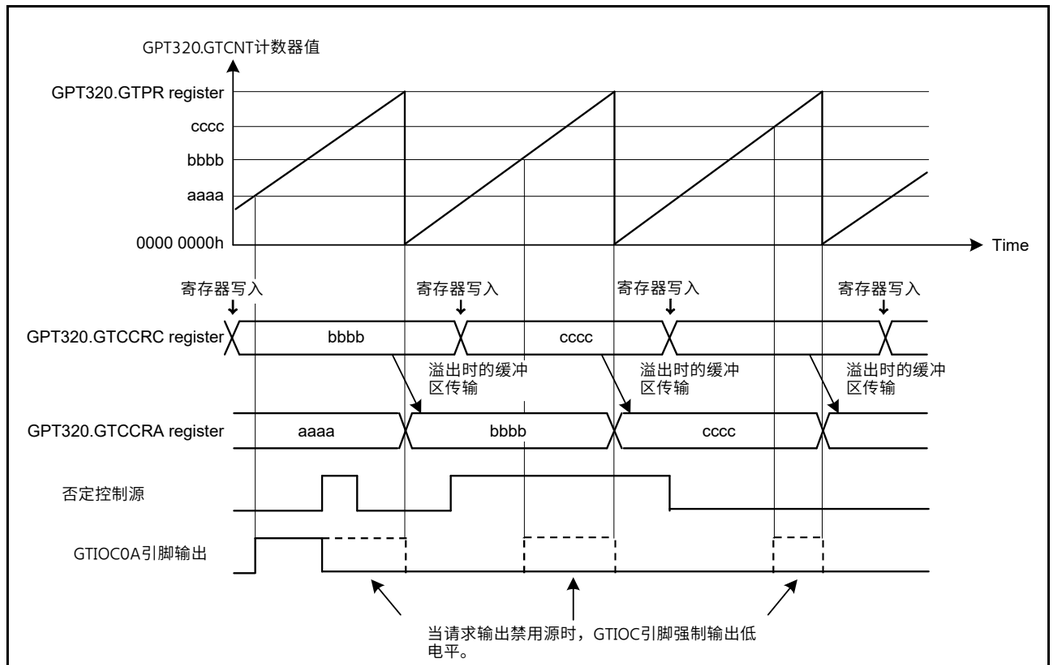


Figure 23.84 GTIOC引脚输出禁用控制操作示例：锯齿波递增计数、缓冲器操作、有效电平1、GTCCRA比较匹配时的高输出、周期结束时的低输出和输出禁用时的低输出

23.8 输出管脚的初始化方法

23.8.1 复位后的引脚设置

GPT寄存器在复位时被初始化。通过PmnPFS寄存器选择端口引脚功能后开始计数，设置GTIOR.OAE和GTIOR.OBE位，并将GPT功能输出到外部引脚。

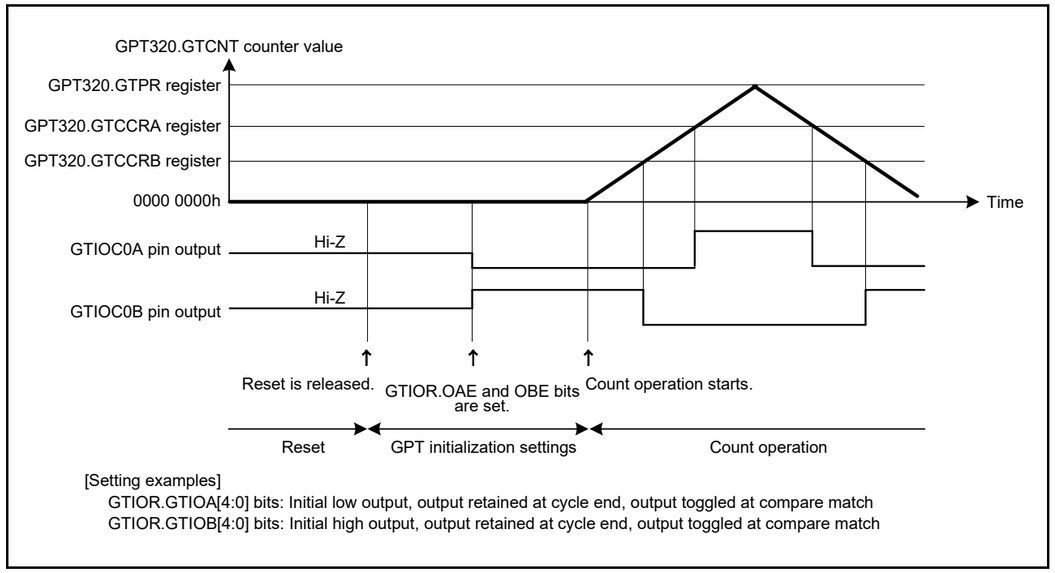


Figure 23.85 Example of pin settings after reset

23.8.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PmnPFS registers of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in the PmnPFS.PMR to 0, to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

When the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting resumes, operation continues from where it stopped. If counting stops, registers should be initialized before counting starts.

23.9 Usage Notes

23.9.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT module is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

23.9.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy the following conditions: GTDVU < GTCCRA and 0 < GTCCRA < GTPR.

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When

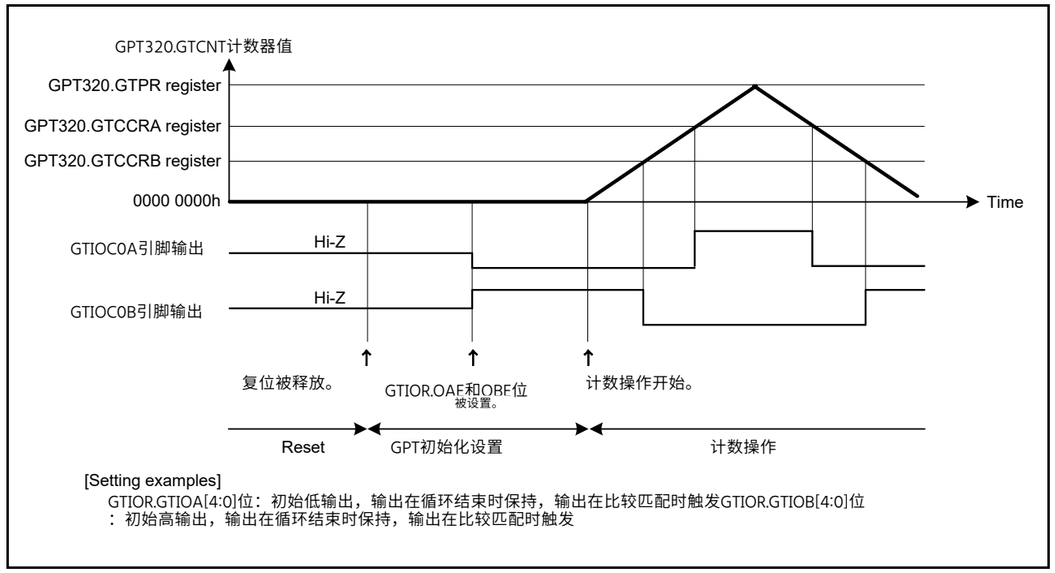


Figure 23.85 复位后的引脚设置示例

23.8.2 由于操作过程中的错误而导致的引脚初始化

如果在GPT操作过程中发生错误，可以在引脚初始化之前进行以下四种引脚处理：

- 将GTIOR中的OAHLD和OBHLD位设置为1，并在计数停止时保留输出
- 将GTIOR中的OAHLD和OBHLD位设置为0，在OADFLT和OBDFLT中指定任意输出值
  GTIOR，并在计数停止时输出任意值
- 通过预先设置IO端口的PDR、PODR和PmnPFS寄存器，将引脚设置为输出任意值作为通用输出端口。将GTIOR中的OAE和OBE位设置为0，并将与PmnPFS.PMR中的引脚相关的控制位设置为0，以允许在发生错误时从设置为通用输出端口的引脚输出任意值。
- 使用POEG功能将输出驱动到高阻抗状态。

进行自动死区时间设置时，计数停止后将GTDTCR.TDE位清零。当计数停止时，只有被GPT外部源改变的寄存器的值会改变。如果计数恢复，则操作从停止处继续。如果计数停止，则应在计数开始前初始化寄存器。

23.9 使用说明

23.9.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用GPT操作。GPT模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

23.9.2 比较匹配操作期间的GTCCRn设置（n=A到F）

(1) 在三角波PWM模式下进行自动死区时间设置时

GTCCRA寄存器必须满足以下条件：GTDVU<GTCCRA和0<GTCCRA<GTPR。

(2) 在三角波PWM模式下未进行自动死区时间设置时

GTCCRA寄存器必须设置在0<GTCCRA<GTPR的范围内。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。什么时候

GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB should be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVU.

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0.

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

23.9.3 Setting Range for GTCNT Counter

The GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

23.9.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[2:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[2:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored. On the other side, there might be cases where an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

23.9.5 Priority Order of Each Event

(1) GTCNT register

Table 23.23 shows a priority order of events updating the GTCNT register.

Table 23.23 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High ↑
Clear by hardware sources set in GTCSR	
Count up or down by hardware sources set in GTUPSR/GTDNSR	
Count operation	Low

GTCCRA>GTPR，没有比较匹配发生。

同样，GTCCRB应设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。当GTCCRB>GTPR时，不发生比较匹配。

(3) 在锯波单发脉冲模式下进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足这些限制，则可能无法获得具有可靠死区时间的正确输出波形。

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVU.

(4) 在锯波单发脉冲模式下未进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0.

同样，必须设置GTCCRE和GTCCRF以满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) 在锯齿波PWM模式下

GTCCRA寄存器必须设置为0<GTCCRA<GTPR。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRA>GTPR，则不会发生比较匹配。

类似地，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRB>GTPR，则不会发生比较匹配。

23.9.3 GTCNT计数器的设置范围

GTCNT计数器寄存器的设置范围必须为0≤GTCNT≤GTPR。

23.9.4 启动和停止GTCNT计数器

通过GTCR.CST位启动和停止GTCNT计数器的控制时序与在GTCR.TPCS[2:0]中选择的计数时钟同步。当GTCR.CST更新时，GTCNT计数器在GTCR.TPCS[2:0]中选择的计数时钟后开始停止。因此，在GTCNT计数器实际启动之前生成的事件将被忽略。另一方面，在GTCR.CST设置为0之后，可能会出现接受事件或发生中断的情况。

23.9.5 每个事件的优先顺序

(1) GTCNT register

表23.23显示了更新GTCNT寄存器的事件的优先顺序。

Table 23.23 更新GTCNT的源的优先顺序

源更新GTCNT	优先顺序
CPU写入（写入GTCNTGTCLR）	High ↑
由GTCSR中设置的硬件源清除	
通过GTUPSRGTDNSR中设置的硬件源进行向上或向下计数	
计数操作	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change. When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), writing by CPU has priority over starting/stopping by hardware sources.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. When there is a conflict between updating the GTCR.CST bit and reading by the CPU, pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to GTCCRm registers, writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. When there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR registers

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

如果硬件源的递增计数和递减计数同时发生，GTCNT计数器值不会改变。当更新GTCNT寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(2) GTCR.CST bit

当GTSSRGTPSR寄存器中设置的硬件源启动停止与CPU写入（写入GTCRGTSTRGTSTP寄存器）发生冲突时，CPU写入优先于硬件源启动停止。

当GTSSR寄存器中设置的硬件源启动和GTPSR寄存器中设置的硬件源停止之间存在冲突时，GTCR.CST位的值不会改变。当更新GTCR.CST位与CPU读取之间存在冲突时，会读取更新前的数据。

(3) GTCCRm寄存器（m=A到F）

当输入捕捉缓冲区传输操作和写入GTCCRm寄存器之间存在冲突时，写入GTCCRm寄存器优先于输入捕捉缓冲区传输操作。当输入捕获与CPU写入计数器寄存器或硬件源更新计数器寄存器之间存在冲突时，会捕获更新前的计数器值。当更新GTCCRm寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(4) GTPR registers

当缓冲区传输操作与写入GTPR寄存器之间存在冲突时，写入GTPR寄存器优先于缓冲区传输操作。当更新GTPR寄存器与CPU读取发生冲突时，读取更新前的数据。

24. Asynchronous General Purpose Timer (AGT)

24.1 Overview

The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events.

This 16-bit timer consists of a reload register and a down counter. The reload register and the down counter are allocated in the same address, and can be accessed with the AGT register.

Table 24.1 lists the AGT specifications, Figure 24.1 shows the AGT block diagram, and Table 24.2 lists the AGT pin configuration.

Table 24.1 AGT specifications

Parameter		Description
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Count source (Operating clock)*2		PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d, AGTSCLK/d, or underflow signal of AGT0*1 selectable. (d = 1, 2, 4, 8, 16, 32, 64, or 128)
Interrupt/Event link function (Output)		• Unterflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input (AGTIOn) is complete in pulse width measurement mode – When the set edge of the external input (AGTIOn) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT and AGTCMA matched (Compare match A function enabled)*3 • Compare match B event signal – When the values of AGT and AGTCMB matched (Compare match B function enabled) • Recovery from Software Standby mode can be perfomed with AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI.
Selectable functions		• Compare match function One or two of the compare match A register and compare match B register is selectable.

Note 1. AGT0 cannot use it. AGT1 connects directly with the underflow event signal from the AGT0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.
Note 3. Compare match A does not have a compare match output pin.

24. 异步通用定时器(AGT)

24.1 Overview

异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。

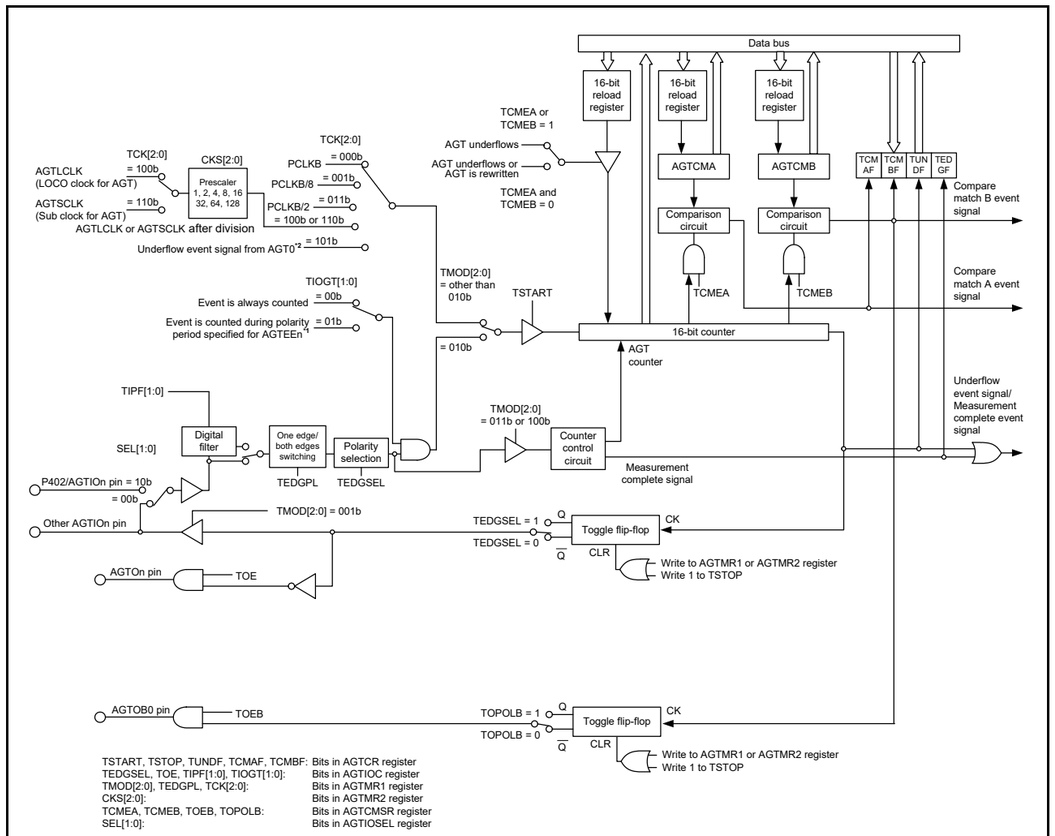
这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配在同一个地址，可以通过AGT寄存器访问。

表24.1列出了AGT规格，图24.1显示了AGT框图，表24.2列出了AGT引脚配置。

Table 24.1 AGT specifications

Parameter		Description
操作模式	定时器模式	计数源被计数
	脉冲输出方式	计数源被计数并在每次定时器下溢时反转输出
	事件计数器模式	计算外部事件
	脉宽测量模式	测量外部脉冲宽度
	脉冲周期测量模式	测量外部脉冲周　　期
计数源（工作时钟）*2		PCLKB、PCLKB2、PCLKB8、AGTLCLKd、AGTSCLKd或下溢信号 AGT0*1可选择。（d=1、2、4、8、16、32、64或128）
中断事件链接功能（输出）		上溢事件信号或测量完成事件信号　计数器下溢时　在脉冲宽度测量模式下外部输入(AGTIOn)的有效宽度测量完成时　输入外部输入(AGTIOn)的设置边沿时在脉冲周期测量模式。　比较匹配A事件信号 当AGT和AGTCMA的值匹配时（启用比较匹配A功能）*3　比较匹配B事件信号 当AGT和AGTCMB的值匹配时（启用比较匹配B功能）　可以使用AGT1_AGTI、AGT1_AGTCMAI或AGT1_AGTCMBI从软件待机模式恢复。
可选择的功能		比较匹配功能 可以选择比较匹配A寄存器和比较匹配B寄存器中的一个或两个。

Note 1. AGT0不能使用它。AGT1直接与来自AGT0定时器的下溢事件信号相连。
Note 2. 满足外设模块时钟（PCLKB）的频率≥计数源时钟的频率。
Note 3. 比较匹配A没有比较匹配输出引脚。



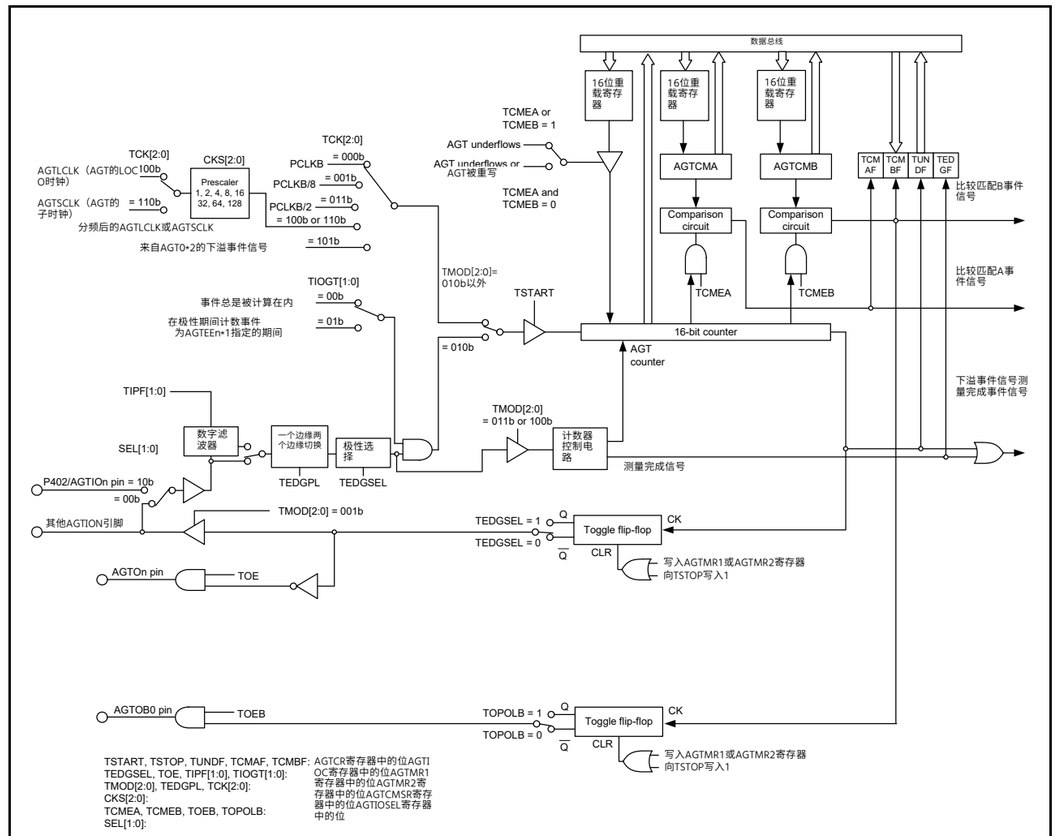
Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGT0 cannot use AGT underflow event. AGT1 uses the underflow of AGT0.

Figure 24.1 AGT block diagram

Table 24.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input for AGT
AGTIOn*1	Input*1/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOB0	Output	Output compare match B output for AGT

Note: Channel number (n = 0, 1)
Note 1. When AGTIO1 is assigned P402, AGTIO1 can only be used as inputs.



Note 1. 极性可以通过AGTISR寄存器中的EEPS位来选择。
Note 2. AGT0不能使用AGT下溢事件。AGT1使用AGT0的下溢。

Figure 24.1 AGT框图

Table 24.2 AGT I/O pins

引脚名称	I/O	Function
AGTEEn	Input	AGT的外部事件输入
AGTIOn*1	Input*1/output	AGT的外部事件输入和脉冲输出
AGTOn	Output	AGT的脉冲输出
AGTOB0	Output	AGT的输出比较匹配B输出

Note: 通道号(n=0 1)
Note 1. 当AGTIO1分配为P402时，AGTIO1只能用作输入。

24.2 Register Descriptions

24.2.1 AGT Counter Register (AGT)

Address(es): AGT0.AGT 4008 4000h, AGT1.AGT 4008 4100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting Range	R/W
b15 to b0	16-bit counter and reload register *1, *2	0000h to FFFFh	R/W

Note 1. When 1 is written to the TSTOP bit in the AGTCR register, the 16-bit counter is forcibly stopped and set to FFFFh.
Note 2. When the TCK[2:0] bit setting in the AGTMR1 register is a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0000h, a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts. The AGTOn and AGTIOn output is toggled.
When the AGT register is set to 0000h in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC and the ELC is generated once immediately after the count starts.
In addition, the AGTOn output toggles even during a period other than the specified count period. When the AGT register is set to 0001h or more, a request signal is generated each time AGT underflows.

AGT is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 24.3.1, Reload Register and Counter Rewrite Operation. The AGT register can be set by a 16-bit memory manipulation instruction.

24.2.2 AGT Compare Match A Register (AGTCMA)

Address(es): AGT0.AGTCMA 4008 4002h, AGT1.AGTCMA 4008 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match A data is stored*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMA register to FFFFh when compare match A is not to be used.

The AGTCMA register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and the compare register A change according to the TSTART bit in the AGTCR register. For details, see section 24.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMA register can be set with a 16-bit memory manipulation instruction.

24.2 注册说明

24.2.1 AGT计数器寄存器(AGT)

Address(es): AGT0.AGT 4008 4000h, AGT1.AGT 4008 4100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	设定范围	R/W
b15 to b0	16位计数器和重载寄存器*1 *2	0000h to FFFFh	R/W

Note 1. 当AGTCR寄存器的TSTOP位写入1时，16位计数器被强制停止并设置为FFFFh。
Note 2. 当AGTMR1寄存器中的TCK[2:0]位设置为001b(PCLKB8)或011b(PCLKB2)以外的值时，如果AGT寄存器设置为0000h，则向ICU、DTC、并在计数开始后立即生成一次ELC。AGTOn和AGTIOn输出被切换。

当AGT寄存器在事件计数器模式下设置为0000h时，无论TCK[2:0]位的值如何，都会在计数开始后立即向ICU、DTC和ELC生成一次请求信号。
此外，即使在指定计数周期以外的周期内，AGTOn输出也会切换。当AGT寄存器设置为0001h或更大时，每次AGT下溢时都会产生一个请求信号。

AGT是一个16位的寄存器。写入值写入重载寄存器，读取值从计数器中读取。

重载寄存器和计数器的状态根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEATCMEB位。有关详细信息，请参阅第24.3.1节，重新加载寄存器和计数器重写手术。AGT寄存器可以通过16位内存操作指令设置。

24.2.2 AGT比较匹配A寄存器(AGTCMA)

Address(es): AGT0.AGTCMA 4008 4002h, AGT1.AGTCMA 4008 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	设定范围	R/W
b15 to b0	16位比较匹配存储数据*1	0000h to FFFFh	R/W

Note 1. 当不使用比较匹配A时，将AGTCMA寄存器设置为FFFFh。

AGTCMA寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器A的状态根据AGTCR寄存器中的TSTART位而改变。有关详细信息，请参见第24.3.2节，重载寄存器和比较寄存器AB重写操作。AGTCMA寄存器可通过16位存储器操作指令进行设置。

24.2.3 AGT Compare Match B Register (AGTCMB)

Address(es): AGT0.AGTCMB 4008 4004h, AGT1.AGTCMB 4008 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match B data is stored*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMB register to FFFFh when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and the compare register B change according to the TSTART bit in the AGTCR register. For details, see section 24.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMB register can be set by a 16-bit memory manipulation instruction.

24.2.4 AGT Control Register (AGTCR)

Address(es): AGT0.AGTCR 4008 4008h, AGT1.AGTCR 4008 4108h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTART	AGT count start*2	0: Count stops 1: Count starts.	R/W
b1	TCSTF	AGT count status flag*2	0: Count stopped 1: Count in progress.	R
b2	TSTOP	AGT count forced stop*1	0: Writing is invalid 1: The count is forcibly stopped.	W
b3	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	TEDGF	Active edge judgment flag	0: No active edge received 1: Active edge received.	R/(W)*3
b5	TUNDF	Underflow flag	0: No underflow 1: Underflow.	R/(W)*3
b6	TCMAF	Compare match A flag	0: No match 1: Match.	R/(W)*3
b7	TCMBF	Compare match B flag	0: No match 1: Match.	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART and TCSTF bits are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using TSTART and TCSTF bits, see section 24.4.1, Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

TSTART bit (AGT count start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When this bit is set to 1, the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stopped) in synchronization with the count source. For details, see section 24.4.1, Count Operation Start and Stop Control.

24.2.3 AGT比较匹配B寄存器(AGTCMB)

Address(es): AGT0.AGTCMB 4008 4004h, AGT1.AGTCMB 4008 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	设定范围	R/W
b15 to b0	存储16位比较匹配B数据*1	0000h to FFFFh	R/W

Note 1. 当不使用比较匹配B时，将AGTCMB寄存器设置为FFFFh。

AGTCMB寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器B的状态根据AGTCR寄存器中的TSTART位改变。有关详细信息，请参见第24.3.2节，重载寄存器和比较寄存器AB重写操作。AGTCMB寄存器可以通过16位存储器操作指令设置。

24.2.4 AGT控制寄存器(AGTCR)

Address(es): AGT0.AGTCR 4008 4008h, AGT1.AGTCR 4008 4108h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSTART	AGT计数开始 *2	0：计数停止1 ：计数开始。	R/W
b1	TCSTF	AGT计数状态标志 *2	0：计数停止1：计数 进行中。	R
b2	TSTOP	AGT计数强制停止 *1	0：写入无效1：强制停止计数 。	W
b3	—	Reserved	读取值为0。写入值应为0。	R/W
b4	TEDGF	有效边沿判断标志	0：未收到有效边沿1：收 到有效边沿。	R/(W)*3
b5	TUNDF	Underflow flag	0: No underflow 1: Underflow.	R/(W)*3
b6	TCMAF	比较匹配A标志	0：不匹配1 ：匹配。	R/(W)*3
b7	TCMBF	比较匹配B标志	0：不匹配1 ：匹配。	R/(W)*3

Note 1. 当1（强制停止计数）写入TSTOP位时，TSTART和TCSTF位同时初始化。
脉冲输出电平也被初始化。读取值为0。
Note 2. 有关使用TSTART和TCSTF位的信息，请参见第24.4.1节，计数操作开始和停止控制。
Note 3. 只能写入0来清除标志。

TSTART位（AGT计数开始）

通过向TSTART位写入1开始计数操作，通过写入0停止计数操作。当该位设置为1时，TCSTF位与计数源同步设置为1（正在进行计数）。此外，在TSTART位写入0后，TCSTF位与计数源同步设置为0（计数停止）。有关详细信息，请参见第24.4.1节，计数操作开始和停止控制。

TCSTF flag (AGT count status flag)

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT count forced stop)

When 1 is written to this bit, the count is forcibly stopped. The read value is 0.

TEDGF flag (Active edge judgment flag)

[Setting condition]

- When the measurement of the active width of the external input (AGTIOn) is complete in pulse width measurement mode
- When the set edge of the external input (AGTIOn) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this flag by software.

TUNDF flag (Underflow flag)

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare match A flag)

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare match B flag)

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

TCSTF标志（AGT计数状态标志）

[Setting condition]

- 当1写入TSTART位时（TCSTF标志设置为1与计数源同步）。

[Clearing conditions]

- 当0写入TSTART位时（TCSTF标志设置为0与计数源同步）
- 当1写入TSTOP位时。

TSTOP位（AGT计数强制停止）

向该位写入1时，强制停止计数。读取值为0。

TEDGF标志（有效边沿判断标志）

[Setting condition]

- 在脉冲宽度测量模式下，外部输入(AGTIOn)的有效宽度测量完成时
- 在脉冲周期测量模式下输入外部输入(AGTIOn)的设置边沿时。

[Clearing condition]

- 当软件向该标志写入0时。

TUNDF flag (Underflow flag)

[Setting condition]

- 当计数器下溢时。

[Clearing condition]

- 当软件向该标志写入0时。

TCMAF标志（比较匹配A标志）

[Setting condition]

- 当AGT寄存器中的值与AGTCMA寄存器中的值匹配时。

[Clearing condition]

- 当软件向该标志写入0时。

TCMBF标志（比较匹配B标志）

[Setting condition]

- 当AGT寄存器中的值与AGTCMB寄存器中的值匹配时。

[Clearing condition]

- 当软件向该标志写入0时。

24.2.5 AGT Mode Register 1 (AGTMR1)

Address(es): AGT0.AGTMR1 4008 4009h, AGT1.AGTMR1 4008 4109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	TMOD[2:0]	Operating mode*3	b2 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode. Other settings are prohibited.	R/W
b3	TEDGPL	Edge polarity*4	0: Single-edge 1: Both-edge.	R/W
b6 to b4	TCK[2:0]	Count source*1, *2, *5	b6 b4 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified by CKS[2:0] bits in the AGTR2 register 1 0 1: Underflow event signal from AGT0*6 1 1 0: Divided clock AGTSCLK specified by CKS[2:0] bits in the AGTR2 register. Other settings are prohibited.	R/W
b7	—	Reserved	The read value is 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, and AGTOB0 pins of the AGT (n = 0, 1). For details on the output level at initialization, see the description of section 24.2.7, AGT I/O Control Register (AGTIOC).
Note 1. When event counter mode is selected, the external input (AGTIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.
Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).
Note 3. The operating mode can only be changed when the count is stopped while both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.
Note 4. The TEDGPL bit is enabled only in event counter mode.
Note 5. To run AGT in Software Standby mode, select AGTLCLK or AGTSCLK.
Note 6. AGT0 cannot use AGT0 underflow. AGT1 uses the AGT0 underflow.

24.2.5 AGT模式寄存器1(AGTMR1)

Address(es): AGT0.AGTMR1 4008 4009h, AGT1.AGTMR1 4008 4109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称		Description	R/W
b2 to b0	TMOD[2:0]	操作模式	*3	b2b0000：定时器模式001：脉冲输出模式010：事件计数器模式011：脉冲宽度测量模式100：脉冲周期测量模式。禁止其他设置。	R/W
b3	TEDGPL	边缘极性	*4	0: Single-edge 1: Both-edge.	R/W
b6 to b4	TCK[2:0]	计数来源	*1, *2, *5	b6b4000：PCLKB001：PCLKB8011：PCLKB2100：由AGTR2寄存器中的CKS[2:0]位指定的分频时钟AGTLCLK101：来自AGT0的下溢事件信号*6110：分频时钟AGTSCLK由AGTR2寄存器中的CKS[2:0]位指定。 禁止其他设置。	R/W
b7	—	Reserved		读取值为0。写入值应为0。	R/W

Note: 对AGTMR1寄存器的写访问初始化AGT(n=0 1)的AGTOn、AGTIOn和AGTOB0引脚的输出。有关初始化时输出电平的详细信息，请参见第24.2.7节AGTIO控制寄存器(AGTIOC)的描述。
Note 1. 选择事件计数器模式时，无论设置如何TCK[2:0] bits.
Note 2. 请勿在计数操作期间切换计数源。只有在TSTART和TCSTF位都在AGTCR寄存器设置为0（停止计数）。
Note 3. 只有在AGTCR寄存器中的TSTART和TCSTF位都设置为0（计数停止）时停止计数，才能更改操作模式。请勿在计数操作期间更改操作模式。
Note 4. TEDGPL位仅在事件计数器模式下启用。
Note 5. 要在软件待机模式下运行AGT，请选择AGTLCLK或AGTSCLK。
Note 6. AGT0不能使用AGT0下溢。AGT1使用AGT0下溢。

24.2.6 AGT Mode Register 2 (AGTMR2)

Address(es): AGT0.AGTMR2 4008 400Ah, AGT1.AGTMR2 4008 410Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKS[2:0]	AGTLCLK/AGTSCLK count source clock frequency division ratio *1, *2, *3	b2 b0 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	LPM	Low Power Mode	0: Normal mode 1: Low power mode.	R/W

Note 1. Do not rewrite the CKS[2:0] bit during count operation. Only rewrite CKS[2:0] when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count stops).
Note 2. When the count source is AGTLCLK or AGTSCLK, CKS[2:0] switch is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] are set to 000b, and wait for 1 cycle of the count source.

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set this bit to 1 to operate in low power. When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- AGT — Read AGT register twice. Only the second reading of data is valid.
- AGT, AGTCMA, AGTCMB, and AGTCR — Allow at least 2 cycles of the count source clock when writing to the register.

24.2.7 AGT I/O Control Register (AGTIOC)

Address(es): AGT0.AGTIOC 4008 400Ch, AGT1.AGTIOC 4008 410Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDGSEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TEDGSEL	I/O polarity switch	Function varies depending on the operating mode. See Table 24.3 and Table 24.4. The TEDGSEL bit switches the AGTOn output polarity and the AGTIOn input/output edge and polarity. In pulse output mode, it only controls the polarity of the AGTOn output and AGTIOn output. AGTOn output and AGTIOn output are initialized when the AGTMR1 register is written and the TSTOP bit in the AGTCR register is written with 1.	R/W

24.2.6 AGT模式寄存器2(AGTMR2)

Address(es): AGT0.AGTMR2 4008 400Ah, AGT1.AGTMR2 4008 410Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LPM	—	—	—	—	CKS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CKS[2:0]	AGTLCLKAGTSCLK计数源时钟分频比 *1, *2, *3	b2 b0 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128.	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	LPM	低功耗模式	0：正常模式1：低功耗模式。	R/W

Note 1. 在计数操作期间不要重写CKS[2:0]位。只有在TSTART和TCSTF位都在AGTCR寄存器设置为0（计数停止）。
Note 2. 当计数源为AGTLCLK或AGTSCLK时，CKS[2:0]开关有效。
Note 3. 当CKS[2:0]不是000b时，不要切换AGTMR1寄存器中的TCK[2:0]位。在CKS[2:0]设置为000b后，切换AGTMR1寄存器中的TCK[2:0]位，并等待计数源的1个周期。

LPM位（低功耗模式）

LPM位设置低功耗操作，这会影响对某些AGT寄存器的访问。将此位设置为1以在低功耗下工作。该位为1时，禁止访问以下寄存器：

- AGT/AGTCMA/AGTCMB/AGTCR.

该位由1变为0后，对寄存器的第一次访问受到如下约束：

- AGT—读取AGT寄存器两次。只有第二次读取数据是有效的。
- AGT、AGTCMA、AGTCMB和AGTCR—写入寄存器时允许至少2个计数源时钟周期。

24.2.7 AGTIO控制寄存器(AGTIOC)

Address(es): AGT0.AGTIOC 4008 400Ch, AGT1.AGTIOC 4008 410Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDGSEL
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TEDGSEL	IO极性开关	功能因操作模式而异。请参见表24.3和表24.4。 TEDGSEL位切换AGTOn输出极性和AGTIon输入输出边沿和极性。在脉冲输出模式下，它只控制AGTOn输出和AGTIOn输出的极性。当写入AGTMR1寄存器并将AGTCR寄存器中的TSTOP位写入1时，初始化AGTOn输出和AGTIOn输出。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	TOE	AGTOn output enable	0: AGTOn output disabled 1: AGTOn output enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	TIPF[1:0]	Input filter *3	b5 b4 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32. These bits specify the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value.	R/W
b7, b6	TIOGT[1:0]	Count control *1, *2	b7 b6 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn. Other settings are prohibited.	R/W

Note 1. When AGTEEn is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby mode, the digital filter function cannot be used.

Table 24.3 AGTIOn I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) 1: Output is started at low (initialization level: low).
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured.
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Table 24.4 AGTOn output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initialization level: low) 1: Output is started at high (initialization level: high).

24.2.8 AGT Event Pin Select Register (AGTISR)

Address(es): AGT0.AGTISR 4008 400Dh, AGT1.AGTISR 4008 410Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	EEPS	AGTEEn polarity selection	0: An event is counted during the low-level period 1: An event is counted during the high-level period.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	位名称	Description	R/W
b1	—	Reserved	该位读取为0。写入值应为0。	R/W
b2	TOE	AGTOn输出使能	0：禁用AGTOn输出1：启用AGTOn输出。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b5, b4	TIPF[1:0]	输入过滤器 *3	b5b400：无滤波器01：滤波器在PCLKB1处采样0：滤波器在PCLKB8处采样11：滤波器在PCLKB32处采样。这些位指定AGTIOn输入的滤波器采样频率。如果对AGTIOn引脚的输入进行采样并且值连续匹配3次，则将该值作为输入值。	R/W
b7, b6	TIOGT[1:0]	计数控制 *1, *2	b7b600：始终计数事件01：在为AGTEEn指定的极性周期内计数事件。禁止其他设置。	R/W

Note 1. 使用AGTEEn时，可以通过AGTISR寄存器中的EEPS位选择计数事件的极性。
Note 2. TIOGT[1:0]位仅在事件计数器模式下启用。
Note 3. 在软件待机模式下执行事件计数器模式操作时，不能使用数字滤波器功能。

Table 24.3 AGTIOnIO边沿和极性切换

操作模式	Function
定时器模式	不曾用过
脉冲输出方式	0：高电平开始输出（初始化电平：高电平）1：低电平开始输出（初始化电平：低电平）。
事件计数器模式	0：上升沿计数1：下降沿计数。
脉宽测量模式	0：测量低电平宽度1：测量高电平宽度。
脉冲周期测量模式	0：从一个上升沿测量到下一个上升沿1：从一个下降沿测量到下一个下降沿。

Table 24.4 AGTOn输出极性切换

操作模式	Function
所有模式	0：低电平开始输出（初始化电平：低电平）1：高电平开始输出（初始化电平：高电平）。

24.2.8 AGT事件引脚选择寄存器(AGTISR)

Address(es): AGT0.AGTISR 4008 400Dh, AGT1.AGTISR 4008 410Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	EEPS	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	EEPS	AGTEEn极性选择	0：在低电平期间计数一个事件1：在高电平期间计数一个事件。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

24.2.9 AGT Compare Match Function Select Register (AGTCMSR)

Address(es): AGT0.AGTCMSR 4008 400Eh, AGT1.AGTCMSR 4008 410Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TOPOLB	TOEB	TCMEB	—	—	—	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCMEA	Compare match A register enable *1, *2	0: Compare match A register disabled 1: Compare match A register enabled.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TCMEB	Compare match B register enable *1, *2	0: Compare match B register disabled 1: Compare match B register enabled.	R/W
b5	TOEB	AGTOBn output enable *1, *2, *3	0: AGTOBn output disabled 1: AGTOBn output enabled.	R/W
b6	TOPOLB	AGTOBn polarity select *1, *2, *3	0: AGTOBn output is started on low 1: AGTOBn output is started on high.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).
Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.
Note 3. This bit is not available in AGT1.

24.2.10 AGT Pin Select Register (AGTIOSEL)

Address(es): AGT0.AGTIOSEL 4008 400Fh, AGT1.AGTIOSEL 4008 410Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TIES	—	—	SEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SEL[1:0]	AGTIOn Pin Select*1	b1 b0 0 0: Select the AGTIOn except for the following pins 0 1: Setting prohibited 1 0: Select the P402/AGTIOn. P402/AGTIOn is input only. It is not possible to output 1 1: Setting prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TIES	AGTIOn Input Enable	0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. You must set the Pin Function Select Register. See section 20, I/O Ports.

The AGTIOSEL register sets the AGTIOn pin when using the AGTIOn in Software Standby mode. The AGTIOSEL register can be set with an 8-bit memory manipulation instruction.

24.2.9 AGT比较匹配功能选择寄存器(AGTCSR)

Address(es): AGT0.AGTCMSR 4008 400Eh, AGT1.AGTCMSR 4008 410Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TOPOLB	TOEB	TCMEB	—	—	—	TCMEA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TCMEA	比较匹配A寄存器使能*1 *2	0：比较匹配A寄存器禁用1：比较匹配A寄存器启用。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	TCMEB	比较匹配B寄存器使能*1 *2	0：比较匹配B寄存器禁用1：比较匹配B寄存器启用。	R/W
b5	TOEB	AGTOBn输出使能*1 *2 *3	0：AGTOBn输出禁用1：AGTOBn输出使能。	R/W
b6	TOPOLB	AGTOBn极性选择*1、*2、*3	0：AGTOBn输出从低电平开始1：AGTOBn输出从高电平开始。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 在计数操作期间不要重写AGCTMSR寄存器。仅当AGTCR寄存器中的TSTART和TCSTF位都设置为0（计数停止）时才重写AGTCMSR寄存器。
Note 2. 在脉冲宽度测量模式或脉冲周期测量模式下不要设置为1。
Note 3. 该位在AGT1中不可用。

24.2.10 AGT引脚选择寄存器(AGTISEL)

Address(es): AGT0.AGTIOSEL 4008 400Fh, AGT1.AGTIOSEL 4008 410Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TIES	—	—	SEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	SEL[1:0]	AGTIOn Pin Select*1	b1b000：选择除以下引脚外的AGTIOn01：禁止设置10：选择P402AGTIOn。 P402AGTIOn仅为输入。不能输出11：禁止设定。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	TIES	AGTION输入启用	0：在软件待机模式下禁用外部事件输入1：在软件待机模式下启用外部事件输入。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 您必须设置引脚功能选择寄存器。请参阅第20节，IO端口。

当在软件待机模式下使用AGTIOn时，AGTIOSEL寄存器设置AGTIOn引脚。AGTIOSEL寄存器可以使用8位存储器操作指令进行设置。

SEL[1:0] bits (AGTIOn Pin Select)

The SEL[1:0] bits select the AGTIOn pin function.

TIES bit (AGTIOn Input Enable)

The TIES bit enables or disables an external event input.

24.3 Operation

24.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA or TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA and TCMEB bits are 0 (compare match A/B register are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or TCMEB bit is 1 (compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 24.2 and Figure 24.3 show the timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value.

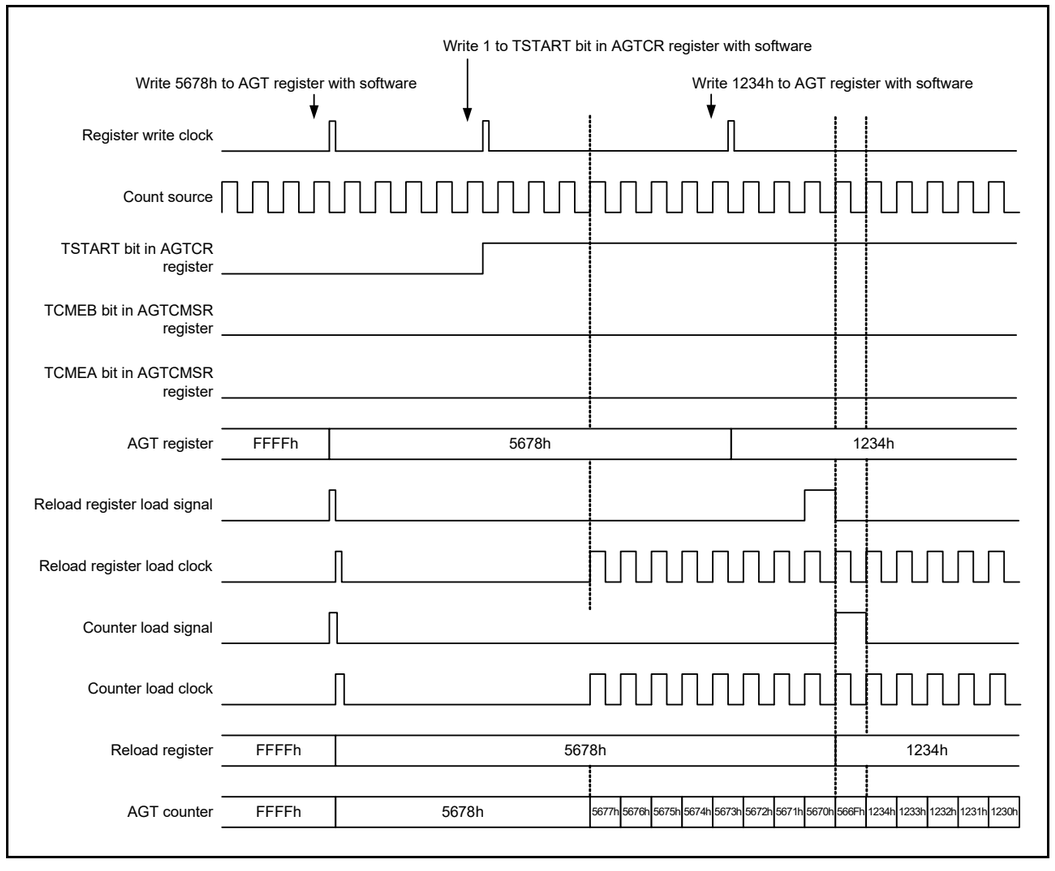


Figure 24.2 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when compare match A register or compare match B register is invalid

SEL[1:0]位（AGTIOn引脚选择）

SEL[1:0]位选择AGTIOn引脚功能。

TIES位（AGTION输入使能）

TIES位启用或禁用外部事件输入。

24.3 Operation

24.3.1 重载寄存器和计数器重写操作

无论操作模式如何，对重载寄存器和计数器的重写操作的时序根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEA或TCMEB位的值而有所不同。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和计数器。当TSTART位为1（计数开始）且TCMEA和TCMEB位为0（比较匹配AB寄存器无效）时，值与计数源同步写入重载寄存器，然后与计数源同步写入计数器下一个计数源。当TSTART位为1（计数开始）且TCMEA位或TCMEB位为1（比较匹配A寄存器或比较匹配B寄存器有效）时，该值与计数源同步写入重载寄存器，然后与计数器的下溢同步到计数器。

图24.2和图24.3显示了使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序。

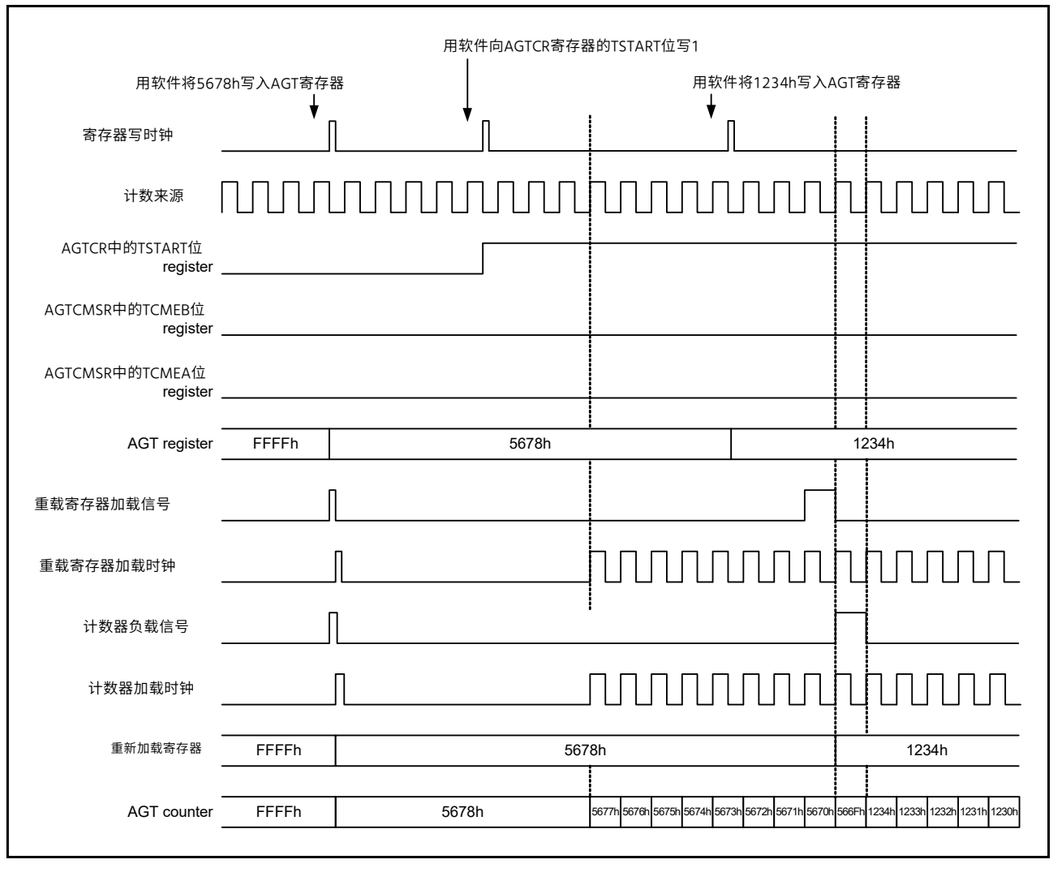


Figure 24.2 当比较匹配A寄存器或比较匹配B寄存器无效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

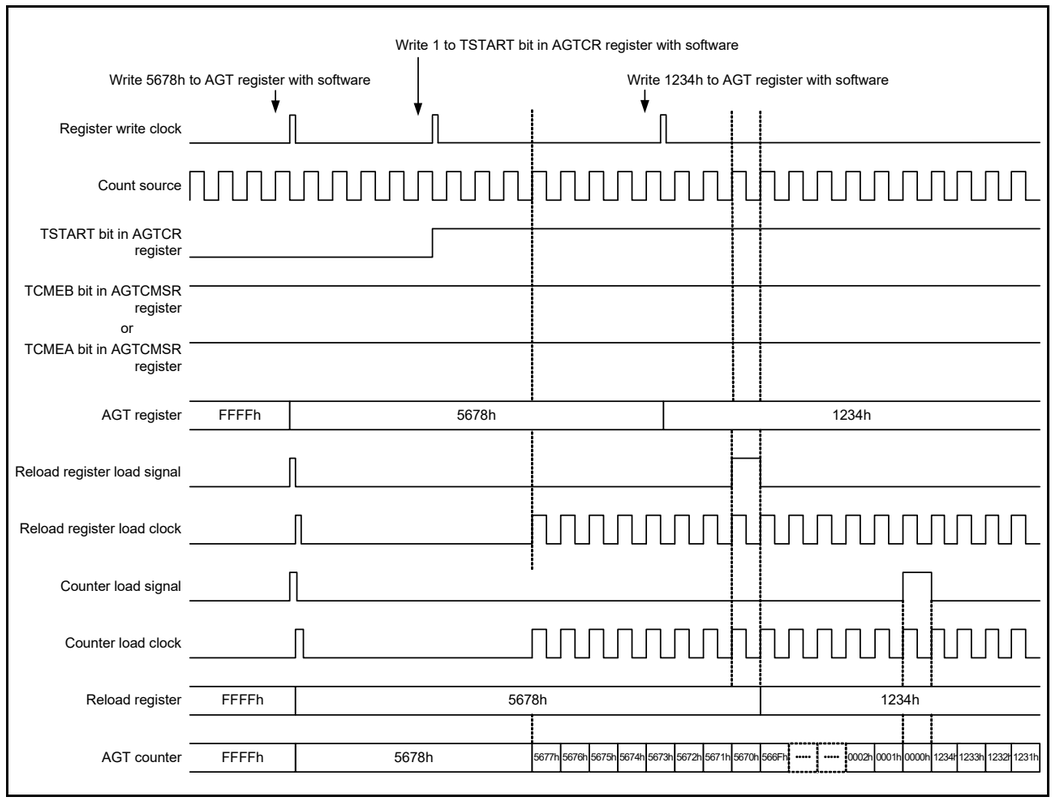


Figure 24.3 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when compare match A register or compare match B register is valid

24.3.2 Reload Register and Compare Register A/B Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 24.4 shows the timing of rewrite operation with TSTART bit value for compare register A. Compare register B is of the same timing as compare register A.

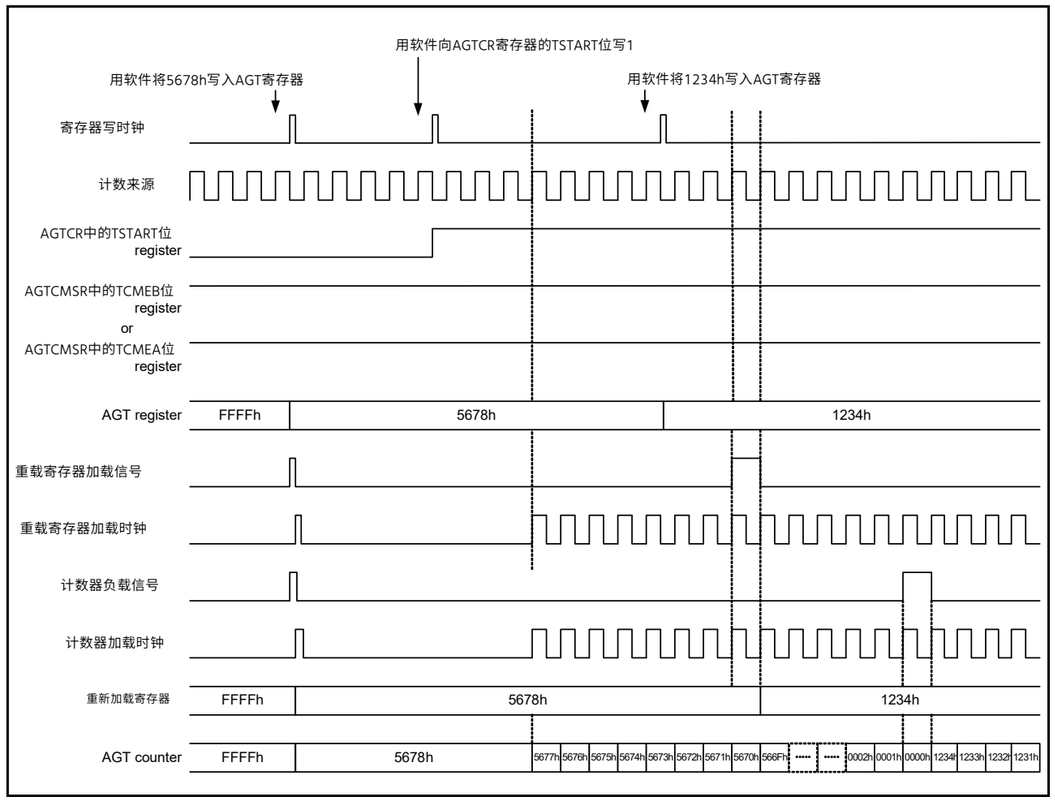


Figure 24.3 当比较匹配A寄存器或比较匹配B寄存器有效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

24.3.2 重载寄存器和比较寄存器AB重写操作

不管操作模式如何，对比较寄存器AB的重写操作的时序取决于AGTCR寄存器中TSTART位的值。当TSTART位为0（计数停止）时，将计数值直接写入重载寄存器和比较寄存器AB。当TSTART位为1（开始计数）时，将值同步写入重载寄存器计数源，然后与计数器的下溢同步到比较寄存器。

图24.4显示了比较寄存器A的TSTART位值的重写操作时序。比较寄存器B与比较寄存器A的时序相同。

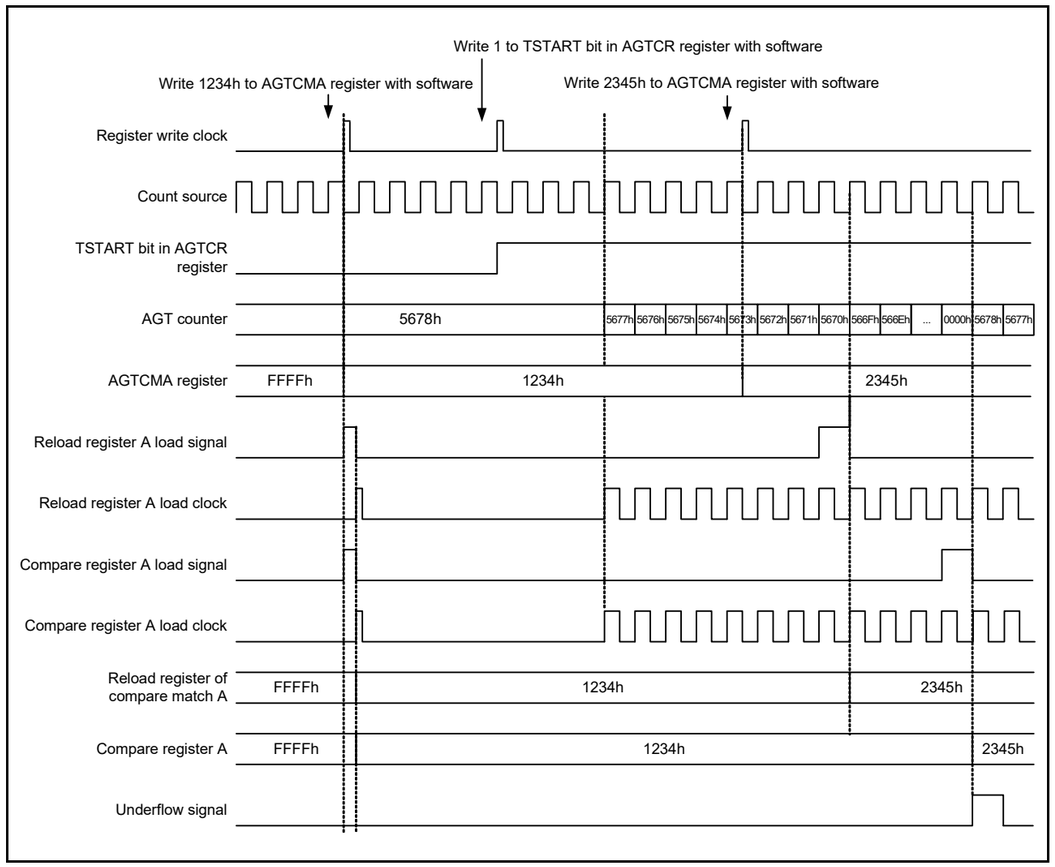


Figure 24.4 Timing of rewrite operation with the TSTART bit value for compare register A

24.3.3 Timer Mode

In this mode, the AGT counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 24.5 shows the operation example in timer mode.

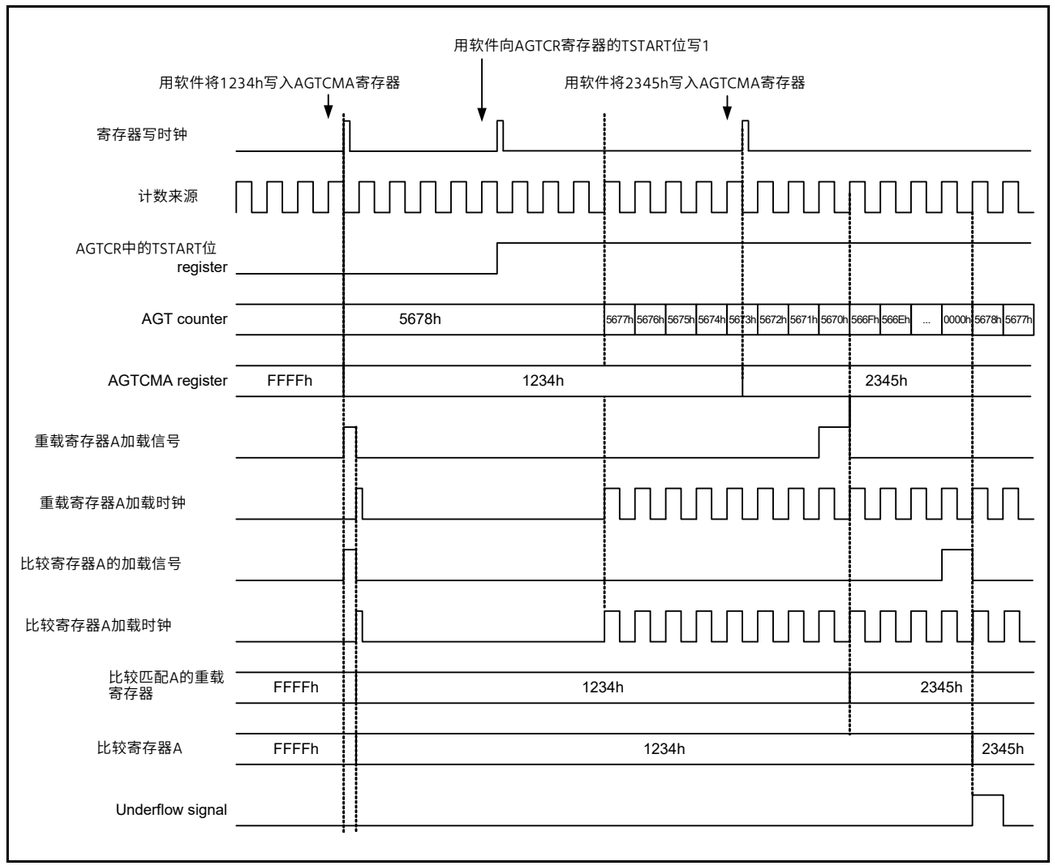


Figure 24.4 比较寄存器A的TSTART位值的重写操作时序

24.3.3 定时器模式

在此模式下，AGT计数器按AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。在定时器模式下，计数值在计数源的每个上升沿减1。当计数值达到0000h并输入下一个计数源时，发生下溢并产生中断请求。

图24.5显示了定时器模式下的操作示例。

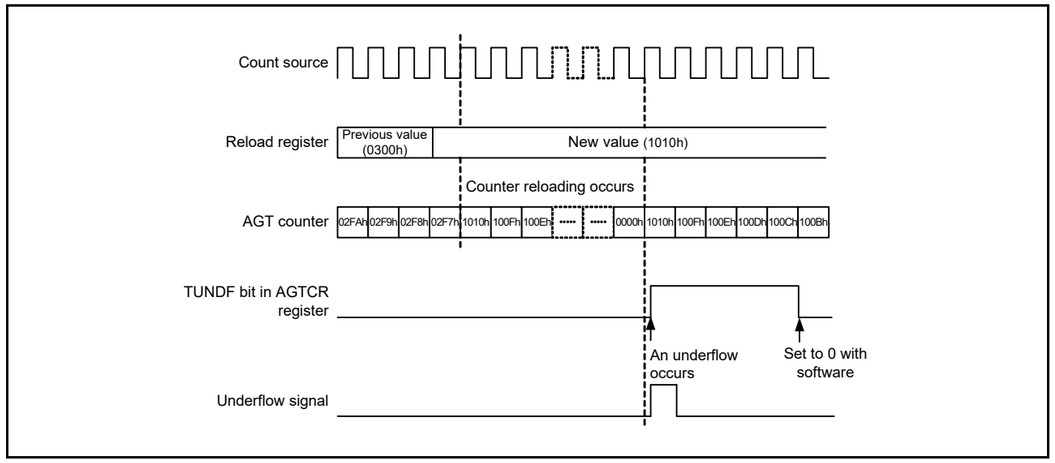


Figure 24.5 Operation example in timer mode

24.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and the output level of the AGTIOn and AGTOn pins inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 24.6 shows the operation example in pulse output mode.

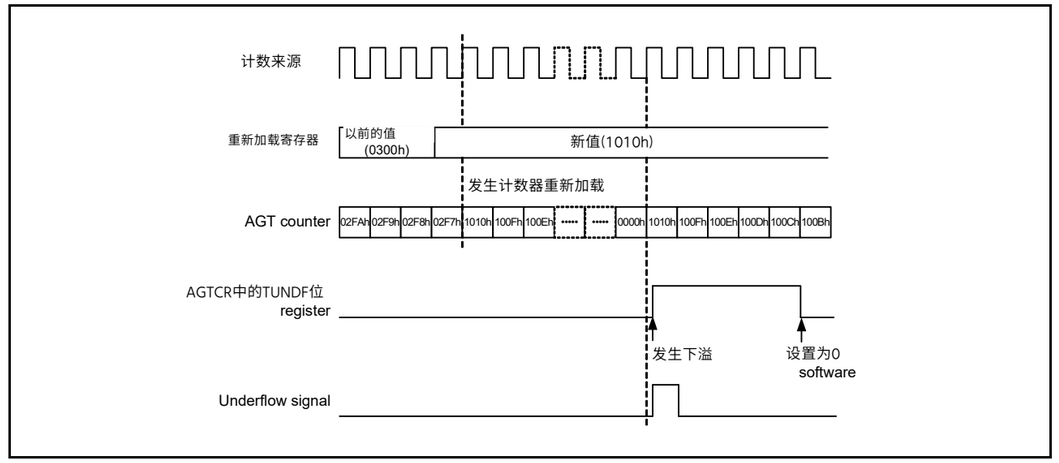


Figure 24.5 定时器模式下的操作示例

24.3.4 脉冲输出方式

在脉冲输出模式下，计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减，并且每次发生下溢时反转AGTIOn和AGTOn引脚的输出电平。

在脉冲输出模式下，计数值在计数源的每个上升沿减1。当计数值达到0000h并输入下一个计数源时，发生下溢并产生中断请求。此外，可以从AGTIOn和AGTOn引脚输出脉冲。每次发生下溢时，输出电平都会反转。AGTOn引脚的脉冲输出可通过AGTIOC寄存器中的TOE位停止。可以通过AGTIOC寄存器中的TEDGSEL位选择输出电平。

图24.6显示了脉冲输出模式下的操作示例。

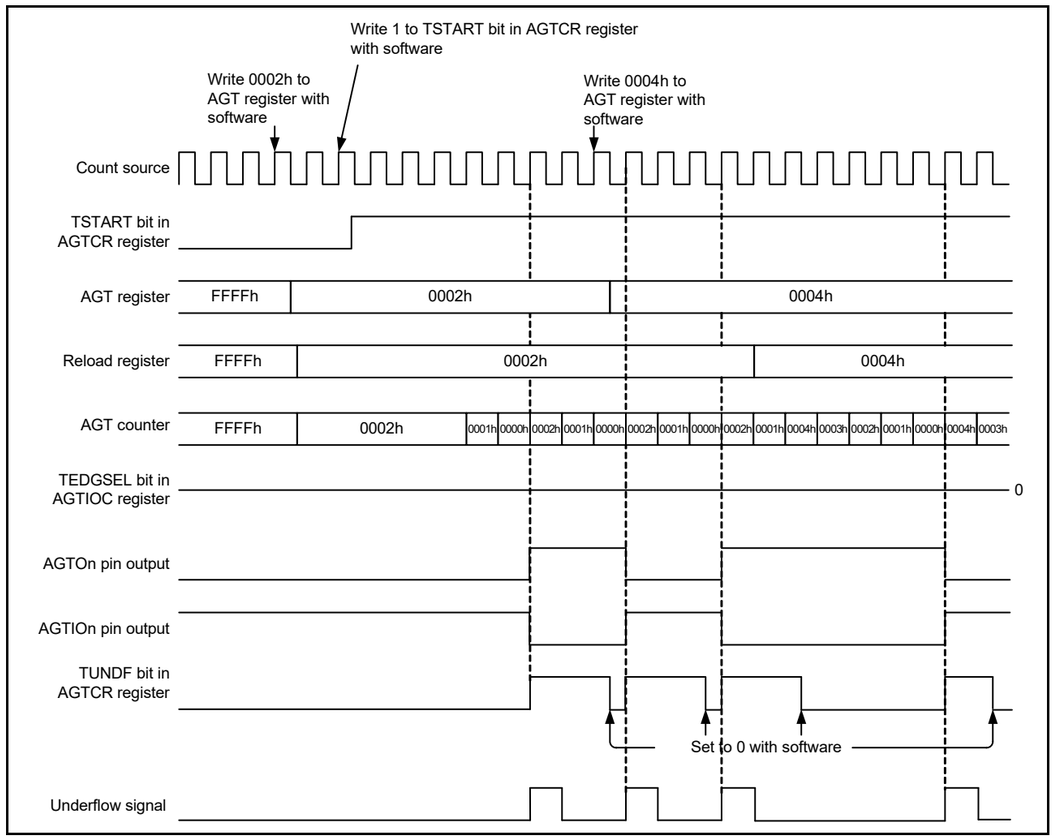


Figure 24.6 Operation example in pulse output mode

24.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal input to the AGTIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC and AGTISR registers. In addition, the filter function for the AGTIOn input can be specified with the TIPF[1:0] bits in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 24.7 shows the operation example in event counter mode.

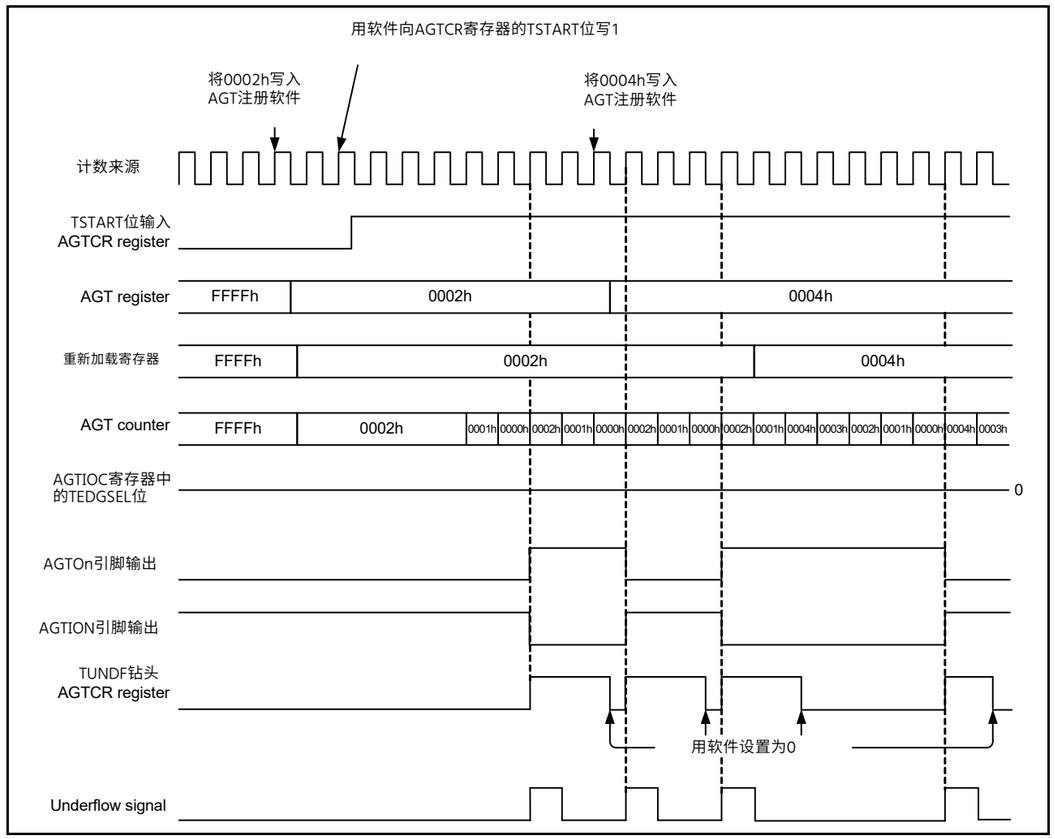


Figure 24.6 脉冲输出模式的动作示例

24.3.5 事件计数器模式

在事件计数器模式下，计数器由输入到AGTIOn引脚的外部事件信号递减。可以使用AGTIOC和AGTISR寄存器中的TIOGT[1:0]位设置计数事件的各种周期。此外，可以使用AGTIOC寄存器中的TIPF[1:0]位指定AGTIOn输入的过滤器功能。即使在事件计数器模式下，也可以切换AGTOn引脚的输出。

图24.7显示了事件计数器模式下的操作示例。

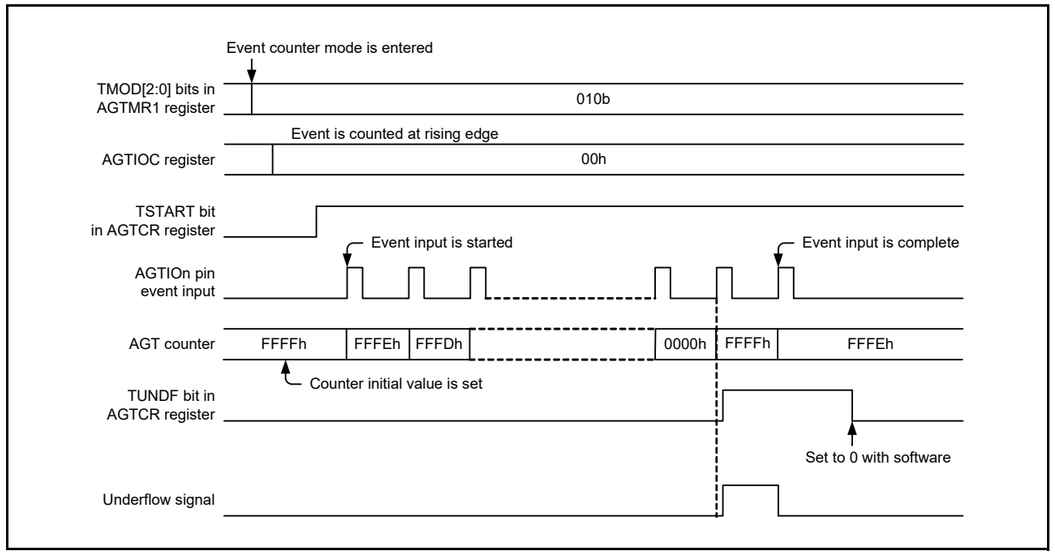


Figure 24.7 Operation example 1 in event counter mode

Figure 24.8 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).

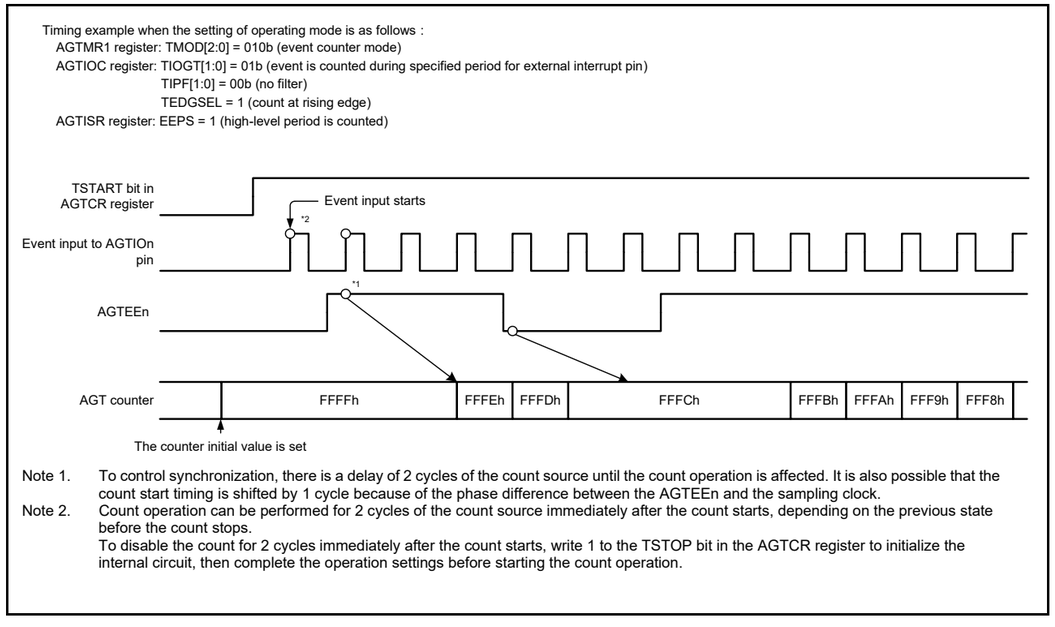


Figure 24.8 Operation example 2 in event counter mode

24.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin

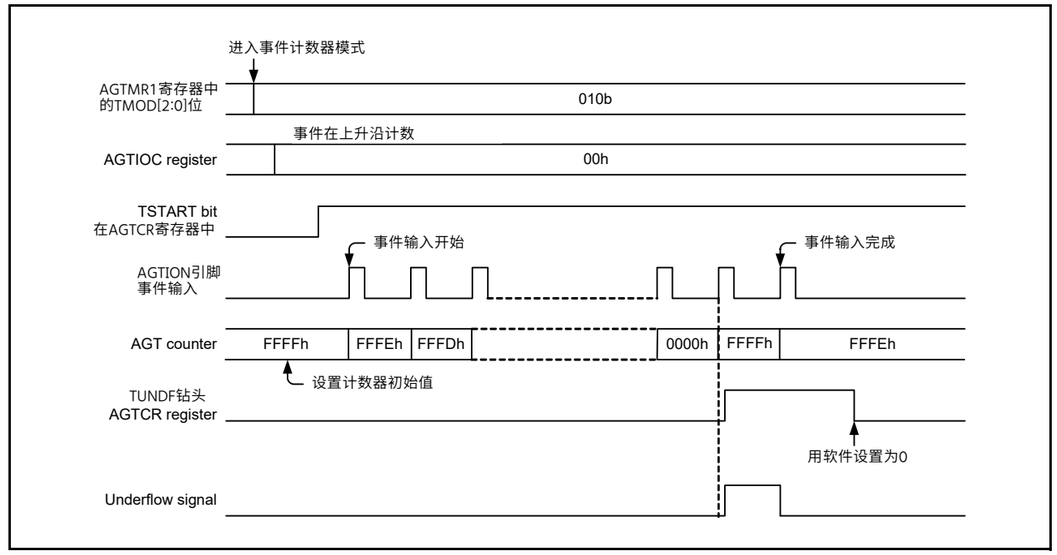


Figure 24.7 事件计数器模式下的操作示例1

图24.8显示了在事件计数器模式下在指定周期内进行计数的操作示例（AGTIOC寄存器中的TIOGT[1:0]位设置为01b）。

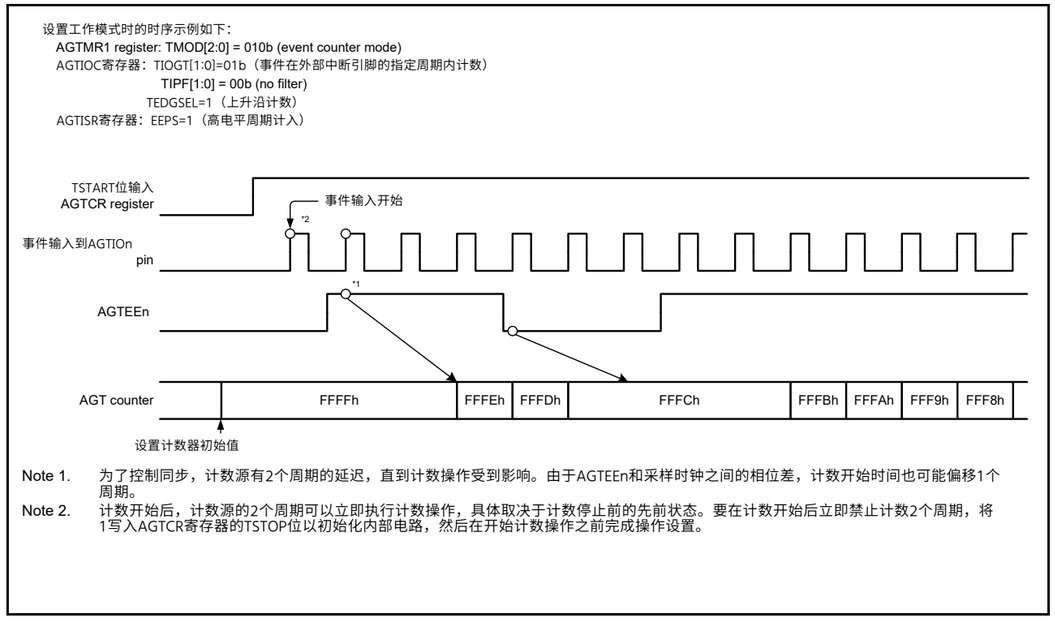


Figure 24.8 事件计数器模式下的操作示例2

24.3.6 脉冲宽度测量模式

在脉冲宽度测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲宽度。当AGTIOC寄存器中的TEDGSEL位指定的电平输入到AGTIOn引脚时，计数器会根据AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTIOn引脚上的指定电平

ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 24.9 shows the operation example in pulse width measurement mode.

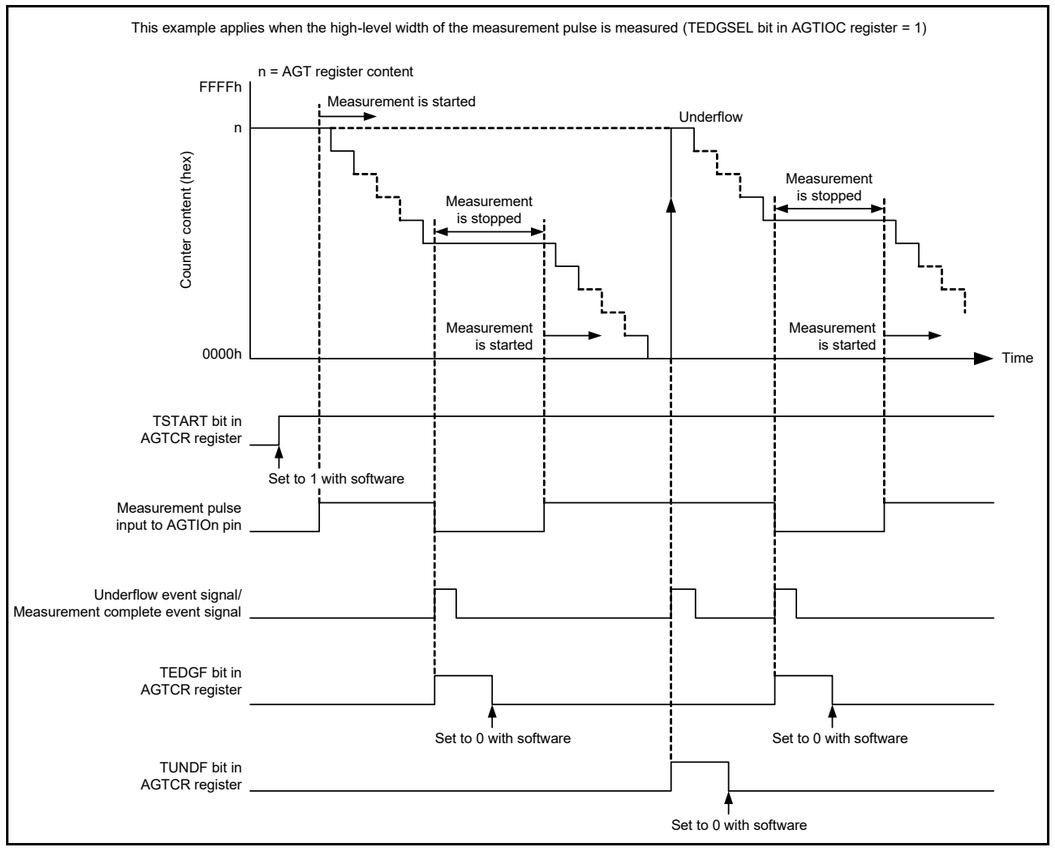


Figure 24.9 Operation example in pulse width measurement mode

24.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with TCK[2:0] bits in the AGTMR1 register. When a pulse with the period specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF bit in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 24.4.5, How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 24.10 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.

结束，计数器停止，AGTCR寄存器中的TEDGF位设置为1（接收到有效边沿），并产生中断请求。通过在计数器停止时读取计数值来执行脉冲宽度数据的测量。此外，当测量期间计数器下溢时，AGTCR寄存器中的TUNDF位设置为1，并产生中断请求。

图24.9显示了脉宽测量模式下的操作示例。

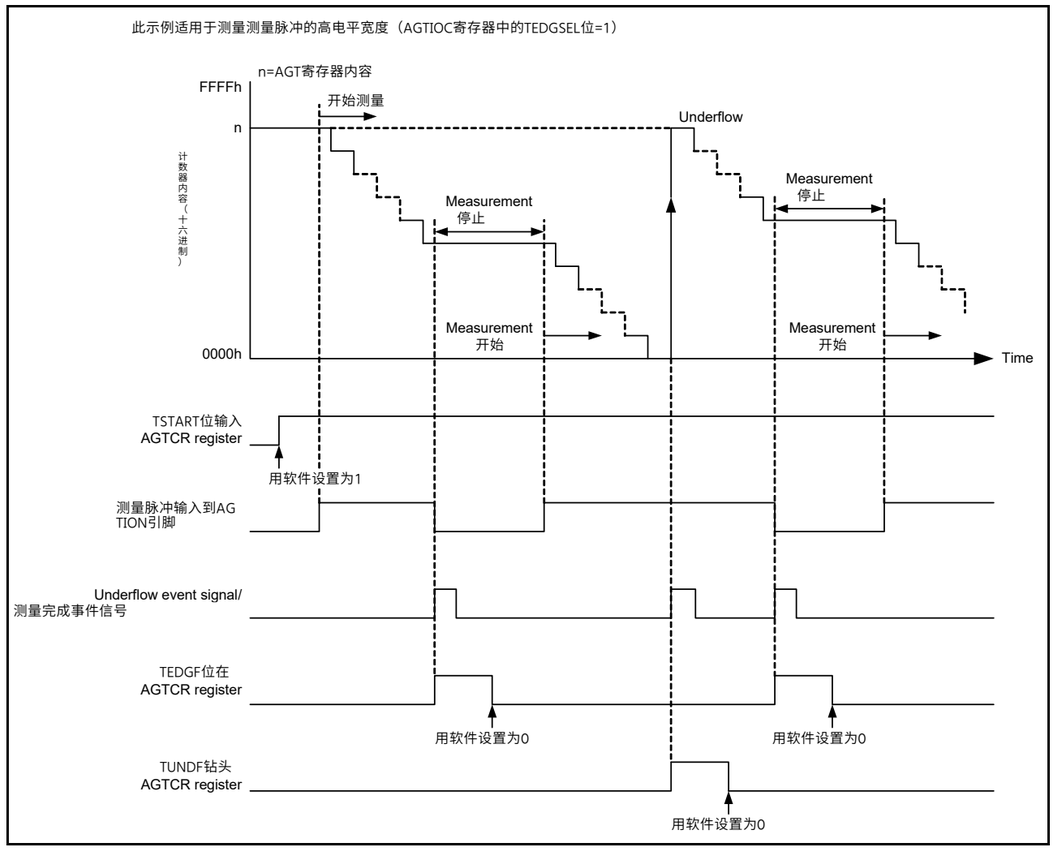


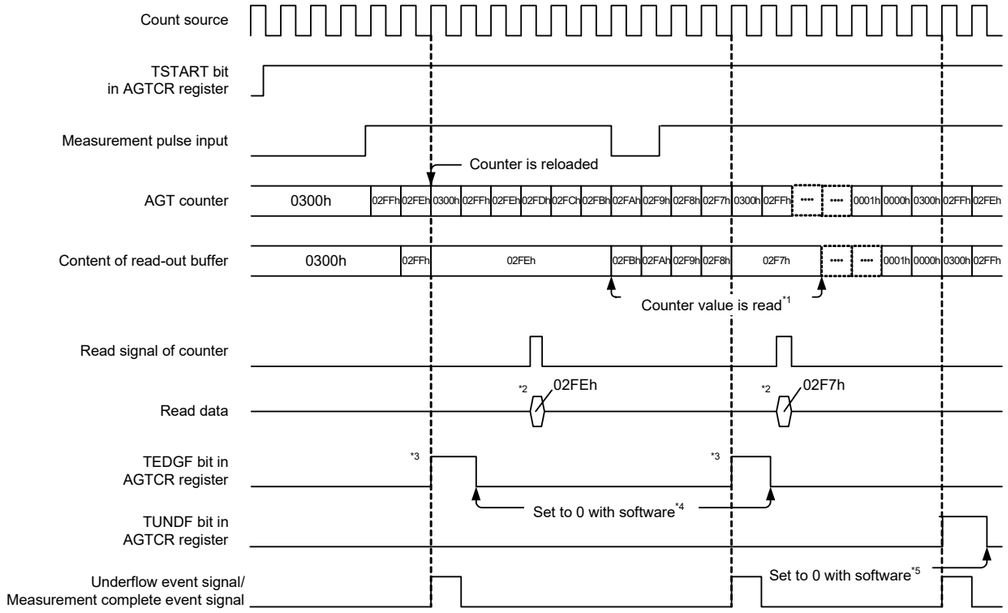
Figure 24.9 脉宽测量模式下的操作示例

24.3.7 脉冲周期测量模式

在脉冲周期测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲周期。计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTIOC寄存器中的TEDGSEL位指定周期的脉冲输入到AGTIOn引脚时，计数值在计数源的上升沿传送到读出缓冲器。重载寄存器中的值在下一个上升沿加载到计数器。同时，AGTCR寄存器中的TEDGF位设置为1（接收到有效边沿）并产生中断请求。此时读取读出缓冲区（AGT寄存器），与重载值的差值（参见第24.4.5节，如何计算事件数、脉冲宽度和脉冲周期）是输入脉冲的周期数据。周期数据被保留，直到读出缓冲器被读取。当计数器下溢时，AGTCR寄存器中的TUNDF位设置为1，并产生中断请求。

图24.10显示了脉冲周期测量模式下的操作示例。

仅测量周期长于计数源周期两倍的输入脉冲。此外，低电平和高电平宽度都必须长于计数源的周期。如果输入比这些条件短的脉冲周期，输入可能会被忽略。



This example applies when the initial value of the AGT register is set to 0300h, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse and the set edge of an external pulse are input, the TEDGF bit in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF bit in the AGTCR register using an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF bit in the AGTCR register using an 8-bit memory manipulation instruction.

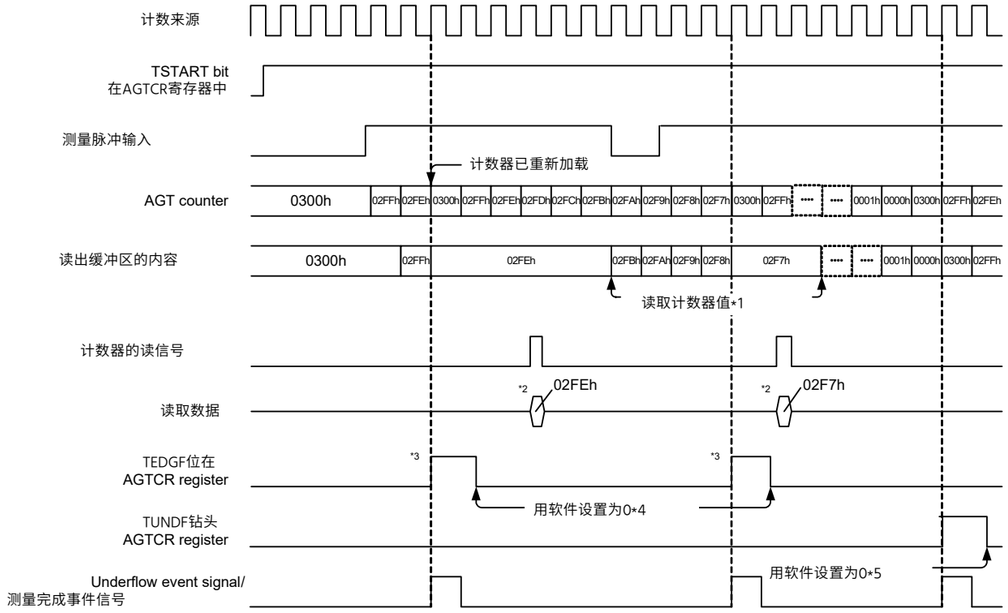
Figure 24.10 Operation example in pulse period measurement mode

24.3.8 Compare Match Function

The compare match function detects matches (compare match) between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF bit in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When the compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 24.3.1, Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOB0 pin is inverted by the match and by the underflow. The output level can be selected with the TOPOLB bit in the AGTCMSR register.

Figure 24.11 shows the operation example in compare match mode.



此示例适用于将AGT寄存器的初始值设置为0300h，将AGTIOC寄存器中的TEDGSEL位设置为0，并测量从一个上升沿到下一个测量脉冲沿的周期的情况。

Note 1. 从TEDGF位设置为1（接收到有效边沿）到输入下一个有效边沿期间，必须从AGT寄存器读取。读出缓冲器的内容一直保留到AGT寄存器被读取。如果在输入有效边沿之前未读取，则保留前一周期的测量结果。
Note 2. 在脉冲周期测量模式下读取AGT寄存器时，会读取读出缓冲区的内容。
Note 3. 当输入测量脉冲的有效边沿和外部脉冲的设置边沿时，AGTCR寄存器中的TEDGF位设置为1（接收到有效边沿）。
Note 4. 要使用软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TEDGF位。
Note 5. 要通过软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TUNDF位。

Figure 24.10 脉冲周期测量模式下的操作示例

24.3.8 比较匹配函数

比较匹配功能检测AGTCMA或AGTCMB寄存器的内容与AGT寄存器的内容之间的匹配（比较匹配）。该功能在AGTCMSR寄存器中的TCMEA或TCMEB位为1时使能（比较匹配A寄存器或比较匹配B寄存器有效）。计数器按AGTMR1寄存器中TCK[2:0]位选择的计数源递减，当AGT和AGTCMA或AGTCMB的值匹配时，AGTCR寄存器中的TCMAFTCMBF位设置为1（匹配），并产生中断请求。

当比较匹配功能启用时，对重载寄存器和计数器的重写操作的时序不同。有关详细信息，请参见第24.3.1节，重载寄存器和计数器重写操作。此外，AGTOB0引脚的输出电平通过匹配和下溢反转。输出电平可以通过AGTCMSR寄存器中的TOPOLB位来选择。

图24.11显示了比较匹配模式下的操作示例。

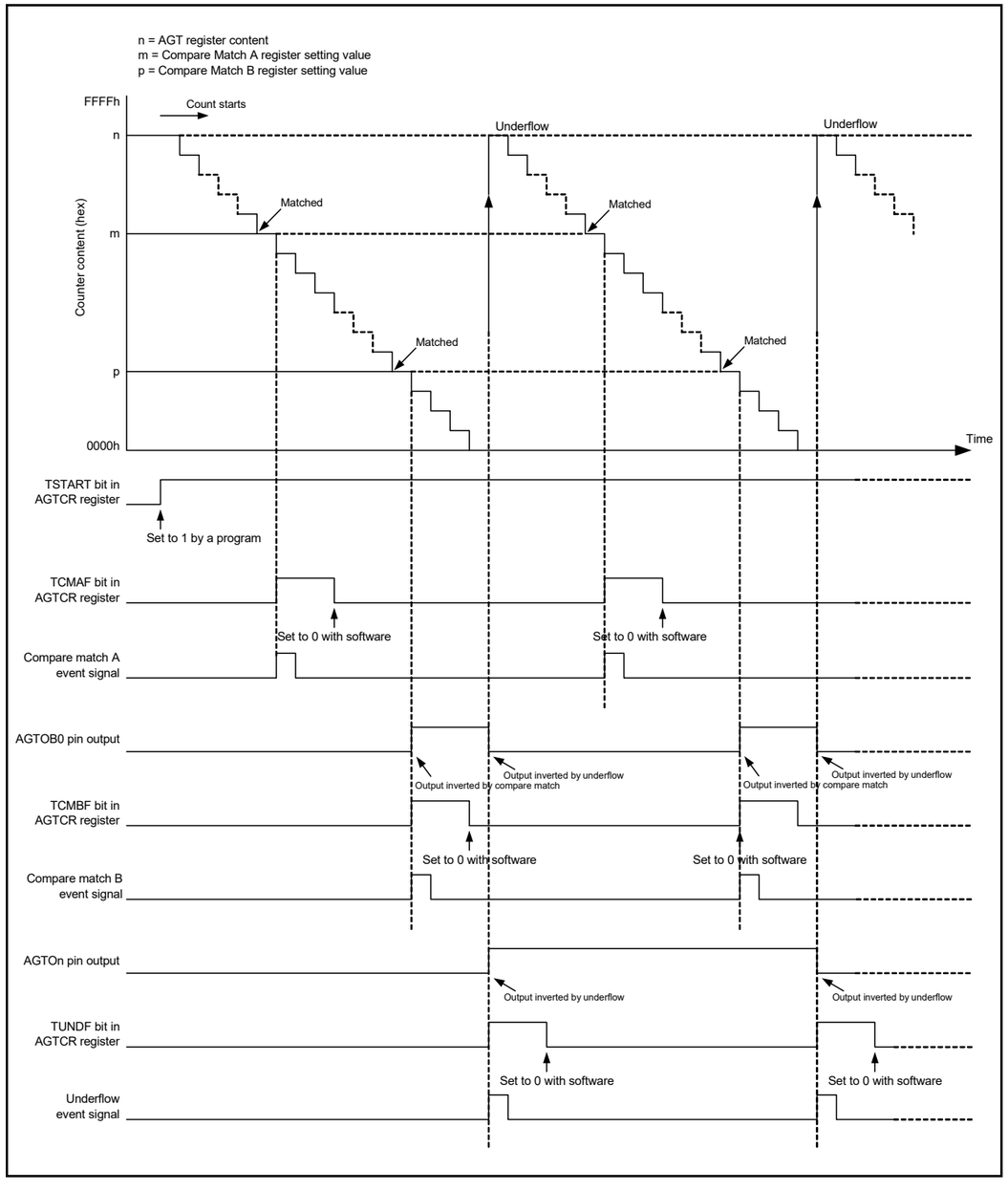


Figure 24.11 Operation example in compare match mode (TOPOLB = 0)

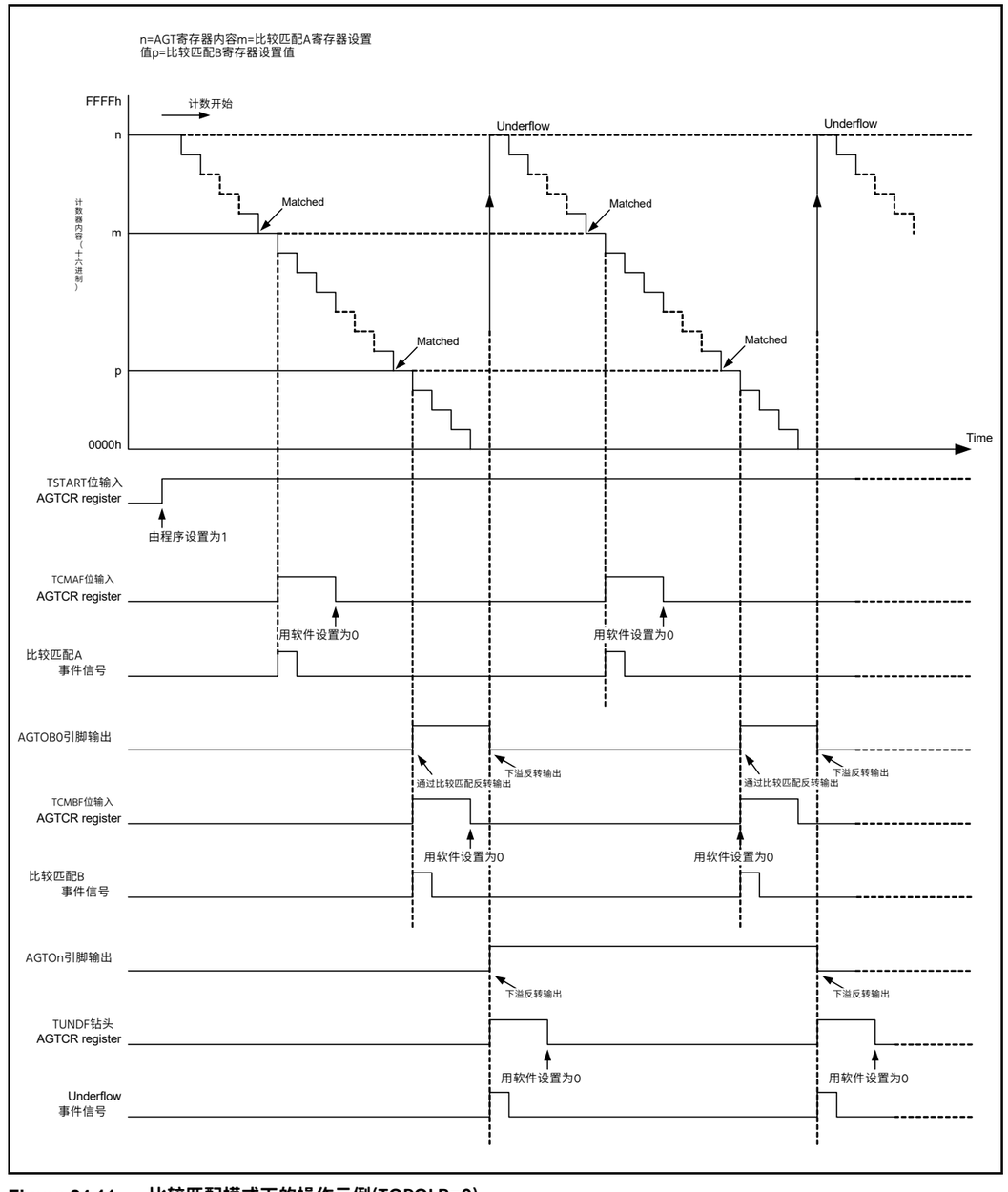


Figure 24.11 比较匹配模式下的操作示例(TOPOLB=0)

24.3.9 Output Settings for each Mode

Table 24.5 to Table 24.7 list the states of pins AGTOn, AGTIOn, and AGTOB0 in each mode.

Table 24.5 AGTOn pin setting

	AGTIOC register		
Operating mode	**TOE bit**	**TEDGSEL bit**	**AGTOn pin output**
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 24.6 AGTIOn pin setting

	AGTIOC register	
Operating mode	**TEDGSEL bit**	**AGTIOn pin I/O**
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 24.7 AGTOB0 pin setting

	AGTCMSR register		
Operating mode	**TOEB bit**	**TOPOLB bit**	**AGTOB0 pin output**
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

24.3.10 Standby Mode

The AGT can operate in Software Standby mode. Set it to Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 24.8 and Table 24.9 show the settings that can be used in Software Standby mode.

24.3.9 每种模式的输出设置

表24.5至表24.7列出了每种模式下引脚AGTOn、AGTIOn和AGTOB0的状态。

Table 24.5 AGTOn引脚设置

	AGTIOC register		
操作模式	**脚趾位**	**TEDGSEL bit**	**AGTOn引脚输出**
所有模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用

Table 24.6 AGTIOn引脚设置

	AGTIOC register	
操作模式	**TEDGSEL bit**	**AGTIOn pin I/O**
定时器模式	0 or 1	Input (not used)
脉冲输出方式	1	正常输出
	0	反相输出
事件计数器模式	0 or 1	Input
脉宽测量模式		
脉冲周期测量模式		

Table 24.7 AGTOB0引脚设置

	AGTCMSR register		
操作模式	**TOEB bit**	**TOPOLB bit**	**AGTOB0引脚输出**
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

24.3.10 待机模式

AGT可以在软件待机模式下运行。将其设置为软件待机模式，计数操作开始（TSTART=1，TCSTF=1）。

表24.8和表24.9显示了可在软件待机模式下使用的设置。

Table 24.8 Usable setting in Software Standby mode (AGT0)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	–
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	–
Event counter mode	– (invalid)	AGTIOn	–
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	–
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	–

Table 24.9 Usable setting in Software Standby mode (AGT1)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Event counter mode	– (invalid)	AGTIOn	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge

Note: Release of Software Standby mode is only AGT1.
Note 1. Only when AGT0 operates in Table 24.8.

24.3.11 Interrupt Sources

The AGT has three interrupt sources for channels n (n = 0, 1) as listed in Table 24.10.

Table 24.10 AGT interrupt sources

Name	Interrupt source	DMAC/DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input (AGTIOn) is complete in pulse width measurement mode • When the set edge of the external input (AGTIOn) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	When the values of AGT and AGTCMA match	Possible
AGTn_AGTCMBI	When the values of AGT and AGTCMB match	Possible

Note: Channel number (n = 0, 1).

24.3.12 Event Signal Output to ELC

The AGT uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGT outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 19, Event Link Controller (ELC).

24.4 Usage Notes

24.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 24.1) is set to other than the event counter mode, or the count source is set to other than AGT0 underflow (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF

Table 24.8 软件待机模式下的可用设置(AGT0)

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 110b	AGTLCLK or AGTSCLK	–
脉冲输出方式	100b or 110b	AGTLCLK or AGTSCLK	–
事件计数器模式	– (invalid)	AGTIOn	–
脉宽测量模式	100b or 110b	AGTLCLK or AGTSCLK	–
脉冲周期测量模式	100b or 110b	AGTLCLK or AGTSCLK	–

Table 24.9 软件待机模式下的可用设置(AGT1)

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 比较匹配AB
脉冲输出方式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 比较匹配AB
事件计数器模式	– (invalid)	AGTIOn	下溢 比较匹配AB
脉宽测量模式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 活动边沿
脉冲周期测量模式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 活动边沿

Note: 软件待机模式的释放只有AGT1。
Note 1. 仅当AGT0在表24.8中运行时。

24.3.11 中断源

AGT具有三个用于通道n(n=0 1)的中断源，如表24.10中所列。

Table 24.10 AGT中断源

Name	中断源	DMAC/DTC activation
AGTn_AGTI	当计数器下溢时 当在脉冲宽度测量模式下完成外部输入(AGTIOn)的有效宽度测量时 当在脉冲周期测量模式下输入外部输入(AGTIOn)的设置边沿时。	Possible
AGTn_AGTCMAI	当AGT和AGTCMA的值匹配时	Possible
AGTn_AGTCMBI	当AGT和AGTCMB的值匹配时	Possible

Note: 通道号(n=0 1)。

24.3.12 事件信号输出到ELC

AGT使用事件链接控制器(ELC)使用中断请求信号作为事件信号执行到指定模块的链接操作。AGT输出比较匹配A、比较匹配B和下溢测量完成信号作为事件信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

24.4 使用说明

24.4.1 计数操作启动和停止控制

- 当操作模式（见表24.1）设置为非事件计数器模式，或计数源设置为非AGT0下溢（TCK[2:0]=101b）时：
  - 当计数停止时，将1（计数开始）写入AGTCR寄存器的TSTART位后，TCSTF

bit in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).

- After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 3 cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 0.
- Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 14, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR.

- When the operating mode (see Table 24.1) is set to event counter mode, or the count source is set to AGT0 underflow (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF bit in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 2 PCLKB cycles. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 14, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR.

24.4.2 Access to Counter Register

When the TSTART and TCSTF bits in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

24.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, AGTCMSR, and AGTIOC) can be changed only when the count is stopped with both the TSTART and TCSTF bits set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of TEDGF, TUNDF, TCMAF, and TCMBF bits are undefined. Before starting the count, write 0 to the following bits:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

24.4.4 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

24.4.5 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement

AGTCR寄存器中的位在计数源的3个周期内保持为0（计数停止）。不要访问除TCSTF位之外的与AGT*1关联的寄存器，直到该位设置为1（正在进行计数）。

- 在计数操作期间将0（计数停止）写入TSTART位后，TCSTF位在计数源的3个周期内保持为1。当TCSTF位设置为0时，停止计数。在此位设置为0之前，请勿访问与AGT*1相关的寄存器，而不是TCSTF位。
- 在将TSTART位从0更改为1之前清除中断寄存器。参见第14节，中断控制器单位(ICU)了解详情。

注1.与AGT相关的寄存器：AGT、AGTCMA、AGTCMB、AGTCR、AGTMR1、AGTMR2、AGTIOC、AGTISR和AGTCMSR。

- 当操作模式（见表24.1）设置为事件计数器模式，或计数源设置为AGT0下溢（TCK[2:0]=101b）时：
  - 在停止计数的同时将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF位保持0（计数停止）2个PCLKB周期。不要访问除TCSTF位之外的与AGT*1关联的寄存器，直到该位设置为1（正在进行计数）。
  - 在计数操作期间将0（计数停止）写入TSTART位后，TCSTF位保持1持续2 PCLKB周期。当TCSTF位设置为0时，停止计数。不要访问与相关的寄存器AGT*1除了TCSTF位之外，直到该位设置为0。
  - 在将TSTART位从0更改为1之前清除中断寄存器。参见第14节，中断控制器单位(ICU)了解详情。

注1.与AGT相关的寄存器：AGT、AGTCMA、AGTCMB、AGTCR、AGTMR1、AGTMR2、AGTIOC、AGTISR和AGTCMSR。

24.4.2 访问计数器寄存器

当AGTCR寄存器中的TSTART和TCSTF位都为1（计数开始）时，连续写入AGT寄存器时，在两次写入之间至少允许计数源时钟的3个周期。

24.4.3 更改模式时

与AGT操作模式相关的寄存器（AGTMR1、AGTMR2、AGTIOC、AGTISR、AGTCMSR和只有在TSTART和TCSTF位都设置为0（计数停止）的情况下停止计数时才能更改AGTIOC）。在计数操作期间不要更改这些寄存器。

当与AGT工作模式相关的寄存器发生变化时，TEDGF、TUNDF、TCMAF和TCMBF位未定义。在开始计数之前，将0写入以下位：

- TEDGF（未收到有效边沿）
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

24.4.4 数字滤波器

使用数字滤波器时，在设置TIPF[1:0]位后以及AGTIOC寄存器中的TEDGSEL位发生变化时，在数字滤波器时钟的5个周期内不要启动定时器操作。

24.4.5 如何计算事件编号、脉冲宽度和脉冲周期

- 在事件计数器模式下，事件编号以数学方式表示如下：
  事件编号=计数器的初始值[AGT寄存器]活动事件结束的计数器值
- 在脉冲宽度测量模式下，脉冲宽度在数学上表示如下：
  脉冲宽度=停止测量的计数器值下一个停止测量的计数器值

- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1

24.4.6 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

24.4.7 When Selecting AGT0 Underflow as the Count Source

Operate the AGT according to the procedures described in this section when selecting the underflow signal of AGT as the count source.

(1) Procedure for starting operation

1. Set AGT0 and AGT1.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1 (write 000b in the AGT1.AGTMR1.TCK[2:0] bits).

24.4.8 Reset of I/O Register

The I/O register of the AGT is not initialized by different types of resets. For details, see section 6, Resets.

24.4.9 When Selecting PCLKB, PCLKB/8, or PCLKB/2 as the Count Source

When a reset is generated, the operation of the AGT cannot be guaranteed. Set the registers associated with AGT again.

24.4.10 When Selecting AGTLCLK or AGTSCLK as the Count Source

The MSTPD2 bit in the MSTPCRD register must be set to 1 except when accessing the AGT1 registers. The MSTPD3 bit in the MSTPCRD register must be set to 1 except when accessing the AGT0 registers. When a reset occurs while MSTPD2 or MSTPD3 is 0, the operation of AGT1 or AGT0 cannot be guaranteed. Set the registers associated with AGT again.

24.4.11 When Switching Source Clock

When switching a clock source by changing SCKCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTIOn, AGTEEn, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

- 在脉冲周期测量模式下，输入脉冲周期在数学上表示如下：
  输入脉冲周期=（计数器初始值[AGT寄存器]读出缓冲器的读取值）+1

24.4.6 当计数被TSTOP位强制停止时

计数器被AGTCR寄存器中的TSTOP位强制停止后，在计数源的1个周期内不要访问以下IO寄存器：

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

24.4.7 选择AGT0下溢作为计数源时

选择AGT的下溢信号作为计数源时，请按照本节所述的步骤操作AGT。

(1) 开始运行的步骤

1. 设置AGT0和AGT1。
2. 启动AGT1的计数操作。
3. 启动AGT0的计数操作。

(2) 停止运行的步骤

1. 停止AGT0的计数操作。
2. 停止AGT1的计数操作。
3. 停止AGT1的计数源时钟（在AGT1.AGTMR1.TCK[2:0]位中写入000b）。

24.4.8 IO寄存器的复位

AGT的IO寄存器不会被不同类型的复位初始化。有关详细信息，请参阅第6节，重置。

24.4.9 选择PCLKB、PCLKB8或PCLKB2作为计数源时

当产生复位时，不能保证AGT的操作。再次设置与AGT关联的寄存器。

24.4.10 选择AGTLCLK或AGTSCLK作为计数源时

除了访问AGT1寄存器时，MSTPCRD寄存器中的MSTPD2位必须设置为1。除了访问AGT0寄存器时，MSTPCRD寄存器中的MSTPD3位必须设置为1。当MSTPD2或MSTPD3为0时发生复位时，不能保证AGT1或AGT0的操作。再次设置与AGT关联的寄存器。

24.4.11 切换源时钟时

当通过改变SCKCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。因此，当使用AGTIOn、AGTEEn或两者输入作为外部事件输入时，不应切换时钟源。如果在使用外部事件输入时切换时钟源，请将输入脉冲宽度延长4个切换源时钟周期的时钟周期。

25. Realtime Clock (RTC)

25.1 Overview

The RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100 year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

The sub-clock oscillator or LOCO can be selected as the count source of the time counters. The RTC uses a 128-Hz clock acquired by dividing the count source by a prescaler. Year, month, date, day-of-week, a.m./p.m. (in 12-hour mode), hour, minute, second, or 32-bit binary is counted by 1/128 second.

Note: Regardless of the use of VBATT function, set the VBTCR1.BPWSWSTP bit to 1 before accessing the RTC registers after cold start. For details, see Figure 12.2, Setting flow of the VBTCR1.BPWSWSTP bit, in section 12, Battery Backup Function.

Table 25.1 lists the RTC specifications, Figure 25.1 shows a block diagram, and Table 25.2 lists the I/O pins.

Table 25.1 RTC specifications

Parameter	Description
Count mode	Calendar count mode/binary count mode
Count source*1	Sub-clock oscillator (XCIN) or LOCO
Clock and calendar functions	• Calendar count mode Year, month, date, day of week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute) Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes Start/stop function The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz) Clock error correction function Clock (1-Hz/64-Hz) output.
Interrupts	• Alarm interrupt (RTC_ALM) As an alarm interrupt condition, selectable for comparison with the following: Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (RTC_PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period • Carry interrupt (RTC_CUP) An interrupt is generated at either of the following conditions: - When a carry from the 64-Hz counter to the second counter is generated - When the 64-Hz counter is changed and the R64CNT register is read at the same time • Return from Software Standby mode can be performed by an alarm interrupt or periodic interrupt.
Time capture function	• Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or the 32-bit binary counter value is captured.
Event link function	Periodic event output (RTC_PRD)

Note 1. The frequency of the peripheral module clock (PCLKB) must be ≥ the frequency of the count source clock.

25. 实时时钟(RTC)

25.1 Overview

RTC有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。

可以选择子时钟振荡器或LOCO作为时间计数器的计数源。RTC使用一个128-Hz时钟，通过预分频器将计数源分频获得。年、月、日、星期、上午、下午（在12小时模式下）时、分、秒或32位二进制按1128秒计数。

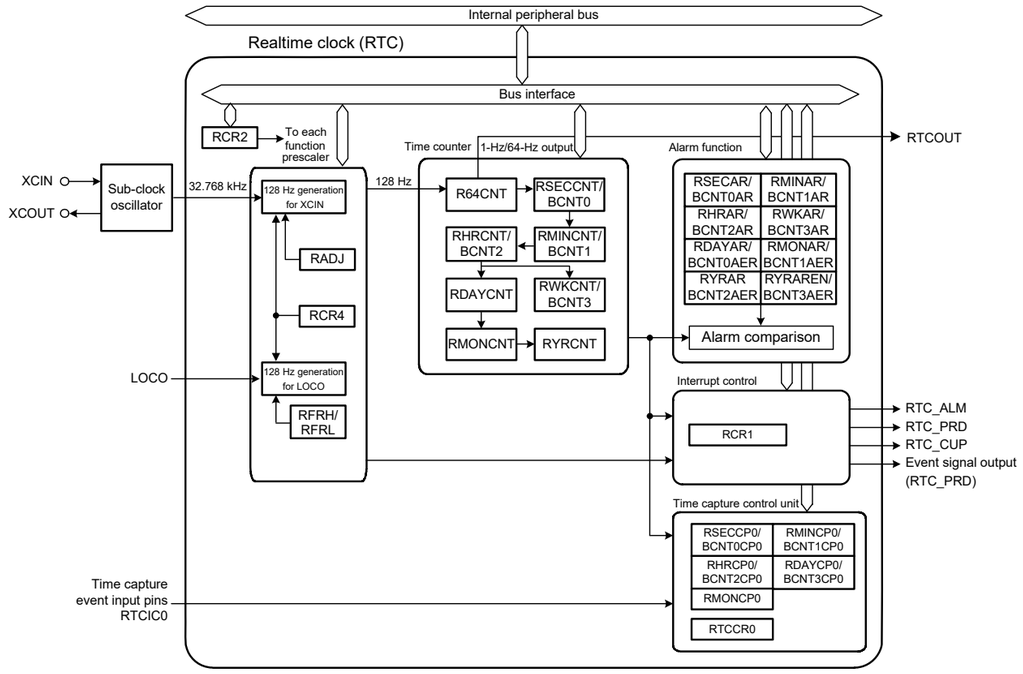
Note: 无论使用VBATT功能，在冷启动后访问RTC寄存器之前将VBTCR1.BPWSWSTP位设置为1。有关详细信息，请参见第12节"电池备份功能"中的图12.2，VBTCR1.BPWSWSTP位的设置流程。

表25.1列出了RTC规范，图25.1显示了框图，表25.2列出了IO引脚。

Table 25.1 RTC specifications

Parameter	Description
计数模式	日历计数模式二进制计数模式
Count source*1	副时钟振荡器(XCIN)或LOCO
时钟和日历功能	日历计数模式 年、月、日、星期、时、分、秒计数，BCD显示12小时24小时模式切换功能30秒调整功能（小于30的数字向下舍入为00秒，大于等于30秒为四舍五入到1分钟）闰年自动调整功能 二进制计数模式 以32位计数秒，二进制显示 两种模式通用 启动停止功能 亚秒数字以二进制单位显示（1Hz、2Hz、4Hz、8Hz、16Hz、32Hz或64Hz） 时钟纠错功能 时钟(1-Hz64-Hz)输出。
Interrupts	报警中断(RTC_ALM) 作为报警中断条件，可选择用于与以下比较： 日历计数模式：可选择年、月、日、星期、小时、分钟或秒 二进制计数模式：32位二进制计数器的每一位 周期性中断(RTC_PRD) 可以选择2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒作为中断周期 进位中断（RTC_CUP） 在以下任一情况下会产生中断：当从64-Hz计数器到第二个计数器产生进位时当64-Hz计数器改变并同时读取R64CNT寄存器时 从软件待机模式返回可以通过报警中断或周期性中断来执行。
时间捕捉功能	当检测到时间捕捉事件输入引脚的边沿时，可以捕捉时间。 对于每个事件输入，都会捕获月、日、小时、分钟和秒，或者捕获32位二进制计数器值。
事件链接功能	周期性事件输出(RTC_PRD)

Note 1. 外围模块时钟(PCLKB)的频率必须是 计数源时钟的频率。



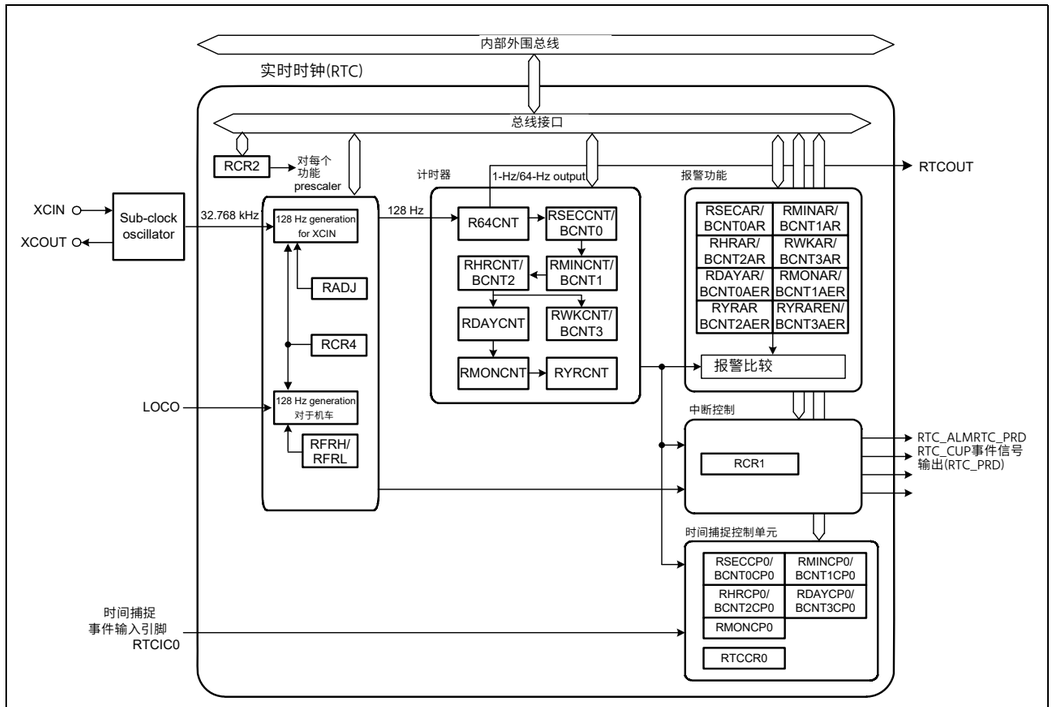
R64CNT: 64-Hz Counter
RSECCNT/BCNT0: Second Counter/Binary Counter 0
RMINCNT/BCNT1: Minute Counter/Binary Counter 1
RHRCNT/BCNT2: Hour Counter/Binary Counter 2
RWKCNT/BCNT3: Day-of-Week Counter/Binary Counter 3
RDAYCNT: Date Counter
RMONCNT: Month Counter
RYRCNT: Year Counter
RCR1: RTC Control Register 1
RCR2: RTC Control Register 2
RCR4: RTC Control Register 4
RADJ: Time Error Adjustment Register
RFRH/RFRL: Frequency Register

RSECAR/BCNT0AR: Second Alarm Register/Binary Counter 0 Alarm Register
RMINAR/BCNT1AR: Minute Alarm Register/Binary counter 1 Alarm Register
RHRAR/BCNT2AR: Hour Alarm Register/Binary Counter 2 Alarm Register
RWKAR/BCNT3AR: Day-of-week Alarm Register/Binary Counter 3 Alarm Register
RDAYAR/BCNT0AER: Date Alarm Register/Binary Counter 0 Alarm Enable Register
RMONAR/BCNT1AER: Month Alarm Register/Binary Counter 1 Alarm Enable Register
RYRAR/BCNT2AER: Year Alarm Register/Binary Counter 2 Alarm Enable Register
RYRAREN/BCNT3AER: Year Alarm Enable Register/Binary Counter 3 Alarm Enable Register
RTCCR0: Time Capture Control Register 0
RSECCPn/BCNT0CP0: Second Capture Register n/BCNT0 Capture Register 0
RMINCPn/BCNT1CP0: Minute Capture Register n/BCNT1 Capture Register 0
RHRCPn/BCNT2CP0: Hour Capture Register n/BCNT2 Capture Register 0
RDAYCPn/BCNT3CP0: Date Capture Register n/BCNT3 Capture Register 0
RMONCP0: Month Capture Register 0

Figure 25.1 RTC block diagram

Table 25.2 RTC I/O pins

Pin name	I/O	Function
XCIN	Input	Connect a 32.768-kHz crystal to these pins
XCOUT	Output	
RTCOUT	Output	This pin is used to output a 1-Hz/64-Hz waveform
RTCIC0	Input	Time capture event input pins



R64CNT：64Hz计数器RSECCNTBCNT0：秒计数器二进制计数器0RMINCNTBCNT1：分计数器二进制计数器1
RHRCNT/BCNT2: 小时计数器二进制计数器2
RWKCNT/BCNT3: Day-of-Week Counter/Binary Counter 3
RDAYCNT: 日期计数器
RMONCNT: 月计数器
RYRCNT: 年计数器
RCR1: RTC控制寄存器1
RCR2: RTC控制寄存器2
RCR4: RTC控制寄存器4
RADJ: 时间误差调整寄存器
RFRH/RFRL: 频率寄存器

RSECAR/BCNT0AR: 第二个报警寄存器二进制计数器0报警寄存器
RMINAR/BCNT1AR: 分钟报警寄存器二进制计数器1报警寄存器
RHRAR/BCNT2AR: 小时报警寄存器二进制计数器2报警寄存器
RWKAR/BCNT3AR: 星期报警寄存器二进制计数器3报警寄存器
RDAYAR/BCNT0AER: 日期报警寄存器二进制计数器0报警使能寄存器
RMONAR/BCNT1AER: 月报警寄存器二进制计数器1报警使能寄存器
RYRAR/BCNT2AER: 年报警寄存器二进制计数器2报警使能寄存器
RYRARENBCNT3AER：年闹钟启用寄存器二进制计数器3闹钟启用寄存器
RTCCR0: 时间捕捉控制寄存器0
RSCCPnBCNT0CP0：第二个捕捉寄存器nBCNT0捕捉寄存器0
RMINCPn/BCNT1CP0: 分钟捕捉寄存器nBCNT1捕捉寄存器0
RHRCPn/BCNT2CP0: 小时捕捉寄存器nBCNT2捕捉寄存器0
RDAYCPnBCNT3CP0：数据捕捉寄存器nBCNT3捕捉寄存器0
RMONCP0: 月捕获寄存器0

Figure 25.1 实时时钟框图

Table 25.2 RTC I/O pins

引脚名称	I/O	Function
XCIN	Input	将32.768kHz晶振连接到这些引脚
XCOUT	Output	
RTCOUT	Output	该引脚用于输出1-Hz64-Hz波形
RTCIC0	Input	时间捕捉事件输入引脚

25.2 Register Descriptions

Write or read from the RTC registers as described in section 25.6.5, Notes on Writing to and Reading from Registers.

If the value in an RTC register after a reset is given as x (undefined bits) in the list, it is not initialized by a reset. When RTC enters the reset state or a low power state during counting operations, for example while the RCR2.START bit is 1, the year, month, day of the week, date, hours, minutes, seconds, and 64-Hz counters continue to operate.

Note: A reset generated while writing to a register might destroy the register value. In addition, do not allow the MCU to enter Software Standby mode immediately after setting any of these registers. For details, see section 25.6.4, Transitions to Low Power Modes after Setting Registers.

25.2.1 64-Hz Counter (R64CNT)

Address(es): RTC.R64CNT 4004 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
Value after reset:	0	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	F64HZ	64 Hz	Indicates the state between 1 Hz and 64 Hz of the sub-second digit	R
b1	F32HZ	32 Hz		R
b2	F16HZ	16 Hz		R
b3	F8HZ	8 Hz		R
b4	F4HZ	4 Hz		R
b5	F2HZ	2 Hz		R
b6	F1HZ	1 Hz		R
b7	—	Reserved	This bit is read as 0	R

The R64CNT counter is used in both calendar count mode and in binary count mode. The 64-Hz counter (R64CNT) generates the period for a second by counting up periods of the 128-Hz clock. The state in the sub-second range can be confirmed by reading this counter.

This counter is set to 00h by an RTC software reset or an execution of a 30-second adjustment. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.2 Second Counter (RSECCNT)/Binary Counter 0 (BCNT0)

(1) In calendar count mode:

Address(es): RTC.RSECCNT 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Count	Counts from 0 to 9 every second. When a carry is generated, 1 is added to the tens place.	R/W
b6 to b4	SEC10[2:0]	10-Second Count	Counts from 0 to 5 for 60-second counting	R/W

25.2 注册说明

如第25.6.5节"写入和读取寄存器的注意事项"中所述，写入或读取RTC寄存器。

如果复位后RTC寄存器中的值在列表中以x（未定义位）的形式给出，则它不会被复位初始化。当RTC在计数操作期间进入复位状态或低功耗状态时，例如当RCR2.START位为1时，年、月、星期、日期、小时、分钟、秒和64-Hz计数器继续运行操作。

Note: 写入寄存器时产生的复位可能会破坏寄存器值。此外，不要让MCU在设置任何这些寄存器后立即进入软件待机模式。有关详细信息，请参阅第25.6.4节，设置寄存器后转换到低功耗模式。

25.2.1 64-Hz Counter (R64CNT)

Address(es): RTC.R64CNT 4004 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
重置后的值:	0	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	F64HZ	64 Hz	指示亚秒数位1Hz到64Hz之间的状态	R
b1	F32HZ	32 Hz		R
b2	F16HZ	16 Hz		R
b3	F8HZ	8 Hz		R
b4	F4HZ	4 Hz		R
b5	F2HZ	2 Hz		R
b6	F1HZ	1 Hz		R
b7	—	Reserved	该位读为0	R

R64CNT计数器用于日历计数模式和二进制计数模式。64-Hz计数器(R64CNT)通过向上计数128-Hz时钟的周期来生成一秒的周期。亚秒范围内的状态可以通过读取该计数器来确认。

该计数器通过RTC软件复位或执行30秒调整设置为00h。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.2 第二个计数器(RSECCNT)二进制计数器0(BCNT0)

(1) 在日历计数模式下：

Address(es): RTC.RSECCNT 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Count	每秒从0计数到9。产生进位时，十位加1。	R/W
b6 to b4	SEC10[2:0]	10-Second Count	从0到5计数60秒	R/W

Bit	Symbol	Bit name	Description	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RSECCNT counter sets and counts the BCD-coded second value. It counts the carries generated once per second in the 64-Hz counter.

The setting range is decimal 00 to 59. The RTC does not operate normally if any other value is set. Before writing to this register, be sure to stop the count operation using the START bit in RCR2.

To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT0 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0 is a read/write 32-bit binary counter b7 to b0 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.3 Minute Counter (RMINCNT)/Binary Counter 1 (BCNT1)

(1) In calendar count mode:

Address(es): RTC.RMINCNT 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Count	Counts from 0 to 9 every minute. When a carry is generated, 1 is added to the tens place.	R/W
b6 to b4	MIN10[2:0]	10-Minute Count	Counts from 0 to 5 for 60-minute counting	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RMINCNT counter sets and counts the BCD-coded minute value. It counts carries generated once per minute in the second counter.

A value from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

Bit	Symbol	位名称	Description	R/W
b7	—	Reserved	将此位设置为0。它作为设置值读取。	R/W

RSECCNT计数器设置并计算BCD编码的第二个值。它对64-Hz计数器中每秒生成一次的进位进行计数。

设置范围为十进制00到59。如果设置任何其他值，RTC将无法正常工作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。

要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT0 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT0是一个读写32位二进制计数器b7到b0，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.3 分钟计数器(RMINCNT)二进制计数器1(BCNT1)

(1) 在日历计数模式下：

Address(es): RTC.RMINCNT 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Count	每分钟从0数到9。产生进位时，十位加1。	R/W
b6 to b4	MIN10[2:0]	10-Minute Count	60分钟从0数到5	R/W
b7	—	Reserved	将此位设置为0。它作为设置值读取。	R/W

RMINCNT计数器设置并计算BCD编码的分钟值。它对第二个计数器中每分钟产生一次的进位进行计数。

可以指定从00到59的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

(2) In binary count mode:

Address(es): RTC.BCNT1 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1 is a read/write 32-bit binary counter b15 to b8 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.4 Hour Counter (RHRCNT)/Binary Counter 2 (BCNT2)

(1) In calendar count mode:

Address(es): RTC.RHRCNT 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Count	Counts from 0 to 9 once every hour. When a carry is generated, 1 is added to the tens place.	R/W
b5, b4	HR10[1:0]	10-Hour Count	Counts from 0 to 2 once per carry from the ones place.	R/W
b6	PM	PM	Time counter setting: 0: a.m. 1: p.m.	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RHRCNT counter sets and counts the BCD-coded hour value. It counts carries generated once every hour in the minute counter. The specifiable time differs based on the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 – from 00 to 11 (in BCD)
- When the RCR2.HR24 bit is 1 – from 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. The PM bit is only enabled when the RCR2.HR24 bit is 0. Otherwise, the setting in the PM bit has no effect. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT2 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

The BCNT2 counter is a read/write 32-bit binary counter b23 to b16 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START

(2) 在二进制计数模式下：

Address(es): RTC.BCNT1 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1是一个读写32位二进制计数器b15到b8，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.4 小时计数器(RHRCNT)二进制计数器2(BCNT2)

(1) 在日历计数模式下：

Address(es): RTC.RHRCNT 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Count	每小时从0数到9次。产生进位时，十位加1。	R/W
b5, b4	HR10[1:0]	10-Hour Count	每次从个位进行一次从0计数到2。	R/W
b6	PM	PM	计时器设置：0：上午1：下午	R/W
b7	—	Reserved	将此位设置为0。它作为设置值读取。	R/W

RHRCNT计数器设置并计算BCD编码的小时值。它在分钟计数器中计算每小时生成一次的进位。可指定的时间因小时模式位(RCR2.HR24)中的设置而异：

- 当RCR2.HR24位为0时 从00到11（以BCD表示）
- 当RCR2.HR24位为1时 从00到23（以BCD表示）。

如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。仅当RCR2.HR24位为0时才启用PM位。否则，PM位中的设置无效。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT2 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[23:16]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT2计数器是一个读写32位二进制计数器b23到b16，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用START停止计数操作

bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.5 Day-of-Week Counter (RWKCNT)/Binary Counter 3 (BCNT3)

(1) In calendar count mode:

Address(es): RTC.RWKCNT 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Counting	b2 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited.	R/W
b7 to b3	—	Reserved	Set these bits to 0. They are read as the set value.	R/W

The RWKCNT counter sets and counts in the coded day-of-week value. It counts carries generated once per day in the hour counter. A value from 0 through 6 can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode:

Address(es): RTC.BCNT3 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3 is a read/write 32-bit binary counter b31 to b24 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

RCR2中的位。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.5 星期计数器(RWKCNT)二进制计数器3(BCNT3)

(1) 在日历计数模式下：

Address(es): RTC.RWKCNT 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Counting	b2b0000：星期日001： 星期一010：星期二011： 星期三100：星期四101： 星期五110：星期六111： 禁止设置。	R/W
b7 to b3	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W

RWKCNT计数器在编码的星期值中设置和计数。它计算小时计数器中每天生成一次的进位。可以指定从0到6的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT3 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3是一个读写32位二进制计数器b31到b24，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.6 Day Counter (RDAYCNT)

Address(es): RTC.RDAYCNT 4004 400Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Count	Counts from 0 to 9 once per day. When a carry is generated, 1 is added to the tens place	R/W
b5, b4	DATE10[1:0]	10-Day Count	Counts from 0 to 3 once per carry from the ones place	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RDAYCNT counter is used in calendar count mode to set and count the BCD-coded date value. It counts carries generated once per day in the hour counter. The count operation depends on the month and whether the year is a leap year. Leap years are determined according to whether the year counter (RYRCNT) value is divisible by 400, 100, and 4.

A value from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. When specifying a value, the range of specifiable days depends on the month and whether the year is a leap year. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.7 Month Counter (RMONCNT)

Address(es): RTC.RMONCNT 4004 400Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
Value after reset:	0	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1-Month Count	Counts from 0 to 9 once per month. When a carry is generated, 1 is added to the tens place	R/W
b4	MON10	10-Month Count	Counts from 0 to 1 once per carry from the ones place	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RMONCNT counter is used in calendar count mode to set and count the BCD-coded month value. It counts carries generated once per month in the date counter.

A value from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.6 日计数器(RDAYCNT)

Address(es): RTC.RDAYCNT 4004 400Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值:	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Count	每天从0数到9次。产生进位时，十位加1	R/W
b5, b4	DATE10[1:0]	10-Day Count	每次从个位进位从0计数到3	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RDAYCNT计数器用于日历计数模式以设置和计数BCD编码的日期值。它计算小时计数器中每天生成一次的进位。计数操作取决于月份以及年份是否为闰年。闰年根据年份计数器(RYRCNT)值是否可被400、100和4整除来确定。

可以指定从01到31的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。指定值时，可指定天数的范围取决于月份以及年份是否为闰年。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.7 月计数器(RMONCNT)

Address(es): RTC.RMONCNT 4004 400Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
重置后的值:	0	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MON1[3:0]	1-Month Count	每月从0数到9次。产生进位时，十位加1	R/W
b4	MON10	10-Month Count	每次从个位进位从0计数到1	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RMONCNT计数器用于日历计数模式以设置和计数BCD编码的月份值。它计算日期计数器中每月生成一次的进位。

可以指定从01到12的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.8 Year Counter (RYRCNT)

Address(es): RTC.RYRCNT 4004 400Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	YR1[3:0]	1-Year Count	Counts from 0 to 9 once per year. When a carry is generated, 1 is added to the tens place.	R/W
b7 to b4	YR10[3:0]	10-Year Count	Counts from 0 to 9 once per carry from ones place. When a carry is generated in the tens place, 1 is added to the hundreds place.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RYRCNT counter is used in calendar count mode to set and count the BCD-coded year value. It counts carries generated once per year in the month counter.

A value from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time.

25.2.9 Second Alarm Register (RSECAR)/Binary Counter 0 Alarm Register (BCNT0AR)

(1) In calendar count mode:

Address(es): RTC.RSECAR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1 Second	Value for the ones place of seconds	R/W
b6 to b4	SEC10[2:0]	10 Seconds	Value for the tens place of seconds	R/W
b7	ENB	ENB	0: The register value is not compared with the RSECCNT counter value 1: The register value is compared with the RSECCNT counter value.	R/W

RSECAR is an alarm register associated with the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, the RSECAR value is compared with the RSECCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR

25.2.8 年计数器(RYRCNT)

Address(es): RTC.RYRCNT 4004 400Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	YR1[3:0]	1-Year Count	每年从0数到9次。产生进位时，十位加1。	R/W
b7 to b4	YR10[3:0]	10-Year Count	每次从一个地方进行一次从0到9计数。当十位产生进位时，百位加1。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RYRCNT计数器在日历计数模式下用于设置和计数BCD编码的年份值。它计算月份计数器中每年生成一次的进位。

可以指定从00到99（BCD格式）的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第25.3.5节中的程序读取64-Hz计数器和时间。

25.2.9 第二个报警寄存器(RSECAR)二进制计数器0报警寄存器(BCNT0AR)

(1) 在日历计数模式下：

Address(es): RTC.RSECAR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	SEC10[2:0]			SEC1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	SEC1[3:0]	1 Second	秒个位的值	R/W
b6 to b4	SEC10[2:0]	10 Seconds	十位秒的值	R/W
b7	ENB	ENB	0：寄存器值不与RSECCNT计数器值比较1：寄存器值与RSECCNT计数器值比较。	R/W

RSCAR是与BCD编码的第二个计数器RSECCNT相关的警报寄存器。当ENB位设置为1时，RSCAR值与RSECCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR

- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RSECAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT0AR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AR is a read/write alarm register associated with the 32-bit binary counter b7 to b0. This register is set to 00h by an RTC software reset.

25.2.10 Minute Alarm Register (RMINAR)/Binary Counter 1 Alarm Register (BCNT1AR)

(1) In calendar count mode:

Address(es): RTC.RMINAR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1 Minute	Value for the ones place of minutes	R/W
b6 to b4	MIN10[2:0]	10 Minutes	Value for the tens place of minutes	R/W
b7	ENB	ENB	0: The register value is not compared with the RMINCNT counter value 1: The register value is compared with the RMINCNT counter value.	R/W

RMINAR is an alarm register associated with the BCD-coded minute counter RMINCNT. When the ENB bit is set to 1, the RMINAR value is compared with the RMINCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RMINAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59的RSCAR值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT0AR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AR是一个与32位二进制计数器b7到b0相关的读写警报寄存器。该寄存器通过RTC软件复位设置为00h。

25.2.10 分钟报警寄存器(RMINAR)二进制计数器1报警寄存器(BCNT1AR)

(1) 在日历计数模式下：

Address(es): RTC.RMINAR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MIN1[3:0]	1 Minute	分钟个位数的值	R/W
b6 to b4	MIN10[2:0]	10 Minutes	十位分值	R/W
b7	ENB	ENB	0：寄存器值不与RMINCNT计数器值比较1：寄存器值与RMINCNT计数器值比较。	R/W

RMINAR是一个与BCD编码的分钟计数器RMINCNT相关的报警寄存器。当ENB位设置为1时，将RMINAR值与RMINCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RMINAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为00h。

(2) In binary count mode:

Address(es): RTC.BCNT1AR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AR is a read/write alarm register associated with the 32-bit binary counter from b15 to b8. This register is set to 00h by an RTC software reset.

25.2.11 Hour Alarm Register (RHRAR)/Binary Counter 2 Alarm Register (BCNT2AR)

(1) In calendar count mode:

Address(es): RTC.RHRAR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1 Hour	Value for the ones place of hours	R/W
b5, b4	HR10[1:0]	10 Hours	Value for the tens place of hours	R/W
b6	PM	PM	Time alarm setting: 0: a.m. 1: p.m.	R/W
b7	ENB	ENB	0: The register value is not compared with the RHRCNT counter value 1: The register value is compared with the RHRCNT counter value.	R/W

RHRAR is an alarm register associated with the BCD-coded hour counter RHRCNT. When the ENB bit is set to 1, the RHRAR value is compared with the RHRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 – From 00 to 11 (in BCD)
- When the RCR2.HR24 bit is 1 – From 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. When the RCR2.HR24 bit is 0, be sure to set the PM bit. When the RCR2.HR24 bit is 1, the setting in the PM bit has no effect. This register is set to 00h by an

(2) 在二进制计数模式下：

Address(es): RTC.BCNT1AR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AR是一个读写报警寄存器，与从b15到b8的32位二进制计数器相关联。该寄存器通过RTC软件复位设置为00h。

25.2.11 小时报警寄存器(RHRAR)二进制计数器2报警寄存器(BCNT2AR)

(1) 在日历计数模式下：

Address(es): RTC.RHRAR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	HR1[3:0]	1 Hour	几个小时的价值	R/W
b5, b4	HR10[1:0]	10 Hours	数十小时的价值	R/W
b6	PM	PM	时间闹铃设置：0 ：上午1：下午	R/W
b7	ENB	ENB	0：寄存器值不与RHRCNT计数器值比较1：寄存器值与RHRCNT计数器值比较。	R/W

RHRAR是一个与BCD编码的小时计数器RHRCNT相关的警报寄存器。当ENB位设置为1时，RHRAR值与RHRCNT值进行比较。从下面的报警寄存器中，只有那些选择与
设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可指定的时间根据小时模式位(RCR2.HR24)中的设置而有所不同：

- 当RCR2.HR24位为0时 从00到11（以BCD表示）
- 当RCR2.HR24位为1时 从00到23（以BCD表示）。

如果指定的值超出此范围，则RTC将无法正确运行。当RCR2.HR24位为0时，请务必设置PM位。当RCR2.HR24位为1时，PM位中的设置无效。该寄存器由一个设置为00h

RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT2AR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AR is a read/write alarm register associated with the 32-bit binary counter b23 to b16. This register is cleared to 00h by an RTC software reset.

25.2.12 Day-of-Week Alarm Register (RWKAR)/Binary Counter 3 Alarm Register (BCNT3AR)

(1) In calendar count mode:

Address(es): RTC.RWKAR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Setting	b2 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited.	R/W
b6 to b3	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RWKCNT counter value 1: The register value is compared with the RWKCNT counter value.	R/W

RWKAR is an alarm register associated with the coded day-of-week counter RWKCNT. When the ENB bit is set to 1, the RWKAR value is compared with the RWKCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RWKAR values from 0 through 6 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate

RTC软件复位。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT2AR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[23:16]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AR是与32位二进制计数器b23至b16相关的读写警报寄存器。该寄存器通过RTC软件复位清零。

25.2.12 星期报警寄存器(RWKAR)二进制计数器3报警寄存器(BCNT3AR)

(1) 在日历计数模式下：

Address(es): RTC.RWKAR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Setting	b2b0000：星期日001： 星期一010：星期二011： 星期三100：星期四101： 星期五110：星期六111： 禁止设置。	R/W
b6 to b3	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RWKCNT计数器值比较1：寄存器值与RWKCNT计数器值比较。	R/W

RWKAR是与编码的星期计数器RWKCNT相关的警报寄存器。当ENB位设置为1时，RWKAR值与RWKCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从0到6（以BCD表示）的RWKAR值。如果指定了超出此范围的值，则RTC不工作

correctly. This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT3AR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AR is a read/write alarm register associated with the 32-bit binary counter b31 to b24. This register is set to 00h by an RTC software reset.

25.2.13 Date Alarm Register (RDAYAR)/Binary Counter 0 Alarm Enable Register (BCNT0AER)

(1) In calendar count mode:

Address(es): RTC.RDAYAR 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1 Day	Value for the ones place of days	R/W
b5, b4	DATE10[1:0]	10 Days	Value for the tens place of days	R/W
b6	—	Reserved	Set this bit to 0. It is read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RDAYCNT counter value 1: The register value is compared with the RDAYCNT counter value.	R/W

RDAYAR is an alarm register associated with the BCD-coded date counter RDAYCNT. When the ENB bit is set to 1, the RDAYAR value is compared with the RDAYCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the corresponding counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RDAYAR values from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

正确。该寄存器通过RTC软件复位设置为00h。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT3AR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AR是与32位二进制计数器b31至b24相关的读写警报寄存器。该寄存器通过RTC软件复位设置为00h。

25.2.13 日期报警寄存器(RDAYAR)二进制计数器0报警使能寄存器(BCNT0AER)

(1) 在日历计数模式下：

Address(es): RTC.RDAYAR 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	DATE1[3:0]	1 Day	几天的地方的价值	R/W
b5, b4	DATE10[1:0]	10 Days	十位天的价值	R/W
b6	—	Reserved	将此位设置为0。它作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RDAYCNT计数器值比较1：寄存器值与RDAYCNT计数器值比较。	R/W

RDAYAR是一个与BCD编码日期计数器RDAYCNT相关的报警寄存器。当ENB位设置为1时，将RDAYAR值与RDAYCNT值进行比较。从下面的报警寄存器中，只有那些选择与
设置为1的ENB位与相应的计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到31（以BCD表示）的RDAYAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为00h。

(2) In binary count mode:

Address(es): RTC.BCNT0AER 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AER is a read/write register to set the alarm enable associated with the 32-bit binary counter b7 to b0. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 00h by an RTC software reset.

25.2.14 Month Alarm Register (RMONAR)/Binary Counter 1 Alarm Enable Register (BCNT1AER)

(1) In calendar count mode:

Address(es): RTC.RMONAR 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1 Month	Value for the ones place of months	R/W
b4	MON10	10 Months	Value for the tens place of months	R/W
b6, b5	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RMONCNT counter value 1: The register value is compared with the RMONCNT counter value.	R/W

RMONAR is an alarm register associated with the BCD-coded month counter RMONCNT. When the ENB bit is set to 1, the RMONAR value is compared with the RMONCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RMONAR values from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 00h by an RTC software reset.

(2) 在二进制计数模式下：

Address(es): RTC.BCNT0AER 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AER是一个读写寄存器，用于设置与32位二进制计数器b7相关的警报使能至b0。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关联的值变为1。该寄存器通过RTC软件复位设置为00h。

25.2.14 月份闹钟寄存器(RMONAR)二进制计数器1闹钟启用寄存器(BCNT1AER)

(1) 在日历计数模式下：

Address(es): RTC.RMONAR 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	MON10	MON1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MON1[3:0]	1 Month	月份个位数的值	R/W
b4	MON10	10 Months	十位月份的值	R/W
b6, b5	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RMONCNT计数器值比较1：寄存器值与RMONCNT计数器值比较。	R/W

RMONAR是一个与BCD编码月份计数器RMONCNT相关的报警寄存器。当ENB位设置为1时，RMONAR值与RMONCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到12（以BCD表示）的RMONAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为00h。

(2) In binary count mode:

Address(es): RTC.BCNT1AER 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AER is a read/write register for setting the alarm enable associated with the 32-bit binary counter b15 to b8. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 00h by an RTC software reset.

25.2.15 Year Alarm Register (RYRAR)/Binary Counter 2 Alarm Enable Register (BCNT2AER)

(1) In calendar count mode:

Address(es): RTC.RYRAR 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	YR1[3:0]	1 Year	Value for the ones place of years	R/W
b7 to b4	YR10[3:0]	10 Years	Value for the tens place of years	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RYRAR is an alarm register associated with the BCD-coded year counter RYRCNT. The RYRAR values from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0000h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT2AER 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ENB[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AER is a read/write register to set the alarm enable associated with the 32-bit binary counter b23 to b16. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 0000h by an RTC software reset.

(2) 在二进制计数模式下：

Address(es): RTC.BCNT1AER 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AER是一个读写寄存器，用于设置与32位二进制计数器b15到b8相关的警报使能。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关联的值变为1。该寄存器通过RTC软件复位设置为00h。

25.2.15 年报警寄存器(RYRAR)二进制计数器2报警使能寄存器(BCNT2AER)

(1) 在日历计数模式下：

Address(es): RTC.RYRAR 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	YR1[3:0]	1 Year	年个地方的价值	R/W
b7 to b4	YR10[3:0]	10 Years	数十年的价值	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RYRAR是一个与BCD编码年份计数器RYRCNT相关联的警报寄存器。可以指定从00到99（BCD格式）的RYRAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0000h。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT2AER 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ENB[23:16]							
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AER是一个读写寄存器，用于设置与32位二进制计数器b23到b16相关联的警报使能。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断关联的值变为1。该寄存器通过RTC软件复位设置为0000h。

25.2.16 Year Alarm Enable Register (RYRAREN)/Binary Counter 3 Alarm Enable Register (BCNT3AER)

(1) In calendar count mode:

Address(es): RTC.RYRAREN 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RYRCNT counter value 1: The register value is compared with the RYRCNT counter value.	R/W

When the ENB bit in RYRAREN is set to 1, the RYRAR value is compared with the RYRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1.This register is set to 00h by an RTC software reset.

(2) In binary count mode:

Address(es): RTC.BCNT3AER 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AER is a read/write register to set the alarm enable associated with the 32-bit binary counter b31 to b24. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]), and when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is set to 00h by an RTC software reset.

25.2.16 年报警使能寄存器(RYRAREN)二进制计数器3报警使能 Register (BCNT3AER)

(1) 在日历计数模式下：

Address(es): RTC.RYRAREN 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RYRCNT计数器值比较1：寄存器值与RYRCNT计数器值比较。	R/W

当RYRAREN中的ENB位设置为1时，RYRAR值与RYRCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值匹配时，与RTC_ALM中断相关的IR标志设置为1。该寄存器通过RTC软件复位设置为00h。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT3AER 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AER是一个读写寄存器，用于设置与32位二进制计数器b31至b24相关的警报使能。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关联的值变为1。该寄存器通过RTC软件复位设置为00h。

25.2.17 RTC Control Register 1 (RCR1)

Address(es): RTC.RCR1 4004 4022h

	b7	b6	b5	b4	b3	b2	b1	b0
	PES[3:0]				RTCOS	PIE	CIE	AIE
Value after reset:	x	x	x	x	0	x	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	AIE	Alarm Interrupt Enable	0: An alarm interrupt request is disabled 1: An alarm interrupt request is enabled.	R/W
b1	CIE	Carry Interrupt Enable	0: A carry interrupt request is disabled 1: A carry interrupt request is enabled.	R/W
b2	PIE	Periodic Interrupt Enable	0: A periodic interrupt request is disabled 1: A periodic interrupt request is enabled.	R/W
b3	RTCOS	RTCOUT Output Select	0: RTCOUT outputs 1 Hz 1: RTCOUT outputs 64 Hz.	R/W
b7 to b4	PES[3:0]	Periodic Interrupt Select	b7 b4 0 1 1 0: A periodic interrupt is generated every 1/256 second*1 0 1 1 1: A periodic interrupt is generated every 1/128 second 1 0 0 0: A periodic interrupt is generated every 1/64 second 1 0 0 1: A periodic interrupt is generated every 1/32 second 1 0 1 0: A periodic interrupt is generated every 1/16 second 1 0 1 1: A periodic interrupt is generated every 1/8 second 1 1 0 0: A periodic interrupt is generated every 1/4 second 1 1 0 1: A periodic interrupt is generated every 1/2 second 1 1 1 0: A periodic interrupt is generated every 1 second 1 1 1 1: A periodic interrupt is generated every 2 seconds. Other settings: No periodic interrupts are generated.	R/W

Note 1. When LOCO is selected (RCR4.RCKSEL = 1) while PES[3:0] = 0110b, a periodic interrupt is generated every 1/128 second.

The RCR1 register is used in both calendar count mode and in binary count mode. Bits AIE, PIE, and PES[3:0] are updated synchronously with the count source. When the RCR1 register is modified, check that all the bits are updated before proceeding.

AIE bit (Alarm Interrupt Enable)

The AIE bit enables or disables alarm interrupt requests.

CIE bit (Carry Interrupt Enable)

The CIE bit enables or disables interrupt requests when a carry to the RSECCNT/BCNT0 register occurs, or when a carry to the 64-Hz counter (R64CNT) occurs while reading the 64-Hz counter.

PIE bit (Periodic Interrupt Enable)

The PIE bit enables or disables a periodic interrupt.

RTCOS bit (RTCOUT Output Select)

The RTCOS bit selects the RTCOUT output period. The RTCOS bit must be rewritten while the count operation is stopped (the RCR2.START bit is 0) and the RTCOUT output is disabled (the RCR2.RTCOE bit is 0). When the RTCOUT is output to an external pin, the RCR2.RTCOE bit must be enabled. For details on controlling the I/O ports, see section 20.5.1, Procedure for Specifying the Pin Functions.

PES[3:0] bits (Periodic Interrupt Select)

The PES[3:0] bits specify the period for the periodic interrupt. A periodic interrupt is generated with the period specified by these bits.

25.2.17 RTC控制寄存器1(RCR1)

Address(es): RTC.RCR1 4004 4022h

	b7	b6	b5	b4	b3	b2	b1	b0
	PES[3:0]				RTCOS	PIE	CIE	AIE
重置后的值:	x	x	x	x	0	x	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	AIE	报警中断使能	0：禁止报警中断请求1：允许报警中断请求。	R/W
b1	CIE	进位中断使能	0：禁止进位中断请求1：使能进位中断请求。	R/W
b2	PIE	周期性中断使能	0：禁用周期性中断请求1：启用周期性中断请求。	R/W
b3	RTCOS	RTCOUT输出选择	0: RTCOUT outputs 1 Hz 1: RTCOUT outputs 64 Hz.	R/W
b7 to b4	PES[3:0]	周期性中断选择	b7b40110：每1256秒产生一个周期性中断*10111：每1128秒产生一个周期性中断1000：每164秒产生一个周期性中断1001:每132秒产生一个周期性中断1010:每116秒产生一个周期性中断1011:每18秒产生一个周期性中断1100:每1产生一个周期性中断4秒1101：每1秒产生一个周期中断1110：每1秒产生一个周期中断1111：每2秒产生一个周期中断。其他设置：不产生周期性中断。	R/W

Note 1. WhenLOCOisselected(RCR4.RCKSEL=1)whilePES[3:0]=0110b aperiodicinterruptisgeneratedevery1128second.

RCR1寄存器用于日历计数模式和二进制计数模式。AIE、PIE和PES[3:0]位与计数源同步更新。修改RCR1寄存器时，在继续之前检查所有位是否都已更新。

AIE位（报警中断使能）

AIE位启用或禁用警报中断请求。

CIE位（进位中断使能）

当发生对RSECCNTBCNT0寄存器的进位，或在读取64-Hz计数器时发生对64-Hz计数器(R64CNT)的进位时，CIE位启用或禁用中断请求。

PIE位（周期性中断使能）

PIE位启用或禁用周期性中断。

RTCOS位（RTCOUT输出选择）

RTCOS位选择RTCOUT输出周期。当计数操作停止（RCR2.START位为0）且RTCOUT输出禁用（RCR2.RTCOE位为0）时，必须重写RTCOS位。当RTCOUT输出到外部引脚时，必须使能RCR2.RTCOE位。有关控制IO端口的详细信息，请参见第20.5.1节，指定引脚功能的过程。

PES[3:0]位（周期性中断选择）

PES[3:0]位指定周期性中断的周期。以这些位指定的周期生成周期性中断。

25.2.18 RTC Control Register 2 (RCR2)

(1) In calendar count mode:

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	START	Start	0: Prescaler and time counter are stopped 1: Prescaler and time counter operate normally.	R/W
b1	RESET	RTC Software Reset	• In writing: 0: Invalid (writing 0 has no effect) 1: The prescaler and the target registers for RTC software reset *1 are initialized. • In reading: 0: Normal time operation in progress, or an RTC software reset has completed 1: RTC software reset in progress.	R/W
b2	ADJ30	30-Second Adjustment	• In writing: 0: Invalid (writing 0 has no effect) 1: 30-second adjustment is executed. • In reading: 0: Normal time operation in progress, or 30-second adjustment has completed 1: 30-second adjustment in progress.	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable*3	0: Automatic adjustment is disabled 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*3	0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds.	R/W
b6	HR24	Hours Mode	0: RTC operates in 12-hour mode 1: RTC operates in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select	0: Calendar count mode 1: Binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCR0, RSECCP0/BCNT0CP0, RMINCP0/BCNT1CP0, RHRCP0/BCNT2CP0, RDAYCP0/BCNT3CP0, RMONCP0, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.
Note 3.

The RCR2 register is related to hours mode, automatic adjustment function, enabling RTCOUT output, 30-second adjustment, RTC software reset, and controlling count operation.

START bit (Start)

The START bit stops or restarts the prescaler or time counter operation. This bit is updated in synchronization with the next cycle of the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software.

When 1 is written to the RESET bit, initialization starts in synchronization with the count source. When the initialization is completed, the RESET bit is automatically set to 0. Check that this bit is set to 0 before proceeding.

25.2.18 RTC控制寄存器2(RCR2)

(1) 在日历计数模式下：

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	ADJ	RTCOE	ADJ30	复位	开始
重置后的值：	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	START	Start	0：预分频器和时间计数器停止1：预分频器和时间计数器正常运行。	R/W
b1	RESET	RTC软件复位	写入：0：无效（写入0无效）1：预分频器和RTC软件复位的目标寄存器*1被初始化。 读取中：0：正常时间操作正在进行，或RTC软件复位已完成1：RTC软件复位正在进行。	R/W
b2	ADJ30	30-Second Adjustment	写入中：0：无效（写入0无效）1：执行30秒调整。 读数中：0：正在进行正常时间操作，或30秒调整已完成1：正在进行30秒调整。	R/W
b3	RTCOE	RTCOUT输出使能	0：RTCOUT输出禁用1：RTCOUT输出启用。	R/W
b4	AADJE	自动调整启用*3	0：禁用自动调整1：启用自动调整。	R/W
b5	AADJP	自动调整期 Select*3	0：RADJ.ADJ[5:0]设置值每分钟根据预分频器的计数值调整1：RADJ.ADJ[5:0]设置值每10秒根据预分频器的计数值调整一次。	R/W
b6	HR24	小时模式	0：RTC以12小时模式运行1：RTC以24小时模式运行。	R/W
b7	CNTMD	计数模式选择	0：日历计数模式1：二进制计数模式。	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCR0, RSECCP0/BCNT0CP0, RMINCP0/BCNT1CP0, RHRCP0/BCNT2CP0, RDAYCP0/BCNT3CP0, RMONCP0, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. 选择Loco时，该位的设置将被禁用。
Note 3.

RCR2寄存器与小时模式、自动调整功能、启用RTCOUT输出、30秒调整、RTC软件复位和控制计数操作有关。

开始位（开始）

START位停止或重新启动预分频器或时间计数器操作。该位与计数源的下一个周期同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。

向RESET位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。在继续之前检查该位是否设置为0。

ADJ30 bit (30-Second Adjustment)

The ADJ30 bit is for 30-second adjustment.

When 1 is written to the ADJ30 bit, the RSECCNT value of 30 seconds or less is rounded down to 00 second and the value of 30 seconds or more is rounded up to 1 minute.

The 30-second adjustment is performed in synchronization with the count source. When 1 is written to this bit, the ADJ30 bit is automatically set to 0 after the 30-second adjustment completes. If 1 is written to the ADJ30 bit, check that the bit is set to 0 before proceeding. When the 30-second adjustment is performed, the prescaler and R64CNT are also reset. The ADJ30 bit is cleared to 0 by an RTC software reset.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time.

When RTCOUT is to be output from an external pin, enable the RTCOE bit and set up the port control for the pin.

AADJE bit (Automatic Adjustment Enable*3)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit.

The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select*3)

The AADJP bit selects the automatic-adjustment period.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit.

The AADJP bit is set to 0 by an RTC software reset.

HR24 bit (Hours Mode)

The HR24 bit specifies whether the RTC operates in 12- or 24-hour mode.

Use the START bit to stop counting before changing the value of the HR24 bit. Do not stop counting (write 0 to the START bit) and change the value of the HR24 bit at the same time.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is complete.

For details on initial settings, see section 25.3.1, Outline of Initial Settings of Registers after Power On.

ADJ30位（30秒调整）

ADJ30位用于30秒调整。

向ADJ30位写入1时，30秒以下的RSECCNT值向下舍入为00秒，30秒以上的值向上舍入为1分钟。

30秒调整与计数源同步进行。当1写入该位时，
30秒调整完成后，ADJ30位自动设置为0。如果将1写入ADJ30位，请在继续之前检查该位是否设置为0。当执行30秒调整时，预分频器和R64CNT也被复位。RTC软件复位将ADJ30位清零。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入
START位）并同时更改RTCOE位的值。

当RTCOUT要从外部引脚输出时，使能RTCOE位并设置引脚的端口控制。

ADJE位（自动调整使能*3）

AADJE位控制（启用或禁用）自动调整。

在更改
AADJE bit.

RTC软件复位将ADJE位设置为0。

AADJP位（自动调整周期选择*3）

AADJP位选择自动调整周期。

在更改
AADJP bit.

AADJP位通过RTC软件复位设置为0。

HR24位（小时模式）

HR24位指定RTC是在12小时还是24小时模式下运行。

在更改HR24位的值之前，使用START位停止计数。不要停止计数（将0写入
START位）并同时更改HR24位的值。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式还是二进制计数模式下运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新，其值在RTC软件复位完成前固定。

有关初始设置的详细信息，请参阅第25.3.1节"通电后寄存器初始设置概要"。

(2) In binary count mode:

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	START	Start	0: The 32-bit binary counter, 64-Hz counter, and prescaler are stopped 1: The 32-bit binary counter, 64-Hz counter, and prescaler are in normal operation.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Invalid (writing 0 has no effect) 1: The prescaler and the target registers for RTC software reset*1 are initialized. • In reading 0: Normal time operation in progress, or an RTC software reset has completed 1: RTC software reset in progress.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output is disabled 1: RTCOUT output is enabled.	R/W
b4	AADJE	Automatic Adjustment Enable*3	0: Automatic adjustment is disabled 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*3	0: Add or subtract the RADJ.ADJ[5:0] bits from the prescaler count value every 32 seconds 1: Add or subtract the RADJ.ADJ[5:0] bits from the prescaler count value every 8 seconds	R/W
b6	—	Reserved	This bit is undefined. The write value should be 0.	R/W
b7	CNTMD	Count Mode Select	0: Calendar count mode 1: Binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCR0, RSECCP0/BCNT0CP0, RMINCP0/BCNT1CP0, RHRCP0/BCNT2CP0, RDAYCP0/BCNT3CP0, RMONCP0, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP

Note 2. When LOCO is selected, the setting of this bit is disabled.

START bit (Start)

The START bit stops or restarts the prescaler or counter (clock) operation. This bit is updated in synchronization with the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software.

When 1 is written to the RESET bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. When 1 is written to the RESET bit, check that the bit is set to 0 before proceeding.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time. When an RTCOUT signal is to be output from an external pin, enable the port control in addition to setting this bit.

(2) 在二进制计数模式下：

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	复位开始	
重置后的值：	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	START	Start	0：32位二进制计数器、64-Hz计数器和预分频器停止1：32位二进制计数器、64-Hz计数器和预分频器正常运行。	R/W
b1	RESET	RTC软件复位	写入0：无效（写入0无效）1：预分频器和RTC软件复位的目标寄存器*1被初始化。 读取中0：正常时间操作正在进行，或RTC软件复位已完成1：RTC软件复位正在进行。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	RTCOE	RTCOUT输出使能	0：禁用RTCOUT输出1：启用RTCOUT输出。	R/W
b4	AADJE	自动调整启用	*3 0：禁用自动调整1：启用自动调整。	R/W
b5	AADJP	自动调整期Select*3	0：每32秒从预分频器计数值中加或减RADJ.ADJ[5:0]位1：每8秒从预分频器计数值中加或减RADJ.ADJ[5:0]位	R/W
b6	—	Reserved	该位未定义。写入值应为0。	R/W
b7	CNTMD	计数模式选择	0：日历计数模式1：二进制计数模式。	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCR0, RSECCP0/BCNT0CP0, RMINCP0/BCNT1CP0, RHRCP0/BCNT2CP0, RDAYCP0/BCNT3CP0, RMONCP0, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP

Note 2. 选择Loco时，该位的设置将被禁用。

开始位（开始）

START位停止或重新启动预分频器或计数器（时钟）操作。该位与计数源同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。

向RESET位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。当向RESET位写入1时，在继续之前检查该位是否设置为0。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。当要从外部引脚输出RTCOUT信号时，除了设置该位外，还启用端口控制。

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit. The AADJE bit is cleared to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Correction period can be selected from 32 second units or 8 second units in binary count mode.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit. The AADJP bit is cleared to 0 by an RTC software reset.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is complete.

For details on initial settings, see section 25.3.1, Outline of Initial Settings of Registers after Power On.

25.2.19 RTC Control Register 4 (RCR4)

Address(es): RTC.RCR4 4004 4028h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RCKSEL
Value after reset:	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RCKSEL	Count Source Select	0: Sub-clock oscillator is selected 1: LOCO is selected.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RCR4 register selects the count source and is used in both calendar count mode and in binary count mode.

When the RCKSEL bit is set to 0, the time is counted with the sub-clock oscillator. When the bit is set to 1, the time is counted with LOCO.

RCKSEL bit (Count Source Select)

The RCKSEL bit selects the count source from the sub-clock oscillator and LOCO.

The count source must be selected only once before specifying the initial settings of the RTC registers at power-on.

ADJE位（自动调整使能）

AADJE位控制（启用或禁用）自动调整。

在更改
ADJE位。通过RTC软件复位将ADJE位清零。

AADJP位（自动调整周期选择）

AADJP位选择自动调整周期。

在二进制计数模式下，校正周期可以从32秒单位或8秒单位中选择。

在更改
AADJP位。AADJP位通过RTC软件复位清零。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式还是二进制计数模式下运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新，其值在RTC软件复位完成前固定。

有关初始设置的详细信息，请参阅第25.3.1节"通电后寄存器初始设置概要"。

25.2.19 RTC控制寄存器4(RCR4)

Address(es): RTC.RCR4 4004 4028h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RCKSEL
重置后的值：	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RCKSEL	计数源选择	0：选择副时钟振荡器1：选择LOCO。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RCR4寄存器选择计数源，用于日历计数模式和二进制计数模式。

当RCKSEL位设置为0时，时间由副时钟振荡器计数。当该位设置为1时，时间以LOCO计数。

RCKSEL位（计数源选择）

RCKSEL位从副时钟振荡器和LOCO中选择计数源。

在上电时指定RTC寄存器的初始设置之前，必须只选择一次计数源。

25.2.20 Frequency Register (RFRH/RFRL)

Address(es): RTC.RFRH 4004 402Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RFC16	Reserved	Write 0 before writing to the RFRL register after a cold start.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): RTC.RFRL 4004 402Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFC[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	RFC[15:0]	Frequency Comparison Value	Write 00FFh to this register when using the LOCO	R/W

RFRL is a register for controlling the prescaler when LOCO is selected.

The RTC time counter operates on a 128-Hz clock signal as the base clock. Therefore, when LOCO is selected, LOCO is divided by the prescaler to generate a 128-Hz clock signal. Set the frequency comparison value in the RFC[15:0] bits to generate a 128-Hz clock from the LOCO frequency. Before writing to RFC[15:0] after a cold start, write 0000h to the RFRH.

A value from 0007h through 01FFh can be specified as the frequency comparison value. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2. The operating frequency of the peripheral module clock and the LOCO should be such that the peripheral module clock is ≥ to the LOCO.

Calculation method of frequency comparison value:

RFC[15:0] = (LOCO clock frequency) / 128 - 1

When the LOCO frequency is 32.768 kHz, the RFRL register must be set to 00FFh.

25.2.20 频率寄存器(RFRHRFRL)

Address(es): RTC.RFRH 4004 402Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RFC16	Reserved	在冷启动后写入RFRL寄存器之前写入0。	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): RTC.RFRL 4004 402Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFC[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b15 to b0	RFC[15:0]	频率比较 Value	使用LOCO时将00FFh写入该寄存器	R/W

RFRL是一个寄存器，用于在选择LOCO时控制预分频器。

RTC时间计数器以128-Hz时钟信号作为基本时钟运行。Therefore whenLOCOisselected LOCOisdividedbythepr escalertogeneratea128-Hzclocksignal设置RFC[15:0]位中的频率比较值以从LOCO频率生成128-Hz时钟。在冷启动后写入RFC[15:0]之前，将0000h写入RFRH。

可以将0007h到01FFh的值指定为频率比较值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必通过设置RCR2中的START位来停止计数操作。外围模块时钟和LOCO的工作频率应使外围模块时钟与LOCO相差　　。

频率比较值的计算方法：

RFC[15:0] = (LOCO clock frequency) / 128 - 1

当LOCO频率为32.768kHz时，RFRL寄存器必须设置为00FFh。

25.2.21 Time Error Adjustment Register (RADJ)

Address(es): RTC.RADJ 4004 402Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	PMADJ[1:0]		ADJ[5:0]					
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b5 to b0	ADJ[5:0]	Adjustment Value	These bits specify the adjustment value from the prescaler	R/W
b7, b6	PMADJ[1:0]	Plus–Minus	b7 b6 0 0: Adjustment is not performed 0 1: Adjustment is performed by the addition to the prescaler 1 0: Adjustment is performed by the subtraction from the prescaler 1 1: Setting prohibited.	R/W

Adjustment is performed by the addition to or subtraction from the prescaler. If the automatic adjustment enable (RCR2.AADJE) bit is 0, adjustment is performed when writing to the RADJ. If the RCR2.AADJE bit is 1, adjustment is performed in the interval specified by the automatic adjustment period select (RCR2.AADJP) bit.

The current adjustment by software (disabling automatic adjustment) might be invalid if the following adjustment value is specified within 320 cycles of the count source after the register setting. To perform adjustment consecutively, wait for 320 cycles or more of the count source after the register setting, then specify the next adjustment value.

RADJ is updated in synchronization with the count source. When RADJ is modified, check that all the bits are updated before continuing with additional processing. This register is cleared to 00h by an RTC software reset. The setting of this register is enabled only when the sub-clock oscillator is selected. When LOCO is selected, adjustment is not performed.

ADJ[5:0] bits (Adjustment Value)

The ADJ[5:0] bits specify the adjustment value (the number of sub-clock cycles) from the prescaler.

PMADJ[1:0] bits (Plus–Minus)

The PMADJ[1:0] bits select whether the clock is set ahead or back depending on the error-adjustment value set in the ADJ[5:0] bits.

25.2.22 Time Capture Control Register 0 (RTCCR0)

Address(es): RTC.RTCCR0 4004 4040h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCEN	—	TCNF[1:0]		—	TCST	TCCT[1:0]	
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	TCCT[1:0]	Time Capture Control	b1 b0 0 0: No event is detected 0 1: Rising edge is detected 1 0: Falling edge is detected 1 1: Both edges are detected.	R/W
b2	TCST	Time Capture Status	0: No event is detected 1: An event is detected.*1	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

25.2.21 时间误差调整寄存器(RADJ)

Address(es): RTC.RADJ 4004 402Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	PMADJ[1:0]		ADJ[5:0]					
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b5 to b0	ADJ[5:0]	调整值	这些位指定来自预分频器的调整值	R/W
b7, b6	PMADJ[1:0]	Plus–Minus	b7b600：不进行调整01：通过预分频器1的加法进行调整0：通过预分频器1的减法进行调整1：禁止设置。	R/W

通过对预分频器进行加法或减法进行调整。如果自动调整使能(RCR2.AADJE)位为0，则在写入RADJ时执行调整。如果RCR2.AADJE位为1，则在自动调整周期选择(RCR2.AADJP)位指定的间隔内执行调整。

如果在寄存器设置后的计数源的320个周期内指定了以下调整值，则通过软件进行的当前调整（禁用自动调整）可能无效。要连续执行调整，请在寄存器设置后等待计数源的320个或更多周期，然后指定下一个调整值。

RADJ与计数源同步更新。当RADJ被修改时，在继续其他处理之前检查所有位是否都已更新。该寄存器通过RTC软件复位清零。该寄存器的设置仅在选择了副时钟振荡器时启用。选择LOCO时，不进行调整。

ADJ[5:0]位（调整值）

ADJ[5:0]位指定来自预分频器的调整值（子时钟周期数）。

PMADJ[1:0] bits (Plus–Minus)

PMADJ[1:0]位根据在
ADJ[5:0] bits.

25.2.22 时间捕捉控制寄存器0(RTCCR0)

Address(es): RTC.RTCCR0 4004 4040h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCEN	—	TCNF[1:0]		—	TCST	TCCT[1:0]	
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	TCCT[1:0]	时间捕捉控制	b1b000：未检测到事件01：检测到上升沿10：检测到下降沿11：检测到两个沿。	R/W
b2	TCST	时间捕捉状态	0：未检测到事件1：检测到事件。*1	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	TCNF[1:0]	Time Capture Noise Filter Control	b5 b4 0 0: Noise filter is off 0 1: Setting prohibited 1 0: Noise filter is on (count source) 1 1: Noise filter is on (count source by divided by 32).	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	TCEN	Time Capture Event Input Pin Enable	0: The RTCIC0 pin is disabled as the time capture event input 1: The RTCIC0 pin is enabled as the time capture event input.	R/W

Note 1. Indicates that an event is detected. Writing 1 to this bit has no effect. Writing 0 sets this bit to 0.

The RTCCR0 register is used both in calendar count mode and in binary count mode. RTCCR0 controls the RTCIC0 pin, respectively.

RTCCR0 is updated in synchronization with the count source. When RTCCR0 is modified, check that all the bits except for the TCST bit are updated before continuing with more processing. This register is cleared to 00h by an RTC software reset. When RTCIC0 is used as the time capture pin, VBTICTLR.VCH0IEN must be set to 1. For more information, see section 12, Battery Backup Function.

TCCT[1:0] bits (Time Capture Control)

The TCCT[1:0] bits control the edge detection of the time capture event input pin, RTCIC0. The detection edge is selectable. The TCCT[1:0] bits must be set while the VBTICTLR.VCH0IEN bit is 1.

TCST bit (Time Capture Status)

The TCST bit indicates that an event of the time capture event input pin, RTCIC0 was detected. When the TCST bit is 0, no event is detected. When the TCST bit is 1, this bit indicates that an event was detected on the associated pin and the capture register is valid. When multiple events are detected, the capture time for the first event is retained.

If an event is detected while the count operation is stopped (the RCR2.START bit is 0), the captured value is not guaranteed. In this case, set the TCST bit to 0 to delete the captured value. Writing 0 sets the TCST bit to 0. Writing any other value except 0 has no effect.

Set the TCST bit while the TCCT[1:0] bits are 00b (no event is detected). The TCST bit is set to 0 in synchronization with the count source. When the TCST bit is set to 0, check that the bit is updated before continuing with additional processing.

TCNF[1:0] bits (Time Capture Noise Filter Control)

The TCNF[1:0] bits control the noise filter of the time capture event input pin (RTCIC0).

When the noise filter is on, the count source divided by 1 or divided by 32 is selectable. In this case, when the input level on the time capture event input pin matches three consecutive times at the set sampling period, the input level is determined.

Set the TCNF[1:0] bits while the TCCT[1:0] bits are 00b (no event is detected). When the noise filter is used, set the TCNF[1:0] bits, wait for 3 cycles of the specified sampling period, then set the TCCT[1:0] bits. Set the TCNF[1:0] bits when the VBTICTLR.VCH0IEN bit is 1.

TCEN bit (Time Capture Event Input Pin Enable)

The TCEN bit enables or disables the time capture event input pin (RTCIC0). When the functions of the time capture event input pin (RTCIC0) are multiplexed, set VBTICTLR first. If the TCEN bit is set to 0, also set the TCCT[1:0] bits to 00b.

Bit	Symbol	位名称	Description	R/W
b5, b4	TCNF[1:0]	时间捕捉噪声过滤器控制	b5b400：噪声过滤器关闭01：设置禁止10：噪声过滤器打开（计数源）11：噪声过滤器打开（计数源除以32）。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	TCEN	时间捕捉事件输入引脚使能	0：禁止RTCIC0引脚作为时间捕捉事件输入1：使能RTCIC0引脚作为时间捕捉事件输入。	R/W

Note 1. 表示检测到事件。向该位写入1无效。写入0将该位设置为0。

RTCCR0寄存器用于日历计数模式和二进制计数模式。RTCCR0分别控制RTCIC0引脚。

RTCCR0与计数源同步更新。修改RTCCR0时，请检查除TCST位之外的所有位是否都已更新，然后再继续进行更多处理。该寄存器通过RTC软件复位清零。当RTCIC0用作时间捕捉引脚时，VBTICTLR.VCH0IEN必须设置为1。有关详细信息，请参阅第12节，电池备份功能。

TCCT[1:0]位（时间捕捉控制）

TCCT[1:0]位控制时间捕捉事件输入引脚RTCIC0的边沿检测。检测边缘是可选的。当VBTICTLR.VCH0IEN位为1时，必须设置TCCT[1:0]位。

TCST位（时间捕捉状态）

TCST位指示检测到时间捕捉事件输入引脚RTCIC0的事件。当TCST位为0时，未检测到任何事件。当TCST位为1时，该位表示在相关引脚上检测到事件并且捕捉寄存器有效。当检测到多个事件时，将保留第一个事件的捕获时间。

如果在计数操作停止时检测到事件（RCR2.START位为0），则不能保证捕获的值。在这种情况下，将TCST位设置为0以删除捕获的值。写入0会将TCST位设置为0。写入除0以外的任何其他值均无效。

当TCCT[1:0]位为00b（未检测到事件）时，设置TCST位。TCST位与计数源同步设置为0。当TCST位设置为0时，在继续进行其他处理之前检查该位是否已更新。

TCNF[1:0]位（时间捕捉噪声滤波器控制）

TCNF[1:0]位控制时间捕捉事件输入引脚(RTCIC0)的噪声滤波器。

当噪声滤波器打开时，计数源除以1或除以32是可选的。在这种情况下，当时间捕捉事件输入引脚上的输入电平在设置的采样周期内连续匹配3次时，确定输入电平。

当TCCT[1:0]位为00b（未检测到事件）时，设置TCNF[1:0]位。使用噪声滤波器时，设置TCNF[1:0]位，等待指定采样周期的3个周期，然后设置TCCT[1:0]位。当VBTICTLR.VCH0IEN位为1时，设置TCNF[1:0]位。

TCEN位（时间捕捉事件输入引脚使能）

TCEN位启用或禁用时间捕捉事件输入引脚(RTCIC0)。当时间捕捉事件输入引脚（RTCIC0）的功能被复用时，首先设置VBTICTLR。如果TCEN位设置为0，也将TCCT[1:0]位设置为00b。

25.2.23 Second Capture Register 0 (RSECCP0) /BCNT0 Capture Register 0 (BCNT0CP0)

(1) In calendar count mode:

Address(es): RTC.RSECCP0 4004 4052h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Capture	Capture value for the ones place of seconds	R
b6 to b4	SEC10[2:0]	10-Second Capture	Capture value for the tens place of seconds	R
b7	—	Reserved	This bit is read as 0 after an RTC software reset	R

RSECCP0 is a read-only register that captures the RSECCNT value when a time capture event is detected.

The event detection time detected by the RTCIC0 pin is stored in the RSECCP0 register. This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

(2) In binary count mode:

Address(es): RTC.BCNT0CP0 4004 4052h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0CPy is a read-only register that captures the BCNT0 value when a time capture event is detected. The event detection times detected by the RTCIC0 pin is stored in the BCNT0CP0 register, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

25.2.24 Minute Capture Register 0 (RMINCP0)/BCNT1 Capture Register 0 (BCNT1CP0)

(1) In calendar count mode:

Address(es): RTC.RMINCP0 4004 4054h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Capture	Capture value for the ones place of minutes	R
b6 to b4	MIN10[2:0]	10-Minute Capture	Capture value for the tens place of minutes	R

25.2.23 第二个捕捉寄存器0(RSCCP0)BCNT0捕捉寄存器0(BCNT0CP0)

(1) 在日历计数模式下：

Address(es): RTC.RSECCP0 4004 4052h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Capture	捕获秒个位的值	R
b6 to b4	SEC10[2:0]	10-Second Capture	十位秒的捕获值	R
b7	—	Reserved	在RTC软件复位后，该位被读取为0	R

RSCCP0是一个只读寄存器，当检测到时间捕捉事件时，它会捕捉RSECCNT值。

RTCIC0引脚检测到的事件检测时间存储在RSCCP0寄存器中。该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT0CP0 4004 4052h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT0CPy是一个只读寄存器，当检测到时间捕捉事件时，它会捕捉BCNT0的值。RTCIC0引脚检测到的事件检测时间分别存储在BCNT0CP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

25.2.24 分钟捕捉寄存器0(RMINCP0)BCNT1捕捉寄存器0(BCNT1CP0)

(1) 在日历计数模式下：

Address(es): RTC.RMINCP0 4004 4054h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Capture	捕获分钟个位的值	R
b6 to b4	MIN10[2:0]	10-Minute Capture	十位分钟的捕获值	R

Bit	Symbol	Bit name	Description	R/W
b7	—	Reserved	This bit is read as 0 after an RTC software reset	R

RMINCP0 is a read-only register that captures the RMINCNT value when a time capture event is detected.

The event detection time detected by the RTCIC0 pin is stored in the RMINCP0 register.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

(2) In binary count mode:

Address(es): RTC.BCNT1CP0 4004 4054h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1CP0 is a read-only register that captures the BCNT1 value when a time capture event is detected.

The event detection times detected by the RTCIC0 pin is stored in the BCNT1CP0 register, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

25.2.25 Hour Capture Register 0 (RHRCP0) /BCNT2 Capture Register 0 (BCNT2CP0)

(1) In calendar count mode:

Address(es): RTC.RHRCP0 4004 4056h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Capture	Capture value for the ones place of hours	R
b5, b4	HR10[1:0]	10-Hour Capture	Capture value for the tens place of hours	R
b6	PM	PM	0: AM. 1: PM.	R
b7	—	Reserved	This bit is read as 0 after an RTC software reset	R

RHRCP0 is a read-only register that captures the RHRCNT value when a time capture event is detected.

The event detection time detected by the RTCIC0 pin is stored in the RHRCP0 register. The PM bit is only enabled when the RCR2.HR24 bit is 0 (in 12-hour mode).

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

Bit	Symbol	位名称	Description	R/W
b7	—	Reserved	在RTC软件复位后，该位被读取为0	R

RMINCP0是一个只读寄存器，在检测到时间捕捉事件时捕捉RMINCNT值。

RTCIC0引脚检测到的事件检测时间存储在RMINCP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT1CP0 4004 4054h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1CP0是一个只读寄存器，当检测到时间捕捉事件时，它会捕捉BCNT1的值。

RTCIC0引脚检测到的事件检测时间分别存储在BCNT1CP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

25.2.25 小时捕捉寄存器0(RHRCP0)BCNT2捕捉寄存器0(BCNT2CP0)

(1) 在日历计数模式下：

Address(es): RTC.RHRCP0 4004 4056h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Capture	为几个小时的地方捕获价值	R
b5, b4	HR10[1:0]	10-Hour Capture	捕捉数十小时的价值	R
b6	PM	PM	0: AM. 1: PM.	R
b7	—	Reserved	在RTC软件复位后，该位被读取为0	R

RHRCP0是一个只读寄存器，它在检测到时间捕捉事件时捕捉RHRCNT值。

RTCIC0引脚检测到的事件检测时间存储在RHRCP0寄存器中。PM位仅在RCR2.HR24位为0时启用（在12小时模式下）。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

(2) In binary count mode:

Address(es): RTC.BCNT2CP0 4004 4056h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT2CP0 is a read-only register that captures the BCNT2 value when a time capture event is detected.

The event detection time detected by the RTCIC0 pin is stored in the BCNT2CP0 register.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

25.2.26 Date Capture Register 0 (RDAYCP0) /BCNT3 Capture Register 0 (BCNT3CP0)

(1) In calendar count mode:

Address(es): RTC.RDAYCP0 4004 405Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Capture	Capture value for the ones place of days	R
b5, b4	DATE10[1:0]	10-Day Capture	Capture value for the tens place of days	R
b7, b6	—	Reserved	These bits are read as 0 after an RTC software reset	R

RDAYCP0 is a read-only register that captures the RDAYCNT value when a time capture event is detected.

The event detection time detected by the RTCIC0 pin is stored in the RDAYCP0 register.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

(2) In binary count mode:

Address(es): RTC.BCNT3CP0 4004 405Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3CP0 is a read-only register that captures the BCNT3 value when a time capture event is detected.

The event detection time detected by the RTCTC0 pin is stored in the BCNT3CP0 register.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

(2) 在二进制计数模式下：

Address(es): RTC.BCNT2CP0 4004 4056h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[23:16]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT2CP0是一个只读寄存器，它在检测到时间捕捉事件时捕捉BCNT2值。

RTCIC0引脚检测到的事件检测时间存储在BCNT2CP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

25.2.26 数据捕捉寄存器0(RDAYCP0)BCNT3捕捉寄存器0(BCNT3CP0)

(1) 在日历计数模式下：

Address(es): RTC.RDAYCP0 4004 405Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Capture	捕获天数的价值	R
b5, b4	DATE10[1:0]	10-Day Capture	十天的捕获值	R
b7, b6	—	Reserved	这些位在RTC软件复位后被读取为0	R

RDAYCP0是一个只读寄存器，它在检测到时间捕捉事件时捕捉RDAYCNT值。

RTCIC0引脚检测到的事件检测时间存储在RDAYCP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

(2) 在二进制计数模式下：

Address(es): RTC.BCNT3CP0 4004 405Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCP0[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3CP0是一个只读寄存器，它在检测到时间捕捉事件时捕捉BCNT3值。

RTCTC0引脚检测到的事件检测时间存储在BCNT3CP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

25.2.27 Month Capture Register 0 (RMONCP0)

(1) In calendar count mode:

Address(es): RTC.RMONCP0 4004 405Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1-Month Capture	Capture value for the ones place of months	R
b4	MON10	10-Month Capture	Capture value for the tens place of months	R
b7 to b5	—	Reserved	These bits are read as 0	R

RMONCP0 is a read-only register that captures the RMONCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0 pin is stored in the RMONCP0 register, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCR0.TCCT[1:0] bits.

25.3 Operation

25.3.1 Outline of Initial Settings of Registers after Power On

After the power is turned on, perform the initial settings for the clock setting, count mode setting, time error adjustment, time setting, alarm, interrupt, and time capture control register.

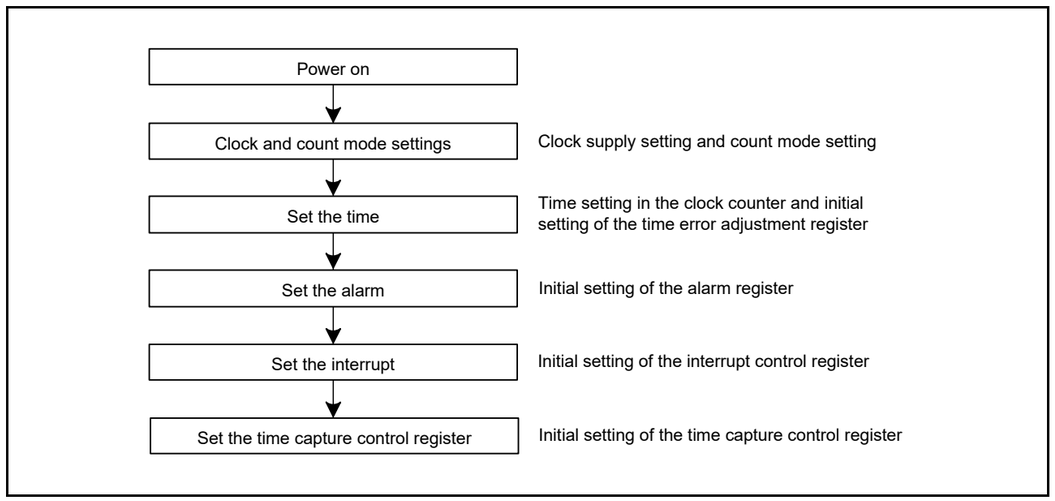


Figure 25.2 Outline of initial settings after a power on

25.3.2 Clock and Count Mode Setting Procedure

Figure 25.3 shows how to set the clock and the count mode.

25.2.27 月份捕捉寄存器0(RMONCP0)

(1) 在日历计数模式下：

Address(es): RTC.RMONCP0 4004 405Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MON1[3:0]	1-Month Capture	捕获月份的某个地方的价值	R
b4	MON10	10-Month Capture	捕获十个月的价值	R
b7 to b5	—	Reserved	这些位被读为0	R

RMONCP0是一个只读寄存器，它在检测到时间捕捉事件时捕捉RMONCNT值。

RTCIC0引脚检测到的事件检测时间分别存储在RMONCP0寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCR0.TCCT[1:0]位停止时间捕捉事件检测。

25.3 Operation

25.3.1 上电后寄存器的初始设置概要

上电后，对时钟设置、计数模式设置、时间误差调整、时间设置、闹钟、中断、时间捕捉控制寄存器进行初始设置。

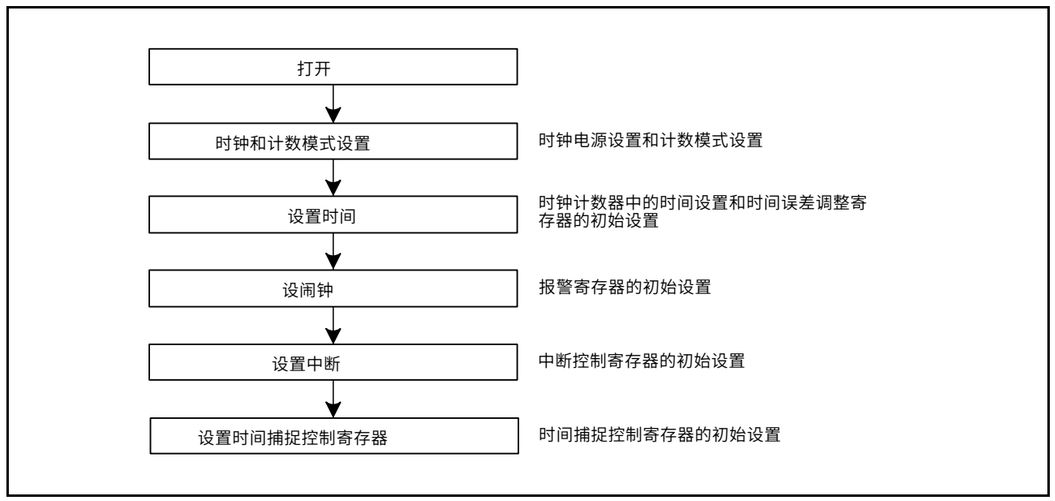
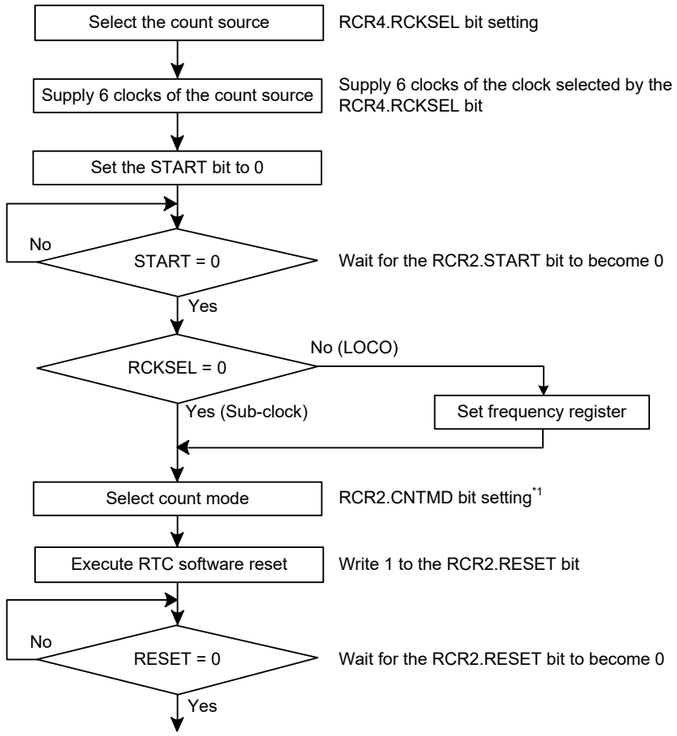


Figure 25.2 通电后的初始设定概要

25.3.2 时钟和计数模式设置程序

图25.3显示了如何设置时钟和计数模式。

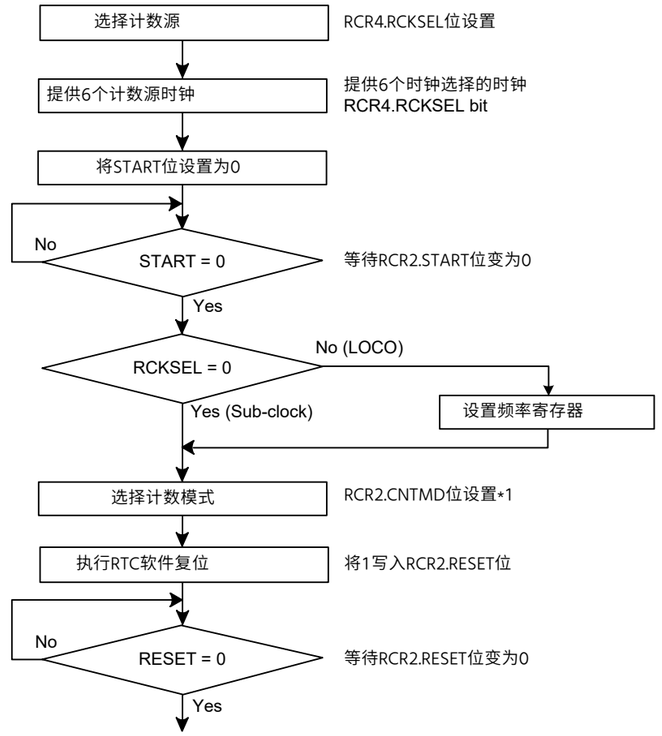


Note 1. This step is not required if the count mode is set concurrently by setting the START bit to 0. A value associated with the count mode setting must be written to the RCR2.CNTMD bit.

Figure 25.3 Clock and count mode setting procedure

25.3.3 Setting the Time

Figure 25.4 shows how to set the time.

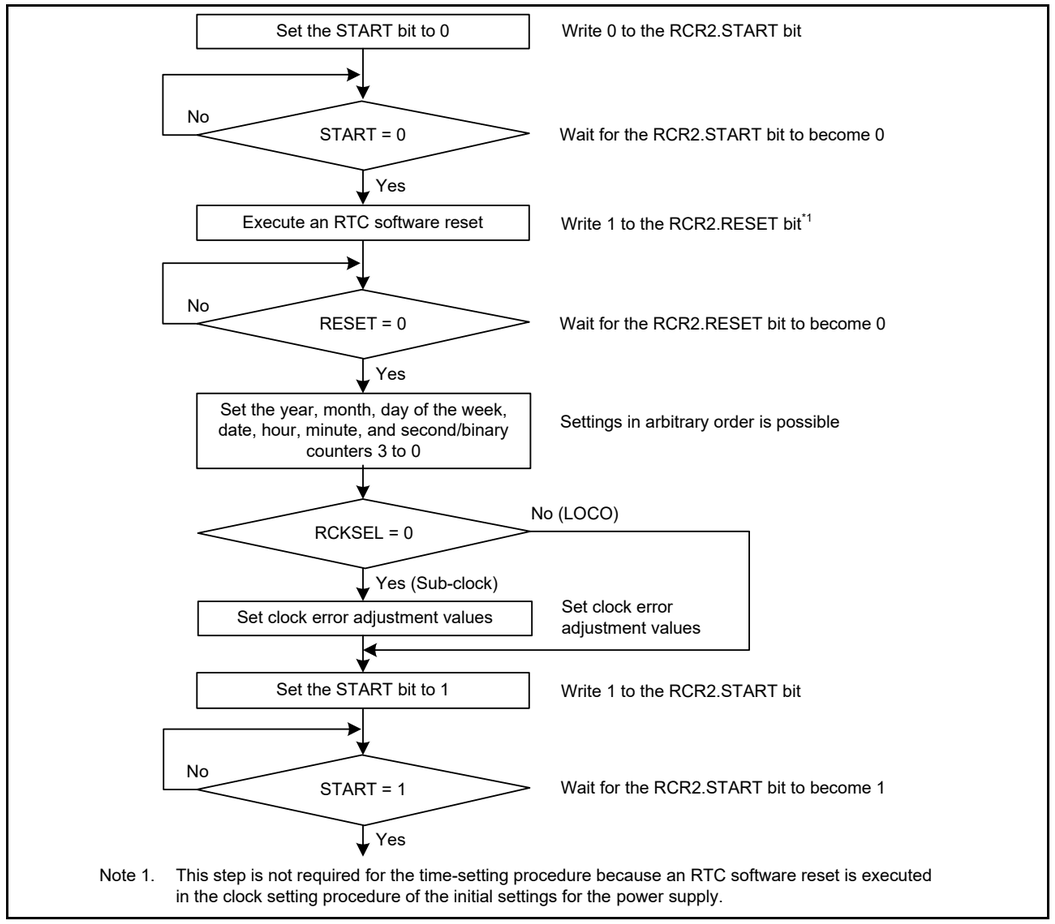


Note 1. 如果通过将START位设置为0同时设置计数模式，则不需要此步骤。
与计数模式设置相关的值必须写入RCR2.CNTMD位。

Figure 25.3 时钟和计数模式设置程序

25.3.3 设置时间

图25.4显示了如何设置时间。



Note 1. This step is not required for the time-setting procedure because an RTC software reset is executed in the clock setting procedure of the initial settings for the power supply.

Figure 25.4 Setting the time

25.3.4 30-Second Adjustment

Figure 25.5 shows how to execute a 30-second adjustment.

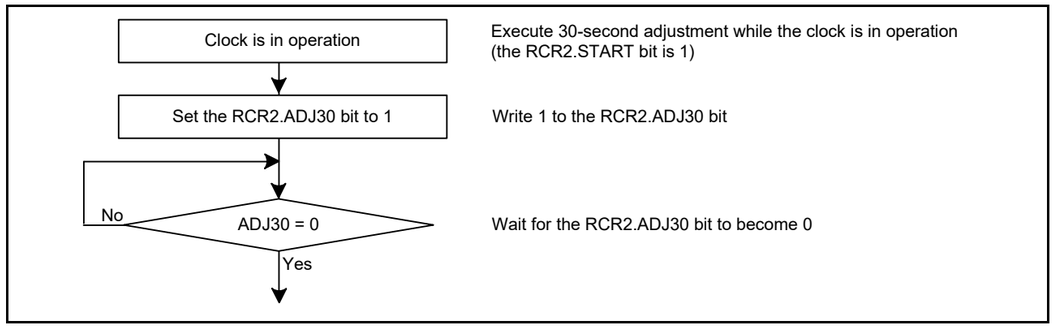
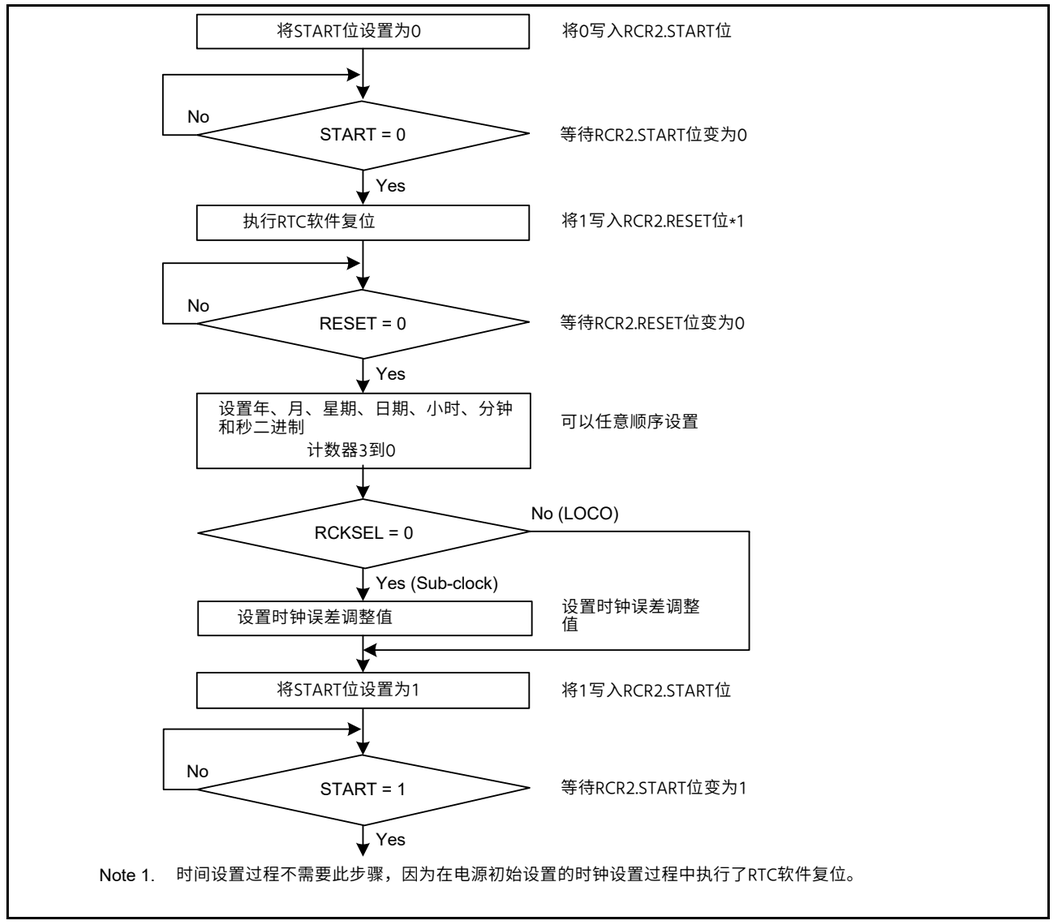


Figure 25.5 30-second adjustment



Note 1. 时间设置过程不需要此步骤，因为在电源初始设置的时钟设置过程中执行了RTC软件复位。

Figure 25.4 设定时间

25.3.4 30-Second Adjustment

图25.5显示了如何执行30秒的调整。

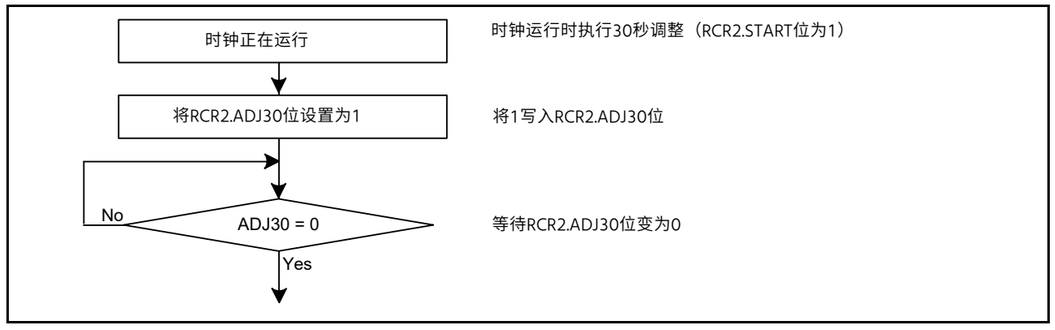
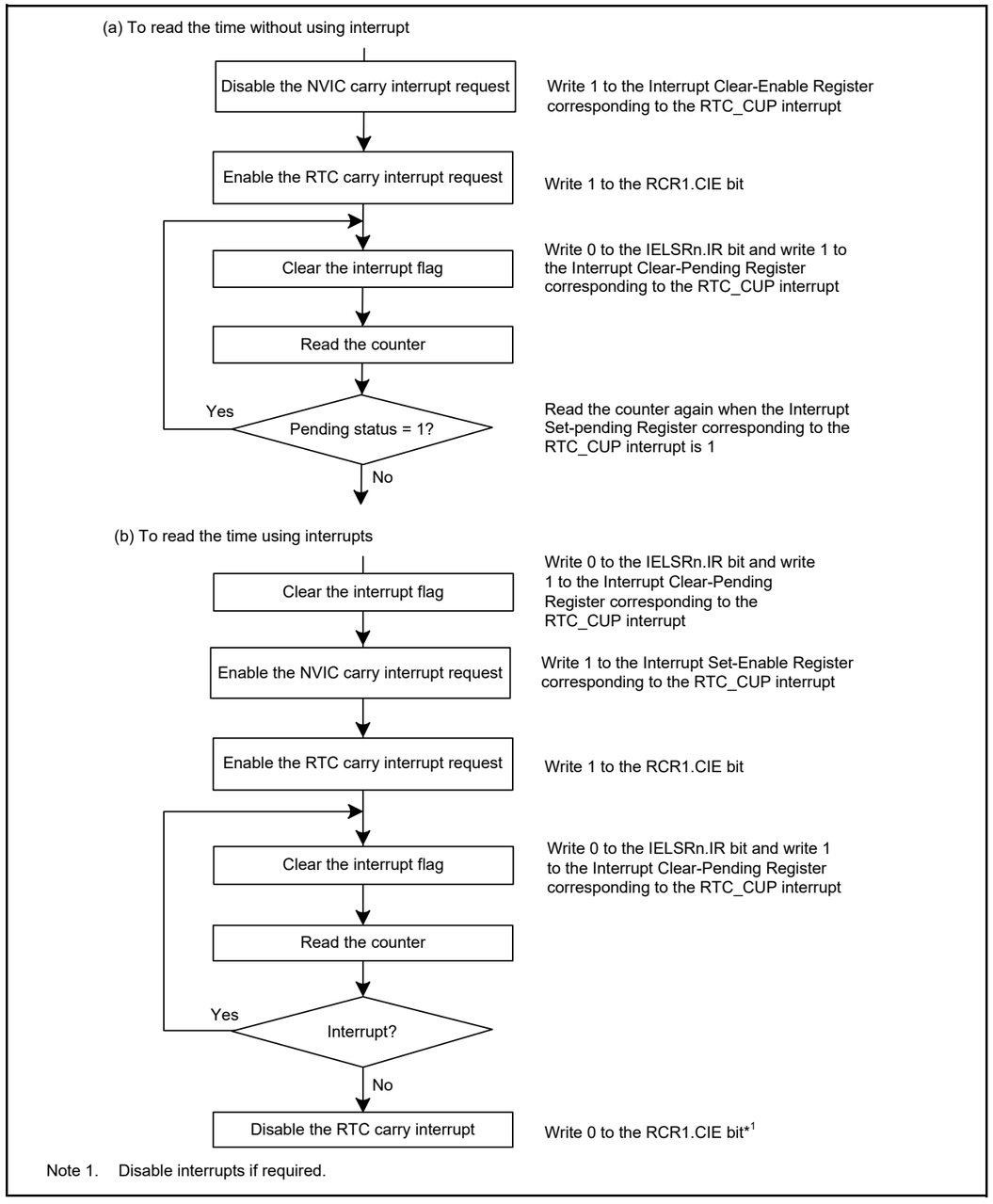


Figure 25.5 30-second adjustment

25.3.5 Reading 64-Hz Counter and Time

Figure 25.6 shows how to read a 64-Hz counter and time.



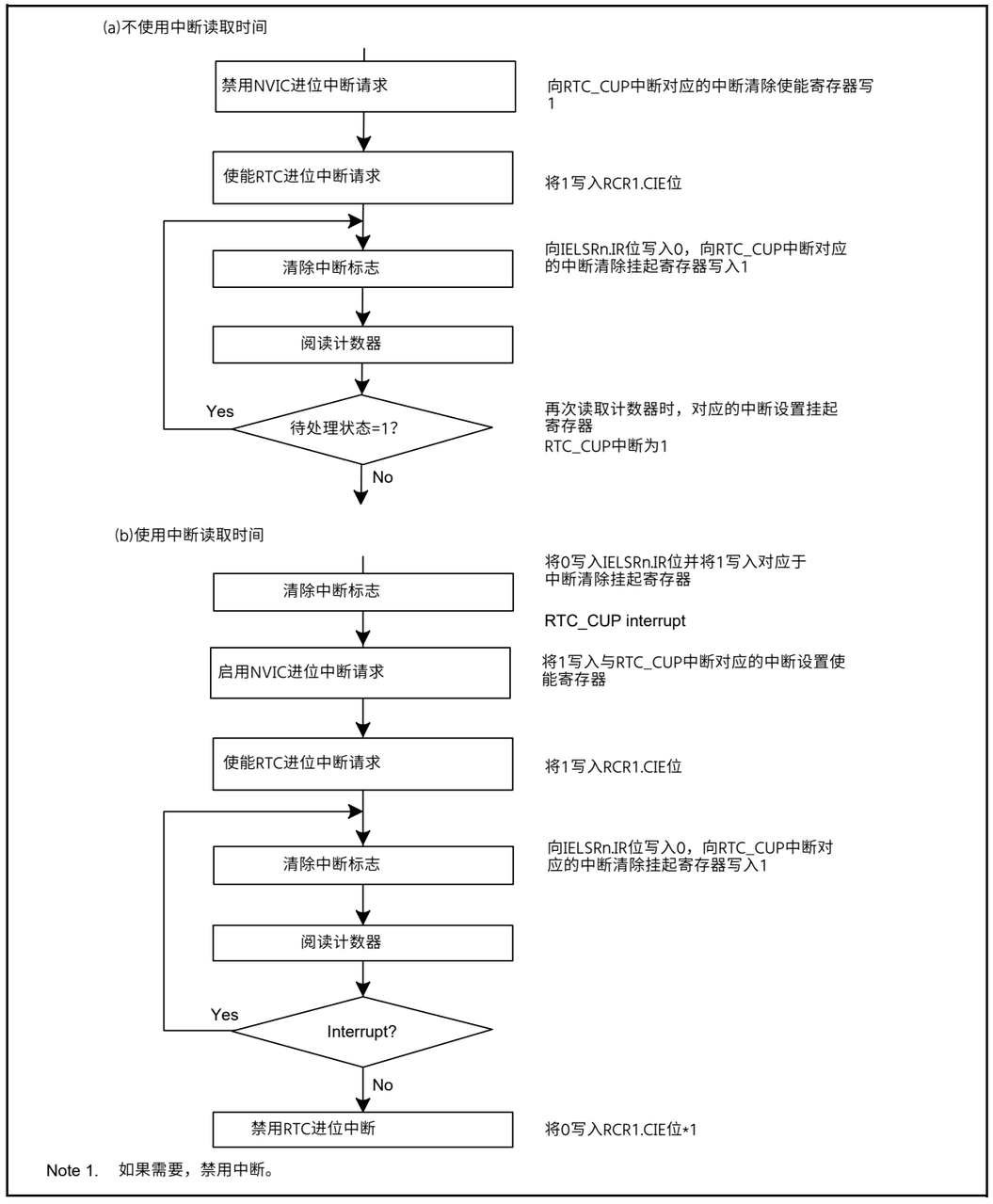
Note 1. Disable interrupts if required.

Figure 25.6 Reading time

If a carry occurs while the 64-Hz counter and time are read, the correct time is not obtained, therefore they must be read again. The procedure for reading the time without using interrupts is shown in (a) in Figure 25.6, and the procedure using carry interrupts is shown in (b). To keep the program simple, method (a) should be used in most cases.

25.3.5 读取64-Hz计数器和时间

图25.6显示了如何读取64-Hz计数器和时间。



Note 1. 如果需要，禁用中断。

Figure 25.6 阅读时间

如果在读取64-Hz计数器和时间时发生进位，则无法获得正确的时间，因此必须再次读取它们。不使用中断读取时间的过程如图25.6(a)所示，使用进位中断的过程如图25.6所示。为保持程序简单，在大多数情况下应使用方法(a)。

25.3.6 Alarm Function

Figure 25.7 shows how to use the alarm function.

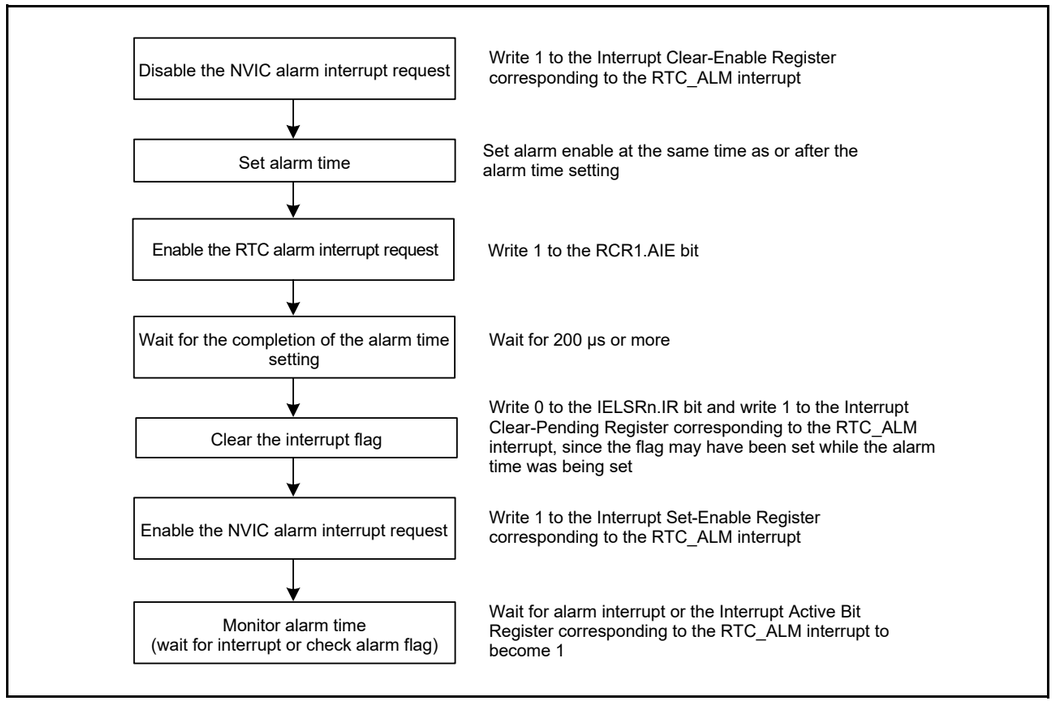


Figure 25.7 Using alarm function

In calendar count mode, an alarm can be generated by any one of year, month, date, day-of-week, hour, minute or second, or any combination of those. Write 1 to the ENB bit in the alarm registers involved in the alarm setting, and set the alarm time in the lower bits. Write 0 to the ENB bit in registers not involved in the alarm setting.

In binary count mode, an alarm can be generated in any bit combination of 32 bits. Write 1 to the ENB bit of the alarm enable register associated with the target bit of the alarm, and set the alarm time in the alarm register. For bits that are not the target of the alarm, write 0 to the ENB bit of the Alarm Enable register.

When the counter and the alarm time match, the IELSRn.IR bit and Interrupt Set-Pending/Clear-Pending Register associated with the RTC_ALM interrupt are set to 1. Alarm detection can be confirmed by reading the Interrupt Set-Pending Register associated with the RTC_ALM interrupt, but an interrupt should be used in most cases. If 1 is set in the Interrupt Set-Enable Register associated with the RTC_ALM interrupt, an alarm interrupt is generated in the event of the alarm, enabling the alarm to be detected.

Writing 0 sets the IELSRn.IR bit associated with the RTC_ALM interrupt to 0. If interrupt is enabled, the Interrupt Set-Pending/Clear-Pending Register and Interrupt Active Bit Register associated with the RTC_ALM interrupt is cleared automatically after exiting the interrupt handler. Otherwise, write 1 to the Interrupt Clear-Pending Register associated with the RTC_ALM interrupt to clear it.

When the counter and the alarm time match in a low power state, the MCU returns from the low power state.

25.3.7 Procedure for Disabling Alarm Interrupt

Figure 25.8 shows the procedure for disabling the enabled alarm interrupt request.

25.3.6 报警功能

图25.7显示了如何使用报警功能。

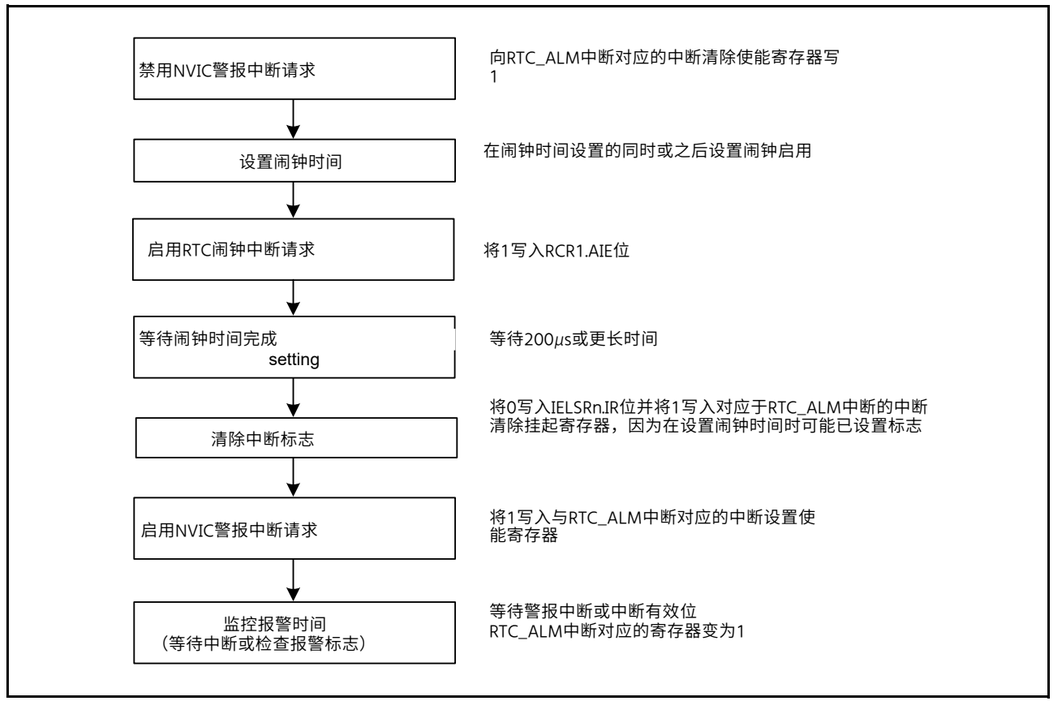


Figure 25.7 使用报警功能

在日历计数模式下，可以通过年、月、日、星期、小时、分钟或秒中的任何一个或它们的任意组合来生成警报。将1写入涉及闹钟设置的闹钟寄存器的ENB位，并在低位设置闹钟时间。将0写入与报警设置无关的寄存器中的ENB位。

在二进制计数模式下，可以以32位的任意位组合产生报警。将1写入与闹钟目标位相关的闹钟使能寄存器的ENB位，并在闹钟寄存器中设置闹钟时间。对于不是警报目标的位，将0写入警报启用寄存器的ENB位。

当计数器和闹钟时间匹配时，与RTC_ALM中断相关的IELSRn.IR位和中断设置挂起清除挂起寄存器设置为1。可以通过读取与RTC_ALM中断相关的中断设置挂起寄存器来确认警报检测，但在大多数情况下应该使用中断。如果在与RTC_ALM中断相关的中断设置使能寄存器中设置为1，则在发生警报时会产生警报中断，从而能够检测到警报。

写入0将与RTC_ALM中断相关的IELSRn.IR位设置为0。如果启用中断，则中断设置
与RTC_ALM中断相关的PendingClear-Pending寄存器和中断有效位寄存器在退出中断处理程序后自动清除。否则，将1写入与RTC_ALM中断相关的中断清除挂起寄存器以将其清除。

当计数器和闹钟时间在低功耗状态下匹配时，MCU从低功耗状态返回。

25.3.7 禁用警报中断的步骤

图25.8显示了禁用启用的警报中断请求的过程。

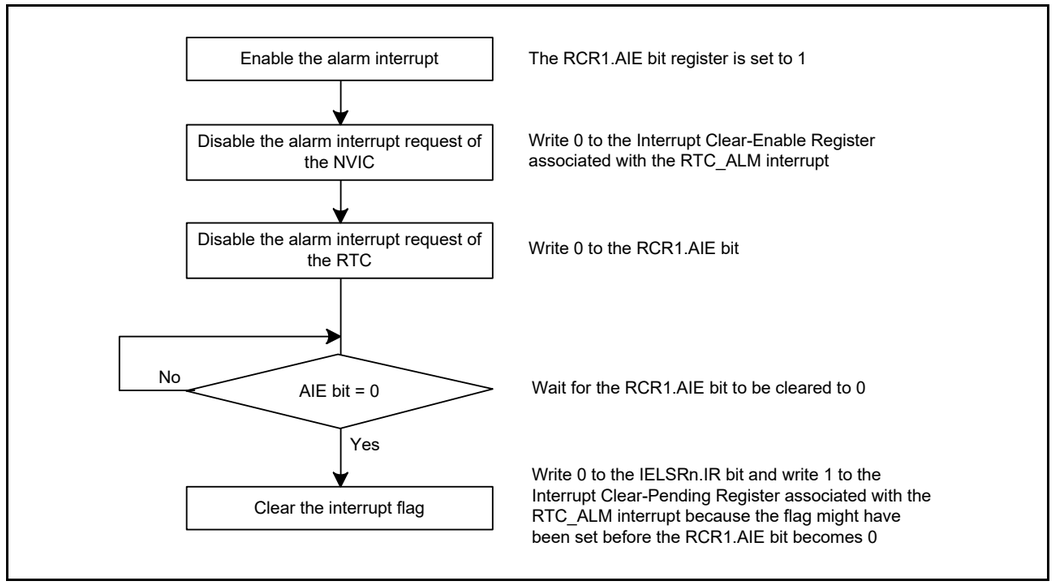


Figure 25.8 Procedure for disabling alarm interrupt request

25.3.8 Time Error Adjustment Function

The time error adjustment function is used to correct errors, running fast or slow, in the time due to variation in the precision of oscillation by the sub-clock oscillator. Because 32,768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low.

The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software.

Use the RCR2.AADJP bit to select automatic adjustment or adjustment by software.

25.3.8.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1. Automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJP bit elapses.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

Register settings (when RCR2.CNTMD = 0):

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 60 (3Ch).

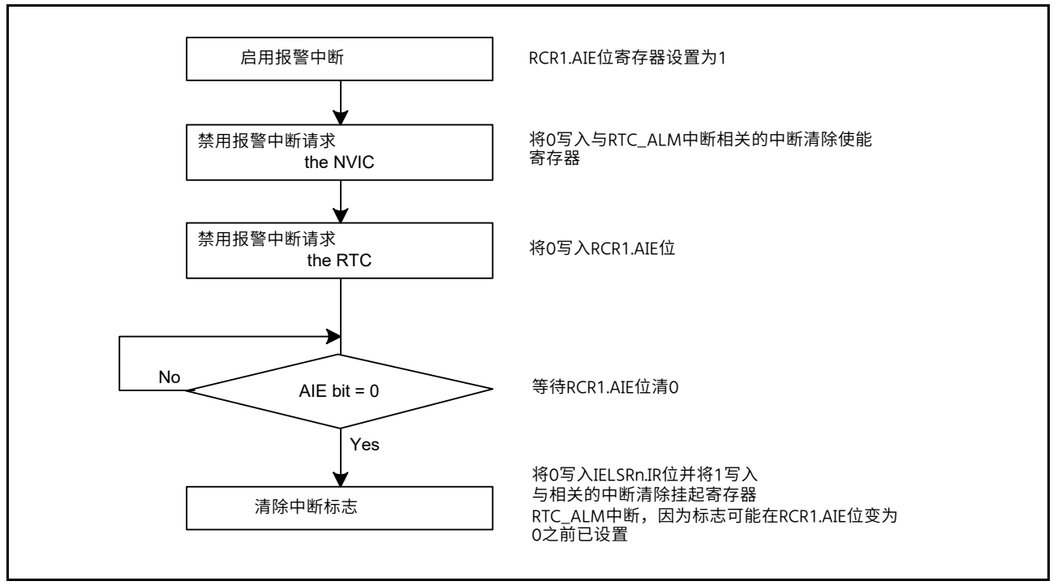


Figure 25.8 禁用报警中断请求的步骤

25.3.8 时间误差调整功能

时间误差调整功能用于校正由于子时钟振荡器的振荡精度变化而导致的时间误差，运行速度快或慢。由于在选择子时钟振荡器时，子时钟振荡器的32 768个周期构成1秒的运行时间，因此如果子时钟频率高，则时钟运行快，如果子时钟频率低，则时钟运行慢。

时间误差调整功能包括：

- 自动调整
- 通过软件调整。

使用RCR2.AADJP位选择自动调整或软件调整。

25.3.8.1 自动调整

通过将RCR2.AADJE位设置为1来启用自动调整。自动调整是每次经过RCR2.AADJP位选择的调整周期时，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) 示例1：运行在32.769kHz的子时钟振荡器

(a) 调整程序

当副时钟振荡器以32.769kHz运行时，每32 769个时钟周期经过1秒。RTC旨在以32 768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每分钟快60个时钟周期，因此调整可以采取将时钟每分钟调回60个周期的形式。

寄存器设置（当RCR2.CNTMD=0时）：

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 60 (3Ch).

(2) Example 2: Sub-clock oscillator running at 32.766 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.766 kHz, 1 second elapses every 32,766 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs slow by 2 clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings: (when RCR2.CNTMD = 0):

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler.)
- RADJ.ADJ[5:0] = 20 (14h).

(3) Example 3: Sub-clock oscillator running at 32.764 kHz

(a) Adjustment procedure

At 32.764 kHz, 1 second elapses on 32,764 clock cycles. Because the RTC operates for 32,768 clock cycles as 1 second, the clock is delayed for 4 clock cycles per second. In 8 seconds, the delay is 32 clock cycles, therefore correction can be made by advancing the clock for 32 clock cycles every 8 seconds.

Register settings when the RCR2.CNTMD bit is 1:

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 32 (20h).

25.3.8.2 Adjustment by software

Enable adjustment by software by setting the RCR2.AADJE bit to 0. Adjustment by software is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register at the time of execution of a write instruction to the RADJ register.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 1 clock cycle per second, so adjustment can take the form of setting the clock back by 1 cycle every second.

(b) Register settings

- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 1 (01h)
  This is written to the RADJ register once per 1-second interrupt.

25.3.8.3 Procedure for changing the mode of adjustment

When changing the mode of adjustment, change the value of the AADJE bit in RCR2 after setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

To change adjustment by software to automatic adjustment:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 1 (automatic adjustment is enabled).
3. Use the RCR2.AADJP bit to select the period of adjustment.
4. In RADJ, set the PMADJ[1:0] bits for addition or subtraction and the ADJ[5:0] bits to the value for use in time error adjustment.

(2) 示例2：以32.766kHz运行的子时钟振荡器

(a) 调整程序

当副时钟振荡器以32.766kHz运行时，每32 766个时钟周期经过1秒。RTC旨在以32 768个时钟周期运行，因此时钟每秒运行2个时钟周期。时钟上的时间每10秒慢20个时钟周期，因此调整可以采取将时钟每10秒向前20个周期的形式。

Register settings: (when RCR2.CNTMD = 0):

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整。）
- RADJ.ADJ[5:0] = 20 (14h).

(3) 示例3：以32.764kHz运行的子时钟振荡器

(a) 调整程序

在32.764kHz时，32 764个时钟周期经过1秒。由于RTC以1秒为单位运行32 768个时钟周期，因此时钟每秒延迟4个时钟周期。在8秒内，延迟为32个时钟周期，因此可以通过每8秒将时钟提前32个时钟周期来进行校正。

RCR2.CNTMD位为1时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 32 (20h).

25.3.8.2 软件调整

通过将RCR2.AADJE位设置为0来启用软件调整。软件调整是在对RADJ执行写指令时将预分频器计数的值与RADJ寄存器中的值相加或相减登记。

(1) 示例1：运行在32.769kHz的子时钟振荡器

(a) 调整程序

当副时钟振荡器以32.769kHz运行时，每32 769个时钟周期经过1秒。RTC旨在以32 768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每秒快1个时钟周期，因此调整可以采取将时钟每秒调回1个周期的形式。

(b) 注册设置

- RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 1 (01h)
  每1秒中断一次将其写入RADJ寄存器。

25.3.8.3 更改调整模式的步骤

改变调节方式时，设置好后改变RCR2中ADJE位的值
RADJ.PMADJ[1:0]位到00b（不执行调整）。

将软件调整改为自动调整：

1. 将RADJ.PMADJ[1:0]位设置为00b（不执行调整）。
2. 将RCR2.AADJE位设置为1（启用自动调整）。
3. 使用RCR2.AADJP位选择调整周期。
4. 在RADJ中，将PMADJ[1:0]位设置为加法或减法，并将ADJ[5:0]位设置为用于时间误差调整的值。

To change automatic adjustment to adjustment by software:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 0 (adjustment by software is enabled).
3. Proceed with the adjustment by setting the RADJ.PMADJ[1:0] bits for addition or subtraction and the RADJ.ADJ[5:0] bits to the value for use in time error adjustment at the desired time. After that, the time is adjusted every time a value is written to the RADJ register.

25.3.8.4 Procedure for stopping adjustment

Stop the adjustment by setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

25.3.8.5 Capturing the time

The RTC is capable of storing the month, date, hour, minute and second/binary counters 3 to 0 by detecting an edge of a signal on a time capture event input pin.

A noise filter can also be used on a time capture event input pin. If the noise filter is enabled, the TCST bit is set to 1 when the input level on the pin matches three times.

The noise filter can be switched on or off for each of the time capture event input pins. VBTICTLR.VCH0IEN should be set to 1 to enable the RTCIC0 input. Operation when the noise filter is off is shown in Figure 25.9 and operation when the noise filter is on is shown in Figure 25.10.

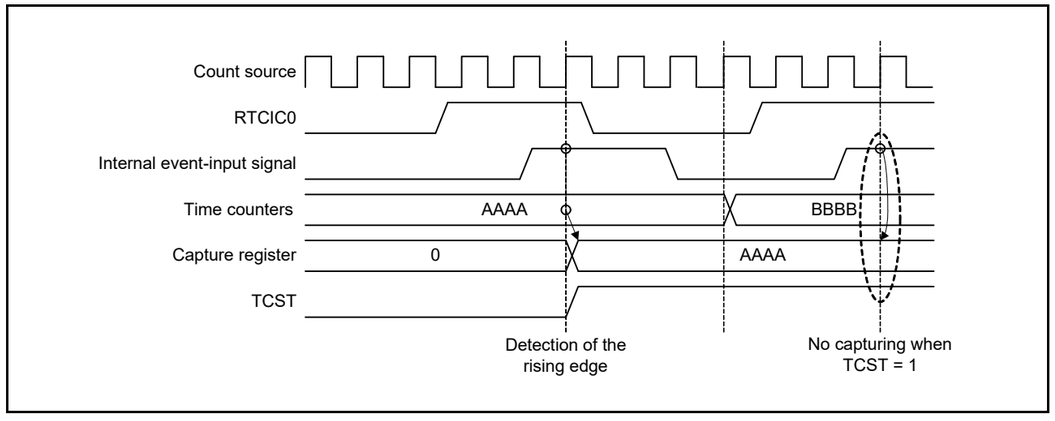


Figure 25.9 Timing of a time capture operation with the filter off

将自动调整更改为软件调整：

1. 将RADJ.PMADJ[1:0]位设置为00b（不执行调整）。
2. 将RCR2.AADJE位设置为0（启用软件调整）。
3. 通过设置RADJ.PMADJ[1:0]位进行加法或减法以及RADJ.ADJ[5:0]位的值用于在所需时间进行时间误差调整。之后，每次将值写入RADJ寄存器时都会调整时间。

25.3.8.4 停止调整的步骤

通过将RADJ.PMADJ[1:0]位设置为00b来停止调整（不执行调整）。

25.3.8.5 捕捉时间

RTC能够通过检测时间捕捉事件输入引脚上的信号沿来存储月、日、小时、分钟和秒二进制计数器3到0。

噪声滤波器也可用于时间捕捉事件输入引脚。如果启用了噪声滤波器，则当引脚上的输入电平匹配3次时，TCST位设置为1。

可以为每个时间捕捉事件输入引脚打开或关闭噪声滤波器。VBTICTLR.VCH0IEN应设置为1以启用RTCIC0输入。噪声滤波器关闭时的操作如图25.9所示，噪声滤波器打开时的操作如图25.10所示。

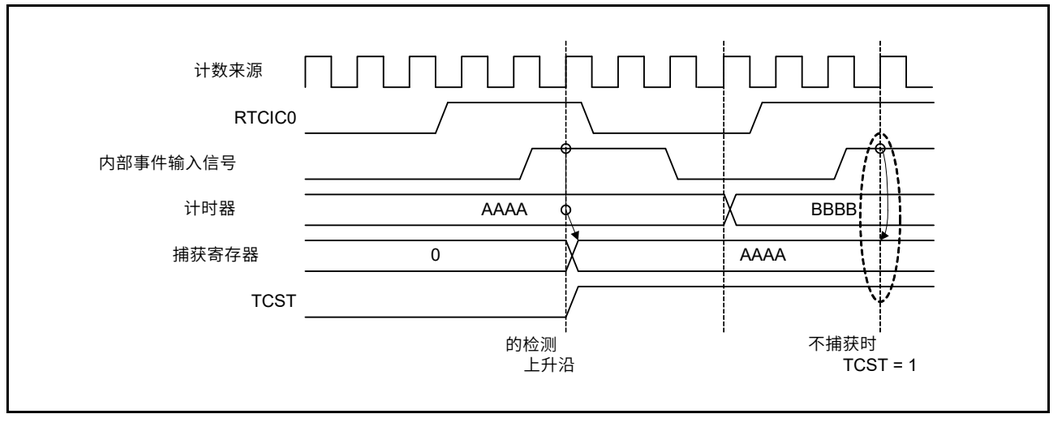


Figure 25.9 过滤器关闭的时间捕获操作的时序

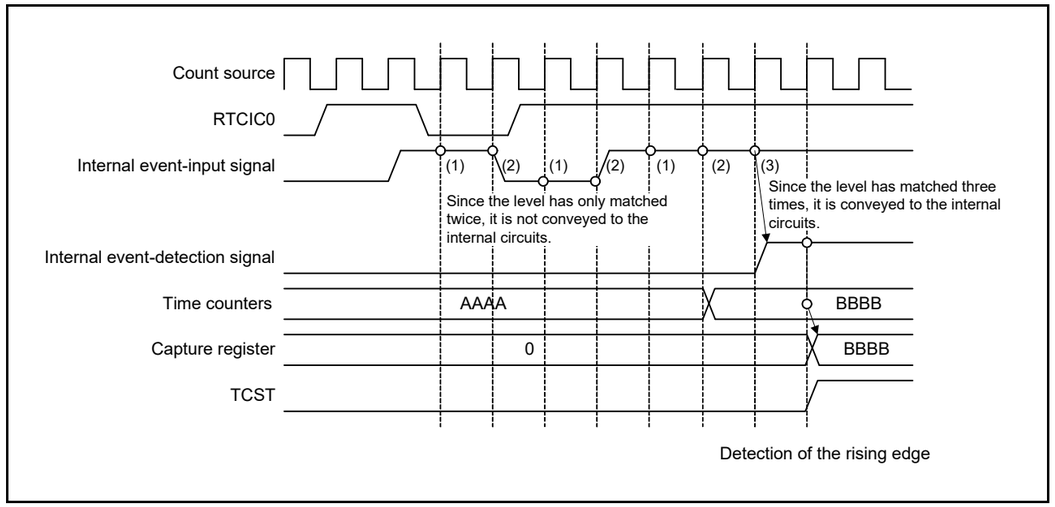


Figure 25.10 Timing of a time capture operation with the filter on

25.4 Interrupt Sources

The RTC has three interrupt sources and are listed in Table 25.3.

Table 25.3 RTC Interrupt sources

Name	Interrupt sources
RTC_ALM	Alarm interrupt
RTC_PRD	Periodic interrupt
RTC_CUP	Carry interrupt

(1) Alarm interrupt (RTC_ALM)

This interrupt is generated based on the comparison result between the alarm registers and RTC counters. For details, see section 25.3.6, Alarm Function.

Because there is a possibility that the interrupt flag might be set to 1 when the settings of the alarm registers match the clock counters, wait for the alarm time settings to be confirmed and clear the IELSRn.IR bit and the Interrupt Set-Pending Register associated with the RTC_ALM interrupt to 0 again after modifying values of the alarm registers. After the interrupt flag for the alarm interrupt is set to 1 and the state is returned to mismatching of the alarm registers and clock counters, the flag is not set again until there is another match or the values of the alarm registers are modified again.

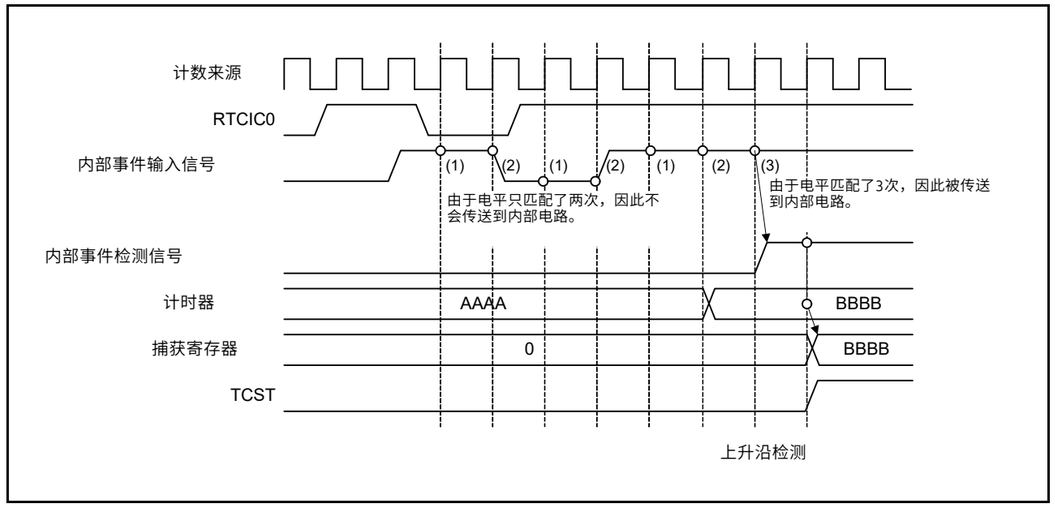


Figure 25.10 开启滤波器的时间捕获操作的时序

25.4 中断源

RTC具有三个中断源，列于表25.3中。

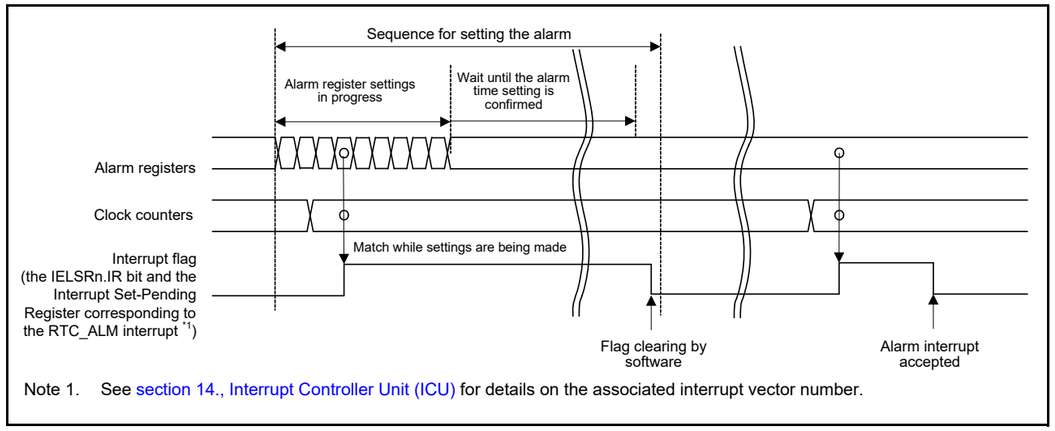
Table 25.3 RTC中断源

Name	中断源
RTC_ALM	报警中断
RTC_PRD	周期性中断
RTC_CUP	进位中断

(1) 闹钟中断(RTC_ALM)

该中断是根据闹钟寄存器和RTC计数器之间的比较结果产生的。有关详细信息，请参见第25.3.6节，报警功能。

因为当闹钟寄存器的设置与时钟计数器匹配时中断标志可能被设置为1，请等待闹钟时间设置被确认并清除IELSRn.IR位和与修改闹钟寄存器的值后，RTC_ALM中断再次为0。报警中断的中断标志置1并返回报警寄存器和时钟计数器不匹配的状态后，直到再次匹配或再次修改报警寄存器的值时才再次设置该标志。



Note 1. See section 14., Interrupt Controller Unit (ICU) for details on the associated interrupt vector number.

Figure 25.11 Timing for the alarm interrupt (RTC_ALM)

(2) Periodic interrupt (RTC_PRD)

This interrupt is generated at intervals of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second. The interrupt interval can be selected through the RCR1.PES[3:0] bits.

(3) Carry interrupt (RTC_CUP)

This interrupt is generated when a carry to the second counter/binary counter 0 occurred or a carry to the R64CNT counter occurred during read access to the 64-Hz counter.

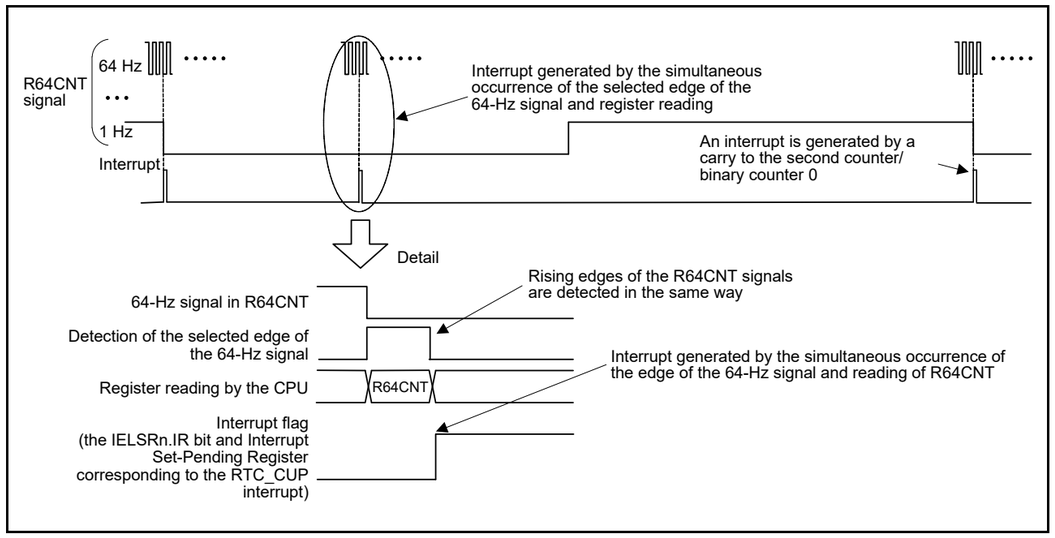
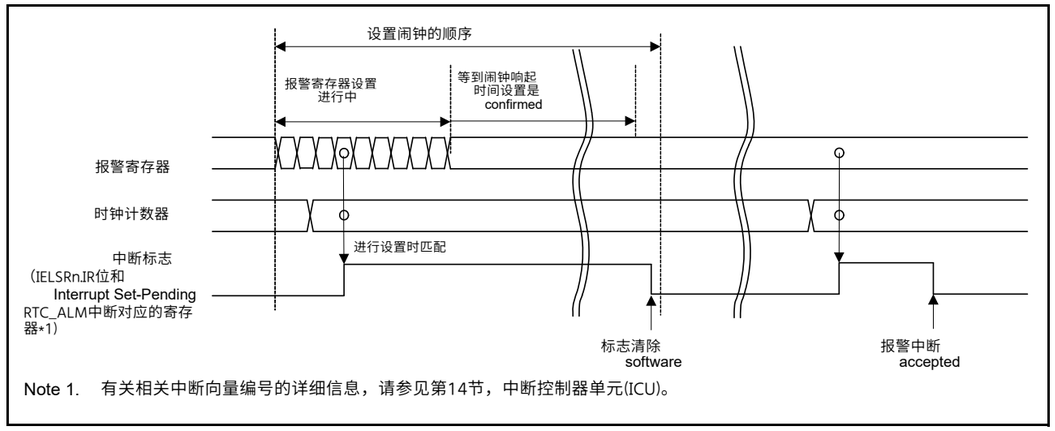


Figure 25.12 Timing for the carry interrupt (RTC_CUP)

25.5 Event Link Output

The RTC generates periodic event output (RTC_PRD) event signals for the Event Link Controller (ELC) that can be used to initiate operations by other modules selected in advance.

The periodic event signal is output at the interval selected from 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, and 2 seconds by setting the RCR1.PES[3:0] bits.



Note 1. 有关相关中断向量编号的详细信息，请参见第14节，中断控制器单元(ICU)。

Figure 25.11 闹钟中断的时序(RTC_ALM)

(2) 周期性中断(RTC_PRD)

此中断以2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒的间隔生成。可以通过RCR1.PES[3:0]位选择中断间隔。

(3) 进位中断(RTC_CUP)

当第二个计数器二进制计数器0的进位发生或在对64-Hz计数器的读访问期间发生对R64CNT计数器的进位时，将产生此中断。

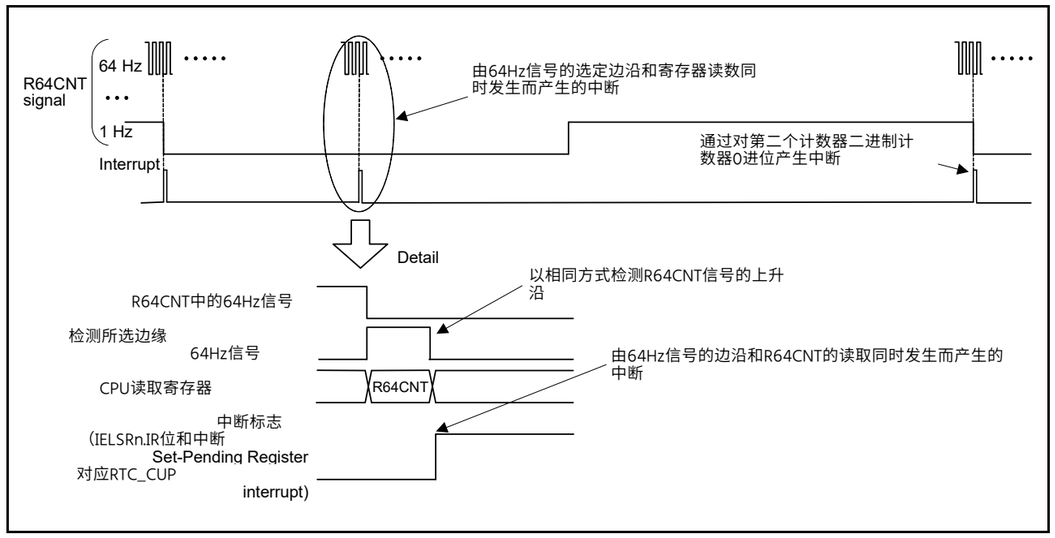


Figure 25.12 进位中断(RTC_CUP)的时序

25.5 事件链接输出

RTC为事件链接控制器(ELC)生成周期性事件输出(RTC_PRD)事件信号，该信号可用于启动预先选择的其他模块的操作。

通过设置RCR1.PES[3:0，以从1256、1128、164、132、116、18、14、12、1和2秒中选择的间隔输出周期性事件信号]位。

The event generation period immediately after the event generation is selected, is not guaranteed.

Note: If event linking from the RTC is used, only set the ELC after setting the RTC, for example, initialization and time settings. Setting the RTC after the ELC can lead to output of unexpected event signals.

25.5.1 Interrupt Handling and Event Linking

The RTC has a bit to enable or disable periodic interrupts. An interrupt request signal is output to the CPU when an interrupt source is generated while the associated enable bit is enabled.

In contrast, an event link output signal is sent to other modules as an event signal through the ELC when an interrupt source is generated, regardless of the setting of the associated interrupt enable bit.

Note: Although alarm and periodic interrupts can still be output during Software Standby mode, the periodic event signals for the ELC are not output.

25.6 Usage Notes

25.6.1 Register Writing during Counting

The following registers must not be written to during counting, that is, while the RCR2.START bit = 1.

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL.

The counter must be stopped before writing to any of the these registers.

25.6.2 Use of Periodic Interrupts

The procedure for using periodic interrupts is shown in Figure 25.13.

The generation and period of the periodic interrupt can be changed by setting the RCR1.PES[3:0] bits. However, because the prescaler R64CNT and RSECCNT/BCNT0 are used to generate interrupts, the interrupt period is not guaranteed immediately after setting the RCR1.PES[3:0] bits. In addition, any of the following can affect the interrupt period:

- Stopping/restarting or resetting counter operation
- Reset by RTC software
- 30-second adjustment by changing the RCR2 value.

When the time error adjustment function is used, the interrupt generation period after adjustment is added or subtracted based on the adjustment value.

不保证选择事件生成后的事件生成周期。

Note: 如果使用来自RTC的事件链接，则仅在设置RTC后设置ELC，例如初始化和时间设置。在ELC之后设置RTC会导致意外事件信号的输出。

25.5.1 中断处理和事件链接

RTC有一个位来启用或禁用周期性中断。当相关使能位使能时产生中断源时，将向CPU输出中断请求信号。

相反，当产生中断源时，事件链接输出信号作为事件信号通过ELC发送到其他模块，而不管相关中断使能位的设置如何。

Note: 虽然在软件待机模式下仍然可以输出警报和周期性中断，但不会输出ELC的周期性事件信号。

25.6 使用说明

25.6.1 计数期间的寄存器写入

计数期间不得写入以下寄存器，即RCR2.START位=1时。

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL.

在写入这些寄存器中的任何一个之前，必须停止计数器。

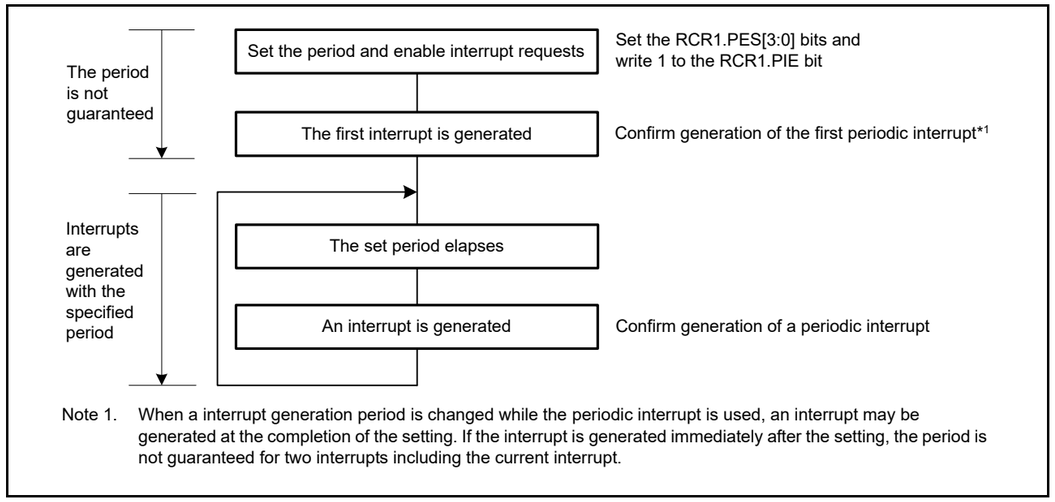
25.6.2 使用周期性中断

使用周期性中断的过程如图25.13所示。

可以通过设置RCR1.PES[3:0]位来更改周期性中断的产生和周期。但是，因为预分频器R64CNT和RSECCNTBCNT0用于产生中断，所以在设置RCR1.PES[3:0]位后不能立即保证中断周期。此外，以下任何一项都会影响中断周期：

- 停止重新启动或重置计数器操作
- 通过RTC软件复位
- 通过更改RCR2值进行30秒调整。

使用时间误差调整功能时，根据调整值加减调整后的中断产生周期。



Note 1. When a interrupt generation period is changed while the periodic interrupt is used, an interrupt may be generated at the completion of the setting. If the interrupt is generated immediately after the setting, the period is not guaranteed for two interrupts including the current interrupt.

Figure 25.13 Using the periodic interrupt function

25.6.3 RTCOUT (1-Hz/64-Hz) Clock Output

Stopping/restarting or resetting counter operation, reset by RTC software, and the 30-second adjustment by changing the RCR2 value, affects the period of RTCOUT (1-Hz/64-Hz) output. When the time error adjustment function is used, the period of RTCOUT (1-Hz/64-Hz) output after adjustment is added or subtracted based on the adjustment value.

25.6.4 Transitions to Low Power Modes after Setting Registers

A transition to a low power state (Software Standby mode or battery backup) during a write to an RTC register might corrupt the value in the register. After setting the register, confirm that the setting is in place before initiating a transition to a low power state.

25.6.5 Notes on Writing to and Reading from Registers

- When reading a counter register such as the second counter after writing to the counter register, follow the procedure in section 25.3.5, Reading 64-Hz Counter and Time
- The value written to the count registers, alarm registers, year alarm enable register, bits RCR2.AADJE, AADJP, and HR24, RCR4 register, or frequency register is reflected when four read operations are performed after writing
- The values written to the RCR1.CIE, RCR1.RTCOS, and RCR2.RTCOE bits can be read immediately after writing
- To read the value from the timer counter after returning from a reset, a period in Software Standby mode, or the battery backup state, wait for1/128 second while the clock is operating (RCR2.START bit = 1)
- After a reset is generated, write to the RTC register after 6 cycles of the count source clock have elapsed.

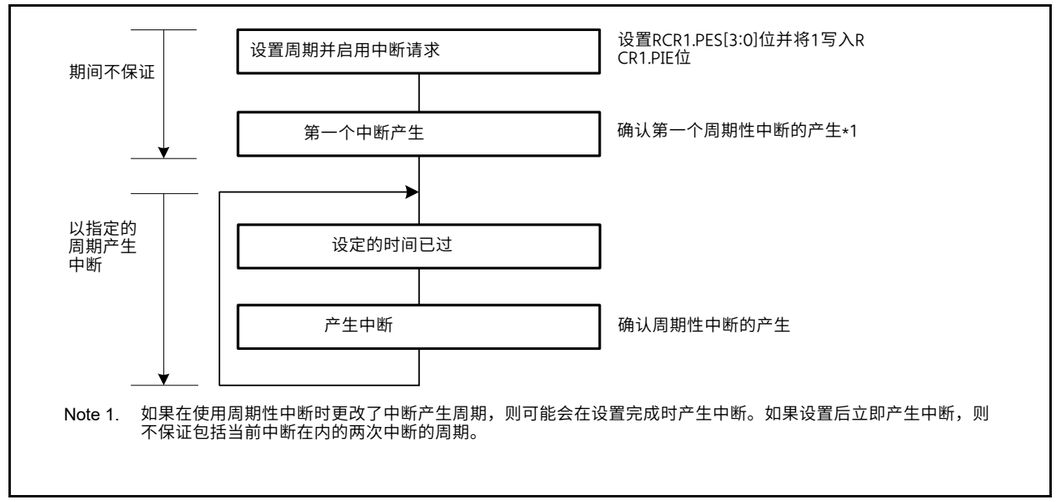
25.6.6 Changing the Count Mode

When changing the count mode (calendar/binary), set the RCR2.START bit to 0, stop the counting operation, then restart it from the initial setting. For details on the initial setting, see section 25.3.1, Outline of Initial Settings of Registers after Power On.

25.6.7 Initialization Procedure when the RTC is not to be Used

Registers in the RTC are not initialized by a reset. Depending on the initial state, the generation of an unintentional interrupt request or operation of the counter might lead to increased power consumption.

For applications that do not require a realtime clock, initialize the registers by following the initialization procedure shown in Figure 25.14.



Note 1. 如果在使用周期性中断时更改了中断产生周期，则可能会在设置完成时产生中断。如果设置后立即产生中断，则不保证包括当前中断在内的两次中断的周期。

Figure 25.13 使用周期性中断功能

25.6.3 RTCOUT(1-Hz64-Hz)时钟输出

停止重新启动或重置计数器操作、由RTC软件重置以及通过更改RCR2值进行的30秒调整，都会影响RTCOUT(1-Hz64-Hz)输出的周期。使用时间误差调整功能时，调整后的RTCOUT（1-Hz64-Hz）输出的周期根据调整值加减。

25.6.4 设置寄存器后转换到低功耗模式

在写入RTC寄存器期间转换到低功耗状态（软件待机模式或电池备份）可能会损坏寄存器中的值。设置寄存器后，在开始转换到低功耗状态之前确认设置到位。

25.6.5 关于写入和读取寄存器的注意事项

- 在写入计数器寄存器后读取计数器寄存器（例如第二个计数器）时，请按照第25.3.5节中的步骤，读取64-Hz计数器和时间
- 写入计数寄存器、闹钟寄存器、年份闹钟启用寄存器、位RCR2.AADJE、AADJP和HR24、RCR4寄存器或频率寄存器在写后进行四次读操作时反映
- 写入RCR1.CIE、RCR1.RTCOS和RCR2.RTCOE位的值可在写入后立即读取
- 要在从复位、软件待机模式或电池备份状态返回后从定时器计数器读取值，请在时钟运行时等待1128秒（RCR2.START位=1）
- 产生复位后，在计数源时钟的6个周期过去后写入RTC寄存器。

25.6.6 更改计数模式

更改计数模式（日历二进制）时，将RCR2.START位设置为0，停止计数操作，然后从初始设置重新启动。有关初始设置的详细信息，请参阅第25.3.1节"通电后寄存器初始设置概要"。

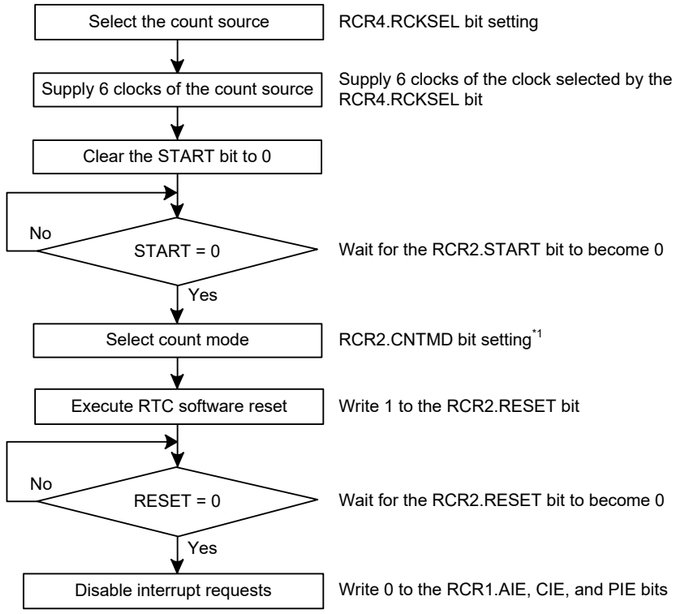
25.6.7 不使用RTC时的初始化程序

RTC中的寄存器不会因复位而初始化。根据初始状态，意外中断请求的生成或计数器的操作可能会导致功耗增加。

对于不需要实时时钟的应用程序，按照图25.14所示的初始化过程初始化寄存器。

Alternatively, when the sub-clock oscillator is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (sub-clock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock oscillator. To stop the sub-clock oscillator, write 1 to the SOSCCR.SOSTP bit.

For details on the setting of the SOSCCR.SOSTP bit, see section 9, Clock Generation Circuit.



Note 1. This step is not required if the count mode is set concurrently by setting the START bit to 0.

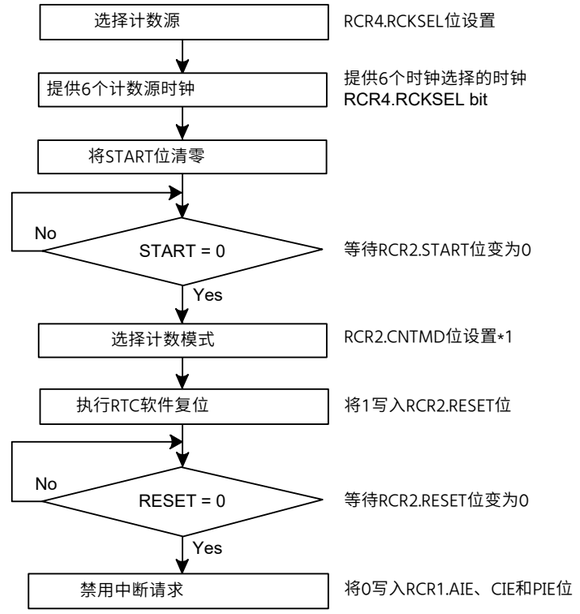
Figure 25.14 Initialization procedure

25.6.8 When Switching Source Clock

When switching a clock source by changing SCKCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. If the RTC periodical interrupt or RTC periodical event output was generated at this time, the interrupt or event is invalid.

或者，当副时钟振荡器不用作系统时钟或实时时钟时，可以通过向RCR4.RCKSEL位写入0（选择副时钟振荡器）并停止副时钟振荡器来停止计数器。要停止副时钟振荡器，将1写入SOSCCR.SOSTP位。

有关SOSCCR.SOSTP位设置的详细信息，请参见第9节，时钟生成电路。



Note 1. 如果通过将START位设置为0同时设置计数模式，则不需要此步骤。

Figure 25.14 初始化程序

25.6.8 切换源时钟时

当通过改变SCKCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。如果此时产生了RTC周期性中断或RTC周期性事件输出，则该中断或事件无效。

26. Watchdog Timer (WDT)

26.1 Overview

The Watchdog Timer (WDT) is a 14-bit down-counter and can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. The refresh-permitted period can be set to refresh the counter and to detect when the system runs out of control.

Table 26.1 lists the WDT specifications and Figure 26.1 shows a block diagram.

Table 26.1 WDT specifications

Parameter	Specifications
Count source	Peripheral clock (PCLKB)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto start mode: Counting automatically starts after a reset, or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated.
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output.

26. 看门狗定时器(WDT)

26.1 Overview

看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。可以设置刷新允许周期来刷新计数器并检测系统何时失控。

表26.1列出了WDT规范，图26.1显示了框图。

Table 26.1 WDT specifications

Parameter	Specifications
计数来源	外设时钟(PCLKB)
时钟分频比	除以4、64、128、512、2 048或8 192
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	自动启动模式：在复位后或发生下溢或刷新错误后自动开始计数 寄存器启动模式：通过写入WDTRR寄存器以刷新开始计数
停止计数器的条件	复位（递减计数器和其他寄存器返回其初始值） 计数器下溢或产生刷新错误。
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
看门狗定时器复位源	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）。
Non-maskable interrupt/interrupt sources	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）。
读取计数器值	递减计数器的值可以通过WDTSR寄存器读取
事件链接功能（输出）	递减计数器下溢事件输出 刷新错误事件输出。
输出信号（内部信号）	复位输出 中断请求输出 睡眠模式计数停止控制输出。

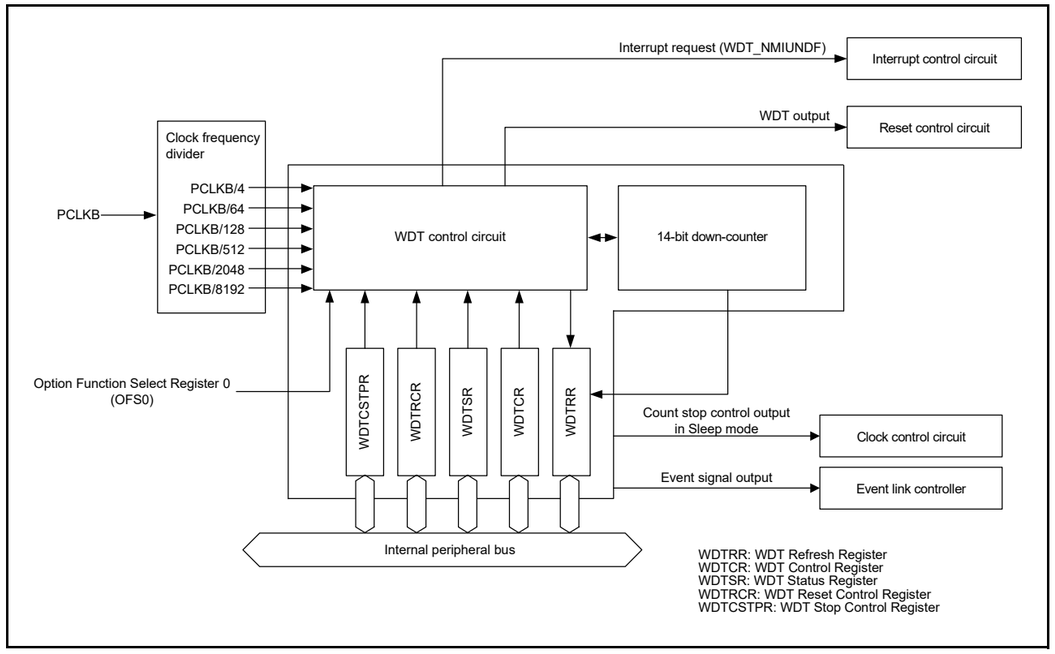


Figure 26.1 WDT block diagram

26.2 Register Descriptions

26.2.1 WDT Refresh Register (WDTRR)

Address(es): WDT.WDTRR 4004 4200h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 00h and then writing FFh to WDTRR (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected by the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected by the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details of the refresh operation, see section 26.3.3, Refresh Operation.

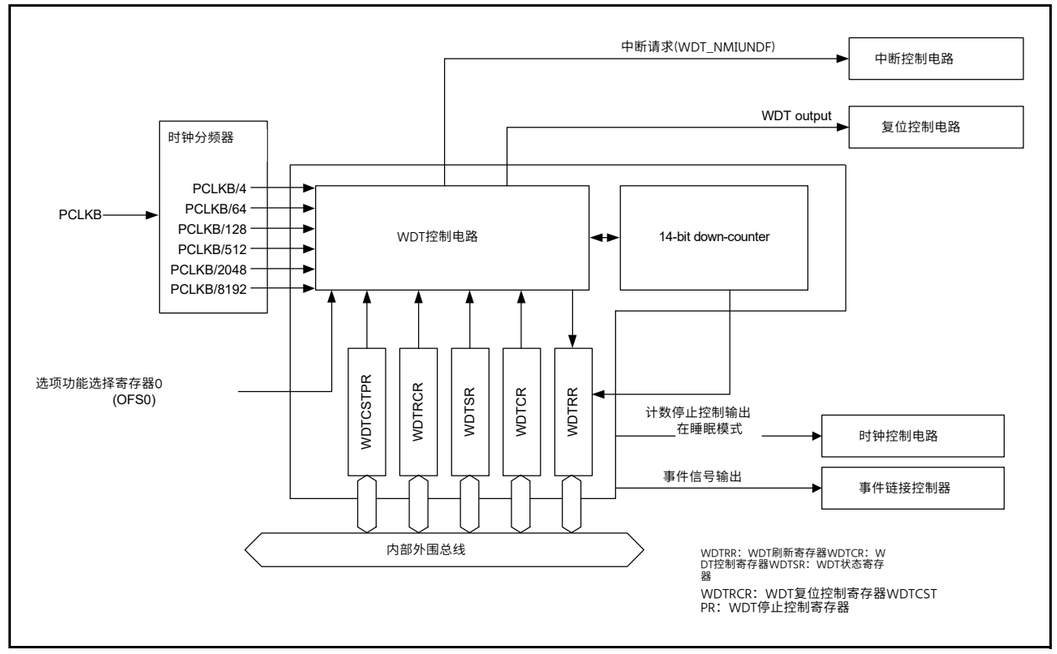


Figure 26.1 看门狗框图

26.2 注册说明

26.2.1 WDT刷新寄存器(WDTRR)

Address(es): WDT.WDTRR 4004 4200h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	通过写入00h然后将FFh写入该寄存器来刷新递减计数器	R/W

WDTRR寄存器刷新WDT的递减计数器。

WDT的递减计数器通过写入00h进行刷新，然后在允许刷新期间将FFh写入WDTRR（刷新操作）。

递减计数器刷新后，在自动启动模式下，它从选项功能选择寄存器0中的WDT超时周期选择位(OFS0.WDTTOPS[1:0])选择的值开始递减计数。在寄存器启动模式下，倒计时从WDT控制寄存器中的超时周期选择位(WDTCR.TOPS[1:0])选择的值开始。

写入00h时，读取值为00h。写入00h以外的值时，读取值为FFh。有关刷新操作的详细信息，请参阅第26.3.3节，刷新操作。

26.2.2 WDT Control Register (WDTCR)

Address(es): WDT.WDTCR 4004 4202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Select	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh).	R/W
b3, b2	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b7 to b4	CKS[3:0]	Clock Division Ratio Select	b7 b4 0 0 0 1: PCLKB/4 0 1 0 0: PCLKB/64 1 1 1 1: PCLKB/128 0 1 1 0: PCLKB/512 0 1 1 1: PCLKB/2048 1 0 0 0: PCLKB/8192. Other setting are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified).	R/W
b11, b10	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b13, b12	RPSS[1:0]	Window Start Position Select	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified).	R/W
b15, b14	—	Reserved	These bits are read as 0 and cannot be modified	R/W

Some constraints apply to writes to the WDTCR register. For details, see section 26.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made for the OFS0 register. For details, see section 26.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period (the period until the down-counter underflows) from 1,024, 4,096, 8,192, and 16,384 cycles, taking the divided clock specified by the CKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (number of PCLKB cycles) until the counter underflows.

Table 26.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

26.2.2 WDT控制寄存器(WDTCR)

Address(es): WDT.WDTCR 4004 4202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
重置后的值:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	TOPS[1:0]	超时时间选择	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh).	R/W
b3, b2	—	Reserved	这些位被读为0，不能修改	R/W
b7 to b4	CKS[3:0]	时钟分频比选择	b7 b4 0 0 0 1: PCLKB/4 0 1 0 0: PCLKB/64 1 1 1 1: PCLKB/128 0 1 1 0: PCLKB/512 0 1 1 1: PCLKB/2048 1 0 0 0: PCLKB/8192. 禁止其他设置。	R/W
b9, b8	RPES[1:0]	窗口结束位置选择	b9b800：75%01：50%10：25%11：0%（未指定窗口结束位置）。	R/W
b11, b10	—	Reserved	这些位被读为0，不能修改	R/W
b13, b12	RPSS[1:0]	窗口起始位置选择	b13b1200：25%01：50%10：75%11：100%（未指定窗口起始位置）。	R/W
b15, b14	—	Reserved	这些位被读为0，不能修改	R/W

一些限制适用于写入WDTCR寄存器。有关详细信息，请参阅第26.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTCR寄存器中的设置被禁用，OptionFunctionSelect中的设置使能寄存器0(OFS0)。WDTCR寄存器的设置也可以对OFS0寄存器进行。有关详细信息，请参阅第26.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

TOPS[1:0]位（超时周期选择）

TOPS[1:0]位从1 024、4 096、8 192和16 384个周期中选择超时周期（直到递减计数器下溢的周期），以CKS[3:0]位指定的分频时钟为1个周期.

向下计数器刷新后，CKS[3:0]和TOPS[1:0]位的组合决定了计数器下溢之前的时间（PCLKB周期数）。

表26.2列出了CKS[3:0]和TOPS[1:0]位设置、超时时间和PCLKB cycles.

Table 26.2 Timeout period settings

CKS[3:0] bits				TOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLKB/4	1024	4096
				0	1		4096	16384
				1	0		8192	32768
				1	1		16384	65536
0	1	0	0	0	0	PCLKB/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	PCLKB/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	1	0	0	0	PCLKB/512	1024	524288
				0	1		4096	2097152
				1	0		8192	4194304
				1	1		16384	8388608
0	1	1	1	0	0	PCLKB/2048	1024	2097152
				0	1		4096	8388608
				1	0		8192	16777216
				1	1		16384	33554432
1	0	0	0	0	0	PCLKB/8192	1024	8388608
				0	1		4096	33554432
				1	0		8192	67108864
				1	1		16384	134217728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the peripheral clock (PCLKB) divided by 4, 64, 128, 512, 2048, and 8,192. Combined with the TOPS[1:0] bit setting, a count period between 4,096 and 134,217,728 PCLKB clock cycles can be selected for the WDT.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. The selected window end position should be a value smaller than the value for the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window end position. The window start position should be set to a value greater than the value for the window end position. If the window start position is set to a value smaller than or equal to the window end position, the window end position is set to 0%.

Table 26.3 lists the counter values for the window start and end positions, and Figure 26.2 shows the refresh-permitted period set by the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 26.2 超时时间设置

CKS[3:0] bits				TOPS[1:0] bits		时钟分频比	超时时间（周期数）	PCLKB时钟周期
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLKB/4	1024	4096
				0	1		4096	16384
				1	0		8192	32768
				1	1		16384	65536
0	1	0	0	0	0	PCLKB/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	PCLKB/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	1	0	0	0	PCLKB/512	1024	524288
				0	1		4096	2097152
				1	0		8192	4194304
				1	1		16384	8388608
0	1	1	1	0	0	PCLKB/2048	1024	2097152
				0	1		4096	8388608
				1	0		8192	16777216
				1	1		16384	33554432
1	0	0	0	0	0	PCLKB/8192	1024	8388608
				0	1		4096	33554432
				1	0		8192	67108864
				1	1		16384	134217728

CKS[3:0]位（时钟分频比选择）

CKS[3:0]位指定用于递减计数器的时钟的分频比。分频比可以从外设时钟(PCLKB)除以4、64、128、512、2048和8 192中选择。结合TOPS[1:0]位设置，可以为WDT选择4 096到134 217 728个PCLKB时钟周期之间的计数周期。

RPES[1:0]位（窗口结束位置选择）

RPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。所选窗口结束位置的值应小于窗口开始位置的值（窗口开始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

RPSS[1:0]位（窗口起始位置选择）

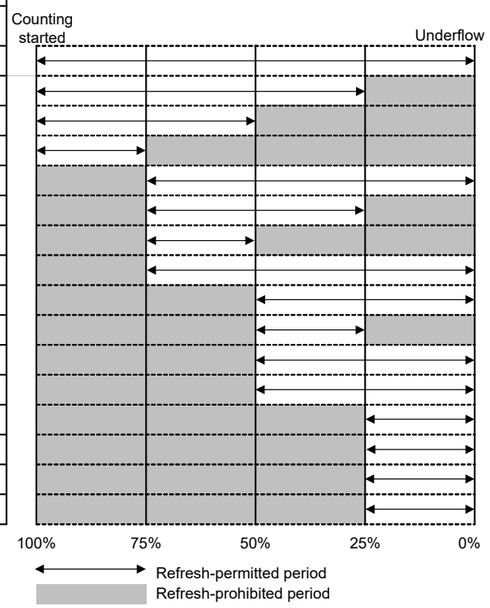
RPSS[1:0]位指定指示允许刷新周期的窗口起始位置。可以为窗口结束位置选择100%、75%、50%或25%的超时时间。窗口起始位置应设置为大于窗口结束位置的值。如果窗口开始位置设置为小于或等于窗口结束位置的值，则窗口结束位置设置为0%。

表26.3列出了窗口开始和结束位置的计数器值，图26.2显示了由RPSS[1:0]、RPES[1:0]和TOPS[1:0]位设置的允许刷新周期。

Table 26.3 Relationship between timeout period and window start and end counter values

TOPS[1:0] bits		Timeout period		Window start and end counter value			
		Cycles	Counter value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] bits		RPES[1:0] bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 26.2 RPSS[1:0] and RPES[1:0] bit settings and refresh-permitted period

26.2.3 WDT Status Register (WDTSR)

Address(es): WDT.WDTSR 4004 4204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

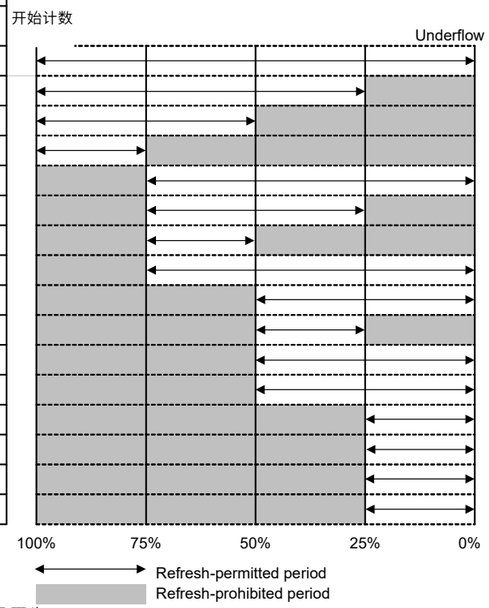
Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R(/W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred.	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

Table 26.3 超时时间与窗口开始和结束计数器值之间的关系

TOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
		Cycles	计数器值	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] bits		RPES[1:0] bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75



Note: 如果窗口结束设置 窗口开始设置，则窗口结束设置设置为0%。

Figure 26.2 RPSS[1:0]和RPES[1:0]位设置和允许刷新周期

26.2.3 WDT状态寄存器(WDTSR)

Address(es): WDT.WDTSR 4004 4204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	递减计数器计数的值	R
b14	UNDFF	Underflow Flag	0：未发生下溢1：发生下溢。	R(/W) *1
b15	REFEF	刷新错误标志	0：未发生刷新错误1：发生刷新错误。	R(/W) *1

Note 1. 只能写入0来清除标志。

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by a value of one count.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. A value of 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles following an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. A value of 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of this flag is ignored for (N+1) PCLKB cycles following a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192.

26.2.4 WDT Reset Control Register (WDTRCR)

Address(es): WDT.WDTRCR 4004 4206h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b7	RSTIRQS	Reset Interrupt Request Select	0: Non-maskable interrupt request or interrupt request output is enabled 1: Reset output is enabled.	R/W

Some constraints apply to writes to the WDTRCR register. For details, see section 26.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made for the OFS0 register. For details, see section 26.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

CNTVAL[13:0]位（递减计数器值）

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差一个计数。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认递减计数器中是否发生下溢。值1表示递减计数器下溢。将0写入UNDFF标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+1)个PCLKB周期。此外，在下溢后的(N+1)个PCLKB周期内忽略标志的清除。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192

REFEF标志（刷新错误标志）

读取REFEF标志以确认是否发生刷新错误。值1表示发生了刷新错误。
将0写入REFEF标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+1)个PCLKB周期。此外，在刷新错误后的(N+1)个PCLKB周期内，该标志的清除将被忽略。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192.

26.2.4 WDT复位控制寄存器(WDTRCR)

Address(es): WDT.WDTRCR 4004 4206h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读为0，不能修改	R/W
b7	RSTIRQS	复位中断请求选择	0：使能不可屏蔽中断请求或中断请求输出1：使能复位输出。	R/W

一些限制适用于写入WDTRCR寄存器。有关详细信息，请参阅第26.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTRCR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。WDTCR寄存器的设置也可以对OFS0寄存器进行。有关详细信息，请参阅第26.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

26.2.5 WDT Count Stop Control Register (WDTCSTPR)

Address(es): WDT.WDTCSTPR 4004 4208h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0 and cannot be modified	R/W
b7	SLCSTP	Sleep-Mode Count Stop Control	0: Count stop is disabled 1: Count is stopped when transition to Sleep mode.	R/W

The WDTCSTPR register controls whether to stop the WDT counter in a low power state. Some constraints apply to writes to the WDTCSTPR register. For details, see section 26.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 26.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (Sleep-Mode Count Stop Control)

The SLCSTP bit selects whether to stop counting when transition to Sleep mode.

26.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 26.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

26.3 Operation

26.3.1 Count Operation in Each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting starts with a refresh by writing to the register.

In auto start mode, counting automatically starts after release from the reset state according to the settings in the Option Function Select Register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the register after the respective registers are set after release from the reset state.

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register.

When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

When the register start mode is selected, the setting for the OFS0 register is disabled while the settings for the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

26.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected and the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

26.2.5 WDT计数停止控制寄存器(WDTCSTPR)

Address(es): WDT.WDTCSTPR 4004 4208h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读为0，不能修改	R/W
b7	SLCSTP	睡眠模式计数停止控制	0：禁止计数停止1：转换到睡眠模式时停止计数。	R/W

WDTCSTPR寄存器控制是否在低功耗状态下停止WDT计数器。一些限制适用于写入WDTCSTPR寄存器。有关详细信息，请参见第26.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

在自动启动模式下，WDTCSTPR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。也可以对OFS0寄存器进行WDTCSTPR寄存器的设置。有关详细信息，请参阅第26.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

SLCSTP位（休眠模式计数停止控制）

SLCSTP位选择在转换到休眠模式时是否停止计数。

26.2.6 选项功能选择寄存器0(OFS0)

有关OFS0寄存器的信息，请参见第26.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

26.3 Operation

26.3.1 每种启动模式下的计数操作

WDT有两种启动模式：

- 自动启动模式，从复位状态释放后自动开始计数
- 寄存器启动模式，在这种模式下，通过写入寄存器来开始计数。

在自动启动模式下，根据选项中的设置从复位状态释放后自动开始计数
功能选择闪存中的寄存器0(OFS0)。

在寄存器启动模式下，从复位状态释放后，在设置各个寄存器后，通过写入寄存器来开始计数。

通过设置OFS0寄存器中的WDT启动模式选择位(OFS0.WDTSTRT)来选择自动启动模式或寄存器启动模式。

选择自动启动模式后，WDT控制寄存器（WDTCR）中的设置，WDTRESET控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）在启用OFS0寄存器中的设置时被禁用。

选择寄存器启动模式时，在WDT的设置时禁用OFS0寄存器的设置
使能控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

26.3.1.1 注册启动模式

当WDT启动模式选择位(OFS0.WDTSTRT)为1时，选择寄存器启动模式并且WDT控制
使能寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

After the reset state is released, set the following to Sleep mode in the WDTCSTPR register:

- Clock division ratio
- Window start and end positions
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transition to Sleep mode in the WDTCSTPR register.

Refresh the down-counter to start counting down from the value set in the Timeout Period Select bits (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs a reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 26.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).

释放复位状态后，在WDTCSTPR寄存器中将以下内容设置为休眠模式：

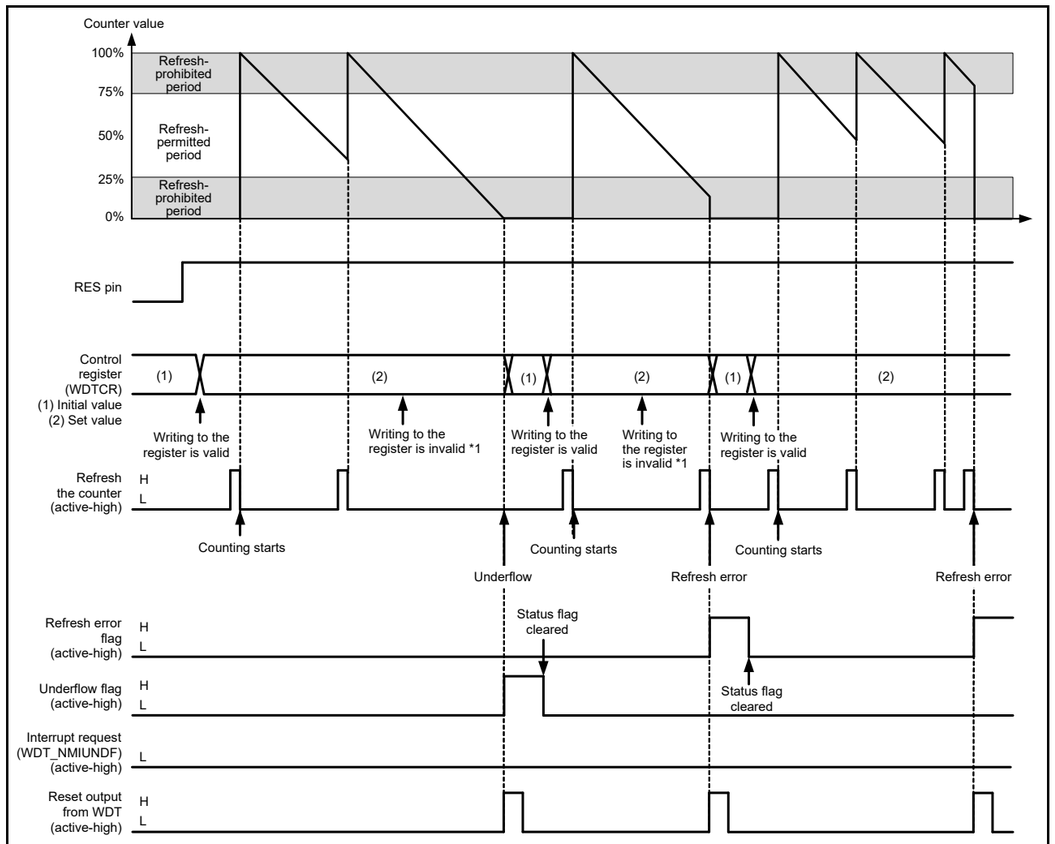
- 时钟分频比
- 窗口开始和结束位置
- WDTCR寄存器中的超时时间
- WDTRCR寄存器中的复位输出或中断请求输出
- 在WDTCSTPR寄存器中转换到休眠模式期间的计数器停止控制。

刷新递减计数器以从超时周期选择位(WDTCR.TOPS[1:0])中设置的值开始递减计数。

此后，只要在可刷新期间刷新了计数器，则每次刷新计数器时都会重置计数器中的值，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果由于程序失控导致递减计数器无法刷新而导致递减计数器下溢，或者由于计数器在刷新允许时间之外刷新而发生刷新错误，则WDT输出复位信号或非可屏蔽中断请求中断请求(WDT_NMIUNDF)。可以在WDT复位中断请求选择位(WDTRCR.RSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断　　允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图26.3显示了以下条件下的操作示例：

- 寄存器启动模式（OFS0.WDTSTRT=1）
- 使能复位输出(WDTRCR.RSTIRQS=1)
- 窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)
- 窗口结束位置为25%(WDTCR.RPES[1:0]=10b)。



Note 1. See 26.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

Figure 26.3 Operation example in register start mode

26.3.1.2 Auto start mode

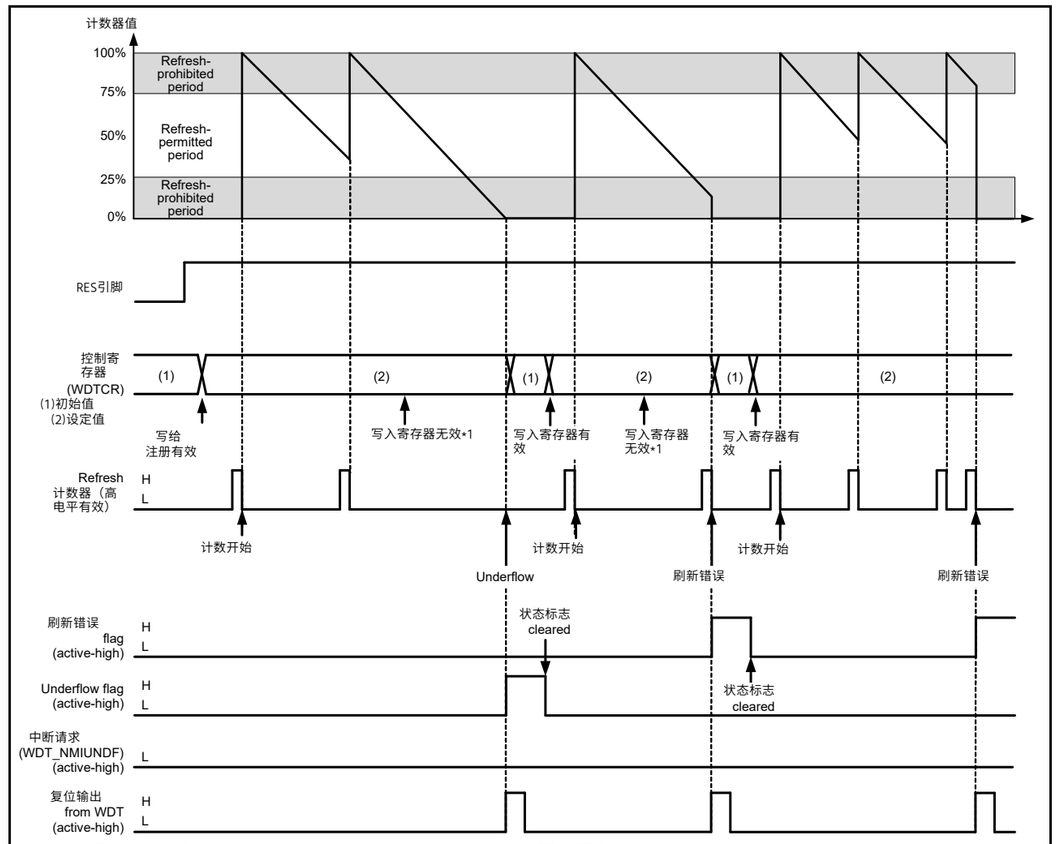
When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected. The WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

Within the reset state, the following values in the Option Function Select register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control during transition to Sleep mode.

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as counting continues.



注1.请参见26.3.2控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

Figure 26.3 寄存器启动模式下的操作示例

26.3.1.2 自动启动模式

当WDT启动模式选择位置（OFS0.WDTSTRT）中的选项功能选择寄存器0（OFS0）为0时，选择了自动启动模式。WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)被禁用，而OFS0寄存器中的设置被启用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下值在WDT寄存器中设置：

- 时钟分频比
- 窗口开始和结束位置
- 超时时间
- 复位输出或中断请求
- 转换到睡眠模式期间的计数器停止控制。

当复位状态解除时，递减计数器自动从WDT中设置的值开始递减计数
超时周期选择位(OFS0.WDTTOPS[1:0])。

此后，只要在可刷新期间刷新了计数器，则每次刷新计数器时都会重置计数器中的值，并继续递减计数。只要继续计数，WDT就不会输出复位信号。

However, if the down-counter underflows because refreshing of the down-counter is not possible due to a runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs a reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/ Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 26.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.WDTRSTIRQS = 0)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).

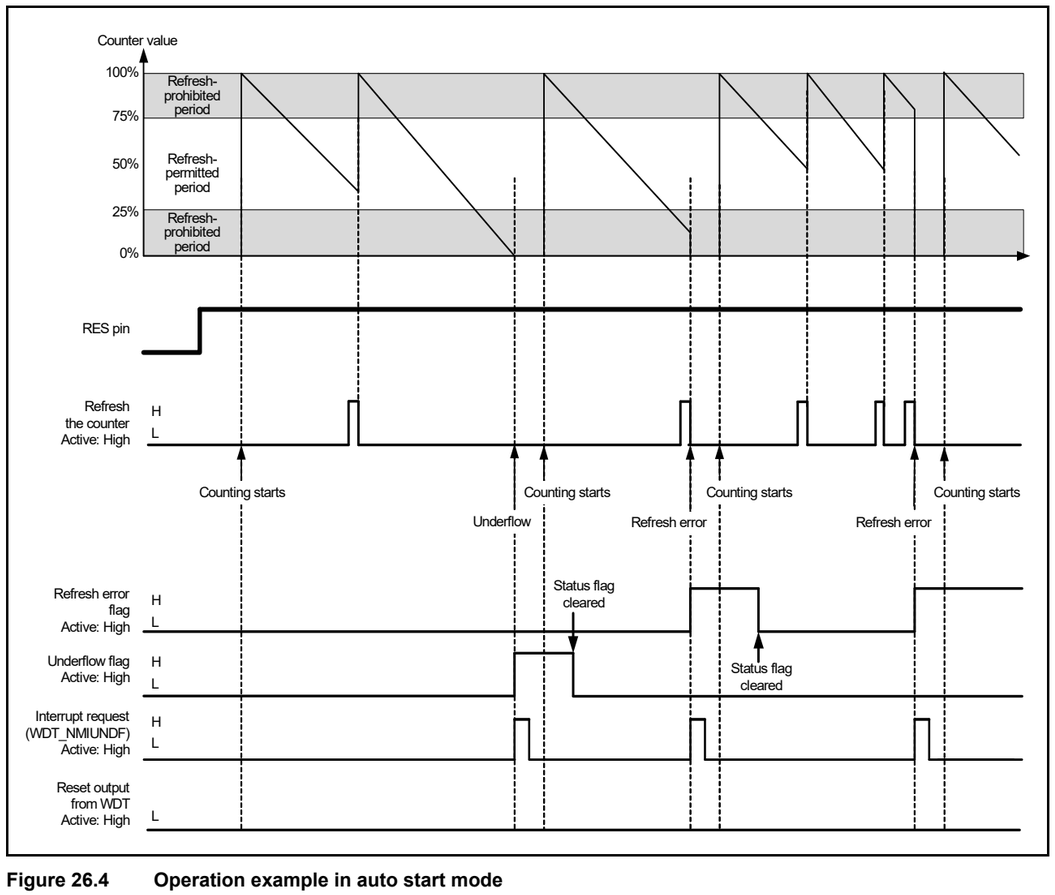


Figure 26.4 Operation example in auto start mode

26.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once between the release from the reset state and the first refresh operation.

After a refresh, (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR, the protection signal in the WDT

但是，如果由于程序失控而无法刷新递减计数器导致递减计数器下溢，或者如果由于刷新允许刷新时间之外的刷新而发生刷新错误，则WDT输出复位信号或不可屏蔽中断请求中断请求（WDT_NMIUNDF）。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期。超时时间的值在递减计数器中设置并重新开始计数。

可以在WDT复位中断请求选择位(OFS0.WDTRSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断　　允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图26.4显示了以下条件下的操作示例（不可屏蔽中断）：

- 自动启动模式（OFS0.WDTSTRT=0）
- 使能不可屏蔽中断请求输出(OFS0.WDTRSTIRQS=0)
- 窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)
- 窗口结束位置为25%(WDTCR.RPES[1:0]=10b)。

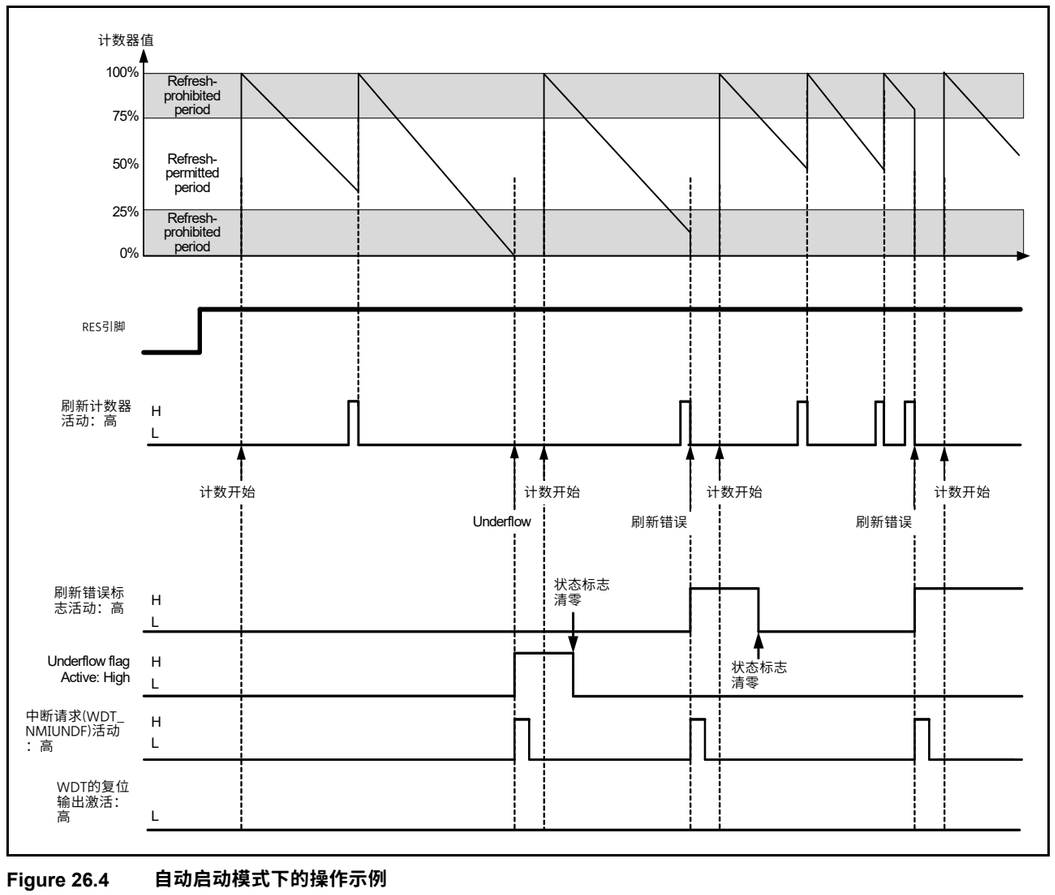


Figure 26.4 自动启动模式下的操作示例

26.3.2 控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入

写入WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)或WDT计数停止控制寄存器(WDTCSTPR)在从复位状态释放到第一次刷新操作之间是可能的。

在刷新（计数开始）或写入WDTCR、WDTRCR或WDTCSTPR后，WDT中的保护信号

becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR against subsequent write attempts. This protection is released by a reset source of the WDT. With other reset sources, the protection is not released.

Figure 26.5 shows control waveforms produced in response to writing to the WDTCR.

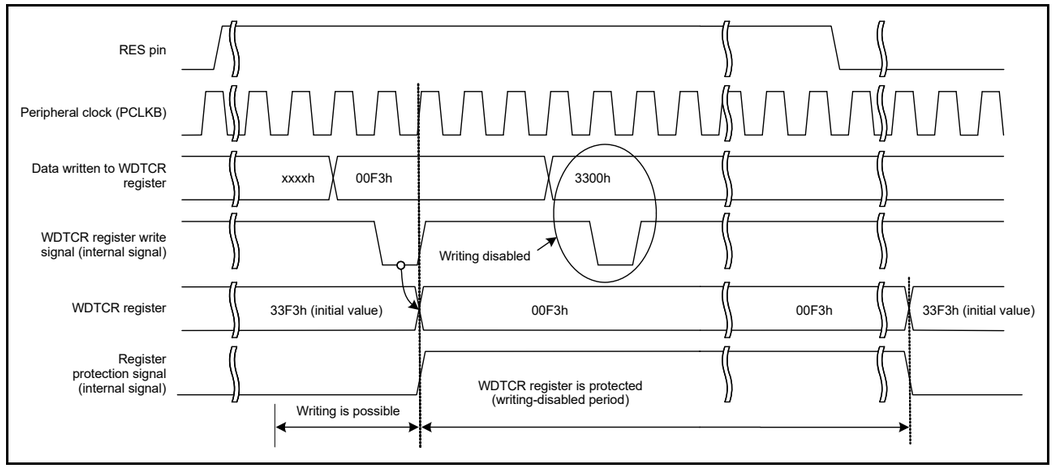


Figure 26.5 Control waveforms produced in response to writes to the WDTCR register

26.3.3 Refresh Operation

The down-counter is refreshed by writing the values 00h and FFh to the WDT Refresh Register (WDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes by writing 00h and FFh to the WDTRR Register.

Correct refreshing is also performed when a register other than WDTRR is accessed or when WDTRR is read between writing 00h and writing FFh to WDTRR.

Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by writing FFh. For this reason, correct refreshing is performed even when 00h is written outside the refresh-permitted period.

[Example write sequences that are valid when refreshing the counter]

- 00h → FFh
- 00h ((n - 1)-th time) → 00h (nth time) → FFh
- 00h → access to another register or read from WDTRR → FFh.

[Example write sequences that are invalid when refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h→ AAh (00h and a value other than FFh) → FFh.

After FFh is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing FFh to WDTRR 4 count cycles before the down-counter underflows.

Figure 26.6 shows the WDT refresh-operation waveforms when the clock division ratio = PCLKB/64.

变为1以保护WDTCR、WDTRCR和WDTCSTPR免受后续写入尝试。该保护由WDT的复位源解除。使用其他复位源时，不会解除保护。

图26.5显示了响应写入WDTCR产生的控制波形。

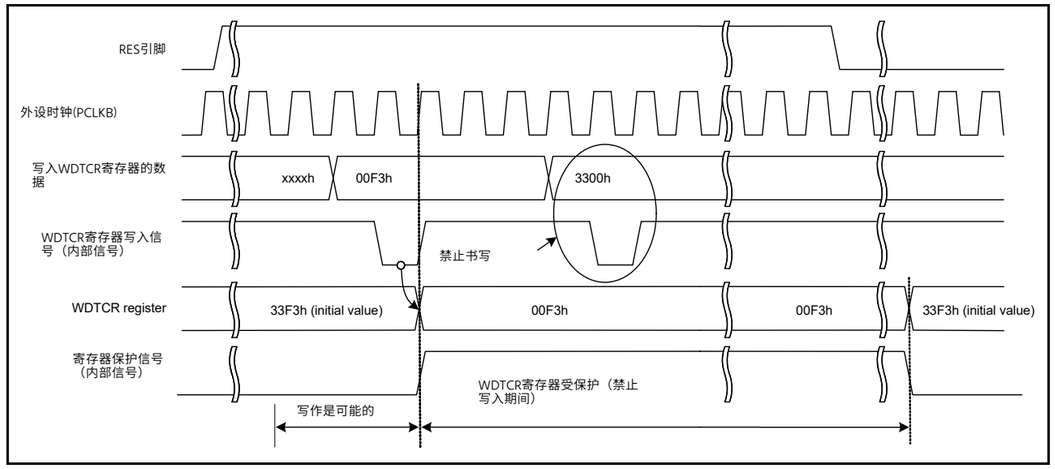


Figure 26.5 响应写入WDTCR寄存器而产生的控制波形

26.3.3 刷新操作

通过将值00h和FFh写入WDT刷新寄存器(WDTRR)来刷新递减计数器。如果在00h之后写入FFh以外的值，则不刷新递减计数器。如果写入无效值，则通过将00h和FFh写入WDTRR寄存器来恢复正确刷新。

当访问WDTRR以外的寄存器或在写入00h和将FFh写入WDTRR之间读取WDTRR时，也会执行正确刷新。

刷新计数器的写操作必须在允许刷新的时间内进行，这由写FFh决定。
因此，即使在刷新允许期间之外写入00h，也会执行正确的刷新。

[刷新计数器时有效的示例写入序列]

- 00h → FFh
- 00h ((n - 1)-th time) → 00h (nth time) → FFh
- 00h→访问另一个寄存器或从WDTRR→FFh读取。

[刷新计数器时无效的写入序列示例]

- 23h（00h以外的值）→FFh
- 00h→54h（FFh以外的值）
- 00h→AAh（00h和FFh以外的值）→FFh。

将FFh写入WDT刷新寄存器(WDTRR)后，刷新递减计数器最多需要4个信号周期进行计数。为满足此要求，请在递减计数器下溢之前的4个计数周期内将FFh写入WDTRR。

图26.6显示了时钟分频比=PCLKB64时的WDT刷新操作波形。

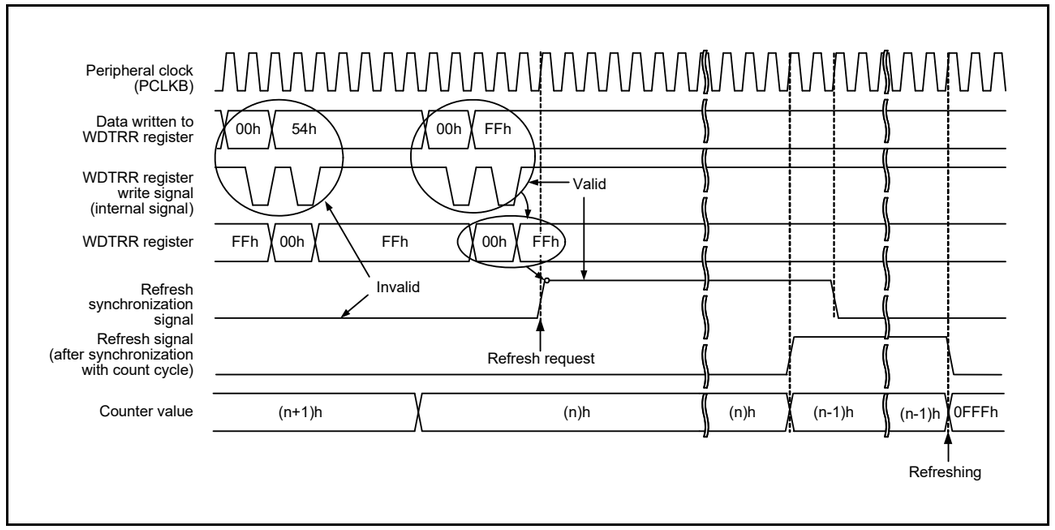


Figure 26.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b

26.3.4 Reset Output

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up and counting down starts again with a refresh. In auto start mode, counting down automatically starts after the reset state is released.

26.3.5 Interrupt Sources

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt (WDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 14, Interrupt Controller Unit (ICU).

Table 26.4 WDT interrupt sources

Name	Interrupt source	DTC activation
WDT_NMIUNDF	• Down-counter underflow • Refresh error	Not possible

26.3.6 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value.

Figure 26.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.

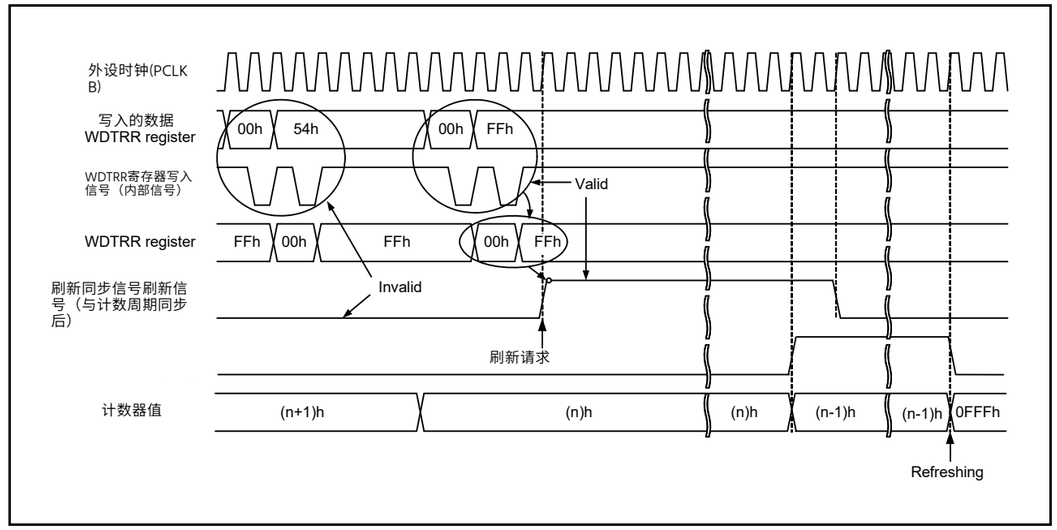


Figure 26.6 WDTCR.CKS[3:0]=0100b WDTCR.TOPS[1:0]=01b时的WDT刷新操作波形

26.3.4 复位输出

在寄存器启动模式下复位中断选择位(WDTRCR.RSTIRQS)设置为1或自动启动时选项功能选择寄存器0(OFS0)中的WDT复位中断请求选择位(OFS0.WDTRSTIRQS)设置为1模式下，当递减计数器出现下溢或发生刷新错误时，会输出1个周期计数的复位信号。

在寄存器启动模式下，递减计数器被初始化（所有位设置为0）并在输出复位信号后停止在该状态。复位状态解除并重新启动程序后，计数器设置并通过刷新重新开始倒计时。在自动启动模式下，复位状态解除后自动开始倒计时。

26.3.5 中断源

当重置中断选择位（wdtrcr.rstirqs）设置为0以寄存器启动模式设置为0，或者wdt重置中断请求选择bit（ofs0.wdtrstirqs）在选项函数selectselectoffertselectoptseoptse0（ofs0）中设置为0（ofs0）在自动启动中设置为0模式下，当计数器下溢或发生刷新错误时，会产生中断(WDT_NMIUNDF)信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

Table 26.4 WDT中断源

Name	中断源	DTC activation
WDT_NMIUNDF	递减计数器下溢 刷新错误	不可能

26.3.6 读取递减计数器值

WDT将计数器值存储在WDT状态的递减计数器值位(WDTSR.CNTVAL[13:0])中登记。检查这些位以获得计数器值。

图26.7显示了在时钟分频比为PCLKB64时读取WDT递减计数器值的处理。

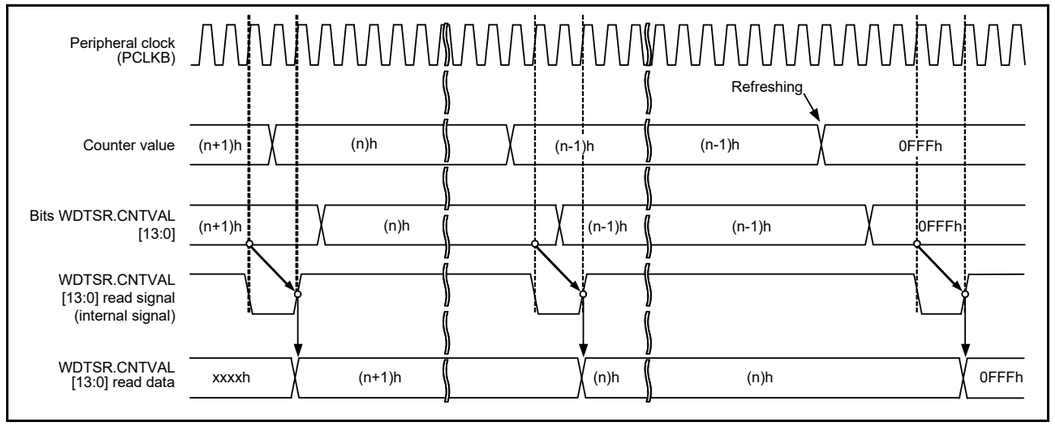


Figure 26.7 Read process for WDT down-counter value when WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b

26.3.7 Associations between Option Function Select Register 0 (OFS0) and WDT Registers

Table 26.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode and the registers used in register start mode. Do not change the OFS0 register setting during WDT operation. For details on the Option Function Select Register 0 (OFS0), see section 7.2.1, Option Function Select Register 0 (OFS0).

Table 26.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep-mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

26.4 Link Operation by ELC

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow and refresh error.

An event signal is output regardless of the setting of the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) in register start mode or auto start mode. An event signal can also be output when the next interrupt source is generated and while the Refresh Error Flag (WDTSR.REFEF) or Underflow Flag (WDTSR.UNDFF) is 1. For details, see section 19, Event Link Controller (ELC).

26.5 Usage Notes

26.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 25h to the ICU Event Link Setting Register n (IELSRn.IELS[7:0]) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1), or when enabling the event link operation (ELSRm.ELS[7:0] = 25h).

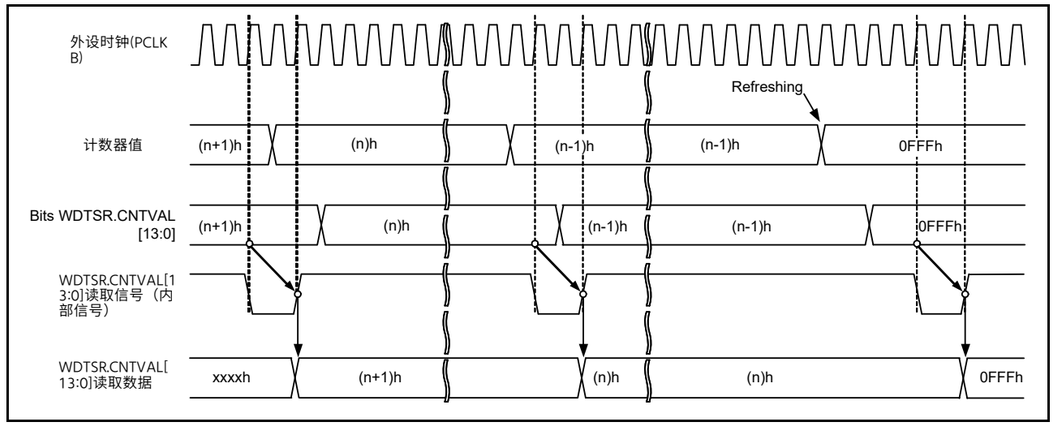


Figure 26.7 WDTCR.CKS[3:0]=0100b WDTCR.TOPS[1:0]=01b时WDT递减计数器值的读取过程

26.3.7 选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联

表26.5列出了用于自动启动模式的选项功能选择寄存器0(OFS0)和用于寄存器启动模式的寄存器之间的关联。请勿在WDT操作期间更改OFS0寄存器设置。有关选项功能选择寄存器0(OFS0)的详细信息，请参见第7.2.1节，选项功能选择寄存器0(OFS0)。

Table 26.5 选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联

控制目标	Function	OFS0寄存器（在自动启动模式下启用）OFS0.WDTSTRT=0	WDT寄存器（在寄存器启动模式下启用）OFS0.WDTSTRT=1
Down-counter	超时时间选择	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	时钟分频比选择	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	窗口起始位置选择	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	窗口结束位置选择	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
复位输出或中断请求输出	复位输出或中断请求输出选择	OFS0.WDTRSTIRQS	WDTCR.RSTIRQS
计数停止	睡眠模式计数停止控制	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

26.4 ELC的链接操作

当ELC将中断请求信号用作事件信号时，WDT能够对先前指定的模块进行链接操作。事件信号由计数器下溢和刷新错误输出。

在寄存器启动模式或自动启动模式下，无论复位中断请求选择位(WDTRCR.RSTIRQS)的设置如何，都会输出事件信号。当产生下一个中断源并且刷新错误标志(WDTSR.REFEF)或下溢标志(WDTSR.UNDFF)为1时，也可以输出事件信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

26.5 使用说明

26.5.1 ICU事件链接设置寄存器n(IELSRn)设置

当启用WDT复位断言（OFS0.WDTRSTIRQS=1或WDTRCR.RSTIRQS=1）或启用事件链接操作（ELSRm.ELS[7:0]=25h)。

27. Independent Watchdog Timer (IWDT)

27.1 Overview

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt on a timer underflow. Because the timer operates using an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a failsafe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The IWDT functions differ from those of the WDT in the following respects:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by the PCLKB)
- IWDT does not support the register start mode
- When transitioning to low power mode, the OFS0.IWDTSTPCTL bit can be used to select whether to stop the counter or not.

Table 27.1 lists the IWDT specifications and Figure 27.1 shows a block diagram.

Table 27.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	Counting automatically starts after a reset
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the IWDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto start mode	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the Independent Watchdog Timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the Independent Watchdog Timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the Independent Watchdog Timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit).

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

To use the IWDT, supply the IWDT-dedicated clock (IWDTCLK). The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

27. 独立看门狗定时器(IWDT)

27.1 Overview

独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或在定时器下溢时产生不可屏蔽中断中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障保护机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。

IWDT的功能与WDT的功能有以下不同：

- 分频的IWDT专用时钟（IWDTCLK）用作计数源（不受PCLKB影响）
- IWDT不支持寄存器启动模式
- 当转换到低功耗模式时，可以使用OFS0.IWDTSTPCTL位来选择是否停止计数器。

表27.1列出了IWDT规范，图27.1显示了框图。

Table 27.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
时钟分频比	除以1、16、32、64、128或256
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	复位后自动开始计数
停止计数器的条件	复位（递减计数器和其他寄存器返回其初始值） 计数器下溢或产生刷新错误（计数自动重新开始）。
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
重置输出源	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）。
Non-maskable interrupt/interrupt sources	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）。
读取计数器值	递减计数器的值可以通过IWDTSR寄存器读取
事件链接功能（输出）	递减计数器下溢事件输出 刷新错误事件输出。
输出信号（内部信号）	复位输出 中断请求输出 睡眠模式计数停止控制输出。
自动启动模式	选择复位后的时钟分频比（OFS0.IWDTCKS[3:0]位） 选择独立看门狗定时器的超时周期（OFS0.IWDTCKS[1:0]位） 选择窗口起始位置独立看门狗定时器（OFS0.IWDTRPSS[1:0]位） 在独立看门狗定时器中选择窗口结束位置（OFS0.IWDTRPES[1:0]位） 选择复位输出或中断请求输出（OFS0.IWDTRSTIRQS位） 在转换到睡眠模式、软件待机模式或贪睡模式时选择减计数停止功能（OFS0.IWDTSTPCTL位）。

Note 1. 满足外围模块时钟（PCLKB）的频率 4×（分频后的计数时钟源的频率）。

要使用IWDT，请提供IWDT专用时钟(IWDTCLK)。总线接口和寄存器使用PCLKB运行，14位计数器和控制电路使用IWDTCLK运行。

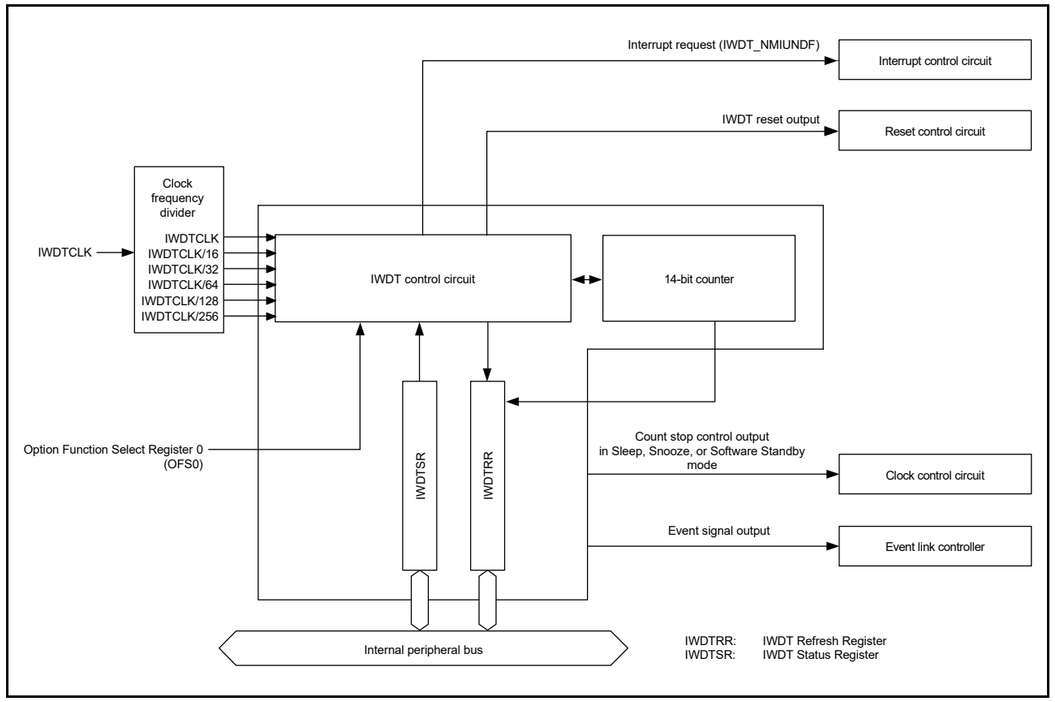


Figure 27.1 IWDT block diagram

27.2 Register Descriptions

27.2.1 IWDT Refresh Register (IWDTRR)

Address(es): IWDT.IWDTRR 4004 4400h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The counter is refreshed by writing 00h and then writing FFh to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 00h and then writing FFh to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected with the IWDT timeout period select bits (OFS0.IWDTTOPS[1:0]) in the Option Function Select Register 0 (OFS0).

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details of the refresh operation, see section 27.3.2, Refresh Operation.

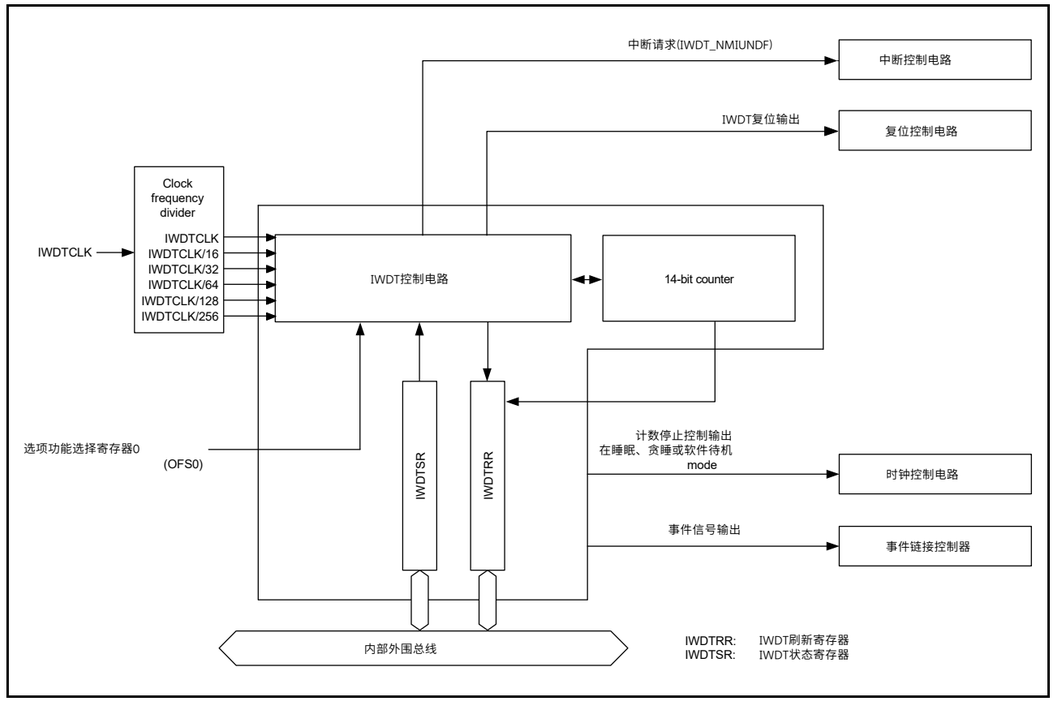


Figure 27.1 IWDT框图

27.2 注册说明

27.2.1 IWDT刷新寄存器(IWDTRR)

Address(es): IWDT.IWDTRR 4004 4400h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	通过写入00h然后将FFh写入该寄存器来刷新计数器	R/W

IWDTRR寄存器刷新IWDT的递减计数器。IWDT的递减计数器通过写入00h进行刷新，然后在允许刷新期间将FFh写入IWDTRR（刷新操作）。递减计数器刷新后，它从选项功能选择寄存器0(OFS0)中的IWDT超时周期选择位(OFS0.IWDTTOPS[1:0])选择的值开始递减计数。

写入00h时，读取值为00h。写入00h以外的值时，读取值为FFh。有关刷新操作的详细信息，请参阅第27.3.2节，刷新操作。

27.2.2 IWDT Status Register (IWDTSR)

Address(es): IWDT.IWDTSR 4004 4404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: Underflow not occurred 1: Underflow occurred.	R/(W)*1
b15	REFEF	Refresh Error Flag	0: Refresh error not occurred 1: Refresh error occurred.	R/(W)*1

Note 1. Only 0 can be written to clear the flag.

CNTVAL[13:0] bits (Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of the flag is ignored for (N+2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N+2) IWDTCLK cycles after a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

27.2.2 IWDT状态寄存器(IWDTSR)

Address(es): IWDT.IWDTSR 4004 4404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	CNTVAL[13:0]	计数器值	递减计数器计数的值	R
b14	UNDFF	Underflow Flag	0：未发生下溢1：发生下溢。	R/(W)*1
b15	REFEF	刷新错误标志	0：未发生刷新错误1：发生刷新错误。	R/(W)*1

Note 1. 只能写入0来清除标志。

CNTVAL[13:0]位（计数器值）

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认递减计数器中是否发生下溢。值1表示递减计数器下溢。将0写入UNDFF标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在下溢后的(N+2)个IWDTCLK周期内忽略标志的清除。N在IWDTCKS[3:0]位中指定如下：

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

REFEF标志（刷新错误标志）

读取REFEF标志以确认是否发生刷新错误。值1表示发生了刷新错误。
将0写入REFEF标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在刷新错误后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

27.2.3 Option Function Select Register 0 (OFS0)

For information on the Option Function Select Register 0 (OFS0), see section 7.2.1, Option Function Select Register 0 (OFS0).

IWDTTOPS[1:0] bits (IWDT Timeout Period Selects)

The IWDTTOPS[1:0] bits select the timeout period, that is, the period until the down-counter underflows from 128, 512, 1024, or 2048 cycles, taking the divided clock specified by the IWDTCKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 27.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 27.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combination with the IWDTTOPS[1:0] bit setting, a count period between 128 and 524288 cycles of the IWDTCLK clock can be selected for the IWDT.

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. The selected window end position should be a

27.2.3 选项功能选择寄存器0(OFS0)

有关选项功能选择寄存器0(OFS0)的信息，请参阅第7.2.1节，选项功能选择寄存器0(OFS0)。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位选择超时周期，即从128、512、1024或2048个周期到递减计数器下溢的周期，取IWDTCKS[3:0]位指定的分频时钟为1个周期。

向下计数器刷新后，IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定了在计数器下溢之前的IWDTCLK周期数。

表27.2列出了IWDTCKS[3:0]和IWDTTOPS[1:0]位设置、超时周期和IWDTCLK周期数之间的关系。

Table 27.2 超时时间设置

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		时钟分频比	超时时间（周期数）	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于递减计数器的时钟分频比。分频比可以从IWDT专用时钟(IWDTCLK)除以1、16、32、64、128和256中选择。结合IWDTTOPS[1:0]位设置，计数周期在128和524288个周期之间可以为IWDT选择IWDTCLK时钟。

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。选定的窗口结束位置应该是

value smaller than the window start position. If the window end position is greater than the window start position, only the window start position setting is enabled.

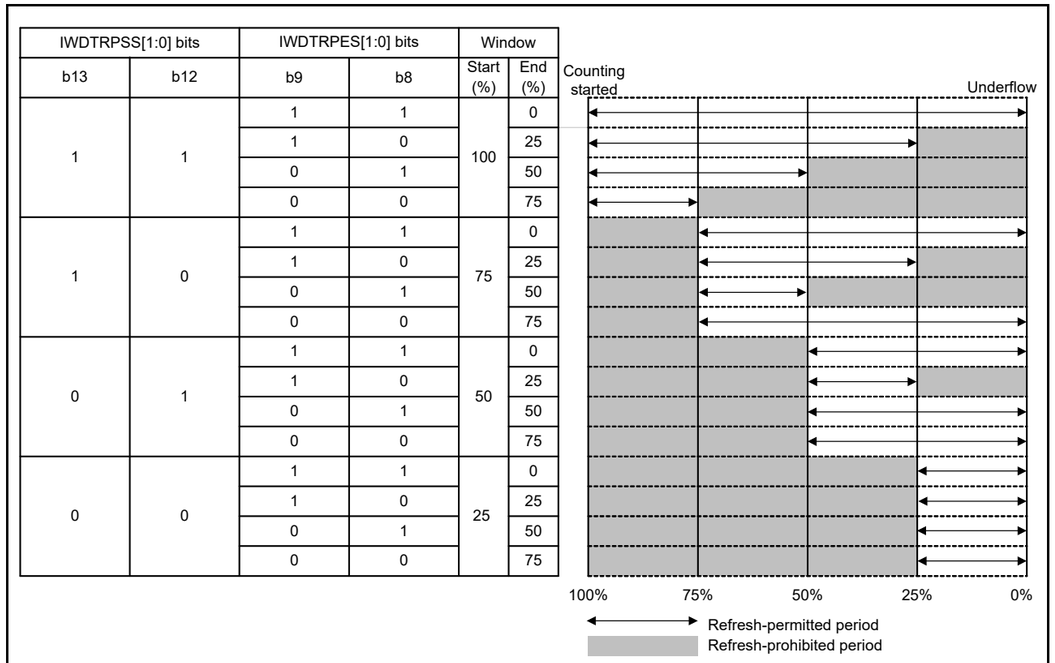
IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. The window start position should be a value greater than the value for the window end position. If the window start position is smaller than or equal to the window end position, the window end position is set to 0%.

Table 27.3 lists the counter values for the window start and end positions and Figure 27.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 27.3 Relationship between timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2048	07FFh	07FFh	05FFh	03FFh	01FFh



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 27.2 IWDTRPSS[1:0] and [IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurred. The value 1 indicates that reset output is selected. The value 0 indicates that a non-maskable interrupt/interrupt is selected.

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether the stop counting on transition to Sleep, Snooze, or Software Standby mode.

值小于窗口起始位置。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

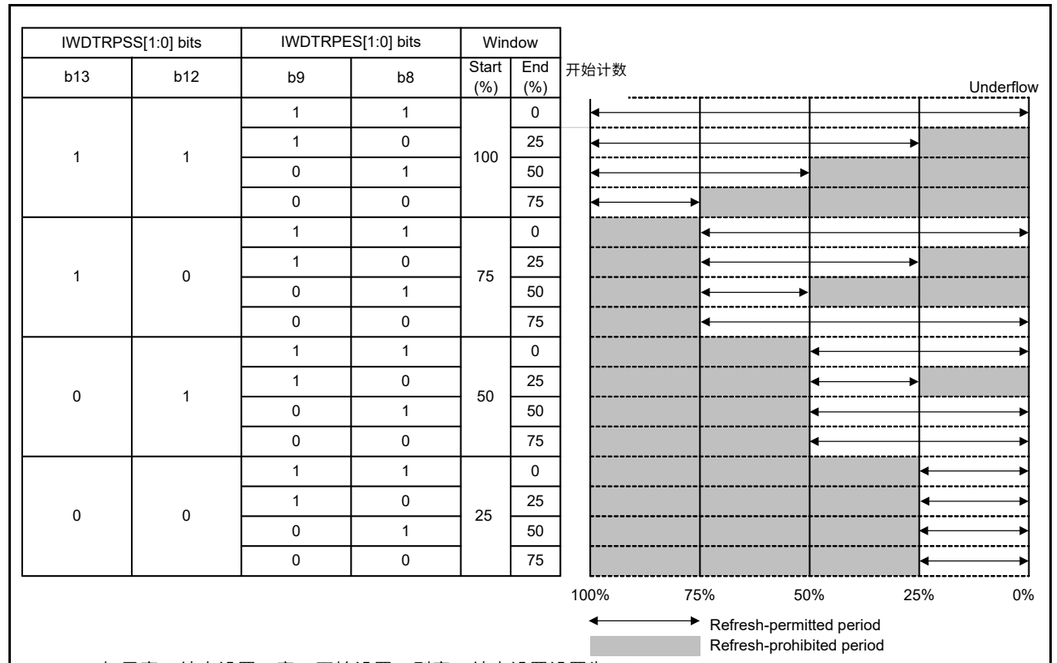
IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定指示刷新允许周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。窗口开始位置的值应大于窗口结束位置的值。如果窗口开始位置小于或等于窗口结束位置，则窗口结束位置设置为0%。

表27.3列出了窗口开始和结束位置的计数器值，图27.2显示了在IWDTRPSS[1:0]、IWDTRPES[1:0]和IWDTTOPS[1:0]位中设置的允许刷新周期。

Table 27.3 超时时间与窗口开始和结束计数器值之间的关系

IWDTTOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
b1	b0	Cycles	计数器值	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2048	07FFh	07FFh	05FFh	03FFh	01FFh



Note: 如果窗口结束设置 窗口开始设置，则窗口结束设置设置为0%。

Figure 27.2 IWDTRPSS[1:0]和[IWDTRPES[1:0]位设置和允许刷新周期

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位指定发生下溢或刷新错误时的行为。值1表示选择了复位输出。值0表示选择了不可屏蔽的中断中断。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位选择在转换到休眠、贪睡或软件待机模式时停止计数。

27.3 Operation

27.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise IWDT is disabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control at transitions to low power mode.

When the reset state is released, the counter automatically starts counting down from the value selected by the IWDT timeout period select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashed or because a refresh error occurred when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, and restarts the count. The reset output or interrupt request can be selected with the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected with the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 27.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.IWDTRSTIRQS = 0)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

27.3 Operation

27.3.1 自动启动模式

当IWDT启动模式选择位置（OFS0.IWDTSTRT）选项函数中选择寄存器0为0时，选择了自动启动模式，否则IWDT将被禁用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
IWDT registers:

- 时钟分频比
- 窗口开始和结束位置
- 超时时间
- 复位输出或中断请求
- 转换到低功耗模式时的计数器停止控制。

当复位状态被释放时，计数器自动从IWDT超时周期选择位(OFS0.IWDTTOPS[1:0])选择的值开始递减计数。

之后，只要程序继续正常运行，并且在允许刷新的时间内刷新计数器，每次刷新计数器时，计数器中的值都会被复位，继续倒计时。只要此过程继续，IWDT就不会输出复位信号。但是，如果由于程序崩溃或尝试刷新允许刷新期间之外的刷新错误而导致计数器下溢，则IWDT将置位复位信号或不可屏蔽中断请求中断请求(IWDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期，重新开始计数。可以通过IWDT复位中断请求选择位(OFS0.IWDTRSTIRQS)选择复位输出或中断请求。可以使用IWDT下溢刷新错误中断　　允许位(NMIER.IWDTEN)选择不可屏蔽的中断请求或中断请求。

图27.3显示了以下条件下的操作示例：

- 自动启动模式（OFS0.IWDTSTRT=0）
- 使能不可屏蔽中断请求输出(OFS0.IWDTRSTIRQS=0)
- 窗口起始位置为75%(OFS0.IWDTRPSS[1:0]=10b)
- 窗口结束位置为25%(OFS0.IWDTRPES[1:0]=10b)。

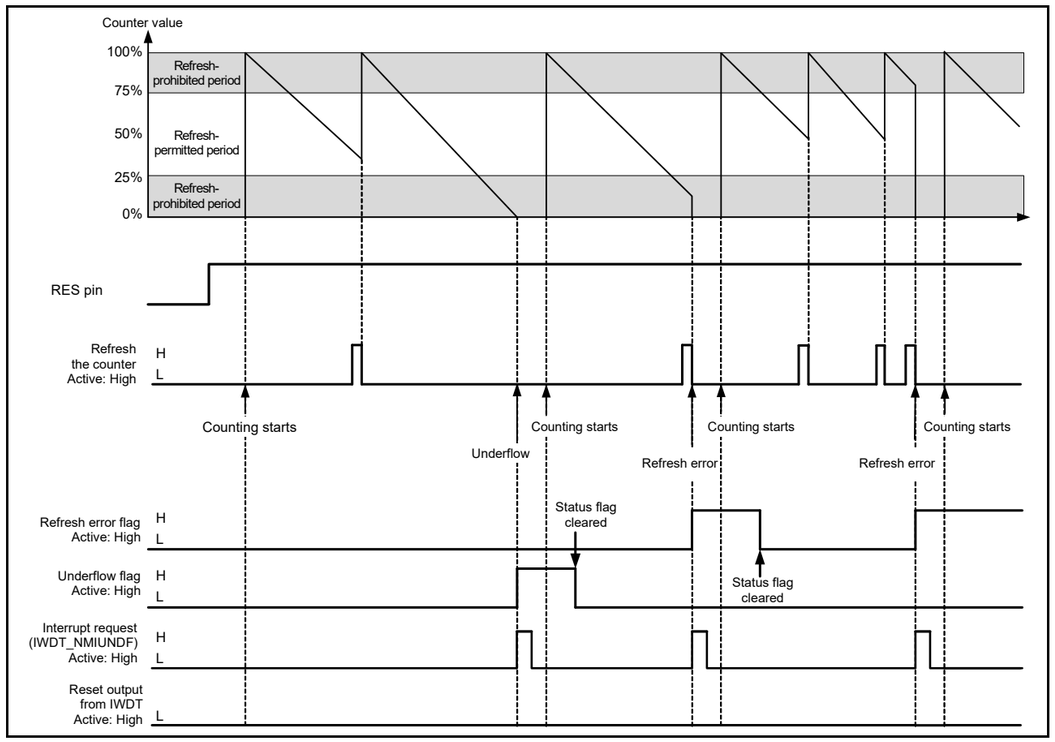


Figure 27.3 Operation example in auto start mode

27.3.2 Refresh Operation

The down-counter is refreshed by writing the values 00h and FFh to the IWDT Refresh Register (IWDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 00h and FFh to the IWDTRR.

When writes are made in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied. Writing 00h ($(n-1)^{th}$ time) → 00h (n^{th} time) → FFh is valid, and the refresh is performed correctly. Even when the first value written before 00h is not 00h, correct refreshing is performed as long as the operation contains the write sequence of 00h → FFh.

Correct refreshing is also performed when a register other than IWDTRR is accessed or IWDTRR is read between writing 00h and writing FFh to IWDTRR.

[Example write sequences that are valid to refresh the counter]

- 00h → FFh
- 00h (n–1th time) → 00h (nth time) → FFh
- 00h → access to another register or read from IWDTRR → FFh.

[Example write sequences that are not valid to refresh the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h → AAh (00h and a value other than FFh) → FFh.

When 00h is written to IWDTRR outside the refresh-permitted period, if FFh is written to IWDTRR in the refresh-permitted period, the writing sequence is valid and refreshing completes.

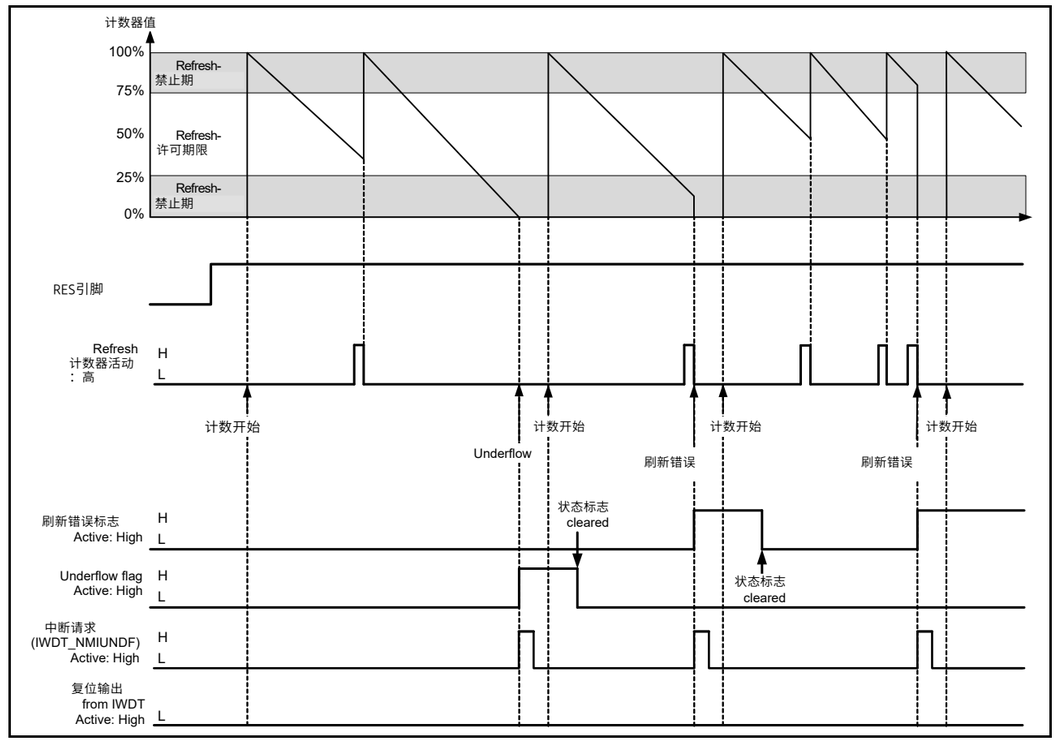


Figure 27.3 自动启动模式下的操作示例

27.3.2 刷新操作

通过将值00h和FFh写入IWDT刷新寄存器(IWDTRR)来刷新递减计数器。如果在00h之后写入FFh以外的值，则不刷新递减计数器。如果写入了无效值，则在向IWDTRR写入00h和FFh时恢复正确刷新。

当以00h（第一次）→00h（第二次）的顺序进行写入时，如果在此之后写入FFh，则满足写入顺序00h→FFh。写入00h（第（n-1）次）→00h（第n次）→FFh有效，刷新正确。即使在00h之前写入的第一个值不是00h，只要操作包含00h→FFh的写入序列，就会执行正确的刷新。

当访问IWDTRR以外的寄存器或在写入00h和将FFh写入IWDTRR之间读取IWDTRR时，也会执行正确刷新。

[对刷新计数器有效的示例写入序列]

- 00h → FFh
- 00h (n–1th time) → 00h (nth time) → FFh
- 00h→访问另一个寄存器或从IWDTRR→FFh读取。

[对刷新计数器无效的示例写入序列]

- 23h（00h以外的值）→FFh
- 00h→54h（FFh以外的值）
- 00h→AAh(00h和FFh以外的值)→FFh。

当00h在刷新允许周期外写入IWDTRR时，如果在刷新允许周期内将FFh写入IWDTRR，则写入序列有效，刷新完成。

After FFh is written to the IWDTRR register, refreshing the counter requires up to 4 cycles of the signal for counting (the IWDT-dedicated clock frequency division ratio select bits (OFS0.IWDTCKS[3:0]) determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 cycle for counting). Therefore, writing FFh to the IWDTRR must be completed 4 count cycles before the end of the refresh-permitted period or a counter underflow. The value of the counter can be checked with the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 1FFFh, even if 00h is written to IWDTRR before 1FFFh is reached (2002h, for example), refreshing occurs if FFh is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 1FFFh
- When the window end position is set to 1FFFh, refreshing occurs if 2003h (4 count cycles before 1FFFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR
- When the refresh-permitted period continues until count 0000h, refreshing can be performed immediately before an underflow. In this case, if 0003h (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR, no underflow occurs and refreshing is performed.

Figure 27.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

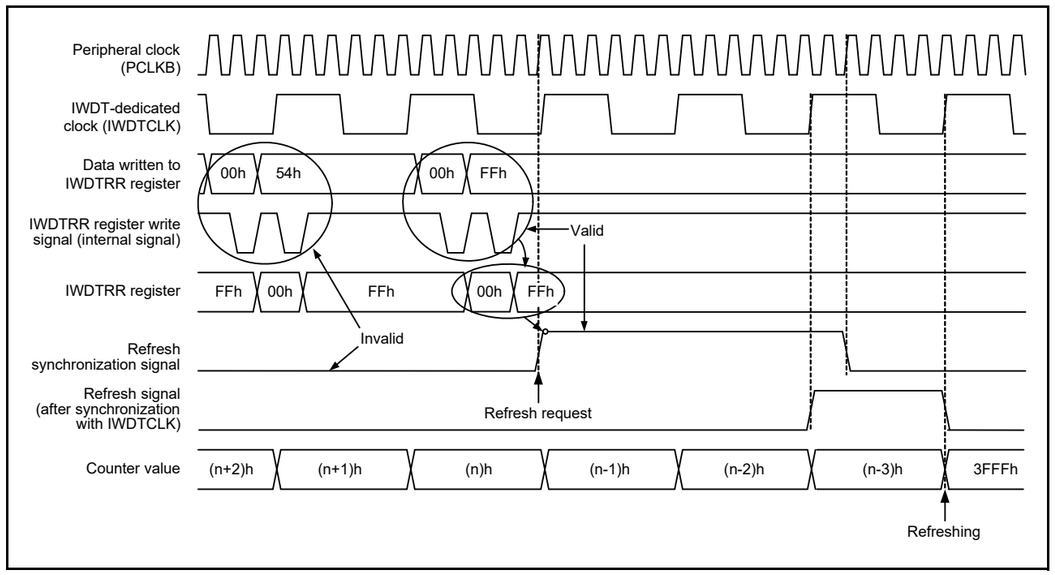


Figure 27.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

27.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output or the source of the interrupt request from the IWDT. Therefore, after a release from the reset state or interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the reset or interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written. After 0 is written to each flag, up to 3 IWDTCLK cycles and 2 PCLKB cycles are required before the value is reflected.

将FFh写入IWDTRR寄存器后，刷新计数器最多需要4个计数信号周期（
IWDT专用时钟分频比选择位(OFS0.IWDTCKS[3:0])决定IWDT专用时钟(IWDTCLK)的多少个周期构成1个计数周期。因此，将FFh写入IWDTRR必须在刷新允许周期结束或计数器下溢之前的4个计数周期内完成。可以使用计数器位(IWDTSR.CNTVAL[13:0])检查计数器的值。

[Example refreshing timings]

- 当窗口起始位置设置为1FFFh时，即使在到达1FFFh之前将00h写入IWDTRR（例如2002h），如果在IWDTSR.CNTVAL[13:0]位的值之后将FFh写入IWDTRR，也会发生刷新达到1FFFh
- 当窗口结束位置设置为1FFFh时，如果在将00h→FFh写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取2003h（1FFFh之前的4个计数周期）或更大的值，则会发生刷新
- 当刷新允许周期持续到计数0000h时，可以在下溢之前立即执行刷新。在这种情况下，如果在将00h→FFh写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0003h（下溢前4个计数周期）或更大的值，则不会发生下溢并执行刷新。

图27.4显示了当PCLKB>IWDTCLK并且时钟分频比为时的IWDT刷新操作波形
IWDTCLK.

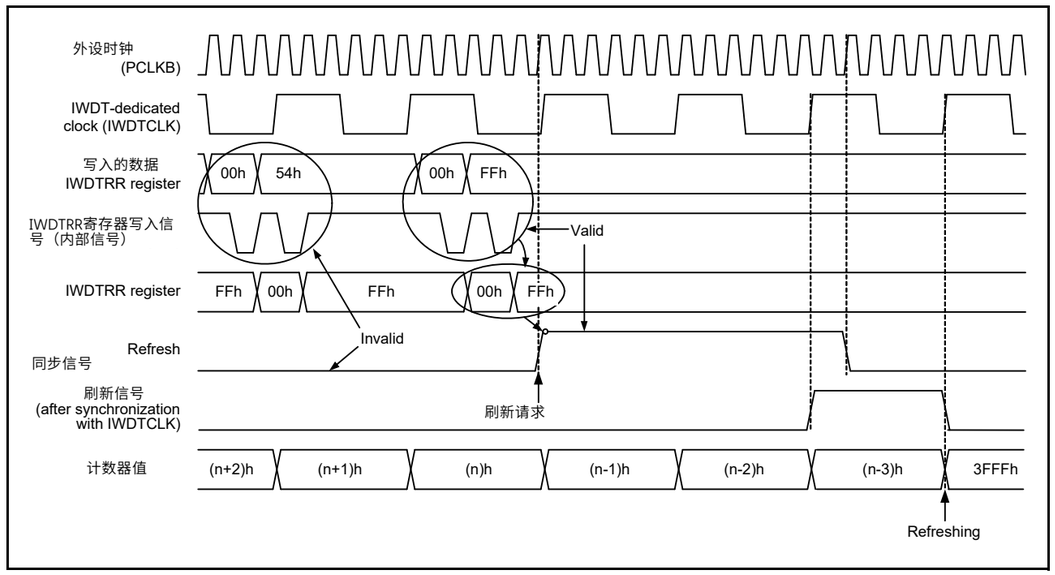


Figure 27.4 OFS0.IWDTCKS[3:0]=0000b OFS0.IWDTCKS[1:0]=11b时的IWDT刷新操作波形

27.3.3 状态标志

刷新错误(IWDTSR.REFEF)和下溢(IWDTSR.UNDFF)标志保留复位信号输出源或来自IWDT的中断请求源。因此，从复位状态释放或产生中断请求后，读取IWDTSR.REFEF和UNDFF标志以检查复位或中断源。对于每个标志，写入0清除该位，写入1无效。

保持状态标志不变不会影响操作。如果在IWDT发出下一次复位或中断请求时未清除标志，则清除较早的复位或中断源并写入新的复位或中断源。将0写入每个标志后，最多需要3个IWDTCLK周期和2个PCLKB周期才能反映该值。

27.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the counter or a refresh error occurs. Counting down automatically starts after the reset output.

27.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt (IWDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 14, Interrupt Controller Unit (ICU).

Table 27.4 IWDT interrupt source

Name	Interrupt source	DTC activation
IWDT_NMIUNDF	Down-counter underflow Refresh error	Not possible

27.3.6 Reading the Down-counter Value

As the counter in IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT status register. Therefore, the counter value can be checked indirectly through the IWDTSR.CNTVAL[13:0] bits.

Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 27.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

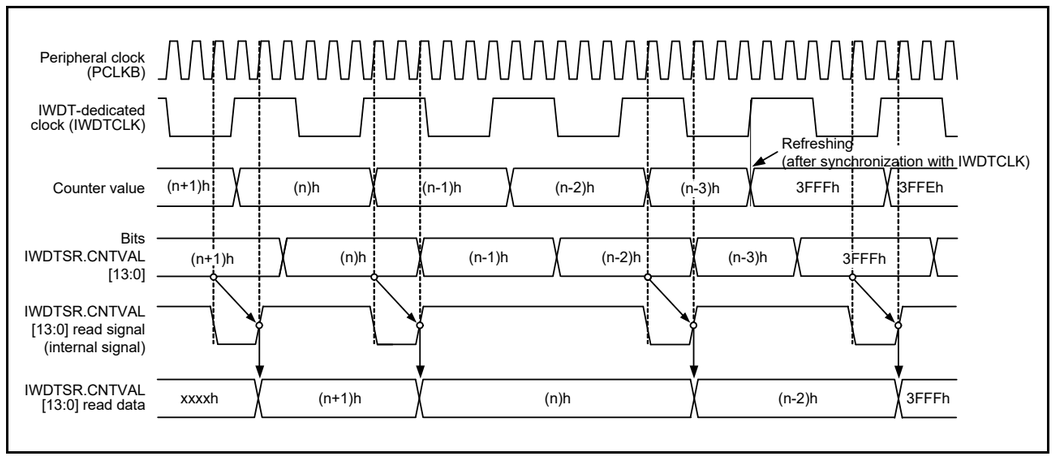


Figure 27.5 Processing for reading IWDT counter value (OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b)

27.4 Link Operation by ELC

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the event link controller (ELC). The event signal is output by the counter underflow and refresh error.

An event signal is output regardless of the setting of the OFS0.WDTRSTIRQS bit. An event signal can also be output at generation of the next interrupt source while the Refresh Error flag (IWDTSR.REFEF) or Underflow flag (IWDTSR.UNDFF) is 1. For details, see section 19, Event Link Controller (ELC).

27.3.4 复位输出

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）的位置为1时，当计数器中的下流或刷新错误发生时，将输出一个重置信号。复位输出后自动开始倒计时。

27.3.5 中断源

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）的位置为0时，当计数器中的下流或刷新错误发生时，会生成中断（IWDT_NMIUNDF）信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

Table 27.4 IWDT中断源

Name	中断源	DTC activation
IWDT_NMIUNDF	Down-counter underflow 刷新错误	不可能

27.3.6 读取递减计数器值

作为IWDT专用时钟(IWDTCLK)中的计数器，无法直接读取计数器值。IWDT将计数器值与外设时钟(PCLKB)同步，并将其存储在IWDT状态寄存器的递减计数器值位(IWDTSR.CNTVAL[13:0])中。因此，可以通过IWDTSR.CNTVAL[13:0]位间接检查计数器值。

读取计数器值需要多个PCLKB时钟周期（最多4个时钟周期），读取的计数器值可能与实际计数器值相差一个计数值。

图27.5显示了当PCLKB>IWDTCLK并且时钟分频比为IWDTCLK时读取IWDT计数器值的处理。

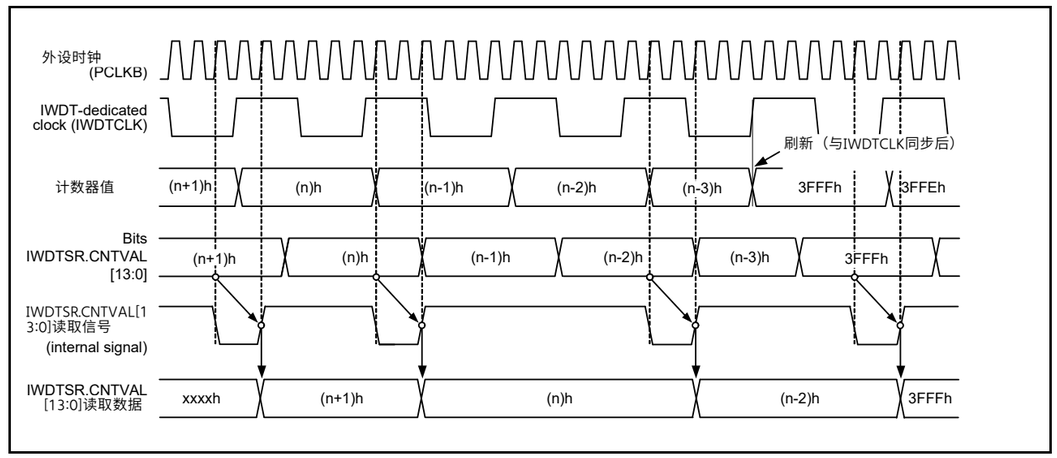


Figure 27.5 读取IWDT计数器值的处理(OFS0.IWDTCKS[3:0]=0000b OFS0.IWDTTOPS[1:0]=11b)

27.4 ELC的链接操作

当中断请求信号被事件链接控制器(ELC)用作事件信号时，IWDT能够对指定模块进行链接操作。事件信号由计数器下溢和刷新错误输出。

无论OFS0.WDTRSTIRQS位的设置如何，都会输出事件信号。当刷新错误标志(IWDTSR.REFEF)或下溢标志(IWDTSR.UNDFF)为1时，也可以在生成下一个中断源时输出事件信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

27.5 Usage Notes

27.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

27.5.2 Clock Division Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

27.5 使用说明

27.5.1 刷新操作

在配置刷新时间时，考虑到给定PCLKB精度和误差范围的变化
IWDTCLK。设置确保可以刷新的值。

27.5.2 时钟分频比设置

满足外围模块时钟（PCLKB）的频率 4 （分频后的计数时钟源的频率）。

28. USB 2.0 Full-Speed Module (USBFS)

28.1 Overview

The MCU provides a USB 2.0 Full-Speed module (USBFS) that operates as a host or device controller compliant with the Universal Serial Bus (USB) specification revision 2.0. The host controller supports USB 2.0 full-speed and low-speed transfers, and the device controller supports USB 2.0 full-speed transfers. The USBFS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification.

The USBFS has FIFO buffer for data transfers, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or the communication requirements for your system.

The MCU supports revision 1.2 of the Battery Charging specification.

Table 28.1 lists the USBFS specifications, Figure 28.1 shows a block diagram, and Table 28.2 lists the I/O pins.

Table 28.1 USBFS specifications

Parameter	Specifications
Features	• USB Device Controller (UDC) and USB 2.0 transceiver supporting host controller, device controller • Host and device controller can be switched by software • Self-power or bus power mode can be selected • Revision 1.2 of Battery Charging specification is supported
	Host controller features: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers.
	Device controller features: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • Control transfer stage control function • Auto response function for SET_ADDRESS request • SOF interpolation.
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer.
Pipe configuration	• FIFO buffer for USB communication • Up to 10 pipes can be selected, including the default control pipe • Pipes 1 to 9 can be assigned any endpoint number.
	Transfer conditions that can be set for each pipe: • Pipe 0: Control transfer with 64-byte single buffer • Pipes 1 and 2: Bulk transfer with 64-byte double buffer 256-byte double buffer for isochronous transfer • Pipes 3 to 5: Bulk transfer with 64-byte double buffer • Pipes 6 to 9: Interrupt transfer with 64-byte single buffer.
Others	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Automatic clearing of the FIFO buffer after the data for the pipe specified in the DnFIFO port (n = 0, 1) is read (DCLRM) • NAK setting function for response PID generated on transfer end (SHTNAK) • On-chip pull-up and pull-down resistors for USB_DP/USB_DM • HOCO clock that can be used as USB clock.
Module-stop function	Module-stop state can be set to reduce power consumption

28. USB2.0全速模块(USBFS)

28.1 Overview

MCU提供USB2.0全速模块(USBFS)，可作为主机或设备控制器运行，符合通用串行总线(USB)规范修订版2.0。主机控制器支持USB2.0全速和低速传输，设备控制器支持USB2.0全速传输。USBFS有一个内部USB收发器，支持USB2.0规范中定义的所有传输类型。

USBFS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或系统的通信要求，可以将任何端点编号分配给管道1到9。

MCU支持电池充电规范的1.2版。

表28.1列出了USBFS规范，图28.1显示了框图，表28.2列出了IO引脚。

Table 28.1 USBFS specifications

Parameter	Specifications
Features	USB设备控制器(UDC)和USB2.0收发器支持主机控制器、设备控制器 主机和设备控制器可通过软件切换 可选择自供电或总线供电模式 支持电池充电规范1.2版
	主机控制器特性： 全速传输(12Mbps)和低速传输(1.5Mbps) SOF和数据包传输的自动调度 同步和中断传输的可编程间隔。
	设备控制器特性： 全速传输(12Mbps)和低速传输(1.5Mbps) 控制传输阶段控制功能 设备状态控制功能 SET_ADDRESS请求的自动响应功能 SOF插值。
通讯数据传输类型	控制传输 批量传输 中断传输 同步传输。
管道配置	用于USB通信的FIFO缓冲区 最多可以选择10个管道，包括默认控制管道 可以为管道1到9分配任何端点编号。
	可为每个管道设置的传输条件： 管道0：使用64字节单缓冲区的控制传输 管道1和2：使用64字节双缓冲区 的批量传输用于同步传输的256字节双缓冲区 管道3到5：使用64字节双缓冲区 的批量传输 管道6到9：使用64字节单缓冲区的中断传输。
Others	使用事务计数的接收结束功能 更改BRDY中断事件通知时序(BFRE)的功能 读取DnFIFO端口(n=0 1)中指定管道的数据后自动清除FIFO缓冲区(DCLRM) NAK设置功能，用于传输结束时生成的响应PID(SHTNAK) USB_DPUSB_DM的片上上拉和下拉电阻 可用作USB时钟的HOCO时钟。
Module-stop function	可设置模块停止状态以降低功耗

Figure 28.1 shows a block diagram of the USBFS.

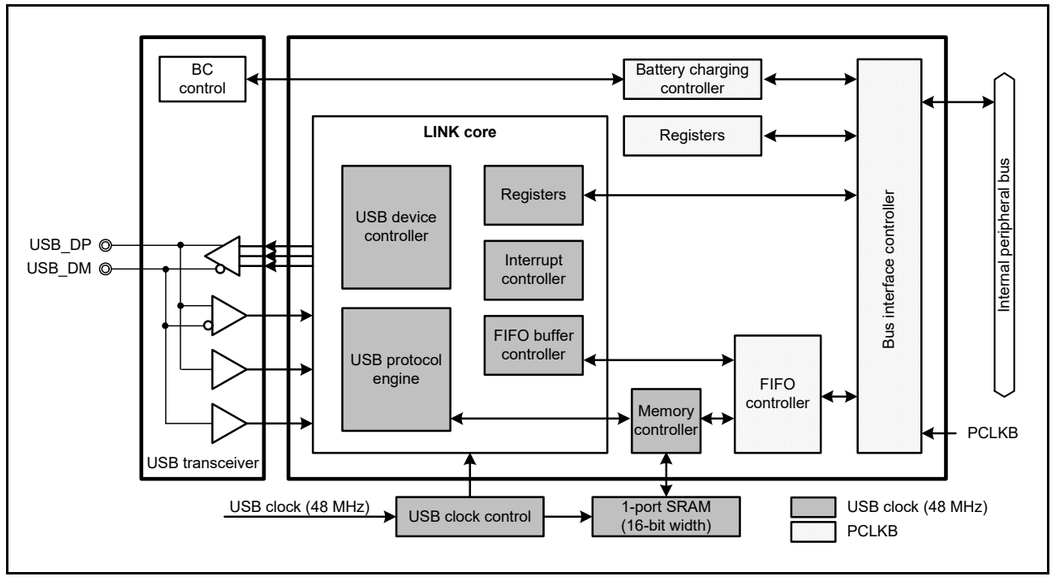


Figure 28.1 USBFS block diagram

Table 28.2 lists the I/O pins of the USBFS.

Table 28.2 USBFS pin configuration

Port	Pin name	I/O	Function
USBFS	USB_DP	I/O	D+ I/O pin for the on-chip USB transceiver. Must be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin for the on-chip USB transceiver. Must be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Must be connected to VBUS signal on the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USBFS is a device controller.*1
	USB_VBUSEN	Output	VBUS (5 V) enable signal for the external power supply IC
	USB_OVRCURA USB_OVRCURB	Input	Overcurrent pins for USBFS. Must be connected to external overcurrent detection signals.
Common	VCC_USB	Input	Power supply for USB transceiver.
	VCC_USB_LDO	Input	Power supply pin for USB transceiver. Apply the same voltage as VCC_USB
	VSS_USB	Input	USB ground pin

Note 1. P407 is 5-V tolerant.

图28.1显示了USBFS的框图。

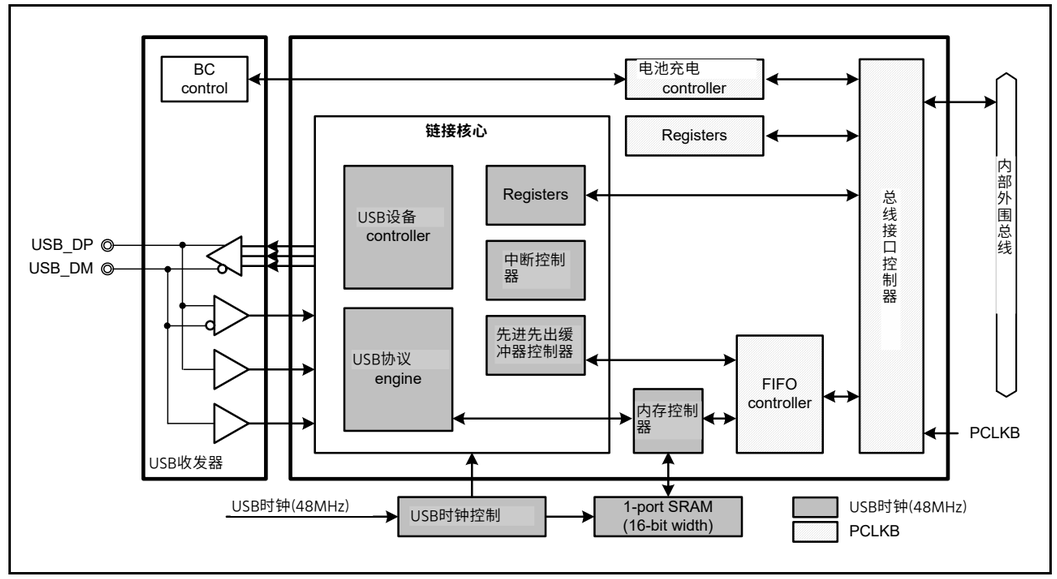


Figure 28.1 USBFS框图

表28.2列出了USBFS的IO引脚。

Table 28.2 USBFS引脚配置

Port	引脚名称	I/O	Function
USBFS	USB_DP	I/O	D+IO用于片上USB收发器的引脚。 必须连接到USB总线的D+引脚。
	USB_DM	I/O	D 片上USB收发器的IO引脚。 必须连接到USB总线的Dpin。
	USB_VBUS	Input	USB电缆连接监视器引脚。 必须连接到USB总线上的VBUS信号。当USBFS为设备控制器时，可以检测VBUS引脚状态（连接或断开）。*1
	USB_VBUSEN	Output	外部电源IC的VBUS(5V)使能信号
	USB_OVRCURA USB_OVRCURB	Input	USBFS的过流引脚。 必须连接外部过流检测信号。
Common	VCC_USB	Input	USB收发器的电源。
	VCC_USB_LDO	Input	USB收发器的电源引脚。施加与VCC_ USB相同的电压
	VSS_USB	Input	USB接地引脚

Note 1. P407可耐受5V。

28.2 Register Descriptions

28.2.1 System Configuration Control Register (SYSCFG)

Address(es): USBFS.SYSCFG 4009 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKE	—	CNEN	—	DCFM	DRPD	DPRPU	DMRPU	—	—	USBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USBE	USBFS Operation Enable	0: Disabled 1: Enabled.	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DMRPU	D- Line Resistor Control*1	0: Line pull-up disabled 1: Line pull-up enabled.	R/W
b4	DPRPU	D+ Line Resistor Control*1	0: Line pull-up disabled 1: Line pull-up enabled.	R/W
b5	DRPD	D+/D– Line Resistor Control	0: Line pull-down disabled 1: Line pull-down enabled.	R/W
b6	DCFM	Controller Function Select	0: Device controller selected 1: Host controller selected.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CNEN	CNEN Single-Ended Receiver Enable	0: Single-ended receiver disabled 1: Single-ended receiver enabled.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	SCKE	USB Clock Enable*2	0: Clock supply to the USBFS stopped 1: Clock supply to the USBFS enabled.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not enable the DMRPU and DPRPU bits at the same time.
Note 2. After writing 1 to the SCKE bit, read it and confirm it is set to 1.

USBE bit (USBFS Operation Enable)

The USBE bit enables or disables operation of the USBFS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 28.3. Only change this bit while the SCKE bit is 1. In host controller mode, this bit must be set to 1 after setting the DRPD bit to 1, eliminating SYSSTS0.LNST[1:0] bit chattering, and confirming that the USB bus state is stable.

Table 28.3 Registers initialized by writing 0 to SYSCFG.USBE bit

Selected function	Register	Bit	Remarks
Device controller	SYSSTS0	LNST[1:0]	Value is saved in host controller mode
	DVSTCTR0	RHST[2:0]	-
	INTSTS0	DVSQ[2:0]	Value is saved in host controller mode
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	Value is saved in host controller mode
	USBVAL	WVALUE[15:0]	Value is saved in host controller mode
	USBINDX	WINDEX[15:0]	Value is saved in host controller mode
	USBLENG	WLENTUH[15:0]	Value is saved in host controller mode
Host controller	DVSTCTR0	RHST[2:0]	-
	FRMNUM	FRNM[10:0]	Value is saved in device controller mode

28.2 注册说明

28.2.1 系统配置控制寄存器(SYSCFG)

Address(es): USBFS.SYSCFG 4009 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKE	—	CNEN	—	DCFM	DRPD	DPRPU	DMRPU	—	—	USBE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	USBE	USBFS操作启用	0：禁用1 ：启用。	R/W
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	DMRPU	D- Line Resistor Control*1	0：线路上拉禁用1：线 路上拉使能。	R/W
b4	DPRPU	D+线路电阻控制*1	0：线路上拉禁用1：线 路上拉使能。	R/W
b5	DRPD	D+D 线路电阻控制	0：禁用线路下拉1：启用 线路下拉。	R/W
b6	DCFM	控制器功能选择	0：选择设备控制器1：选择 主机控制器。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	CNEN	CNEN Single-Ended Receiver Enable	0：禁用单端接收器1：启用单端 接收器。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W
b10	SCKE	USB时钟启用*2	0：停止向USBFS提供时钟1：使能向US BFS提供时钟。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 不要同时使能DMRPU和DPRPU位。
Note 2. 向SCKE位写入1后，读取它并确认其设置为1。

USBE位（USBFS操作使能）

USBE位启用或禁用USBFS的操作。

将USBE位从1更改为0会初始化表28.3中列出的位。仅在SCKE位为1时更改该位。
在主机控制器模式下，必须在将DRPD位设置为1后将该位设置为1，消除SYSSTS0.LNST[1:0]位抖动，并确认USB总线状态稳定。

Table 28.3 通过向SYSCFG.USBE位写入0来初始化寄存器

所选功能	Register	Bit	Remarks
设备控制器	SYSSTS0	LNST[1:0]	值以主机控制器模式保存
	DVSTCTR0	RHST[2:0]	-
	INTSTS0	DVSQ[2:0]	值以主机控制器模式保存
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	值以主机控制器模式保存
	USBVAL	WVALUE[15:0]	值以主机控制器模式保存
	USBINDX	WINDEX[15:0]	值以主机控制器模式保存
	USBLENG	WLENTUH[15:0]	值以主机控制器模式保存
主机控制器	DVSTCTR0	RHST[2:0]	-
	FRMNUM	FRNM[10:0]	值保存在设备控制器模式中

DMRPU bit (D- Line Resistor Control*1)

The DMRPU bit enables or disables pulling up the D- line in device controller mode.

When the DMRPU bit is set to 1 in device controller mode, the USBFS pulls up the D- line to notify the USB host that it attached as a low-speed device. Changing the DMRPU bit from 1 to 0 releases the pull-up, thereby notifying the USB host that it detached.

Set this bit to 0 in host controller mode.

DPRPU bit (D+ Line Resistor Control*1)

The DPRPU bit enables or disables pulling up the D+ line in device controller mode.

When the DPRPU bit is set to 1 in device controller mode, the USBFS pulls up the D+ line to notify the USB host that it attached. Changing the DPRPU bit from 1 to 0 releases the pull-up, thereby notifying the USB host that it detached.

Set this bit to 0 in host controller mode.

DRPD bit (D+/D– Line Resistor Control)

The DRPD bit enables or disables pulling down D+ and D- lines in host controller mode.

Set this bit to 1 in host controller mode and to 0 in device controller mode.

DCFM bit (Controller Function Select)

The DCFM bit selects the host or device function of the USBFS.

Only change this bit when the DMRPU, DPRPU, and DRPD bits are 0.

CNEN bit (CNEN Single-Ended Receiver Enable)

Setting the CNEN bit to 1 enables the single-ended receiver and sets the LNST bit to monitor the status of D+ and D- lines.

The CNEN bit is used when the USBFS operates as a portable device for battery charging.

SCKE bit (USB Clock Enable*2)

The SCKE bit stops or enables supplying 48-MHz clock supply to the USB.

When this bit is 0, only SYSCFG can be read from and written to. No other USB-related registers can be read from or written to.

28.2.2 System Configuration Status Register 0 (SYSSTS0)

Address(es): USBFS.SYSSTS0 4009 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	—	—	—	—	LNST[1:0]	
Value after reset:	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor	Indicates the status of the USB data lines. See Table 28.4.	R
b2	—	Reserved	The read value is undefined.	R
b5 to b3	—	Reserved	These bits are read as 0.	R
b6	HTACT	USB Host Sequencer Status Monitor	0: Host sequencer completely stopped 1: Host sequencer not completely stopped.	R
b13 to b7	—	Reserved	These bits are read as 0.	R

DMRPU位（DLine电阻控制*1）

DMRPU位启用或禁用在设备控制器模式下上拉Dline。

当DMRPU位在设备控制器模式下设置为1时，USBFS拉高Dline以通知USB主机它作为低速设备连接。将DMRPU位从1更改为0会释放上拉电阻，从而通知USB主机它已分离。

在主机控制器模式下将此位设置为0。

DPRPU位（D+线路电阻控制*1）

DPRPU位启用或禁用在设备控制器模式下上拉D+线。

当DPRPU位在设备控制器模式下设置为1时，USBFS拉高D+线以通知USB主机它已连接。将DPRPU位从1更改为0会释放上拉电阻，从而通知USB主机它已分离。

在主机控制器模式下将此位设置为0。

DRPD位（D+D 线路电阻控制）

DRPD位在主机控制器模式下启用或禁用下拉D+和Dlines。

在主机控制器模式下将此位设置为1，在设备控制器模式下设置为0。

DCFM位（控制器功能选择）

DCFM位选择USBFS的主机或设备功能。

仅当DMRPU、DPRPU和DRPD位为0时更改该位。

CNEN位（CNEN单端接收器使能）

将CNEN位设置为1使能单端接收器并设置LNST位以监控D+和D线的状态。

当USBFS作为便携式设备进行电池充电时使用CNEN位。

SCKE位（USB时钟使能*2）

SCKE位停止或启用向USB提供48MHz时钟电源。

当该位为0时，只能读取和写入SYSCFG。无法读取或写入其他与USB相关的寄存器。

28.2.2 系统配置状态寄存器0(SYSSTS0)

Address(es): USBFS.SYSSTS0 4009 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	—	—	—	—	LNST[1:0]	
重置后的值:	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	LNST[1:0]	USB数据线状态监视器	指示USB数据线的状态。见表28.4。	R
b2	—	Reserved	读取值未定义。	R
b5 to b3	—	Reserved	这些位读为0。	R
b6	HTACT	USB主机定序器状态 Monitor	0：主机定序器完全停止1：主机定序器未完全停止。	R
b13 to b7	—	Reserved	这些位读为0。	R

Bit	Symbol	Bit name	Description	R/W
b15, b14	OVCMON[1:0]	External USB_OVRCURA/ USB_OVRCURB Input Pin Monitor	OVCMON[1] bit indicates the USB_OVRCURA pin status OVCMON[0] bit indicates the USB_OVRCURB pin status.	R

Note 1. Depends on the status of the USB_OVRCURA/USB_OVRCURB pins.

LNST[1:0] bits (USB Data Line Status Monitor)

The LNST[1:0] bits indicate the state of the USB data lines (D+ and D-). For details, see Table 28.4.

In device controller mode, read the LNST[1:0] bits after connection processing (SYSCFG.DPRPU bit = 1) or after enabling pull-down of the lines (SYSCFG.DRPD bit = 1) in host controller mode.

HTACT bit (USB Host Sequencer Status Monitor)

The HTACT bit is 0 when the host sequencer of the USBFS is completely stopped.

In host controller mode, check that the HTACT bit is 0 before setting the DVSTCTR0.UACT bit to 0 to place the USBFS in a suspended state or setting the SCKE bit to 0 to stop the clock supply during communication.

OVCMON[1:0] bits (External USB_OVRCURA/ USB_OVRCURB Input Pin Monitor)

The OCVMON[1:0] bits indicate the status of the overcurrent signals from an external power supply IC.

Table 28.4 Status of USB data bus lines (D+ line, D- line)

LNST[1:0] bits	During full-speed operation	During low-speed operation
00b	SE0	SE0
01b	J-State	K-State
10b	K-State	J-State
11b	SE1	SE1

28.2.3 Device State Control Register 0 (DVSTCTR0)

Address(es): USBFS.DVSTCTR0 4009 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	RHST[2:0]	USB Bus Reset Status	• In host controller mode: b2 b0 0 0 0: Communication speed indeterminate (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection. • In device controller mode: b2 b0 0 0 0: Communication speed indeterminate 0 0 1: USB bus reset in progress or low-speed connection 0 1 0: USB bus reset in progress or full-speed connection.	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	UACT	USB Bus Enable	0: Downstream port disabled (SOF transmission disabled) 1: Downstream port enabled (SOF transmission enabled).	R/W
b5	RESUME	Resume Output	0: Resume signal not output 1: Resume signal output.	R/W

Bit	Symbol	位名称	Description	R/W
b15, b14	OVCMON[1:0]	外部USB_OVRCURAUSB_OVRCURB输入引脚 Monitor	OVCMON[1]位指示USB_OVRCURA引脚状态OVCMON[0]位指示USB_OVRCURB引脚状态。	R

Note 1. 取决于USB_OVRCURAUSB_OVRCURB引脚的状态。

LNST[1:0]位（USB数据线状态监视器）

LNST[1:0]位指示USB数据线（D+和D−）的状态。详见表28.4。

在设备控制器模式下，在主机控制器模式下连接处理（SYSCFG.DPRPU位=1）或启用线路下拉（SYSCFG.DRPD位=1）之后读取LNST[1:0]位。

HTACT位（USB主机定序器状态监视器）

当USBFS的主机定序器完全停止时，HTACT位为0。

在主机控制器模式下，在将DVSTCTR0.UACT位设置为0以将USBFS置于挂起状态或将SCKE位设置为0以在通信期间停止时钟供应之前，请检查HTACT位是否为0。

OVCMON[1:0]位（外部USB_OVRCURAUSB_OVRCURB输入引脚监视器）

OCVMON[1:0]位指示来自外部电源IC的过流信号的状态。

Table 28.4 USB数据总线状态（D+线、Dline）

LNST[1:0] bits	全速运行期间	低速运转时
00b	SE0	SE0
01b	J-State	K-State
10b	K-State	J-State
11b	SE1	SE1

28.2.3 设备状态控制寄存器0(DVSTCTR0)

Address(es): USBFS.DVSTCTR0 4009 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	RHST[2:0]	USB总线复位状态	在主机控制器模式下：b2b0000：通信速度不确定（通电状态或无连接）1xx：USB总线复位正在进行中001：低速连接010：全速连接。 在设备控制器模式下：b2b0000：通信速度不确定001：USB总线正在复位或低速连接010：USB总线正在复位或全速连接。	R
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	UACT	USB总线启用	0：禁用下行端口（禁用SOF传输）1：启用下行端口（启用SOF传输）。	R/W
b5	RESUME	恢复输出	0：不输出恢复信号1：输出恢复信号。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	USBRST	USB Bus Reset Output	0: USB bus reset signal not output 1: USB bus reset signal output.	R/W
b7	RWUPE	Wakeup Detection Enable	0: Downstream port wakeup disabled 1: Downstream port wakeup enabled.	R/W
b8	WKUP	Wakeup Output	0: Remote wakeup signal not output 1: Remote wakeup signal output.	R/W
b9	VBUSEN	USB_VBUSEN Output Pin Control	0: External USB_VBUSEN pin outputs low 1: External USB_VBUSEN pin outputs high.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

RHST[2:0] bits (USB Bus Reset Status)

The RHST[2:0] bits indicate the status of the USB bus reset.

In host controller mode, writing 1 to the USBRST bit causes the RHST[2:0] bits to set to 100b. When 0 is written to the USBRST bit and the USBFS ends the SE0 state, the RHST[2:0] bits update to a new value.

In device controller mode, if the USBFS detects a USB bus reset, the RHST[2:0] bits are set to 010b if the DPRPU bit is 1 or 001b if the DMRPU is 1, and a DVST interrupt is generated.

UACT bit (USB Bus Enable)

When set to 1 in host controller mode, the UACT bit enables USB bus operation by controlling SOF packet transmission to the USB bus in addition to data and reception. The USBFS starts SOF packet output within one frame period after this bit is set to 1. When UACT is set to 0, the USB enters the idle state after the SOF packet output.

With this bit set to 0, the USB enters an idle state after outputting SOF packets.

The USB sets the UACT bit to 0 on any of the following conditions:

- A DTCH interrupt is detected during communication (when UACT = 1)
- An EOFERR interrupt is detected during communication (when UACT = 1).

Always write 1 to the UACT bit at the end of the USB bus reset processing (writing 0 to the USBRST bit) or at the end of resume processing from the suspended state (writing 0 to the RESUME bit).

In device controller mode, always set this bit to 0.

RESUME bit (Resume Output)

The RESUME bit controls the resume signal output in host controller mode.

When this bit is set to 1, the USBFS drives the USB port to the K-state and outputs the resume signal. The USBFS sets the bit to 1 on detection of a remote wakeup signal while the RWUPE bit is 1 and in the USB suspended state.

The USBFS continues outputting the K-state while the RESUME bit is 1, until the bit is set to 0 by software. The RESUME bit must be 1 (resume period) for the time defined in the USB 2.0 specification. Only set this bit to 1 while the interface is in the suspended state. Write 1 to the UACT bit simultaneously with the end of the resume processing (writing 0 to the RESUME bit).

Always set this bit to 0 in device controller mode.

USBRST bit (USB Bus Reset Output)

The USBRST bit controls the output of the USB bus reset signal in host controller mode. When this bit is set to 1, the USBFS drives the USB port to the SE0 state to reset the USB bus. The USBFS continues outputting SE0 while the USBRST bit is 1, until the bit is cleared to 0 by software. The USBRST bit must be 1 (USB bus reset period) for the time defined in the USB 2.0 specification.

Writing 1 to this bit during communication (UACT bit = 1) or during resume processing (RESUME bit = 1) prevents the USBFS from starting USB bus reset processing until both the UACT and RESUME bits become 0. Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (writing 0 to the USBRST bit).

Bit	Symbol	位名称	Description	R/W
b6	USBRST	USB总线复位输出	0：USB总线复位信号不输出1：USB总线复位信号输出。	R/W
b7	RWUPE	唤醒检测启用	0：禁用下行端口唤醒1：启用下行端口唤醒。	R/W
b8	WKUP	唤醒输出	0：不输出远程唤醒信号1：输出远程唤醒信号。	R/W
b9	VBUSEN	USB_VBUSEN输出引脚Control	0：外部USB_VBUSEN引脚输出低电平1：外部USB_VBUSEN引脚输出高电平。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

x: Don't care

RHST[2:0]位（USB总线复位状态）

RHST[2:0]位指示USB总线复位的状态。

在主机控制器模式下，将1写入USBRST位会导致RHST[2:0]位设置为100b。当0被写入USBRST位和USBFS结束SE0状态，RHST[2:0]位更新为新值。

在设备控制器模式下，如果USBFS检测到USB总线复位，如果DPRPU位为1，则RHST[2:0]位设置为010b，如果DMRPU为1，则设置为001b，并产生DVST中断。

UACT位（USB总线使能）

在主机控制器模式下设置为1时，UACT位通过控制向USB总线发送SOF数据包以及数据和接收来启用USB总线操作。USBFS在该位设置为1后的一帧周期内开始SOF数据包输出。当UACT设置为0时，USB在SOF数据包输出后进入空闲状态。

该位设置为0，USB输出SOF数据包后进入空闲状态。

USB在以下任一条件下将UACT位设置为0：

- 在通信期间检测到DTCH中断（当UACT=1时）
- 通信期间检测到EOFERR中断（当UACT=1时）。

在USB总线复位处理结束（将0写入USBRST位）或从挂起状态恢复处理结束（将0写入RESUME位）时，始终向UACT位写入1。

在设备控制器模式下，始终将此位设置为0。

RESUME位（恢复输出）

RESUME位控制主机控制器模式下的恢复信号输出。

当该位设置为1时，USBFS将USB端口驱动到K状态并输出恢复信号。当RUPE位为1且处于USB挂起状态时，USBFS在检测到远程唤醒信号时将该位设置为1。

当RESUME位为1时，USBFS继续输出K状态，直到该位被软件设置为0。在USB2.0规范中定义的时间内，RESUME位必须为1（恢复周期）。仅当接口处于挂起状态时将此位设置为1。在恢复处理结束的同时向UACT位写入1（向RESUME位写入0）。

在设备控制器模式下始终将此位设置为0。

USBRST位（USB总线复位输出）

USBRST位控制主机控制器模式下USB总线复位信号的输出。当该位设置为1时，USBFS将USB端口驱动到SE0状态以复位USB总线。USBFS继续输出SE0而USBRST位为1，直到该位被软件清零。在USB2.0规范中定义的时间内，USBRST位必须为1（USB总线复位周期）。

在通信期间（UACT位=1）或恢复处理期间（RESUME位=1）向该位写入1可防止USBFS开始USB总线复位处理，直到UACT和RESUME位都变为0。同时向UACT位写入1USB总线复位处理结束（向USBRST位写入0）。

Always set this bit to 0 in device controller mode.

RWUPE bit (Wakeup Detection Enable)

The RWUPE bit enables or disables remote wakeup signals (resume signals) from downstream peripheral devices in host controller mode. When this bit is set to 1, the USBFS detects a remote wakeup signal (K-state for 2.5 µs) from a downstream peripheral device, and it performs resume processing, driving the K-state.

When this bit set to 0, the USBFS ignores remote wakeup signals (K-states) from peripheral devices connected to the USB port. Do not stop the internal clock while the RWUPE bit is 1, even in the suspended state (SYSCFG.SCKE bit must be set to 1).

Always set this bit to 0 in device controller mode.

WKUP bit (Wakeup Output)

The WKUP bit enables or disables remote wakeup signals (resume signals) to the USB bus in device controller mode.

The USBFS controls the output timing of the remote wakeup signals. When this bit is set to 1, the USBFS clears it to 0 after outputting the K-state for 10 ms. The USB 2.0 specification specifies that the USB bus idle state must be maintained for 5 ms or longer before a remote wakeup signal is sent. If the USB writes 1 to this bit immediately after detecting the suspended state, the K-state is output after 2 ms.

Only write 1 to this bit when the device is in the suspended state (INTSTS0.DVSQ[2:0] bits = 1xxb) and the USB host enables the remote wakeup signal. Do not stop the internal clock while this bit is 1, even in the suspended state (SYSCFG.SCKE bit is 1). Set this bit to 0 in host controller mode.

28.2.4 CFIFO Port Register (CFIFO/CFIFOL)
D0FIFO Port Register (D0FIFO/D0FIFOL)
D1FIFO Port Register (D1FIFO/D1FIFOL)

(1) When the MBW bit is 1

Address(es): USBFS.CFIFO 4009 0014h, USBFS.D0FIFO 4009 0018h, USBFS.D1FIFO 4009 001Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(2) When the MBW bit is 0

Address(es): USBFS.CFIFOL 4009 0014h, USBFS.D0FIFOL 4009 0018h, USBFS.D1FIFOL 4009 001Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	FIFOPORT[15:0]*1	FIFO Port	Read receive data from the FIFO buffer or write transmit data to the FIFO buffer by accessing these bits.	R/W

Note 1. The valid bits depend on the MBW settings (CFIFOSEL.MBW, D0FIFOSEL.MBW, and D1FIFOSEL.MBW) and BIGEND settings (CFIFOSEL.BIGEND, D0FIFOSEL.BIGEND, and D1FIFOSEL.BIGEND) in the associated port select register. See Table 28.5 and Table 28.6.

Three FIFO ports are available:

- CFIFO
- D0FIFO

在设备控制器模式下始终将此位设置为0。

RUPE位（唤醒检测使能）

在主机控制器模式下，RWUPE位启用或禁用来自下游外围设备的远程唤醒信号（恢复信号）。当该位设置为1时，USBFS检测到来自下游外围设备的远程唤醒信号（K状态持续2.5µs），并执行恢复处理，驱动K状态。

当该位设置为0时，USBFS忽略来自连接到USBFS的外围设备的远程唤醒信号（K状态）
USB端口。请勿在RHUPE位为1时停止内部时钟，即使处于挂起状态（SYSCFG.SCKE位必须设置为1）。

在设备控制器模式下始终将此位设置为0。

WKUP位（唤醒输出）

WKUP位在设备控制器模式下启用或禁用到USB总线的远程唤醒信号（恢复信号）。

USBFS控制远程唤醒信号的输出时序。当该位设置为1时，USBFS在输出K状态10ms后将其清除为0。USB2.0规范规定，在发送远程唤醒信号之前，USB总线空闲状态必须保持5ms或更长时间。如果USB在检测到挂起状态后立即向该位写入1，则在2ms后输出K-state。

仅当设备处于挂起状态（INTSTS0.DVSQ[2:0]位=1xxb）且USB主机使能远程唤醒信号时向该位写入1。当该位为1时不要停止内部时钟，即使处于挂起状态（SYSCFG.SCKE位为1）。在主机控制器模式下将此位设置为0。

28.2.4 CFIFO端口寄存器(CFIFOCFIFOL)
D0FIFO端口寄存器(D0FIFOD0FIFOL)D1FIF
O端口寄存器(D1FIFOD1FIFOL)

(1)MBW位为1时

Address(es): USBFS.CFIFO 4009 0014h, USBFS.D0FIFO 4009 0018h, USBFS.D1FIFO 4009 001Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(2)MBW位为0时

Address(es): USBFS.CFIFOL 4009 0014h, USBFS.D0FIFOL 4009 0018h, USBFS.D1FIFOL 4009 001Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	FIFOPORT[15:0]*1	FIFO Port	通过访问这些位从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。	R/W

Note 1. 有效位取决于相关端口选择寄存器中的MBW设置（CFIFOSEL.MBW、D0FIFOSEL.MBW和D1FIFOSEL.MBW）和BIGEND设置（CFIFOSEL.BIGEND、D0FIFOSEL.BIGEND和D1FIFOSEL.BIGEND）。请参见表28.5和表28.6。

三个FIFO端口可用：

- CFIFO
- D0FIFO

- D1FIFO.

Each FIFO port is configured with:

- A port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port select register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR).

Each FIFO port has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port.
- Access to the FIFO buffer for DMA or DTC transfers is through the D0FIFO or D1FIFO port.
- The D0FIFO and D1FIFO ports can also be accessed by the CPU.
- When using functions specific to the FIFO port, such as the DMA or DTC transfer function, the pipe number selected in the CURPIPE[3:0] bits of the Port Select Register cannot be changed.
- Registers configuring a FIFO port do not affect other FIFO ports.
- The same pipe must not be assigned to two or more FIFO ports.
- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU.

FIFOPORT[15:0] bits (FIFO Port)

When the FIFOPORT bit is accessed, the USBFS reads the received data from the FIFO buffer or writes the transmission data to the FIFO buffer. The FIFO port register can be accessed only when the FRDY bit in the associated port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

The valid bits in the FIFO port register depend on the MBW and BIGEND settings in the port select register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL). See Table 28.5 and Table 28.6.

Table 28.5 Endian operation in 16-bit access

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 28.6 Endian operation in 8-bit access

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	Access prohibited*1	N + 0 data
1	Access prohibited*1	N + 0 data

Note 1. Writing to or reading from an access-prohibited area is not allowed.

- D1FIFO.

每个FIFO端口配置有：

- 处理从FIFO缓冲区读取数据和将数据写入FIFO缓冲区的端口寄存器（CFIFO、D0FIFO或D1FIFO）
- 选择分配给FIFO端口的管道的端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）
- 端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）。

每个FIFO端口具有以下约束：

- 通过CFIFO端口访问DCP控制传输的FIFO缓冲区。
- 通过D0FIFO或D1FIFO端口访问DMA或DTC传输的FIFO缓冲区。
- CPU也可以访问D0FIFO和D1FIFO端口。
- 当使用特定于FIFO端口的功能时，例如DMA或DTC传输功能，在端口选择寄存器的CURPIPE[3:0]位中选择的管道编号不能更改。
- 配置FIFO端口的寄存器不会影响其他FIFO端口。
- 不得将同一管道分配给两个或多个FIFO端口。
- 有两种FIFO缓冲区状态，一种授予CPU访问权限，另一种授予串行接口引擎(SIE)。当SIE有访问权限时，CPU不能访问FIFO缓冲区。

FIFOPORT[15:0]位（FIFO端口）

当访问FIFOPORT位时，USBFS从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。只有当相关端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）中的FRDY位为1时，才能访问FIFO端口寄存器。

FIFO端口寄存器中的有效位取决于端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）中的MBW和BIGEND设置。请参见表28.5和表28.6。

Table 28.5 16位访问中的字节序操作

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 28.6 8位访问中的字节序操作

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	禁止访问*1	N + 0 data
1	禁止访问*1	N + 0 data

Note 1. 不允许写入或读取禁止访问的区域。

28.2.5 CFIFO Port Select Register (CFIFOSEL) D0FIFO Port Select Register (D0FIFOSEL) D1FIFO Port Select Register (D1FIFOSEL)

CFIFOSEL

Address(es): USBFS.CFIFOSEL 4009 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	CFIFO Port Access Pipe Specification	b3 b0 0 0 0 0: DCP (Default control pipe) 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	ISEL	CFIFO Port Access Direction When DCP is Selected	0: Reading from the buffer memory is selected 1: Writing to the buffer memory is selected.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BIGEND	CFIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	MBW	CFIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	REW	Buffer Pointer Rewind	0: The buffer pointer is not rewound 1: The buffer pointer is rewound.	R/W*1
b15	RCNT	Read Count Mode	0: The DTLN[8:0] bits (CFIFOCTR.DTLN[8:0], D0FIFOCTR.DTLN[8:0], D1FIFOCTR.DTLN[8:0]) are cleared when all received data is read from the CFIFO. In double buffer mode, the DTLN[8:0] bit value is cleared when all data is read from only a single plane. 1: The DTLN[8:0] bits decrement each time the received data is read from the CFIFO.	R/W

Note 1. Only 0 can be read.

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (CFIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number used to read or write data through the CFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process.

Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

28.2.5 CFIFO端口选择寄存器(CFIFOSEL) D0FIFO端口选择寄存器(D0FIFOSEL)D1FIFO端口选择寄存器(D1FIFOSEL)

CFIFOSEL

Address(es): USBFS.CFIFOSEL 4009 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CURPIPE[3:0]	CFIFO端口访问管道规范	b3b00000：DCP（默认控制管道） 0001：管道10010：管道20011：管道30100：管道40101：管道50110：管道60111：管道71000：管道81001：管道9。禁止其他设置。	R/W
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	ISEL	CFIFO端口访问方向何时已选择DCP	0：选择从缓冲存储器读取1：选择写入缓冲存储器。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	BIGEND	CFIFO端口字节序控制	0：小端1：大端。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W
b10	MBW	CFIFO端口访问位宽	0: 8-bit width 1: 16-bit width.	R/W
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	REW	缓冲区指针倒带	0：缓冲区指针不倒带1：缓冲区指针倒带。	R/W*1
b15	RCNT	读取计数模式	0：DTLN[8:0]位（CFIFOCTR.DTLN[8:0]，D0FIFOCTR.DTLN[8:0]、D1FIFOCTR.DTLN[8:0]）在从CFIFO读取所有接收数据时被清除。在双缓冲模式下，当仅从单个平面读取所有数据时，清除DTLN[8:0]位的值。1：每次从CFIFO读取接收到的数据时，DTLN[8:0]位递减。	R/W

Note 1. 只能读取0。

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（CFIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过CFIFO端口读取或写入数据的管道号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。

不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

During FIFO buffer access, the current pipe specification is maintained until the access is complete, even if software attempts to change the CURPIPE[3:0] setting. Access continues after the current value is written back to the CURPIPE[3:0] bits.

ISEL bit (CFIFO Port Access Direction When DCP is Selected)

After writing a new value to the ISEL bit with the DCP as the selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process. Set the ISEL bit and the CURPIPE[3:0] bits simultaneously.

MBW bit (CFIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the CFIFO port.

When the selected pipe is receiving, set the CURPIPE[3:0] bits and MBW bits simultaneously. After a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in the MBW bit.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit width to 16-bit width while data is written to the buffer memory.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering, this setting enables re-reading of the currently-read FIFO buffer plane from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

D0FIFOSEL, D1FIFOSEL

Address(es): USBFS.D0FIFOSEL 4009 0028h, USBFS.D1FIFOSEL 4009 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO Port Access Pipe Specification	b3 b0 0 0 0 0: No pipe specification 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BIGEND	FIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

在FIFO缓冲区访问期间，即使软件尝试更改CURPIPE[3:0]设置，当前管道规范也会保持到访问完成。将当前值写回CURPIPE[3:0]位后继续访问。

ISEL位（选择DCP时的CFIFO端口访问方向）

在以DCP作为选定管道的情况下将新值写入ISEL位后，读取该位以检查写入的值是否与读取的值一致，然后再进行下一个过程。同时设置ISEL位和CURPIPE[3:0]位。

MBW位（CFIFO端口访问位宽度）

MBW位指定访问CFIFO端口的位宽。

当所选管道正在接收时，同时设置CURPIPE[3:0]位和MBW位。在写入这些位开始从FIFO缓冲区读取数据后，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，使用MBW位中设置的访问大小进行读取。

当所选管道正在传输时，在将数据写入缓冲存储器时，位宽不能从8位宽更改为16位宽。

即使选择了16位宽度，也可以通过字节访问控制写入奇数个字节。

REW位（缓冲区指针倒带）

REW位指定是否倒回缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在双缓冲中，此设置允许从第一个条目重新读取当前读取的FIFO缓冲区平面。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将REW位设置为1之前，请务必检查FRDY位是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

D0FIFOSEL, D1FIFOSEL

Address(es): USBFS.D0FIFOSEL 4009 0028h, USBFS.D1FIFOSEL 4009 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO端口访问管道 Specification	b3b00000：无管道规格0001：管道10010：管道20011：管道30100：管道40101：管道50110：管道60111：管道71000：管道81001：管道9。禁止其他设置。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	BIGEND	FIFO端口字节序控制	0：小端1：大端。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b10	MBW	FIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	DREQE	DMA/DTC Transfer Request Enable	0: DMA/DTC transfer request is disabled 1: DMA/DTC transfer request is enabled.	R/W
b13	DCLRM	Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read	0: Auto buffer clear mode is disabled 1: Auto buffer clear mode is enabled.	R/W
b14	REW	Buffer Pointer Rewind	0: The buffer pointer is not rewound 1: The buffer pointer is rewound.	R/W*1
b15	RCNT	Read Count Mode	0: DTLN[8:0] bits (CFIFOCTR.DTLN[8:0], D0FIFOCTR.DTLN[8:0], D1FIFOCTR.DTLN[8:0]) cleared when all receive data is read from DnFIFO. (In double buffer mode, the DTLN bit Value is cleared when all data is read from only a single plane.) 1: DTLN[8:0] bits decrement each time receive data is read from DnFIFO. (n = 0, 1)	R/W

Note 1. Only 0 can be read.

The same pipe must not be specified by the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected. The pipe number must not be changed while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number used to read or write data through the D0FIFO port or D1FIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, the current pipe specification is maintained until the access is complete, even if software attempts to change the CURPIPE[3:0] setting. Access continues after the current value is written back to the CURPIPE[3:0] bits.

MBW bit (FIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the D0FIFO port or D1FIFO port.

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in the MBW bit. Set the CURPIPE[3:0] bits and the MBW bit simultaneously.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit width to 16-bit width while data is being written to the FIFO memory.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

DREQE bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. To enable DMA or DTC transfer requests, set this bit to 1 after setting the CURPIPE[3:0] bits. To change the CURPIPE[3:0] setting, first set this bit to 0.

DCLRM bit (Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read)

The DCLRM bit enables or disables automatic FIFO buffer clearing after data in the selected pipe is read.

When this bit is set to 1, on receiving a zero-length packet while the FIFO buffer assigned to the selected pipe is empty, or when reading of a received short packet is complete while the PIPECFG.BFRE bit is 1, the USBFS sets the BCLR bit in the FIFO Port Control Register to 1.

When using the USBFS with the SOFCFG.BRDYM bit set to 1, set this bit to 0.

Bit	Symbol	位名称	Description	R/W
b10	MBW	FIFO端口访问位宽	0: 8-bit width 1: 16-bit width.	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b12	DREQE	DMADTC传输请求 Enable	0：禁用DMADTC传输请求1：启用DMA DTC传输请求。	R/W
b13	DCLRM	自动缓冲存储器清除模式 后访问 读取指定的管道数据	0：禁用自动缓冲区清除模式1：启用 自动缓冲区清除模式。	R/W
b14	REW	缓冲区指针倒带	0：缓冲区指针不倒带1：缓冲区指 针倒带。	R/W*1
b15	RCNT	读取计数模式	0：当从DnFIFO读取所有接收数据时，DTLN[8:0]位（CFIFOCTR.DTLN[8:0]、D0FIFOCTR.DTLN[8:0]、D1FIFOCTR.DTLN[8:0]）清零。（在双缓冲模式下，仅从单个平面读取所有数据时，清除DTLN位的值。）1：每次从DnFIFO读取接收数据时，DTLN[8:0]位递减。(n=0 1)	R/W

Note 1. 只能读取0。

CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位不得指定相同的管道。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。启用DMA或DTC传输时，不得更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过D0FIFO端口或D1FIFO端口读取或写入数据的管道号。
写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，即使软件尝试更改CURPIPE[3:0]设置，当前管道规范也会保持到访问完成。将当前值写回CURPIPE[3:0]位后继续访问。

MBW位（FIFO端口访问位宽）

MBW位指定访问D0FIFO端口或D1FIFO端口的位宽。

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，使用MBW位中设置的访问大小进行读取。同时设置CURPIPE[3:0]位和MBW位。

当所选管道正在传输时，位宽不能从8位宽更改为16位宽，同时数据正在写入FIFO存储器。

即使选择了16位宽度，也可以通过字节访问控制写入奇数个字节。

DREQE位（DMADTC传输请求使能）

DREQE位启用或禁用DMA或DTC传输请求的发出。要启用DMA或DTC传输请求，请在设置CURPIPE[3:0]位后将此位设置为1。要更改CURPIPE[3:0]设置，首先将该位设置为0。

DCLRM位（读取指定管道数据后访问的自动缓冲存储器清除模式）

在读取所选管道中的数据后，DCLRM位启用或禁用自动FIFO缓冲区清除。

当该位设置为1时，在分配给所选管道的FIFO缓冲区为空时接收到零长度数据包，或者当PIPECFG.BFRE位为1时完成读取接收到的短数据包时，USBFS设置FIFO端口控制寄存器中的BCLR位为1。

当使用SOFCFG.BRDYM位设置为1的USBFS时，将此位设置为0。

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering, this setting enables re-reading of the currently-read FIFO buffer plane from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting this bit to 1, always check that the FRDY bit is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

The RCNT bit specifies the read mode for the value in the CFIFOCTR.DTLN bit. When accessing DnFIFO with the PIPECFG.BFRE bit set to 1, set the RCNT bit to 0.

28.2.6 CFIFO Port Control Register (CFIFOCTR) D0FIFO Port Control Register (D0FIFOCTR) D1FIFO Port Control Register (D1FIFOCTR)

Address(es): USBFS.CFIFOCTR 4009 0022h, USBFS.D0FIFOCTR 4009 002Ah, USBFS.D1FIFOCTR 4009 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	DTLN[8:0]	Receive Data Length	Indicates the received data length. These bits indicate different values depending on the setting of the RCNT bit setting in the port select register. For details, see the description of the DTLN[8:0] bits in this section.	R
b12 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FRDY	FIFO Port Ready	0: FIFO port access disabled 1: FIFO port access enabled.	R
b14	BCLR	CPU Buffer Clear	0: Does not operate 1: FIFO buffer cleared in the CPU.	R/W*1
b15	BVAL	Buffer Memory Valid Flag	0: Invalid 1: Writing ended.	R/W

Note 1. Only 0 can be read.

The CFIFOCTR, D0FIFOCTR, and D1FIFOCTR registers correspond to the CFIFO, D0FIFO, and D1FIFO buffers.

DTLN[8:0] bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the receive data.

While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the DnFIFOSEL.RCNT bit (n = 0, 1), as follows:

- RCNT = 0
  The USBFS sets the DTLN[8:0] bits to indicate the length of the received data until the CPU or DMA/DTC has read all of the received data from a single FIFO buffer plane.
  While the PIPECFG.BFRE bit = 1, the USB retains the length of the received data until the BCLR bit is set to 1, even after all the data is read.
- RCNT = 1
  The USBFS decrements the value indicated by the DTLN[8:0] bits each time data is read from the FIFO buffer. The value is decremented by 1 when the MBW bit is 0, and by 2 when the MBW bit is 1.

REW位（缓冲区指针倒带）

REW位指定是否倒回缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在双缓冲中，此设置允许从第一个条目重新读取当前读取的FIFO缓冲区平面。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将此位设置为1之前，请始终检查FRDY位是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

RCNT位指定CFIFOCTR.DTLN位中值的读取模式。当使用DnFIFO访问PIPECFG.BFRE位设置为1，将RCNT位设置为0。

28.2.6 CFIFO端口控制寄存器(CFIFOCTR) D0FIFO端口控制寄存器(D0FIFOCTR)D1FIFO端口控制寄存器(D1FIFOCTR)

Address(es): USBFS.CFIFOCTR 4009 0022h, USBFS.D0FIFOCTR 4009 002Ah, USBFS.D1FIFOCTR 4009 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	DTLN[8:0]	接收数据长度	表示接收到的数据长度。 这些位表示不同的值，具体取决于端口选择寄存器中的RCNT位设置。有关详细信息，请参见本节中对DTLN[8:0]位的说明。	R
b12 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	FRDY	FIFO端口就绪	0：禁止FIFO端口访问1：使能FIFO端口访问。	R
b14	BCLR	CPU缓冲区清除	0：不操作1：CPU中清除FIFO缓冲区。	R/W*1
b15	BVAL	缓冲存储器有效标志	0：无效1：写入结束。	R/W

Note 1. 只能读取0。

CFIFOCTR、D0FIFOCTR和D1FIFOCTR寄存器对应于CFIFO、D0FIFO和D1FIFO缓冲区。

DTLN[8:0]位（接收数据长度）

DTLN[8:0]位指示接收数据的长度。

在读取FIFO缓冲区时，DTLN[8:0]位指示不同的值，具体取决于DnFIFOSEL.RCNT位(n=0 1)，如下所示：

- RCNT = 0
  USBFS设置DTLN[8:0]位以指示接收数据的长度，直到CPU或DMADTC从单个FIFO缓冲平面读取所有接收数据。当PIPECFG.BFRE位=1时，USB将保留接收数据的长度，直到BCLR位设置为1，即使在读取所有数据之后也是如此。
- RCNT = 1
  每次从FIFO缓冲区读取数据时，USBFS都会递减DTLN[8:0]位指示的值。MBW位为0时减1，MBW位为1时减2。

The USBFS sets these bits to 0 when all the data is read from one FIFO buffer plane. In double buffer mode, if data is received in one FIFO buffer plane before all the data is read from the other plane, the USBFS sets these bits to indicate the length of the received data in the former plane when all of the data is read from the latter plane.

FRDY bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU or DMA/DTC.

In the following cases, the USBFS sets the FRDY bit to 1 but data cannot be read through the FIFO port because there is no data to be read. In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit = 1.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer in the CPU for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBFS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBFS to clear the FIFO buffer regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is transmitting, if 1 is written to the BVAL flag and the BCLR bit simultaneously, the USBFS clears the data that is already written, enabling transmission of a zero-length packet.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY bit in the FIFO Port Control Register is 1 (set by the USBFS).

BVAL flag (Buffer Memory Valid Flag)

Set the BVAL flag to 1 when data is completely written to the FIFO buffer in the CPU for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set this flag to 1 in the following cases:

- To transmit a short packet, set this flag to 1 after data is written
- To transmit a zero-length packet, set this flag to 1 before data is written to the FIFO buffer.

The USBFS then switches the FIFO buffer from the CPU to the SIE, enabling transmission.

When data of the maximum packet size is written for the pipe in continuous transfer mode, the USBFS sets the BVAL flag to 1 and switches the FIFO buffer from the CPU to the SIE, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBFS). When the selected pipe is receiving, do not set the BVAL flag to 1.

28.2.7 Interrupt Enable Register 0 (INTENB0)

Address(es): USBFS.INTENB0 4009 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

当从一个FIFO缓冲平面读取所有数据时，USBFS将这些位设置为0。在双缓冲区模式下，如果在一个FIFO缓冲区平面中的所有数据都从另一个平面读取之前接收到数据，则USBFS设置这些位以指示从前一个平面中读取所有数据时接收到的数据的长度后一个平面。

FRDY位（FIFO端口就绪）

FRDY位指示FIFO端口是否可以被CPU或DMADTC访问。

在以下情况下，USBFS将FRDY位设置为1，但由于没有要读取的数据，因此无法通过FIFO端口读取数据。在这些情况下，将BCLR位设置为1以清除FIFO缓冲区，并启用下一个数据的发送和接收。

- 当分配给所选管道的FIFO缓冲区为空时，接收到零长度数据包
- 当PIPECFG.BFRE位=1时，接收到一个短数据包并完全读取数据。

BCLR位（CPU缓冲区清除）

将BCLR位设置为1以清除CPU中所选管道的FIFO缓冲区。

当分配给所选管道的FIFO缓冲区设置为双缓冲区模式时，USBFS仅清除
即使两个平面都已启用读取，也有FIFO缓冲区。

当DCP为选定管道时，将BCLR位设置为1允许USBFS清除FIFO缓冲区，而不管CPU或SIE是否具有访问权限。要在SIE具有访问权限时清除缓冲区，请将DCPCTR.PID[1:0]位设置为00b（NAK响应），然后再将BCLR位设置为1。

当所选管道正在传输时，如果同时向BVAL标志和BCLR位写入1，则USBFS会清除已写入的数据，从而可以传输零长度数据包。

WhentheselectedpipeisnottheDCP onlywrite1totheBCLRbitwhiletheFRDYbitintheFIFOPortControl
寄存器为1（由USBFS设置）。

BVAL标志（缓冲存储器有效标志）

当数据完全写入CPU中所选管道的FIFO缓冲区时，将BVAL标志设置为1
CURPIPE[3:0].

当所选管道正在传输时，在以下情况下将此标志设置为1：

- 要发送短数据包，请在写入数据后将此标志设置为1
- 要发送长度为零的数据包，请在将数据写入FIFO缓冲区之前将此标志设置为1。

然后USBFS将FIFO缓冲区从CPU切换到SIE，从而启用传输。

当在连续传输模式下为管道写入最大数据包大小的数据时，USBFS将BVAL标志设置为1，并将FIFO缓冲区从CPU切换到SIE，从而启用传输。

仅在FRDY位为1（由USBFS设置）时将1写入BVAL标志。当所选管道正在接收时，不要将BVAL标志设置为1。

28.2.7 中断使能寄存器0(INTENB0)

Address(es): USBFS.INTENB0 4009 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b8	BRDYE	Buffer Ready Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b9	NRDYE	Buffer Not Ready Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b10	BEMPE	Buffer Empty Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b11	CTRE	Control Transfer Stage Transition Interrupt Enable*1	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b12	DVSE	Device State Transition Interrupt Enable*1	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b13	SOFE	Frame Number Update Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b14	RSME	Resume Interrupt Enable*1	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15	VBSE	VBUS Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

Note 1. The RSME, DVSE, and CTRE bits can only be set to 1 in device controller mode. Do not set these bits to 1 in host controller mode.

When a status flag in the INTSTS0 register is set to 1 and the associated interrupt request enable bit setting in the INTENB0 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB0 register setting, the status flag in the INTSTS0 register is set to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB0 register is switched from 0 to 1 while the associated status flag in the INTSTS0 register is set to 1, a USBFS interrupt is requested.

28.2.8 Interrupt Enable Register 1 (INTENB1)

Address(es): USBFS.INTENB1 4009 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PDDETINTE0	PDDETINT0 Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SACKE	Setup Transaction Normal Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	SIGNE	Setup Transaction Error Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	EOFERRE	EOF Error Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b10 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	ATTCHE	Connection Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b12	DTCHE	Disconnection Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	BCHGE	USB Bus Change Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

Bit	Symbol	位名称	Description	R/W
b8	BRDYE	缓冲区就绪中断使能	0：禁止中断输出1：允许中断输出。	R/W
b9	NRDYE	缓冲区未就绪响应中断使能	0：禁止中断输出1：允许中断输出。	R/W
b10	BEMPE	缓冲区空中断使能	0：禁止中断输出1：允许中断输出。	R/W
b11	CTRE	控制传输阶段转换中断Enable*1	0：禁止中断输出1：允许中断输出。	R/W
b12	DVSE	设备状态转换中断启用*1	0：禁止中断输出1：允许中断输出。	R/W
b13	SOFE	帧号更新中断使能	0：禁止中断输出1：允许中断输出。	R/W
b14	RSME	恢复中断使能*1	0：禁止中断输出1：允许中断输出。	R/W
b15	VBSE	VBUS中断使能	0：禁止中断输出1：允许中断输出。	R/W

Note 1. RSME、DVSE和CTRE位只能在设备控制器模式下设置为1。不要在主机控制器模式下将这些位设置为1。

当INTSTS0寄存器中的状态标志设置为1并且相关的中断请求使能位设置在INTENB0寄存器为1，USBFS发出USBFS中断请求。

无论INTENB0寄存器设置如何，INTSTS0寄存器中的状态标志都会设置为1，以响应满足相关条件的状态变化。

当INTENB0寄存器中的中断请求使能位从0切换到1且INTSTS0寄存器中的相关状态标志设置为1时，请求USBFS中断。

28.2.8 中断使能寄存器1(INTENB1)

Address(es): USBFS.INTENB1 4009 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PDDETINTE0	PDDETINT0检测中断使能	0：禁止中断输出1：允许中断输出。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SACKE	设置事务正常响应中断使能	0：禁止中断输出1：允许中断输出。	R/W
b5	SIGNE	设置事务错误中断Enable	0：禁止中断输出1：允许中断输出。	R/W
b6	EOFERRE	EOF错误检测中断使能	0：禁止中断输出1：允许中断输出。	R/W
b10 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11	ATTCHE	连接检测中断使能	0：禁止中断输出1：允许中断输出。	R/W
b12	DTCHE	断线检测中断Enable	0：禁止中断输出1：允许中断输出。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	BCHGE	USB总线变化中断使能	0：禁止中断输出1：允许中断输出。	R/W

Bit	Symbol	Bit name	Description	R/W
b15	OVRCRE	Overcurrent Input Change Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

Note: The bits in INTENB1 can only be set to 1 in host controller mode. Do not set these bits to 1 in device controller mode.

INTENB1 specifies the interrupt masks in host controller mode and for the setup transaction.

When a status flag in the INTSTS1 register is set to 1 and the associated interrupt request enable bit setting in the INTENB1 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB1 register setting, the status flag in the INTSTS1 register is set to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB1 register is switched from 0 to 1 while the associated status flag in the INTSTS1 register is set to 1, a USBFS interrupt is requested.

Do not enable interrupts in device controller mode.

28.2.9 BRDY Interrupt Enable Register (BRDYENB)

Address(es): USBFS.BRDYENB 4009 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BRDYE	BRDY Interrupt Enable for Pipe 0	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b1	PIPE1BRDYE	BRDY Interrupt Enable for Pipe 1	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b2	PIPE2BRDYE	BRDY Interrupt Enable for Pipe 2	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3	PIPE3BRDYE	BRDY Interrupt Enable for Pipe 3	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b4	PIPE4BRDYE	BRDY Interrupt Enable for Pipe 4	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	PIPE5BRDYE	BRDY Interrupt Enable for Pipe 5	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	PIPE6BRDYE	BRDY Interrupt Enable for Pipe 6	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b7	PIPE7BRDYE	BRDY Interrupt Enable for Pipe 7	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b8	PIPE8BRDYE	BRDY Interrupt Enable for Pipe 8	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b9	PIPE9BRDYE	BRDY Interrupt Enable for Pipe 9	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The BRDYENB register enables or disables the INTSTS0.BRDY bit to be set to 1 when the BRDY interrupt is detected for each pipe.

When a status flag in the BRDYSTS register is set to 1 and the associated PIPEnBRDYE bit (n = 0 to 9) setting in the BRDYENB register is 1, the INTSTS0.BRDY flag is set to 1. In this case, if the BRDYE bit in INTENB0 is 1, the USBFS generates a BRDY interrupt request.

While at least one PIPEnBRDY bit indicates 1, the USBFS generates the BRDY interrupt request when the associated interrupt enable bit in the BRDYENB register is changed from 0 to 1 by software.

Bit	Symbol	位名称	Description	R/W
b15	OVRCRE	过流输入变化中断 Enable	0：禁止中断输出1：允许中断输出。	R/W

Note: INTENB1中的位只能在主机控制器模式下设置为1。不要在设备控制器模式下将这些位设置为1。

INTENB1指定主机控制器模式和设置事务的中断掩码。

当INTSTS1寄存器中的状态标志设置为1并且相关的中断请求使能位设置在INTENB1寄存器为1，USBFS发出USBFS中断请求。

无论INTENB1寄存器设置如何，INTSTS1寄存器中的状态标志都会设置为1，以响应满足相关条件的状态变化。

当INTENB1寄存器中的中断请求使能位从0切换到1且INTSTS1寄存器中的相关状态标志设置为1时，请求USBFS中断。

不要在设备控制器模式下启用中断。

28.2.9 BRDY中断使能寄存器(BRDYENB)

Address(es): USBFS.BRDYENB 4009 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BRDYE	管道0的BRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b1	PIPE1BRDYE	管道1的BRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b2	PIPE2BRDYE	管道2的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b3	PIPE3BRDYE	管道3的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b4	PIPE4BRDYE	管道4的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b5	PIPE5BRDYE	管道5的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b6	PIPE6BRDYE	管道6的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b7	PIPE7BRDYE	管道7的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b8	PIPE8BRDYE	管道8的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b9	PIPE9BRDYE	管道9的BRDY中断启用	0：禁止中断输出1：允许中断输出。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当检测到每个管道的BRDY中断时，BRDYENB寄存器启用或禁用INTSTS0.BRDY位以设置为1。

当BRDYSTS寄存器中的状态标志设置为1并且相关的PIPEnBRDYE位（n=0到9）在BRDYENB寄存器为1，INTSTS0.BRDY标志设置为1。在这种情况下，如果INTENB0中的BRDYE位为1，则USBFS产生一个BRDY中断请求。

当至少一个PIPEnBRDY位指示1时，当BRDYENB寄存器中相关的中断使能位由软件从0变为1时，USBFS产生BRDY中断请求。

28.2.10 NRDY Interrupt Enable Register (NRDYENB)

Address(es): USBFS.NRDYENB 4009 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0NRDYE	NRDY Interrupt Enable for Pipe 0	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b1	PIPE1NRDYE	NRDY Interrupt Enable for Pipe 1	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b2	PIPE2NRDYE	NRDY Interrupt Enable for Pipe 2	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3	PIPE3NRDYE	NRDY Interrupt Enable for Pipe 3	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b4	PIPE4NRDYE	NRDY Interrupt Enable for Pipe 4	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	PIPE5NRDYE	NRDY Interrupt Enable for Pipe 5	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	PIPE6NRDYE	NRDY Interrupt Enable for Pipe 6	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b7	PIPE7NRDYE	NRDY Interrupt Enable for Pipe 7	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b8	PIPE8NRDYE	NRDY Interrupt Enable for Pipe 8	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b9	PIPE9NRDYE	NRDY Interrupt Enable for Pipe 9	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The NRDYENB register enables or disables the INTSTS0.NRDY bit to be set to 1 when the NRDY interrupt is detected for each pipe.

When a status flag in the NRDYSTS register is set to 1 and the associated PIPEnNRDYE (n = 0 to 9) bit setting in the NRDYENB register is 1, the INTSTS0.NRDY flag is set to 1. In this case, if the NRDYE bit in INTENB0 is 1, the USBFS generates a NRDY interrupt request.

While at least one PIPEnNRDY bit indicates 1, the USBFS generates the NRDY interrupt request when the associated interrupt enable bit in the NRDYENB register is changed from 0 to 1 by software.

28.2.11 BEMP Interrupt Enable Register (BEMPENB)

Address(es): USBFS.BEMPENB 4009 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BEMPE	BEMP Interrupt Enable for Pipe 0	0: Interrupt output disabled 1: Interrupt output enabled.	R/W

28.2.10 NRDY中断使能寄存器(NRDYENB)

Address(es): USBFS.NRDYENB 4009 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0NRDYE	管道0的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b1	PIPE1NRDYE	管道1的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b2	PIPE2NRDYE	管道2的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b3	PIPE3NRDYE	管道3的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b4	PIPE4NRDYE	管道4的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b5	PIPE5NRDYE	管道5的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b6	PIPE6NRDYE	管道6的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b7	PIPE7NRDYE	管道7的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b8	PIPE8NRDYE	管道8的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b9	PIPE9NRDYE	管道9的NRDY中断使能	0：禁止中断输出1：允许中断输出。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当检测到每个管道的NRDY中断时，NRDYENB寄存器启用或禁用INTSTS0.NRDY位设置为1。

当NRDYSTS寄存器中的状态标志设置为1并且相关的PIPEnNRDYE（n=0到9）位设置NRDYENB寄存器为1，INTSTS0.NRDY标志设置为1。在这种情况下，如果INTENB0中的NRDYE位为1，则USBFS产生一个NRDY中断请求。

当至少一个PIPEnNRDY位指示1时，当NRDYENB寄存器中相关的中断使能位由软件从0变为1时，USBFS产生NRDY中断请求。

28.2.11 BEMP中断使能寄存器(BEMPENB)

Address(es): USBFS.BEMPENB 4009 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BEMPE	管道0的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	PIPE1BEMPE	BEMP Interrupt Enable for Pipe 1	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b2	PIPE2BEMPE	BEMP Interrupt Enable for Pipe 2	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b3	PIPE3BEMPE	BEMP Interrupt Enable for Pipe 3	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b4	PIPE4BEMPE	BEMP Interrupt Enable for Pipe 4	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b5	PIPE5BEMPE	BEMP Interrupt Enable for Pipe 5	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b6	PIPE6BEMPE	BEMP Interrupt Enable for Pipe 6	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b7	PIPE7BEMPE	BEMP Interrupt Enable for Pipe 7	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b8	PIPE8BEMPE	BEMP Interrupt Enable for Pipe 8	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b9	PIPE9BEMPE	BEMP Interrupt Enable for Pipe 9	0: Interrupt output disabled 1: Interrupt output enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The BEMPENB register enables or disables the INTSTS0.BEMP bit to be set to 1 when the BEMP interrupt is detected for each pipe.

When a status flag in the BEMPSTS register is set to 1 and the associated PIPEnBEMPE (n = 0 to 9) bit setting in the BEMPENB register is 1, the INTSTS0.BEMP flag is set to 1. In this case, if the BEMPE bit in INTENB0 is 1, the USBFS generates a BEMP interrupt request.

While at least one PIPEnBEMP bit indicates 1, the USBFS generates the BEMP interrupt request when the associated interrupt enable bit in the BEMPENB register is changed from 0 to 1 by software.

28.2.12 SOF Output Configuration Register (SOFCFG)

Address(es): USBFS.SOFCFG 4009 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	EDGESTS	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	EDGESTS	Edge Interrupt Output Status Monitor*1	Indicates 1 during the edge processing of an edge interrupt output signal.	R
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	BRDYM	BRDY Interrupt Status Clear Timing	0: BRDY flag cleared by software 1: BRDY flag cleared by the USBFS through a data read from the FIFO buffer or data write to the FIFO buffer.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	TRNENSEL	Transaction-Enabled Time Select*1	0: Not low-speed communication 1: Low-speed communication.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Confirm that this bit is 0 before stopping the clock supply to the USBFS.

Bit	Symbol	位名称	Description	R/W
b1	PIPE1BEMPE	管道1的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b2	PIPE2BEMPE	管道2的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b3	PIPE3BEMPE	管道3的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b4	PIPE4BEMPE	管道4的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b5	PIPE5BEMPE	管道5的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b6	PIPE6BEMPE	管道6的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b7	PIPE7BEMPE	管道7的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b8	PIPE8BEMPE	管道8的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b9	PIPE9BEMPE	管道9的BEMP中断启用	0：禁止中断输出1：允许中断输出。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当检测到每个管道的BEMP中断时，BEMPENB寄存器启用或禁用INTSTS0.BEMP位设置为1。

当BEMPSTS寄存器中的状态标志设置为1并且在BEMPENB寄存器为1，INTSTS0.BEMP标志设置为1。在这种情况下，如果INTENB0中的BEMPE位为1，则USBFS产生一个BEMP中断请求。

虽然至少有一个PIPEnBEMP位指示1，但当BEMPENB寄存器中相关的中断使能位由软件从0变为1时，USBFS会产生BEMP中断请求。

28.2.12 SOF输出配置寄存器(SOFCFG)

Address(es): USBFS.SOFCFG 4009 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	EDGESTS	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	EDGESTS	边沿中断输出状态监视器*1	在边沿中断输出信号的边沿处理期间表示1。	R
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	BRDYM	BRDY中断状态清除时序	0：BRDY标志由软件清除1：BRDY标志由USBFS通过从FIFO缓冲区读取数据或向FIFO缓冲区写入数据清除。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	TRNENSEL	Transaction-Enabled Time Select*1	0：非低速通讯1：低速通讯。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在停止向USBFS提供时钟之前，请确认该位为0。

EDGESTS bit (Edge Interrupt Output Status Monitor)

The EDGESTS bit indicates 1 during the edge processing of an edge interrupt output signal. Confirm that this bit is 0 before stopping the clock supply to the USBFS.

BRDYM bit (BRDY Interrupt Status Clear Timing)

The BRDYM bit specifies the timing for clearing the BRDY interrupt status for each pipe.

TRNENSEL bit (Transaction-Enabled Time Select)

When the USB port is in use for full- or low-speed communications, the TRNENSEL bit specifies the timing with which the USBFS issues tokens in a frame (transaction-enabled time).

Set this bit to 1 when a low-speed device is connected. The bit is only valid in host controller mode. Set this bit to 0 in device controller mode.

28.2.13 Interrupt Status Register 0 (INTSTS0)

Address(es): USBFS.INTSTS0 4009 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	0/1*1	0	0	0	0	0*2	0*3	0*3	0/1*3	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage	b2 b0 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error.	R
b3	VALID	USB Request Reception	0: Setup packet is not received 1: Setup packet is received.	R/W*4
b6 to b4	DVSQ[2:0]	Device State	b6 b4 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x: Suspended state.	R
b7	VBSTS	VBUS Input Status	0: USB_VBUS pin is low 1: USB_VBUS pin is high.	R
b8	BRDY	Buffer Ready Interrupt Status	0: BRDY interrupts are not generated 1: BRDY interrupts are generated.	R
b9	NRDY	Buffer Not Ready Interrupt Status	0: NRDY interrupts are not generated 1: NRDY interrupts are generated.	R
b10	BEMP	Buffer Empty Interrupt Status	0: BEMP interrupts are not generated 1: BEMP interrupts are generated.	R
b11	CTRT	Control Transfer Stage Transition Interrupt Status*5	0: Control transfer stage transition interrupts are not generated 1: Control transfer stage transition interrupts are generated.	R/W*4
b12	DVST	Device State Transition Interrupt Status*5	0: Device state transition interrupts are not generated 1: Device state transition interrupts are generated.	R/W*4
b13	SOFR	Frame Number Refresh Interrupt Status	0: SOF interrupts are not generated 1: SOF interrupts are generated.	R/W*4
b14	RESM	Resume Interrupt Status*5,*6	0: Resume interrupts are not generated 1: Resume interrupts are generated.	R/W*4

EDGESTS位（边缘中断输出状态监视器）

在边沿中断输出信号的边沿处理期间，EDGESTS位指示1。在停止向USBFS提供时钟之前，请确认该位为0。

BRDYM位（BRDY中断状态清除时序）

BRDYM位指定清除每个管道的BRDY中断状态的时序。

TRNENSEL位（事务使能时间选择）

当USB端口用于全速或低速通信时，TRNENSEL位指定USBFS在帧中发出令牌的时间（事务启用时间）。

当连接了低速设备时，将此位设置为1。该位仅在主机控制器模式下有效。在设备控制器模式下将此位设置为0。

28.2.13 中断状态寄存器0(INTSTS0)

Address(es): USBFS.INTSTS0 4009 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
重置后的值:	0	0	0	0/1*1	0	0	0	0	0*2	0*3	0*3	0/1*3	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CTSQ[2:0]	控制转移阶段	b2b0000：空闲或设置阶段001：控制读取数据阶段010：控制读取状态阶段011：控制写入数据阶段100：控制写入状态阶段101：控制写入（无数据）状态阶段110：控制传输顺序错误。	R
b3	VALID	USB请求接收	0：未接收到设置包1：接收到设置包。	R/W*4
b6 to b4	DVSQ[2:0]	设备状态	b6b4000：通电状态001：默认状态010：地址状态011：配置状态1xx：挂起状态。	R
b7	VBSTS	VBUS输入状态	0：USB_VBUS引脚为低电平1：USB_VBUS引脚为高电平。	R
b8	BRDY	缓冲区就绪中断状态	0：不产生BRDY中断1：产生BRDY中断。	R
b9	NRDY	缓冲区未就绪中断Status	0：不产生NRDY中断1：产生NRDY中断。	R
b10	BEMP	缓冲区空中断状态	0：不产生BEMP中断1：产生BEMP中断。	R
b11	CTRT	控制转移阶段转换中断状态 *5	0：不产生控制转移阶段转换中断1：产生控制转移阶段转换中断。	R/W*4
b12	DVST	设备状态转换中断状态 *5	0：不产生设备状态转换中断1：产生设备状态转换中断。	R/W*4
b13	SOFR	帧号刷新中断状态	0：不产生SOF中断1：产生SOF中断。	R/W*4
b14	RESM	恢复中断状态 *5,*6	0：不产生恢复中断1：产生恢复中断。	R/W*4

Bit	Symbol	Bit name	Description	R/W
b15	VBINT	VBUS Interrupt Status*6	0: VBUS interrupts are not generated 1: VBUS interrupts are generated.	R/W*4

x: Don't care

Note 1. The value is 0 when the MCU is reset and 1 after a USB bus reset.
Note 2. The value is 1 when the USB_VBUS pin is high and 0 when the USB_VBUS pin is low.
Note 3. The value is 000b when the MCU is reset and 001b after a USB bus reset.
Note 4. To clear the VBINT, RESM, SOFR, DVST, CTRT, or VALID bits, write 0 only to the bits to be cleared. Write 1 to the other bits. Do not write 0 to the status bits indicating 0.
Note 5. The status of the RESM, DVST, and CTRT bits are changed only in device controller mode. Set the associated interrupt enable bits to 0 (disabled) in host controller mode.
Note 6. The USBFS detects a change in the status indicated by the VBINT and RESM bits even while the clock supply is stopped (SCKE bit = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status through software.

CTSQ[2:0] bits (Control Transfer Stage)

In host controller mode, the read value of the CTSQ[2:0] bits is invalid.

VALID bit (USB Request Reception)

In host controller mode, the read value of the VALID bit is invalid.

DVSQ[2:0] bits (Device State)

The DVSQ[2:0] bits are initialized by a USB bus reset. In host controller mode, the read value is invalid.

BRDY bit (Buffer Ready Interrupt Status)

The BRDY bit indicates the BRDY interrupt status.

The USBFS sets the BRDY bit to 1 when it detects a BRDY interrupt status (PIPEnBRDY = 1, n = 0 to 9) on at least one pipe for which BRDY interrupts are enabled (BRDYENB.PIPEnBRDYE = 1).

For the conditions that cause the PIPEnBRDY status to be asserted, see section 28.3.3.1, BRDY interrupt.

The USBFS sets the BRDY bit to 0 when software writes 0 to all the PIPEnBRDY bits associated with the PIPEnBRDYE bits that are set to 1. The BRDY bit cannot be set to 0 even if 0 is written to this bit by software.

NRDY bit (Buffer Not Ready Interrupt Status)

The USBFS sets the NRDY bit to 1 when at least one PIPEnNRDY bit (n = 0 to 9) is set to 1 for the PIPENRDY bits associated with the PIPEnNRDYE bits (n = 0 to 9) that is set to 1 (when the USBFS detects the NRDY interrupt status in at least one pipe from the pipes for which software enables the NRDY interrupt output).

For the conditions that cause the PIPEnNRDY status to be asserted, see section 28.3.3.2, NRDY interrupt.

The USBFS sets the NRDY bit to 0 when software writes 0 to all the PIPEnNRDY bits associated with the PIPEnNRDYE bits that are set to 1. The NRDY bit cannot be set to 0 even if 0 is written to this bit by software.

BEMP bit (Buffer Empty Interrupt Status)

The BEMP bit indicates the BEMP interrupt status.

The USBFS sets the BEMP bit to 1 when it detects a BEMP interrupt status (PIPEnBEMP = 1, n = 0 to 9) on at least one pipe for which BEMP interrupts are enabled (BEMPENB.PIPEnBEMPE = 1).

For the conditions that cause the PIPEnBEMP status to be asserted, see section 28.3.3.3, BEMP interrupt.

The USBFS sets the BEMP bit to 0 when software writes 0 to all of the PIPEnBEMP bits associated with the PIPEnBEMPE bits that are set to 1. Writing 0 to the BEMP bit in software does not clear the bit.

CTRT bit (Control Transfer Stage Transition Interrupt Status)

In device controller mode, the USBFS updates the value of the CTSQ[2:0] bits and sets the CTRT bit to 1 when detecting a change in the control transfer stage. When a control transfer stage transition interrupt is generated, clear the CTRT bit before the USBFS detects the next control transfer stage transition.

Values read from the CTRT bit in host controller mode are invalid.

Bit	Symbol	位名称		Description	R/W
b15	VBINT	VBUS中断状态	*6	0：不产生VBUS中断1：产生VBUS中断。	R/W*4

x：不关心注

1。 MCU复位时为0，USB总线复位后为1。
Note 2. 当USB_VBUS引脚为高电平时值为1，当USB_VBUS引脚为低电平时值为0。
Note 3. MCU复位时值为000b，USB总线复位后值为001b。
Note 4. 要清除VBINT、RESM、SOFR、DVST、CTRT或VALID位，只需将0写入要清除的位。将1写入其他位。
不要将0写入指示0的状态位。
Note 5. RESM、DVST和CTRT位的状态仅在设备控制器模式下更改。在主机控制器模式下，将相关的中断使能位设置为0（禁用）。

Note 6. USBFS检测到由VBINT和RESM位指示的状态变化，即使在时钟供应停止（SCKE位=0）时，它也会在相关的中断请求位为1时请求中断。在清除时钟之前启用时钟供应通过软件状态。

CTSQ[2:0]位（控制传输阶段）

在主机控制器模式下，CTSQ[2:0]位的读取值无效。

有效位（USB请求接收）

在主机控制器模式下，VALID位的读取值无效。

DVSQ[2:0]位（设备状态）

DVSQ[2:0]位由USB总线复位初始化。在主机控制器模式下，读取的值无效。

BRDY位（缓冲区就绪中断状态）

BRDY位指示BRDY中断状态。

当USBFS在至少一个启用了BRDY中断(BRDYENB.PIPEnBRDYE=1)的管道上检测到BRDY中断状态(PIPEnBRDY=1 n=0到9)时，将BRDY位设置为1。

有关导致PIPEnBRDY状态被断言的条件，请参见第28.3.3.1节，BRDY中断。

USBFS将BRDY位设置为0，当软件将0写入与PIPEnBRDYE位设置为1。即使软件向该位写入0，BRDY位也不能设置为0。

NRDY位（缓冲区未就绪中断状态）

当与设置为1的PIPEnNRDYE位（n=0至9）相关的PIPENRDY位（当USBFS检测软件启用NRDY中断输出的管道中的至少一个管道中的NRDY中断状态）。

有关导致PIPEnNRDY状态被断言的条件，请参见第28.3.3.2节，NRDY中断。

USBFS将NRDY位设置为0，当软件将0写入与PIPEnNRDYE位设置为1。即使软件向该位写入0，NRDY位也不能设置为0。

BEMP位（缓冲区空中断状态）

BEMP位指示BEMP中断状态。

当USBFS在至少一个启用了BEMP中断(BEMPENB.PIPEnBEMPE=1)的管道上检测到BEMP中断状态(PIPEnBEMP=1 n=0到9)时，将BEMP位设置为1。

有关导致PIPEnBEMP状态被断言的条件，请参阅第28.3.3.3节，BEMP中断。

USBFS将BEMP位设置为0，当软件将0写入与PIPEnBEMPE位设置为1。在软件中将0写入BEMP位不会清除该位。

CTRT位（控制传输阶段转换中断状态）

在设备控制器模式下，当检测到控制传输阶段发生变化时，USBFS会更新CTSQ[2:0]位的值并将CTRT位设置为1。当产生控制传输阶段转换中断时，在USBFS检测到下一个控制传输阶段转换之前清除CTRT位。

在主机控制器模式下从CTRT位读取的值无效。

DVST bit (Device State Transition Interrupt Status)

In device controller mode, the USBFS updates the value of the DVSQ[2:0] bits and sets the DVST bit to 1 when detecting a change in the device state. When a device state transition interrupt is generated, clear the DVST bit before the USBFS detects the next device state transition.

Values read from the DVST bit in host controller mode are invalid.

SOFR bit (Frame Number Refresh Interrupt Status)

In host controller mode, the USBFS sets the SOFR bit to 1 when updating the frame number (when the DVSTCTR0.UACT bit is set to 1 by software). An SOFR interrupt is detected every 1 ms.

In device controller mode, the USBFS sets the SOFR bit to 1 when updating the frame number. An SOFR interrupt is detected every 1 ms.

The USBFS can detect an SOFR interrupt through the internal interpolation function even when a corrupted SOF packet is received from the USB host.

RESM bit (Resume Interrupt Status)

In device controller mode, the USBFS sets the RESM bit to 1 when detecting the falling edge of the signal on the USB_DP pin in the suspended state (DVSQ[2:0] = 1xxb). Values read from the RESM bit in host controller mode are invalid.

VBINT bit (VBUS Interrupt Status)

The USBFS sets the VBINT bit to 1 when detecting a level change (high to low or low to high) in the USB_VBUS pin input value. The USBFS sets the VBSTS bit to indicate the USB_VBUS pin input value. When a VBUS interrupt is generated, eliminate transient elements by reading the VBSTS bit at least three times through software processing and check that the values read are the same.

28.2.14 Interrupt Status Register 1 (INTSTS1)

Address(es): USBFS.INTSTS1 4009 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PDDETINT0	PDDET0 Detection Interrupt Status	0: PDDET0 detection interrupts are not generated 1: PDDET0 detection interrupts are generated.	R/W *1
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SACK	Setup Transaction Normal Response Interrupt Status	0: SACK interrupts are not generated 1: SACK interrupts are generated.	R/W *1
b5	SIGN	Setup Transaction Error Interrupt Status	0: SIGN interrupts are not generated 1: SIGN interrupts are generated.	R/W *1
b6	EOFERR	EOF Error Detection Interrupt Status	0: EOFERR interrupts are not generated 1: EOFERR interrupts are generated.	R/W *1
b10 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	ATTCH	ATTCH Interrupt Status	0: ATTCH interrupts are not generated 1: ATTCH interrupts are generated.	R/W *1
b12	DTCH	USB Disconnection Detection Interrupt Status	0: DTCH interrupts are not generated. 1: DTCH interrupts are generated.	R/W *1
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

DVST位（设备状态转换中断状态）

在设备控制器模式下，USBFS在检测到设备状态发生变化时更新DVSQ[2:0]位的值并将DVST位设置为1。当产生器件状态转换中断时，在USBFS检测到下一个器件状态转换之前清零DVST位。

在主机控制器模式下从DVST位读取的值无效。

SOFR位（帧号刷新中断状态）

在主机控制器模式下，USBFS在更新帧号时将SOFR位设置为1（当DVSTCTR0.UACT位由软件设置为1）。每1ms检测一次SOFR中断。

在设备控制器模式下，USBFS在更新帧号时将SOFR位设置为1。每1ms检测一次SOFR中断。

即使从USB主机接收到损坏的SOF数据包，USBFS也可以通过内部插值功能检测SOFR中断。

RESM位（恢复中断状态）

在设备控制器模式下，USBFS在检测到信号的下降沿时将RE SM位设置为1
USB_DP引脚处于挂起状态(DVSQ[2:0]=1xxb)。在主机控制器模式下从RESM位读取的值无效。

VBINT位（VBUS中断状态）

当检测到USB_VBUS引脚输入值的电平变化（从高到低或从低到高）时，USBFS将VBINT位设置为1。USBFS设置VBSTS位以指示USB_VBUS引脚输入值。当产生VBUS中断时，通过软件处理至少3次读取VBSTS位来消除瞬态元素，并检查读取的值是否相同。

28.2.14 中断状态寄存器1(INTSTS1)

Address(es): USBFS.INTSTS1 4009 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PDDETINT0	PDDET0检测中断状态	0：不产生PDDET0检测中断1：产生PDDET0检测中断。	R/W *1
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SACK	设置事务正常响应中断状态	0：不产生SACK中断1：产生SACK中断。	R/W *1
b5	SIGN	设置事务错误中断状态	0：不产生SIGN中断1：产生SIGN中断。	R/W *1
b6	EOFERR	EOF错误检测中断状态	0：不产生EOFERR中断1：产生EOFERR中断。	R/W *1
b10 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11	ATTCH	ATTCH中断状态	0：不产生ATTCH中断1：产生ATTCH中断。	R/W *1
b12	DTCH	USB断线检测中断Status	0：不产生DTCH中断。1：产生DTCH中断。	R/W *1
b13	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	BCHG	USB Bus Change Interrupt Status*2	0: BCHG interrupts are not generated 1: BCHG interrupts are generated.	R/W *1
b15	OVRCR	Overcurrent Input Change Interrupt Status*2	0: OVRCR interrupts are not generated 1: OVRCR interrupts are generated.	R/W *1

Note 1. To clear the bits in INTSTS1, write 0 only to the bits to be cleared. Write 1 to the other bits.
Note 2. The USBFS detects a change in the status in the OVRCR or BCHG bit even when the clock supply is stopped (SYSCFG.SCKE = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply (SYSCFG.SCKE = 1) before clearing the status through software. No other interrupts can be detected while the clock supply is stopped (SYSCFG.SCKE bit = 0).

INTSTS1 is used to confirm the status of each interrupt in host controller mode. Only enable the status change interrupts indicated in the bits in INTSTS1 in host controller mode.

PDDETINTE0 bit (PDDET0 Detection Interrupt Status)

The PDDETINT0 bit indicates the status of the portable device detection interrupt in host controller mode. This bit is set to 1 when the USBFS detects a level change (high to low or low to high) in the input value to the VDPDET pin of the USB physical layer transceiver (PHY). The USBFS sets the PDDETSTS0 bit to indicate the VDPDET input value. When the PDDETINT interrupt is generated, eliminate transient elements by reading the PDDETSTS0 bit at least three times through software processing and check that the values read are the same.

SACK bit (Setup Transaction Normal Response Interrupt Status)

The SACK bit indicates the status of the setup transaction normal response interrupt in host controller mode.

The USBFS detects the SACK interrupt and sets this bit to 1 when an ACK response is returned from the peripheral device during the setup transactions issued by the USBFS. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

Values read from the SACK bit in device controller mode are invalid.

SIGN bit (Setup Transaction Error Interrupt Status)

The SIGN bit indicates the status of the setup transaction error interrupt in host controller mode.

The USBFS detects the SIGN interrupt and sets this bit to 1 when an ACK response is not returned from the peripheral device three consecutive times during the setup transactions issued by the USBFS. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions:

- Timeout is detected by the USBFS when the peripheral device has returned no response
- A corrupted ACK packet is received
- A handshake other than ACK (NAK, NYET, or STALL) is received.

Values read from the SIGN bit in device controller mode are invalid.

EOFERR bit (EOF Error Detection Interrupt Status)

The EOFERR bit indicates the status of the EOFERR interrupt in host controller mode.

The USBFS detects the EOFERR interrupt and sets this bit to 1 on detecting that communication did not complete at the EOF2 timing defined in the USB 2.0 specification. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

After detecting the EOFERR interrupt, the USBFS controls the hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt was detected to 0
- Puts the port in which the EOFERR interrupt occurred into the idle state.

Software must terminate all pipes in which communications are currently being carried out and re-enumerate the USB port.

Bit	Symbol	位名称	Description	R/W
b14	BCHG	USB总线更改中断状态*2	0：不产生BCHG中断1：产生BCHG中断。	R/W *1
b15	OVRCR	过流输入变化中断 Status*2	0：不产生OVRCR中断1：产生OVRCR中断。	R/W *1

Note 1. 要清除INTSTS1中的位，只需将0写入要清除的位。将1写入其他位。
Note 2. 即使在停止提供时钟（SYSCFG.SCKE=0）时，USBFS也会检测到OVRCR或BCHG位的状态变化，并在相关的中断请求位为1时请求中断。启用时钟提供（SYSCFG.SCKE=1)在通过软件清除状态之前。停止提供时钟（SYSCFG.SCKE位=0）时，不会检测到其他中断。

INTSTS1用于确认主机控制器模式下每个中断的状态。仅在主机控制器模式下启用INTSTS1位中指示的状态更改中断。

PDDETINTE0位（PDDET0检测中断状态）

PDDETINT0位指示主机控制器模式下便携式设备检测中断的状态。当USBFS检测到USB物理层收发器(PHY)的VDPDET引脚的输入值发生电平变化（从高到低或从低到高）时，该位设置为1。USBFS设置PDDETSTS0位以指示VDPDET输入值。当产生PDDETINT中断时，通过软件处理至少3次读取PDDETSTS0位来消除瞬态元素，并检查读取的值是否相同。

SACK位（设置事务正常响应中断状态）

SACK位指示主机控制器模式下设置事务正常响应中断的状态。

在USBFS发出的设置事务期间，当外围设备返回ACK响应时，USBFS检测到SACK中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

在设备控制器模式下从SACK位读取的值无效。

SIGN位（设置事务错误中断状态）

SIGN位指示主机控制器模式下设置事务错误中断的状态。

在USBFS发出的设置事务期间，如果连续3次未从外围设备返回ACK响应，USBFS检测到SIGN中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

当三个连续的设置事务发生以下任何响应条件时，USBFS检测到SIGN中断：

- 当外围设备没有返回响应时，USBFS检测到超时
- 收到损坏的ACK数据包
- 收到除ACK（NAK、NYET或STALL）以外的握手。

在设备控制器模式下从SIGN位读取的值无效。

EOFERR位（EOF错误检测中断状态）

EOFERR位指示主机控制器模式下EOFERR中断的状态。

USBFS检测到EOFERR中断并在检测到通信未完成时将该位设置为1
USB2.0规范中定义的EOF2时序。如果相关的中断使能位由软件设置为1，则
USBFS产生中断。

检测到EOFERR中断后，USBFS对硬件进行如下控制，而不考虑相关的中断使能位设置：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将发生EOFERR中断的端口置于空闲状态。

软件必须终止当前正在执行通信的所有管道并重新枚举USB端口。

Values read from the EOFERR bit in device controller mode are invalid.

ATTCH bit (ATTCH Interrupt Status)

The ATTCH bit indicates the status of USB attach detection interrupts in host controller mode.

The USBFS detects the ATTCH interrupt and sets this bit to 1 on detecting a J- or K-state on the full- or low-speed signal level for 2.5 µs. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects the ATTCH interrupt on any of the following conditions:

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs.

Values read from the ATTCH bit in device controller mode are invalid.

DTCH bit (USB Disconnection Detection Interrupt Status)

The DTCH bit indicates the status of USB disconnection detection interrupts in host controller mode.

The USBFS detects the DTCH interrupt and sets this bit to 1 on detecting a USB bus detach event. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects bus detach events based on the USB 2.0 specification.

After detecting the DTCH interrupt, the USBFS controls hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt was detected to 0
- Puts the port in which the DTCH interrupt is generated into the idle state.

Software must terminate all pipes in which communications are currently being carried out and invoke the wait state for attaching to the USB port (waiting for ATTCH interrupt generation).

Values read from the DTCH flag in device controller mode are invalid.

BCHG bit (USB Bus Change Interrupt Status)

The BCHG bit indicates the status of USB bus change interrupts in host controller mode.

The USBFS detects the BCHG interrupt and sets this bit to 1 when a change in the full- or low-speed signal level occurs on the USB port. This includes any change from J-state, K-state, or SE0 to J-state, K-state, or SE0. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS sets the LNST[1:0] bits to indicate the current input state of the USB port. When a BCHG interrupt is generated, eliminate transient elements by repeat reading the LNST[1:0] bits by software until the same value is read at least three times.

Change in the USB bus state can be detected while the internal clock is stopped.

Values read from the BCHG flag in device controller mode are invalid.

OVRCR bit (Overcurrent Input Change Interrupt Status)

The OVRCR bit indicates the status of the USB_OVRCURA and USB_OVRCURB input pin change interrupts.

The USBFS detects the OVRCR interrupt and sets this bit to 1 when a change (high to low or low to high) occurs in at least one of the input values to the USB_OVRCURA and USB_OVRCURB pins. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

在设备控制器模式下从EOFERR位读取的值无效。

ATTCH位（ATTCH中断状态）

ATTCH位指示主机控制器模式下USB连接检测中断的状态。

USBFS检测到ATTCH中断，并在检测到全速或低速信号电平上的JorK状态持续2.5µs时将该位设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS在以下任何条件下检测ATTCH中断：

- K-state、SE0或SE1变为J-state，J-state持续2.5µs
- J-state、SE0或SE1变为K-state，K-state持续2.5µs。

在设备控制器模式下从ATTCH位读取的值无效。

DTCH位（USB断线检测中断状态）

DTCH位指示主机控制器模式下USB断开检测中断的状态。

USBFS检测到DTCH中断并在检测到USB总线分离事件时将该位设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS根据USB2.0规范检测总线分离事件。

检测到DTCH中断后，USBFS对硬件进行如下控制，而不管相关的中断使能位设置如何：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将产生DTCH中断的端口置于空闲状态。

软件必须终止当前正在执行通信的所有管道并调用等待状态以连接到USB端口（等待ATTCH中断生成）。

在设备控制器模式下从DTCH标志读取的值无效。

BCHG位（USB总线更改中断状态）

BCHG位指示主机控制器模式下USB总线更改中断的状态。

当USB端口上发生全速或低速信号电平变化时，USBFS检测到BCHG中断并将该位设置为1。这包括从J-state、K-state或SE0到J-state、K-state或SE0的任何更改。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS设置LNST[1:0]位以指示USB端口的当前输入状态。当产生BCHG中断时，通过软件重复读取LNST[1:0]位来消除瞬态元素，直到至少读取3次相同的值。

当内部时钟停止时，可以检测到USB总线状态的变化。

在设备控制器模式下从BCHG标志读取的值无效。

OVRCR位（过流输入变化中断状态）

OVRCR位指示USB_OVRCURA和USB_OVRCURB输入引脚变化中断的状态。

当USB_OVRCURA和USB_OVRCURB引脚的至少一个输入值发生变化（从高到低或从低到高）时，USBFS检测到OVRCR中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

28.2.15 BRDY Interrupt Status Register (BRDYSTS)

Address(es): USBFS.BRDYSTS 4009 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BRDY	BRDY Interrupt Status for Pipe 0*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b1	PIPE1BRDY	BRDY Interrupt Status for Pipe 1*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b2	PIPE2BRDY	BRDY Interrupt Status for Pipe 2*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b3	PIPE3BRDY	BRDY Interrupt Status for Pipe 3*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b4	PIPE4BRDY	BRDY Interrupt Status for Pipe 4*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b5	PIPE5BRDY	BRDY Interrupt Status for Pipe 5*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b6	PIPE6BRDY	BRDY Interrupt Status for Pipe 6*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b7	PIPE7BRDY	BRDY Interrupt Status for Pipe 7*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b8	PIPE8BRDY	BRDY Interrupt Status for Pipe 8*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b9	PIPE9BRDY	BRDY Interrupt Status for Pipe 9*2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated by the bits in BRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

Note 2. When the SOFCFG.BRDYM bit is set to 0, clear the BRDY interrupts before accessing the FIFO.

28.2.16 NRDY Interrupt Status Register (NRDYSTS)

Address(es): USBFS.NRDYSTS 4009 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0NRDY	NRDY Interrupt Status for Pipe 0	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b1	PIPE1NRDY	NRDY Interrupt Status for Pipe 1	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b2	PIPE2NRDY	NRDY Interrupt Status for Pipe 2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b3	PIPE3NRDY	NRDY Interrupt Status for Pipe 3	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1

28.2.15 BRDY中断状态寄存器(BRDYSTS)

Address(es): USBFS.BRDYSTS 4009 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BRDY	管道0*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b1	PIPE1BRDY	管道1*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b2	PIPE2BRDY	管道2*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b3	PIPE3BRDY	管道3*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b4	PIPE4BRDY	管道4*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b5	PIPE5BRDY	管道5*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b6	PIPE6BRDY	管道6*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b7	PIPE7BRDY	管道7*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b8	PIPE8BRDY	管道8*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b9	PIPE9BRDY	管道9*2的BRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当SOFCFG.BRDYM位设置为0时，要清除BRDYSTS中位指示的状态，只需将0写入要清除的位。将1写入其他位。

Note 2. 当SOFCFG.BRDYM位设置为0时，在访问FIFO之前清除BRDY中断。

28.2.16 NRDY中断状态寄存器(NRDYSTS)

Address(es): USBFS.NRDYSTS 4009 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0NRDY	管道0的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b1	PIPE1NRDY	管道1的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b2	PIPE2NRDY	管道2的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b3	PIPE3NRDY	管道3的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1

Bit	Symbol	Bit name	Description	R/W
b4	PIPE4NRDY	NRDY Interrupt Status for Pipe 4	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b5	PIPE5NRDY	NRDY Interrupt Status for Pipe 5	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b6	PIPE6NRDY	NRDY Interrupt Status for Pipe 6	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b7	PIPE7NRDY	NRDY Interrupt Status for Pipe 7	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b8	PIPE8NRDY	NRDY Interrupt Status for Pipe 8	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b9	PIPE9NRDY	NRDY Interrupt Status for Pipe 9	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated by the bits in NRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

28.2.17 BEMP Interrupt Status Register (BEMPSTS)

Address(es): USBFS.BEMPSTS 4009 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMP	PIPE8BEMP	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	PIPE3BEMP	PIPE2BEMP	PIPE1BEMP	PIPE0BEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BEMP	BEMP Interrupt Status for Pipe 0	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b1	PIPE1BEMP	BEMP Interrupt Status for Pipe 1	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b2	PIPE2BEMP	BEMP Interrupt Status for Pipe 2	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b3	PIPE3BEMP	BEMP Interrupt Status for Pipe 3	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b4	PIPE4BEMP	BEMP Interrupt Status for Pipe 4	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b5	PIPE5BEMP	BEMP Interrupt Status for Pipe 5	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b6	PIPE6BEMP	BEMP Interrupt Status for Pipe 6	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b7	PIPE7BEMP	BEMP Interrupt Status for Pipe 7	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b8	PIPE8BEMP	BEMP Interrupt Status for Pipe 8	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b9	PIPE9BEMP	BEMP Interrupt Status for Pipe 9	0: Interrupts are not generated 1: Interrupts are generated.	R/W *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated by the bits in BEMPSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

Bit	Symbol	位名称	Description	R/W
b4	PIPE4NRDY	管道4的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b5	PIPE5NRDY	管道5的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b6	PIPE6NRDY	管道6的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b7	PIPE7NRDY	管道7的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b8	PIPE8NRDY	管道8的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b9	PIPE9NRDY	管道9的NRDY中断状态	0：不产生中断1：产生中断。	R/W *1
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 要清除NRDYSTS中的位指示的状态，只需将0写入要清除的位。将1写入其他位。

28.2.17 BEMP中断状态寄存器(BEMPSTS)

Address(es): USBFS.BEMPSTS 4009 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMP	PIPE8BEMP	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	PIPE3BEMP	PIPE2BEMP	PIPE1BEMP	PIPE0BEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BEMP	管道0的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b1	PIPE1BEMP	管道1的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b2	PIPE2BEMP	管道2的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b3	PIPE3BEMP	管道3的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b4	PIPE4BEMP	管道4的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b5	PIPE5BEMP	管道5的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b6	PIPE6BEMP	管道6的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b7	PIPE7BEMP	管道7的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b8	PIPE8BEMP	管道8的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b9	PIPE9BEMP	管道9的BEMP中断状态	0：不产生中断1：产生中断。	R/W *1
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 要清除BEMPSTS中的位指示的状态，只需将0写入要清除的位。将1写入其他位。

28.2.18 Frame Number Register (FRMNUM)

Address(es): USBFS.FRMNUM 4009 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FRNM[10:0]	Frame Number	Latest frame number	R
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	CRCE	Receive Data Error	0: No error 1: An error occurred.	R/W*1
b15	OVRN	Overrun/Underrun Detection Status	0: No error 1: An error occurred.	R/W*1

Note 1. To clear the status, write 0 only to the bits to be cleared. Write 1 to the other bits.

FRNM[10:0] bits (Frame Number)

The FRNM[10:0] bits indicate the latest frame number for the USBFS after issuing of an SOF packet every 1 ms or writing to the FRNM[10:0] bits at the SOF packet reception.

CRCE bit (Receive Data Error)

The CRCE bit is set to 1 when a CRC error or bit stuffing error occurs during isochronous transfer. On detecting a CRC error in host controller mode, the USBFS generates an internal NRDY interrupt.

To clear the CRCE bit, write 0 to it while writing 1 to the other bits in the FRMNUM register.

OVRN bit (Overrun/Underrun Detection Status)

The OVRN bit is set to 1 when an overrun or underrun error occurs during isochronous transfer. To clear the bit, write 0 to it while writing 1 to the other bits in the FRMNUM register.

In host controller mode, the OVRN bit is set to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the time to issue an OUT token comes before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the time to issue an IN token comes when no FIFO buffer planes are empty.

In device controller mode, the OVRN bit is set to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the IN token is received before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the OUT token is received when no FIFO buffer planes are empty.

28.2.18 帧号寄存器(FRMNUM)

Address(es): USBFS.FRMNUM 4009 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	FRNM[10:0]	帧号	最新帧号	R
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	CRCE	接收数据错误	0：无错误1：发生错误。	R/W*1
b15	OVRN	OverrunUnderrun检测状态	0：无错误1：发生错误。	R/W*1

Note 1. 要清除状态，只向要清除的位写入0。将1写入其他位。

FRNM[10:0]位（帧号）

FRNM[10:0]位指示每1ms发出SOF数据包或在SOF数据包接收时写入FRNM[10:0]位后USBFS的最新帧号。

CRCE位（接收数据错误）

当同步传输期间发生CRC错误或位填充错误时，CRCE位设置为1。在主机控制器模式下检测到CRC错误时，USBFS会生成内部NRDY中断。

要清除CRCE位，请向其写入0，同时向FRMNUM寄存器中的其他位写入1。

OVRN位（溢出欠载检测状态）

当同步传输期间发生溢出或欠载错误时，OVRN位设置为1。要清除该位，请向其写入0，同时向FRMNUM寄存器中的其他位写入1。

在主机控制器模式下，OVRN位在以下任一条件下设置为1：

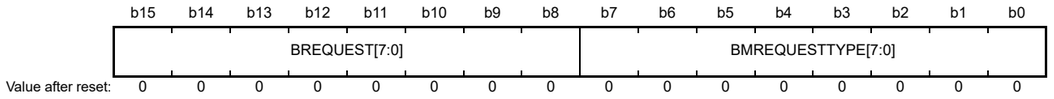
- 对于传输同步管道，发出OUT令牌的时间出现在所有传输数据写入FIFO缓冲区之前
- 对于接收同步管道，在没有FIFO缓冲区平面为空时发出IN令牌。

在设备控制器模式下，OVRN位在以下任一条件下设置为1：

- 对于传输同步管道，在所有传输数据写入FIFO缓冲区之前接收到IN令牌
- 对于接收同步管道，当没有FIFO缓冲区平面为空时接收OUT令牌。

28.2.19 USB Request Type Register (USBREQ)

Address(es): USBFS.USBREQ 4009 0054h



Bit	Symbol	Bit name	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	Request Type	These bits store the USB request bmRequestType value	R/W*1
b15 to b8	BREQUEST[7:0]	Request	These bits store the USB request bRequest value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are read/write.

USBREQ stores setup requests for control transfers.

In device controller mode, the USBREQ stores the received values of bRequest and bmRequestType. In host controller mode, it sets the bRequest and bmRequestType values to be transmitted.

USBREQ is initialized by a USB bus reset.

BMREQUESTTYPE[7:0] bits (Request Type)

The BMREQUESTTYPE[7:0] bits hold the bmRequestType value of USB requests.

- In host controller mode:
  Set these bits to the value of the USB request data in the setup transactions for transmission. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in the setup transactions for reception. Writing to these bits has no effect.

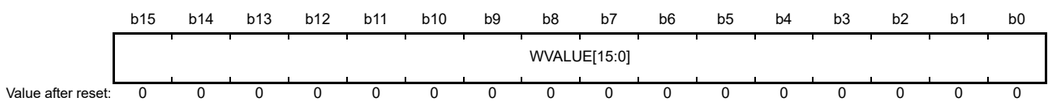
BREQUEST[7:0] bits (Request)

The BREQUEST[7:0] bits store the bRequest value of the USB request.

- In host controller mode:
  Set these bits to the value of the USB request data in setup transmission transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in the setup transactions for reception. Writing to these bits has no effect.

28.2.20 USB Request Value Register (USBVAL)

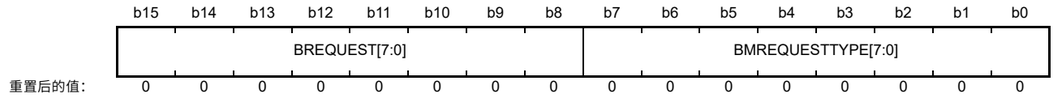
Address(es): USBFS.USBVAL 4009 0056h



Bit	Symbol	Bit name	Description	R/W
b15 to b0	WVALUE[15:0]	Value	These bits store the USB request wValue value	R/W*1

28.2.19 USB请求类型寄存器(USBREQ)

Address(es): USBFS.USBREQ 4009 0054h



Bit	Symbol	位名称	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	请求类型	这些位存储USB请求bmRequestType值	R/W*1
b15 to b8	BREQUEST[7:0]	Request	这些位存储USB请求bRequest值	R/W*1

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位是读写的。

USBREQ存储控制传输的设置请求。

在设备控制器模式下，USBREQ存储接收到的bRequest和bmRequestType值。在主机控制器模式下，它设置要传输的bRequest和bmRequestType值。

USBREQ由USB总线复位初始化。

BMREQUESTTYPE[7:0]位（请求类型）

BMREQUESTTYPE[7:0]位保存USB请求的bmRequestType值。

- 在主机控制器模式下：
  将这些位设置为用于传输的设置事务中的USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示用于接收的设置事务中的USB请求数据的值。写入这些位无效。

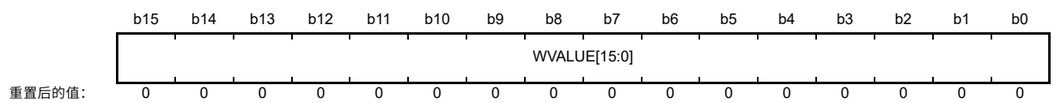
BREQUEST[7:0]位（请求）

BREQUEST[7:0]位存储USB请求的bRequest值。

- 在主机控制器模式下：
  在设置传输事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示用于接收的设置事务中的USB请求数据的值。写入这些位无效。

28.2.20 USB请求值寄存器(USBVAL)

Address(es): USBFS.USBVAL 4009 0056h



Bit	Symbol	位名称	Description	R/W
b15 to b0	WVALUE[15:0]	Value	这些位存储USB请求wValue值	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write.

In device controller mode, USBVAL stores the received value of wValue. In host controller mode, it is set to the wValue value to be transmitted is set.

USBVAL is initialized by a USB bus reset.

WVALUE[15:0] bits (Value)

The WVALUE[15:0] bits store the wValue value of the USB request.

- In host controller mode:
  Set these bits to the wValue value of USB requests in the setup transactions for transmission. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wValue value of USB requests in the setup transactions for reception. Writing to these bits has no effect.

28.2.21 USB Request Index Register (USBINDX)

Address(es): USBFS.USBINDX 4009 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WINDEX[15:0]	Index	These bits store the USB request wIndex value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write.

USBINDX stores setup requests for control transfers.

In device controller mode, the USBINDX stores the received wIndex value. In host controller mode, the USBINDX sets the wIndex value to be transmitted.

USBINDX is initialized by a USB bus reset.

WINDEX[15:0] bits (Index)

The WINDEX[15:0] bits hold the value of a USB request.

- In host controller mode:
  Set these bits to the wIndex value of USB requests in the setup transactions for transmission. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wIndex value of USB requests in the setup transactions for reception. Writing to these bits has no effect.

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写的。

在设备控制器模式下，USBVAL存储接收到的wValue值。在主机控制器模式下，它被设置为要传输的wValue值。

USBVAL由USB总线复位初始化。

WVALUE[15:0]位（值）

WVALUE[15:0]位存储USB请求的wValue值。

- 在主机控制器模式下：
  将这些位设置为传输设置事务中USB请求的wValue值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求的wValue值。写入这些位无效。

28.2.21 USB请求索引寄存器(USBINDX)

Address(es): USBFS.USBINDX 4009 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WINDEX[15:0]	Index	这些位存储USB请求wIndex值	R/W*1

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写的。

USBINDX存储控制传输的设置请求。

在设备控制器模式下，USBINDX存储接收到的wIndex值。在主机控制器模式下，USBINDX设置要传输的wIndex值。

USBINDX由USB总线复位初始化。

WINDEX[15:0]位（索引）

WINDEX[15:0]位保存USB请求的值。

- 在主机控制器模式下：
  将这些位设置为传输设置事务中USB请求的wIndex值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求的wIndex值。写入这些位无效。

28.2.22 USB Request Length Register (USBLENG)

Address(es): USBFS.USBLENG 4009 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	These bits store the USB request wLength value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write.

USBLENG stores setup requests for control transfers.

In device controller mode, the USBLENG stores the received value of wLength. In host controller mode, the USBLENG sets the value of wLength to be transmitted.

USBLENG is initialized by a USB bus reset.

WLENTUH[15:0] bits (Length)

The WLENTUH[15:0] bits hold the wLength value of a USB request.

- In host controller mode:
  Set these bits to the wLength value in USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wLength value in USB requests received in reception setup transactions. Writing to the bits has no effect.

28.2.23 DCP Configuration Register (DCPCFG)

Address(es): USBFS.DCPCFG 4009 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DIR	Transfer Direction*1	0: Data receiving direction 1: Data transmitting direction.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Pipe kept open at the end of transfer 1: Pipe disabled at the end of transfer.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set this bit while the PID is NAK. Before setting this bit, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

DIR bit (Transfer Direction)

In host controller mode, the DIR bit sets the transfer direction of the data stage and status stage for control transfers. In

28.2.22 USB请求长度寄存器(USBLENG)

Address(es): USBFS.USBLENG 4009 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	这些位存储USB请求wLength值	R/W*1

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写的。

USBLENG存储控制传输的设置请求。

在设备控制器模式下，USBLENG存储接收到的wLength值。在主机控制器模式下，USBLENG设置要传输的wLength的值。

USBLENG由USB总线复位初始化。

WLENTUH[15:0]位（长度）

WLENTUH[15:0]位保存USB请求的wLength值。

- 在主机控制器模式下：
  在传输设置事务中将这些位设置为USB请求中的wLength值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示在接收设置事务中收到的USB请求中的wLength值。写入位无效。

28.2.23 DCP配置寄存器(DCPCFG)

Address(es): USBFS.DCPCFG 4009 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称		Description	R/W
b3 to b0	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b4	DIR	转移方向	*1	0：数据接收方向1：数据发送方向。	R/W
b6, b5	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b7	SHTNAK	传输结束时禁用管道	*1	0：管道在传输结束时保持打开1：管道在传输结束时禁用。	R/W
b15 to b8	—	Reserved		这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在PID为NAK时设置该位。在设置该位之前，请检查DCPCTR.PBUSY位是否为0，然后更改DCPCTR.PID[1:0]位用于DCP从BUF到NAK。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。

DIR位（传输方向）

在主机控制器模式下，DIR位设置控制传输的数据阶段和状态阶段的传输方向。在

device controller mode, set the DIR bit to 0.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change PID to NAK on transfer end when the selected pipe is receiving. It is only valid when the selected pipe is receiving.

When the SHTNAK bit is 1, the USBFS changes the DCPCTR.PID[1:0] bits for the DCP to NAK on determining that a transfer has ended. The USBFS determines that the transfer has ended on the following condition:

- A short packet, including a zero-length packet, is successfully received.

28.2.24 DCP Maximum Packet Size Register (DCPMAXP)

Address(es): USBFS.DCPMAXP 4009 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	MXPS[6:0]	Maximum Packet Size*1	These bits set the maximum amount of data (maximum packet size) in payloads for the DCP. b6 b0 0 0 0 1 0 0 0: 8 bytes 0 0 1 0 0 0 0: 16 bytes 0 0 1 1 0 0 0: 24 bytes 0 1 0 0 0 0 0: 32 bytes 0 1 0 1 0 0 0: 40 bytes 0 1 1 0 0 0 0: 48 bytes 0 1 1 1 0 0 0: 56 bytes 1 0 0 0 0 0 0: 64 bytes 1 0 0 1 0 0 0: 72 bytes 1 0 1 0 0 0 0: 80 bytes 1 0 1 1 0 0 0: 88 bytes 1 1 0 0 0 0 0: 96 bytes 1 1 0 1 0 0 0: 104 bytes 1 1 1 0 0 0 0: 112 bytes 1 1 1 1 0 0 0: 120 bytes Other settings are prohibited.	R/W
b11 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select*2	b15 b12 0 0 0 0: Address 0000 0 0 0 1: Address 0001 0 0 1 0: Address 0010 0 0 1 1: Address 0011 0 1 0 0: Address 0100 0 1 0 1: Address 0101 Other settings are prohibited.	R/W

Note 1. Only set the MXPS[6:0] bits while PID is NAK. Before setting these bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required. After modifying the MXPS[6:0] bits and the DCP is set to the CURPIPE[3:0] bits in a port select register, clear the buffer by setting the BCLR bit the port control register to 1.

Note 2. Only set the DEVSEL[3:0] bits while PID is NAK and the DCPCTR.SUREQ bit is 0. Before setting these bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

MXPS[6:0] bits (Maximum Packet Size*1)

The MXPS[6:0] bits specify the maximum data payload (maximum packet size) for the DCP. The initial value is 40h (64 bytes). Set the bits to a USB 2.0-compliant value. Do not write to the FIFO buffer or set PID = BUF while MXPS[6:0] is set to 0.

设备控制器模式，将DIR位设置为0。

SHTNAK位（传输结束时管道禁用）

SHTNAK位指定当所选管道正在接收时，是否在传输结束时将PID更改为NAK。仅在所选管道正在接收时有效。

当SHTNAK位为1时，USBFS在确定传输已结束时将DCPCR.PID[1:0]位更改为DCP为NAK。USBFS在以下条件下确定传输已结束：

- 成功接收到一个短数据包，包括一个长度为零的数据包。

28.2.24 DCP最大数据包大小寄存器(DCPMAXP)

Address(es): USBFS.DCPMAXP 4009 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
重置后的值：	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	MXPS[6:0]	最大数据包大小*1	这些位设置DCP有效载荷中的最大数据量（最大数据包大小）。b6b00001000：8字节0010000：16字节0011000：24字节0100000：32字节0101000：40字节0110000：48字节0111000：56字节1000000：64字节1001000：72字节1010000：80字节1011000：88字节1100000：96字节1101000：104字节1110000：112字节1111000：120字节禁止其他设置。	R/W
b11 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b12	DEVSEL[3:0]	Device Select*2	b15b120000：地址000000 01：地址00010010：地址0 0100011：地址00110100： 地址01000101：地址0101 禁止其他设置。	R/W

Note 1. 仅在PID为NAK时设置MXPS[6:0]位。在设置这些位之前，请检查DCPCTR.PBUSY位是否为0，然后将DCP的DCPCTR.PID[1:0]位从BUF更改为NAK。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。修改MXPS[6:0]位并将DCP设置为端口选择寄存器中的CURPIPE[3:0]位后，通过将端口控制寄存器的BCLR位设置为1来清除缓冲区。

Note 2. 仅在PID为NAK且DCPCTR.SUREQ位为0时设置DEVSEL[3:0]位。在设置这些位之前，请检查DCPCTR.PBUSY位是否为0，然后更改DCPCTR.PID[1:0]从BUF到NAK的DCP位。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。

MXPS[6:0]位（最大数据包大小*1）

MXPS[6:0]位指定DCP的最大数据有效载荷（最大数据包大小）。初始值为40h（64字节）。将这些位设置为符合USB2.0的值。当MXPS[6:0]设置为0时，不要写入FIFO缓冲区或设置PID=BUF。

DEVSEL[3:0] bits (Device Select*2)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target peripheral device for a control transfer. Set up the device address in the associated DEVADDn (n = 0 to 5) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0000b.

28.2.25 DCP Control Register (DCPCTR)

Address(es): USBFS.DCPCTR 4009 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	—	—	SUREQ CLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b2	CCPL	Control Transfer End Enable	0: Invalid 1: Control transfer completion enabled.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: DCP not used for the transaction 1: DCP in used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Monitor	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	Sets the sequence toggle bit in DCP transfers: 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1.	R/W*1
b8	SQCLR	Sequence Toggle Bit Clear*2	Clears the sequence toggle bit in DCP transfers: 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0.	R/W*1
b10, b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	SUREQCLR	SUREQ Bit Clear	Clears the SUREQ bit in host controller mode: 0: Invalid (writing 0 has no effect) 1: Clear SUREQ to 0.	R/W*1
b13, b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	SUREQ	Setup Token Transmission	Sets up token transmission in host controller mode: 0: Invalid (writing 0 has no effect) 1: Transmit setup packet.	R/W
b15	BSTS	Buffer Status	0: Buffer access disabled 1: Buffer access enabled.	R

Note 1. This bit is read as 0.
Note 2. Only set the SQSET and SQCLR bits to 1 while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits for the DCP from BUF to NAK. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

PID[1:0] bits (Response PID)

The PID[1:0] bits control the USBFS response type during control transfers.

In host controller mode, to change the PID[1:0] setting from NAK to BUF:

- When the transmitting direction is set:

DEVSEL[3:0]位（设备选择*2）

在主机控制器模式下，DEVSEL[3:0]位指定目标外围设备的地址以进行控制传输。首先在相关的DEVADDn（n=0到5）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0000b。

28.2.25 DCP控制寄存器(DCPCTR)

Address(es): USBFS.DCPCTR 4009 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	—	—	SUREQ CLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1b000：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应。	R/W
b2	CCPL	控制传输结束使能	0：无效1：控制传输完成使能。	R/W
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	PBUSY	管道忙	0：DCP不用于事务1：DCP用于事务。	R
b6	SQMON	序列切换位监视器	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置*2	设置DCP传输中的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值设置为DATA1。	R/W*1
b8	SQCLR	序列切换位清除*2	清除DCP传输中的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值清除到DATA0。	R/W*1
b10, b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11	SUREQCLR	SUEQ位清零	在主机控制器模式下清除SUREQ位：0：无效（写入0无效）1：将SUREQ清除为0。	R/W*1
b13, b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	SUREQ	设置令牌传输	在主机控制器模式下设置令牌传输：0：无效（写入0无效）1：传输设置数据包。	R/W
b15	BSTS	缓冲区状态	0：禁止缓冲区访问1：允许缓冲区访问。	R

Note 1. 该位读为0。
Note 2. 仅当PID为NAK时将SQSET和SQCLR位设置为1。在设置这些位之前，请检查PBUSY位是否为0，然后将DCP的PID[1:0]位从BUF更改为NAK。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。

PID[1:0]位（响应PID）

PID[1:0]位在控制传输期间控制USBFS响应类型。

在主机控制器模式下，要将PID[1:0]设置从NAK更改为BUF：

- 设置传输方向时：

a. Write all of the transmit data to the FIFO buffer while the DVSTCTR0.UACT bit is 1 and PID is NAK.

b. Set PID[1:0] bits to 01b (BUF).
The USBFS then executes the OUT transaction.

- When the receiving direction is set:

a. Check that the FIFO buffer is empty (or empty the buffer) while the DVSTCTR0.UACT bit is 1 and PID is NAK.

- Set PID[1:0] bits to 01b (BUF).
The USBFS then executes the IN transaction.

The USBFS changes the PID[1:0] setting as follows:

- When the PID[1:0] bits are set to BUF (01b) by software and the USBFS has received data exceeding MaxPacketSize, the USBFS sets the PID[1:0] to STALL (11b)
- When a reception error, such as a CRC error, is detected three times consecutively, the USBFS sets the PID[1:0] bits to NAK (00b)
- On receiving the STALL handshake, the USBFS sets PID[1:0] to STALL (11b).

In device controller mode, the USBFS changes the PID[1:0] setting as follows:

- On receiving a setup packet, the USBFS sets PID[1:0] to NAK (00b). The USBFS then sets the INTSTS0.VALID bit to 1, and the PID[1:0] setting cannot be changed until software clears the VALID bit to 0.
- When the PID[1:0] bits are set to BUF (01b) by software and the USBFS has received data exceeding MaxPacketSize, the USBFS sets PID[1:0] to STALL (11b)
- On detecting a control transfer sequence error, the USBFS sets PID[1:0] to STALL (1xb)
- On detecting a USBFS bus reset, the USBFS sets PID[1:0] to NAK.

The USBFS does not check the PID[1:0] setting while processing a SET_ADDRESS request.

The PID[1:0] bits are initialized by a USB bus reset.

CCPL bit (Control Transfer End Enable)

In device controller mode, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed. When the bit is set to 1 by software while the associated PID[1:0] bits are set to BUF, the USBFS completes the control transfer status stage.

During control read transfers, the USBFS transmits the ACK handshake in response to the OUT transaction from the USB host. During control write or no-data control transfers, it transmits the zero-length packet in response to the IN transaction from the USB host. On detecting a SET_ADDRESS request, the USBFS operates in auto response mode from the setup stage up to status stage completion regardless of the CCPL bit setting.

The USBFS changes the CCPL bit from 1 to 0 on receiving a new setup packet. Software cannot write 1 to the bit while the INTSTS0.VALID bit is 1. The CCPL bit is initialized by a USB bus reset.

In host controller mode, always write 0 to the CCPL bit.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether DCP is used for the transaction when USBFS changes the PID[1:0] bits from BUF to NAK. The USBFS changes the PBUSY bit from 0 to 1 at the start of a USBFS transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

After PID is set to NAK by software, the value in the PBUSY bit indicates whether changes to pipe settings can proceed.

For details, see section 28.3.4.1, Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Monitor)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

The USBFS toggles the SQMON bit on successful completion of the transaction. It does not toggle the bit, however, when a DATA-PID mismatch occurs during a transfer in the receiving direction.

一个。当DVSTCTR0.UACT位为1且PID为NAK时，将所有发送数据写入FIFO缓冲区。

湾。将PID[1:0]位设置为01b(BUF)。
然后USBFS执行OUT事务。

- 设置接收方向时：

一个。在DVSTCTR0.UACT位为1且PID为NAK时检查FIFO缓冲区是否为空（或清空缓冲区）。

- 将PID[1:0]位设置为01b(BUF)。
然后USBFS执行IN事务。

USBFS更改PID[1:0]设置如下：

- 当PID[1:0]位被软件设置为BUF(01b)并且USBFS接收到的数据超过MaxPacketSize，USBFS将PID[1:0]设置为STALL(11b)
- 当连续3次检测到接收错误（例如CRC错误）时，USBFS将PID[1:0]位设置为NAK(00b)
- 在接收到STALL握手时，USBFS将PID[1:0]设置为STALL(11b)。

在设备控制器模式下，USBFS将PID[1:0]设置更改如下：

- 接收到设置数据包后，USBFS将PID[1:0]设置为NAK(00b)。然后USBFS将INTSTS0.VALID位设置为1，并且PID[1:0]设置不能更改，直到软件将VALID位清除为0。
- 当PID[1:0]位被软件设置为BUF(01b)并且USBFS接收到的数据超过MaxPacketSize，USBFS将PID[1:0]设置为STALL(11b)
- 在检测到控制传输序列错误时，USBFS将PID[1:0]设置为STALL(1xb)
- 在检测到USBFS总线复位时，USBFS将PID[1:0]设置为NAK。

USBFS在处理SET_ADDRESS请求时不检查PID[1:0]设置。

PID[1:0]位由USB总线复位初始化。

CCPL位（控制传输结束使能）

在设备控制器模式下，将CCPL位设置为1可以完成控制传输的状态阶段。
当该位由软件设置为1且相关的PID[1:0]位设置为BUF时，USBFS完成控制传输状态阶段。

在控制读取传输期间，USBFS发送ACK握手以响应来自USB主机的OUT事务。在控制写入或无数据控制传输期间，它传输零长度数据包以响应来自USB主机的IN事务。在检测到SET_ADDRESS请求时，USBFS从设置阶段到状态阶段完成以自动响应模式运行，无论CCPL位设置如何。

USBFS在接收到新的设置数据包时将CCPL位从1更改为0。当INTSTS0.VALID位为1时，软件不能向该位写入1。
CCPL位由USB总线复位初始化。

在主机控制器模式下，始终将0写入CCPL位。

PBUSY位（管道忙）

PBUSY位指示当USBFS将PID[1:0]位从BUF更改为
纳克。USBFS在所选管道的USBFS事务开始时将PBUSY位从0更改为1，并在完成一个事务时将PBUSY位从1更改为0。

在软件将PID设置为NAK后，PBUSY位中的值指示是否可以继续对管道设置进行更改。

详见28.3.4.1管道控制寄存器切换流程。

SQMON位（序列切换位监视器）

SQMON位指示DCP传输期间下一个事务的序列切换位的预期值。

USBFS在事务成功完成时切换SQMON位。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，它不会切换该位。

In device controller mode, the USBFS sets the SQMON bit to 1 (specifies DATA1 as the expected value) on successful reception of the setup packet.

In device controller mode, the USBFS does not reference this bit during IN or OUT transactions at the status stage, and it does not toggle the bit on normal completion.

SQSET bit (Sequence Toggle Bit Set*2)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR bit (Sequence Toggle Bit Clear*2)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer. The SQCLR bit is read as 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR bit (SUREQ Bit Clear)

In host controller mode, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The bit is read as 0.

If transfer stops while the SUREQ bit is set to 1 in a setup transaction, set the SUREQCLR bit to 1 by software. This is not required at the end of a normal setup transaction, because the USBFS automatically clears the SUREQ bit to 0.

Only control the SUREQ bit through the SUREQCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a bus disconnection was detected.

In device controller mode, always write 0 to this bit.

SUREQ bit (Setup Token Transmission)

In host controller mode, setting the SUREQ bit to 1 triggers the USBFS to transmit the setup packet. After completing the setup transaction process, the USBFS generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0. The USBFS also clears the SUREQ bit to 0 when software sets the SUREQCLR bit to 1.

Before setting the SUREQ bit to 1, set the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the target USB request in the setup transaction. Also check that the PID[1:0] bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not change the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is complete (SUREQ bit = 1). Write 1 to the SUREQ bit only when transmitting the setup token. Otherwise, write 0.

In device controller mode, always write 0 to this bit.

BSTS bit (Buffer Status)

The BSTS bit indicates the status of access to the DCP FIFO buffer. The meaning of this bit varies as follows depending on the CFIFOSEL.ISEL setting:

- When ISEL = 0, the bit indicates whether received data can be read from the buffer
- When ISEL = 1, the bit indicates whether transmitted data can be written to the buffer.

在设备控制器模式下，USBFS在成功接收到设置数据包时将SQMON位设置为1（指定DATA1作为预期值）。

在设备控制器模式下，USBFS在状态阶段的IN或OUT事务期间不引用该位，并且它不会在正常完成时切换该位。

SQSET位（序列切换位设置*2）

SQSET位将DATA1指定为DCP传输期间下一个事务的序列切换位的预期值。

不要同时将SQCLR和SQSET位设置为1。

SQCLR位（序列切换位清除*2）

SQCLR位将DATA0指定为DCP传输期间下一个事务的序列切换位的预期值。SQCLR位读为0。

不要同时将SQCLR和SQSET位设置为1。

SUREQCLR位（SUREQ位清零）

在主机控制器模式下，将SUREQCLR位设置为1会将SUREQ位清除为0。该位被读取为0。

如果在设置事务中将SUREQ位设置为1时传输停止，则通过软件将SUREQCLR位设置为1。在正常设置事务结束时不需要这样做，因为USBFS会自动将SUREQ位清除为0。

当DVSTCTR0.UACT位为0时，仅通过SUREQCLR位控制SUREQ位。当UACT为0时，由于检测到总线断开，通信停止或没有传输发生。

在设备控制器模式下，始终向该位写入0。

SUREQ位（设置令牌传输）

在主机控制器模式下，将SUREQ位设置为1会触发USBFS发送设置数据包。完成设置事务处理后，USBFS产生SACK或SIGN中断并将SUREQ位清零。当软件将SUREQCLR位设置为1时，USBFS也将SUREQ位清零。

在将SUREQ位设置为1之前，适当地设置DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX和USBLENG以在设置事务中传输目标USB请求。还要检查DCP的PID[1:0]位是否设置为NAK。将SUREQ位设置为1后，在设置事务完成（SUREQ位=1）之前，不要更改DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX或USBLENG。将1写入

仅在发送设置令牌时才使用SUEQ位。否则，写0。

在设备控制器模式下，始终向该位写入0。

BSTS位（缓冲区状态）

BSTS位指示访问DCPFIFO缓冲区的状态。根据CFIFOSEL.ISEL设置，该位的含义如下所示：

- 当ISEL=0时，该位指示是否可以从缓冲区中读取接收到的数据
- 当ISEL=1时，该位指示是否可以将发送的数据写入缓冲区。

28.2.26 Pipe Window Select Register (PIPESEL)

Address(es): USBFS.PIPESEL 4009 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	PIPESEL[3:0]	Pipe Window Select	b3 b0 0 0 0 0: No pipe selected 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9 Other settings are prohibited.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Set pipes 1 to 9 using the PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN registers (n = 0 to 9).

After selecting the pipe in the PIPESEL register, set the pipe functions using PIPECFG, PIPEMAXP, and PIPEPERI registers.The PIPEnCTR, PIPEnTRE, and PIPEnTRN registers can be set independently of the pipe selection in the PIPESEL register.

PIPESEL[3:0] bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number associated with the PIPECFG, PIPEMAXP, and PIPEPERI registers used for data writing and reading. Selecting a pipe number in the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI associated with the selected pipe number.

When PIPESEL[3:0] = 0000b, 0 is read from all of the bits in PIPECFG, PIPEMAXP, and PIPEPERI. Writing to these bits is invalid.

28.2.26 管道窗口选择寄存器(PIPESEL)

Address(es): USBFS.PIPESEL 4009 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	PIPESEL[3:0]	管道窗口选择	b3b00000：未选择管道000 1：管道10010：管道20011 ：管道30100：管道40101： 管道50110：管道60111：管 道71000：管道81001：管道 9禁止其他设置。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

使用PIPESEL、PIPECFG、PIPEMAXP、PIPEPERI、PIPEnCTR、PIPEnTRE和PIPEnTRN寄存器（n=0到9）设置管道1到9。

在PIPESEL寄存器中选择管道后，使用PIPECFG、PIPEMAXP和PIPEPERI寄存器设置管道功能。PIPEnCTR、PIPEnTRE和PIPEnTRN寄存器可以独立于PIPESEL寄存器中的管道选择进行设置。

PIPESEL[3:0]位（管道窗口选择）

PIPESEL[3:0]位选择与用于数据写入和读取的PIPECFG、PIPEMAXP和PIPEPERI寄存器相关的管道编号。在PIPESEL[3:0]位中选择一个管道编号允许写入和读取与所选管道编号相关的PIPECFG、PIPEMAXP和PIPEPERI。

当PIPESEL[3:0]=0000b时，从PIPECFG、PIPEMAXP和PIPEPERI中的所有位读取0。写入这些位无效。

28.2.27 Pipe Configuration Register (PIPECFG)

Address(es): USBFS.PIPECFG 4009 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number*1	These bits specify the endpoint number for the selected pipe. Setting 0000b indicates the pipe is not used.	R/W
b4	DIR	Transfer Direction*2,*3	0: Receiving direction 1: Transmitting direction.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Pipe operation continued after transfer ends 1: Pipe operation disabled after transfer ends.	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9	DBLB	Double Buffer Mode*2,*3	0: Single buffer 1: Double buffer.	R/W
b10	BFRE	BRDY Interrupt Operation Specification*2,*3	0: BRDY interrupt generated on transmitting or receiving data 1: BRDY interrupt generated on completion of reading data.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	TYPE[1:0]	Transfer Type*1	• Pipes 1 and 2 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Isochronous transfer. • Pipes 3 to 5 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Setting prohibited. • Pipes 6 to 9 b15 b14 0 0: Pipe not used 0 1: Setting prohibited 1 0: Interrupt transfer 1 1: Setting prohibited.	R/W

Note 1. Only set the TYPE[1:0], SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the USBFS changes the PID[1:0] bits to 00 (NAK), checking the PBUSY bit through software is not required.

Note 2. Only set the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through software is not required.

Note 3. To change the BFRE, DBLB, or DIR bits after completing USB communication on the selected pipe, in addition to the constraints described in Note 2., write 1 and then 0 to the PIPEnCTR.ACLRM bit continuously through software to clear the FIFO buffer assigned to the selected pipe.

PIPECFG specifies the transfer type, FIFO buffer access direction, and endpoint numbers for pipes 1 to 9. It also selects single or double buffer mode, and whether to continue or disable pipe operation at the end of transfer.

28.2.27 管道配置寄存器(PIPECFG)

Address(es): USBFS.PIPECFG 4009 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number*1	这些位指定所选管道的端点编号。设置0000b表示不使用管道。	R/W
b4	DIR	Transfer Direction*2,*3	0：接收方向1：发送方向。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	SHTNAK	管道在传输结束时禁用*1	0：传输结束后管道操作继续1：传输结束后管道操作无效。	R/W
b8	—	Reserved	该位读取为0。写入值应为0。	R/W
b9	DBLB	双缓冲模式*2 *3	0：单缓冲区1：双缓冲区。	R/W
b10	BFRE	BRDY中断操作Specification*2,*3	0：发送或接收数据时产生BRDY中断1：完成读取数据时产生BRDY中断。	R/W
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15, b14	TYPE[1:0]	Transfer Type*1	管道1和2b15b14 0 0：未使用管道 0 1：批量传输 1 0：禁止设定 1 1: Isochronous transfer. 管道3至5b15 b14 0 0：未使用管道 0 1：批量传输 1 0：禁止设定 1 1：禁止设置。 管道6至9b15 b14 0 0：未使用管道 0 1：禁止设置 1 0：中断传输 1 1：禁止设置。	R/W

Note 1. 仅在PID为NAK时设置TYPE[1:0]、SHTNAK和EPNUM[3:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果USBFS将PID[1:0]位更改为00(NAK)，则不需要通过软件检查PBUSY位。

Note 2. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置BFRE、DBLB和DIR位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则不需要通过软件检查PBUSY位。

Note 3. 要在所选管道上完成USB通信后更改BFRE、DBLB或DIR位，除了注释2中描述的约束之外，通过软件连续向PIPEnCTR.ACLRM位写入1和0，以清除分配的FIFO缓冲区到选定的管道。

PIPECFG指定管道1到9的传输类型、FIFO缓冲区访问方向和端点编号。它还选择单缓冲区或双缓冲区模式，以及在传输结束时是继续还是禁用管道操作。

EPNUM[3:0] bits (Endpoint Number*1)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe. Setting 0000b indicates the pipe is not used.

Set these bits so that the combination of the DIR and EPNUM[3:0] settings is different from those for other pipes. The EPNUM[3:0] bits can be set to 0000b for all pipes.

DIR bit (Transfer Direction*2,*3)

The DIR bit specifies the transfer direction for the selected pipe.

When software sets this bit to 0, the USBFS uses the selected pipe for receiving. When software sets this bit to 1, the USBFS uses the selected pipe for transmitting.

SHTNAK bit (Pipe Disabled at End of Transfer*1)

The SHTNAK bit specifies whether to change the PIPEnCTR.PID[1:0] bits to 00b (NAK) at the end of transfer when the selected pipe is set in the receiving direction. The bit is valid for pipes 1 to 5 in the receiving direction.

When software sets this bit to 1 for a receiving pipe, the USBFS changes the associated PIPEnCTR.PID[1:0] bits to 00b (NAK) on determining the transfer end. The USBFS determines that the transfer has ended on the following conditions:

- A short packet (including a zero-length packet) is successfully received
- The transaction counter is used and the number of packets specified for the transaction counter are successfully received.

DBLB bit (Double Buffer Mode*2,*3)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe. The bit is valid for pipes 1 to 5.

BFRE bit (BRDY Interrupt Operation Specification*2,*3)

The BFRE bit specifies the BRDY interrupt generation timing from the USBFS to the CPU for the selected pipe.

When software sets the BFRE bit to 1 and the selected pipe is receiving, the USBFS detects the transfer completion and generates the BRDY interrupt on reading the packet.

When a BRDY interrupt is generated with this setting, write 1 to the BCLR bit in the Port Control Register with software. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.

When the BFRE bit is set to 1 by software and the selected pipe is transmitting, the USBFS does not generate the BRDY interrupt. For details, see section 28.3.3.1, BRDY interrupt.

TYPE[1:0] bits (Transfer Type*1)

The TYPE[1:0] bits specify the transfer type for the pipe selected in the PIPESEL.PIPESEL[3:0] bits. Before setting PID to BUF and starting USB communication on the selected pipe, set the TYPE[1:0] bits to a value other than 00b.

EPNUM[3:0]位（端点编号*1）

EPNUM[3:0]位指定所选管道的端点号。设置0000b表示不使用管道。

设置这些位，以便DIR和EPNUM[3:0]设置的组合不同于其他管道的设置。这
对于所有管道，EPNUM[3:0]位可以设置为0000b。

DIR位（传输方向*2 *3）

DIR位指定所选管道的传输方向。

当软件将此位设置为0时，USBFS使用所选管道进行接收。当软件将该位设置为1时，
USBFS使用选定的管道进行传输。

SHTNAK位（传输结束时管道禁用*1）

SHTNAK位指定当所选管道设置为接收方向时，是否在传输结束时将PIPEnCTR.PID[1:0]位更改为00b(NAK)。该位对接收方向的管道1到5有效。

当软件将该位设置为接收管道时，USBFS在确定传输结束时将相关的PIPEnCTR.PID[1:0]位更改为00b(NAK)。USBFS在以下条件下确定传输已结束：

- 成功接收短包（包括零长度包）
- 使用事务计数器并成功接收为事务计数器指定的数据包数量。

DBLB位(双缓冲模式*2 *3)

DBLB位为所选管道使用的FIFO缓冲区选择单缓冲区模式或双缓冲区模式。该位对管道1到5有效。

BFRE位(BRDY中断操作规范*2 *3)

BFRE位为所选管道指定从USBFS到CPU的BRDY中断生成时序。

当软件将BFRE位设置为1并且所选管道正在接收时，USBFS检测到传输完成并在读取数据包时产生BRDY中断。

当使用该设置产生BRDY中断时，用软件将1写入端口控制寄存器中的BCLR位。在将1写入BCLR位之前，分配给所选管道的FIFO缓冲区不会用于接收。

当BFRE位被软件设置为1并且所选管道正在发送时，USBFS不会产生BRDY中断。有关详细信息，请参阅第28.3.3.1节，BRDY中断。

TYPE[1:0]位（传输类型*1）

TYPE[1:0]位指定在PIPESEL.PIPESEL[3:0]位中选择的管道的传输类型。在将PID设置为BUF并在所选管道上启动USB通信之前，请将TYPE[1:0]位设置为00b以外的值。

28.2.28 Pipe Maximum Packet Size Register (PIPEMAXP)

Address(es): USBFS.PIPEMAXP 4009 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0/1 *1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	MXPS[8:0]	Maximum Packet Size*2	• Pipes 1 and 2: 1 byte (001h) to 256 bytes (100h) • Pipes 3 to 5: 8 bytes (008h), 16 bytes (010h) 32 bytes (020h), 64 bytes (040h) (Bits [8:7] and [2:0] not supported.) • Pipes 6 to 9: 1 byte (001h) to 64 bytes (040h) (Bits [8:7] not supported.)	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select*3	b3 b0 0 0 0 0: Address 0000 0 0 0 1: Address 0001 0 0 1 0: Address 0010 0 0 1 1: Address 0011 0 1 0 0: Address 0100 0 1 0 1: Address 0101. Other settings are prohibited.	R/W

Note 1. The value of the MXPS[8:0] bits is 000h when no pipe is selected in the PIPESEL.PIPESEL[3:0] bits and 040h when a pipe is selected.

Note 2. Only set the MXPS[8:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through software is not required.

Note 3. Only set the DEVSEL[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the USBFS changes the PID[1:0] bits to 00 (NAK), checking the PBUSY bit through software is not required.

PIPEMAXP specifies the maximum packet size for pipes 1 to 9.

MXPS[8:0] bits (Maximum Packet Size*2)

The MXPS[8:0] bits specify the maximum data payload (maximum packet size) for the selected pipe.

Set these bits to the appropriate value for each transfer type based on the USB 2.0 specification. When MXPS[8:0] = 0, do not write to the FIFO buffer or set PID to BUF. These writes have no effect.

DEVSEL[3:0] bits (Device Select*3)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target device for USB communication. Set up the device address in the associated DEVADDn (n = 0 to 5) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0000b.

28.2.28 管道最大数据包大小寄存器(PIPEMAXP)

Address(es): USBFS.PIPEMAXP 4009 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0/1 *1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	MXPS[8:0]	最大数据包大小*2	管道1和2： 1字节(001h)到256字节(100h) 管道3到5： 8字节(008h)、16字节(010h)32字节(020h)、64字节(040h)（不支持位[8:7]和[2:0]。） 管道6到9： 1字节(001h)到64字节(040h)（不支持位[8:7]。）	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b12	DEVSEL[3:0]	Device Select*3	b3b00000：地址00000001：地址00010010：地址00100011：地址00110100：地址01000101：地址0101。 禁止其他设置。	R/W

Note 1. 当在管道中选择未选择管道时，MXPS[8：0]位的值为000H。pipesel[3：0]位和选择管道时040H。

Note 2. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置MXPS[8:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则不需要通过软件检查PBUSY位。

Note 3. 仅在PID为NAK时设置DEVSEL[3:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果USBFS将PID[1:0]位更改为00(NAK)，则不需要通过软件检查PBUSY位。

PIPEMAXP指定管道1到9的最大数据包大小。

MXPS[8:0]位（最大数据包大小*2）

MXPS[8:0]位指定所选管道的最大数据有效负载（最大数据包大小）。

根据USB2.0规范将这些位设置为每种传输类型的适当值。当MXPS[8:0]=0时，不要写入FIFO缓冲区或将PID设置为BUF。这些写入没有效果。

DEVSEL[3:0]位（设备选择*3）

在主机控制器模式下，DEVSEL[3:0]位指定USB通信的目标设备的地址。首先在相关的DEVADDn（n=0到5）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0000b。

28.2.29 Pipe Cycle Control Register (PIPEPERI)

Address(es): USBFS.PIPEPERI 4009 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	IITV[2:0] *1	Interval Error Detection Interval	Specifies the interval error detection timing for the selected pipe as the n-th power of 2 of the frame timing	R/W
b11 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	IFIS	Isochronous IN Buffer Flush	0: The buffer not flushed 1: The buffer is flushed.	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set the IITV[2:0] bits while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through software is not required.

PIPEPERI selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfers, and sets the interval error detection interval for pipes 1 to 9.

IITV[2:0] bits (Interval Error Detection Interval)

To change the IITV[2:0] bits to another value after they are set and USB communication is performed, set the PIPEnCTR.PID[1:0] bits to 00b (NAK) and then set the PIPEnCTR.ACLRM bit to 1 to initialize the interval timer.

The IITV[2:0] bits are not provided for pipes 3 to 5. Write 000b to bit positions of the IITV[2:0] bits associated with pipes 3 to 5.

IFIS bit (Isochronous IN Buffer Flush)

The IFIS bit specifies whether to flush the buffer when the pipe selected in the PIPESEL.PIPESEL[3:0] bits is used for isochronous IN transfers.

In device controller mode when the selected pipe is for isochronous IN transfers, the USBFS automatically clears the FIFO buffer if the USBFS fails to receive the IN token from the USB host within the interval set in the IITV[2:0] bits in terms of frames. When double buffering is specified (PIPECFG.DBLB = 1), the USBFS only clears the data in the previously used plane.

The USBFS clears the FIFO buffer on receiving the SOF packet immediately after the frame in which the USBFS expected to receive the IN token. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time the SOF packet is expected to be received by using the internal interpolation function.

When the host controller function is selected, set this bit to 0. When the selected pipe is not for isochronous transfer, set this bit to 0.

28.2.29 管道周期控制寄存器(PIPEPERI)

Address(es): USBFS.PIPEPERI 4009 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	IITV[2:0] *1	间隔错误检测间隔	将所选管道的间隔错误检测时间指定为帧时间的2的n次方	R/W
b11 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	IFIS	同步IN缓冲区刷新	0：缓冲区未刷新1：缓 冲区已刷新。	R/W
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在PID为NAK时设置IITV[2:0]位。在设置这些位之前，请检查PBUSY位是否为0，然后更改PID[1:0]位从01b(BUF)到00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则不需要通过软件检查PBUSY位。

PIPEPERI选择在同步IN传输期间发生间隔错误时是否刷新缓冲区，并设置管道1到9的间隔错误检测间隔。

IITV[2:0]位（间隔错误检测间隔）

要在设置IITV[2:0]位并在执行USB通信后将其更改为另一个值，请设置PIPEnCTR.PID[1:0]位为00b(NAK)，然后将PIPEnCTR.ACLRM位设置为1以初始化间隔定时器。

不为管道3到5提供IITV[2:0]位。将000b写入与管道3到5相关联的IITV[2:0]位的位位置。

IFIS位（同步IN缓冲区刷新）

IFIS位指定当在PIPESEL.PIPESEL[3:0]位中选择的管道用于同步IN传输时是否刷新缓冲区。

在设备控制器模式下，当所选管道用于同步IN传输时，USBFS会自动清除
如果USBFS未能在IITV[2:0]位（以帧为单位）设置的间隔内接收来自USB主机的IN令牌，则FIFO缓冲区。当指定双缓冲时（PIPECFG.DBLB=1），USBFS只清除先前使用的平面中的数据。

在USBFS预期接收IN令牌的帧之后，USBFS在接收到SOF数据包后立即清除FIFO缓冲区。即使SOF数据包损坏，FIFO缓冲区也会在预期接收SOF数据包时使用内部插值功能清除。

Whenthehostcontrollerfunctionisselected setthisbitto0.Whentheselectedpipeisnotforisochronoustransfer set thisbitto0.

28.2.30 PIPEn Control Registers (PIPEnCTR) (n = 1 to 9)

PIPEnCTR (n = 1 to 5)

Address(es): USBFS.PIPE1CTR 4009 0070h, USBFS.PIPE2CTR 4009 0072h, USBFS.PIPE3CTR 4009 0074h, USBFS.PIPE4CTR 4009 0076h, USBFS.PIPE5CTR 4009 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: The selected pipe is not used for the transaction 1: The selected pipe is used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	Sets the sequence toggle bit for pipe n: 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1.	R/W*1
b8	SQCLR	Sequence Toggle Bit Clear*2	Clears the sequence toggle bit for pipe n: 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0.	R/W*1
b9	ACLRM	Auto Buffer Clear Mode*3	0: Disabled 1: Enabled (all buffers initialized).	R/W
b10	ATREPM	Auto Response Mode*2	0: Auto response disabled 1: Auto response enabled.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	INBUFM	Transmit Buffer Monitor	0: There are no data to be transmitted in the FIFO buffer 1: There is data to be transmitted in the FIFO buffer.	R
b15	BSTS	Buffer Status	0: Buffer access by the CPU disabled 1: Buffer access by the CPU enabled.	R

Note 1. Only 0 can be read.
Note 2. Only set the ATREPM bit or write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through software is not required.
Note 3. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the USBFS changes the PID[1:0] bits to 00 (NAK), checking the PBUSY bit through software is not required.

PIPEnCTR can be set for any pipe selection in the PIPESEL register.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction on the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USBFS transfer. Table 28.7 and Table 28.8 show the basic operations of the USBFS (when there are no errors in the communication packets) based on the PID[1:0] bit setting.

After changing the PID[1:0] setting from BUF to NAK through software during USBFS communication on the selected pipe, check that the PBUSY bit is 1 to determine if USBFS transfer on the selected pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

28.2.30 PIPEn控制寄存器(PIPEnCTR)(n=1到9)

PIPEnCTR (n = 1 to 5)

Address(es): USBFS.PIPE1CTR 4009 0070h, USBFS.PIPE2CTR 4009 0072h, USBFS.PIPE3CTR 4009 0074h, USBFS.PIPE4CTR 4009 0076h, USBFS.PIPE5CTR 4009 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1b000：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应。	R/W
b4 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	PBUSY	管道忙	0：所选管道不用于事务1：所选管道用于事务。	R
b6	SQMON	序列切换位 Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置*2	设置管道n的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值设置为DATA1。	R/W*1
b8	SQCLR	序列切换位 Clear*2	清除管道n的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值清除到DATA0。	R/W*1
b9	ACLRM	自动缓冲区清除模式*3	0：禁用1：启用（所有缓冲区都已初始化）。	R/W
b10	ATREPM	自动响应模式*2	0：禁用自动响应1：启用自动响应。	R/W
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	INBUFM	发送缓冲区监视器	0：FIFO缓冲区中没有要发送的数据1：FIFO缓冲区中有要发送的数据。	R
b15	BSTS	缓冲区状态	0：禁止CPU访问缓冲区1：允许CPU访问缓冲区。	R

Note 1. 只能读取0。
Note 2. PID为NAK时，仅设置ATREPM位或将1写入SQCLR或SQSET位。在设置这些位之前，请检查PBUSY位为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则不需要通过软件检查PBUSY位。
Note 3. 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。在设置该位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果USBFS将PID[1:0]位更改为00(NAK)，不需要通过软件检查PBUSY位。

PIPEnCTR可以为PIPESEL寄存器中的任何管道选择设置。

PID[1:0]位（响应PID）

PID[1:0]位指定所选管道上下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联管道进行USBFS传输。
表28.7和表28.8显示了基于PID[1:0]位设置的USBFS的基本操作（当通信数据包没有错误时）。

在选定管道上的USBFS通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以确定选定管道上的USBFS传输是否实际进入NAK状态。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。

The USBFS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBFS sets PID to NAK on recognizing completion of the transfer when the selected pipe is receiving and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software
- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBFS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBFS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode.

To specify the response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, transition to NAK and then BUF.

Table 28.7 Operation of the USBFS based on the PID[1:0] setting in host controller mode

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
00b (NAK)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens
01b (BUF)	Bulk or interrupt	Does not depend on the setting	Issues tokens when the DVSTCTR0.UACT bit is 1 and the FIFO buffer associated with the selected pipe is ready for transmission and reception. Does not issue tokens when the DVSTCTR0.UACT bit is 0 or the FIFO buffer associated with the selected pipe is not ready for transmission or reception.
	Isochronous	Does not depend on the setting	Issues tokens regardless of the status of the FIFO buffer associated with the selected pipe
10b (STALL) or 11b (STALL)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens

Table 28.8 Operation of the USBFS based on the PID[1:0] setting in device controller mode (1 of 2)

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
00b (NAK)	Bulk or interrupt	Does not depend on the setting	Returns NAK in response to the token from the USB host
	Isochronous	Does not depend on the setting	Returns nothing in response to the token from the USB host

USBFS在以下情况下更改PIPEnCTR.PID[1:0]设置：

- USBFS在识别到传输完成时将PID设置为NAK，当所选管道正在接收并且所选管道的PIPECFG.SHTNAK位由软件设置为1
- USBFS在接收到有效载荷超过所选管道的最大数据包大小的数据包时将PID设置为STALL(11b)
- USBFS在设备控制器模式下检测到USB总线复位时将PID设置为NAK
- USBFS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK
- USBFS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)。

要指定响应类型，请按如下方式设置PID[1:0]位：

- 要从NAK(00b)转换到STALL，请设置10b
- 要从BUF(01b)转换到STALL，请设置11b
- 要从STALL(11b)转换到NAK，请设置10b，然后设置00b
- 要从STALL过渡到BUF，先过渡到NAK，然后再过渡到BUF。

Table 28.7 USBFS在主机控制器模式下基于PID[1:0]设置的操作

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
00b (NAK)	不依赖于设置	不依赖于设置	不发行代币
01b (BUF)	批量或中断	不依赖于设置	当DVSTCTR0.UACT位为1并且与所选管道关联的FIFO缓冲区已准备好进行发送和接收时，发出令牌。当DVSTCTR0.UACT位为0或与所选管道关联的FIFO缓冲区尚未准备好进行发送或接收。
	Isochronous	不依赖于设置	无论与所选管道关联的FIFO缓冲区的状态如何，都会发出令牌
10b (STALL) or 11b (STALL)	不依赖于设置	不依赖于设置	不发行代币

Table 28.8 基于设备控制器模式下的PID[1:0]设置的USBFS操作（1of2）

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
00b (NAK)	批量或中断	不依赖于设置	返回NAK以响应来自USB主机的令牌
	Isochronous	不依赖于设置	响应来自USB主机的令牌，不返回任何内容

Table 28.8 Operation of the USBFS based on the PID[1:0] setting in device controller mode (2 of 2)

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
01b (BUF)	Bulk	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Interrupt	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Bulk or interrupt	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the FIFO buffer associated with the selected pipe is ready for transmission. Otherwise, returns NAK.
	Isochronous	Receiving direction (DIR = 0)	Receives data in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, discards the data.
	Isochronous	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the associated FIFO buffer is ready for transmission. Otherwise, transmits a zero-length packet.
10b (STALL) or 11b (STALL)	Bulk or interrupt	Does not depend on the setting	Returns STALL in response to the token from the USB host
	Isochronous	Does not depend on the setting	Returns nothing in response to the token from the USB host

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is currently used for the transaction.

The USBFS changes the PBUSY bit from 0 to 1 at the start of the USBFS transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit with software after PID is set to NAK allows you to check whether changing the pipe setting is possible. For details, see section 28.3.4.1, Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

When the selected pipe is not the isochronous transfer type, the USBFS toggles the SQMON bit on successful completion of the transaction. However, the USBFS does not toggle the SQMON flag when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set*2)

Setting the SQSET bit to 1 through software allows the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USBFS sets the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear*2)

Setting the SQCLR bit to 1 through software allows the USBFS to clear the expected value of the sequence toggle bit for the next transaction of the selected pipe to DATA0. The USBFS sets the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode*3)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 28.9 shows the data cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which this processing is required.

Table 28.9 Data cleared by the USBFS when ACLRM = 1 (1 of 2)

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe (two FIFO buffers in double buffer mode)	When initializing the selected pipe

Table 28.8 基于设备控制器模式下的PID[1:0]设置的USBFS操作（2之2）

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
01b (BUF)	Bulk	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK以响应来自USB主机的OUT令牌
	Interrupt	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK以响应来自USB主机的OUT令牌
	批量或中断	发射方向(DIR=1)	传输数据以响应来自USB主机的令牌，如果 与所选管道关联的FIFO缓冲区已准备好进行传输。否则， 返回NAK。
	Isochronous	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据以响应来自USB主机的OUT令牌。 否则，丢弃数据。
	Isochronous	发射方向(DIR=1)	如果关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，发送零长度数据包。
10b (STALL) or 11b (STALL)	批量或中断	不依赖于设置	返回STALL以响应来自USB主机的令牌
	Isochronous	不依赖于设置	响应来自USB主机的令牌，不返回任何内容

PBUSY位（管道忙）

PBUSY位指示所选管道当前是否用于事务。

USBFS在所选管道的USBFS事务开始时将PBUSY位从0更改为1，并在完成一个事务时将PBUSY位从1更改为0。

在PID设置为NAK后，用软件读取PBUSY位可以检查是否可以更改管道设置。详见28.3.4.1管道控制寄存器切换流程。

SQMON位（序列切换位确认）

SQMON位指示所选管道的下一个事务的序列切换位的预期值。

当所选管道不是同步传输类型时，USBFS在事务成功完成时切换SQMON位。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBFS不会切换SQMON标志。

SQSET位（序列切换位设置*2）

通过软件将SQSET位设置为1允许USBFS将DATA1设置为所选管道下一个事务的序列切换位的预期值。USBFS将SQSET位设置为0。

SQCLR位（序列切换位清除*2）

通过软件将SQCLR位设置为1允许USBFS将所选管道的下一个事务的序列切换位的预期值清除为DATA0。USBFS将SQCLR位设置为0。

ACLRM位（自动缓冲区清除模式*3）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。彻底清除数据库中的数据FIFO缓冲区分配给所选管道，向ACLRM位连续写入1和0。

表28.9显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 28.9 当ACLRM=1(1of2)时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	FIFO缓冲区中的所有数据分配给选定的管道（两个双缓冲模式下的FIFO缓冲）	初始化选定管道时

Table 28.9 Data cleared by the USBFS when ACLRM = 1 (2 of 2)

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value
3	Internal flags related to the PIPECFG.BFRE bit	When changing the PIPECFG.BFRE setting
4	FIFO buffer toggle control	When changing the PIPECFG.DBLB setting
5	Internal flags related to the transaction count	When forcing the transaction count function to terminate

ATREPM bit (Auto Response Mode*2)

The ATREPM bit enables or disables auto response mode for the selected pipe.

This bit can be set to 1 in device controller mode when the selected pipe is for bulk transfer. When the bit is set to 1, the USBFS responds to the token from the USB host as follows:

- When the selected pipe is set for Bulk IN transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 1):
  a. When the ATREPM bit = 1 and PID = BUF, the USBFS transmits a zero-length packet in response to the IN token.
  b. The USBFS updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USBFS receives ACK from the USB host. In a single transaction, the IN token is received, a zero-length packet is transmitted, and then ACK is received. The USBFS does not generate the BRDY or BEMP interrupt.
- When the selected pipe is set for Bulk OUT transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 0):
  - When the ATREPM bit = 1 and PID = BUF, the USBFS returns NAK in response to the OUT token and generates an NRDY interrupt.

For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode. When the selected pipe uses isochronous transfer, always set this bit to 0.

In host controller mode, always set the ATREPM bit to 0.

INBUFM bit (Transmit Buffer Monitor)

The INBUMFM bit indicates the FIFO buffer status for the selected pipe in the transmitting direction.

When the selected pipe is transmitting (PIPECFG.DIR = 1), the USBFS sets this bit to 1 when the CPU or DMA/DTC completes writing data to at least one FIFO buffer plane.

The USBFS sets this bit to 0 when it completes transmitting the data from the FIFO buffer plane to which all the data is written. In double buffer mode (PIPECFG.DBLB = 1), the USBFS sets the INBUFM bit to 0 when the it completes transmitting the data from the two FIFO buffer planes before the CPU or DMA/DTC completes writing data to one FIFO buffer plane.

The INBUFM bit indicates the same value as the BSTS bit when the selected pipe is receiving (PIPECFG.DIR = 0).

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 28.10.

Table 28.9 当ACLRM=1(2of2)时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时
3	与PIPECFG.BFRE位相关的内部标志	更改PIPECFG.BFRE设置时
4	FIFO缓冲区切换控制	更改PIPECFG.DBLB设置时
5	与事务计数相关的内部标志	强制事务计数函数终止时

ATREPM位（自动响应模式*2）

ATREPM位启用或禁用所选管道的自动响应模式。

当所选管道用于批量传输时，该位可以在设备控制器模式下设置为1。当该位设置为1时，USBFS对来自USB主机的令牌的响应如下：

- 当所选管道设置为批量输入传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=1）：

  一个。当ATREPM位=1且PID=BUF时，USBFS发送一个长度为零的数据包以响应IN令牌。

  湾。每次USBFS从USB主机接收到ACK时，USBFS都会更新（允许切换）序列切换位(DATA-PID)。在单个事务中，收到IN令牌，发送零长度数据包，然后收到ACK。USBFS不会产生BRDY或BEMP中断。

- 当所选管道设置为批量输出传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=0）：
  - 当ATREPM位=1且PID=BUF时，USBFS返回NAK以响应OUT令牌并产生NRDY中断。

对于自动响应模式下的USB通信，当FIFO缓冲区为空时，将ATREPM位设置为1。在自动响应模式下的USB通信期间不要写入FIFO缓冲区。当所选管道使用同步传输时，始终将此位设置为0。

在主机控制器模式下，始终将ATREPM位设置为0。

INBUFM位（发送缓冲区监视器）

INBUMFM位指示发送方向上所选管道的FIFO缓冲区状态。

当所选管道正在传输时（PIPECFG.DIR=1），当CPU或DMADTC完成将数据写入至少一个FIFO缓冲区平面时，USBFS将该位设置为1。

当USBFS完成从写入所有数据的FIFO缓冲区平面传输数据时，该位设置为0。在双缓冲模式(PIPECFG.DBLB=1)中，当USBFS在CPU或DMADTC完成将数据写入一个FIFO缓冲层之前完成从两个FIFO缓冲层传输数据时，将INBUFM位设置为0。

当所选管道正在接收(PIPECFG.DIR=0)时，INBUFM位指示与BSTS位相同的值。

BSTS位（缓冲区状态）

BSTS位指示所选管道的FIFO缓冲区状态。

BSTS位的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表28.10所示。

Table 28.10 BSTS bit operation

DIR value	BFRE value	DCLRM value	BSTS bit function
0	0	0	Set to 1 when received data can be read from the FIFO buffer, and set to 0 on completion of data read
		1	Setting prohibited
	1	0	Set to 1 when received data can be read from the FIFO buffer, and set to 0 when software sets the BCLR bit in the Port Control Register to 1 after the data read is complete
		1	Set to 1 when received data can be read from the FIFO buffer, and set to 0 on completion of data read
1	0	0	Set to 1 when transmitted data can be written to the FIFO buffer, and set to 0 on completion of data write
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

PIPEnCTR (n = 6 to 9)

Address(es): USBFS.PIPE6CTR 4009 007Ah, USBFS.PIPE7CTR 4009 007Ch, USBFS.PIPE8CTR 4009 007Eh, USBFS.PIPE9CTR 4009 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: The selected pipe is not used for the transaction 1: The selected pipe is used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	Sets the sequence toggle bit for pipe n: 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W *1
b8	SQCLR	Sequence Toggle Bit Clear*2	Clears the sequence toggle bit for pipe n: 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0. This bit is read as 0.	R/W *1
b9	ACLRM	Auto Buffer Clear Mode*2,*3	0: Disabled 1: Enabled (all buffers are initialized).	R/W
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	BSTS	Buffer Status	0: Buffer access disabled 1: Buffer access enabled.	R

Note 1. Only 0 can be read. Only 1 can be written.
Note 2. Only write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through software is not required.
Note 3. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through software is not required.

Table 28.10 BSTS位操作

方向值	BFRE value	DCLRM value	BSTS位功能
0	0	0	接收到的数据可以从FIFO缓冲区读取时设置为1，数据读取完成时设置为0
		1	禁止设定
	1	0	当接收到的数据可以从FIFO缓冲区中读取时设置为1，当数据读取完成后软件将端口控制寄存器中的BCLR位设置为1时设置为0
		1	接收到的数据可以从FIFO缓冲区读取时设置为1，数据读取完成时设置为0
1	0	0	发送的数据可以写入FIFO缓冲区时设置为1，数据写入完成时设置为0
		1	禁止设定
	1	0	禁止设定
		1	禁止设定

PIPEnCTR (n = 6 to 9)

Address(es): USBFS.PIPE6CTR 4009 007Ah, USBFS.PIPE7CTR 4009 007Ch, USBFS.PIPE8CTR 4009 007Eh, USBFS.PIPE9CTR 4009 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1b000：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应。	R/W
b4 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	PBUSY	管道忙	0：所选管道不用于事务1：所选管道用于事务。	R
b6	SQMON	序列切换位 Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置*2	设置管道n的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值设置为DATA1。该位读为0。	R/W *1
b8	SQCLR	序列切换位 Clear*2	清除管道n的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值清除到DATA0。该位读为0。	R/W *1
b9	ACLRM	自动缓冲区清除模式*2 *3	0：禁用1：启用（初始化所有缓冲区）。	R/W
b14 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	BSTS	缓冲区状态	0：禁止缓冲区访问1：允许缓冲区访问。	R

Note 1. 只能读取0。只能写1个。
Note 2. PID为NAK时，仅向SQCLR或SQSET位写入1。在设置这些位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则不需要通过软件检查PBUSY位。

Note 3. 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。
在设置该位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则不需要通过软件检查PBUSY位。

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the selected pipe for USB transfer. Table 28.7 and Table 28.7 show the basic operation of the USBFS depending on the PID[1:0] setting when there are no errors in the transmitted and received packets.

After changing the PID[1:0] setting from BUF to NAK through software during USB communication on the selected pipe, check that the PBUSY bit is 1 to determine if USB transfer on the selected pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

The USBFS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBFS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBFS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode.

To specify each response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, set 00b (NAK) and then 01b (BUF).

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is currently used for the transaction.

The USBFS changes the PBUSY bit from 0 to 1 at the start of the USBFS transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit through software after PID is set to NAK allows you to check whether changing the pipe setting is possible.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

The USBFS toggles the SQMON bit on successful completion of the transaction. However, the USBFS does not toggle the SQMON bit when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set*2)

Setting the SQSET bit to 1 through software allows the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the selected pipe. The USBFS sets the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear*2)

Setting the SQCLR bit to 1 through software allows the USBFS to clear the expected value of the sequence toggle bit for the next transaction of the selected pipe to DATA0. The USBFS sets the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode*2,*3)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 28.11 shows the data cleared by writing 1 and 0 continuously to the ACLRM bit and the cases in which this processing is required.

PID[1:0]位（响应PID）

PID[1:0]位指定所选管道的下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用所选管道进行USB传输。表28.7和表28.7显示了USB FS在发送和接收数据包中没有错误时根据PID[1:0]设置的基本操作。

在选定管道上的USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1以确定选定管道上的USB传输是否实际进入NAK状态。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。

USBFS在以下情况下更改PIPEnCTR.PID[1:0]设置：

- USBFS在接收到有效载荷超过所选管道的最大数据包大小的数据包时将PID设置为STALL(11b)
- USBFS在设备控制器模式下检测到USB总线复位时将PID设置为NAK
- USBFS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK
- USBFS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)。

要指定每种响应类型，请按如下方式设置PID[1:0]位：

- 要从NAK(00b)转换到STALL，请设置10b
- 要从BUF(01b)转换到STALL，请设置11b
- 要从STALL(11b)转换到NAK，请设置10b，然后设置00b
- 要从STALL转换到BUF，请设置00b(NAK)，然后设置01b(BUF)。

PBUSY位（管道忙）

PBUSY位指示所选管道当前是否用于事务。

USBFS在所选管道的USBFS事务开始时将PBUSY位从0更改为1，并在完成一个事务时将PBUSY位从1更改为0。

在PID设置为NAK后通过软件读取PBUSY位可以检查是否可以更改管道设置。

SQMON位（序列切换位确认）

SQMON位指示所选管道的下一个事务的序列切换位的预期值。

USBFS在事务成功完成时切换SQMON位。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBFS不会触发SQMON位。

SQSET位（序列切换位设置*2）

通过软件将SQSET位设置为1允许USBFS将DATA1设置为所选管道下一个事务的序列切换位的预期值。USBFS将SQSET位设置为0。

SQCLR位（序列切换位清除*2）

通过软件将SQCLR位设置为1允许USBFS将所选管道的下一个事务的序列切换位的预期值清除为DATA0。USBFS将SQCLR位设置为0。

ACLRM位（自动缓冲区清除模式*2 *3）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。彻底清除数据库中的数据FIFO缓冲区分配给所选管道，向ACLRM位连续写入1和0。

表28.11显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 28.11 Data cleared by USBFS when ACLRM = 1

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe	When initializing the selected pipe
2	The interval count value when the selected pipe is for interrupt transfer and the host controller is selected	When resetting the interval count value
3	Internal flags related to the PIPECFG.BFRE bit	When changing the PIPECFG.BFRE setting
4	Internal flags related to the transaction count	When forcing the transaction count function to terminate

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 28.10.

28.2.31 PIPEn Transaction Counter Enable Register (PIPEnTRE) (n = 1 to 5)

Address(es): USBFS.PIPE1TRE 4009 0090h, USBFS.PIPE2TRE 4009 0094h, USBFS.PIPE3TRE 4009 0098h, USBFS.PIPE4TRE 4009 009Ch, USBFS.PIPE5TRE 4009 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TRCLR	Transaction Counter Clear	0: Invalid (writing 0 has no effect) 1: Clear the current counter value.	R/W
b9	TRENB	Transaction Counter Enable	0: Transaction counter disabled 1: Transaction counter enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set each bit in PIPEnTRE while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, then change the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through software is not required.

TRCLR bit (Transaction Counter Clear)

When the TRCLR bit is set to 1, the USBFS clears the current value of the transaction counter associated with the selected pipe and then sets the TRCLR bit to 0.

TRENB bit (Transaction Counter Enable)

The TRENB bit enables or disables the transaction counter.

For receiving pipes, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through software allows the USBFS to control hardware on having received the number of packets equal to the TRNCNT[15:0] setting, as follows:

- When the PIPECFG.SHTNAK bit is 1, the USBFS changes the PID bits to NAK for the associated pipe on having received the number of packets equal to the TRNCNT[15:0] setting
- When the PIPECFG.BFRE bit is 1, the USBFS asserts the BRDY interrupt on having received the number of packets equal to the TRNCNT[15:0] setting and then reading the last received data.

For transmitting pipes, set the TRENB bit to 0.

When the transaction counter is not used, set this bit to 0. When the transaction counter is used, set the TRNCNT[15:0] bits before setting this bit to 1. Set this bit to 1 before receiving the first packet to be counted by the transaction counter.

Table 28.11 ACLRM=1时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	分配给所选管道的FIFO缓冲区中的所有数据	初始化选定管道时
2	所选管道用于中断传输且选择主机控制器时的间隔计数值	重置间隔计数值时
3	与PIPECFG.BFRE位相关的内部标志	更改PIPECFG.BFRE设置时
4	与事务计数相关的内部标志	强制事务计数函数终止时

BSTS位（缓冲区状态）

BSTS位指示所选管道的FIFO缓冲区状态。

BSTS位的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表28.10所示。

28.2.31 PIPEn事务计数器使能寄存器(PIPEnTRE)(n=1到5)

Address(es): USBFS.PIPE1TRE 4009 0090h, USBFS.PIPE2TRE 4009 0094h, USBFS.PIPE3TRE 4009 0098h, USBFS.PIPE4TRE 4009 009Ch, USBFS.PIPE5TRE 4009 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	TRCLR	交易计数器清除	0：无效（写0无效）1：清除当前计数器值。	R/W
b9	TRENB	事务计数器启用	0：事务计数器禁用1：事务计数器启用。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 当PID为NAK时，设置PIPEnTRE中的每个位。在设置这些位之前，检查PIPEnCTR.PBUSY位是否为0，然后将所选管道的PIPEnCTR.PID[1:0]位从BUF更改为NAK。如果USBFS将PID[1:0]位更改为NAK，则不需要通过软件检查PBUSY位。

TRCLR位（事务计数器清零）

当TRCLR位设置为1时，USBFS清除与所选管道关联的事务计数器的当前值，然后将TRCLR位设置为0。

TRENB位（事务计数器使能）

TRENB位启用或禁用事务计数器。

对于接收管道，在设置接收管道的总包数后，将TRENB位设置为1
PIPEnTRN.TRNCNT[15:0]位通过软件允许USBFS在接收到等于TRNCNT[15:0]设置的数据包数量时控制硬件，如下所示：

- 当PIPECFG.SHTNAK位为1时，USBFS在接收到等于TRNCNT[15:0]设置的数据包数量时将关联管道的PID位更改为NAK
- 当PIPECFG.BFRE位为1时，USBFS在接收到等于TRNCNT[15:0]设置的数据包数量并读取最后接收到的数据时断言BRDY中断。

对于传输管道，将TRENB位设置为0。

当不使用事务计数器时，将该位设置为0。当使用事务计数器时，将该位设置为1之前设置TRNCNT[15:0]位。在接收第一个要计数的数据包之前将该位设置为1由交易柜台。

28.2.32 PIPEn Transaction Counter Register (PIPEnTRN) (n = 1 to 5)

Address(es): USBFS.PIPE1TRN 4009 0092h, USBFS.PIPE2TRN 4009 0096h, USBFS.PIPE3TRN 4009 009Ah, USBFS.PIPE4TRN 4009 009Eh, USBFS.PIPE5TRN 4009 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	TRNCNT[15:0]	Transaction Counter	• When written to: Specifies the total number of packets (number of transactions) to be received by the selected pipe • When read from: Indicates the specified number of transactions if the PIPEnTRE.TRENB bit is 0. Indicates the number of currently counted transactions if the PIPEnTRE.TRENB bit is 1.	R/W

The PIPEnTRN registers retain their current setting during a USB bus reset.

TRNCNT[15:0] bits (Transaction Counter)

The USBFS increments the value of the TRNCNT[15:0] bits by 1 when all of the following conditions are satisfied on receiving the packet:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting.

The USBFS sets the value of the TRNCNT[15:0] bits to 0 when any of the following conditions are satisfied:

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet
- The payload of the received packet aligns with the PIPEMAXP.MXPS[8:0] setting.

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The USBFS received a short packet.

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The PIPEnTRE.TRCLR bit is set to 1 by software.

For transmitting pipes, set the TRNCNT[15:0] bits to 0. When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.

Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is only enabled when the PIPEnTRE.TRENB bit is 0. To set the number of transactions to be transferred, set the TRCLR bit to 1 to clear the current counter value before setting the PIPEnTRE.TRENB bit to 1.

28.2.32 PIPEn事务计数器寄存器(PIPEnTRN)(n=1到5)

Address(es): USBFS.PIPE1TRN 4009 0092h, USBFS.PIPE2TRN 4009 0096h, USBFS.PIPE3TRN 4009 009Ah, USBFS.PIPE4TRN 4009 009Eh, USBFS.PIPE5TRN 4009 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	TRNCNT[15:0]	交易柜台	当写给： 指定所选管道要接收的数据包总数（事务数） 从以下位置读取时： 表示指定的事务数，如果PIPEnTRE.TRENB位为0。 如果PIPEnTRE.TRENB位为1，则指示当前计数的事务数。	R/W

在USB总线复位期间，PIPEnTRN寄存器保持其当前设置。

TRNCNT[15:0]位（事务计数器）

当接收到数据包时满足以下所有条件时，USBFS将TRNCNT[15:0]位的值加1：

- PIPEnTRE.TRENB位=1
- (TRNCNT[15:0]设定值≠当前计数器值+1)收到数据包
- 接收到的数据包的有效负载与PIPEMAXP.MXPS[8:0]设置一致。

当满足以下任一条件时，USBFS将TRNCNT[15:0]位的值设置为0：

满足以下所有条件：

- PIPEnTRE.TRENB位=1
- (TRNCNT[15:0]设置值=当前计数器值+1)接收数据包时
- 接收到的数据包的有效负载与PIPEMAXP.MXPS[8:0]设置一致。

满足以下所有条件：

- PIPEnTRE.TRENB位=1
- USBFS收到一个短数据包。

满足以下所有条件：

- PIPEnTRE.TRENB位=1
- PIPEnTRE.TRCLR位由软件设置为1。

对于传输管道，将TRNCNT[15:0]位设置为0。当不使用事务计数器时，将TRNCNT[15:0]位设置为0。

设置要传输到TRNCNT[15:0]位的事务数仅在PIPEnTRE.TRENB位为0。要设置要传输的事务数，请将TRCLR位设置为1以清除当前计数器值，然后再将PIPEnTRE.TRENB位设置为1。

28.2.33 Device Address n Configuration Register (DEVADDn) (n = 0 to 5)

Address(es): USBFS.DEVADD0 4009 00D0h, USBFS.DEVADD1 4009 00D2h, USBFS.DEVADD2 4009 00D4h, USBFS.DEVADD3 4009 00D6h, USBFS.DEVADD4 4009 00D8h, USBFS.DEVADD5 4009 00DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7, b6	USBSPD[1:0]	Transfer Speed of Communication Target Device	b7 b6 0 0: DEVADDn not used 0 1: Low-speed 1 0: Full-speed 1 1: Setting prohibited.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DEVADDn register specifies the transfer speed of the peripheral device that is the communication target for pipes 0 to 9.

In host controller mode, set all DEVADDn bits before starting communication to any pipes. Only change the bits in DEVADDn when no valid pipes are using the bit settings. A valid pipe is defined as one that satisfies both of the following conditions:

- DEVADDn is selected in the DEVSEL[3:0] bits
- The PID[1:0] bits are set to BUF for the selected pipe, or the selected pipe is the DCP with the DCPCTR.SUREQ bit set to 1.

In device controller mode, set all bits in this register to 0.

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

The USBSPD[1:0] bits specify the USB transfer speed of the target peripheral device.

In host controller mode, the USBFS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.

28.2.34 USB Module Control Register (USBMC)

Address(es): USBFS.USBMC 4009 00CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDDUSBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	VDDUSBE	USB Reference Power Supply Circuit On/Off Control	0: USB reference power supply circuit off 1: USB reference power supply circuit on.	R/W
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VDDUSBE bit (USB Reference Power Supply Circuit On/Off Control)

The USB reference power supply circuit generates the reference voltage for battery charging. Set this bit to 1 when using the battery charging function.

28.2.33 器件地址n配置寄存器(DEVADDn)(n=0到5)

Address(es): USBFS.DEVADD0 4009 00D0h, USBFS.DEVADD1 4009 00D2h, USBFS.DEVADD2 4009 00D4h, USBFS.DEVADD3 4009 00D6h, USBFS.DEVADD4 4009 00D8h, USBFS.DEVADD5 4009 00DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7, b6	USBSPD[1:0]	通讯传输速度 目标设备	b7b600：DEVADDn未使用01：低速10：全速11：禁止设置。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DEVADDn寄存器指定作为管道0到9的通信目标的外围设备的传输速度。

在主机控制器模式下，在开始与任何管道通信之前设置所有DEVADDn位。仅更改中的位DEVADDn当没有有效管道使用位设置时。有效管道被定义为同时满足以下两个条件的管道：

- DEVADDn在DEVSEL[3:0]位中选择
- 所选管道的PID[1:0]位设置为BUF，或者所选管道是DCPCTR.SUREQ位设置为1的DCP。

在设备控制器模式下，将此寄存器中的所有位设置为0。

USBSPD[1:0]位（通信目标设备的传输速度）

USBSPD[1:0]位指定目标外围设备的USB传输速度。

在主机控制器模式下，USBFS根据USBSPD[1:0]设置生成数据包。在设备控制器模式下，将这些位设置为00b。

28.2.34 USB模块控制寄存器(USBMC)

Address(es): USBFS.USBMC 4009 00CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDDUSBE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	VDDUSBE	USB参考电源电路 On/Off Control	0：USB参考电源电路关闭1：USB参考电源电路打开。	R/W
b1	—	Reserved	该位读取为1。写入值应为1。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VDDUSBE位（USB参考电源电路开关控制）

USB参考电源电路产生电池充电的参考电压。使用电池充电功能时将此位设置为1。

28.2.35 BC Control Register 0 (USBBCCTRL0)

Address(es): USBFS.USBBCCTRL0 4009 00B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PDDETSTS0	CHGDETSTS0	BATCHGE0	—	VDMSRCE0	IDPSINKE0	VDPSRCE0	IDMSINKE0	IDPSRCE0	RPDMDE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPDME0	D- Pin Pull-Down Control	0: Pull-down off 1: Pull-down on.	R/W
b1	IDPSRCE0	D+ Pin IDPSRC Output Control	0: Stop 1: 10 µA output.	R/W
b2	IDMSINKE0	D- Pin 0.6 V Input Detection (Comparator and Sink) Control	0: Detection off 1: Detection on (comparator and sink current on).	R/W
b3	VDPSRCE0	D+ Pin VDPSRC (0.6 V) Output Control	0: Stop 1: 0.6 V output.	R/W
b4	IDPSINKE0	D+ Pin 0.6 V Input Detection (Comparator and Sink) Control	0: Detection off 1: Detection on (comparator and sink current on).	R/W
b5	VDMSRCE0	D- Pin VDMSRC (0.6 V) Output Control	0: Stop 1: 0.6 V output.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	BATCHGE0	BC (Battery Charger) Function General Enable Control	0: Disabled 1: Enabled.	R/W
b8	CHGDETSTS0	D- Pin 0.6 V Input Detection Status*1	0: Not detected 1: Detected.	R
b9	PDDETSTS0	D+ Pin 0.6 V Input Detection Status*2	0: Not detected 1: Detected.	R
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Valid when IDMSINKE0 = 1.
Note 2. Valid when IDPSINKE0 = 1.

RPDME0 bit (D- Pin Pull-Down Control)

When using the battery charging function, set the RPDME0 bit to 1 to control the pull-down resistor of the D- pin.

IDPSRCE0 bit (D+ Pin IDPSRC Output Control)

When the IDPSRCE0 bit is set to 1 in device controller mode, the current output is enabled on detection of the data connection pin and the D+ pin is pulled up.

IDMSINKE0 bit (D- Pin 0.6 V Input Detection (Comparator and Sink) Control)

When the IDMSINKE0 bit is set to 1 in device controller mode, the USBFS detects whether VDMSRC (0.6 V), output from the host to D- on primary detection, is connected, or whether VDPSRC (0.6 V), output from the device to D+, is connected to D- by the host.

VDPSRCE0 bit (D+ Pin VDPSRC (0.6 V) Output Control)

When the VDPSRCE0 bit is set to 1 in device controller mode, output is enabled on primary detection and VDPSRC (0.6 V) is applied to D+.

IDPSINKE0 bit (D+ Pin 0.6 V Input Detection (Comparator and Sink) Control)

When the IDPSINKE0 bit is set to 1 in device controller mode, the USBFS detects whether VDMSRC (0.6 V), output from the device to D-, is connected to D+ (DCP) by the host. In host controller mode, the USBFS detects whether VDPSRC (0.6 V), output from the device to D+ on primary detection, is connected.

28.2.35 BC控制寄存器0(USBBCCTRL0)

Address(es): USBFS.USBBCCTRL0 4009 00B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PDDETSTS0	CHGDETSTS0	BATCHGE0	—	VDMSRCE0	IDPSINKE0	VDPSRCE0	IDMSINKE0	IDPSRCE0	RPDMDE0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPDME0	D- Pin Pull-Down Control	0：下拉关闭1 ：下拉打开。	R/W
b1	IDPSRCE0	D+引脚IDPSRC输出控制	0：停止1：10µ A输出。	R/W
b2	IDMSINKE0	DPin0.6V输入检测（比较器和灌电流）控制	0：检测关闭1：检测开启（比较器和灌电流开启）。	R/W
b3	VDPSRCE0	D+引脚VDPSRC(0.6V)输出Control	0：停止1：0.6 V输出。	R/W
b4	IDPSINKE0	D+引脚0.6V输入检测（比较器和灌电流）控制	0：检测关闭1：检测开启（比较器和灌电流开启）。	R/W
b5	VDMSRCE0	D- Pin VDMSRC (0.6 V) Output Control	0：停止1：0.6 V输出。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	BATCHGE0	BC (Battery Charger) Function 通用启用控制	0：禁用1 ：启用。	R/W
b8	CHGDETSTS0	DPin0.6V输入检测状态 *1	0：未检测到1 ：检测到。	R
b9	PDDETSTS0	D+引脚0.6V输入检测Status*2	0：未检测到1 ：检测到。	R
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当IDMSINKE0=1时有效。
Note 2. 当IDPSINKE0=1时有效。

RPDME0位（DPin下拉控制）

使用电池充电功能时，设置RPDME0位为1来控制Dpin的下拉电阻。

IDPSRCE0位（D+引脚IDPSRC输出控制）

当IDPSRCE0位在设备控制器模式下设置为1时，在检测到数据连接引脚且D+引脚上拉时启用电流输出。

IDMSINKE0位（DPin0.6V输入检测（比较器和接收器）控制）

当IDMSINKE0位在设备控制器模式下设置为1时，USBFS检测从主机输出到Don主检测的VDMSRC(0.6V)是否连接，或者从设备输出到D+的VDPSRC(0.6V)是否连接，通过主机连接到D。

VDPSRCE0位（D+引脚VDPSRC(0.6V)输出控制）

当VDPSRCE0位在设备控制器模式下设置为1时，在主检测和VDPSRC（0.6 V)应用于D+。

IDPSINKE0位（D+引脚0.6V输入检测（比较器和接收器）控制）

当IDPSINKE0位在设备控制器模式下设置为1时，USBFS检测从设备输出到D-的VDMSRC(0.6V)是否被主机连接到D+(DCP)。在主机控制器模式下，USBFS检测是否连接了主检测时从设备输出到D+的VDPSRC(0.6V)。

VDMSRCE0 bit (D- Pin VDMSRC (0.6 V) Output Control)

When the VDMSRCE0 bit is set to 1 in device controller mode, output is enabled on secondary detection and VDMSRC (0.6 V) is applied to D-. In host controller mode, output is enabled on primary detection and VDMSRC (0.6 V) is applied to D-.

CHGDETSTS0 flag (D- Pin 0.6 V Input Detection Status)

In host controller mode, the CHGDETSTS0 flag is set to 1 if the USBFS detects whether VDMSRC (0.6 V), output from the host to D- during primary detection, is connected, or whether VDPSRC (0.6 V), output from the device to D+, is connected to D- by the host.

PDDETSTS0 flag (D+ Pin 0.6 V Input Detection Status)

In device controller mode, the PDDETSTS0 flag is set to 1 if the USBFS detects whether VDMSRC (0.6 V), output from the device to D- during secondary detection, is connected to D+ (DCP) by the host.

In host controller mode, this bit is set to 1 if the USBFS detects whether VDPSRC (0.6 V), output from the device to D+ during primary detection, is connected.

28.3 Operation

28.3.1 System Control

This section describes register settings required for initializing the USBFS and controlling power consumption.

28.3.1.1 Setting data to the USBFS-related registers

Setting the SYSCFG.USBE bit to 1 after starting the clock supply to the USB (SYSCFG.SCKE bit = 1) enables and starts USBFS operation.

28.3.1.2 Selecting the controller function

The USBFS can operate as either a host or device controller.

Use the SYSCFG.DCFM bit to select one of these USBFS functions. The DCFM bit must be changed in the initial settings immediately after a reset or in the D+ pull-up-disabled state (SYSCFG.DPRPU bit = 0) and D+ and D- pull-down-disabled state (SYSCFG.DRPD bit = 0).

28.3.1.3 Controlling the USBFS data bus using resistors

The USBFS provides pull-up and pull-down resistors for the D+ and D- lines. Pull these lines up or down by setting the SYSCFG.DPRPU, SYSCFG.DMRPU, and SYSCFG.DRPD bits.

In device controller mode, confirm that connection to the USB host is made, then set the SYSCFG.DPRPU bit to 1 to pull up the D+ line (in full-speed communication), or set the SYSCFG.DMRPU bit to 1 to pull up the D- line (in low-speed communication).

When the SYSCFG.DPRPU (during full-speed) or the SYSCFG.DMRPU (during low-speed) bit is set to 0 during communication with a PC, the USBFS disables the pull-up resistor of the USB data line, thereby notifying the USB host of disconnection.

In host controller mode, set the SYSCFG.DRPD bit to 1 to pull down the D+ and D- lines.

Table 28.12 Control settings for the USBFS data bus resistors

SYSCFG register settings			USB data bus control		
DRPD bit	DPRPU Bit	DMRPU Bit	D–	D+	Function
0	0	0	Open	Open	When resistors not used
0	1	0	Open	Pull-up	When operating as the device controller at full-speed
0	0	1	Pull-up	Open	When operating as the device controller at low-speed
1	0	0	Pull-down	Pull-down	When operating as a host controller
Other settings			—	—	Setting prohibited

VDMSRCE0位（DPinVDMSRC(0.6V)输出控制）

当VDMSRCE0位在设备控制器模式下设置为1时，在次级检测时启用输出，并且VDMSRC(0.6V)应用于D−。在主机控制器模式下，在初级检测时启用输出，并将VDMSRC(0.6V)应用于D−。

CHGDETSTS0标志（DPin0.6V输入检测状态）

在主机控制器模式下，如果USBFS检测到VDMSRC(0.6V)（在主检测期间从主机输出到D+）是否连接，或者VDPSRC(0.6V)（从设备输出到D+）是否连接，则CHGDETSTS0标志设置为1，通过主机连接到D。

PDDETSTS0标志（D+引脚0.6V输入检测状态）

在设备控制器模式下，如果USBFS检测到在二次检测期间从设备输出到D的VDMSRC(0.6V)是否被主机连接到D+(DCP)，则PDDETSTS0标志设置为1。

在主机控制器模式下，如果USBFS检测到在主检测期间从设备输出到D+的VDPSRC(0.6V)是否连接，则该位设置为1。

28.3 Operation

28.3.1 系统控制

本节介绍初始化USBFS和控制功耗所需的寄存器设置。

28.3.1.1 将数据设置到USBFS相关寄存器

在开始向USB提供时钟（SYSCFG.SCKE位=1）后将SYSCFG.USBE位设置为1启用并启动USBFS operation.

28.3.1.2 选择控制器功能

USBFS可以作为主机或设备控制器运行。

使用SYSCFG.DCFM位选择这些USBFS功能之一。DCFM位必须在复位后立即更改为初始设置或在D+上拉禁用状态（SYSCFG.DPRPU位=0）和D+和Dpulldown禁用状态（SYSCFG.DRPD位=0）。

28.3.1.3 使用电阻控制USBFS数据总线

USBFS为D+和Dlines提供上拉和下拉电阻。通过设置SYSCFG.DPRPU、SYSCFG.DMRPU和SYSCFG.DRPD位。

在设备控制器模式下，确认与USB主机的连接已建立，然后将SYSCFG.DPRPU位设置为1以上拉D+线（全速通信），或将SYSCFG.DMRPU位设置为1以上拉Dline（低速通信）。

当SYSCFG.DPRPU（全速期间）或SYSCFG.DMRPU（低速期间）位在与PC通信期间设置为0时，USBFS禁用USB数据线的上拉电阻，从而通知USB主机断开。

在主机控制器模式下，将SYSCFG.DRPD位设置为1以拉低D+和Dlines。

Table 28.12 USBFS数据总线电阻的控制设置

SYSCFG寄存器设置			USB数据总线控制		
DRPD bit	DPRPU Bit	DMRPU Bit	D–	D+	Function
0	0	0	Open	Open	不使用电阻时
0	1	0	Open	Pull-up	作为设备控制器全速运行时
0	0	1	Pull-up	Open	作为设备控制器以低速运行时
1	0	0	Pull-down	Pull-down	作为主机控制器运行时
其他设置			—	—	禁止设定

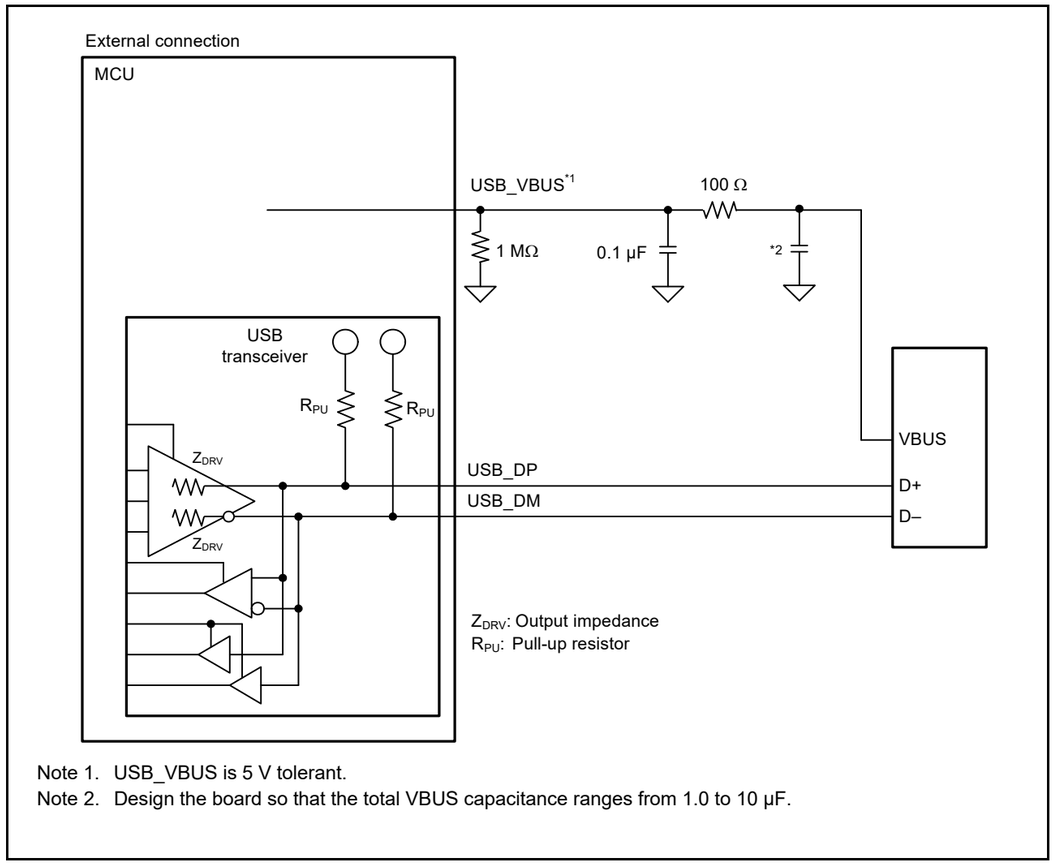
28.3.1.4 Example of USB external connection circuits

The host recognizes a USB device when one of the data lines is pulled up. The MCU can use switching of the internal pull-up resistor for this. Also, bus-powered devices do not require external regulators because the MCU provides a power supply in the USB-PHY.

Figure 28.2 show examples of external circuits for USB connection.

The USBFS controls the pull-up resistor of the D+ line and the pull-down resistor of D+ and D- lines. Select pull-up and pull-down for the lines in the SYSCFG.DPRPU and SYSCFG.DRPD bits. In device controller mode, the pull-up resistor of USB data line is disabled if SYSCFG.DPRPU bit is set to 0 while communicating with the USB host. The USBFS can use this to notify the USB host of a device disconnect.

Figure 28.2 shows an example of functional connection of the USB connector in the self-powered state.



Note 1. USB_VBUS is 5 V tolerant.
Note 2. Design the board so that the total VBUS capacitance ranges from 1.0 to 10 μF.

Figure 28.2 Example device connection in self-powered state

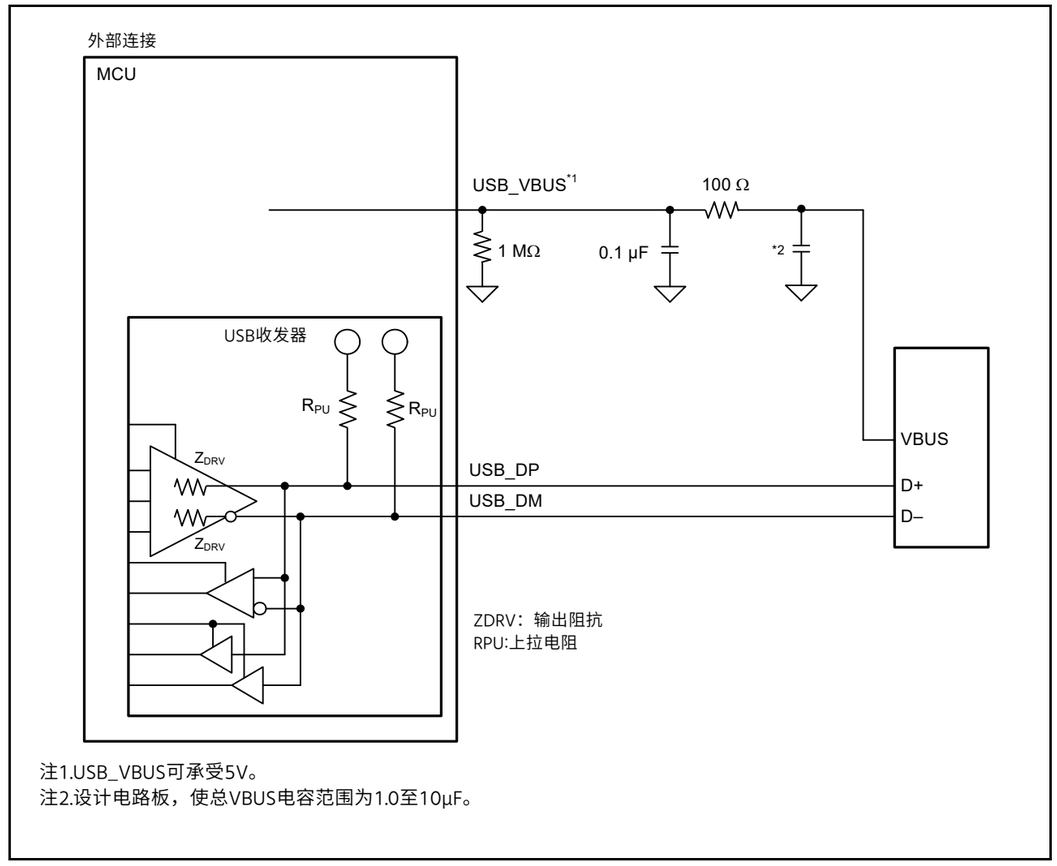
28.3.1.4 USB外部连接电路示例

当其中一根数据线被拉起时，主机识别USB设备。为此，MCU可以使用内部上拉电阻的切换。此外，总线供电设备不需要外部稳压器，因为MCU在USB-PHY中提供电源。

图28.2显示了USB连接的外部电路示例。

USBFS控制D+线的上拉电阻和D+和Dlines的下拉电阻。为SYSCFG.DPRPU和SYSCFG.DRPD位中的线路选择上拉和下拉。在设备控制器模式下，如果在与USB主机通信时将SYSCFG.DPRPU位设置为0，则禁用USB数据线的上拉电阻。USBFS可以使用它来通知USB主机设备断开连接。

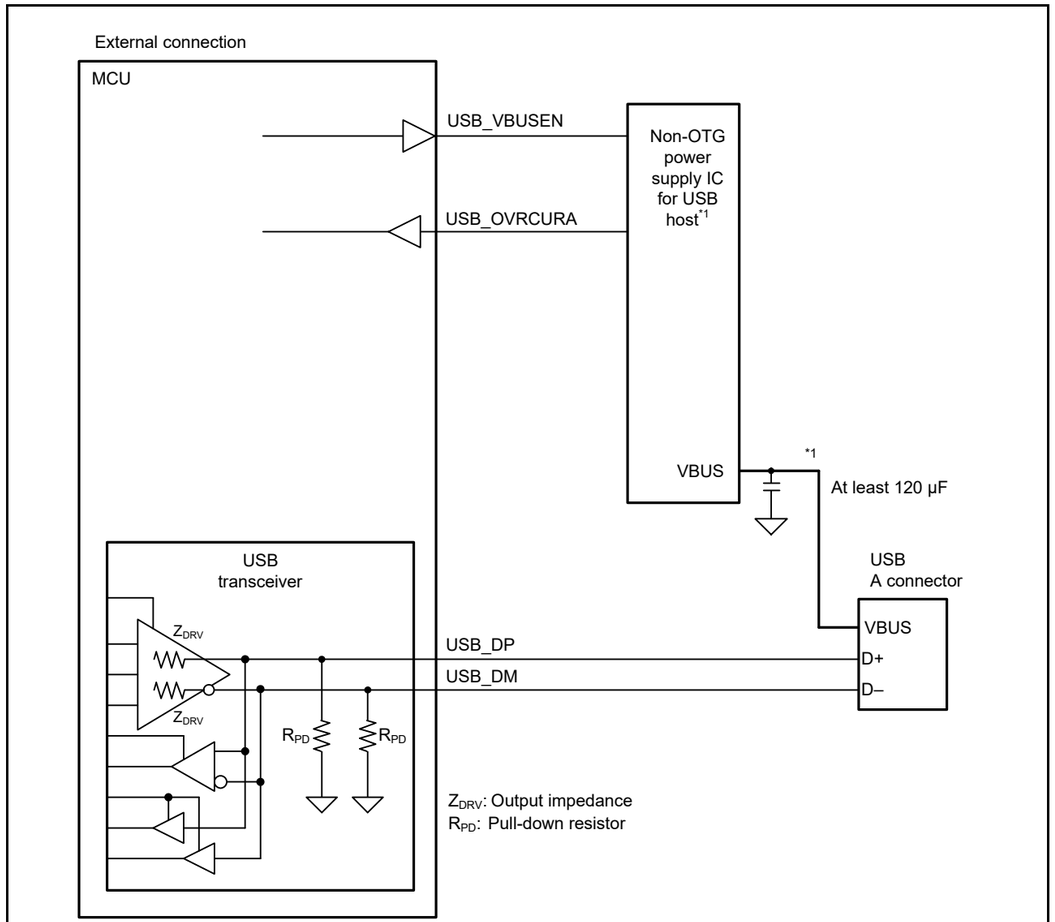
图28.2显示了自供电状态下USB连接器的功能连接示例。



注1.USB_VBUS可承受5V。
注2.设计电路板，使总VBUS电容范围为1.0至10μF。

Figure 28.2 自供电状态下的示例设备连接

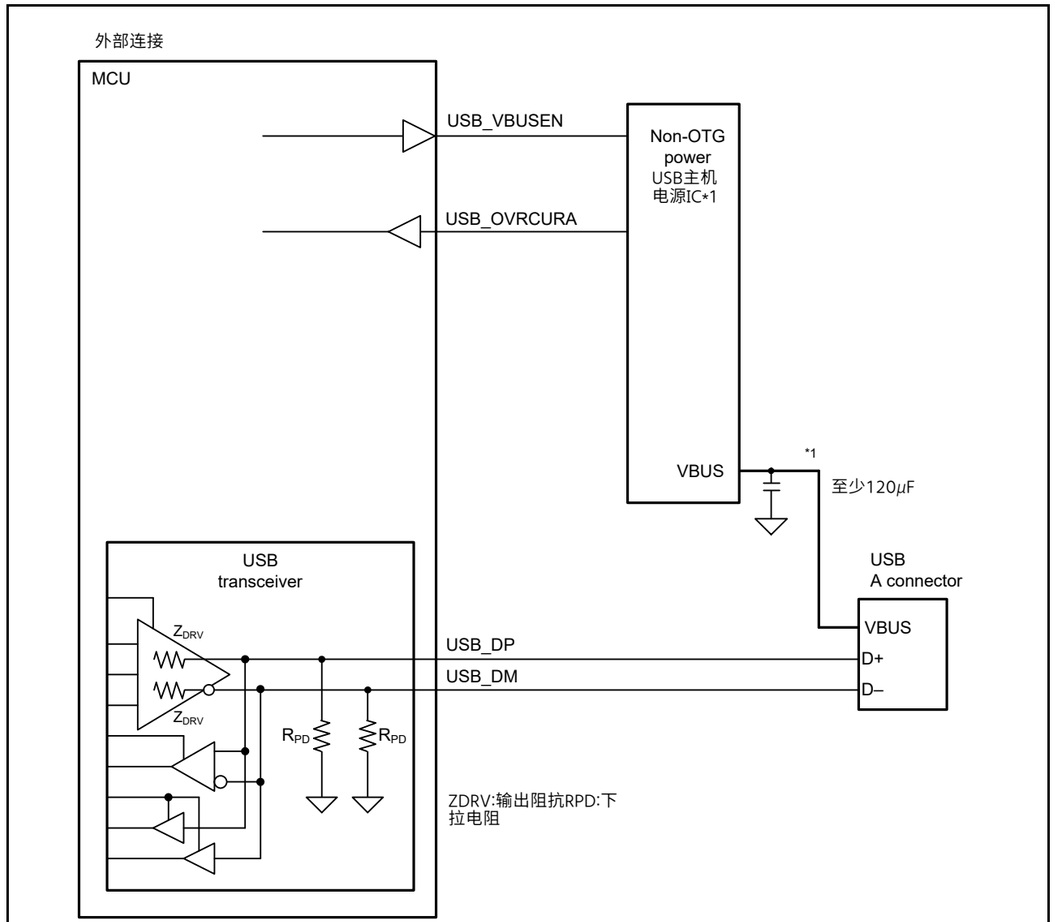
Figure 28.3 shows an example of host connection of the USB connector.



Note 1. When Battery Charging Specification Rev 1.2 is to be supported, ensure that the power supply IC and the VBUS wiring width are enough for at least 1.5 A.

Figure 28.3 Example host connection

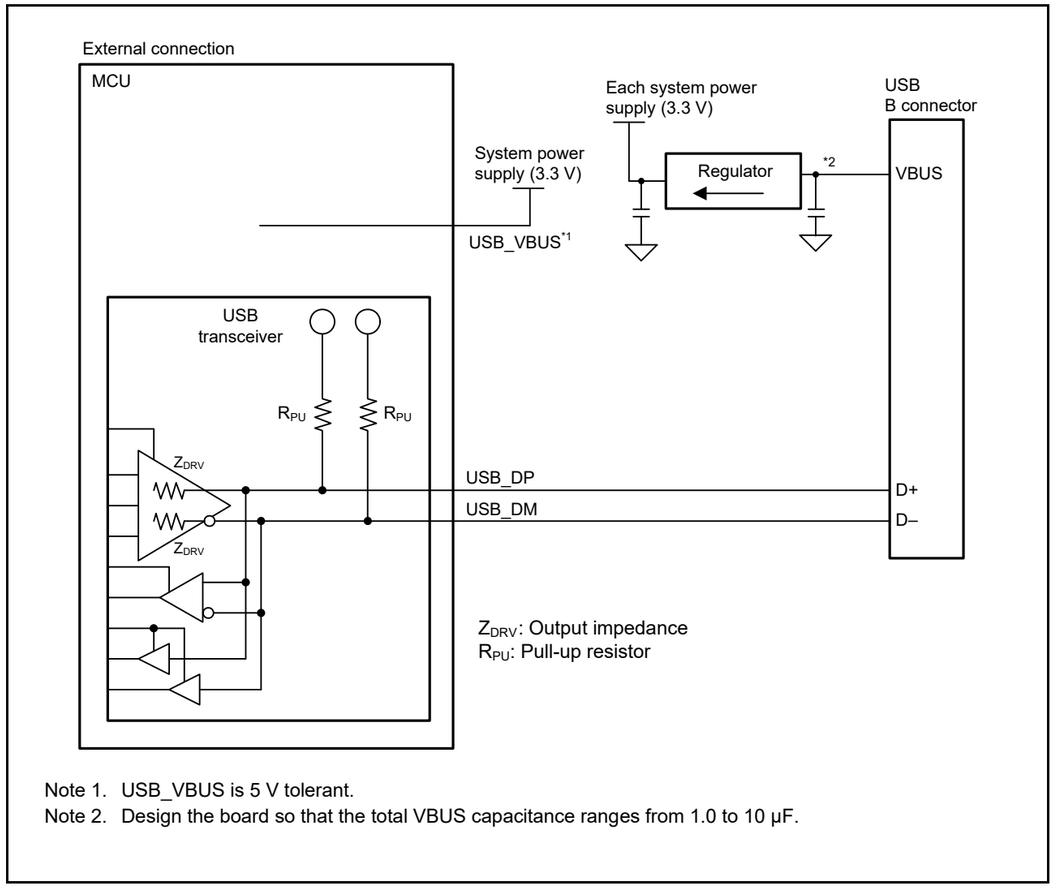
图28.3显示了USB连接器的主机连接示例。



注1.支持电池充电规范Rev1.2时，请确保电源IC和VBUS布线宽度足以满足至少1.5A的需求。

Figure 28.3 主机连接示例

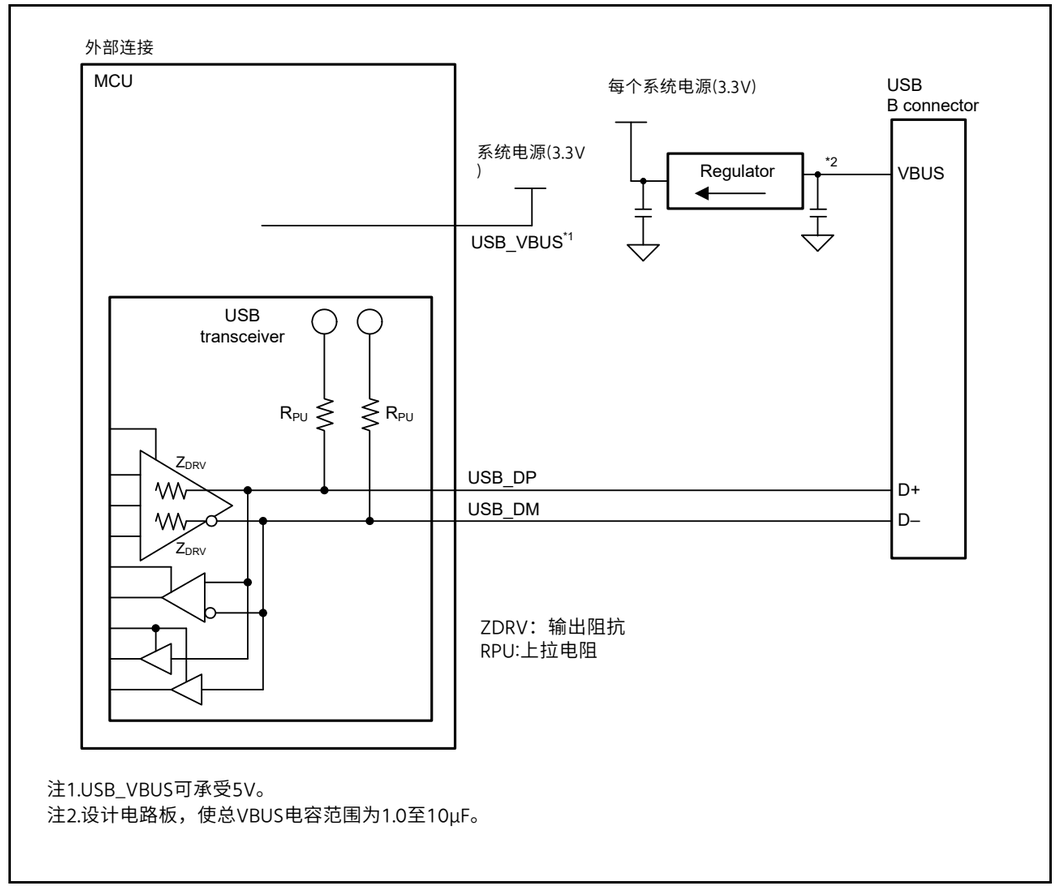
Figure 28.4 shows an example of functional connection of the USB connector in bus-powered state.



Note 1. USB_VBUS is 5 V tolerant.
Note 2. Design the board so that the total VBUS capacitance ranges from 1.0 to 10 μF.

Figure 28.4 Example device connection in bus-powered state 1

图28.4显示了USB连接器在总线供电状态下的功能连接示例。



注1.USB_VBUS可承受5V。
注2.设计电路板，使总VBUS电容范围为1.0至10μF。

Figure 28.4 总线供电状态1中的示例设备连接

Figure 28.5 shows an example of functional connection of the USB connector in bus-powered state 2.

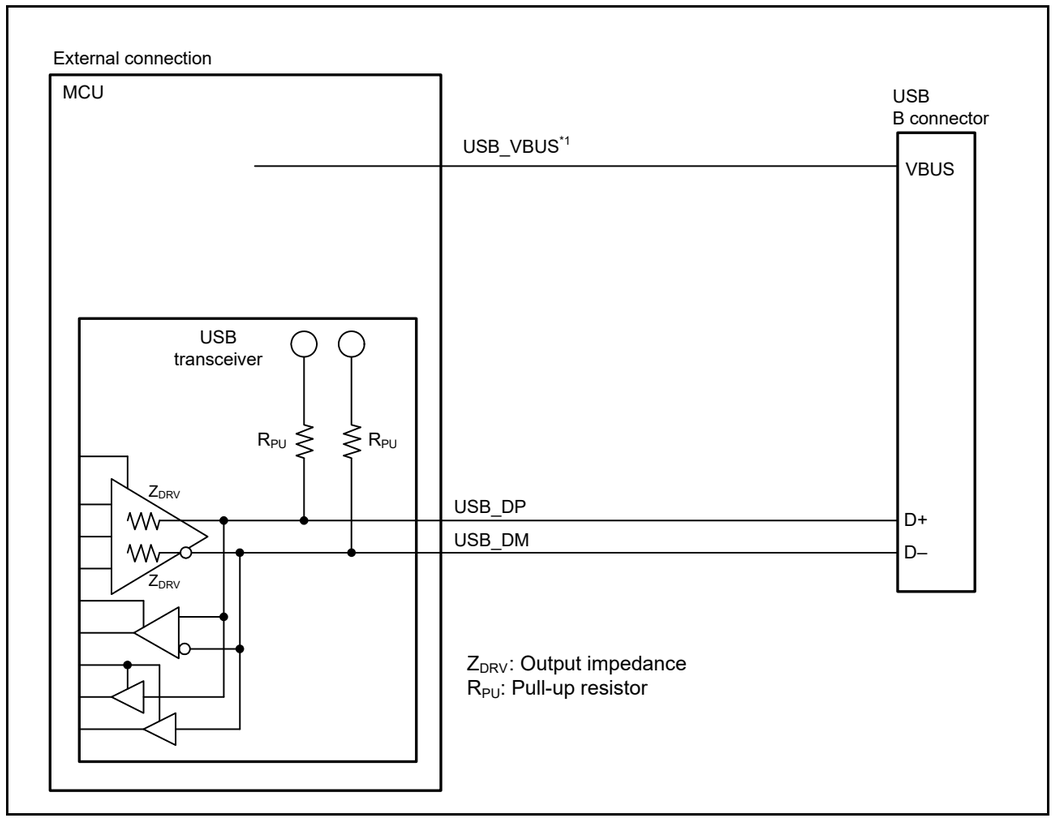


Figure 28.5 Example device connection in bus-powered state 2

The examples of external circuits given in this section are simplified circuits, and their operation in every system is not guaranteed.

图28.5显示了USB连接器在总线供电状态2下的功能连接示例。

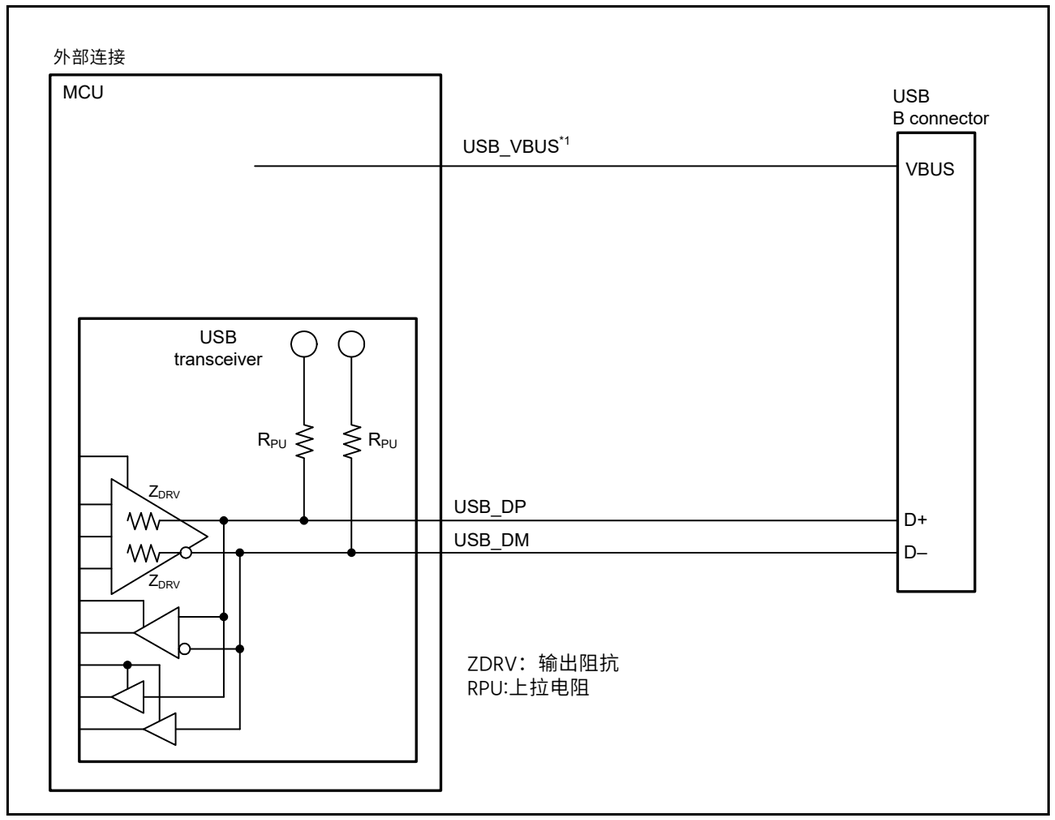
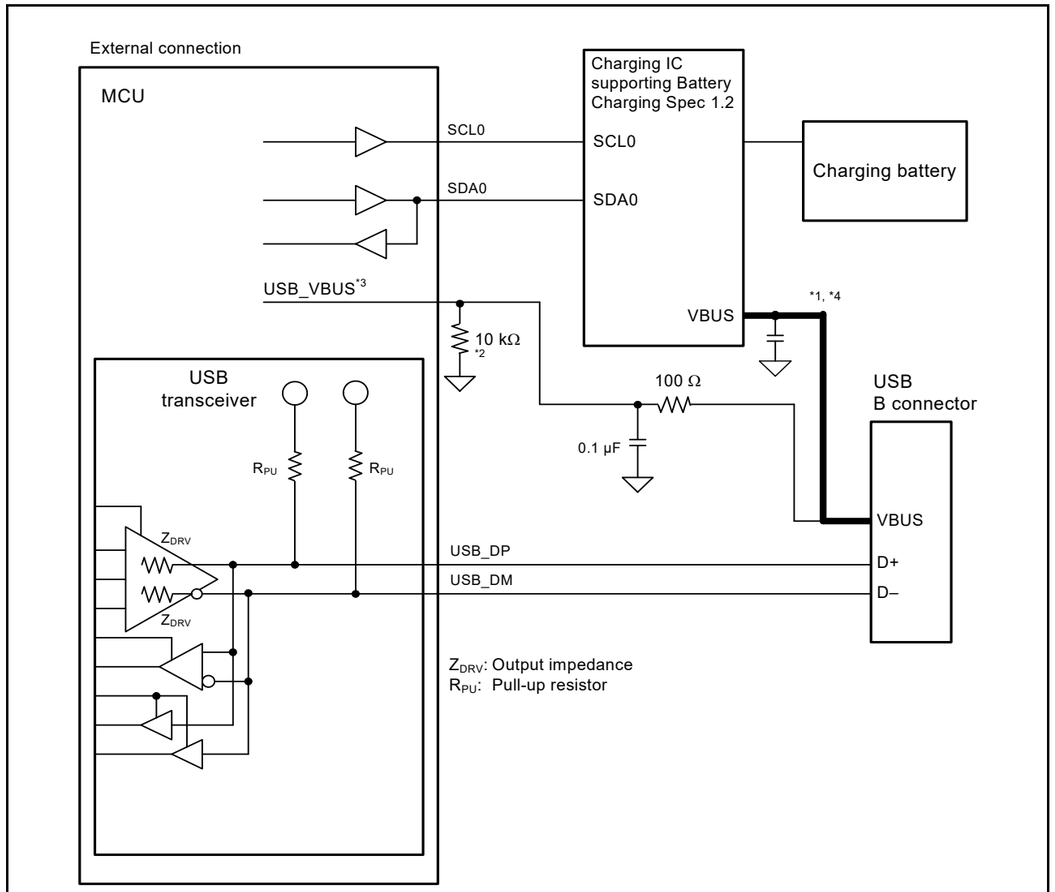


Figure 28.5 总线供电状态2中的示例设备连接

本节中给出的外部电路示例是简化电路，不保证它们在每个系统中的操作。

Figure 28.6 shows an example of functional connection of the USB connector with Battery Charging Rev 1.2 supported.



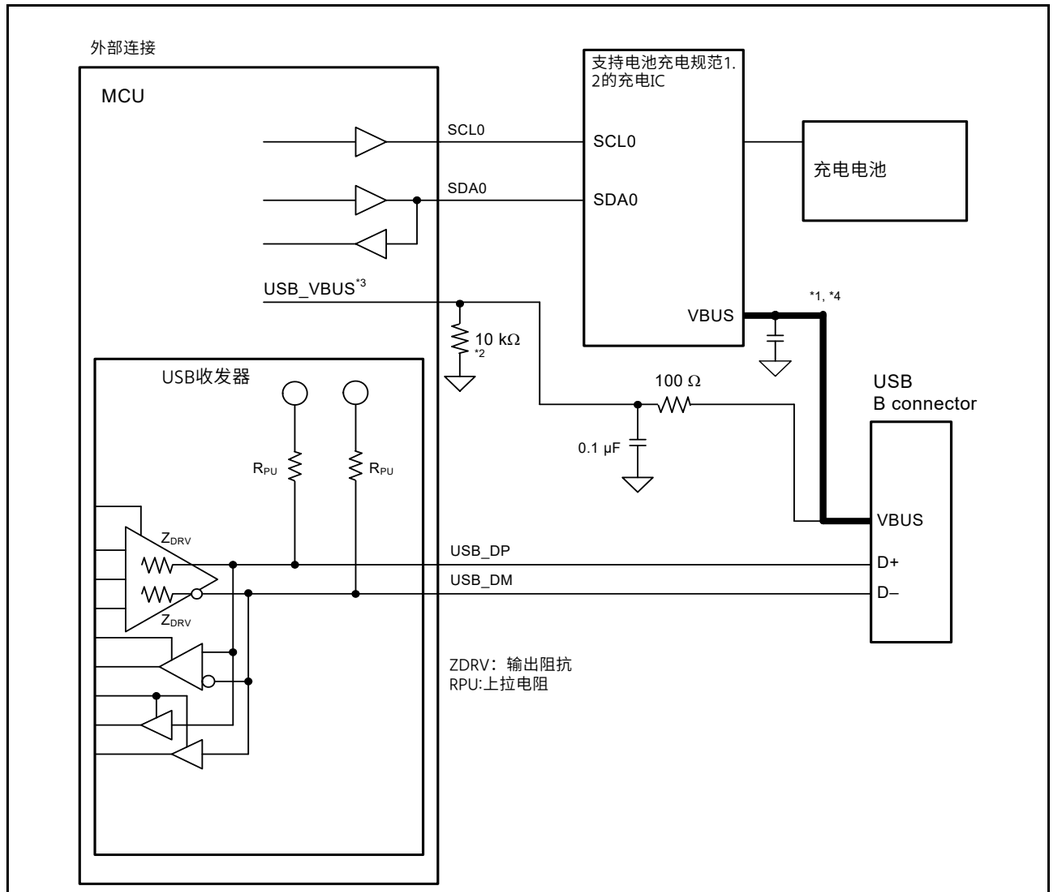
Note 1. When Battery Charging Specification Rev 1.2 is to be supported, ensure that the VBUS wiring width is enough for at least 1.5 A (shown in bold lines).
Note 2. Use a resistor value such that the discharging time of VBUS is within 500 ms.
Note 3. USB_VBUS is 5 V tolerant.
Note 4. Design the board so that the total VBUS capacitance ranges from 1.0 to 10 µF.

Figure 28.6 Example of functional connection with Battery Charging Specification Rev 1.2 supported

28.3.2 Interrupt Sources

Table 28.13 lists the interrupt sources in the USBFS. When an interrupt generation condition is satisfied and the interrupt output is enabled using the associated interrupt enable register, a USBFS interrupt request is issued to the Interrupt Controller Unit and a USBFS interrupt is generated. See section 14, Interrupt Controller Unit (ICU).

图28.6显示了支持电池充电Rev1.2的USB连接器的功能连接示例。



Note 1. 当要支持电池充电规范Rev1.2时，确保VBUS布线宽度足以满足至少1.5A（以粗线显示）。
Note 2. 请使用使VBUS的放电时间在500ms以内的电阻值。
Note 3. USB_VBUS可承受5V。
Note 4. 设计电路板，使总VBUS电容范围为1.0到10µF。

Figure 28.6 支持电池充电规范Rev1.2的功能连接示例

28.3.2 中断源

表28.13列出了USBFS中的中断源。当满足中断产生条件并使用相关的中断使能寄存器使能中断输出时，将向中断控制器单元发出USBFS中断请求并产生USBFS中断。参见第14节，中断控制器单元(ICU)。

Table 28.13 Interrupt sources (1 of 2)

Bit to be set	Name	Interrupt source	Applicable controller function	Status flag
VBINT	VBUS interrupt	• A change in the state of the USB_VBUS input pin was detected (low to high or high to low)	Host or device*1	INTSTS0.VBSTS
RESM	Resume interrupt	• A change in the state of the USB bus was detected in the Suspended state (J-state to K-state or J-state to SE0).	Device	—
SOFR	Frame number update interrupt	In host controller mode: • An SOF packet with a different frame number was transmitted. In device controller mode: • An SOF packet with a different frame number was received.	Host/device	—
DVST	Device state transition interrupt	One of the following device state transitions was detected: • USB bus reset detected • Suspended state detected • SET_ADDRESS request received • SET_CONFIGURATION request received.	Device	INTSTS0.DVSQ[2:0]
CTRT	Control transfer stage transition interrupt	A control transfer stage transition was detected because of one of the following: • Setup stage completed • Control write transfer status stage transition occurred • Control read transfer status stage transition occurred • Control transfer completed • Control transfer sequence error occurred.	Device	INTSTS0.CTSQ[2:0]
BEMP	Buffer empty interrupt	• The buffer is empty after all FIFO buffer data was transmitted • A packet larger than the maximum packet size was received.	Host/device	BEMPSTS.PIPEnBEMP
NRDY	Buffer not ready interrupt	In host controller mode: • A STALL response was received from the peripheral device in response to the issued token • The response from the peripheral device in response to the issued token was not received successfully (no response three times consecutively or packet reception error three times consecutively) • An overrun or underrun error occurred during isochronous transfer In device controller mode: • NAK was returned for an IN or OUT token while the PID[1:0] bits were set to 01b (BUF) • A CRC error or bit stuffing error occurred during data reception in isochronous transfer • An overrun or underrun occurred during data reception in isochronous transfer.	Host/device	NRDYSTS.PIPEnNRDY
BRDY	Buffer ready interrupt	• The buffer is ready (read or write state)	Host/device	BRDYSTS.PIPEnBRDY
OVRCR	Overcurrent input change interrupt	• USB_OVRCURA or USB_OVRCURB input pin state change was detected (low to high or high to low)	Host	INTSTS1.OVRCR
BCHG	Bus change interrupt	• USB bus state change was detected	Host/device	SYSSTS0.LNST[1:0]
DTCH	Disconnection detection during full-speed operation	• Peripheral device disconnect was detected in full-speed operation	Host	DVSTCTR0.RHST[2:0]
ATTCH	Device connection detection	• J-state or K-state was detected on the USB bus for 2.5 µs continuously This interrupt can be used to check whether peripheral devices are connected.	Host	—
EOFERR	EOF error detection	• An EOF error was detected for a peripheral device	Host	—

Table 28.13 中断源(1of2)

要设置的位	Name	中断源	适用控制器功能	状态标志
VBINT	VBUS interrupt	检测到USB_VBUS输入引脚的状态变化（从低到高或从高到低）	主机或设备*1	INTSTS0.VBSTS
RESM	恢复中断	在暂停状态（J状态到K状态或J状态到SE0）中检测到USB总线状态的变化。	Device	—
SOFR	帧号更新中断	在主机控制器模式下： 传输了具有不同帧号的SOF数据包。在设备控制器模式下： 接收到具有不同帧号的SOF数据包。	Host/device	—
DVST	设备状态转换中断	检测到以下设备状态转换之一： 检测到USB总线复位 检测到挂起状态 收到SET_ADDRESS请求 收到SET_CONFIGURATION请求。	Device	INTSTS0.DVSQ[2:0]
CTRT	控制转移阶段转换中断	由于以下原因之一检测到控制传输阶段转换： 设置阶段完成 发生控制写入传输状态阶段转换 发生控制读取传输状态阶段转换 控制传输完成 发生控制传输序列错误。	Device	INTSTS0.CTSQ[2:0]
BEMP	缓冲区空中断	发送完所有FIFO缓冲区数据后缓冲区为空 接收到的数据包大于最大数据包大小。	Host/device	BEMPSTS.PIPEnBEMP
NRDY	缓冲区未就绪中断	在主机控制器模式下： 从外围设备接收到响应发出的令牌的STALL响应 未成功接收到外围设备对发出的令牌的响应（连续3次无响应或3次数据包接收错误 同步传输期间发生溢出或欠载错误在设备控制器模式下： 当PID[1:0]位设置为01b(BUF)时，为IN或OUT令牌返回NAK CRC错误或位填充同步传输的数据接收过程中发生错误 同步传输的数据接收过程中发生溢出或欠载。	Host/device	NRDYSTS.PIPEnNRDY
BRDY	缓冲区就绪中断	缓冲区准备就绪（读或写状态）	Host/device	BRDYSTS.PIPEnBRDY
OVRCR	过流输入变化中断	检测到USB_OVRCURA或USB_OVRCURB输入引脚状态变化（从低到高或从高到低）	Host	INTSTS1.OVRCR
BCHG	总线变化中断	检测到USB总线状态更改	Host/device	SYSSTS0.LNST[1:0]
DTCH	全速运行时的断线检测	在全速运行中检测到外围设备断开连接	Host	DVSTCTR0.RHST[2:0]
ATTCH	设备连接检测	连续2.5µs在USB总线上检测到J状态或K状态此中断可用于检查外围设备是否已连接。	Host	—
EOFERR	EOF错误检测	检测到外围设备的EOF错误	Host	—

Table 28.13 Interrupt sources (2 of 2)

Bit to be set	Name	Interrupt source	Applicable controller function	Status flag
SACK	Normal setup operation	• A setup transaction normal response (ACK) was received	Host	—
SIGN	Setup error	• A setup transaction error (no response or ACK packet corruption) was detected three consecutive times	Host	—
PDDEINT0	Portable device detection interrupt	• A connection of the portable device was detected	Host	INTSTS1.PDDETINT0

Note 1. Although this interrupt can be generated in host controller mode, it is not usually used in this mode.

Table 28.13 中断源（2个中的2个）

要设置的位	Name	中断源	适用控制器功能	状态标志
SACK	正常设置操作	收到设置事务正常响应(ACK)	Host	—
SIGN	设置错误	连续3次检测到设置事务错误（无响应或ACK数据包损坏）	Host	—
PDDEINT0	便携式设备检测中断	检测到便携式设备的连接	Host	INTSTS1.PDDETINT0

Note 1. 虽然在主机控制器模式下可以产生此中断，但通常不会在此模式下使用。

Figure 28.7 shows the circuits related to the USBFS interrupts.

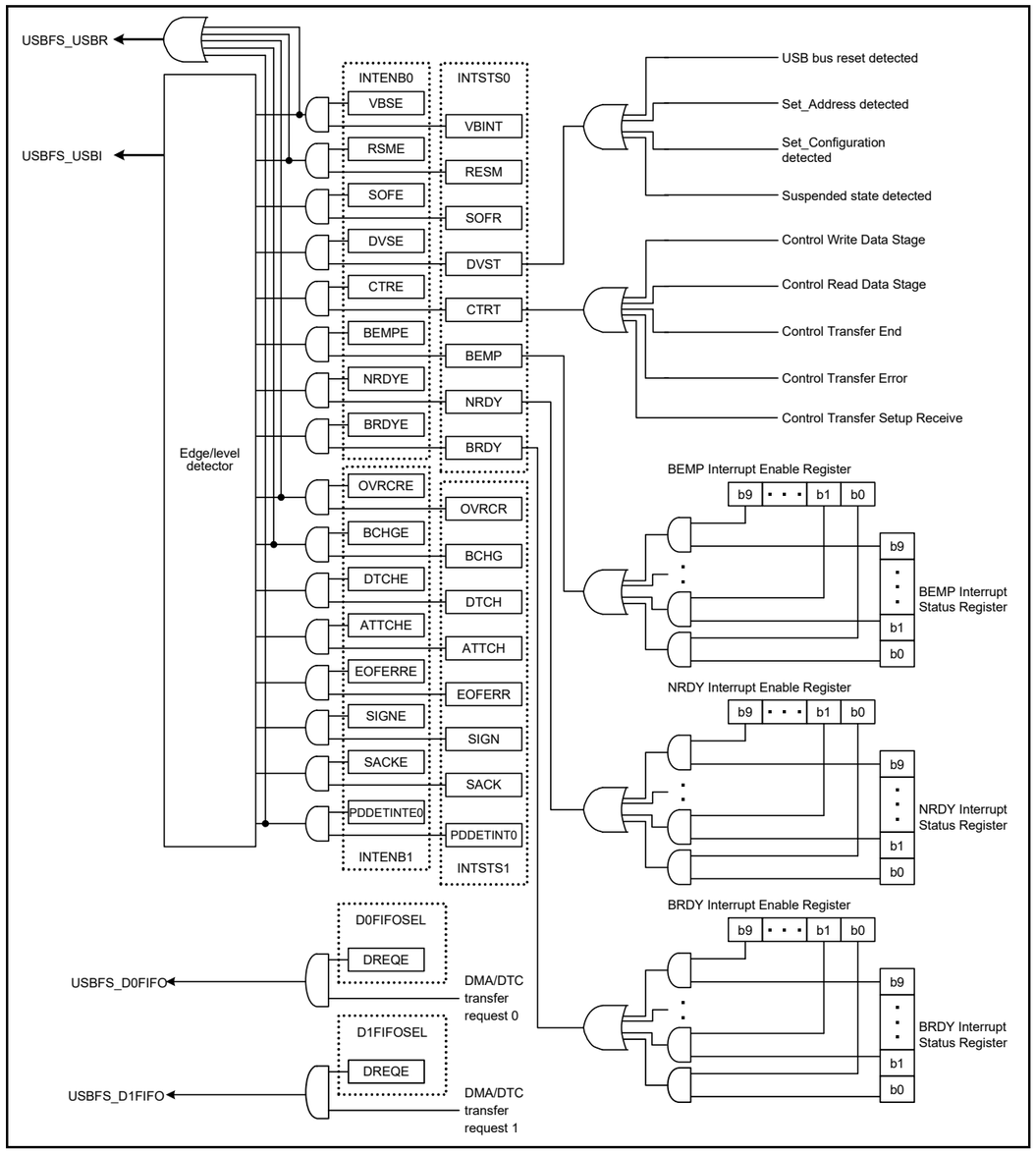


Figure 28.7 USBFS interrupt-related circuits

图28.7显示了与USBFS中断相关的电路。

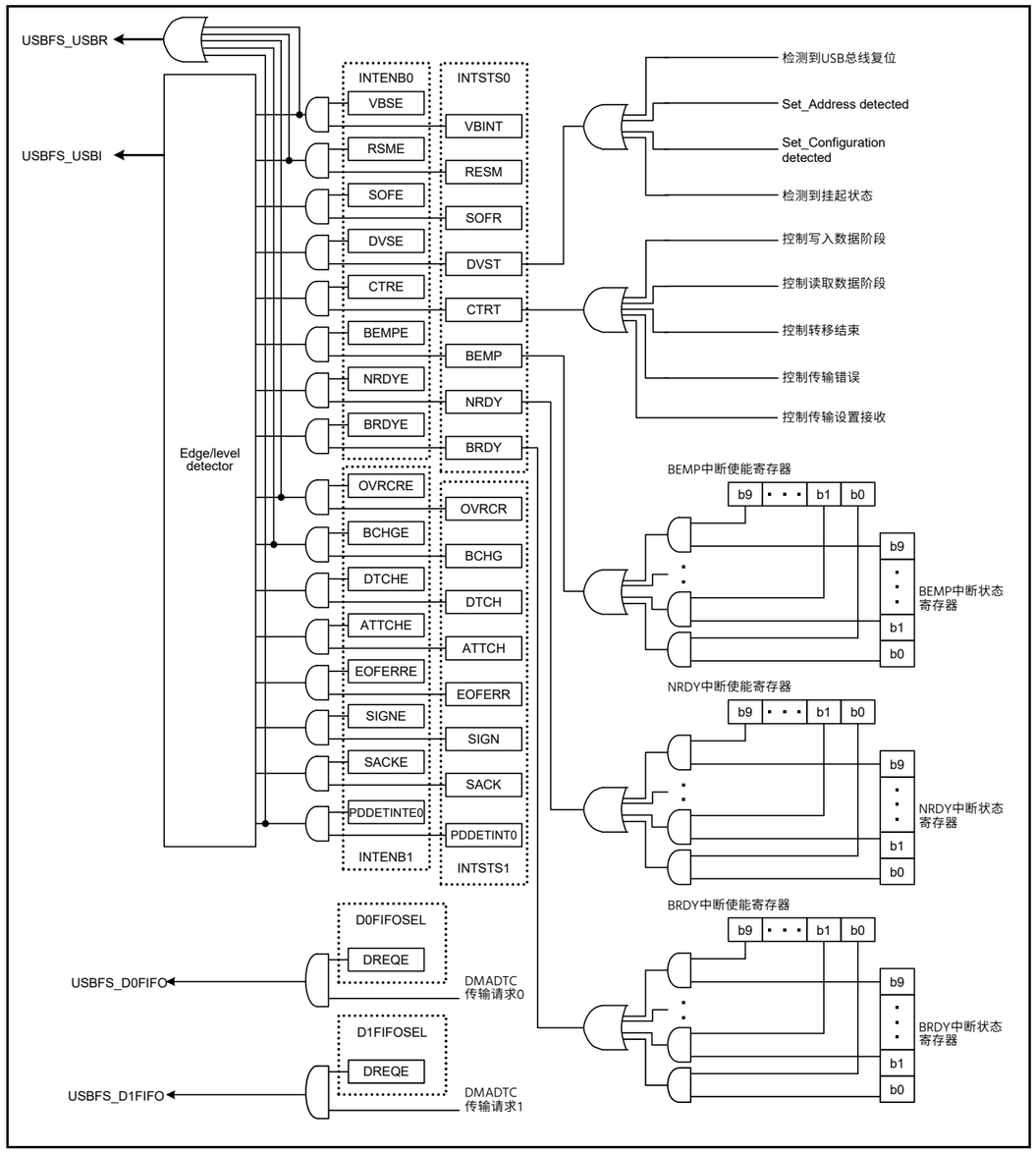


Figure 28.7 USBFS interrupt-related circuits

Table 28.14 shows the interrupts generated by the USBFS.

Table 28.14 USBFS interrupts

Interrupt name	Interrupt status flag	DTC activation	DMAC activation	Priority
D0FIFO	DMA transfer request 0	Possible	Possible	High
D1FIFO	DMA transfer request 1	Possible	Possible	↑
USBFS_USBI	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent input change interrupt, bus change interrupt, disconnection detection during full-speed operation, device connection detection, EOF error detection, normal setup operation, setup error, and portable device detection interrupt	Not possible	Not possible	↓ Low
USBFS_USBR	VBUS interrupt, resume interrupt, overcurrent input change interrupt, and portable device detection interrupt	Not possible	Not possible	—

28.3.3 Interrupt Descriptions

28.3.3.1 BRDY interrupt

The BRDY interrupt is generated in both host and device controller modes. This section describes the conditions in which the USBFS sets the associated bit in BRDYSTS to 1. Under these conditions, the USBFS generates a BRDY interrupt if software sets 1 to the bit in BRDYENB associated with the given pipe, and 1 to the INTENB0.BRDYE bit.

The conditions for generating and clearing the BRDY interrupt depend on the SOFCFG.BRDYM and PIPECFG.BFRE settings for each pipe as follows:

(1) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.

On any of the following conditions, the USBFS generates an internal BRDY interrupt request trigger and sets 1 to the BRDYSTS.PIPEnBRDY bit associated with the selected pipe.

(a) For transmitting pipes

- When the DIR bit is changed from 0 to 1 by software
- When packet transmission is complete for a pipe while write-access from the CPU to the FIFO buffer for the pipe is disabled (when the BSTS bit is read as 0)
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is complete
- When the hardware flushes the buffer of the pipe for isochronous transfers
- When 1 is written to the PIPEnCTR.ACLRM bit, which causes the FIFO buffer to transition from the write-disabled to write-enabled state.

No request trigger is generated for the DCP during data transmission for control transfers.

(b) For receiving pipes

- When packet reception completes successfully therefore, enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the selected pipe is disabled (when the BSTS bit is read as 0). No request trigger is generated for transactions in which a DATA-PID mismatch has occurred.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode. No request trigger is generated until completion of reading data from the currently-read FIFO buffer, even if reception by the other FIFO buffer completes.

In device controller mode, the BRDY interrupt is not generated in the status stage of control transfers. The PIPEnBRDY

表28.14显示了USBFS产生的中断。

Table 28.14 USBFS interrupts

中断名称	中断状态标志	DTC activation	DMAC activation	Priority
D0FIFO	DMA传输请求0	Possible	Possible	High
D1FIFO	DMA传输请求1	Possible	Possible	↑
USBFS_USBI	VBUS中断、恢复中断、帧号更新中断、设备状态转移中断、控制转移阶段转移中断、缓冲器空中断、 缓冲器未就绪中断、缓冲器就绪中断、过流输入改变中断、总线改变中断、全速期间断开检测操作、设备连接检测、EOF错误检测、正常设置操作、设置错误和便携式设备检测中断	不可能	不可能	↓ Low
USBFS_USBR	VBUS中断、恢复中断、过流输入变化中断、便携设备检测中断	不可能	不可能	—

28.3.3 中断说明

28.3.3.1 BRDY interrupt

在主机和设备控制器模式下都会产生BRDY中断。本节描述USBFS将BRDYSTS中的相关位设置为1的条件。在这些条件下，如果软件将BRDYENB中与给定管道相关的位设置为1，并且将INTENB0.BRDYE设置为1，USBFS将生成BRDY中断少量。

产生和清除BRDY中断的条件取决于每个管道的SOFCFG.BRDYM和PIPECFG.BFRE设置，如下所示：

(1) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=0时

通过这些设置，BRDY中断指示FIFO端口可访问。

在以下任一条件下，USBFS产生内部BRDY中断请求触发并将1设置为BRDYSTS.PIPEnBRDY位与所选管道相关联。

(a) 用于传输管道

- 当DIR位由软件从0变为1时
- 当管道的数据包传输完成而从CPU到管道的FIFO缓冲区的写访问被禁用时（当BSTS位被读取为0时）
- 双缓冲模式下，当一个FIFO缓冲区在完成向另一个FIFO缓冲区写入数据时为空时
- 直到完成向当前写入的FIFO缓冲区写入数据之前，不会生成请求触发，即使传输到另一个FIFO缓冲区已完成
- 当硬件刷新管道缓冲区以进行同步传输时
- 当1写入PIPEnCTR.ACLRM位时，这会导致FIFO缓冲区从写禁止状态转换为写使能状态。

在控制传输的数据传输期间，不会为DCP生成请求触发。

(b) 用于接收管道

- 因此，当数据包接收成功完成时，允许读取FIFO缓冲区，同时禁止从CPU对所选管道的FIFO缓冲区的读取访问（当BSTS位被读取为0时）。对于发生DATA-PID不匹配的事务，不会生成请求触发器。
- 当一个FIFO缓冲区在双缓冲区模式下完成从另一个FIFO缓冲区读取数据后启用读取。在从当前读取的FIFO缓冲区读取数据完成之前，不会生成请求触发，即使其他FIFO缓冲区的接收完成也是如此。

在设备控制器模式下，在控制传输的状态阶段不会产生BRDY中断。PIPEnBRDY

interrupt status of the selected pipe can be set to 0 by writing 0 to the associated PIPEnBRDY bit through software. In this case, write 1 to the PIPEnBRDY bits for the other pipes. Clear the BRDY status before accessing the FIFO buffer.

(2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1

With these settings, the USBFS generates a BRDY interrupt on completion of reading all data for a single transfer using the receiving pipe, and sets 1 to the bit in BRDYSTS associated with the selected pipe.

On any of the following conditions, the USBFS determines that the last data for a single transfer was received:

- When a short packet including a zero-length packet is received
- When the PIPEn transaction counter register (PIPEnTRN) is used and the number of packets specified in the PIPEnTRN.TRNCNT[15:0] bits are completely received.

When the data is completely read after any of the above conditions is satisfied, the USBFS determines that all data for a single transfer is completely read.

When a zero-length packet is received while the FIFO buffer is empty, the USBFS determines that all data for a single transfer is completely read when the FRDY bit in the FIFO Port Control Register is 1 and the DTLN[8:0] bits are 0. In this case, to start the next transfer, write 1 to the BCLR bit in the associated Port Control Register through software. With these settings, the USBFS does not detect a BRDY interrupt for the transmitting pipe.

The PIPEnBRDY interrupt status of a pipe can be set to 0 by writing 0 to the associated BRDYSTS.PIPEnBRDY bit through software. In this case, the other PIPEnBRDY bits for the other pipes must be set to 1.

In this mode, do not change the PIPECFG.BFRE bit setting until all data for a single transfer is processed. When it is required to change the PIPECFG.BFRE bit before completion of processing, all FIFO buffers for the pipe must be cleared using the PIPEnCTR.ACLRM bit.

(3) When SOFCFG.BRDYM = 1 and PIPECFG.BFRE = 0

With these settings, the BRDYSTS.PIPEnBRDY values are linked to the BSTS bit setting for each pipe. In other words, the BRDY interrupt status bits (PIPEnBRDY) are set to 1 or 0 by the USB depending on the FIFO buffer status.

(a) For transmitting pipes

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for write access, and are set to 0 when it is not ready. The BRDY interrupt is not generated for the DCP in the transmitting direction even when it is ready for write access.

(b) For receiving pipes

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for read access, and are set to 0 when all data are read (not ready for read access).

When a zero-length packet is received while the FIFO buffer is empty, the associated bit is set to 1 and the BRDY interrupt is continuously generated until software writes 1 to BCLR. With this setting, the PIPEnBRDY bit cannot be set to 0 by software. When the SOFCFG.BRDYM bit is set to 1, set the PIPECFG.BFRE bit for all pipes to 0.

通过软件将0写入相关的PIPEnBRDY位，可以将所选管道的中断状态设置为0。在这种情况下，将1写入其他管道的PIPEnBRDY位。在访问FIFO缓冲区之前清除BRDY状态。

(2) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=1时

使用这些设置，USBFS在完成使用接收管道读取所有数据以进行单次传输时生成BRDY中断，并将BRDYSTS中与所选管道关联的位设置为1。

在以下任何一种情况下，USBFS都会确定接收到单次传输的最后一个数据：

- 当接收到包含零长度数据包的短数据包时
- 当使用PIPEn事务计数器寄存器(PIPEnTRN)并且在PIPEnTRN.TRNCNT[15:0]位被完全接收。

满足以上任一条件后，当数据全部读取完毕时，USBFS判断单次传输的所有数据全部读取完毕。

当FIFO缓冲区为空时接收到零长度数据包时，当FIFO端口控制寄存器中的FRDY位为1且DTLN[8:0]位为0.在这种情况下，要开始下一次传输，通过软件将1写入相关端口控制寄存器中的BCLR位。使用这些设置，USBFS不会检测到传输管道的BRDY中断。

通过软件将0写入相关的BRDYSTS.PIPEnBRDY位，可以将管道的PIPEnBRDY中断状态设置为0。在这种情况下，其他管道的其他PIPEnBRDY位必须设置为1。

在此模式下，在处理完单次传输的所有数据之前，不要更改PIPECFG.BFRE位设置。当需要在处理完成之前更改PIPECFG.BFRE位时，必须使用PIPEnCTR.ACLRM位清除管道的所有FIFO缓冲区。

(3) 当SOFCFG.BRDYM=1且PIPECFG.BFRE=0时

通过这些设置，BRDYSTS.PIPEnBRDY值链接到每个管道的BSTS位设置。换言之，BRDY中断状态位(PIPEnBRDY)由USB设置为1或0，具体取决于FIFO缓冲区状态。

(a) 用于传输管道

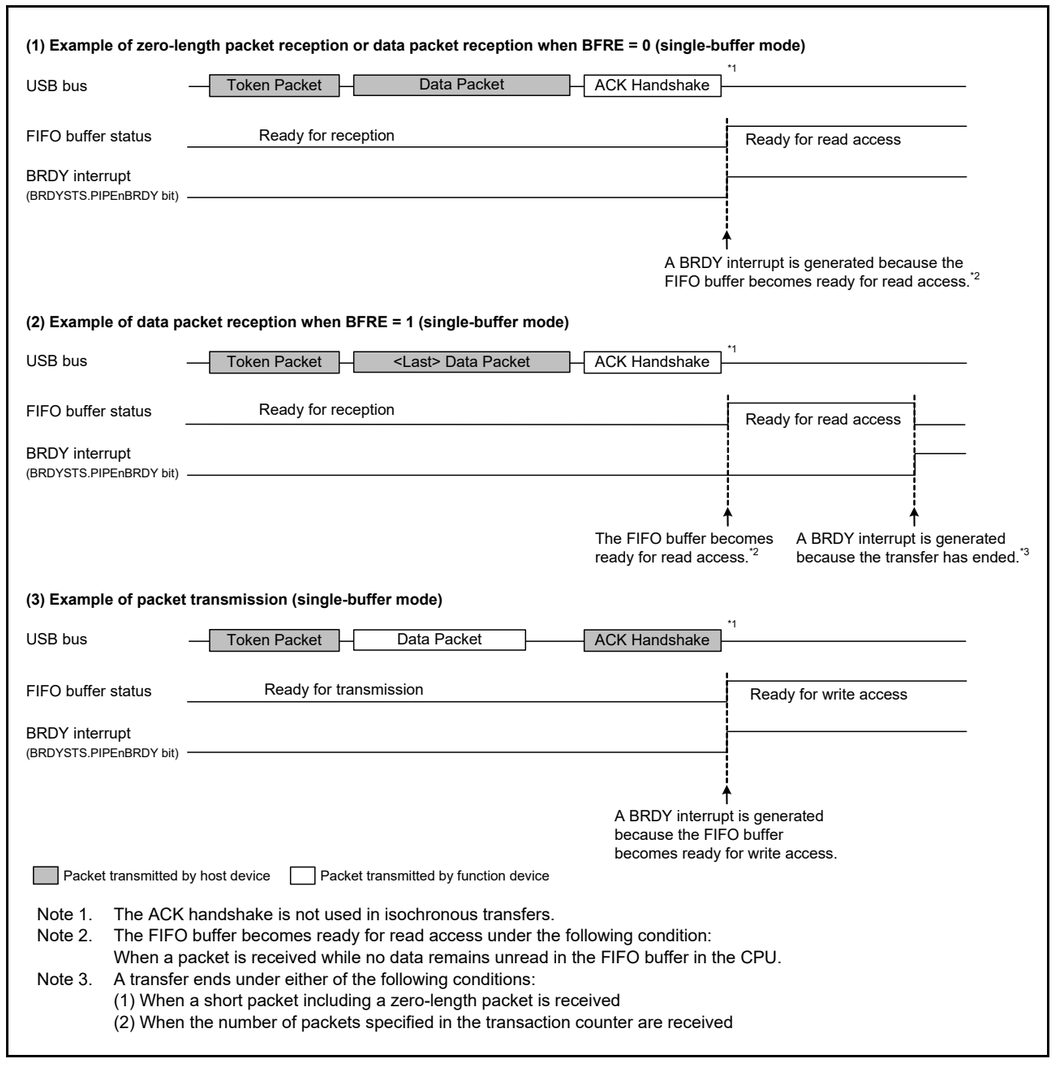
当FIFO缓冲区准备好进行写访问时，BRDY中断状态位设置为1，当它未准备好时设置为0。发送方向上的DCP不会产生BRDY中断，即使它已准备好进行写访问。

(b) 用于接收管道

当FIFO缓冲区准备好进行读访问时，BRDY中断状态位设置为1，当所有数据都读完（未准备好进行读访问）时，BRDY中断状态位设置为0。

当FIFO缓冲区为空时接收到零长度数据包时，相关位设置为1，并且持续产生BRDY中断，直到软件将1写入BCLR。使用此设置，PIPEnBRDY位不能通过软件设置为0。当SOFCFG.BRDYM位设置为1时，将所有管道的PIPECFG.BFRE位设置为0。

Figure 28.8 shows the timing of BRDY interrupt generation.



Note 1. The ACK handshake is not used in isochronous transfers.
Note 2. The FIFO buffer becomes ready for read access under the following condition:
When a packet is received while no data remains unread in the FIFO buffer in the CPU.
Note 3. A transfer ends under either of the following conditions:
(1) When a short packet including a zero-length packet is received
(2) When the number of packets specified in the transaction counter are received

Figure 28.8 Timing of BRDY interrupt generation

The condition for clearing the INTSTS0.BRDY bit depends on the SOFCFG.BRDYM bit setting as shown in Table 28.15.

Table 28.15 Condition for clearing BRDY bit

BRDYM bit	Condition for clearing BRDY bit
0	When all bits in BRDYSTS are set to 0 by software
1	When the BSTS bits for all pipes become 0

图28.8显示了BRDY中断产生的时序。

Note 1. ACK握手不用于同步传输。
Note 2. 在以下条件下，FIFO缓冲区准备好进行读取访问：
当CPU的FIFO缓冲区中没有未读取的数据时接收到数据包。
Note 3. 传输在以下任一条件下结束：(1)当接收到包含零长度数据包的短数据包时(2)当接收到事务计数器中指定数量的数据包时

Figure 28.8 BRDY中断产生的时序

清除INTSTS0.BRDY位的条件取决于SOFCFG.BRDYM位设置，如表28.15所示。

Table 28.15 清除BRDY位的条件

BRDYM bit	清除BRDY位的条件
0	当BRDYSTS中的所有位由软件设置为0时
1	当所有管道的BSTS位变为0时

28.3.3.2 NRDY interrupt

On generating an internal NRDY interrupt request for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated PIPEnNRDY bit in NRDYSTS to 1. If the associated bit in NRDYENB is set to 1 by software, the USBFS sets the INTSTS0.NRDY bit to 1 and generates a USBFS interrupt.

This section describes the conditions in which the USBFS generates the internal NRDY interrupt request for a given pipe.

The internal NRDY interrupt request is not generated during setup transaction execution in host controller mode. During setup transactions in host controller mode, the SACK or SIGN interrupt is detected.

The internal NRDY interrupt request is not generated during status stage execution of the control transfer in device controller mode.

(1) In host controller mode

(a) For transmitting pipes

On any of the following conditions, the USBFS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBFS transmits a zero-length packet following the OUT token and sets the associated NRDYSTS.PIPEnNRDY bit and the FRMNUM.OVRN bit to 1.
- During communications other than setup transactions on pipes not used for isochronous transfers, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device
  - An error is detected in the packet from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the associated PID[1:0] setting for the pipe to NAK.
- During communications other than setup transactions, when the STALL handshake is received from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the PID[1:0] setting for the associated pipe to STALL (11b).

(b) For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBFS discards the received data for the IN token and sets the PIPEnNRDY bit associated with the pipe and the OVRN bit to 1. When a packet error is detected in the received data for the IN token, the USBFS also sets the FRMNUM.CRCE bit to 1.
- For non-isochronous transfer pipes, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device for the IN token issued by the USBFS (when timeout is detected before detection of the DATA packet from the peripheral device)
  - An error is detected in the packet from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the associated PID[1:0] setting for the pipe to NAK.
- For isochronous transfer pipes, when no response is returned from the peripheral device for the IN token (when timeout is detected before detection of the DATA packet from the peripheral device) or an error is detected in the packet from the peripheral device. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe to 1. The PID[1:0] setting for the pipe is not changed.
- For isochronous transfer pipes, when a CRC error or a bit stuffing error is detected in the received data packet. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe and the CRCE bit to 1.
- When the STALL handshake is received. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe to 1 and changes the PID[1:0] setting for the associated pipe to STALL.

28.3.3.2 NRDY interrupt

在为PID位由软件设置为BUF的管道生成内部NRDY中断请求时，USBFS将NRDYSTS中的相关PIPEnNRDY位设置为1。如果NRDYENB中的相关位由软件设置为1，则USBFS设置INTSTS0.NRDY位为1并产生USBFS中断。

本节描述USBFS为给定管道生成内部NRDY中断请求的条件。

内部NRDY中断请求在主控制器模式下的设置事务执行期间不会产生。在主机控制器模式下的设置事务期间，检测到SACK或SIGN中断。

在设备控制器模式下控制传输的状态阶段执行期间，不会产生内部NRDY中断请求。

(1) 在主机控制器模式下

(a) 用于传输管道

在以下任何一种情况下，USBFS都会检测到NRDY中断：

- 对于同步传输管道，当发出OUT令牌的时间到来时，FIFO缓冲区中没有要传输的数据。在这种情况下，USBFS在OUT令牌之后发送一个长度为零的数据包，并将相关的NRDYSTS.PIPEnNRDY位和FRMNUM.OVRN位设置为1。
- 在不用于同步传输的管道上的设置事务以外的通信期间，当以下两种情况的任意组合连续发生3次时：
  - 外围设备没有返回响应（当在检测到来自外围设备的握手包之前检测到超时时
  - 在来自外围设备的数据包中检测到错误。在这种情况下，USBFS设置关联的PIPEnNRDY位为1并将管道的相关PID[1:0]设置更改为NAK。
- 在设置事务以外的通信期间，当从外围设备接收到STALL握手时。在这种情况下，USBFS将相关的PIPEnNRDY位设置为1，并将相关管道的PID[1:0]设置更改为STALL(11b)。

(b) 用于接收管道

- 对于同步传输管道，当发出IN令牌的时间到来但FIFO缓冲区中没有可用空间时。在这种情况下，USBFS丢弃接收到的IN令牌数据，并将与管道关联的PIPEnNRDY位和OVRN位设置为1。当在接收到的IN令牌数据中检测到数据包错误时，USBFS也会设置FRMNUM.CRCE位为1。
- 对于非等时传输管道，当下列两种情况的任意组合连续出现3次时：
  - USBFS发出的IN令牌没有从外围设备返回响应（当在检测到来自外围设备的DATA包之前检测到超时时）
  - 在来自外围设备的数据包中检测到错误。在这种情况下，USBFS设置关联的PIPEnNRDY位为1并将管道的相关PID[1:0]设置更改为NAK。
- 对于同步传输管道，当外围设备没有返回对IN令牌的响应时（在检测到来自外围设备的DATA数据包之前检测到超时）或在来自外围设备的数据包中检测到错误。在这种情况下，USBFS将与管道关联的PIPEnNRDY位设置为1。管道的PID[1:0]设置不会更改。
- 对于同步传输管道，当在接收到的数据包中检测到CRC错误或位填充错误时。在这种情况下，USBFS将与管道关联的PIPEnNRDY位和CRCE位设置为1。
- 当收到STALL握手时。在这种情况下，USBFS将与管道关联的PIPEnNRDY位设置为1，并将关联管道的PID[1:0]设置更改为STALL。

(2) In device controller mode

(a) For transmitting pipes

- When an IN token is received while there is no data to be transmitted in the FIFO buffer. In this case, the USBFS generates a NRDY interrupt request on reception of the IN token and sets the NRDYSTS.PIPEnNRDY bit to 1. For an isochronous transfer pipe in which an interrupt is generated, the USBFS transmits a zero-length packet and sets the FRMNUM.OVRN bit to 1.

(b) For receiving pipes

- When an OUT token is received but there is no space available in the FIFO buffer. For an isochronous transfer pipe in which an interrupt is generated, the USBFS generates a NRDY interrupt request on reception of the OUT token and sets the PIPEnNRDY bit to 1 and OVRN bit to 1. For a non-isochronous transfer pipe in which an interrupt is generated, the USBFS generates a NRDY interrupt request when a NAK handshake is transferred after the data following the OUT token is received, and sets the PIPEnNRDY bit to 1. The NRDY interrupt request is not generated during retransmission because of a DATA-PID mismatch. In addition, the NRDY interrupt request is not generated if an error occurs in the DATA packet.
- For isochronous transfer pipes, when a token is not received successfully within an interval frame. In this case, the USBFS generates an NRDY interrupt request when the SOF is received, and sets the PIPEnNRDY bit to 1.

Figure 28.9 shows the timing of NRDY interrupt generation when the device controller is selected.

(2) 在设备控制器模式下

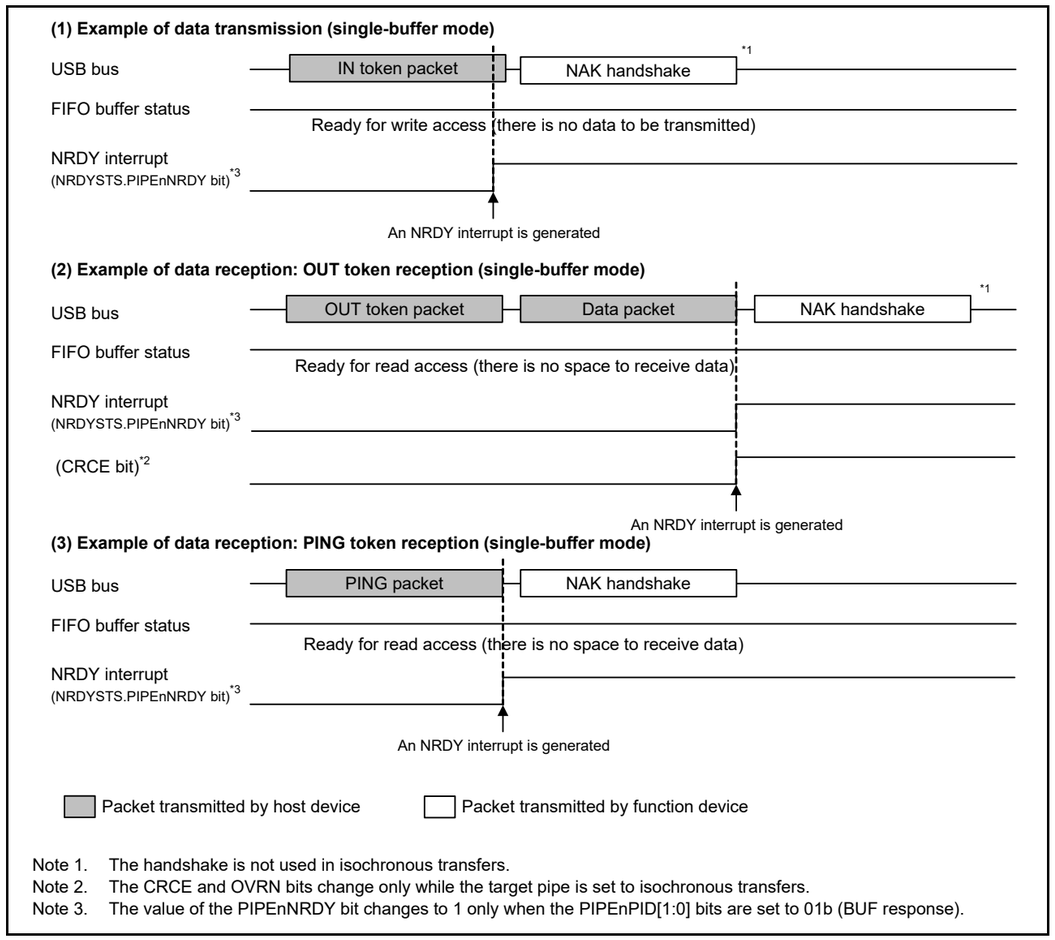
(a) 用于传输管道

- 当FIFO缓冲区中没有要传输的数据时接收到IN令牌。在这种情况下，USBFS在接收到IN令牌时产生一个NRDY中断请求，并将NRDYSTS.PIPEnNRDY位设置为1。对于产生中断的同步传输管道，USBFS发送一个长度为零的数据包并将FRMNUM.OVRN位为1。

(b) 用于接收管道

- 当接收到OUT令牌但FIFO缓冲区中没有可用空间时。对于产生中断的同步传输管道，USBFS在接收到OUT令牌时产生一个NRDY中断请求，并将PIPEnNRDY位设置为1，并将OVRN位设置为1。USBFS在接收到OUT令牌之后的数据后，在传输NAK握手时产生NRDY中断请求，并将PIPEnNRDY位设置为1。由于DATA-PID不匹配，重传期间不会产生NRDY中断请求。此外，如果DATA包发生错误，则不会产生NRDY中断请求。
- 对于同步传输管道，当在间隔帧内未成功接收到令牌时。在这种情况下，USBFS在接收到SOF时产生一个NRDY中断请求，并将PIPEnNRDY位设置为1。

图28.9显示了选择设备控制器时NRDY中断产生的时序。



Note 1. The handshake is not used in isochronous transfers.
Note 2. The CRCE and OVRN bits change only while the target pipe is set to isochronous transfers.
Note 3. The value of the PIPEnNRDY bit changes to 1 only when the PIPEnPID[1:0] bits are set to 01b (BUF response).

Figure 28.9 Timing of NRDY interrupt generation in device controller mode

28.3.3.3 BEMP interrupt

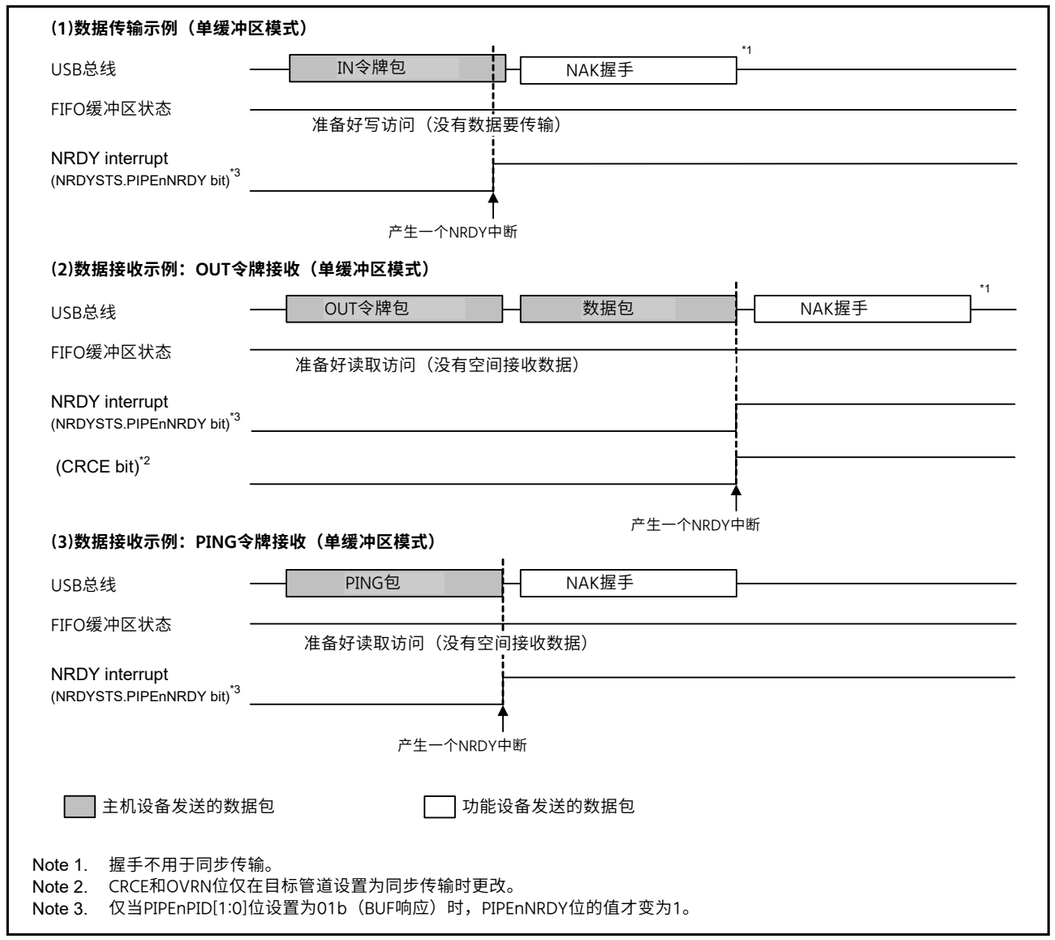
On detecting a BEMP interrupt for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated BEMPSTS.PIPEnBEMP bit to 1. If the associated bit in BEMPENB is set to 1 by software, the USBFS sets the INTSTS0.BEMP bit to 1 and generates a USBFS interrupt. This section describes the conditions in which the USBFS generates an internal BEMP interrupt request.

(1) For transmitting pipes

When the FIFO buffer of the associated pipe is empty on completion of transmission, including zero-length packet transmission, and in single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for a non-DCP pipe.

The internal BEMP interrupt request is not generated on any of the following conditions:

- When the CPU or DMA/DTC has already started writing data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode
- When the buffer is cleared (emptied) by setting the PIPEnCTR.ACLRM or the BCLR bit in the port control register to 1
- When an IN transfer (zero-length packet transmission) is performed during the control transfer status stage in device



Note 1. 握手不用于同步传输。
Note 2. CRCE和OVRN位仅在目标管道设置为同步传输时更改。
Note 3. 仅当PIPEnPID[1:0]位设置为01b（BUF响应）时，PIPEnNRDY位的值才变为1。

Figure 28.9 设备控制器模式下NRDY中断产生的时序

28.3.3.3 BEMP interrupt

在检测到PID位被软件设置为BUF的管道的BEMP中断时，USBFS将相关的BEMPSTS.PIPEnBEMP位设置为1。如果BEMPENB中的相关位被软件设置为1，USBFS将设置
INTSTS0.BEMP位为1并产生USBFS中断。本节介绍USBFS产生内部BEMP中断请求的条件。

(1) 用于传输管道

当相关管道的FIFO缓冲区在传输完成时为空时，包括零长度数据包传输，并且在单缓冲区模式下，内部BEMP中断请求与非DCP管道的BRDY中断同时生成。

在以下任何情况下都不会产生内部BEMP中断请求：

- 当CPU或DMADTC在双缓冲模式下从一个FIFO缓冲区完成数据传输后已经开始向CPU的FIFO缓冲区写入数据时
- 当通过将端口控制寄存器中的PIPEnCTR.ACLRM或BCLR位设置为1来清除（清空）缓冲区时
- 在设备的控制传输状态阶段执行IN传输（零长度数据包传输）时

controller mode.

(2) For receiving pipes

When a successfully-received data packet size exceeds the specified maximum packet size. In this case, the USBFS generates a BEMP interrupt request, sets the associated BEMPSTS.PIPEnBEMP bit to 1, discards the received data, and changes the associated PID[1:0] setting for the pipe to STALL (11b). The USBFS returns no response in host controller mode, and returns STALL response in device controller mode.

The internal BEMP interrupt request is not generated on any of the following conditions:

- When a CRC error or a bit stuffing error is detected in the received data
- When a setup transaction is performed:
  - Writing 0 to the BEMPSTS.PIPEnBEMP bit clears the status
  - Writing 1 to the BEMPSTS.PIPEnBEMP bit has no effect.

Figure 28.10 shows the timing of BEMP interrupt generation in device controller mode.

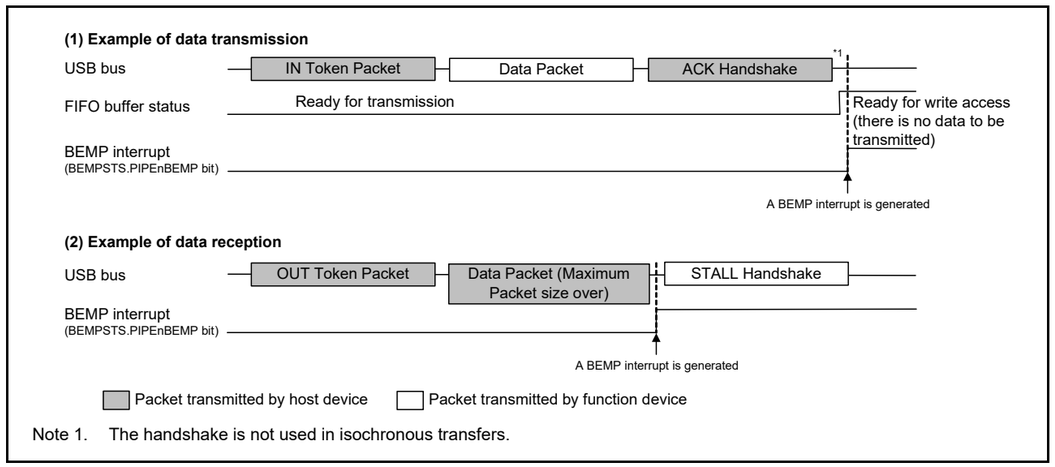


Figure 28.10 Timing of BEMP interrupt generation in device controller mode

28.3.3.4 Device state transition interrupt (device controller mode)

Figure 28.11 shows a diagram of device state transitions in the USBFS. The USBFS controls device states and generates device state transition interrupts. However, recovery from the suspended state (resume signal detection) is detected by means of the resumed interrupt. Device state transition interrupts can be enabled or disabled independently in INTENB0. Devices whose states have changed can be checked in the INTSTS0.DVSQ[2:0] bits.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is detected.

The USBFS controls device states, and device state transition interrupts can be generated, only in device controller mode.

控制器模式。

(2) 用于接收管道

当成功接收的数据包大小超过指定的最大包大小时。在这种情况下，USBFS生成一个BEMP中断请求，将相关的BEMPSTS.PIPEnBEMP位设置为1，丢弃接收到的数据，并将管道的相关PID[1:0]设置更改为STALL(11b)。USBFS在主机控制器模式下不返回响应，在设备控制器模式下返回STALL响应。

在以下任何情况下都不会产生内部BEMP中断请求：

- 在接收到的数据中检测到CRC错误或位填充错误时
- 执行设置事务时：
  - 将0写入BEMPSTS.PIPEnBEMP位可清除状态
  - 向BEMPSTS.PIPEnBEMP位写入1无效。

图28.10显示了设备控制器模式下BEMP中断产生的时序。

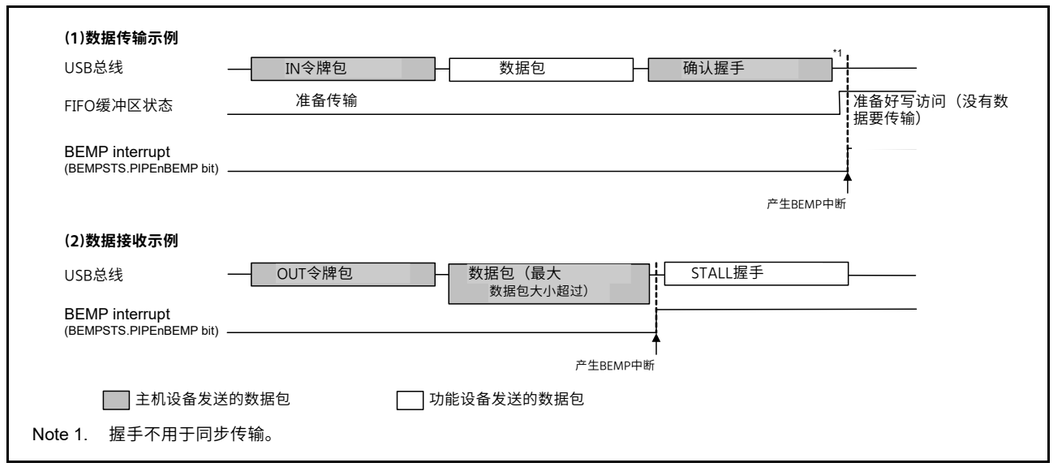


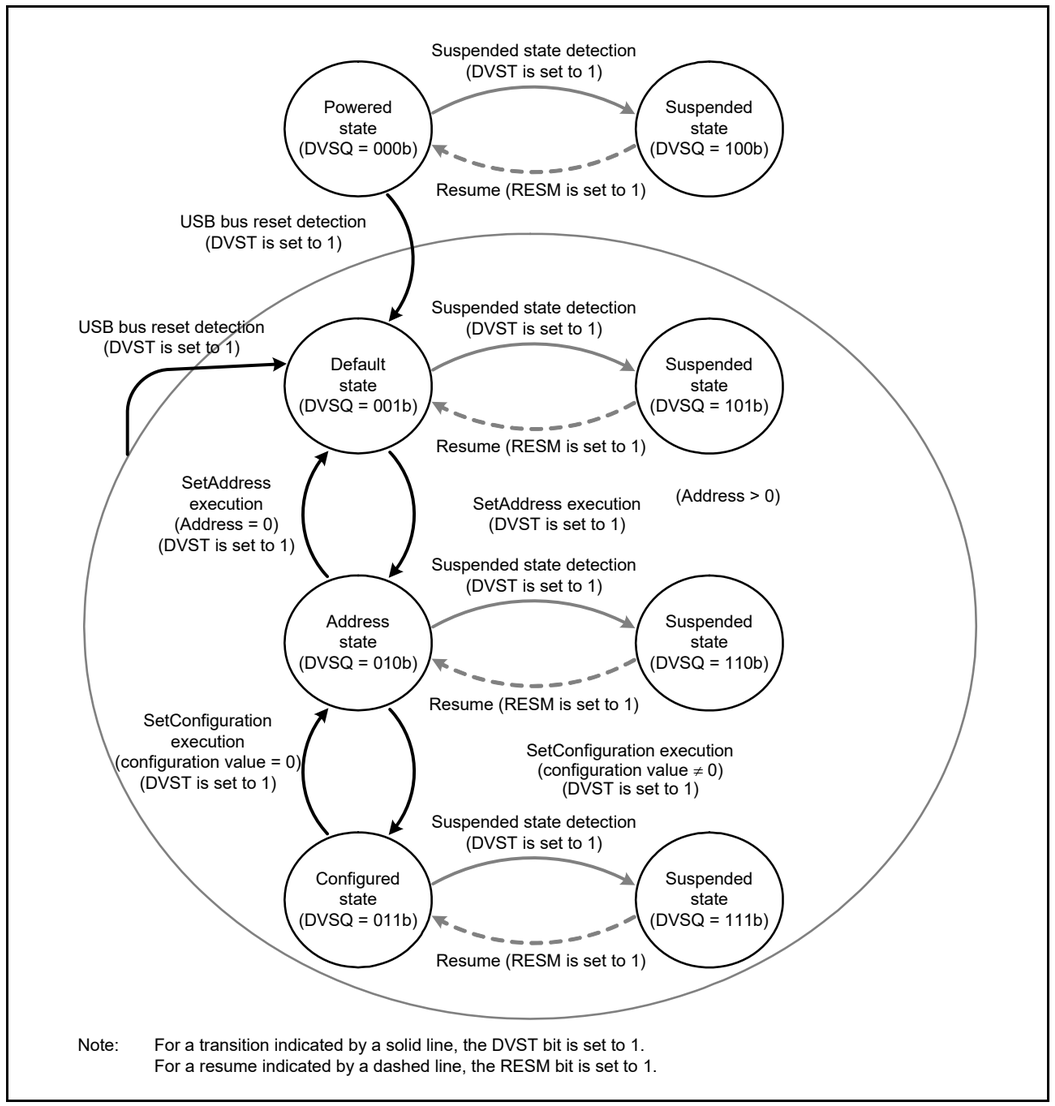
Figure 28.10 设备控制器模式下BEMP中断产生的时序

28.3.3.4 设备状态转换中断（设备控制器模式）

图28.11显示了USBFS中的设备状态转换图。USBFS控制设备状态并产生设备状态转换中断。然而，通过恢复中断检测从暂停状态的恢复（恢复信号检测）。可以在INTENB0中独立启用或禁用设备状态转换中断。可以在INTSTS0.DVSQ[2:0]位中检查状态已更改的设备。

当转换到默认状态时，检测到USB总线复位后会产生设备状态转换中断。

USBFS控制设备状态，并且只能在设备控制器模式下产生设备状态转换中断。



Note: For a transition indicated by a solid line, the DVST bit is set to 1.
For a resume indicated by a dashed line, the RESM bit is set to 1.

Figure 28.11 Device state transitions

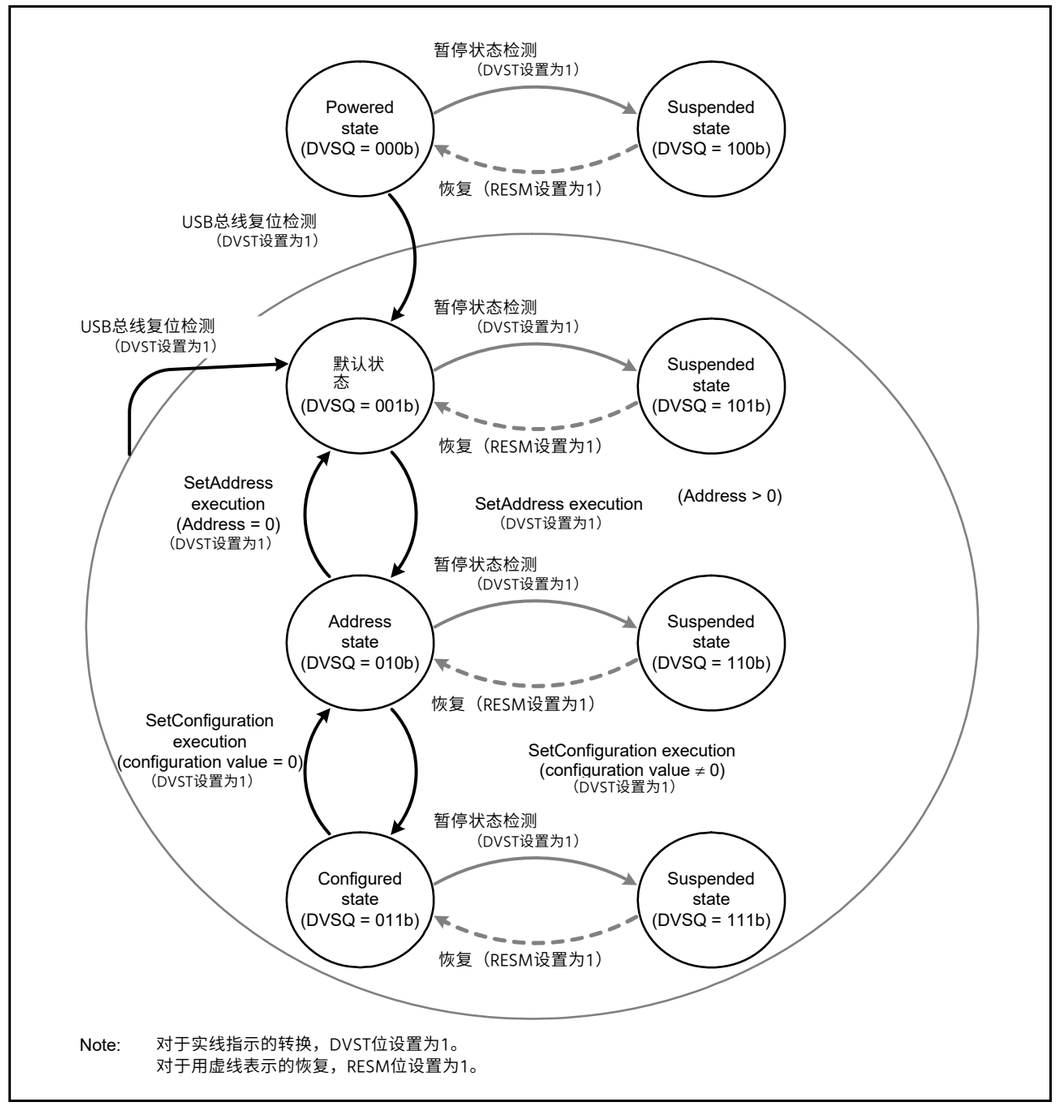
28.3.3.5 Control transfer stage transition interrupt (device controller mode)

Figure 28.12 shows a diagram of the control transfer stage transitions of the USBFS. The USBFS controls the control transfer sequence and generates control transfer stage transition interrupts. Control transfer stage transition interrupts can be enabled or disabled independently in INTENB0. Transfer stages that have transitioned can be checked in the INTSTS0.CTSQ[2:0] bits.

Control transfer stage transition interrupts are generated only in device controller mode. This section describes control transfer sequence errors. When an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).

(1) Control read transfer errors

- An OUT token is received but no data is transferred in response to the IN token at the data stage



Note: 对于实线指示的转换，DVST位设置为1。
对于用虚线表示的恢复，RESM位设置为1。

Figure 28.11 设备状态转换

28.3.3.5 控制转移阶段转换中断（设备控制器模式）

图28.12显示了USBFS的控制传输阶段转换图。USBFS控制控制传输序列并产生控制传输阶段转换中断。控制转移阶段转换中断可以在INTENB0中独立启用或禁用。可以在INTSTS0.CTSQ[2:0]位中检查已转换的传输阶段。

控制转移阶段转换中断仅在设备控制器模式下产生。本节描述控制传输序列错误。发生错误时，DCPCTR.PID[1:0]位设置为1xb（STALL响应）。

(1) 控制读取传输错误

- 接收到OUT令牌，但在数据阶段没有响应IN令牌传输数据

- An IN token is received at the status stage
- A data packet with DATAPID = DATA0 is received at the status stage.

(2) Control write transfer errors

- An IN token is received but no ACK is returned in response to the OUT token at the data stage
- A data packet with DATAPID = DATA0 is received as the first data packet at the data stage
- An OUT token is received at the status stage.

(3) Control write no data transfer errors

- An OUT token is received at the status stage.

At the control write transfer data stage, if the receive data length exceeds the wLength value of the USB request, it cannot be recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT = 1), the CTSQ[2:0] = 110b value is saved until the CTRT bit is set to 0, clearing the interrupt status. While CTSQ[2:0] = 110b is being saved, no CTRT interrupt for ending the setup stage is generated even when a new USB request is received. The USBFS saves the setup stage completion status, and generates a CTRT interrupt after software clears the interrupt status.

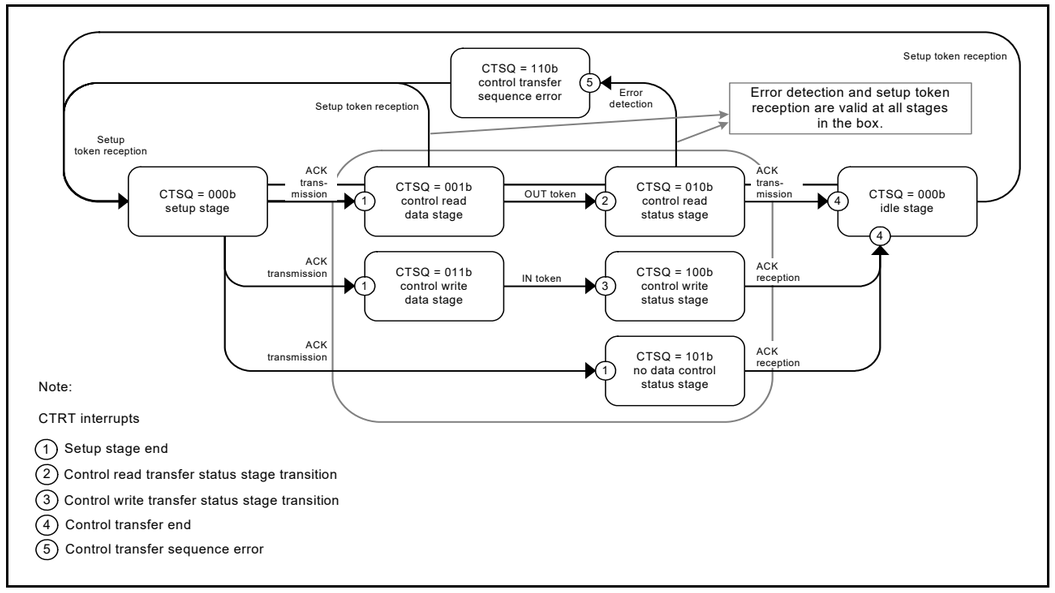


Figure 28.12 Control transfer stage transitions

28.3.3.6 Frame update interrupt

In host controller mode, an interrupt is generated when the frame number is updated.

In device controller mode, an SOFR interrupt is generated when the frame number is updated. The USBFS updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

28.3.3.7 VBUS interrupt

When the USB_VBUS pin level changes, a VBUS interrupt is generated. The level of the USB_VBUS pin can be checked with the INTSTS0.VBSTS bit. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. If the system is activated with the host controller connected, the first VBUS interrupt is not generated, because there is no change in the USB_VBUS pin level.

- 在状态阶段收到一个IN令牌
- 在状态阶段接收到一个DATAPID=DATA0的数据包。

(2) 控制写入传输错误

- 在数据阶段接收到IN令牌但没有返回ACK以响应OUT令牌
- DATAPID=DATA0的数据包作为数据阶段的第一个数据包被接收
- 在状态阶段收到一个OUT令牌。

(3) 控制写入无数据传输错误

- 在状态阶段收到一个OUT令牌。

在控制写传输数据阶段，如果接收到的数据长度超过USB请求的wLength值，则不能被识别为控制传输序列错误。在控制读取传输状态阶段，除了零长度数据包之外的数据包被一个ACK响应接收并且传输正常结束。

当CTRT中断响应序列错误(INTSTS0.CTRT=1)时，将保存CTSQ[2:0]=110b值，直到CTRT位设置为0，清除中断状态。在保存CTSQ[2:0]=110b时，即使收到新的USB请求，也不会产生用于结束设置阶段的CTRT中断。USBFS保存设置阶段完成状态，并在软件清除中断状态后产生CTRT中断。

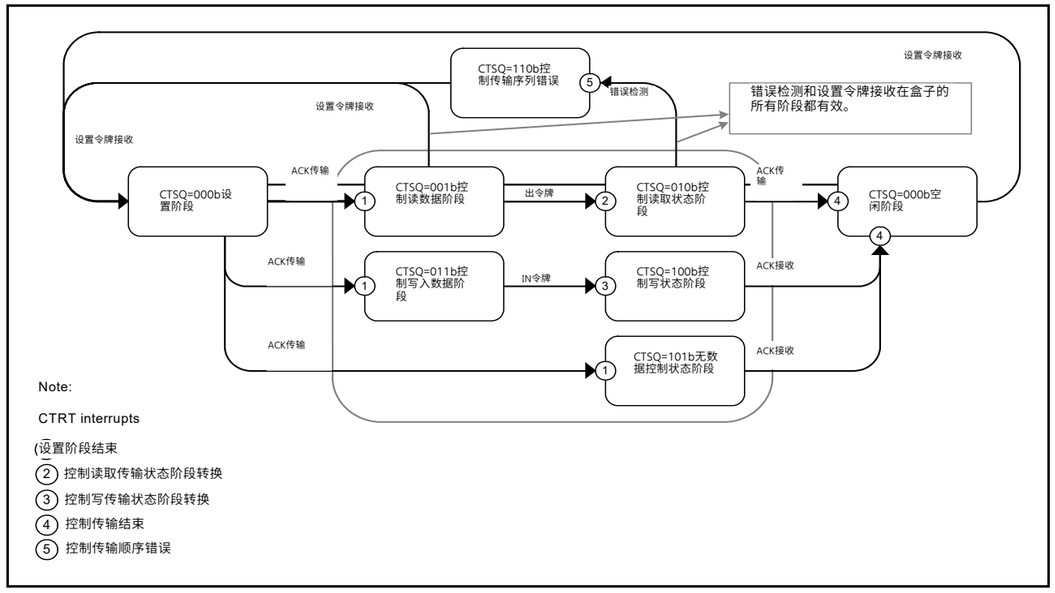


Figure 28.12 控制转移阶段转换

28.3.3.6 帧更新中断

在主机控制器模式下，更新帧号时会产生中断。

在设备控制器模式下，更新帧号时会产生SOFR中断。如果USBFS在全速运行期间检测到新的SOF数据包，则USBFS会更新帧号并生成SOFR中断。

28.3.3.7 VBUS interrupt

当USB_VBUS引脚电平改变时，会产生VBUS中断。USB_VBUS引脚的电平可以通过INTSTS0.VBSTS位检查。主控制器是连接还是断开可以使用VBUS中断来确认。如果系统在连接主机控制器的情况下激活，则不会产生第一个VBUS中断，因为USB_VBUS引脚电平没有变化。

28.3.3.8 Resume interrupt

In device controller mode, a resume interrupt is generated when the device state is the Suspend state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the Suspend state is detected by means of the resume interrupt.

In host controller mode, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

28.3.3.9 OVRCR interrupt

An OVRCR interrupt is generated when the USB_OVRCURA or USB_OVRCURB pin level has changed. The levels of the USB_OVRCURA and USB_OVRCURB pins can be checked in the SYSSTS0.OVCMON[1:0] bits. The external power supply IC can check whether overcurrent is detected using the OVRCR interrupt.

28.3.3.10 BCHG interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether a peripheral device is connected and can also be used to detect a remote wakeup in host controller mode. The BCHG interrupt is generated in both host and device controller modes.

28.3.3.11 DTCH interrupt

A DTCH interrupt is generated when a USB bus disconnect is detected in host controller mode. The USBFS detects bus disconnects in compliance with the USB 2.0 specification.

On interrupt detection, all pipes in which communications are carried out for the relevant port must be terminated by software. The pipes enter the wait state for a bus connection to the port, waiting for an ATTCH interrupt to occur. Regardless of the value set in the associated interrupt enable bit, the USBFS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt is detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state.

28.3.3.12 SACK interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet is received from the peripheral device in host controller mode. The SACK interrupt can be used to confirm that the setup transaction is successfully complete.

28.3.3.13 SIGN interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet has not been correctly received from the peripheral device three consecutive times in host controller mode. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

28.3.3.14 ATTCH interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 µs in host controller mode. To be more specific, an ATTCH interrupt is detected on any of the following conditions:

- When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 µs
- When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 µs.

28.3.3.15 EOFERR interrupt

An EOFERR interrupt occurs when the USBFS detects that communication is not complete at the EOF2 timing defined in the USB 2.0 specification.

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software, and the port must be re-enumerated. Regardless of the value set in the associated interrupt enable bit, the USBFS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt is detected to 0

28.3.3.8 恢复中断

在设备控制器模式下，当设备状态为Suspend状态且USB总线状态发生变化（从J-state到K-state，或从J-state到SE0）时，会产生恢复中断。通过恢复中断检测从挂起状态的恢复。

在主机控制器模式下，不会产生恢复中断。使用BCHG中断来检测USB总线状态的变化。

28.3.3.9 OVRCR interrupt

当USB_OVRCURA或USB_OVRCURB引脚电平发生变化时，会产生OVRCR中断。USB_OVRCURA和USB_OVRCURB引脚的电平可以在SYSSTS0.OVCMON[1:0]位中检查。外部电源IC可以使用OVRCR中断检查是否检测到过电流。

28.3.3.10 BCHG interrupt

当USB总线状态改变时会产生BCHG中断。BCHG中断可用于检测是否连接了外围设备，也可用于检测主机控制器模式下的远程唤醒。BCHG中断在主机和设备控制器模式下产生。

28.3.3.11 DTCH interrupt

当在主机控制器模式下检测到USB总线断开连接时，会产生DTCH中断。USBFS检测符合USB2.0规范的总线断开连接。

在检测到中断时，为相关端口执行通信的所有管道必须由软件终止。管道进入等待状态，等待总线连接到端口，等待ATTCH中断发生。无论相关中断使能位中设置的值如何，USBFS硬件：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态。

28.3.3.12 SACK中断

当在主机控制器模式下从外围设备接收到对发送的设置数据包的ACK响应时，将产生SACK中断。SACK中断可用于确认设置事务成功完成。

28.3.3.13 标志中断

如果在主机控制器模式下连续三次未从外围设备正确接收到已发送的设置数据包的ACK响应，则会产生SIGN中断。SIGN中断可用于检测没有从外围设备发送的ACK响应或ACK数据包的损坏。

28.3.3.14 ATTCH interrupt

在主机控制器模式下，当在USB端口上检测到全速信号电平的J状态或K状态持续2.5µs时，将产生ATTCH中断。更具体地说，在以下任何条件下都会检测到ATTCH中断：

- 当K-state、SE0或SE1变为J-state时，J-state持续2.5μs
- 当J-state、SE0或SE1变为K-state时，K-state持续2.5μs。

28.3.3.15 EOFERR interrupt

当USBFS检测到在USB2.0规范中定义的EOF2时序未完成通信时，将发生EOFERR中断。

在检测到中断时，所有为相关端口执行通信的管道必须由软件终止，并且必须重新枚举该端口。无论相关中断使能位中设置的值如何，USBFS硬件：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0

- Puts the port in which the EOFERR interrupt is generated into the idle state.

28.3.3.16 Portable device detection interrupt

A portable device detection interrupt is generated when the USBFS detects a level change (high to low or low to high) in the PDDET output from the USB-PHY. When a portable device detection interrupt is generated, use software to repeat the reading of the PDDETSTS0 bit until the same value is read three or more times to debounce the signal.

28.3.4 Pipe Control

Table 28.16 lists the pipe settings for the USBFS. USB data transfer is performed through logical pipes that software associates with endpoints. The USBFS has 10 pipes for data transfer. Set up the pipes based on your system specifications.

Table 28.16 Pipe settings

Register name	Bit name	Setting	Remarks
DCPCFG PIPECFG	TYPE	Transfer type	Pipes 1 to 9: Settable
	BFRE	BRDY interrupt mode	Pipes 1 to 5: Settable
	DBLB	Double buffer select	Pipes 1 to 5: Settable
	DIR	Transfer direction select	IN or OUT settable
	EPNUM	Endpoint number	Pipes 1 to 9: Settable A value other than 0000b must be set when the pipe is used.
	SHTNAK	Disabled state select for pipe when transfer ends	Pipes 1 and 2: Settable only for bulk transfers Pipes 3 to 5: Settable
DCPMAXP PIPEMAXP	DEVSEL	Device select	Referenced only in host controller mode
	MXPS	Maximum packet size	Compliant with the USB 2.0 specification
PIPEPERI	IFIS	Buffer flush	Pipes 1 and 2: Settable only for isochronous transfers Pipes 3 to 9: Setting disabled
	IITV	Interval counter	Pipes 1 and 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Settable only in host controller mode
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit
	INBUFM	IN buffer monitor	Available only for pipes 1 to 5
	SUREQ	Setup request	Settable only for the DCP and controlled in host controller mode
	SUREQCLR	SUREQ clear	Settable only for the DCP and controlled in host controller mode
	ATREPM	Auto response mode	Pipes 1 to 5: Settable only in device controller mode
	ACLRM	Auto buffer clear	Pipes 1 to 9: Settable
	SQCLR	Sequence clear	Clears the data toggle bit
	SQSET	Sequence set	Sets the data toggle bit
	SQMON	Sequence monitor	Monitors the data toggle bit
	PBUSY	Pipe busy status	-
	PID	Response PID	See section 28.3.4.6, Response PID
PIPEnTRE	TRENB	Transaction counter enable	Pipes 1 to 5: Settable
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Settable
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Settable

28.3.4.1 Pipe control register switching procedures

The following bits in the pipe control registers can be changed only when USB communication is prohibited (PID = NAK).

Do not change the following registers and bits when USB communication is enabled (PID = BUF):

- 将产生EOFERR中断的端口置于空闲状态。

28.3.3.16 便携式设备检测中断

当USBFS在USB-PHY的PDDET输出中检测到电平变化（从高到低或从低到高）时，会产生便携式设备检测中断。当产生便携式设备检测中断时，使用软件重复读取PDDETSTS0位，直到读取相同的值3次或更多次，以对信号进行去抖。

28.3.4 管道控制

表28.16列出了USBFS的管道设置。USB数据传输是通过软件与端点关联的逻辑管道执行的。USBFS有10个用于数据传输的管道。根据您的系统规格设置管道。

Table 28.16 管道设置

注册名称	位名称	Setting	Remarks
DCPCFG PIPECFG	TYPE	传输类型	管道1至9：可设置
	BFRE	BRDY中断模式	管道1至5：可设置
	DBLB	双缓冲选择	管道1至5：可设置
	DIR	传输方向选择	输入或输出可设置
	EPNUM	端点编号	管道1至9：可设置 使用管道时，必须设置0000b以外的值。
	SHTNAK	传输结束时管道的禁用状态选择	管道1和2：仅可设置用于批量传输 管道3至5：可设置
DCPMAXP PIPEMAXP	DEVSEL	设备选择	仅在主机控制器模式下引用
	MXPS	最大数据包大小	符合USB2.0规范
PIPEPERI	IFIS	缓冲区刷新	管道1和2：仅可设置用于同步传输 管道3到9：设置禁用
	IITV	间隔计数器	管道1和2：仅可设置用于同步传输 管道3到5：禁用设置 管道6到9：仅在主机控制器模式下可设置
DCPCTR PIPEnCTR	BSTS	缓冲状态	对于DCP，接收缓冲区状态和发送缓冲区状态通过ISEL位切换
	INBUFM	IN缓冲监视器	仅适用于管道1至5
	SUREQ	设置请求	只能为DCP设置并在主机控制器模式下控制
	SUREQCLR	SUREQ clear	只能为DCP设置并在主机控制器模式下控制
	ATREPM	自动响应模式	管道1到5：仅在设备控制器模式下可设置
	ACLRM	自动缓冲区清除	管道1至9：可设置
	SQCLR	序列清晰	清除数据切换位
	SQSET	序列集	设置数据切换位
	SQMON	序列监视器	监控数据切换位
	PBUSY	管道繁忙状态	-
	PID	响应PID	请参阅第28.3.4.6节，响应PID
PIPEnTRE	TRENB	事务计数器启用	管道1至5：可设置
	TRCLR	当前交易柜台清零	管道1至5：可设置
PIPEnTRN	TRNCNT	交易柜台	管道1至5：可设置

28.3.4.1 管道控制寄存器切换程序

只有当USB通信被禁止（PID=
NAK).

当启用USB通信(PID=BUF)时，请勿更改以下寄存器和位：

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN.

To set these bits when USB communication is enabled (PID = BUF):

1. A request to change the bits in the pipe control register occurs.
2. Set the PID[1:0] bits associated with the pipe to NAK.
3. Wait until the associated PBUSY bit is set to 0.
4. Set the bits in the pipe control register.

The following bits in the pipe control registers can be changed only when the selected pipe information has not been set in the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Do not set the following registers when the CURPIPE[3:0] bits are set:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEMAXP and PIPEPERI.

To change pipe information, you must set the CURPIPE[3:0] bits in the port select registers to a pipe other than the one to be changed. For the DCP, the buffer must be cleared using the BCLR bit in the Port Control Register after the pipe information is changed.

28.3.4.2 Transfer types

The PIPECFG.TYPE[1:0] bits specify the following transfer types for each pipe:

- DCP: No setting is required (fixed at control transfer)
- Pipes 1 and 2: Set to bulk or isochronous transfer
- Pipes 3 to 5: Set to bulk transfer
- Pipes 6 to 9: Set to interrupt transfer.

28.3.4.3 Endpoint number

The PIPECFG.EPNUM[3:0] bits set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to 15.

- DCP: No setting is required (fixed at endpoint 0)
- Pipes 1 to 9: Select and set the endpoint numbers from 1 to 15 so that the combination of the PIPECFG.DIR and EPNUM[3:0] bits is unique.

28.3.4.4 Maximum packet size setting

The DCPMAXP.MXPS[6:0] and PIPEMAXP.MXPS[8:0] bits specify the maximum packet size for each pipe. The DCP and pipes 1 to 5 can be set to any of the maximum pipe sizes defined in the USB 2.0 specification. For pipes 6 to 9, the maximum packet size is 64 bytes. Set the maximum packet size as follows before starting a transfer (PID = BUF):

- DCP: Set to 8, 16, 32, or 64
- Pipes 1 to 5: Set to 8, 16, 32, or 64 for bulk transfers
- Pipes 1 and 2: Set between 1 and 256 for isochronous transfers
- Pipes 6 to 9: Set to a value between 1 and 64.

28.3.4.5 Transaction counter for pipes 1 to 5 in the receiving direction

When the specified number of transactions is complete in the data packet receiving direction, the USBFS recognizes that

- DCPCFG和DCPMAXP中的位
- DCPCTR中的SQCLR和SQSET位
- PIPECFG、PIPEMAXP和PIPEPERI中的位
- PIPEnCTR中的ATREPM、ACLRM、SQCLR和SQSET位
- PIPEnTRE和PIPEnTRN中的位。

要在启用USB通信(PID=BUF)时设置这些位：

1. 发生更改管道控制寄存器中的位的请求。
2. 将与管道关联的PID[1:0]位设置为NAK。
3. 等到相关的PBUSY位设置为0。
4. 设置管道控制寄存器中的位。

只有在CFIFOSEL、D0FIFOSEL和D1FIFOSEL的CURPIPE[3:0]位中未设置所选管道信息时，才能更改管道控制寄存器中的以下位。

设置CURPIPE[3:0]位时不要设置以下寄存器：

- DCPCFG和DCPMAXP中的位
- PIPECFG、PIPEMAXP和PIPEPERI中的位。

要更改管道信息，您必须将端口选择寄存器中的CURPIPE[3:0]位设置为要更改的管道以外的管道。对于DCP，必须在管道信息更改后使用端口控制寄存器中的BCLR位清除缓冲区。

28.3.4.2 传输类型

PIPECFG.TYPE[1:0]位为每个管道指定以下传输类型：

- DCP：无需设置（控制转移时固定）
- 管道1和2：设置为批量传输或同步传输
- 管道3到5：设置为批量传输
- 管道6到9：设置为中断传输。

28.3.4.3 端点编号

PIPECFG.EPNUM[3:0]位设置每个管道的端点号。DCP固定在端点0。其他管道可以设置从端点1到15。

- DCP：无需设置（固定在端点0）
- 管道1到9：选择并设置从1到15的端点编号，以便PIPECFG.DIR和EPNUM[3:0]位是唯一的。

28.3.4.4 最大数据包大小设置

DCPMAXP.MXPS[6:0]和PIPEMAXP.MXPS[8:0]位指定每个管道的最大数据包大小。DCP和管道1到5可以设置为USB2.0规范中定义的任何最大管道尺寸。对于管道6到9，最大数据包大小为64字节。在开始传输之前设置最大数据包大小如下（PID=BUF）：

- DCP：设置为8、16、32或64
- 管道1到5：设置为8、16、32或64以进行批量传输
- 管道1和2：设置在1和256之间，用于同步传输
- 管道6到9：设置为1到64之间的值。

28.3.4.5 接收方向上管道1到5的事务计数器

当在数据包接收方向完成指定数量的事务时，USBFS识别

the transfer ended. Two transaction counters are provided:

- The PIPEnTRN register that specifies the number of transactions to be executed
- The current counter that internally counts the number of executed transactions.

If the PIPECFG.SHTNAK bit is set to 1, when the current counter value matches the specified number of transactions, the associated PIPEnCTR.PID[1:0] bits are set to NAK and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The data read from PIPEnTRN differs depending on the PIPEnTRE.TRENB setting as follows:

- The TRENB bit = 0: Specified transaction counter value can be read
- The TRENB bit = 1: Current counter value indicating the internally counted number of executed transactions can be read.

The following constraints apply when working with the TRCLR bit:

- If the transactions are counted and PID = BUF, the current counter cannot be cleared
- If there is any data left in the buffer, the current counter cannot be cleared.

28.3.4.6 Response PID

The PID[1:0] bits in DCPCTR and PIPEnCTR set the response PID for each pipe. This section describes the USBFS operation with different response PID settings.

(1) Software response PID settings in host controller mode

Select the response PID to specify the execution of transactions as follows:

- NAK setting: Using pipes is disabled and no transactions are executed
- BUF setting: Transactions are executed based on the FIFO buffer state:
  - OUT direction: An OUT token is issued if the FIFO buffer contains transmit data.
  - IN direction: An IN token is issued if the FIFO buffer is not full and can receive data.
- STALL setting: Using pipes is disabled and no transactions are executed.

Note: Use the DCPCTR.SUREQ bit to execute setup transactions for the DCP.

(2) Software response PID settings in device controller mode

Select the response PID to respond to transactions from the host as follows:

- NAK setting: A NAK response is returned to all generated transactions
- BUF setting: A response is returned to transactions based on the FIFO buffer
- STALL setting: A STALL response is returned to all generated transactions.

Note: For setup transactions, an ACK response is always returned, regardless of the PID[1:0] setting, and the USB request is stored in the register.

Sections (3) and (4) describe situations in which the USBFS writes to the PID[1:0] bits because of specific transaction results.

(3) Hardware response PID settings in host controller mode

- NAK setting: PID = NAK is set in the following cases, and issuing of tokens is automatically stopped:
  - When a non-isochronous transfer is performed and an NRDY interrupt is generated (For details, see section 28.3.3.2, NRDY interrupt.)
  - If a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
  - If transaction counting ends when the SHTNAK bit is set to 1 for bulk transfers.
- BUF setting: The USBFS does not write this setting.

转移结束。提供了两个交易柜台：

- PIPEnTRN寄存器，指定要执行的事务数
- 内部计算已执行事务数的当前计数器。

如果PIPECFG.SHTNAK位设置为1，则当当前计数器值与指定的事务数匹配时，相关的PIPEnCTR.PID[1:0]位将设置为NAK，并禁用后续传输。通过PIPEnTRE.TRCLR位初始化事务计数器功能的当前计数器，事务可以从头开始重新计数。从PIPEnTRN读取的数据因PIPEnTRE.TRENB设置而异，如下所示：

- TRENB位=0：可以读取指定的事务计数器值
- TRENB位=1：可以读取表示内部计数的已执行事务数的当前计数器值。

使用TRCLR位时适用以下约束：

- 如果事务被计数并且PID=BUF，则当前计数器不能被清除
- 如果缓冲区中还有任何数据，则无法清除当前计数器。

28.3.4.6 响应PID

DCPCTR和PIPEnCTR中的PID[1:0]位设置每个管道的响应PID。本节介绍具有不同响应PID设置的USBFS操作。

(1) 主机控制器模式下的软件响应PID设置

选择响应PID来指定事务的执行，如下所示：

- NAK设置：禁用使用管道并且不执行任何事务
- BUF设置：根据FIFO缓冲区状态执行事务：
  - OUT方向：如果FIFO缓冲区包含发送数据，则发出OUT令牌。
  - IN方向：如果FIFO缓冲区未满并且可以接收数据，则发出IN令牌。
- STALL设置：禁用使用管道并且不执行任何事务。

Note: 使用DCPCTR.SUREQ位执行DCP的设置事务。

(2) 设备控制器模式下的软件响应PID设置

选择响应PID以响应来自主机的事务，如下所示：

- NAK设置：向所有生成的事务返回NAK响应
- BUF设置：根据FIFO缓冲区向事务返回响应
- STALL设置：向所有生成的事务返回一个STALL响应。

Note: 对于设置事务，无论PID[1:0]设置如何，总是返回一个ACK 响应，并且USB请求存储在寄存器中。

第(3)和(4)节描述了USBFS由于特定事务结果而写入PID[1:0]位的情况。

(3) 主机控制器模式下的硬件响应PID设置

- NAK设置：PID=NAK在以下情况下设置，并且自动停止发行令牌：
  - 当执行非同步传输并产生NRDY中断时（详情请参阅第28.3.3.2节，NRDY中断。）
  - 如果在PIPECFG.SHTNAK位设置为1以进行批量传输时接收到短数据包
  - 如果在SHTNAK位设置为1以进行批量传输时事务计数结束。
- BUF设置：USBFS不写入此设置。

- STALL setting: PID = STALL is set in the following cases, and issuing of tokens is automatically stopped:
  - When STALL is received in response to a transmitted token
  - When a received data packet exceeds the maximum packet size.

(4) Hardware response PID settings in device controller mode

- NAK setting: PID = NAK is set in the following cases, and a NAK response is returned to transactions:
  - When the setup token is received normally (DCP only)
  - If transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers.
- BUF setting: There is no BUF writing by the USBFS
- STALL setting: PID = STALL is set in the following cases, and a STALL response is returned to transactions:
  - When a received data packet exceeds the maximum packet size
  - When a control transfer sequence error is detected (DCP only).

28.3.4.7 Data PID sequence bit

The USBFS automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit toggles on ACK handshake reception. When data is received, the sequence bit toggles on ACK handshake transmission. The SQCLR and SQSET bits in DCPCTR and PIPEnCTR registers can be used to change the data PID sequence bit.

In device controller mode when control transfers are used, the USBFS automatically sets the sequence bit for stage transitions. DATA1 is returned when the setup stage ends. The sequence bit is not referenced and PID = DATA1 is returned in the status stage. Therefore, no software settings are required. However, in host controller mode when control transfers are used, the sequence bit must be set by software for the stage transitions.

For ClearFeature requests for transmission or reception, the data PID sequence bit must be set by software in both host and device controller modes.

28.3.4.8 Response PID = NAK function

The USBFS provides a function for disabling pipe operation (PID response = NAK) when the final data packet of a transaction is received. The USBFS automatically distinguishes this based on reception of a short packet or the transaction counter. Enable this function by setting the PIPECFG.SHTNAK bit to 1.

When the double buffer mode is used for the FIFO buffer, this function enables reception of data packets in transfer units. If pipe operation is disabled, software must enable the pipe again (PID response = BUF).

The response PID = NAK function can only be used for bulk transfers.

28.3.4.9 Auto response mode

For bulk transfer pipes (1 to 5), when the PIPEnCTR.ATREPM bit is set to 1, a transition is made in auto response mode. During an OUT transfer (PIPECFG.DIR = 0), OUT-NAK mode is invoked, and during an IN transfer (DIR = 1), null auto response mode is invoked.

28.3.4.10 OUT-NAK mode

For bulk OUT transfer pipes, NAK is returned in response to an OUT token, and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To transition from normal mode to OUT-NAK mode, specify OUT-NAK mode while pipe operation is disabled (PID[1:0] = 00b for NAK response). Next, enable pipe operation (PID[1:0] = 01b for BUF response), on which OUT-NAK mode becomes valid. If an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is returned to the host.

To transition from OUT-NAK mode to normal mode, cancel OUT-NAK mode while pipe operation is disabled (NAK). Next enable pipe operation (BUF). In normal mode, reception of OUT data is enabled.

- STALL设置：PID=STALL在以下情况下设置，并且自动停止发行令牌：
  - 当接收到STALL以响应传输的令牌时
  - 当接收到的数据包超过最大包大小时。

(4) 设备控制器模式下的硬件响应PID设置

- NAK设置：PID=NAK在以下情况下设置，并向事务返回NAK响应：
  - 正常接收设置令牌时（仅DCP）
  - 如果在PIPECFG.SHTNAK位设置为1以进行批量传输时，事务计数结束或收到短数据包。
- BUF设置：USBFS没有写入BUF
- STALL设置：PID=STALL在以下情况下设置，并向事务返回STALL响应：
  - 当接收到的数据包超过最大包大小时
  - 当检测到控制传输序列错误时（仅限DCP）。

28.3.4.7 数据PID序列位

当数据在控制传输数据阶段、批量传输和中断传输成功传输时，USBFS会自动切换数据PID中的序列位。下一个要发送的数据PID的序列位可以通过DCPCTR和PIPEnCTR中的SQMON位来确认。发送数据时，序列位在ACK握手接收时切换。当接收到数据时，序列位在ACK握手传输上切换。DCPCTR和PIPEnCTR寄存器中的SQCLR和SQSET位可用于更改数据PID序列位。

在使用控制传输的设备控制器模式下，USBFS自动设置阶段转换的序列位。DATA1在设置阶段结束时返回。不引用序列位，在状态阶段返回PID=DATA1。因此，不需要任何软件设置。但是，在使用控制传输的主机控制器模式下，必须由软件设置序列位以进行阶段转换。

对于发送或接收的ClearFeature请求，数据PID序列位必须由软件在主机和设备控制器模式下设置。

28.3.4.8 响应PID=NAK功能

USBFS提供了在接收到事务的最终数据包时禁用管道操作（PID响应=NAK）的功能。USBFS根据收到的短数据包或事务计数器自动区分这一点。通过将PIPECFG.SHTNAK位设置为1来启用此功能。

当FIFO缓冲区使用双缓冲区模式时，此功能可以接收以传输为单位的数据包。
如果管道操作被禁用，软件必须再次启用管道（PID响应=BUF）。

响应PID=NAK函数只能用于批量传输。

28.3.4.9 自动响应模式

对于批量传输管道（1到5），当PIPEnCTR.ATREPM位设置为1时，将在自动响应模式下进行转换。在OUT传输期间(PIPECFG.DIR=0)，将调用OUT-NAK模式，在IN传输期间(DIR=1)，将调用空自动响应模式。

28.3.4.10 OUT-NAK mode

对于批量OUT传输管道，NAK响应OUT令牌返回，并且当PIPEnCTR.ATREPM位设置为1时输出NRDY中断。要从正常模式转换到OUT-NAK模式，请指定OUT-NAK模式，同时管道操作被禁用（PID[1:0]=00b用于NAK响应）。接下来，启用管道操作（PID[1:0]=01b用于BUF响应），此时OUT-NAK模式变为有效。如果在禁用管道操作之前立即收到OUT令牌，则正常接收令牌数据，并向主机返回ACK。

要从OUT-NAK模式转换到正常模式，请在禁用管道操作(NAK)时取消OUT-NAK模式。
接下来启用管道操作(BUF)。在正常模式下，可以接收OUT数据。

28.3.4.11 Null auto response mode

For bulk IN transfer pipes, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To transition from normal mode to null auto response mode, specify null auto response mode while pipe operation is disabled (response PID = NAK). Next enable pipe operation (response PID = BUF) on which null auto response mode becomes valid. Before setting null auto response mode, check that PIPEnCTR.INBUFM = 0, because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, empty the buffer using the PIPEnCTR.ACLRM bit. Do not write data from the FIFO port while a transition to null auto response mode is being made.

To transition from null auto response mode to normal mode, keep pipe operation disabled (response PID = NAK) for the period of the zero-length packet transmission (about 10 µs) before canceling the null auto response mode. In normal mode, data can be written to the FIFO port so packet transmission to the host is enabled by enabling pipe operation (response PID = BUF).

28.3.5 FIFO Buffer Memory

The USBFS provides a FIFO buffer for data transfers, and it manages the memory area used for each pipe. The FIFO buffer has two states depending on whether the access right is assigned to the system (CPU side) or the USBFS (SIE side).

(1) Buffer status

Table 28.17 and Table 28.18 show the buffer status in the USBFS. The FIFO buffer status can be confirmed using the DCPCTR.BSTS and PIPEnCTR.INBUFM bits. The transfer direction for the FIFO buffer can be specified in either the PIPECFG.DIR or CFIFOSEL.ISEL bit (when DCP is selected). The INBUFM bit is valid for pipes 0 to 5 in the transmitting direction.

When a transmitting pipe uses double buffering, software can read the BSTS bit to monitor the FIFO buffer status on the CPU side and the INBUFM bit to monitor the FIFO buffer status on the SIE side. When the BEMP interrupt does not show the buffer empty status because write access to the FIFO port by the CPU or DMA/DTC is slow, software can use the INBUFM bit to confirm the end of transmission.

Table 28.17 Buffer status indicated by BSTS bit

ISEL or DIR	BSTS	Buffer memory status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet is received. Reading from the FIFO port is allowed. Note: When a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	The transmission is not complete. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	The transmission is complete. CPU write is allowed.

Table 28.18 Buffer status indicated by INBUFM bit

DIR	INBUFM	Buffer memory status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	The transmission is complete. There is no waiting data to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

28.3.6 FIFO Buffer Clearing

Table 28.19 shows the methods for clearing the FIFO buffer. The FIFO buffer can be cleared using BCLR in the port control register, DnFIFOSEL.DCLRM, or the PIPEnCTR.ACLRM bit.

Single or double buffering can be selected for pipes 1 to 5 in the PIPECFG.DBLB bit.

28.3.4.11 空自动响应模式

对于批量IN传输管道，当PIPEnCTR.ATREPM位设置为1时，将连续传输零长度数据包。

要从正常模式转换为空自动响应模式，请在禁用管道操作时指定空自动响应模式（响应PID=NAK）。接下来启用空自动响应模式有效的管道操作（响应PID=BUF）。在设置空自动响应模式之前，请检查PIPEnCTR.INBUFM=0，因为只有在缓冲区为空时才能设置模式。如果INBUFM位为1，则使用PIPEnCTR.ACLRM位清空缓冲区。在转换到空自动响应模式时，不要从FIFO端口写入数据。

要从空值自动响应模式转换到正常模式，在取消空值自动响应模式之前，在零长度数据包传输期间（约10µs）保持管道操作禁用（响应PID=NAK）。在正常模式下，数据可以写入FIFO端口，因此通过启用管道操作（响应PID=BUF）启用到主机的数据包传输。

28.3.5 先进先出缓冲存储器

USBFS为数据传输提供FIFO缓冲区，并管理用于每个管道的内存区域。根据访问权限是分配给系统（CPU端）还是USBFS（SIE端），FIFO缓冲区有两种状态。

(1) 缓冲状态

表28.17和表28.18显示了USBFS中的缓冲区状态。FIFO缓冲区状态可以使用确认DCPCTR.BSTS和PIPEnCTR.INBUFM位。FIFO缓冲区的传输方向可以在任一pipecfg.dir或cfifosel.isel位（选择DCP时）。INBUFM位对传输方向的管道0到5有效。

当传输管道使用双缓冲时，软件可以读取BSTS位来监控CPU侧的FIFO缓冲区状态，以及读取INBUFM位来监控SIE侧的FIFO缓冲区状态。当BEMP中断由于CPU或DMADTC对FIFO端口的写访问速度慢而没有显示缓冲区空状态时，软件可以使用INBUFM位来确认传输结束。

Table 28.17 由BSTS位指示的缓冲区状态

ISEL或DIR	BSTS	缓冲存储器状态
0 (receiving direction)	0	没有接收到数据，或正在接收数据。禁止从FIFO端口读取。
0 (receiving direction)	1	有接收数据，或接收到零长度数据包。允许从FIFO端口读取。笔记： 当接收到零长度数据包时，无法读取，必须清除缓冲区。
1 (transmitting direction)	0	传输不完整。禁止写入FIFO端口。
1 (transmitting direction)	1	传输完成。允许CPU写入。

Table 28.18 INBUFM位指示的缓冲区状态

DIR	INBUFM	缓冲存储器状态
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	传输完成。没有等待传输的数据。
1 (transmitting direction)	1	FIFO端口已将数据写入缓冲区。有数据要传输。

28.3.6 FIFO缓冲区清除

表28.19显示了清除FIFO缓冲区的方法。可以使用端口控制寄存器中的BCLR、DnFIFOSEL.DCLRM或PIPEnCTR.ACLRM位清除FIFO缓冲区。

可以在PIPECFG.DBLB位中为管道1到5选择单缓冲或双缓冲。

Table 28.19 Buffer clearing methods

FIFO buffer clearing mode	Clearing FIFO buffer on the CPU side	Mode for automatically clearing the FIFO buffer after reading the specified pipe data	Auto buffer clear mode for discarding all received packets
Register used	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Bit used	BCLR	DCLRM	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid.	1: Mode valid 0: Mode invalid.

(1) Auto buffer clear mode function

The USBFS discards all received data packets if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet is received, the ACK response is returned to the host controller. The auto buffer clear mode function can only be set in the FIFO buffer reading direction.

Setting the ACLRM bit to 1 and then to 0 clears the FIFO buffer of the selected pipe regardless of the access direction. An access cycle of at least 100 ns is required for the internal hardware sequence processing between ACLRM = 1 and ACLRM = 0.

28.3.7 FIFO Port Functions

Table 28.20 shows the settings for the FIFO port functions. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, set the BVAL flag in the port control register to end writing. To send a zero-length packet, use the BCLR bit to clear the buffer, and then set the BVAL flag to end writing.

In reading, reception of new packets is automatically enabled when all data is read. Data cannot be read when a zero-length packet is received (DTLN[8:0] = 0), so use the BCLR bit to clear the buffer. The length of the received data can be confirmed in the DTLN[8:0] bits in the port control register.

Table 28.20 FIFO port function settings

Register name	Bit name	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	Selects DTLN[8:0] read mode
	REW	FIFO buffer rewind (re-read, rewrite)
	DCLRM	Automatically clears receive data for a specified pipe after the data is read (only for DnFIFO)
	DREQE	Enables DMA/DTC transfers (only for DnFIFO)
	MBW	FIFO port access bit width
	BIGEND	Selects FIFO port endian
	ISEL	FIFO port access direction (only for DCP)
	CURPIPE	Selects the current pipe
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	Ends writing to the FIFO memory
	BCLR	Clears the FIFO buffer on the CPU
	DTLN	Checks the length of received data

(1) FIFO port selection

Table 28.21 shows the pipes that can be selected with the different FIFO ports. The pipe to be accessed must be selected with the CURPIPE[3:0] bits in the port select register. After the pipe is selected, software must check whether the written value can be read correctly from the CURPIPE[3:0] bits. If the previous pipe number is read, it indicates that the USBFS is modifying the pipe. Next, software checks that the FRDY bit in the Port Control Register is 1.

In addition, software must specify the bus width to be accessed with the MBW bit in the port select register. The FIFO buffer access direction conforms to the PIPECFG.DIR setting. Only in the DCP that the ISEL bit in the port select register determines the direction.

Table 28.19 缓冲区清除方法

FIFO缓冲区清除模式	清除FIFO缓冲区CPU端	读取指定管道数据后自动清除FIFO缓冲区的模式	自动缓冲区清除模式，用于丢弃所有接收到的数据包
注册使用	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
使用的位	BCLR	DCLRM	ACLRM
清算条件	通过写1清除	1：模式有效0 ：模式无效。	1：模式有效0 ：模式无效。

(1) 自动缓冲清除模式功能

如果PIPEnCTR.ACLRM位设置为1，USBFS将丢弃所有接收到的数据包。如果接收到正确的数据包，则向主机控制器返回ACK响应。自动缓冲区清除模式功能只能在FIFO缓冲区读取方向设置。

无论访问方向如何，将ACLRM位设置为1，然后设置为0都会清除所选管道的FIFO缓冲区。ACLRM=1和之间的内部硬件序列处理需要至少100ns的访问周期
ACLRM = 0.

28.3.7 FIFO端口功能

表28.20显示了FIFO端口功能的设置。在写访问中，在达到最大数据包大小之前写入数据会自动启用数据传输。要在达到最大数据包大小之前启用传输，请设置端口控制寄存器中的BVAL标志以结束写入。要发送零长度数据包，请使用BCLR位清除缓冲区，然后设置BVAL标志以结束写入。

在读取中，当所有数据被读取时，自动启用新数据包的接收。接收到零长度数据包时（DTLN[8:0]=0）无法读取数据，因此使用BCLR位清除缓冲区。接收数据的长度可以在端口控制寄存器的DTLN[8:0]位中确认。

Table 28.20 FIFO端口功能设置

注册名称	位名称	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	选择DTLN[8:0]读取模式
	REW	FIFO缓冲区倒带（重新读取、重写）
	DCLRM	读取数据后自动清除指定管道的接收数据（仅适用于DnFIFO）
	DREQE	启用DMADTC传输（仅适用于DnFIFO）
	MBW	FIFO端口访问位宽
	BIGEND	选择FIFO端口字节序
	ISEL	FIFO端口访问方向（仅适用于DCP）
	CURPIPE	选择当前管道
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	结束对FIFO存储器的写入
	BCLR	清除CPU上的FIFO缓冲区
	DTLN	检查接收数据的长度

(1) 先进先出端口选择

表28.21显示了可以使用不同FIFO端口选择的管道。必须使用端口选择寄存器中的CURPIPE[3:0]位来选择要访问的管道。选择管道后，软件必须检查是否可以从CURPIPE[3:0]位正确读取写入的值。如果读取到之前的管道号，说明USBFS正在修改管道。接下来，软件检查端口控制寄存器中的FRDY位是否为1。

此外，软件必须通过端口选择寄存器中的MBW位指定要访问的总线宽度。FIFO缓冲区访问方向符合PIPECFG.DIR设置。只有在DCP中，端口选择寄存器中的ISEL位才决定方向。

Table 28.21 FIFO port access by pipe

Pipe	Access method	Port that can be used
DCP	CPU access	CFIFO port register
Pipe 1 to Pipe 9	CPU access	• CFIFO port register • D0FIFO/D1FIFO port register
	DMA/DTC access	D0FIFO/D1FIFO port register

(2) REW bit

It is possible to temporarily stop access to the pipe currently being accessed, access a different pipe, and then continue processing the first pipe again. Use the REW bit in the port select register for this processing.

If a pipe is selected in the CURPIPE[3:0] bits in the port select register with the REW bit set to 1, the pointer used for reading from and writing to the FIFO buffer is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with 0 set for the REW bit, data can be read and written in continuation from the previous selection, without the pointer being reset. To access the FIFO port, software must check that the FRDY bit in the port control register is 1 after selecting a pipe.

28.3.8 DMA Transfers (D0FIFO and D1FIFO Ports)

(1) Overview of DMA transfers

For pipes 1 to 9, the FIFO port can be accessed using the DMAC. When buffer access for a pipe targeted for DMA transfer is enabled, a DMA transfer request is issued.

Select the unit of transfer to the FIFO port in the DnFIFOSEL.MBW bit, and select the pipe targeted for the DMA transfer in the DnFIFOSEL.CURPIPE[3:0] bits. Do not change the selected pipe during the DMA transfer.

(2) DnFIFO auto clear mode (D0FIFO and D1FIFO port reading direction)

If 1 is set in the DnFIFOSEL.DCLRM bit, the USBFS automatically clears the FIFO buffer of the selected pipe when reading of data from the FIFO buffer is complete.

Table 28.22 shows the packet reception and FIFO buffer clearing processing by software for each of the settings. As shown in the table, the buffer clearing conditions depend on the value set in the PIPECFG.BFRE bit. Using the DnFIFOSEL.DCLRM bit eliminates the need for the buffer to be cleared by software in any situation that requires buffer clearing. This enables DMA transfers without involving software.

The DnFIFO auto clear mode can only be set in the FIFO buffer reading direction.

Table 28.22 Packet reception and FIFO buffer clearing processing by software

Buffer status when packet is received	Register setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	No clearing required	No clearing required	No clearing required	No clearing required
Zero-length packet reception	Clearing required	Clearing required	No clearing required	No clearing required
Normal short packet reception	No clearing required	Clearing required	No clearing required	No clearing required
Transaction count end	No clearing required	Clearing required	No clearing required	No clearing required

28.3.9 Control Transfers Using DCP

In the data stage of control transfers, data is transferred using the Default Control Pipe (DCP). The DCP FIFO buffer is a 64-byte single buffer with a fixed area for both control reads and control writes. The FIFO buffer can only be accessed through the CFIFO port.

Table 28.21 通过管道访问FIFO端口

Pipe	访问方法	可以使用的端口
DCP	CPU访问	CFIFO端口寄存器
管道1到管道9	CPU访问	CFIFO端口寄存器 D0FIFOD1FIFO端口寄存器
	DMA/DTC access	D0FIFOD1FIFO端口寄存器

(2) REW位

可以暂时停止对当前正在访问的管道的访问，访问不同的管道，然后再次继续处理第一个管道。使用端口选择寄存器中的REW位进行此处理。

如果在端口选择寄存器的CURPIPE[3:0]位中选择了一个管道，并且REW位设置为1，则用于读取和写入FIFO缓冲区的指针复位，可以进行读取或写入从第一个字节开始。如果在REW位设置为0的情况下选择管道，则可以从先前的选择继续读取和写入数据，而无需重置指针。要访问FIFO端口，软件必须在选择管道后检查端口控制寄存器中的FRDY位是否为1。

28.3.8 DMA传输（D0FIFO和D1FIFO端口）

(1) DMA传输概述

对于管道1到9，可以使用DMAC访问FIFO端口。当启用以DMA传输为目标的管道的缓冲区访问时，将发出DMA传输请求。

在DnFIFOSEL.MBW位中选择传输到FIFO端口的单位，并在DnFIFOSEL.CURPIPE[3:0]位中选择DMA传输的目标管道。在DMA传输期间不要更改选定的管道。

(2) DnFIFO自动清除模式（D0FIFO和D1FIFO端口读取方向）

如果DnFIFOSEL.DCLRM位设置为1，USBFS会在从FIFO缓冲区读取数据完成时自动清除所选管道的FIFO缓冲区。

表28.22显示了软件对每个设置的数据包接收和FIFO缓冲区清除处理。如表所示，缓冲区清除条件取决于PIPECFG.BFRE位中设置的值。使用DnFIFOSEL.DCLRM位无需在任何需要清除缓冲区的情况下通过软件清除缓冲区。这可以在不涉及软件的情况下实现DMA传输。

DnFIFO自动清除模式只能设置在FIFO缓冲区读取方向。

Table 28.22 通过软件进行数据包接收和FIFO缓冲区清除处理

收到数据包时的缓冲区状态	注册设置			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
缓冲区已满	无需清算	无需清算	无需清算	无需清算
零长度数据包接收	需要清算	需要清算	无需清算	无需清算
正常短包接收	无需清算	需要清算	无需清算	无需清算
交易计数结束	无需清算	需要清算	无需清算	无需清算

28.3.9 使用DCP进行控制传输

在控制传输的数据阶段，使用默认控制管道(DCP)传输数据。DCPFIFO缓冲区是一个64字节的单缓冲区，具有用于控制读取和控制写入的固定区域。FIFO缓冲区只能通过CFIFO端口访问。

28.3.9.1 Control transfers in host controller mode

(1) Setup stage

The USQREQ, USBVAL, USBINDX, and USBLENG registers are used to transmit USB requests for setup transactions. Writing the setup packet data to the registers and then writing 1 to the DCPCTR.SUREQ bit transmits the specified data for the setup transaction. On completion of the transaction, the SUREQ bit is set to 0. Do not change these USB request registers while SUREQ = 1.

When an attached function device is detected, software must issue the first setup transaction for the device using this sequence with the DCPMAXP.DEVSEL[3:0] bits set to 0 and the DEVADD0.USBSPD[1:0] bits set appropriately.

When an attached function device is shifted to the Address state, software must issue setup transactions using this sequence with the assigned USB address set in the DEVSEL[3:0] bits and the bits in DEVADDn associated with the specified USB address set appropriately. For example, when PIPEMAXP.DEVSEL[3:0] = 0010b, make appropriate settings in DEVADD2. When PIPEMAXP.DEVSEL[3:0] = 0101b, make appropriate settings in DEVADD5.

When the setup transaction data is sent, an interrupt request is generated based on the response from the peripheral device (SIGN or SACK bit in INTSTS1). This interrupt request allows software to check the setup transaction result.

A DATA0 data packet (USB request) for the setup transaction is always transmitted regardless of the status of the DCPCTR.SQMON bit.

(2) Data stage

The data stage is used to transfer data using the DCP FIFO buffer.

Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit. Specify the transfer direction in the DCPCFG.DIR bit.

For the first data packet of the data stage, the data PID must be transferred as DATA1. Set data PID = DATA1 in the DCPCTR.SQSET bit and set the PID bits = BUF. Completion of data transfer is detected using the BRDY or BEMP interrupt.

For control write transfers, when the number of data bytes to be sent is an integer multiple of the maximum packet size, software must send a zero-length packet at the end.

(3) Status stage

The status stage is used for zero-length packet data transfers in the reverse direction of the data stage. As in the data stage, data is transfered using the DCP FIFO buffer. Transactions are executed using the same procedure as the data stage.

Data packets in the status stage must be transmitted and received with the data PID set to DATA1 using the DCPCTR.SQSET bit.

When a zero-length packet is received, check the receive-data length in the CFIFOCTR.DTLN[8:0] bits after a BRDY interrupt is generated, and then clear the FIFO buffer using the BCLR bit.

28.3.9.2 Control transfers in device controller mode

(1) Setup stage

The USBFS sends an ACK response to a normal setup packet for the USBFS. The USBFS operates in the setup stage as follows:

On receiving a new setup packet, the USBFS sets the following bits:

- Sets the INTSTS0.VALID bit to 1
- Sets the DCPCTR.PID[1:0] bits to NAK
- Sets the DCPCTR.CCPL bit to 0.

When the USBFS receives a data packet following a setup packet, it stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Before performing the response processing for a control transfer, set the VALID flag to 0. When the VALID bit = 1, PID

28.3.9.1 主机控制器模式下的控制传输

(1) 设置阶段

USQREQ、USBVAL、USBINDX和USBLENG寄存器用于传输设置事务的USB请求。将设置数据包数据写入寄存器，然后向DCPCTR.SUREQ位写入1，以传输设置事务的指定数据。事务完成后，SUREQ位设置为0。在SUREQ=1时不要更改这些USB请求寄存器。

当检测到连接的功能设备时，软件必须使用此序列为设备发出第一个设置事务，并将DCPMAXP.DEVSEL[3:0]位设置为0，并适当设置DEVADD0.USBSPD[1:0]位。

当连接的功能器件转移到地址状态时，软件必须使用此序列发出设置事务，并在DEVSEL[3:0]位中设置分配的USB地址，并适当设置与指定USB地址相关的DEVADDn中的位。例如，当PIPEMAXP.DEVSEL[3:0]=0010b时，在DEVADD2中进行适当的设置。当PIPEMAXP.DEVSEL[3:0]=0101b时，在DEVADD5中进行适当的设置。

发送设置事务数据时，根据外围设备的响应（INTSTS1中的SIGN或SACK位）生成中断请求。该中断请求允许软件检查设置事务结果。

一个DATA0数据包（USB请求）用于设置事务总是被传输，无论状态如何
DCPCTR.SQMON bit.

(2) 数据阶段

数据级用于使用DCPFIFO缓冲区传输数据。

在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。在DCPCFG.DIR位中指定传输方向。

对于数据阶段的第一个数据包，数据PID必须作为DATA1传输。在DCPCTR.SQSET位中设置数据PID=DATA1，并设置PID位=BUF。使用BRDY或BEMP中断检测数据传输的完成。

对于控制写传输，当要发送的数据字节数是最大数据包大小的整数倍时，软件必须在最后发送一个长度为零的数据包。

(3) 状态阶段

状态阶段用于在数据阶段的相反方向上进行零长度分组数据传输。与数据阶段一样，使用DCPFIFO缓冲区传输数据。事务使用与数据阶段相同的过程执行。

状态阶段的数据包必须在数据PID设置为DATA1的情况下使用
DCPCTR.SQSET bit.

当接收到零长度数据包时，在产生BRDY中断后检查CFIFOCTR.DTLN[8:0]位中的接收数据长度，然后使用BCLR位清除FIFO缓冲区。

28.3.9.2 设备控制器模式下的控制传输

(1) 设置阶段

USBFS向USBFS的正常设置数据包发送ACK响应。USBFS在设置阶段运行如下：

在接收到新的设置数据包时，USBFS设置以下位：

- 将INTSTS0.VALID位设置为1
- 将DCPCTR.PID[1:0]位设置为NAK
- 将DCPCTR.CCPL位设置为0。

当USBFS在setup数据包之后接收到数据包时，它会将USB请求参数存储在USBREQ中，
USBVAL, USBINDX, and USBLENG.

在执行控制传输的响应处理之前，将VALID标志设置为0。当VALID位=1时，PID

= BUF cannot be set, and the data stage cannot be terminated.

Using the VALID bit function, the USBFS can suspend the current request being processed when it receives a new USB request during a control transfer and return a response to the latest request.

In addition, the USBFS automatically detects the direction bit (bmRequestType bit [8]) and the request data length (wLength) in the received USB request. The USBFS also distinguishes between control read transfers, control write transfers, no-data control transfers, and control stage transitions. For an incorrect sequence, a sequence error occurs in the control transfer stage transition interrupt, and the interrupt is reported to software. For the stage control of the USBFS, see Figure 28.12.

(2) Data stage

The DCP must be used to execute data transfers for received USB requests. Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit.

If the transfer data is larger than the size of the DCP FIFO buffer, perform data transfer using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

(3) Status stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to BUF.

After the specified settings are made, the USBFS automatically executes the status stage according to the data transfer direction determined at the setup stage. The procedure is as follows:

- For control read transfers
  The USBFS receives a zero-length packet from the USB host and transmits an ACK response.
- For control write transfers and no-data control transfers
  The USBFS transmits a zero-length packet and receives an ACK response from the USB host.

(4) Control transfer auto response function

The USBFS automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, a response from software is required.

- bmRequestType is not 00h: Any transfer other than a control write transfer
- wIndex is not 00h: Request error
- wLength is not 00h: Any transfer other than a no-data control transfer
- wValue is larger than 7Fh: Request error
- INTSTS0.DVSQ[2:0] are 011b (Configured state): Control transfer of a device state error.

For all requests other than the SET_ADDRESS request, a response is required from the associated software.

28.3.10 Bulk Transfers (Pipes 1 to 5)

The FIFO buffer usage (single/double buffer setting) can be selected for bulk transfers. The USBFS provides the following functions for bulk transfers:

- BRDY interrupt function (PIPECFG.BFRE bit), see section 28.3.3.1, (2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1.
- Transaction count function (PIPEnTRE.TRENB, TRCLR, and PIPEnTRN.TRNCNT[15:0] bits), see section 28.3.4.5, Transaction counter for pipes 1 to 5 in the receiving direction.
- Response PID = NAK function (PIPECFG.SHTNAK bit), see section 28.3.4.8, Response PID = NAK function.
- Auto response mode (PIPEnCTR.ATREPM bit), see section 28.3.4.9, Auto response mode.

28.3.11 Interrupt Transfers (Pipes 6 to 9)

In device controller mode, the USBFS performs interrupt transfers based on the timing dictated by the host controller.

In host controller mode, software can set the timing for issuing tokens using the interval counter.

=BUF不能设置，数据阶段不能终止。

使用VALID位功能，USBFS可以在控制传输期间收到新的USB请求时暂停当前正在处理的请求，并返回对最新请求的响应。

此外，USBFS会自动检测接收到的USB请求中的方向位（bmRequestTypebit[8]）和请求数据长度（wLength）。USBFS还区分控制读取传输、控制写入传输、无数据控制传输和控制阶段转换。对于不正确的序列，在控制转移阶段转换中断中发生序列错误，并将中断报告给软件。USBFS的阶段控制见图28.12。

(2) 数据阶段

DCP必须用于执行接收到的USB请求的数据传输。在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。

如果传输数据大于DCPFIFO缓冲区的大小，则使用控制写传输的BRDY中断和控制读传输的BEMP中断执行数据传输。

(3) 状态阶段

通过将DCPCTR.CCPL位设置为1而将DCPCTR.PID[1:0]位设置为BUF来终止控制传输。

完成指定设置后，USBFS根据设置阶段确定的数据传输方向自动执行状态阶段。程序如下：

- 对于控制读取传输
  USBFS从USB主机接收零长度数据包并发送ACK响应。
- 用于控制写传输和无数据控制传输
  USBFS发送一个长度为零的数据包并接收来自USB主机的ACK响应。

(4) 控制转移自动响应功能

USBFS自动响应正确的SET_ADDRESS请求。如果出现以下任何错误SET_ADDRESS请求，需要软件的响应。

- bmRequestType不是00h：控制写入传输以外的任何传输
- wIndex不是00h：请求错误
- wLength不是00h：除无数据控制传输之外的任何传输
- wValue大于7Fh：请求错误
- INTSTS0.DVSQ[2:0]为011b（已配置状态）：设备状态错误的控制传输。

对于除SET_ADDRESS请求之外的所有请求，都需要相关软件的响应。

28.3.10 批量传输（管道1到5）

可以为批量传输选择FIFO缓冲区使用（单双缓冲区设置）。USBFS为批量传输提供以下功能：

- BRDY中断功能（PIPECFG.BFRE位），见第28.3.3.1节，(2)当SOFCFG.BRDYM=0和PIPECFG.BFRE = 1.
- 事务计数函数（PIPEnTRE.TRENB、TRCLR和PIPEnTRN.TRNCNT[15:0]位），请参见第28.3.4.5节，接收方向上管道1到5的事务计数器。
- 响应PID=NAK功能（PIPECFG.SHTNAK位），请参见第28.3.4.8节，响应PID=NAK功能。
- 自动响应模式（PIPEnCTR.ATREPM位），请参见第28.3.4.9节，自动响应模式。

28.3.11 中断传输（管道6到9）

在设备控制器模式下，USBFS根据主机控制器规定的时序执行中断传输。

在主机控制器模式下，软件可以使用间隔计数器设置发布令牌的时间。

28.3.11.1 Interval counter for interrupt transfers in host controller mode

Specify the transaction interval for interrupt transfers in the PIPEPERI.IITV[2:0] bits.

(1) The USBFS issues interrupt transfer tokens based on this interval.Counter initialization

The USBFS initializes the interval counter under the following conditions:

- Power-on reset
  This initializes the IITV[2:0] bits.
- FIFO buffer initialization using the PIPEnCTR.ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value. Setting the PIPEnCTR.ACLRM bit to 0 starts counting from the value set in IITV[2:0].

The interval counter is not initialized in the following case:

- USB bus reset or USB suspended:
  The IITV[2:0] bits are not initialized. Setting 1 to the DVSTCTR0.UACT bit starts counting from the value saved before entering the USB bus reset state or USB Suspended state.

(2) Operation when tokens cannot be transmitted or received even on token generation

No token is generated in the following cases even at token generation time. In these cases, the USBFS tries to execute the transaction in the next interval.

- When the PID is set to NAK or STALL
- When the FIFO buffer is full at token transmit time in the receiving (IN) direction
- When there is no data to be transmitted in the FIFO buffer at token transmit time in the transmitting (OUT) direction.

28.3.12 Isochronous Transfers (Pipes 1 and 2)

The USBFS provides the following functions for isochronous transfers:

- Notification of isochronous transfer error
- Interval counter (specified in the PIPEPERI.IITV[2:0] bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (specified in the PIPEPERI.IFIS bit).

28.3.12.1 Error detection in isochronous transfers

The USBFS provides a function for detecting the errors described in this section, so that when errors occur in isochronous transfers, they can be controlled by software. Table 28.23 and Table 28.24 show the priority order for errors detected by the USBFS and the associated interrupts.

(a) PID errors

- The PID value of the received packet is invalid.

(b) CRC errors and bit stuffing errors

- A CRC error is found in a received packet or the bit stuffing is invalid.

(c) Maximum packet size exceeded

- The data size of the received packet exceeds the specified maximum packet size.

(d) Overrun and underrun errors

In host controller mode:

- The FIFO buffer is full at token transmit time in the IN (receiving) direction
- There is no data to be sent in the FIFO buffer at token transmit time in the OUT (transmitting) direction.

28.3.11.1 主机控制器模式下中断传输的间隔计数器

在PIPEPERI.IITV[2:0]位中指定中断传输的事务间隔。

(1) USBFS基于此时间间隔发出中断传输令牌。计数器初始化

USBFS在以下条件下初始化间隔计数器：

- Power-on reset
  这将初始化IITV[2:0]位。
- 使用PIPEnCTR.ACLRM位初始化FIFO缓冲区：
  这不会初始化IITV[2:0]位，但会初始化计数值。将PIPEnCTR.ACLRM位设置为0从IITV[2:0]中设置的值开始计数。

在以下情况下不初始化间隔计数器：

- USB总线复位或USB挂起：
  IITV[2:0]位未初始化。将DVSTCTR0.UACT位置1从进入USB总线复位状态或USB暂停状态之前保存的值开始计数。

(2) 即使在生成令牌时也无法发送或接收令牌时的操作

在以下情况下，即使在生成令牌时也不会生成令牌。在这些情况下，USBFS会尝试在下一个时间间隔执行事务。

- 当PID设置为NAK或STALL时
- 当FIFO缓冲区在接收(IN)方向的令牌传输时间已满时
- 在发送(OUT)方向的令牌发送时间，当FIFO缓冲区中没有要发送的数据时。

28.3.12 同步传输（管道1和2）

USBFS为同步传输提供以下功能：

- 同步传输错误通知
- 间隔计数器（在PIPEPERI.IITV[2:0]位中指定）
- 同步IN传输数据设置控制（IDLY功能）
- 同步IN传输缓冲区刷新功能（在PIPEPERI.IFIS位中指定）。

28.3.12.1 同步传输中的错误检测

USBFS提供了检测本节所述的错误的功能，以便在同步传输中发生错误时，可以通过软件进行控制。表28.23和表28.24显示了USBFS检测到的错误和相关中断的优先级顺序。

(a) PID错误

- 接收到的数据包的PID值无效。

(b) CRC错误和位填充错误

- 在收到的数据包中发现CRC错误或位填充无效。

(c) 超出最大数据包大小

- 接收到的数据包的数据大小超过了指定的最大数据包大小。

(d) 溢出和欠载错误

在主机控制器模式下：

- FIFO缓冲区在IN（接收）方向的令牌发送时间已满
- 在OUT（发送）方向的令牌发送时，FIFO缓冲区中没有要发送的数据。

In device controller mode:

- There is no data to be sent in the FIFO buffer at token receive time in the IN (transmitting) direction
- The FIFO buffer is full at token receive time in the OUT (receiving) direction.

(e) Interval errors

In device controller mode, the following cases are treated as an interval error:

- Failure to receive an IN token in the interval frame during an isochronous IN transfer
- Failure to receive an OUT token in the interval frame during an isochronous OUT transfer.

Table 28.23 Error detection for token transmission and reception

Detection priority	Error	Generated interrupt and status
1	PID error	No interrupts are generated in either host or device controller mode (ignored as a corrupted packet)
2	CRC or bit stuffing error	No interrupts are generated in either host or device controller mode (ignored as a corrupted packet)
3	Overrun or underrun error	An NRDY interrupt is generated to set the FRMNUM.OVRN bit to 1 in both host and device controller modes. In device controller mode, a zero-length packet is transmitted in response to an IN token. No data packets are received in response to OUT token.
4	Interval error	An NRDY interrupt is generated in device controller mode. No interrupt is generated in host controller mode.

Table 28.24 Error detection for data packet reception

Detection priority	Error	Generated interrupt and status
1	PID error	No interrupts are generated (ignored as a corrupted packet)
2	CRC or bit stuffing error	An NRDY interrupt is generated and the FRMNUM.CRCE bit is set to 1 in both host and device controller modes
3	Maximum packet size exceeded error	A BEMP interrupt is generated and the PID[1:0] bits set to STALL in both host and device controller modes

28.3.12.2 DATA-PID

In device controller mode, the USBFS responds as follows to a received PID:

(1) IN direction

- DATA0: Transmitted as data packet PID
- DATA1: Not transmitted
- DATA2: Not transmitted
- mDATA: Not transmitted.

(2) OUT direction

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Packets ignored
- mDATA: Packets ignored.

28.3.12.3 Interval counter

The isochronous transfer interval can be set in the PIPEPERI.IITV[2:0] bits. In device controller mode, the interval

在设备控制器模式下：

- 在IN（发送）方向的令牌接收时间，FIFO缓冲区中没有要发送的数据
- FIFO缓冲区在OUT（接收）方向上的令牌接收时间已满。

(e) 间隔错误

在设备控制器模式下，以下情况被视为间隔错误：

- 在同步IN传输期间未能在间隔帧中接收IN令牌
- 在同步OUT传输期间未能在间隔帧中接收OUT令牌。

Table 28.23 令牌发送和接收的错误检测

检测优先级	Error	产生的中断和状态
1	PID错误	在主机或设备控制器模式下都不会产生中断（被忽略为损坏的数据包）
2	CRC或位填充错误	在主机或设备控制器模式下都不会产生中断（被忽略为损坏的数据包）
3	溢出或欠载错误	在主机和设备控制器模式下，都会产生一个NRDY中断来将FRMNUM.OVRN位设置为1。在设备控制器模式下，发送一个零长度数据包以响应IN令牌。 没有接收到响应OUT令牌的数据包。
4	间隔误差	在设备控制器模式下会产生一个NRDY中断。在主机控制器模式下不产生中断。

Table 28.24 数据包接收错误检测

检测优先级	Error	产生的中断和状态
1	PID错误	不产生中断（作为损坏的数据包被忽略）
2	CRC或位填充错误	在主机和设备控制器模式下都会产生一个NRDY中断并且FRMNUM.CRCE位设置为1
3	超出最大数据包大小错误	在主机和设备控制器模式下都会产生BEMP中断并且PID[1:0]位设置为STALL

28.3.12.2 DATA-PID

在设备控制器模式下，USBFS对收到的PID做出如下响应：

(1) 在方向

- DATA0：作为数据包PID发送
- DATA1：未发送
- DATA2：未传输
- mDATA：未传输。

(2) 出方向

- DATA0：作为数据包PID正常接收
- DATA1：作为数据包PID正常接收
- DATA2：数据包被忽略
- mDATA：数据包被忽略。

28.3.12.3 间隔计数器

同步传输间隔可以在PIPEPERI.IITV[2:0]位中设置。在设备控制器模式下，间隔

counter enables the functions as shown in Table 28.25. In host controller mode, the USBFS generates the token issuance timing, and the interval counter operation is the same as that for interrupt transfers.

Table 28.25 Interval counter function in device controller mode

Transfer direction	Function	Conditions for detection
IN	Transmit buffer flush	Failure to receive an IN token successfully in the interval frame during an isochronous IN transfer
OUT	Notification of no reception of token	Failure to receive an OUT token successfully in the interval frame during an isochronous OUT transfer

The interval count is performed when an SOF is received or for interpolated SOFs, so the isochronism can be maintained even if an SOF is corrupt. The frame interval can be set to 2^{IITV} frames.

(1) Counter initialization in device controller mode

The USBFS initializes the interval counter under the following conditions:

- Power-on reset:
  This initializes the PIPEPERI.IITV[2:0] bits.
- FIFO buffer initialization using the ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value.

After the interval counter is initialized, the interval count starts under either of the following conditions when a packet is transferred successfully:

- An SOF is received after data is transmitted in response to an IN token when PID = BUF
- An SOF is received after data is received in response to an OUT token when PID = BUF.

The interval counter is not initialized in the following conditions:

- When the PID[1:0] bits are set to NAK or STALL
  This does not stop the interval timer. The USBFS attempts the transaction in the next interval.
- When the USB bus is reset or USBFS is suspended
  This does not initialize the IITV[2:0] bits. When an SOF is received, the interval counter starts counting from the value set before SOF was received.

(2) Interval counting and transfer control in host controller mode

The USBFS controls the interval between token issuance operations based on the PIPEPERI.IITV[2:0] bit settings. Specifically, the USBFS issues a token for a selected pipe once every 2^{IITV} frames.

The USBFS starts counting the token issuance interval at the frame following the frame in which the PID[1:0] bits are set to BUF by software.

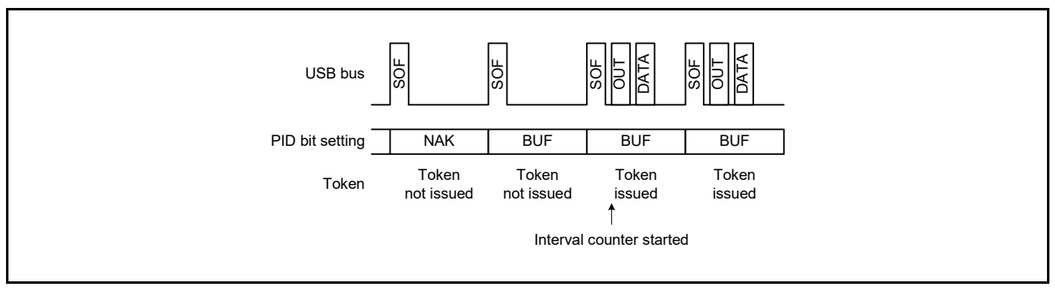


Figure 28.13 Token issuance when IITV = 0

计数器启用表28.25中所示的功能。在主机控制器模式下，USBFS产生令牌发布时序，间隔计数器操作与中断传输相同。

Table 28.25 设备控制器模式下的间隔计数器功能

转移方向	Function	检测条件
IN	发送缓冲区刷新	在等时IN传输期间未能在间隔帧中成功接收IN令牌
OUT	未收到令牌的通知	在等时期间未能在间隔帧中成功接收OUT令牌 转出

间隔计数在接收到SOF时执行或对插值SOF执行，因此即使SOF损坏也可以保持等时性。帧间隔可以设置为2个IITV帧。

(1) 设备控制器模式下的计数器初始化

USBFS在以下条件下初始化间隔计数器：

- Power-on reset:
  这将初始化PIPEPERI.IITV[2:0]位。
- 使用ACLRM位初始化FIFO缓冲区：
  这不会初始化IITV[2:0]位，但会初始化计数值。

间隔计数器初始化后，当数据包传输成功时，间隔计数在以下任一条件下开始：

- 当PID=BUF时，响应IN令牌传输数据后收到SOF
- 当PID=BUF时，接收到响应于OUT令牌的数据后接收到SOF。

间隔计数器在以下情况下不会初始化：

- 当PID[1:0]位设置为NAK或STALL
  这不会停止间隔计时器。USBFS在下一个间隔尝试事务。
- 当USB总线复位或USBFS暂停时
  这不会初始化IITV[2:0]位。当接收到SOF时，间隔计数器从接收到SOF之前设置的值开始计数。

(2) 主机控制器模式下的间隔计数和传输控制

USBFS根据PIPEPERI.IITV[2:0]位设置控制令牌发布操作之间的间隔。
具体来说，USBFS每2个IITV帧为所选管道发布一次令牌。

USBFS在PID[1:0]位被软件设置为BUF的帧之后的帧开始计算令牌发布间隔。

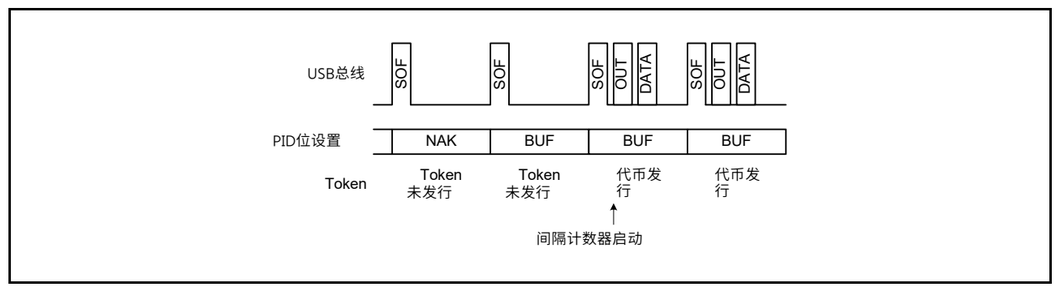


Figure 28.13 IITV=0时的代币发行

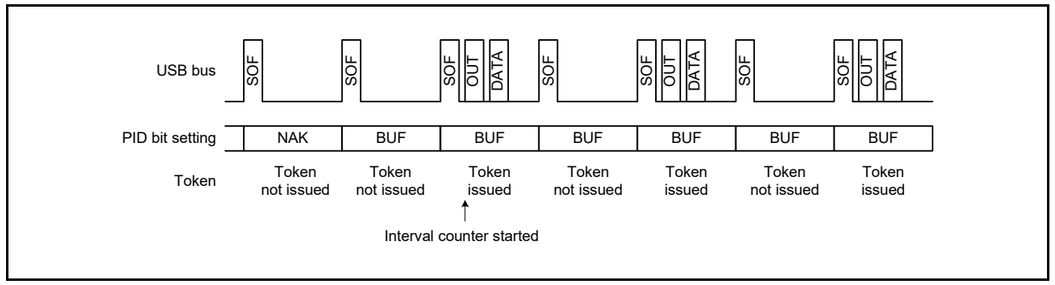


Figure 28.14 Token issuance when IITV = 1

When the selected pipe is set for isochronous transfers, the USB carries out the following operation in addition to controlling the token issuance interval. The USB issues a token even when the NRDY interrupt generation condition is satisfied.

(a) When the selected pipe is for isochronous IN transfers

The USBFS generates an NRDY interrupt when the USBFS issues an IN token but does not receive a packet successfully from a peripheral device (no response or packet error).

The USBFS sets the FRMNUM.OVRN bit to 1, generating an NRDY interrupt, when the time to issue an IN token comes while the USBFS cannot receive data because the FIFO buffer is full, because the CPU or DMAC/DTC is too slow in reading data from the FIFO buffer.

(b) When the selected pipe is for isochronous OUT transfers

The USBFS sets the OVRN bit to 1, generating an NRDY interrupt and transmitting a zero-length packet, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer, because the CPU or DMAC/DTC is too slow in writing data to the FIFO buffer.

The token issuance interval is reset on any of the following conditions:

- When the USBFS is reset through a reset pin
  This initializes the IITV[2:0] bits.
- When the PIPEnCTR.ACLRM bit is set to 1 by software.

(3) Interval counting and transfer control in device controller mode

(a) When the selected pipe is for isochronous OUT transfers

The USBFS generates an NRDY interrupt when it fails to receive a data packet within the interval set by the PIPEPERI.IITV[2:0] bits.

The USBFS also generates an NRDY interrupt when it fails to receive data because of a CRC error or other errors contained in the data packet or because of FIFO buffer is full.

The NRDY interrupt is generated on SOF packet reception. Even if the SOF packet is corrupted, internal interpolation allows the interrupt to be generated when the SOF packet is received. However, when the IITV bits are set to a value other than 0, the USBFS generates an NRDY interrupt on receiving an SOF packet for every interval after interval counting starts.

When the PID[1:0] bits are set to NAK by software after starting the interval timer, the USBFS does not generate an NRDY interrupt on receiving an SOF packet.

The timing for starting interval counting depend on the IITV[2:0] setting as follows:

- When the IITV[2:0] bits = 0:
  Interval counting starts at the next frame after software changes the PID[1:0] bits of the selected pipe to BUF.

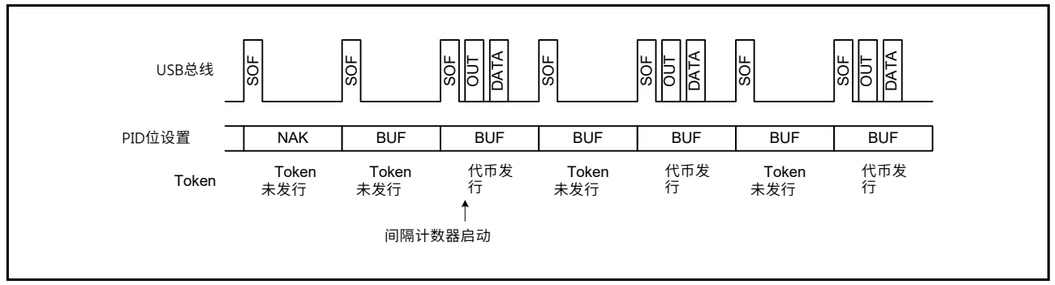


Figure 28.14 IITV=1时的代币发行

当所选管道设置为同步传输时，USB除了控制令牌发布间隔外，还会执行以下操作。即使满足NRDY中断生成条件，USB也会发出令牌。

(a) 当所选管道用于同步IN传输时

当USBFS发出IN令牌但未成功接收到来自外围设备的数据包（无响应或数据包错误）时，USBFS生成NRDY中断。

USBFS将FRMNUM.OVRN位设置为1，产生一个NRDY中断，此时发出IN令牌的时间到了，而USBFS无法接收数据，因为FIFO缓冲区已满，因为CPU或DMACDTC读取数据太慢从FIFO缓冲区。

(b) 当所选管道用于同步OUT传输时

USBFS将OVRN位设置为1，产生一个NRDY中断并发送一个长度为零的数据包，当发出OUT令牌的时间到来而FIFO缓冲区中没有要发送的数据时，因为CPU或DMACDTC是将数据写入FIFO缓冲区太慢。

令牌发行间隔在以下任何条件下重置：

- 当USBFS通过复位引脚复位时
  这将初始化IITV[2:0]位。
- 当PIPEnCTR.ACLRM位由软件设置为1时。

(3) 设备控制器模式下的间隔计数和传输控制

(a) 当所选管道用于同步OUT传输时

当USBFS在由
PIPEPERI.IITV[2:0] bits.

当由于数据包中包含的CRC错误或其他错误或由于FIFO缓冲区已满而无法接收数据时，USBFS也会产生NRDY中断。

NRDY中断在SOF数据包接收时产生。即使SOF数据包损坏，内部插值也允许在接收到SOF数据包时产生中断。但是，当IITV位设置为0以外的值时，USBFS会在间隔计数开始后的每个间隔接收到SOF数据包时产生NRDY中断。

当PID[1:0]位在启动间隔定时器后由软件设置为NAK时，USBFS不会产生
接收到SOF数据包时的NRDY中断。

开始间隔计数的时间取决于IITV[2:0]设置，如下所示：

- 当IITV[2:0]位=0时：
  在软件将所选管道的PID[1:0]位更改为BUF后，间隔计数从下一帧开始。

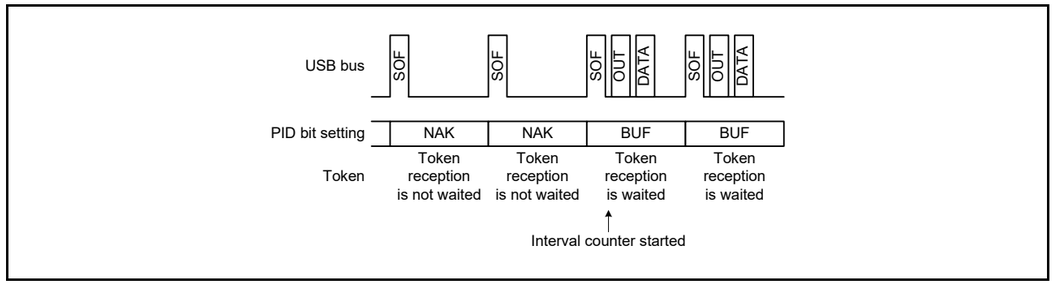


Figure 28.15 Relationship between frames and expected token reception when IITV = 0

- When the IITV ≠ 0: The interval counting starts on completion of successful reception of the first data packet after the PID[1:0] bits for the selected pipe are modified to BUF.

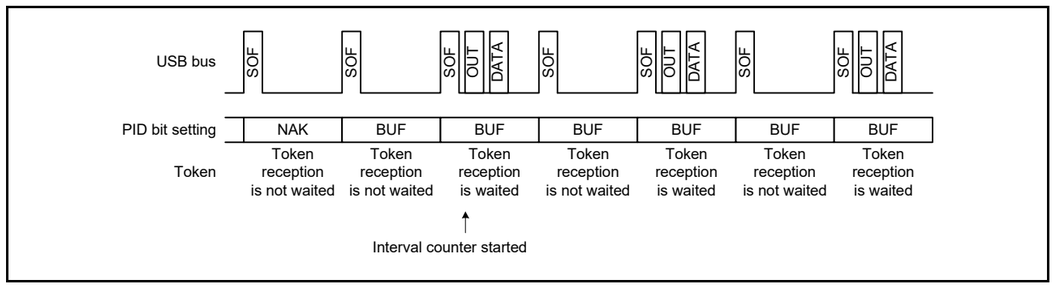


Figure 28.16 Relationship between frames and expected token reception when IITV ≠ 0

(b) When the selected pipe is for isochronous IN transfers

The PIPEPERI.IFIS bit must be 1 for this use case. When IFIS = 0, the USBFS transmits a data packet in response to a received IN token regardless of the PIPEPERI.IITV[2:0] setting.

When IFIS is 1 and there is data to be transmitted in the FIFO buffer, the USBFS clears the FIFO buffer when it fails to receive an IN token in the frame at the interval set in the IITV[2:0] bits.

The USBFS also clears the FIFO buffer when it fails to receive an IN token successfully because of a bus error, such as a CRC error, contained in the IN token.

The FIFO buffer is cleared on SOF packet reception. Even if the SOF packet is corrupted, the internal interpolation allows the FIFO buffer to be cleared when the SOF packet is received.

The timing to start interval counting depends on the IITV[2:0] setting, as with OUT transfers.

The interval is counted on any of the following conditions in device controller mode:

- When a hardware reset is applied to the USBFS (which also sets the IITV[2:0] bits to 000b)
- When the PIPEnCTR.ACLRM bit is set to 1 by software
- When the USBFS detects a USB bus reset.

(4) Transmit data setup for isochronous transfers in device controller mode

With isochronous data transmission using the USBFS in device controller mode, after data is written to the FIFO buffer, a data packet can be transmitted in the first frame after the SOF packet is detected. This isochronous transfer transmit data setup function can identify the frame that started transmission.

When the double buffering is used, transmission is only enabled for the buffer where data writing was completed first, even after the data write to both buffers is complete. Accordingly, even if multiple IN tokens are received, only the one packet of FIFO buffer data is transmitted.

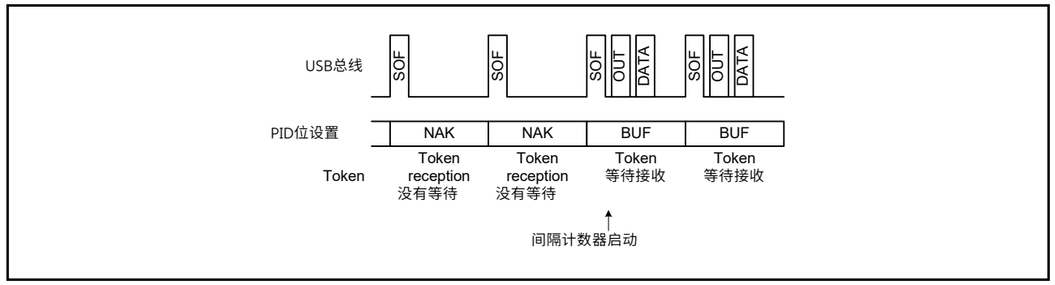


Figure 28.15 IITV=0时帧与预期令牌接收之间的关系

- 当IITV≠0时：将所选管道的PID[1:0]位修改为BUF后，成功接收第一个数据包完成后，开始间隔计数。

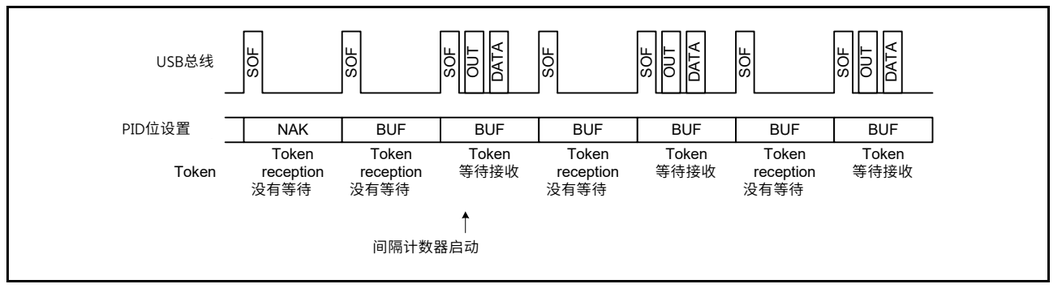


Figure 28.16 IITV≠0时帧与预期令牌接收的关系

(b) 当所选管道用于同步IN传输时

对于此用例，PIPEPERI.IFIS位必须为1。当IFIS=0时，无论PIPEPERI.IITV[2:0]设置如何，USBFS都会发送一个数据包以响应接收到的IN令牌。

当IFIS为1且FIFO缓冲区中有数据要发送时，如果USBFS在IITV[2:0]位设置的时间间隔内未能接收到帧中的IN令牌，则清除FIFO缓冲区。

当USBFS由于总线错误（例如
CRC错误，包含在IN令牌中。

FIFO缓冲区在SOF数据包接收时被清除。即使SOF数据包损坏，内部插值也允许在接收到SOF数据包时清除FIFO缓冲区。

开始间隔计数的时间取决于IITV[2:0]设置，与OUT传输一样。

在设备控制器模式下，根据以下任何条件计算间隔：

- 当对USBFS应用硬件复位时（也将IITV[2:0]位设置为000b）
- 当PIPEnCTR.ACLRM位由软件设置为1时
- 当USBFS检测到USB总线复位时。

(4) 设备控制器模式下同步传输的传输数据设置

在设备控制器模式下使用USBFS进行同步数据传输，数据写入FIFO缓冲区后，可在检测到SOF包后的第一帧发送数据包。此同步传输传输数据设置功能可以识别开始传输的帧。

使用双缓冲时，仅对先完成数据写入的缓冲区启用传输，即使在两个缓冲区的数据写入完成后也是如此。因此，即使接收到多个IN令牌，也仅发送一包FIFO缓冲器数据。

When the FIFO buffer is ready to transmit data when an IN token is received, the data is transferred and a normal response is returned. However, if the FIFO buffer cannot transmit data, a zero-length packet is transmitted and an underrun error occurs.

Figure 28.17 shows an example transmission using the isochronous transfer transmission data setup function when IITV = 0 (every frame) is set.

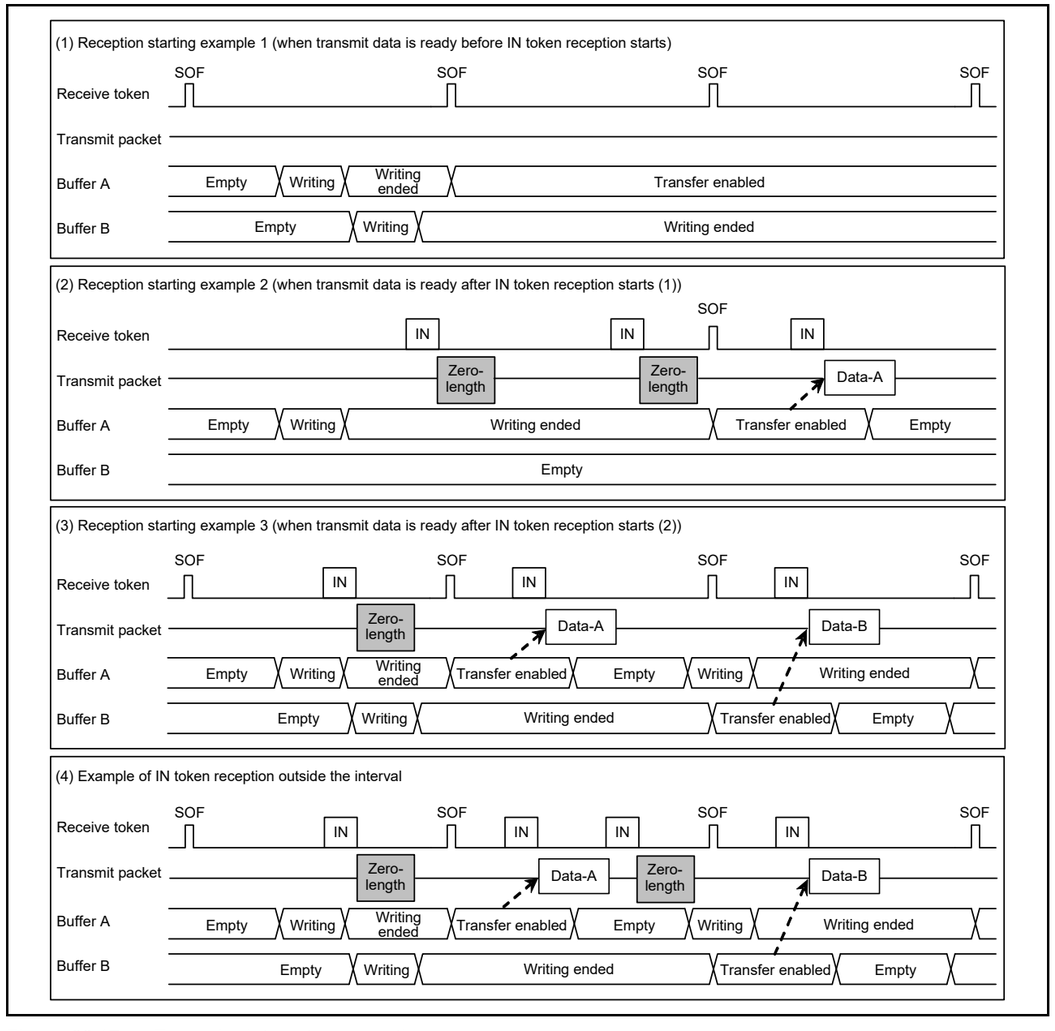


Figure 28.17 Example data setup operation

(5) Transmit buffer flush for isochronous transfers in device controller mode

In device controller mode during isochronous data transmission, if the USBFS receives an SOF packet for the next frame without receiving an IN token in the interval frame, it operates as if the IN token is corrupt and clears the buffer that is enabled for transmission, putting that buffer in the writing enabled state.

When double buffering is used and writing to both buffers is complete, the cleared FIFO buffer is assumed to be the one where the data was transmitted in the interval frame, and transmission is enabled for the FIFO buffer that was not cleared on SOF packet reception.

The timing of the buffer flush function depends on the PIPEPERI.IITV[2:0] setting as follows:

当接收到IN令牌时，当FIFO缓冲区准备好传输数据时，将传输数据并返回正常响应。但是，如果FIFO缓冲区无法传输数据，则会传输零长度数据包并发生欠载错误。

图28.17显示了在设置IITV=0（每帧）时使用同步传输传输数据设置功能的传输示例。

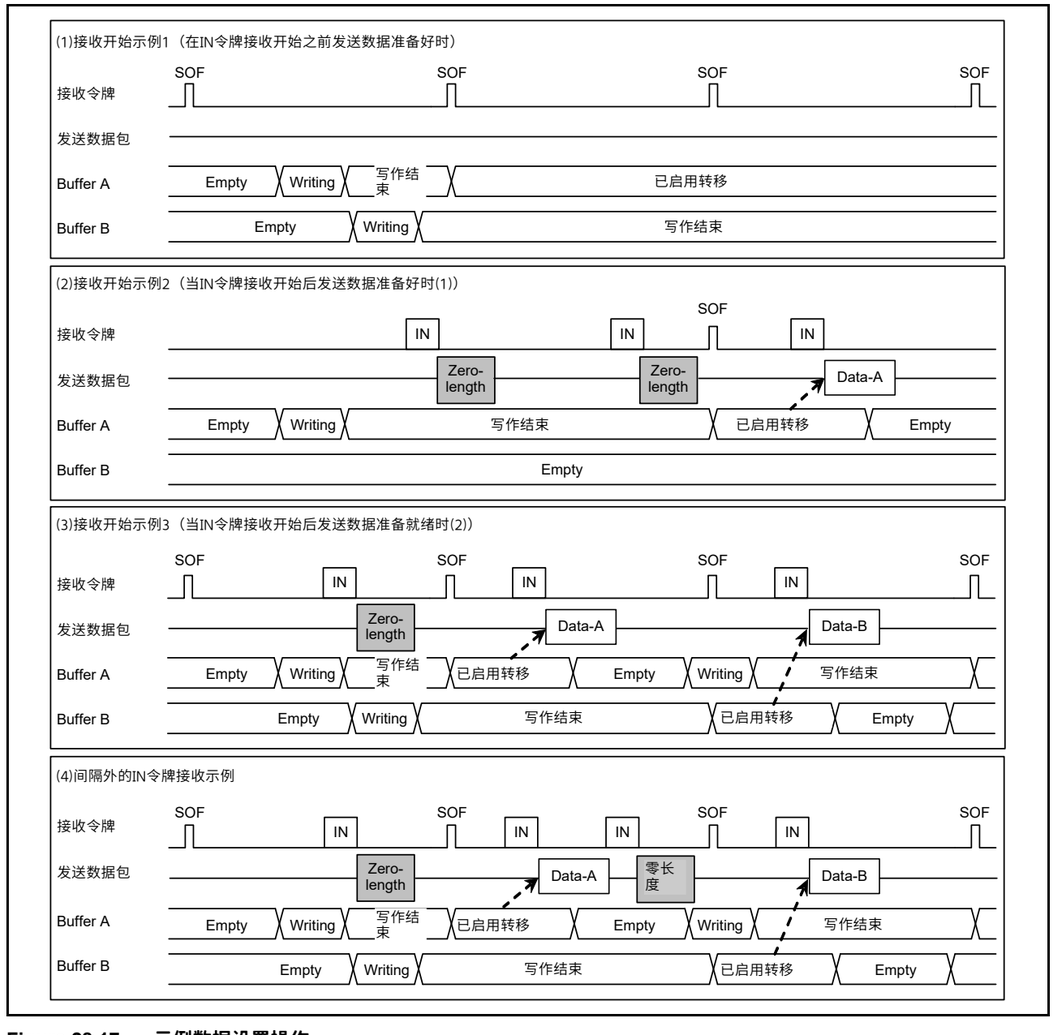


Figure 28.17 示例数据设置操作

(5) 设备控制器模式下同步传输的传输缓冲区刷新

在同步数据传输期间的设备控制器模式下，如果USBFS接收到下一帧的SOF数据包，而在间隔帧中没有接收到IN令牌，则它会像IN令牌损坏一样操作并清除启用传输的缓冲区，将该缓冲区处于写入启用状态。

当使用双缓冲并完成对两个缓冲区的写入时，已清除的FIFO缓冲区被假定为在间隔帧中传输数据的缓冲区，并为接收SOF数据包时未清除的FIFO缓冲区启用传输。

缓冲区刷新功能的时间取决于PIPEPERI.IITV[2:0]设置，如下所示：

- When IITV = 0:
  The buffer flush operation starts from the first frame after the pipe is enabled.
- When IITV ≠ 0:
  The buffer flush operation starts after the first normal transaction.

Figure 28.18 shows an example buffer flush. When an unanticipated token is received before the interval frame, the USBFS sends the write data or a zero-length packet as an underrun error, depending on the data setup status.

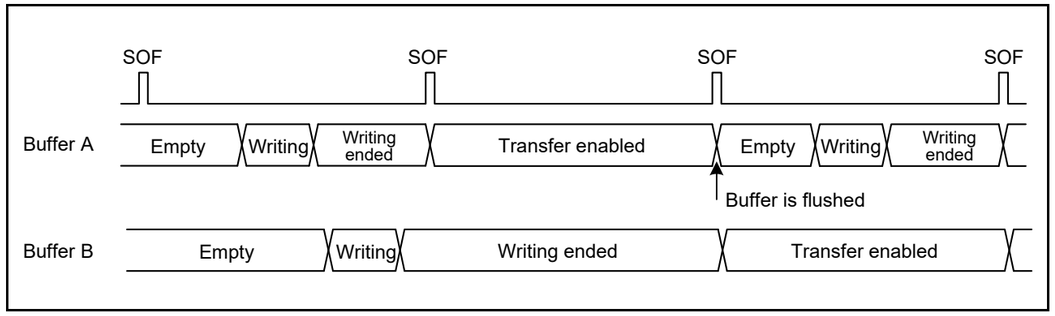


Figure 28.18 Example buffer flush operation

Figure 28.19 shows an example interval error occurrence. There are five types of interval errors, as shown in the figure. An interval error occurs at timing ① in the figure, and the buffer flush function is activated.

If an interval error occurs during an IN transfer, the buffer flush function is activated. If it occurs during an OUT transfer, an NRDY interrupt is generated. Use the FRMNUM.OVRN bit to distinguish between this and NRDY interrupts triggered by received packet errors and overrun errors.

For tokens that are shaded in the figure, responses are returned based on the FIFO buffer status.

- IN direction:
  - If the buffer is ready to transfer data, the data is transferred and a normal response is returned
  - If the buffer is not ready to transfer data, a zero-length packet is transmitted and an underrun error occurs.
- OUT direction:
  - If the buffer is ready to receive data, the data is received and a normal response is returned
  - If the buffer is not ready to receive data, the received data is discarded and an overrun error occurs.

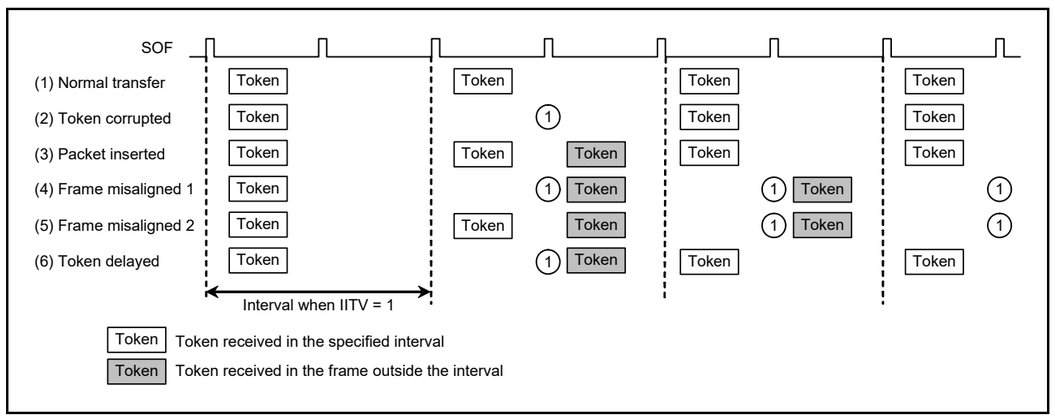


Figure 28.19 Example interval error occurrence when IITV = 1

- When IITV = 0:
  缓冲区刷新操作从启用管道后的第一帧开始。
- When IITV ≠ 0:
  缓冲区刷新操作在第一个正常事务之后开始。

图28.18显示了一个示例缓冲区刷新。当在间隔帧之前收到未预料到的令牌时，
USBFS根据数据设置状态将写入数据或零长度数据包作为欠载错误发送。

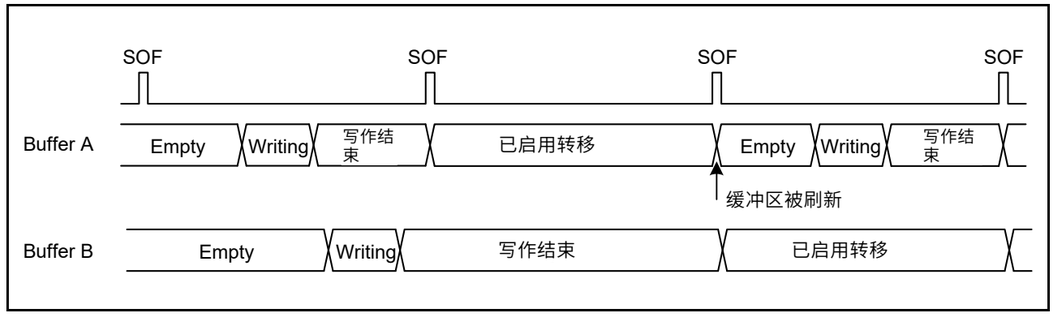


Figure 28.18 缓冲区刷新操作示例

图28.19显示了一个发生间隔错误的示例。如图所示，有五种区间误差。
定时出现间隔错误 ① 图中，缓冲区刷新功能被激活。

如果在IN传输期间发生间隔错误，则会激活缓冲区刷新功能。如果它发生在OUT传输期间，则会产生NRDY中断。使用FRMNUM.OVRN位来区分此中断和由接收数据包错误和溢出错误触发的NRDY中断。

对于图中带阴影的令牌，根据FIFO缓冲区状态返回响应。

- IN direction:
  - 如果缓冲区准备好传输数据，则传输数据并返回正常响应
  - 如果缓冲区尚未准备好传输数据，则会传输零长度数据包并发生欠载错误。
- OUT direction:
  - 如果缓冲区准备好接收数据，则接收数据并返回正常响应
  - 如果缓冲区没有准备好接收数据，则丢弃接收到的数据并发生溢出错误。

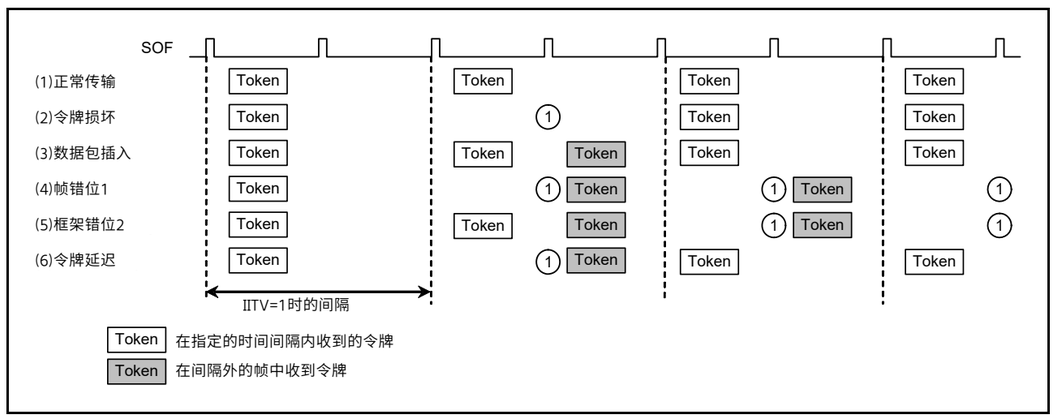


Figure 28.19 IITV=1时发生的示例间隔错误

28.3.13 SOF Interpolation Function

In device controller mode, if packet reception is disabled at intervals of 1 ms because the SOF packet is corrupted or missing, the USBFS interpolates the SOF. SOF interpolation begins when the USBE and SCKE bits in SYSCFG are set to 1 and an SOF packet is received. The interpolation function is initialized under the following conditions:

- MCU reset
- USB bus reset
- Suspended state detection.

The SOF interpolation operates as follows:

- The interpolation function is not activated until an SOF packet is received.
- When the first SOF packet is received, interpolation is performed by counting 1 ms on the 48-MHz internal clock
- When the second and subsequent SOF packets are received, interpolation is performed at the previous reception interval
- Interpolation is not performed in the suspended state or on reception of a USB bus reset.

The USBFS supports the following functions controlled by SOF packet reception. These functions operate normally with SOF interpolation if the SOF packet is missing:

- Updating of the frame number
- SOFR interrupt timing
- Isochronous transfer interval count.

If an SOF packet is missing during full-speed operation, the FRMNUM.FRNM[10:0] bits are not updated.

28.3.14 Pipe Schedule

28.3.14.1 Conditions for generating transactions

In host controller mode and when the DVSTCTR0.UACT bit is set to 1, the USBFS generates transactions under the conditions shown in Table 28.26.

Table 28.26 Conditions for generating transactions

Transaction	Conditions for generation				
	DIR	PID	IITV0	Buffer state	SUREQ
Setup	—*1	—*1	—*1	—*1	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	Invalid	Receive area exists	—*1
	OUT	BUF	Invalid	Transmit data exists	—*1
Interrupt transfer	IN	BUF	Valid	Receive area exists	—*1
	OUT	BUF	Valid	Transmit data exists	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. An em dash (—) in the table indicates that the condition is unrelated to the generating of tokens. "Valid" indicates that, for interrupt transfers and isochronous transfers, a transaction is generated only in transfer frames that are based on the interval counter. "Invalid" indicates that a transaction is generated regardless of the interval counter.
Note 2. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.
Note 3. This indicates that a transaction is generated regardless of whether there is any data to be transmitted. If there is no data to be transmitted, however, a zero-length packet is transmitted.

28.3.13 SOF插值函数

在设备控制器模式下，如果由于SOF数据包损坏或丢失而每隔1ms禁用数据包接收，则USBFS会内插SOF。当SYSCFG中的USBE和SCKE位设置为1并且接收到SOF数据包时，SOF内插开始。插值函数在以下条件下初始化：

- MCU reset
- USB总线复位
- 暂停状态检测。

SOF插值操作如下：

- 在接收到SOF数据包之前，不会激活插值功能。
- 当接收到第一个SOF数据包时，通过在48-MHz内部时钟上计数1ms来执行插值
- 当接收到第二个和随后的SOF数据包时，以先前的接收间隔执行插值
- 在挂起状态或接收到USB总线复位时不执行插值。

USBFS支持以下由SOF数据包接收控制的功能。这些功能正常运行
如果SOF数据包丢失，则SOF插值：

- 更新帧号
- SOFR中断时序
- 同步传输间隔计数。

如果在全速运行期间丢失SOF数据包，则不会更新FRMNUM.FRNM[10:0]位。

28.3.14 管道计划

28.3.14.1 产生交易的条件

在主机控制器模式下，当DVSTCTR0.UACT位设置为1时，USBFS在表28.26所示的条件下生成事务。

Table 28.26 产生交易的条件

Transaction	生成条件				
	DIR	PID	IITV0	缓冲状态	SUREQ
Setup	—*1	—*1	—*1	—*1	1 setting
控制传输数据阶段、状态阶段、批量传输	IN	BUF	Invalid	接收区存在	—*1
	OUT	BUF	Invalid	传输数据存在	—*1
中断传输	IN	BUF	Valid	接收区存在	—*1
	OUT	BUF	Valid	传输数据存在	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. 表中的破折号(—)表示该条件与令牌的生成无关。"有效"表示，对于中断传输和同步传输，事务仅在基于间隔计数器的传输帧中生成。"无效"表示无论间隔计数器如何都生成事务。

Note 2. 这表示不管是否有接收区域，都会产生一个事务。但是，如果没有接收区域，则丢弃接收到的数据。

Note 3. 这表明无论是否有任何数据要传输，都会生成一个事务。然而，如果没有要传输的数据，则传输零长度数据包。

28.3.14.2 Transfer schedule

This section describes the transfer scheduling within a frame of the USBFS. After the USBFS sends an SOF, the transfer is performed in the following sequence:

1. Execution of periodic transfers:
   A pipe is searched for in the order of pipe 1 → pipe 2 → pipe 6 → pipe 7 → pipe 8 → pipe 9, and then if there is a pipe for which an isochronous or interrupt transfer transaction can be generated, the transaction is generated.
2. Setup transactions for control transfers:
   The DCP is checked, and if a setup transaction is possible, it is sent.
3. Execution of bulk transfers, control transfer data stages, and control transfer status stages:
   A pipe is searched for in the order of DCP → pipe 1 → pipe 2 → pipe 3 → pipe 4 → pipe 5, and if there is a pipe for which a transaction is for a bulk transfer, a control transfer data stage, or a control transfer status stage, the transaction is generated.
   When a transaction is generated, processing moves to the next transaction pipe regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, this step is repeated.

28.3.14.3 Enabling USB communication

Setting the DVSTCTR0.UACT bit to 1 initiates an SOF transmission, and transaction generation is enabled. Setting the UACT bit to 0 stops SOF transmission and the suspended state is invoked. If the UACT setting is changed from 1 to 0, processing stops after the next SOF is sent.

28.3.15 Battery Charging Detection Processing

It is possible to control the processing for data contact detection (D+ line contact check), primary detection (charger detection), and secondary detection (charger verification), which are defined in the Battery Charging specification. This section describes the required operations for an individual function device and a host device.

28.3.15.1 Processing in device controller mode

The following processing is required when operating the USBFS as a portable device for battery charging:

1. Detect when the data lines (D+ and D-) have made contact and start the processing for primary detection.
2. After primary detection starts, wait 40 ms for masking, then check the D- voltage level to confirm the primary detection result.
3. If the charger is detected during primary detection, start secondary detection.
4. After secondary detection starts, wait 40 ms for masking, then check the D+ voltage level to confirm the secondary detection result.

For step 1., after VBUS is detected using the VBINT and VBSTS bits:

1. Wait for 300 to 900 ms, then set the VDPSRCE0 and IDMSINKE0 bits in the USBBCCTRL0 register.
2. Set the IDPSRCE0 bit.
3. After a change from high to low on the D+ line is detected using the LNST[1:0] bits, clear the IDPSRCE0 bit, and set the VDPSRCE0 and IDMSINKE0 bits simultaneously*1.

For step 2., set the VDPSRCE0 and IDMSINKE0 bits and wait 40 ms, then use the CHGDETSTS0 bit to verify the primary detection result*2.

For step 3., if the CHGDETSTS0 bit is set in step 2., verify that the charger is detected, then clear the VDPSRCE0 and IDMSINKE0 bits, and set the VDMSRCE0 and IDPSINKE0 bits.

For step 4., set the VDMSRCE0 and IDPSINKE0 bits and wait for 40 ms, then use the PDDETSTS0 bit to verify the secondary detection result.

Figure 28.20 shows the process flow.

Note 1. The Battery Charging specification describes two implementation methods for data contact detection (D+/D- line contact check). One method is to detect a change to logic low due to the pull-down resistor of the host device when the D+ and D- lines have made contact with the target, while the D+ line is held at logic high by applying a

28.3.14.2 转移时间表

本节介绍USBFS帧内的传输调度。USBFS发送SOF后，传输按以下顺序执行：

1. 执行定期转账：
   按照管道1 管道2 管道6 管道7 管道8 管道9的顺序搜索管道，然后如果存在可以生成等时或中断传输事务的管道，则生成事务.
2. 为控制转移设置交易：
   DCP被检查，如果设置事务是可能的，它被发送。
3. 批量传输、控制传输数据阶段和控制传输状态阶段的执行：
   管道按照DCP 管道1 管道2 管道3 管道4 管道5的顺序进行搜索，如果存在用于批量传输、控制传输数据阶段或控制转移状态阶段，交易产生。生成事务时，无论来自外围设备的响应是ACK还是NAK，处理都会移至下一个事务管道。如果帧内有时间进行传输，则重复此步骤。

28.3.14.3 启用USB通信

将DVSTCR0.UACT位设置为1启动SOF传输，并启用事务生成。将UACT位设置为0会停止SOF传输并调用挂起状态。如果UACT设置从1更改为0，则在发送下一个SOF后处理停止。

28.3.15 电池充电检测处理

可以控制电池充电规范中定义的数据接触检测（D+线路接触检查）、一次检测（充电器检测）和二次检测（充电器验证）的处理。本节介绍单个功能设备和主机设备所需的操作。

28.3.15.1 设备控制器模式下的处理

将USBFS作为便携式设备进行电池充电时，需要进行以下处理：

1. 检测数据线（D+和D−）何时接触并开始进行初步检测处理。
2. 初级检测开始后，等待40ms进行屏蔽，然后检查Dvoltage电平以确认初级检测结果。
3. 如果在初级检测期间检测到充电器，则启动次级检测。
4. 二次检测开始后，等待40ms屏蔽，然后检查D+电压电平，确认二次检测结果。

对于第1步，在使用VBINT和VBSTS位检测到VBUS后：

1. 等待300到900ms，然后设置USBBCCTRL0寄存器中的VDPSRCE0和IDMSINKE0位。
2. 设置IDPSRCE0位。
3. 使用LNST[1:0]位检测到D+线上从高到低的变化后，清零IDPSRCE0位，并同时设置VDPSRCE0和IDMSINKE0位*1。

对于第2步，设置VDPSRCE0和IDMSINKE0位并等待40ms，然后使用CHGDETSTS0位验证主检测结果*2。

对于第3步，如果在第2步中设置了CHGDETSTS0位，则验证是否检测到充电器，然后清除VDPSRCE0和IDMSINKE0位，并设置VDMSRCE0和IDPSINKE0位。

对于第4步，设置VDMSRCE0和IDPSINKE0位并等待40ms，然后使用PDDETSTS0位验证二次检测结果。

图28.20显示了处理流程。

注1.电池充电规范描述了数据接触检测（D+Dline接触检测）的两种实现方法。一种方法是在D+和D线与目标接触时检测到由于主机设备的下拉电阻而导致的逻辑低电平变化，而D+线通过施加一个保持在逻辑高电平

current of 7 to 13 µA on the D+ line. The other method is to wait for 300 to 900 ms after VBUS is detected.

Note 2. During primary detection, when the voltage on the D- line is detected to be 0.25 to 0.4 V or above and 0.8 to 2.0 V or below, the target device is recognized as the host device for battery charging, that is, charging downstream port. When using a USB transceiver in which the CHGDETSTS0 bit only indicates that the voltage on the D- line is 0.25 to 0.4 V or above, add the processing to check that the voltage on D- line is 0.8 V to 2.0 V or below using the LNST[1:0] bits, as required.

D+线上的电流为7至13μA。另一种方法是在检测到VBUS后等待300到900ms。注2.一次检测时，检测到Dline上的电压为0.25至0.4V或以上和0.8至2.0

V或以下，目标设备被识别为主机设备进行电池充电，即充电下游端口。当使用CHGDETSTS0位仅指示Dline上的电压为0.25至0.4V或以上的USB收发器时，使用LNST[1添加处理以检查Dline上的电压是否为0.8V至2.0V或以下：0]位，根据需要。

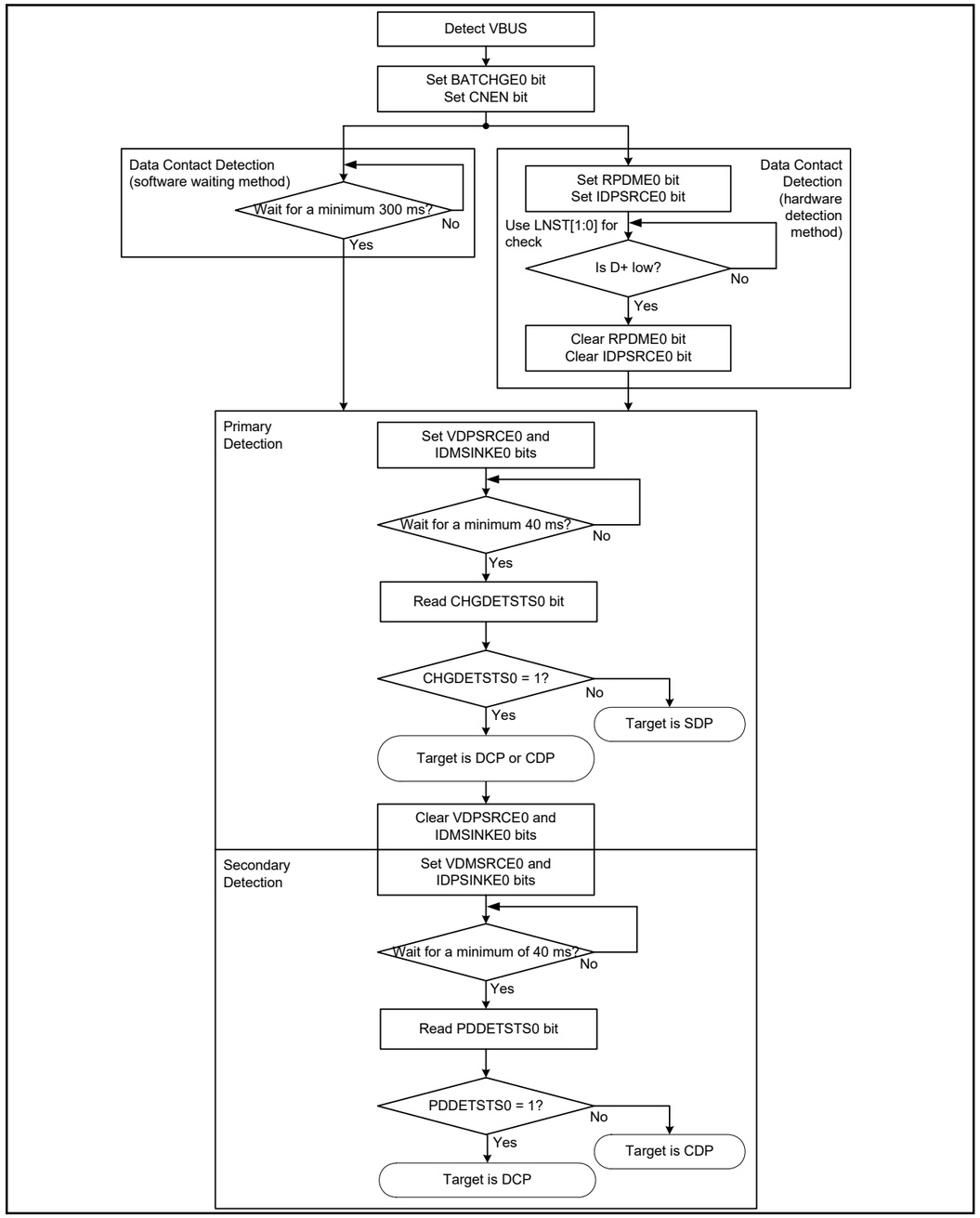


Figure 28.20 Process flow for operating as portable device

28.3.15.2 Processing when host controller is selected

The following processing is required when operating the USBFS as a charging downstream port for battery charging:

1. Start driving the VBUS.

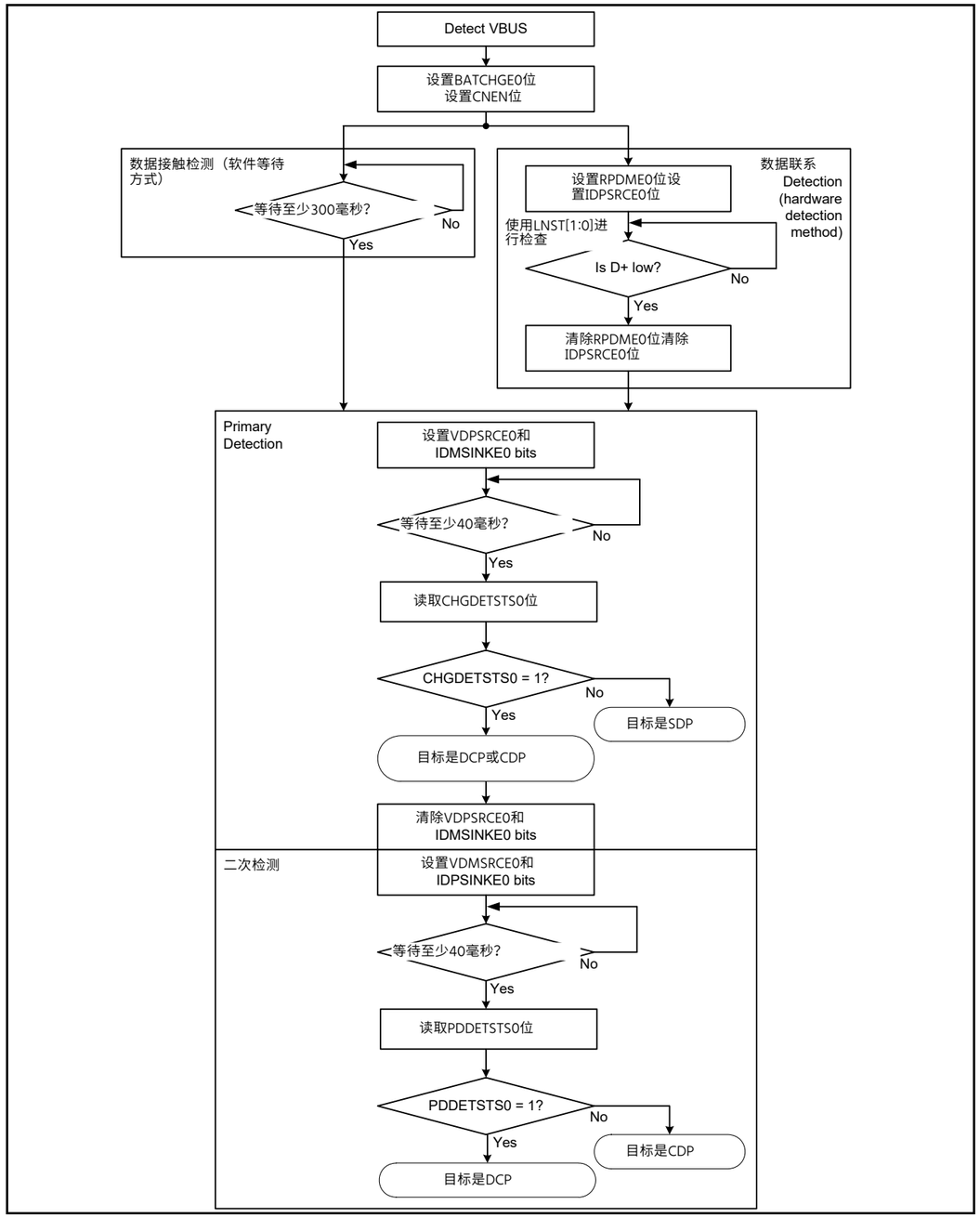


Figure 28.20 作为便携式设备操作的工艺流程

28.3.15.2 选择主机控制器时的处理

将USBFS作为充电下行端口进行电池充电时，需要进行以下处理：

1. 开始驱动VBUS。

2. Enable the portable device detection circuit.
3. Monitor the portable device detection signal, and start driving the D- line if the detection signal is high.
4. Detect when the portable device detection signal is a low level and stop driving the D- line.

The following processing can also be used in associated with the battery charging specification:

a. After disconnection is detected, start driving the D- line within 200 ms

b. After connection is detected, stop driving the D- line within 10 ms.

The D- line must be driven to allow the portable device to detect the primary detection described in section 28.3.15.1, Processing in device controller mode. Steps 1. to 4. apply when the portable device detection function is provided by hardware. This method is to drive the D- line when the portable device is detected.

Steps a. and b. apply when the portable device function is not provided or available by hardware. Regardless of detection of the portable device, the D- line is driven in the disconnected state and not in the connected state. In the battery charging specification, either of these methods can be used.

For steps 3. and 4., after a change in the portable device detection signal is detected using the PDDETINT interrupt, the current signal state can be confirmed by reading the PDDETSTS0 bit. Steps a and b can be performed only in a software timer.

2. 启用便携式设备检测电路。
3. 监测便携设备检测信号，如果检测信号为高，则开始驱动Dline。
4. 检测便携设备检测信号何时为低电平，停止驱动Dline。

以下处理也可用于与电池充电规范相关联：

一个。检测到断线后，200ms内开始驱动Dline

湾。检测到连接后，请在10ms内停止驱动Dline。

必须驱动Dline以允许便携式设备检测第28.3.15.1节"设备控制器模式下的处理"中描述的主要检测。当便携式设备检测功能由硬件提供时，应用步骤1.至4.。此方法是在检测到便携式设备时驱动Dline。

步骤一。和b。当便携式设备功能不由硬件提供或不可用时适用。无论是否检测到便携式设备，Dline都在断开状态而不是连接状态下驱动。在电池充电规范中，可以使用这两种方法中的任何一种。

对于步骤3.和4.，在使用PDDETINT中断检测到便携式设备检测信号的变化后，可以通过读取PDDETSTS0位来确认当前信号状态。步骤a和b只能在软件定时器中执行。

Figure 28.21 show the process flow for steps 1 to 4 and the process flow for steps a to b, respectively.

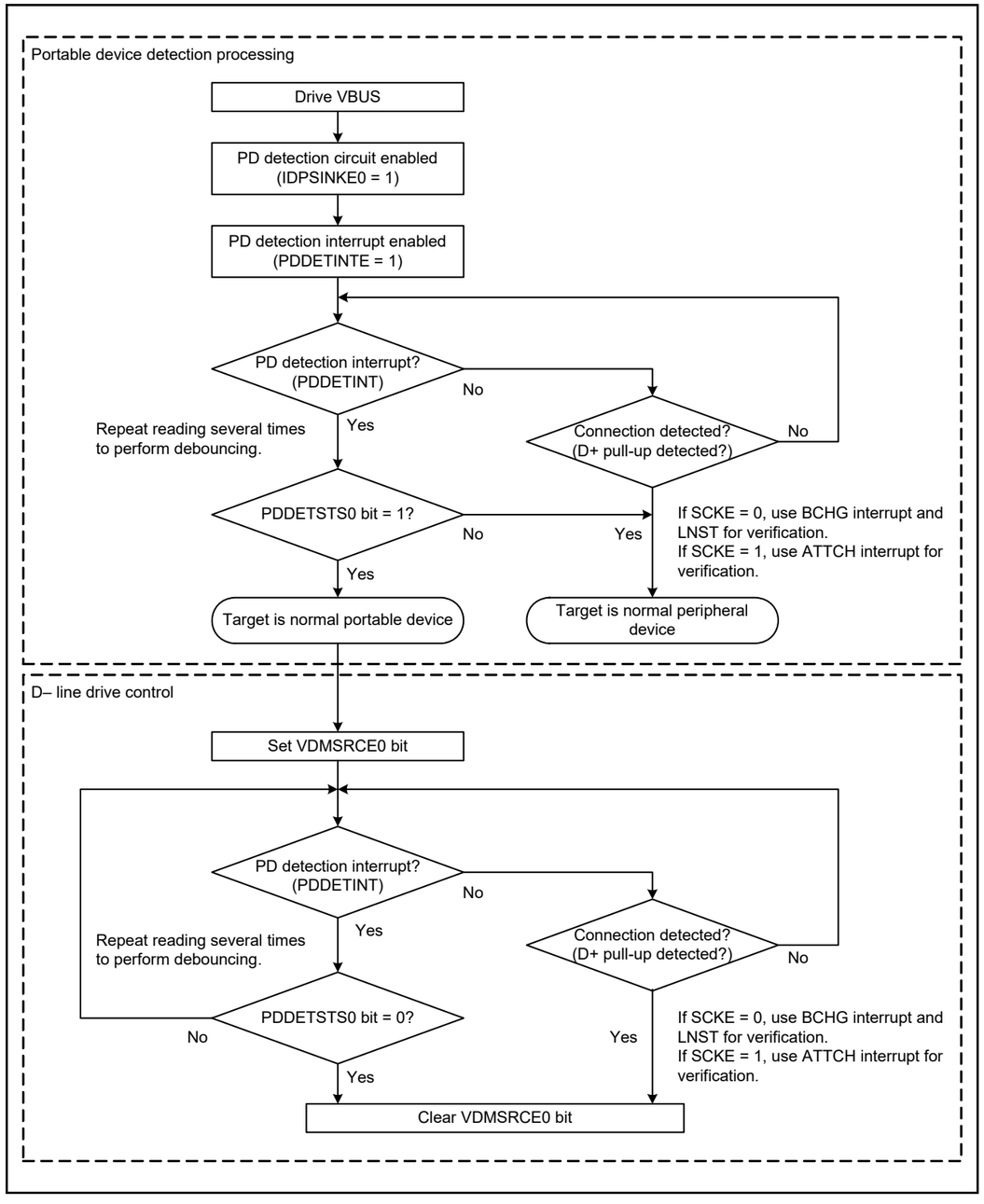


Figure 28.21 Process flow for operating as charging downstream port (steps 1 to 4)

图28.21分别显示了步骤1到4的处理流程和步骤a到b的处理流程。

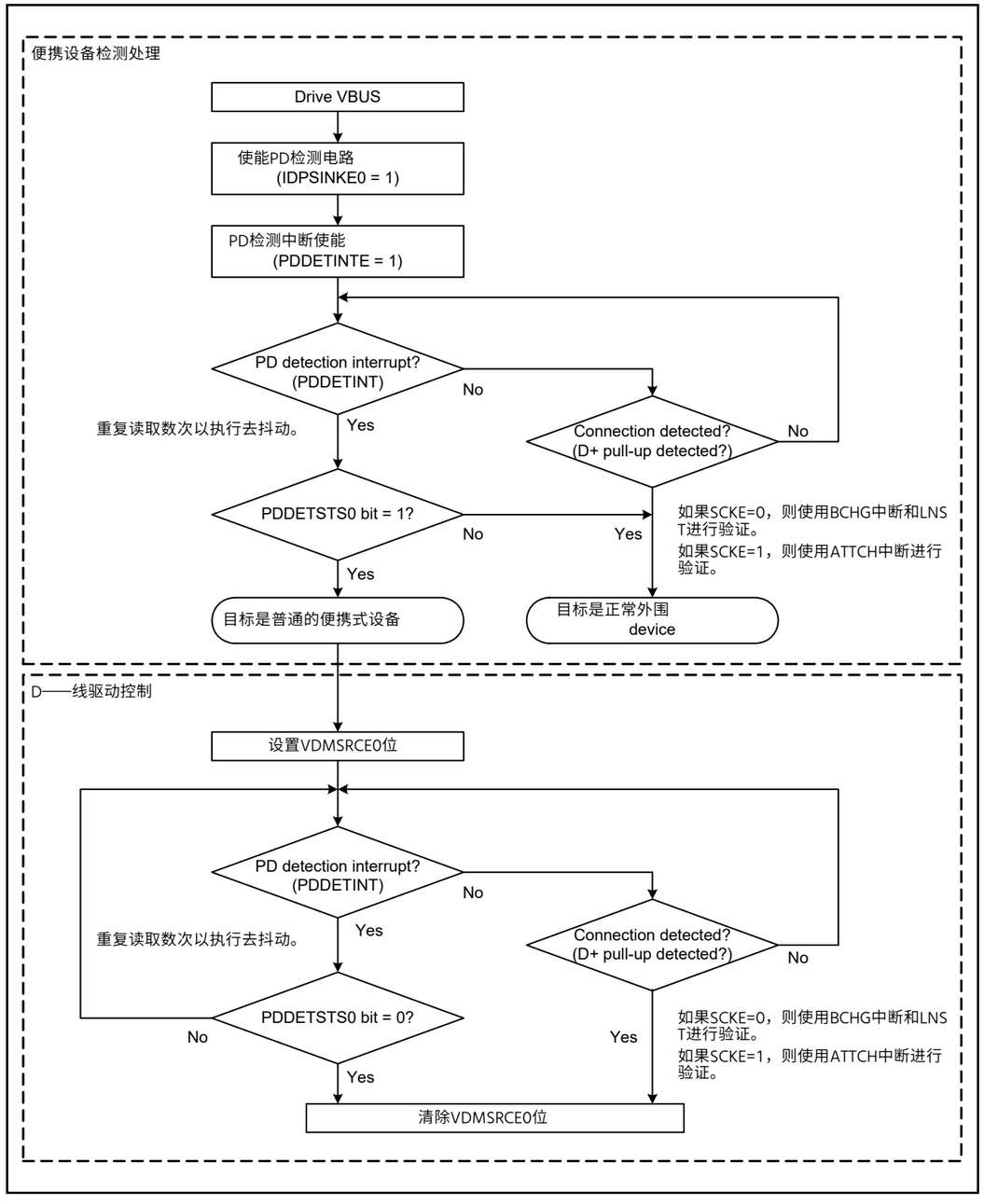


Figure 28.21 作为充电下游端口操作的工艺流程（步骤1至4）

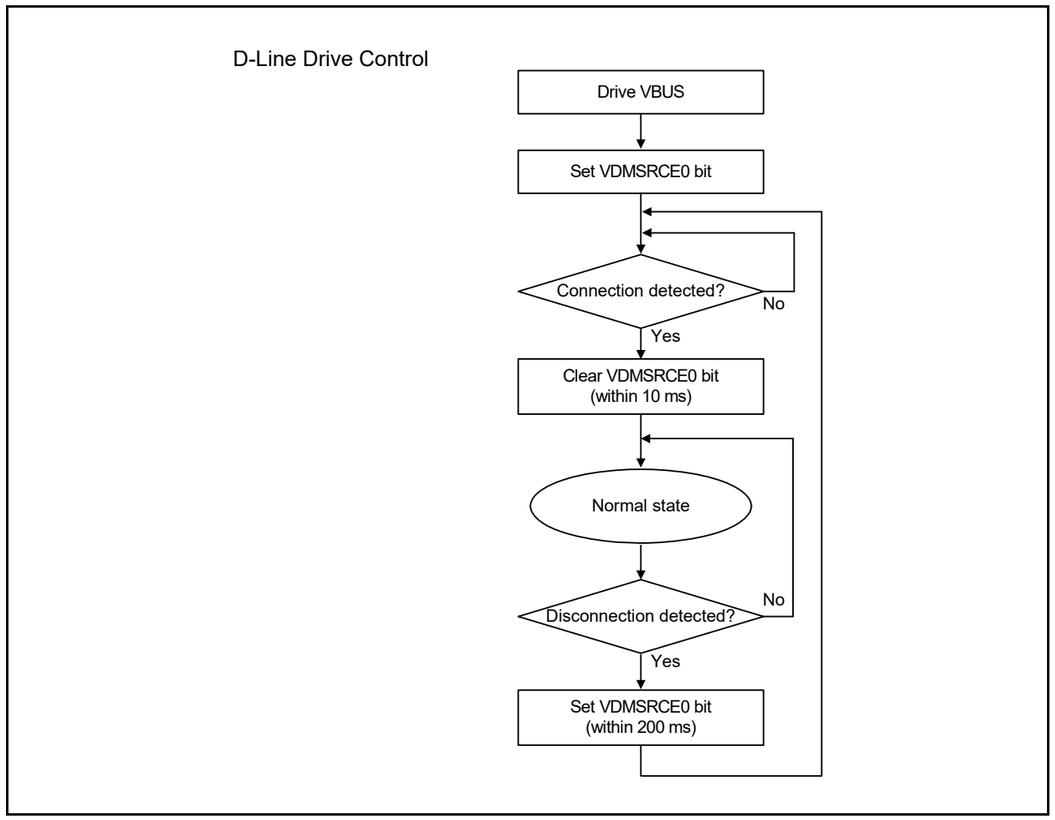


Figure 28.22 Process flow for operating as charging downstream port (steps a to b)

28.4 Usage Notes

28.4.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable USBFS operation. The USBFS is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

28.4.2 Clearing the Interrupt Status Register on Exiting Software Standby Mode

Because the input buffer is always enabled in Software Standby mode, an unexpected interrupt might occur under the following conditions:

- When the interrupt is enabled in Normal mode
- When the interrupt is disabled in Software Standby mode
- When the input level of the pin that cancels software standby is changed in Software Standby mode.

These conditions might cause the associated interrupt flag in the Interrupt Status Register to set unexpectedly. After the MCU exits Software Standby mode, the unexpected interrupt might be sent to the interrupt controller. To avoid this, always clear the INTSTS0 and INTSTS1 registers in the canceling sequence.

28.4.3 Clearing the Interrupt Status Register after Setting Up the Port Function

The input buffer is disabled before the PmnPFS.PSEL and PmnPFS.PMR port is set up, so the internal signal is fixed high or low. The input buffer is enabled after setting the ports so that the external pin state is propagated to the MCU. An

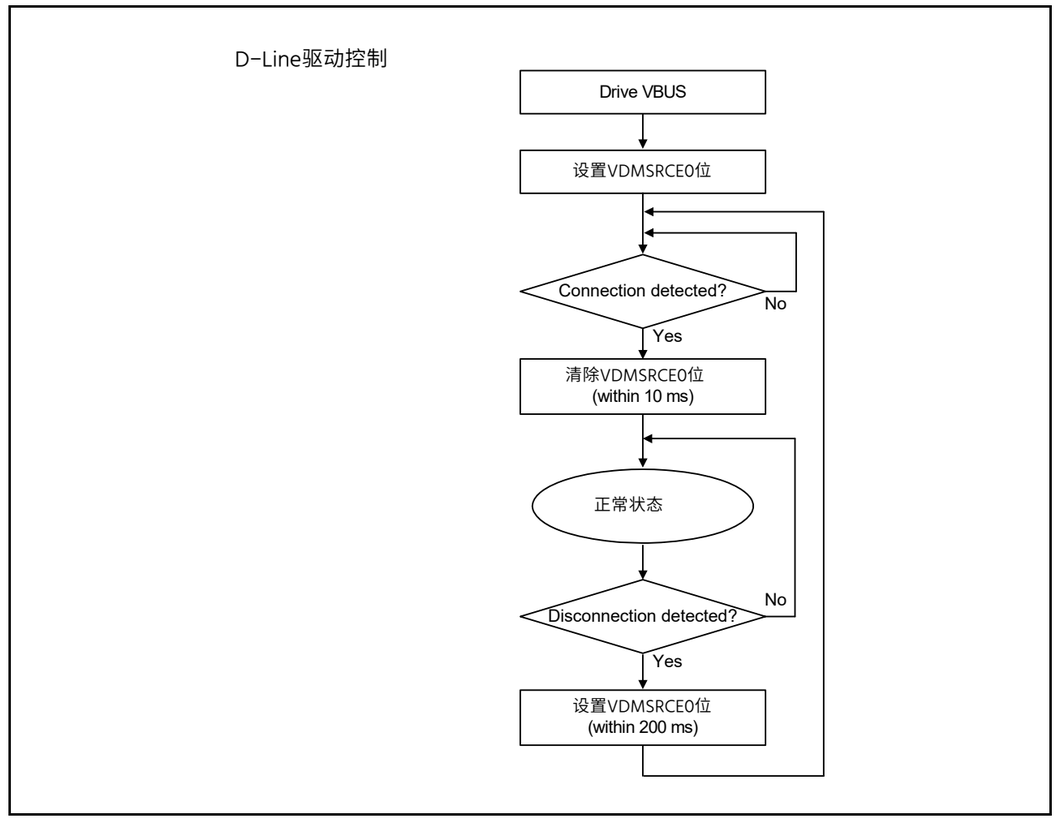


Figure 28.22 作为充电下游端口操作的工艺流程（步骤a到b）

28.4 使用说明

28.4.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用USBFS操作。USBFS在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

28.4.2 退出软件待机模式时清除中断状态寄存器

由于在软件待机模式下始终启用输入缓冲区，因此在以下情况下可能会发生意外中断：

- 在正常模式下启用中断时
- 在软件待机模式下禁用中断时
- 当取消软件待机的引脚的输入电平在软件待机模式下发生变化时。

这些情况可能会导致中断状态寄存器中的相关中断标志意外设置。之后MCU退出软件待机模式，意外中断可能被发送到中断控制器。为避免这种情况，请始终在取消序列中清除INTSTS0和INTSTS1寄存器。

28.4.3 设置端口功能后清除中断状态寄存器

在设置PmnPFS.PSEL和PmnPFS.PMR端口之前，输入缓冲器被禁用，因此内部信号固定为高电平或低电平。设置端口后启用输入缓冲器，以便将外部引脚状态传播到MCU。一个

unexpected interrupt might occur at this time, causing the VBINT and OVRCR bits in INTSTS0 and INTSTS1, or other interrupt status flags to set to 1. To avoid a malfunction, always clear the INTSTS0 and INTSTS1 registers after setting up the ports.

此时可能会发生意外中断，导致INTSTS0和INTSTS1中的VBINT和OVRCR位或其他中断状态标志设置为1。为避免故障，请务必在设置端口后清除INTSTS0和INTSTS1寄存器。

29. Serial Communications Interface (SCI)

29.1 Overview

The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface.

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI channel has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

Table 29.1 lists the SCI specifications, Figure 29.1 shows a block diagram, and Table 29.2 lists the I/O pins by mode.

Note: In this section, PCLK refers to PCLKA.

Table 29.1 SCI specifications (1 of 2)

Parameter	Description
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple IIC • Simple SPI.
Transfer speed	Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications	Transmitter: Continuous transmission possible using double-buffering structure Receiver: Continuous reception possible using double-buffering structure
I/O pins	See Table 29.2.
Data transfer	Selectable as LSB-first or MSB-first transfer
Interrupt sources	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and address match Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode)
Module-stop function	Module-stop state can be set for each channel
Snooze end request	SCI0 address mismatch (SCI0_DCUF)

29. 串行通信接口(SCI)

29.1 Overview

串行通信接口(SCI)可配置为五个异步和同步串行接口：

- 异步接口（UART和异步通信接口适配器(ACIA)）
- 8位时钟同步接口
- Simple IIC (master-only)
- 简单的SPI
- 智能卡接口。

智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。
每个SCI通道都有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。

表29.1列出了SCI规范，图29.1显示了框图，表29.2列出了按模式划分的IO引脚。

Note: 在本节中，PCLK指的是PCLKA。

Table 29.1 SCI规范(1of2)

Parameter	Description
串行通信模式	异步 时钟同步 智能卡接口 简单IIC 简单SPI。
传输速度	可通过片上波特率发生器指定比特率
Full-duplex communications	发送器：使用双缓冲结构可以连续发送接收器：使用双缓冲结构可以连续接收
I/O pins	见表29.2。
数据传输	可选择LSB优先或MSB优先传输
中断源	发送结束、发送数据空、接收数据满、接收错误、接收数据就绪、地址匹配开始条件、重启条件或停止条件的生成完成（对于简单IIC模式）
Module-stop function	每个通道可设置模块停止状态
暂停结束请求	SCI0地址不匹配(SCI0_DCUF)

Table 29.1 SCI specifications (2 of 2)

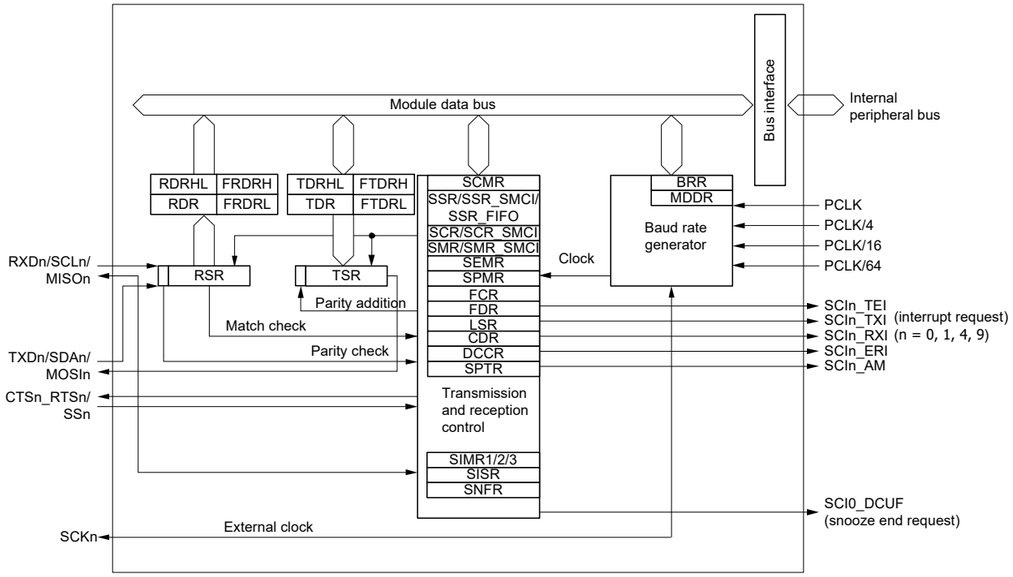
Parameter		Description
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission/Reception	Selectable to 1-stage register or 16-stage FIFO (only SCI0 and SCI1 support FIFO)
	Address match	Interrupt request/event output can be issued on detecting a match between the received data and the value in the compare match register
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued on detecting a mismatch between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by reading from SPTR register
	Clock source	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled between multiple processors
	Noise cancellation	Digital noise filters included on the signal paths from RXDn pin inputs
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission/Reception	Selectable to 1-stage register or 16-stage FIFO
Smart card interface mode	Error processing	Error signal can be automatically transmitted on detecting a parity error during reception
		Data can be automatically retransmitted on receiving an error signal during transmission
	Data type	Both direct and inverse convention are supported
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Detection of errors	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	SS input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high
	Clock settings	Configurable between four clock phase and clock polarity settings
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output (SCIn_ERI*1) for receive error or error signal detection
		Receive data full event output (SCIn_RXI*1, *2)
		Transmit data empty event output (SCIn_TXI*1, *2)
		Transmit end event output (SCIn_TEI*1, *2)
		Address match event output (SCIn_AM*1)

Note 1. Channel number (n = 0, 1, 4, 9).
Note 2. Using this event link function is prohibited when the FIFO operation is selected in asynchronous mode.

Table 29.1 SCI规范（2个中的2个）

Parameter		Description
异步模式	数据长度	7、8或9位
	传输停止位	1或2位
	Parity	偶校验、奇校验或无校验
	接收错误检测	奇偶校验、溢出和成帧错误
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	Transmission/Reception	可选择1级寄存器或16级FIFO（仅SCI0和SCI1支持FIFO）
	地址匹配	检测到接收数据与比较匹配寄存器中的值匹配时，可发出中断请求事件输出
	地址不匹配（仅SCI0）接收数据	检测到接收到的数据与比较匹配寄存器中的值不匹配时，可以发出贪睡结束请求
	Start-bit detection	可选择低电平或下降沿检测
	断线检测	通过从SPTR寄存器读取可检测到的帧错误中断
	时钟源	可选择内部或外部时钟
	Double-speed mode	波特率发生器双速模式可选
	多处理器通讯功能	在多个处理器之间启用串行通信
	噪音消除	RXDn引脚输入的信号路径上包含数字噪声滤波器
时钟同步模式	数据长度	8 bits
	接收错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	Transmission/Reception	可选择1级寄存器或16级FIFO
智能卡接口方式	错误处理	在接收过程中检测到奇偶校验错误时可以自动发送错误信号
		传输过程中接收到错误信号可自动重传数据
	数据类型	支持直接和反向约定
简单IIC模式	传输格式	I2C总线格式（仅MSB优先）
	操作模式	主机（仅限单主机操作）
	传输率	高达400kbps
	噪音消除	来自SCLn和SDAn引脚输入的信号路径包含数字噪声滤波器，并提供可调节的噪声消除间隔
简单SPI模式	数据长度	8 bits
	错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	SS输入引脚功能	通过将SSn引脚驱动为高电平，可以在输出引脚上调用高阻抗状态
	时钟设置	可在四个时钟相位和时钟极性设置之间进行配置
比特率调制功能		通过校正片上波特率发生器的输出来减少错误
事件链接功能		错误事件输出(SCIn_ERI*1)用于接收错误或错误信号检测
		接收数据满事件输出（SCIn_RXI*1 *2）
		发送数据空事件输出（SCIn_TXI*1 *2）
		发送结束事件输出(SCIn_TEI*1 *2)
		地址匹配事件输出(SCIn_AM*1)

Note 1. 通道号（n=0、1、4、9）。
Note 2. 在异步模式下选择FIFO操作时，禁止使用此事件链接功能。



RSR: Receive Shift Register
RDR: Receive Data Register
TSR: Transmit Shift Register
TDR: Transmit Data Register
SMR/SMR_SMCI:Serial Mode Register
SCR/SCR_SMCI:Serial Control Register
SSR/SSR_SMCI/SSR_FIFO*1:Serial Status Register
SCMR: Smart Card Mode Register
BRR: Bit Rate Register
MDDR: Modulation Duty Register
SEMR: Serial Extended Mode Register
SPMR: SPI Mode Register
SNFR: Noise Filter Setting Register
SIMR1/2/3: I2C Mode Register 1/2/3
SISR: I2C Status Register

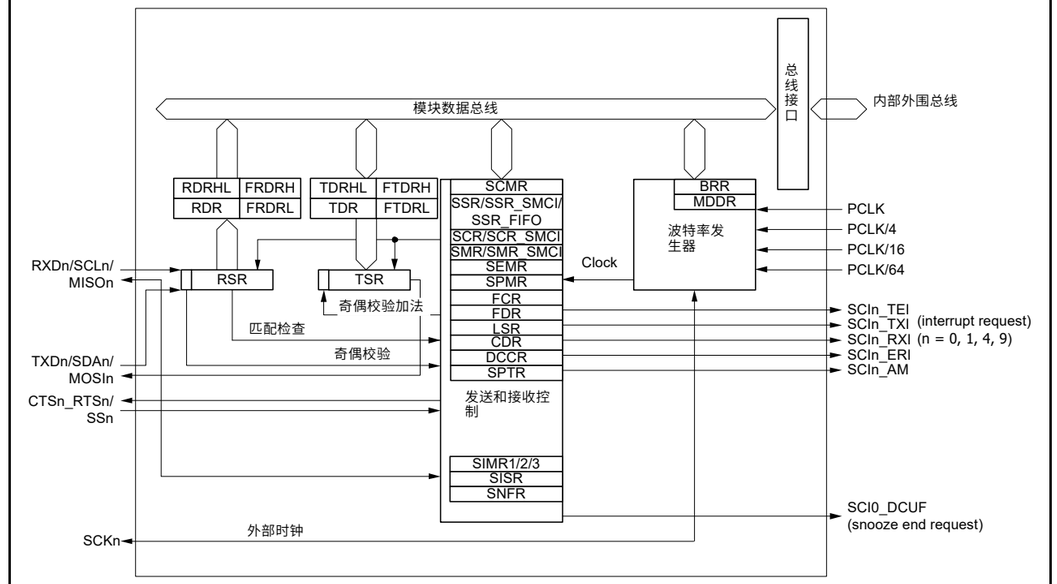
RDRHL: Receive 9-bit Data Register
FRDRH/L*1: Receive FIFO Data Register
TDRHL: Transmit 9-bit Data Register
FTDRH/L*1: Transmit FIFO Data Register
FCR*1: FIFO Control Register
FDR*1: FIFO Data Count Register
LSR*1: Line Status Register
CDR: Compare Match Data Register
DCCR: Data Compare Match Control Register
SPTR: Serial Port Register

Note 1. SCI0 and SCI1 only

Figure 29.1 SCI block diagram

Table 29.2 SCI I/O pins (1 of 2)

Channel	Pin name	Input/Output	Function
SCI0	SCK0	Input/Output	SCI0 clock input/output
	RXD0/SCL0/ MISO0	Input/Output	SCI0 receive data input SCI0 I2C clock input/output SCI0 slave transmit data input/output
	TXD0/SDA0/ MOSI0	Input/Output	SCI0 transmit data output SCI0 I2C data input/output SCI0 master transmit data input/output
	SS0/CTS0_RTS0	Input/Output	SCI0 chip select input, active-low SCI0 transfer start control input/output, active-low



RSR: 接收移位寄存器
RDR: 接收数据寄存器
TSR: 发送移位寄存器
TDR: 发送数据寄存器
SMRSMR_SMCI：串行模式寄存器SCRSC R_SMCI：串行控制寄存器
SSRSSR_SMCISSR_FIFO*1：串行状态寄存器
SCMR: 智能卡模式寄存器
BRR: 比特率寄存器
MDDR: 调制占空比寄存器
SEMR: 串行扩展模式寄存器
SPMR: SPI模式寄存器
SNFR: 噪声滤波器设置寄存器
SIMR1/2/3: I2C模式寄存器123
SISR: 我2C状态寄存器

RDRHL: 接收9位数据寄存器
FRDRHL*1：接收FIFO数据寄存器
TDRHL: 发送9位数据寄存器
FTDRHL*1：发送FIFO数据寄存器
FCR*1: 先进先出控制寄存器
FDR*1: FIFO数据计数寄存器
LSR*1: 线路状态寄存器
CDR: 比较匹配数据寄存器
DCCR: 数据比较匹配控制寄存器
SPTR: 串口寄存器

Note 1. 仅限SCI0和SCI1

Figure 29.1 SCI框图

Table 29.2 SCIIO引脚（2个中的1个）

Channel	引脚名称	Input/Output	Function
SCI0	SCK0	Input/Output	SCI0 clock input/output
	RXD0/SCL0/ MISO0	Input/Output	SCI0接收数据输入 SCI0 I2C clock input/output SCI0从机发送数据输入输出
	TXD0/SDA0/ MOSI0	Input/Output	SCI0发送数据输出SCI0I2C 数据输入输出 SCI0主机发送数据输入输出
	SS0/CTS0_RTS0	Input/Output	SCI0片选输入，低电平有效 SCI0传输开始控制输入输出，低电平有效

Table 29.2 SCI I/O pins (2 of 2)

Channel	Pin name	Input/Output	Function
SCI1	SCK1	Input/Output	SCI1 clock input/output
	RXD1/SCL1/ MISO1	Input/Output	SCI1 receive data input SCI1 I2C clock input/output SCI1 slave transmit data input/output
	TXD1/SDA1/ MOSI1	Input/Output	SCI1 transmit data output SCI1 I2C data input/output SCI1 master transmit data input/output
	SS1/CTS1_RTS1	Input/Output	SCI1 chip select input, active-low SCI1 transfer start control input/output, active-low
SCI4	SCK4	Input/Output	SCI4 clock input/output
	RXD4/SCL4/ MISO4	Input/Output	SCI4 receive data input SCI4 I2C clock input/output SCI4 slave transmit data input/output
	TXD4/SDA4/ MOSI4	Input/Output	SCI4 transmit data output SCI4 I2C data input/output SCI4 master transmit data input/output
	SS4/CTS4_RTS4	Input/Output	SCI4 chip select input, active-low SCI4 transfer start control input/output, active-low
SCI9	SCK9	Input/Output	SCI9 clock input/output
	RXD9/SCL9/ MISO9	Input/Output	SCI9 receive data input SCI9 I2C clock input/output SCI9 slave transmit data input/output
	TXD9/SDA9/ MOSI9	Input/Output	SCI9 transmit data output SCI9 I2C data input/output SCI9 master transmit data input/output
	SS9/CTS9_RTS9	Input/Output	SCI9 chip select input, active-low SCI9 transfer start control input/output, active-low

29.2 Register Descriptions

29.2.1 Receive Shift Register (RSR)

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, the data is automatically transferred to the RDR, RDRHL, or the receive FIFO register. The RSR register cannot be directly accessed by the CPU.

29.2.2 Receive Data Register (RDR)

Address(es): SCI0.RDR 4007 0005h, SCI1.RDR 4007 0025h, SCI4.RDR 4007 0085h, SCI9.RDR 4007 0125h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores receive data. When one frame of serial data is received, it is transferred from RSR to RDR, and the RSR register can receive more data. Because RSR and RDR function as a double buffer, continuous received operations can be performed.

Read the RDR register only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next frame of data is received before reading the received data from the RDR register, an overrun error occurs. The CPU cannot write to the RDR.

Table 29.2 SCIIO引脚（2个中的2个）

Channel	引脚名称	Input/Output	Function
SCI1	SCK1	Input/Output	SCI1 clock input/output
	RXD1/SCL1/ MISO1	Input/Output	SCI1接收数据输入 SCI1 I2C clock input/output SCI1从机发送数据输入输出
	TXD1/SDA1/ MOSI1	Input/Output	SCI1发送数据输出SCI1I2C 数据输入输出 SCI1主机发送数据输入输出
	SS1/CTS1_RTS1	Input/Output	SCI1片选输入，低电平有效 SCI1传输开始控制输入输出，低电平有效
SCI4	SCK4	Input/Output	SCI4 clock input/output
	RXD4/SCL4/ MISO4	Input/Output	SCI4接收数据输入 SCI4 I2C clock input/output SCI4从机发送数据输入输出
	TXD4/SDA4/ MOSI4	Input/Output	SCI4发送数据输出SCI4I2C 数据输入输出 SCI4主机发送数据输入输出
	SS4/CTS4_RTS4	Input/Output	SCI4片选输入，低电平有效 SCI4传输开始控制输入输出，低电平有效
SCI9	SCK9	Input/Output	SCI9 clock input/output
	RXD9/SCL9/ MISO9	Input/Output	SCI9接收数据输入 SCI9 I2C clock input/output SCI9从机发送数据输入输出
	TXD9/SDA9/ MOSI9	Input/Output	SCI9发送数据输出SCI9I2C 数据输入输出 SCI9主机发送数据输入输出
	SS9/CTS9_RTS9	Input/Output	SCI9片选输入，低电平有效 SCI9传输启动控制输入输出，低电平有效

29.2 注册说明

29.2.1 接收移位寄存器(RSR)

RSR是一个移位寄存器，它接收从RXDn引脚输入的串行数据并将其转换为并行数据。当接收到一帧数据时，数据会自动传输到RDR、RDRHL或接收FIFO寄存器。CPU不能直接访问RSR寄存器。

29.2.2 接收数据寄存器(RDR)

Address(es): SCI0.RDR 4007 0005h, SCI1.RDR 4007 0025h, SCI4.RDR 4007 0085h, SCI9.RDR 4007 0125h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0

RDR是一个8位寄存器，用于存储接收数据。当接收到一帧串行数据时，将其从RSR传输到RDR，而RSR寄存器可以接收更多的数据。由于RSR和RDR用作双缓冲器，因此可以执行连续接收操作。

在接收数据完全中断(SCIn_RXI)发生后，仅读取一次RDR寄存器。

Note: 如果在从RDR寄存器读取接收数据之前接收到下一帧数据，则会发生溢出错误。CPU无法写入RDR。

29.2.3 Receive 9-bit Data Register (RDRHL)

Address(es): SCI0.RDRHL 4007 0010h, SCI1.RDRHL 4007 0030h, SCI4.RDRHL 4007 0090h, SCI9.RDRHL 4007 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDRHL is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are the shadow register of RDR, so access to RDRHL affects RDR. Access to RDRHL is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from RSR to the RDR/RDRHL registers, allowing RSR register to receive more data.

RSR and RDRHL form a double-buffered structure to enable continuous reception. RDRHL should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL. The CPU cannot write to the RDRHL register.

Bits [15:9] of the RDRHL register are fixed to 0. These bits are read as 0. The write value should be 0.

29.2.4 Receive FIFO Data Register H, L, HL (FRDRH, FRDRL, FRDRHL)

Receive FIFO Data Register H (FRDRH)

Address(es): SCI0.FRDRH 4007 0010h, SCI1.FRDRH 4007 0030h

Receive FIFO Data Register L (FRDRL)

Address(es): SCI0.FRDRL 4007 0011h, SCI1.FRDRL 4007 0031h

Receive FIFO Data Register HL (FRDRHL)

Address(es): SCI0.FRDRHL 4007 0010h, SCI1.FRDRHL 4007 0030h

	SCIn.FRDRHL															
	SCIn.FRDRH								SCIn.FRDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	RDAT[8:0]	Serial Receive Data	Received serial data, valid only in asynchronous mode, including multi-processor or clock synchronous mode, and with FIFO selected	R
b9	MPB	Multi-Processor Bit Flag	Multi-processor bit associated with serial receive data (RDAT[8:0]): 0: Data transmission cycle 1: ID transmission cycle. MPB is valid only in asynchronous mode with SMR.MP = 1 and FIFO selected.	R
b10	DR	Receive Data Ready Flag	0: Receiving is in progress, or no received data remains in FRDRH and FRDRL after a normal completion of received data 1: Next receive data is not received for a period after a normal completion of received data.	R*1

29.2.3 接收9位数据寄存器(RDRHL)

Address(es): SCI0.RDRHL 4007 0010h, SCI1.RDRHL 4007 0030h, SCI4.RDRHL 4007 0090h, SCI9.RDRHL 4007 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDRHL是一个16位寄存器，用于存储接收到的数据。选择异步模式和9位数据长度时，请使用此寄存器。

RDRHL的低8位是RDR的影子寄存器，所以访问RDRHL会影响RDR。如果选择7位或8位数据长度，则禁止访问RDRHL。

接收到一帧数据后，接收到的数据从RSR传送到RDRRDRHL寄存器，允许
RSR寄存器接收更多数据。

RSR和RDRHL形成一个双缓冲结构以实现连续接收。只有在发出接收数据完全中断(SCIn_RXI)请求时才应读取RDRHL。在从RDRHL读取接收到的数据之前接收到下一帧数据时，会发生溢出错误。CPU无法写入RDRHL寄存器。

RDRHL寄存器的位[15:9]固定为0。这些位被读取为0。写入值应为0。

29.2.4 接收FIFO数据寄存器H L HL(FRDRH FRDRL FRDRHL)

接收FIFO数据寄存器H(FRDRH)

Address(es): SCI0.FRDRH 4007 0010h, SCI1.FRDRH 4007 0030h

接收FIFO数据寄存器L(FRRDL)

Address(es): SCI0.FRDRL 4007 0011h, SCI1.FRDRL 4007 0031h

接收FIFO数据寄存器HL(FRDRHL)

Address(es): SCI0.FRDRHL 4007 0010h, SCI1.FRDRHL 4007 0030h

	SCIn.FRDRHL															
	SCIn.FRDRH								SCIn.FRDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	RDAT[8:0]	串行接收数据	接收到的串行数据，仅在异步模式下有效，包括多处理器或时钟同步模式，并选择FIFO	R
b9	MPB	多处理器位标志	与串行接收数据相关的多处理器位（RDAT[8:0]）：0：数据传输周期1：ID传输周期。MPB仅在SMR.MP=1且异步模式下有效 FIFO selected.	R
b10	DR	接收数据就绪标志	0：接收中，或接收数据正常完成后FRRDH和FRRDL中没有接收数据1：接收数据正常完成后一段时间内没有接收到下一个接收数据。	R*1

Bit	Symbol	Bit name	Description	R/W
b11	PER	Parity Error Flag	0: No parity error occurred in the first data of FRDRH and FRDRL 1: A parity error occurred in the first data of FRDRH and FRDRL.	R
b12	FER	Framing Error Flag	0: No framing error occurred in the first data of FRDRH and FRDRL 1: A framing error occurred in the first data of FRDRH and FRDRL.	R
b13	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error occurred.	R*1
b14	RDF	Receive FIFO Data Full Flag	0: The amount of received data written in FRDRH and FRDRL is below the specified received triggering number 1: The amount of received data written in FRDRH and FRDRL is equal to or greater than the specified received triggering number.	R*1
b15	—	Reserved	This bit is read as 0	R

Note 1. If this flag is read, it is same as a read from the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of FRDRL and FRDRH.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information. This register is valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode.

The SCI completes reception of one frame of serial data by transferring the received data from the RSR register into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full, subsequent serial receive data is lost. The CPU can read from FRDRH and FRDRL but cannot write to them.

Reading 1 from the RDF, ORER, or DR flags of the FRDRH register is the same as reading those bits from the SSR_FIFO register. When writing 0 to clear a flag in the SSR_FIFO register after reading the FRDRH register, write 0 only to the flag that is to be cleared and write 1 to the other flags.

When reading both the FRDRH and FRDRL registers, read in order from FRDRH to FRDRL. The FRDRHL register can be accessed in 16-bit units.

29.2.5 Transmit Data Register (TDR)

Address(es): SCI0.TDR 4007 0003h, SCI1.TDR 4007 0023h, SCI4.TDR 4007 0083h, SCI9.TDR 4007 0123h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TDR is an 8-bit register that stores transmit data.

When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission.

The double-buffered structure of TDR and TSR enables continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to TSR to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

Bit	Symbol	位名称	Description	R/W
b11	PER	奇偶校验错误标志	0：FRRDH和FRDRL的第一个数据没有发生奇偶校验错误1：FRRDH和FRDRL的第一个数据发生了奇偶校验错误。	R
b12	FER	成帧错误标志	0：FRRDH和FRDRL的第一个数据没有发生帧错误1：FRRDH和FRDRL的第一个数据发生了帧错误。	R
b13	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R*1
b14	RDF	接收FIFO数据满标志	0：写入FRDRH和FRDRL的接收数据量小于指定的接收触发数1：写入FRDRH和FRDRL的接收数据量等于或大于指定的接收触发数。	R*1
b15	—	Reserved	该位读为0	R

Note 1. 如果读取该标志，则与从SSR_FIFO寄存器读取相同。将0写入SSR_FIFO寄存器以清除标志。

FRDRHL是一个16位的寄存器，由FRDRL和FRDRH组成。

FRDRH和FRDRL构成一个16级的FIFO寄存器，用于存储串行接收数据和相关的状态信息。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

SCI通过将接收到的数据从RSR寄存器传送到FRDRH和FRDRL用于存储。执行连续接收，直到存储16个阶段。如果在FRDRH和FRDRL中没有接收到数据时读取数据，则该值未定义。当FRDRH和FRDRL已满时，后续的串行接收数据会丢失。CPU可以从FRDRH和FRDRL读取，但不能写入它们。

从FRDRH寄存器的RDF、ORER或DR标志读取1与从SSR_FIFO寄存器。在读取FRDRH寄存器后写入0以清除SSR_FIFO寄存器中的标志时，仅将0写入要清除的标志，将1写入其他标志。

读取FRDRH和FRDRL寄存器时，按从FRDRH到FRDRL的顺序读取。FRDRHL寄存器可以以16位为单位进行访问。

29.2.5 发送数据寄存器(TDR)

Address(es): SCI0.TDR 4007 0003h, SCI1.TDR 4007 0023h, SCI4.TDR 4007 0083h, SCI9.TDR 4007 0123h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

TDR是一个8位寄存器，用于存储发送数据。

当SCI检测到TSR为空时，它将写入TDR的发送数据传送到TSR并开始发送。

TDR和TSR的双缓冲结构可实现连续串行传输。如果在发送一帧数据时，下一个发送数据已经写入TDR，则SCI将写入的数据传输到TSR继续发送。

CPU可以随时读取或写入TDR。每次发送数据空中断(SCIn_TXI)后，仅将发送数据写入TDR一次。

29.2.6 Transmit 9-Bit Data Register (TDRHL)

Address(es): SCI0.TDRHL 4007 000Eh, SCI1.TDRHL 4007 002Eh, SCI4.TDRHL 4007 008Eh, SCI9.TDRHL 4007 012Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDRHL is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are the shadow register of TDR, so access to TDRHL affects TDR. Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in TSR, the transmit data stored in TDRHL is transferred to TSR and transmission starts.

TSR and TDRHL have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation continues by transferring the data to TSR.

The CPU can read and write to TDRHL. Bits [15:9] in TDRHL are fixed to 1. These bits are read as 1. The write value should be 1.

Write transmit data to TDRHL only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

29.2.7 Transmit FIFO Data Register H, L, HL (FTDRH, FTDRL, FTDRHL)

Transmit FIFO Data Register H (FTDRH)

Address(es): SCI0.FTDRH 4007 000Eh, SCI1.FTDRH 4007 002Eh

Transmit FIFO Data Register L (FTDRL)

Address(es): SCI0.FTDRL 4007 000Fh, SCI1.FTDRL 4007 002Fh

Transmit FIFO Data Register HL (FTDRHL)

Address(es): SCI0.FTDRHL 4007 000Eh, SCI1.FTDRHL 4007 002Eh

	SCIn.FTDRHL															
	SCIn.FTDRH								SCIn.FTDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b8 to b0	TDAT[8:0]	Serial Transmit Data	Serial write data, valid only in asynchronous mode including multi-processor, and clock synchronous mode, and with FIFO selected	W
b9	MPBT	Multi-Processor Transfer Bit Flag	Value of the multi-processor bit in the transmission frame: 0: Data transmission cycle 1: ID transmission cycle. MPBT is valid only in asynchronous mode with SMR.MP = 1 and FIFO selected.	W
b15 to b10	—	Reserved	The write value should be 1	W

FTDRHL is a 16-bit register that consists of FTDRH and FTDRL.

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and the multi-processor

29.2.6 发送9位数据寄存器(TDRHL)

Address(es): SCI0.TDRHL 4007 000Eh, SCI1.TDRHL 4007 002Eh, SCI4.TDRHL 4007 008Eh, SCI9.TDRHL 4007 012Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDRHL是一个16位寄存器，用于存储发送数据。选择异步模式和9位数据长度时，请使用此寄存器。

TDRHL的低8位是TDR的影子寄存器，所以访问TDRHL会影响TDR。如果选择7位或8位数据长度，则禁止访问TDRHL寄存器。

当在TSR中检测到空空间时，存储在TDRHL中的发送数据被传送到TSR并开始发送。

TSR和TDRHL具有双缓冲结构，以支持连续传输。当传输完一帧数据后，下一个要传输的数据存储在TDRHL中时，通过将数据传输到TSR继续传输操作。

CPU可以读取和写入TDRHL。TDRHL中的位[15:9]固定为1。这些位被读取为1。写入值应为1。

当发出发送数据空中断(SCIn_TXI)请求时，仅将发送数据写入TDRHL一次。

29.2.7 发送FIFO数据寄存器H L HL(FTDRH FTDRL FTDRHL)

发送FIFO数据寄存器H(FTDRH)

Address(es): SCI0.FTDRH 4007 000Eh, SCI1.FTDRH 4007 002Eh

发送FIFO数据寄存器L(FTDRL)

Address(es): SCI0.FTDRL 4007 000Fh, SCI1.FTDRL 4007 002Fh

发送FIFO数据寄存器HL(FTDRHL)

Address(es): SCI0.FTDRHL 4007 000Eh, SCI1.FTDRHL 4007 002Eh

	SCIn.FTDRHL															
	SCIn.FTDRH								SCIn.FTDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MPBT	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b8 to b0	TDAT[8:0]	串行传输数据	串行写入数据，仅在异步模式（包括多处理器）和时钟同步模式下有效，并且选择了FIFO	W
b9	MPBT	多处理器传输位标志	传输帧中多处理器位的值：0：数据传输周期1：ID传输周期。MPBT仅在SMR.MP=1且选择了FIFO的异步模式下有效。	W
b15 to b10	—	Reserved	写入值应为1	W

FTDRHL是一个16位寄存器，由FTDRH和FTDRL组成。

FTDRH和FTDRL构成一个16级FIFO寄存器，用于存储串行传输的数据和多处理器

transfer bit. This register is valid only in asynchronous mode, including multi-processor mode and clock synchronous mode.

When the SCI detects that the TSR register is empty, it transmits data written in FTDRH and FTDRL into TSR and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDRHL is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to FTDRH and FTDRL but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in order from FTDRH to FTDRL.

MPBT flag (Multi-Processor Transfer Bit Flag)

Selects the multi-processor bit of the transmit frame. When FCR.FM = 1, SSR.MPBT is not valid.

29.2.8 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to TSR, then sends the data to the TXDn pin. The CPU cannot directly access TSR.

29.2.9 Serial Mode Register (SMR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SMR 4007 0000h, SCI1.SMR 4007 0020h, SCI4.SMR 4007 0080h, SCI9.SMR 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1.	R/W*4
b2	MP	Multi-Processor Mode	Valid only in asynchronous mode: 0: Multi-processor communications function is disabled 1: Multi-processor communications function is enabled.	R/W*4
b3	STOP	Stop Bit Length	Valid only in asynchronous mode: 0: 1 stop bit 1: 2 stop bits.	R/W*4
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Selects even parity 1: Selects odd parity.	R/W*4
b5	PE	Parity Enable	Valid only in asynchronous mode: • When transmitting: 0: Parity bit is not added 1: Parity bit is added. • When receiving: 0: Parity bit is not checked 1: Parity bit is checked.	R/W*4
b6	CHR	Character Length	Valid only in asynchronous mode*2. Selects character length in combination with the CHR1 bit in SCMR: CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3.	R/W*4

传输位。该寄存器仅在异步模式下有效，包括多处理器模式和时钟同步模式。

当SCI检测到TSR寄存器为空时，将写入FTDRH和FTDRL的数据发送到TSR并开始串行传输。执行连续串行传输，直到在FTDRH和FTDRL中没有剩余传输数据。当FTDRHL充满传输数据时，不能再写入数据。如果尝试写入新数据，则忽略该数据。

CPU可以写入FTDRH和FTDRL但不能读取它们。

当同时写入FTDRH和FTDRL寄存器时，按照从FTDRH到FTDRL的顺序写入。

MPBT标志（多处理器传输位标志）

选择发送帧的多处理器位。当FCR.FM=1时，SSR.MPBT无效。

29.2.8 发送移位寄存器(TSR)

TSR是传送串行数据的移位寄存器。为了进行串行数据传输，SCI首先自动将发送数据从TDR、TDRHL或发送FIFO传输到TSR，然后将数据发送到TXDn引脚。CPU不能直接访问TSR。

29.2.9 非智能卡接口模式的串行模式寄存器(SMR)(SCMR.SMIF=0)

Address(es): SCI0.SMR 4007 0000h, SCI1.SMR 4007 0020h, SCI4.SMR 4007 0080h, SCI9.SMR 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKS[1:0]	时钟选择	b1 b0 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1.	R/W*4
b2	MP	Multi-Processor Mode	仅在异步模式下有效：0：禁用多处理器通信功能1：启用多处理器通信功能。	R/W*4
b3	STOP	停止位长度	仅在异步模式下有效：0：1个停止位1：2个停止位。	R/W*4
b4	PM	奇偶校验模式	仅在PE位为1时有效：0：选择偶校验1：选择奇校验。	R/W*4
b5	PE	奇偶校验使能	仅在异步模式下有效：　发送时：0：不添加奇偶校验位1：添加奇偶校验位。　接收时：0：不检查奇偶校验位1：检查奇偶校验位。	R/W*4
b6	CHR	字符长度	仅在异步模式下有效*2。 结合CHR1位选择字符长度 SCMR: CHR1 CHR 0 0：以9位数据长度发送接收 0 1：以9位数据长度发送接收 1 0：发送接收8位数据长度（初始值） 1 1：以7位数据长度发送接收*3。	R/W*4

Bit	Symbol	Bit name	Description	R/W
b7	CM	Communication Mode	0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode.	R/W*4

Note 1. n is the decimal notation of the value of n in BRR. See section 29.2.17, Bit Rate Register (BRR).
Note 2. In any mode other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB bit [7] in TDR is not transmitted.
Note 4. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

SMR sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, see section 29.2.17, Bit Rate Register (BRR).

MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The settings of the PE and PM bits are invalid in multi-processor mode.

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception.

The setting of the PM bit is invalid in multi-processor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception.

Regardless of the setting of the PE bit, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the CHR1 bit in SCMR.

In modes other than asynchronous mode, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode.

Bit	Symbol	位名称	Description	R/W
b7	CM	通讯方式	0：异步模式或简单IIC模式1：时钟同步模式或简单SPI模式。	R/W*4

Note 1. n是BRR中n值的十进制表示法。请参阅第29.2.17节，比特率寄存器(BRR)。
Note 2. 在异步模式以外的任何模式下，该位设置无效，使用固定的8位数据长度。
Note 3. LSB-first是固定的，并且不传输TDR中的MSB位[7]。
Note 4. 仅当SCR中的TE=0和SCR中的RE=0时才可写（串行发送和接收都被禁用）。

SMR设置片内波特率发生器的通信格式和时钟源。

CKS[1:0]位（时钟选择）

CKS[1:0]位选择片内波特率发生器的时钟源。

有关这些位的设置与波特率之间的关系，请参见第29.2.17节，比特率寄存器(BRR)。

MP位（多处理器模式）

MP位禁用或启用多处理器通信功能。PE和PM位的设置在多处理器模式下无效。

停止位（停止位长度）

STOP位选择传输中的停止位长度。

在接收中，无论该位设置如何，都只检查第一个停止位。如果第二个停止位为0，则将其视为下一个发送帧的起始位。

PM位（奇偶校验模式）

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。

PM位的设置在多处理器模式下无效。

PE位（奇偶校验使能）

当PE位设置为1时，发送数据时添加奇偶校验位，接收时检查奇偶校验位。

无论PE位的设置如何，在多处理器格式中都不会添加或检查奇偶校验位。

CHR位（字符长度）

CHR位与SCMR中的CHR1位一起选择发送和接收的数据长度。

在异步模式以外的模式中，使用8位的固定数据长度。

CM位（通信模式）

CM位选择通信模式：

- 异步模式或简单IIC模式
- 时钟同步模式或简单的SPI模式。

29.2.10 Serial Mode Register for Smart Card Interface Mode (SMR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SMR_SMCI 4007 0000h, SCI1.SMR_SMCI 4007 0020h, SCI4.SMR_SMCI 4007 0080h, SCI9.SMR_SMCI 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1.	R/W*2
b3, b2	BCP[1:0]	Base Clock Pulse	Selects the number of base clock cycles in combination with the BCP2 bit in SCMR. Table 29.3 lists the combinations of the SCMR.BCP2 bit and SMR.BCP[1:0] bits.	R/W*2
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Selects even parity 1: Selects odd parity.	R/W*2
b5	PE	Parity Enable	When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
b6	BLK	Block Transfer Mode	0: Non-block transfer mode operation 1: Block transfer mode operation.	R/W*2
b7	GM	GSM Mode	0: Non-GSM mode operation 1: GSM mode operation.	R/W*2

Note 1. n is the decimal notation of the value of n in BRR. See section 29.2.17, Bit Rate Register (BRR).
Note 2. Writable only when SCR_SMCI.TE = 0 and SCR_SMCI.RE = 0 (both serial transmission and reception are disabled).

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, see section 29.2.17, Bit Rate Register (BRR).

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode.

Set these bits in combination with the SCMR.BCP2 bit.

For details, see section 29.6.4, Receive Data Sampling Timing and Reception Margin.

Table 29.3 Combinations of SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits (1 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00	93 clock cycles (S = 93)*1
0	01	128 clock cycles (S = 128)*1
0	10	186 clock cycles (S = 186)*1
0	11	512 clock cycles (S = 512)*1
1	00	32 clock cycles (S = 32)*1 (initial value)
1	01	64 clock cycles (S = 64)*1

29.2.10 智能卡接口模式的串行模式寄存器(SMR_SMCI)(SCMR.SMIF=1)

Address(es): SCI0.SMR_SMCI 4007 0000h, SCI1.SMR_SMCI 4007 0020h, SCI4.SMR_SMCI 4007 0080h, SCI9.SMR_SMCI 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKS[1:0]	时钟选择	b1 b0 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1.	R/W*2
b3, b2	BCP[1:0]	基本时钟脉冲	结合SCMR中的BCP2位选择基本时钟周期数。表29.3列出了SCMR.BCP2位和 SMR.BCP[1:0] bits.	R/W*2
b4	PM	奇偶校验模式	仅在PE位为1时有效：0：选择 偶校验1：选择奇校验。	R/W*2
b5	PE	奇偶校验使能	当该位设置为1时，发送数据时添加一个奇偶校验位，并检查接收数据的奇偶校验。在智能卡接口模式下将此位设置为1。	R/W*2
b6	BLK	块传输模式	0：非块传输模式操作1：块传输模式 操作。	R/W*2
b7	GM	GSM Mode	0：非GSM模式操作1：GSM 模式操作。	R/W*2

Note 1. n是BRR中n值的十进制表示法。请参阅第29.2.17节，比特率寄存器(BRR)。
Note 2. 仅当SCR_SMCI.TE=0且SCR_SMCI.RE=0时可写（串行传输和接收均禁用）。

SMR_SMCI寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0]位（时钟选择）

CKS[1:0]位选择片内波特率发生器的时钟源。

有关这些位的设置与波特率之间的关系，请参见第29.2.17节，比特率寄存器(BRR)。

BCP[1:0]位（基本时钟脉冲）

BCP[1:0]位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。

将这些位与SCMR.BCP2位一起设置。

有关详细信息，请参阅第29.6.4节，接收数据采样时序和接收余量。

Table 29.3 SCMR.BCP2位和SMR_SMCI.BCP[1:0]位的组合（1of2）

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
0	00	93个时钟周期(S=93)*1
0	01	128个时钟周期(S=128)*1
0	10	186个时钟周期(S=186)*1
0	11	512个时钟周期(S=512)*1
1	00	32个时钟周期(S=32)*1（初始值）
1	01	64个时钟周期(S=64)*1

Table 29.3 Combinations of SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits (2 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
1	10	372 clock cycles (S = 372)*1
1	11	256 clock cycles (S = 256)*1

Note 1. S is the value of S in BRR (see section 29.2.17, Bit Rate Register (BRR)).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd).

For details on the usage of this bit in smart card interface mode, see section 29.6.2, Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1.

The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK bit (Block Transfer Mode)

Setting the BLK bit to 1 enables block transfer mode operation.

For details, see section 29.6.3, Block Transfer Mode.

GM bit (GSM Mode)

Setting the GM bit to 1 enables GSM mode operation.

In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETU (elementary time unit = 1-bit transfer time) from the start, and the clock output control function is enabled. For details, see section 29.6.6, Serial Data Transmission (Except in Block Transfer Mode) and section 29.6.8, Clock Output Control.

29.2.11 Serial Control Register (SCR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SCR 4007 0002h, SCI1.SCR 4007 0022h, SCI4.SCR 4007 0082h, SCI9.SCR 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	Asynchronous mode: b1 b0 0 0: On-chip baud rate generator. The SCKn pin is available for use as an I/O port according to the I/O port settings 0 1: On-chip baud rate generator. A clock with the same frequency as the bit rate is output from the SCKn pin 1 x: External clock. A clock with a frequency 16 times the bit rate should be input from the SCKn pin when SEMR.ABCS bit is 0. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. Clock synchronous mode: b1 b0 0 x: Internal clock. The SCKn pin functions as the clock output pin 1 x: External clock. The SCKn pin functions as the clock input pin.	R/W*1

Table 29.3 SCMR.BCP2位和SMR_SMCI.BCP[1:0]位的组合（2个中的2个）

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
1	10	372个时钟周期(S=372)*1
1	11	256个时钟周期(S=256)*1

Note 1. S是BRR中S的值（参见第29.2.17节，比特率寄存器(BRR)）。

PM位（奇偶校验模式）

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。

有关该位在智能卡接口模式下的使用详情，请参见第29.6.2节，数据格式（块中除外）Transfer Mode).

PE位（奇偶校验使能）

将PE位设置为1。

发送数据前添加奇偶校验位，接收时校验奇偶校验位。

BLK位（块传输模式）

将BLK位设置为1可启用块传输模式操作。

有关详细信息，请参阅第29.6.3节，块传输模式。

GM位（GSM模式）

将GM位设置为1启用GSM模式操作。

在GSM模式下，SSR_SMCI.TEND标志设置时序从开始前移到11.0ETU（基本时间单位=1位传输时间），并启用时钟输出控制功能。有关详细信息，请参见第29.6.6节，串行数据传输（块传输模式除外）和第29.6.8节，时钟输出控制。

29.2.11 非智能卡接口模式的串行控制寄存器(SCR)(SCMR.SMIF=0)

Address(es): SCI0.SCR 4007 0002h, SCI1.SCR 4007 0022h, SCI4.SCR 4007 0082h, SCI9.SCR 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKE[1:0]	时钟使能	异步模式：b1b000：片内波特率发生器。 根据IO端口设置，SCKn引脚可用作IO端口01：片内波特率发生器。 从SCKn引脚输出与比特率相同频率的时钟1x：外部时钟。 当SEMR.ABCS位为0时，应从SCKn引脚输入频率为16倍比特率的时钟。当SEMR.ABCS位为1时，输入频率为8倍比特率的时钟信号。 时钟同步模式：b1b00x： 内部时钟。 SCKn引脚用作时钟输出引脚1x：外部时钟。 SCKn引脚用作时钟输入引脚。	R/W*1

Bit	Symbol	Bit name	Description	R/W
b2	TEIE	Transmit End Interrupt Enable	0: SCIn_TEI interrupt request is disabled 1: SCIn_TEI interrupt request is enabled.	R/W
b3	MPIE	Multi-Processor Interrupt Enable	Valid in asynchronous mode when SMR.MP = 1: 0: Non multi-processor reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and non multi-processor reception is resumed.	R/W*3
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled.	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled.	R/W*2
b6	RIE	Receive Interrupt Enable	0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled.	R/W
b7	TIE	Transmit Interrupt Enable	0: SCIn_TXI interrupt request is disabled 1: SCIn_TXI interrupt request is enabled.	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.

Note 2. 1 can be written only when TE = 0 and RE = 0, and the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. When the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.

Note 3. When writing new value to a bit other than the MPIE bit of this register during multi-processor mode (SMR.MP bit = 1), write 0 to MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by read-modify-write when using a bit manipulation instruction.

The SCR register controls operation and the clock source selection for transmission and reception.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and SCKn pin function.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables an SCIn_TEI interrupt request. Set the TEIE bit to 0 to disable the interrupt request.

In simple IIC mode, SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STI). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags RDRF, RDF, ORER, and FER in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE is automatically set to 0, and non multi-processor reception resumes. For details, see section 29.4, Multi-Processor Communications Function.

When the receive data that includes the MPB bit is set to 0, the receive data is not transferred from the RSR to the RDR, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the receive data that includes the MPB bit is set to 1, the MPIE bit is automatically set to 0, the SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and the setting of the ORER and FER flags to 1 is enabled.

Set MPIE to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception.

When the RE bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Set the reception format in the SMR before setting the RE bit to 1.

When non-FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER

Bit	Symbol	位名称	Description	R/W
b2	TEIE	发送结束中断使能	0：禁止SCIn_TEI中断请求1：使能SCIn_TEI中断请求。	R/W
b3	MPIE	多处理器中断使能	SMR.MP=1时在异步模式下有效：0：非多处理器接收1：当多处理器位设置为0的数据是 接收时，不读取数据，并且将SSR中的状态标志RDRF、ORER和FER设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动设置为0，并恢复非多处理器接收。	R/W*3
b4	RE	接收启用	0：禁用串行接收1：启用串行接收。	R/W*2
b5	TE	发送启用	0：禁用串行传输1：启用串行传输。	R/W*2
b6	RIE	接收中断使能	0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI和SCIn_ERI中断请求。	R/W
b7	TIE	发送中断使能	0：禁止SCIn_TXI中断请求1：使能SCIn_TXI中断请求。	R/W

x：不关心注

1。 仅当TE=0且RE=0时可写。

Note 2. 只有在TE=0且RE=0且SMR.CM位为1时才能写入1。设置TE或RE为1后，TE和RE只能写入0。当SMR.CM位为0且SIMR1.IICM位为0时，在任何情况下都可以写入。

Note 3. 在多处理器模式下（SMR.MP位=1）向该寄存器的MPIE位以外的位写入新值时，使用存储指令将0写入MPIE位，以避免通过读取意外将MPIE位设置为1使用位操作指令时的修改-写入。

SCR寄存器控制发送和接收的操作和时钟源选择。

CKE[1:0]位（时钟使能）

CKE[1:0]位选择时钟源和SCKn引脚功能。

TEIE位（发送结束中断使能）

TEIE位启用或禁用SCIn_TEI中断请求。将TEIE位设置为0以禁用中断请求。

在简单IIC模式下，SCIn_TEI在完成发出启动、重新启动或停止条件(STI)时分配给中断。在这种情况下，TEIE位可用于启用或禁用STI。

MPIE位（多处理器中断使能）

当MPIE位设置为1并且接收到多处理器位设置为0的数据时，不读取数据并且将SSRSSR_FIFO中的状态标志RDRF、RDF、ORER和FER设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE自动设置为0，并且非多处理器接收恢复。有关详细信息，请参阅第29.4节，多处理器通信功能。

当包含MPB位的接收数据设置为0时，接收数据不会从RSR传送到RDR，不会检测到接收错误，并且将标志ORER和FER设置为1被禁用。

当包含MPB位的接收数据设置为1时，MPIE位自动设置为0，SCIn_RXI和SCIn_ERI中断请求被启用（如果SCR中的RIE位设置为1），并且ORER和FER标志设置为1被启用。

如果不使用多处理器通信功能，则将MPIE设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。

当RE位设置为1时，串行接收通过检测异步模式下的起始位或时钟同步模式下的同步时钟输入来启动。在将RE位设置为1之前，在SMR中设置接收格式。

Whennon-FIFOoperationisselectedandreceptionishaltedbysettingtheREbitto0 theRDRF ORER FER andPER

flags in SSR are not affected and the previous values are saved.

When FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous values are saved.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When the TE bit is set to 1, serial transmission starts by writing transmit data to TDR. Set the transmission format in the SMR register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

Setting the RIE bit to 0 disables SCIn_RXI and SCIn_ERI interrupt requests.

To cancel an SCIn_ERI interrupt request, read 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO, then set the flag to 0, or set the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt request.

Setting the TIE bit to 0 disables an SCIn_TXI interrupt request. TIE should be set to 1 when the TE bit is 1. The SCIn_TXI interrupt occurs after the TE and TIE bits are set to 1 simultaneously, before transfer starts.

29.2.12 Serial Control Register for Smart Card Interface Mode (SCR_SMCI)(SCMR.SMIF = 1)

Address(es): SCI0.SCR_SMCI 4007 0002h, SCI1.SCR_SMCI 4007 0022h, SCI4.SCR_SMCI 4007 0082h, SCI9.SCR_SMCI 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• When GM in SMR_SMCI = 0: b1 b0 0 0: Output disabled The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: Clock output. 1 x: Setting prohibited. • When GM in SMR_SMCI = 1: b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	This bit should be 0 in smart card interface mode	R/W
b3	MPIE	Multi-Processor Interrupt Enable	This bit should be 0 in smart card interface mode	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled.	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled.	R/W*2
b6	RIE	Receive Interrupt Enable	0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled.	R/W

SSR中的标志不受影响，之前的值被保存。

WhenFIFOoperationisselectedandreceptionishaltedbysettingtheREbitto0 theRDF ORER FER PER andDRflagsinSSR_FIFOarenotaffectedandthepreviousvaluesaresaved.

TE位（发送使能）

TE位启用或禁用串行传输。

当TE位设置为1时，串行发送通过将发送数据写入TDR开始。设置传输格式
将TE位设置为1之前的SMR寄存器。

RIE位（接收中断使能）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

将RIE位设置为0会禁用SCIn_RXI和SCIn_ERI中断请求。

要取消SCIn_ERI中断请求，请从SSRSSR_FIFO中的ORER、FER或PER标志读取1，然后将该标志设置为0，或将RIE位设置为0。

TIE位（发送中断使能）

TIE位启用或禁用SCIn_TXI中断请求。

将TIE位设置为0将禁用SCIn_TXI中断请求。当TE位为1时，应将TIE设置为1。
SCIn_TXI中断发生在TE和TIE位同时设置为1之后，在传输开始之前。

29.2.12 智能卡接口模式的串行控制寄存器(SCR_SMCI)(SCMR.SMIF=1)

Address(es): SCI0.SCR_SMCI 4007 0002h, SCI1.SCR_SMCI 4007 0022h, SCI4.SCR_SMCI 4007 0082h, SCI9.SCR_SMCI 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKE[1:0]	时钟使能	当SMR_SMCI中的GM=0时：b1 b000：输出禁用 根据IO端口设置，SCKn引脚可用作IO端口。01：时钟输出。1x：禁止设置。 当SMR_SMCI中的GM=1时：b1 b000：输出固定低x1：时钟输 出10：输出固定高。	R/W*1
b2	TEIE	发送结束中断使能	该位在智能卡接口模式下应为0	R/W
b3	MPIE	多处理器中断使能	该位在智能卡接口模式下应为0	R/W
b4	RE	接收启用	0：禁用串行接收1：启用串 行接收。	R/W*2
b5	TE	发送启用	0：禁用串行传输1：启用串行传 输。	R/W*2
b6	RIE	接收中断使能	0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn _RXI和SCIn_ERI中断请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	TIE	Transmit Interrupt Enable	0: SCIn_TXI interrupt request is disabled 1: SCIn_TXI interrupt request is enabled.	R/W

x: Don't care
Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written to TE and RE.

SCR_SMCI sets transmission control, interrupt control, and reception and clock source selection for transmission and reception.

For details on interrupt requests, see section 29.10, Interrupt Sources.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin.

In GSM mode, clock output can be dynamically switched. For details, see section 29.6.8, Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

Set the TEIE bit to 0 in smart card interface mode.

RE bit (Receive Enable)

The RE bit enables or disables serial reception.

When this bit is set to 1, serial reception starts by detecting the start bit. Set the reception format in the SMR_SMCI register before setting the RE bit to 1.

When reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous values are saved.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When this bit is set to 1, serial transmission starts by writing transmit data to TDR. Set the transmission format in the SMR_SMCI register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

Setting the RIE bit to 0 disables SCIn_RXI and SCIn_ERI interrupt requests.

To cancel an SCIn_ERI interrupt request, read 1 from the ORER, FER, or PER flag in SSR_SMCI, and then set the flag to 0, or set the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables an SCIn_TXI interrupt request.

Setting the TIE bit to 0 disables an SCIn_TXI interrupt request. TIE should be set to 1 when the TE bit is 1. The SCIn_TXI interrupt occurs after the TE and TIE bits are set to 1 simultaneously, before transfer starts.

Bit	Symbol	位名称	Description	R/W
b7	TIE	发送中断使能	0：禁止SCIn_TXI中断请求1：使能SCIn_ TXI中断请求。	R/W

x：不关心注
1。 仅当TE=0且RE=0时可写。
Note 2. 只有在TE=0和RE=0时才能写入1。将TE或RE设置为1后，TE和RE只能写入0。

SCR_SMCI设置发送和接收的发送控制、中断控制以及接收和时钟源选择。

有关中断请求的详细信息，请参见第29.10节，中断源。

CKE[1:0]位（时钟使能）

CKE[1:0]位控制SCKn引脚的时钟输出。

在GSM模式下，时钟输出可以动态切换。有关详细信息，请参见第29.6.8节，时钟输出控制。

TEIE位（发送结束中断使能）

在智能卡接口模式下将TEIE位设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。

当该位设置为1时，串行接收通过检测起始位开始。在将RE位设置为1之前，在SMR_SMCI寄存器中设置接收格式。

当通过将RE位设置为0来停止接收时，SSR_SMCI中的ORER、FER和PER标志不受影响，并且之前的值被保存。

TE位（发送使能）

TE位启用或禁用串行传输。

当该位设置为1时，串行传输通过将发送数据写入TDR开始。设置传输格式
将TE位设置为1之前的SMR_SMCI寄存器。

RIE位（接收中断使能）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

将RIE位设置为0会禁用SCIn_RXI和SCIn_ERI中断请求。

要取消SCIn_ERI中断请求，请从SSR_SMCI中的ORER、FER或PER标志读取1，然后将该标志设置为0，或者将RIE位设置为0。

TIE位（发送中断使能）

TIE位启用或禁用SCIn_TXI中断请求。

将TIE位设置为0将禁用SCIn_TXI中断请求。当TE位为1时，应将TIE设置为1。
SCIn_TXI中断发生在TE和TIE位同时设置为1之后，在传输开始之前。

29.2.13 Serial Status Register (SSR) for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)

Address(es): SCI0.SSR 4007 0004h, SCI1.SSR 4007 0024h, SCI4.SSR 4007 0084h, SCI9.SSR 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Sets the multi-processor bit in the transmission frame: 0: Data transmission cycle 1: ID transmission cycle.	R/W
b1	MPB	Multi-Processor	Value of the multi-processor bit in the reception frame: 0: Data transmission cycle 1: ID transmission cycle.	R
b2	TEND	Transmit End Flag	0: A character is transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: No received data is in RDR register 1: Received data is in RDR register.	R/(W)*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data is in TDR register 1: No transmit data is in TDR register.	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides the SCI status flags and transmission and reception multi-processor bits.

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit selects the multi-processor bit in the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 to disable serial transmission and the FCR.FM bit is set to 0 (non-FIFO selected)
- When the SCR.TE bit is set to 1, the TEND flag is not affected and keeps the value 1
- When the TDR register is not updated at the time of transmission of the tail-end bit of a character being transmitted.

[Clearing conditions]

- When transmit data is written to the TDR register when the SCR.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 when the SCR.TE bit is 1.

29.2.13 用于非智能卡接口和非FIFO模式的串行状态寄存器(SSR)（SCMR.SMIF=0和FCR.FM=0）

Address(es): SCI0.SSR 4007 0004h, SCI1.SSR 4007 0024h, SCI4.SSR 4007 0084h, SCI9.SSR 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	位名称	Description	R/W
b0	MPBT	多处理器位传输	设置传输帧中的多处理器位：0：数据传输周期1：ID传输周期。	R/W
b1	MPB	Multi-Processor	接收帧中多处理器位的值：0：数据发送周期1：ID发送周期。	R
b2	TEND	发送结束标志	0：传送一个字符1：字符传送完成。	R
b3	PER	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*1
b4	FER	成帧错误标志	0：未发生帧错误1：发生帧错误。	R/(W)*1
b5	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b6	RDRF	接收数据满标志	0：RDR寄存器中没有接收到的数据1：RDR寄存器中接收到的数据。	R/(W)*1
b7	TDRE	传输数据空标志	0：发送数据在TDR寄存器1：没有发送数据在TDR寄存器。	R/(W)*1

Note 1. 读1后只能写0清除标志。

SSR寄存器提供SCI状态标志和发送和接收多处理器位。

MPBT位（多处理器位传输）

MPBT位选择发送帧中的多处理器位。

MPB bit (Multi-Processor)

MPB位保存接收帧中多处理器位的值。该位不改变时SCR.RE位为0。

TEND标志（发送结束标志）

TEND标志表示传输完成。

[Setting conditions]

- 当SCR.TE位设置为0以禁用串行传输且FCR.FM位设置为0（选择非FIFO）时
- 当SCR.TE位设置为1时，TEND标志不受影响并保持值1
- 当TDR寄存器在发送字符的尾端位时未更新时。

[Clearing conditions]

- 当SCR.TE位为1时将发送数据写入TDR寄存器
- 当SCR.TE位为1时，读取TDRE=1后将0写入TDRE。

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurs during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode and the address match function is disabled (DCCR.DCME = 0).

  Although receive data is transferred to RDR when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to PER, read the PER bit to check that it was actually set to 0.

When the SCR.RE is set to 0 to disable serial reception, the PER flag is not affected and keeps its previous value.

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurs during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode and the address match function is disabled (DCCR.DCME = 0).

  In 2-stop mode, only the first stop bit is checked but the second stop bit is not checked. Although received data is transferred to RDR when the framing error occurs, no SCIn_RXI interrupt request occurs. Also, when the FER flag is set to 1, the subsequent received data is not transferred to RDR.

[Clearing condition]

- When 0 is written to FER after reading FER = 1. After writing 0 to FER, read the FER bit to check that its value is 0.

When the SCR.RE bit is set to 0, the FER flag is not affected and keeps its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurs during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before the receive data that does not have a parity error and a framing error is read from RDR.

  In RDR, data received prior to an overrun error occurrence is kept, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, reception data is not forwarded to RDR. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to ORER, read the ORER bit to check that it was actually set to 0.

When the RE bit in SCR is set to 0, the ORER flag is not affected and keeps its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When RDRF is set to 0 after 1 is read

PER标志（奇偶校验错误标志）

PER标志表示异步模式接收时发生奇偶校验错误，接收异常结束。

[Setting condition]

- 当在异步模式下接收期间检测到奇偶校验错误并且地址匹配功能被禁用（DCCR.DCME=0）。

  尽管发生奇偶校验错误时将接收数据传输到RDR，但不会发生SCIn_RXI中断请求。当PER标志设置为1时，后续接收数据不传输到RDR。【结算条件】

- 当读取PER=1后将0写入PER。将0写入PER后，读取PER位以检查它是否实际设置为0。

当SCR.RE设置为0以禁用串行接收时，PER标志不受影响并保持其先前的值。

FER标志（帧错误标志）

FER标志表示在异步模式接收过程中发生了帧错误，接收异常结束。

[Setting condition]

- 在异步模式下接收期间采样0作为停止位并且禁用地址匹配功能(DCCR.DCME=0)。

在2-stop模式下，只检查第一个停止位，但不检查第二个停止位。虽然发生帧错误时接收到的数据被传输到RDR，但不会发生SCIn_RXI中断请求。此外，当FER标志设置为1时，后续接收的数据不会传输到RDR。【结算条件】

- 当读取FER=1后向FER写入0。向FER写入0后，读取FER位以检查其值是否为0。

当SCR.RE位设置为0时，FER标志不受影响并保持其先前的值。

ORER标志（溢出错误标志）

ORER标志表示接收过程中发生溢出错误，接收异常结束。

[Setting condition]

- 在没有奇偶校验错误和帧错误的接收数据之前接收到下一个数据时，从RDR读取。

在RDR中，会保留发生溢出错误之前接收到的数据，但会丢失发生溢出错误之后接收到的数据。当ORER标志设置为1时，接收数据不转发到RDR。在时钟同步模式下，串行发送和接收停止。【结算条件】

- 当读取ORER=1后向ORER写入0。向ORER写入0后，读取ORER位以检查它是否实际设置为0。

当SCR中的RE位设置为0时，ORER标志不受影响并保持其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

- 当接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

- 读取1后将RDRF设置为0时

- When data is read from the RDR register.

Note: Do not clear RDRF flag by accessing RDRF bit in SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When TDRE is set to 0 after 1 is read
- When SCR.TE is 1, data is written to the TDR register.

Note: Do not clear TDRE flag by accessing TDRE bit in SSR register unless communication is aborted.

29.2.14 Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1)

Address(es): SCI0.SSR_FIFO 4007 0004h, SCI1.SSR_FIFO 4007 0024h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

Bit	Symbol	Bit name	Description	R/W
b0	DR	Receive Data Ready Flag	0: Receiving is in progress, or no received data remains in FRDRHL after a normal completion of received data (receive FIFO is empty) 1: The next received data is not received for a period after a normal completion of received data, and when the amount of data stored in the FIFO is equal to or less than the received triggering number.	R/(W)*1
b1	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b2	TEND	Transmit End Flag	0: A character is transmitted 1: Character transfer is complete.	R/(W)*1
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: A framing error occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error occurred.	R/(W)*1
b6	RDF	Receive FIFO Data Full Flag	0: The amount of receive data written in FRDRHL is below the specified receive triggering number 1: The amount of receive data written in FRDRHL is equal to or greater than the specified receive triggering number.	R/(W)*1
b7	TDFE	Transmit FIFO Data Empty Flag	0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.	R/(W)*1

Note 1. Only 0 can be written to this bit to clear the flag after reading 1.

The SSR_FIFO register provides the SCI with FIFO mode status flags.

- 从RDR寄存器读取数据时。

Note: 除非通信中止，否则不要通过访问SSR寄存器中的RDRF位来清除RDRF标志。

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

- 当SCR.TE位为0时
- 当数据从TDR寄存器传输到TSR寄存器时。

[Clearing conditions]

- 读取1后TDRE设置为0时
- 当SCR.TE为1时，数据被写入TDR寄存器。

Note: 除非通信中止，否则不要通过访问SSR寄存器中的TDRE位来清除TDRE标志。

29.2.14 非智能卡接口和FIFO模式的串行状态寄存器(SSR_FIFO)（SCMR.SMIF=0和FCR.FM=1）

Address(es): SCI0.SSR_FIFO 4007 0004h, SCI1.SSR_FIFO 4007 0024h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDFE	RDF	ORER	FER	PER	TEND	—	DR
重置后的值:	1	0	0	0	0	0	x	0

Bit	Symbol	位名称	Description	R/W
b0	DR	接收数据就绪标志	0：接收中，或者接收数据正常完成后FRDRHL中没有接收到的数据（接收FIFO为空）1：一段时间内没有接收到下一个接收数据 接收数据正常完成后，且FIFO中存储的数据量等于或小于接收触发数时。	R/(W)*1
b1	—	Reserved	读取值未定义。写入值应为1。	R/W
b2	TEND	发送结束标志	0：传送一个字符1：字符传送完成。	R/(W)*1
b3	PER	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*1
b4	FER	成帧错误标志	0：未发生帧错误1：发生帧错误。	R/(W)*1
b5	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b6	RDF	接收FIFO数据满标志	0：写入FRDRHL的接收数据量低于指定的接收触发数 1：写入FRDRHL的接收数据量为 等于或大于指定的接收触发数。	R/(W)*1
b7	TDFE	发送FIFO数据空标志	0：写入FTDRHL的发送数据量超过指定的发送触发数1：写入FTDRHL的发送数据量等于或小于指定的发送触发数。	R/(W)*1

Note 1. 读取1后，只能向该位写入0以清除标志。

SSR_FIFO寄存器为SCI提供FIFO模式状态标志。

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number, and that no subsequent data is received after the elapse of 15 ETUs (Elementary Time Units) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, and when FIFO is selected.

In clock synchronous mode, this flag is not set to 1.

[Setting condition]

- When FRDRHL contains less data than the specified receive triggering number, and no subsequent data is received after the elapse of 15 ETUs*1 from the last stop bit, and the SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR, and after all the received data are read
- When the FCR.FM bit changes from 0 to 1.

Note 1. This is equivalent to 1.5 frames in the 8-bit format with one stop bit.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, so transmission is halted.

[Setting condition]

- TEND is set to 1 when FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written to FTDRHL when the SCR.TE bit is 1
- When 0 is written to TEND after 1 is read from TEND, when the SCR.TE bit is 1
- When the FCR.FM bit changes from 0 to 1.

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When data is received and a parity error is detected, and the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to PER after reading PER = 1.

The reception operation is continuous when receive data is stored to the FRDRHL register even when a parity error occurs while data is received.

When the SCR.RE bit is set to 0, the PER flag is not affected and the previous state is kept.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When 0 is sampled as the stop bit during reception and the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to FER after reading FER = 1.

The reception operation is continuous, and the receive data is stored to the FRDRHL register even when a framing error

DR标志（接收数据就绪标志）

DR标志表示存储在接收FIFO数据寄存器(FRDRHL)中的数据量低于指定的接收触发数，并且从最后一个停止位开始经过15个ETU（基本时间单位）后没有接收到后续数据在异步模式下。该标志仅在异步模式（包括多处理器模式）和选择FIFO时有效。

在时钟同步模式下，该标志不设置为1。

[Setting condition]

- 当FRDRHL包含的数据少于指定的接收触发数，并且从最后一个停止位开始经过15个ETU*1后没有接收到后续数据，并且SSR_FIFO.FER和SSR_FIFO.PER标志为0。

[Clearing conditions]

- 从DR读取1时，并且在读取所有接收到的数据之后
- 当FCR.FM位从0变为1时。

注1.这相当于8位格式的1.5帧，带有一位停止位。

TEND标志（发送结束标志）

TEND标志表明FTDRHL在发送串行字符的最后一位时不包含有效数据，因此停止发送。

[Setting condition]

- 当发送1字节串行字符的最后一位时，如果FTDRHL不包含发送数据，则TEND设置为1。

[Clearing conditions]

- 当SCR.TE位为1时将发送数据写入FTDRHL
- 当从TEND读取1后向TEND写入0时，当SCR.TE位为1时
- 当FCR.FM位从0变为1时。

PER标志（奇偶校验错误标志）

PER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在奇偶校验错误。

[Setting condition]

- 当接收到数据并检测到奇偶校验错误时，地址匹配功能被禁用（DCCR.DCME=0）。

[Clearing condition]

- 在读取PER=1后将0写入PER时。

当接收数据被存储到FRDRHL寄存器时，接收操作是连续的，即使在接收数据时发生奇偶校验错误。

当SCR.RE位设置为0时，PER标志不受影响并保持之前的状态。

FER标志（帧错误标志）

FER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在帧错误。

[Setting condition]

- 当在接收期间采样0作为停止位并且地址匹配功能被禁用(DCCR.DCME=0)。

[Clearing condition]

- 当读取FER=1后将0写入FER。

接收操作是连续的，即使发生帧错误，接收数据也会存储到FRDRHL寄存器中

occurs while data is received.

When the SCR.RE bit is set to 0, the FER flag is not affected and the previous state is kept.

ORER flag (Overrun Error Flag)

The ORER flag indicates that the receive operation stopped abnormally because an overrun error occurred.

[Setting condition]

- When the next serial reception completes while the receive FIFO is full with 16-byte receive data.

[Clearing condition]

- When 0 is written after 1 is read from ORER.

When the SCR.RE bit is set to 0, the ORER flag is not affected and the previous state is kept.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that receive data is transferred to the FRDRHL register, and the amount of data in FRDRHL is equal to or exceeds the specified receive triggering number. When RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- When the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL,*1 and the FIFO is not empty.

[Clearing conditions]

- When 0 is written after 1 is read from RDF
- When FRDRHL is read by the DMAC or DTC but only when block transfer is the last transmission
- When the setting condition and clearing condition occur at the same time. After that, when the amount of data stored in the FRDRHL register is the same or greater than the RTRG value, RDF is set to 1 after 1 PCLK.

Note: Do not clear RDF flags by accessing RDF bit in the SSR register before reading receive data unless communication is aborted.

Note 1. Because the FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that when data is transferred from FTDRHL into TSR, the amount of data in FTDRHL has fallen below the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- When the TE bit in SCR is 0
- When the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.*1

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DTC or DMAC is activated
- When 0 is written to the TDFE flag after reading TDFE = 1.
  When the setting condition and the clearing condition occur at the same time, the TDFE flag is 0. Thereafter, when the amount of data stored in FTDRHL register is equal to or less than the TTRG value, TDFE is set to 1 after 1 PCLK.

Note: Do not clear TDFE flags by accessing TDFE bit in the SSR register before writing transmit data unless communication is aborted.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, the maximum amount of data that can be written when the TDFE flag is set to 1 is 16 minus FDR.T[4:0]. If more data is written, data is discarded.

在接收数据时发生。

当SCR.RE位设置为0时，FER标志不受影响，保持之前的状态。

ORER标志（溢出错误标志）

ORER标志指示接收操作由于发生溢出错误而异常停止。

[Setting condition]

- 当接收FIFO充满16字节接收数据时，下一次串行接收完成。

[Clearing condition]

- 从ORER读取1后写入0。

当SCR.RE位设置为0时，ORER标志不受影响并保持之前的状态。

RDF标志（接收FIFO数据满标志）

RDF标志表示接收数据被传送到FRDRHL寄存器，并且FRDRHL中的数据量等于或超过指定的接收触发数。当RTRG设置为0时，即使接收FIFO中的数据量等于0，RDF标志也不会设置。

[Setting condition]

- 当接收数据量等于或大于指定的接收触发数时存储在FRDRHL *1且FIFO不为空。

[Clearing conditions]

- 从RDF读取1后写入0时
- 当DMAC或DTC读取FRDRHL但仅当块传输是最后一次传输时
- 当设置条件和清除条件同时出现时。之后，当FRDRHL寄存器中存储的数据量等于或大于RTRG值时，RDF在1个PCLK后设置为1。

注意：除非通信中止，否则在读取接收数据之前不要通过访问SSR寄存器中的RDF位来清除RDF标志。注1.由于FRDRHL为16级FIFO寄存器，RDF为1时可读取的最大数据量等于指定的接收触发数。如果在读取FRDRHL中的所有数据后尝试读取，则数据未定义。

TDFE标志（发送FIFO数据空标志）

TDFE标志表示当数据从FTDRHL传输到TSR时，FTDRHL中的数据量已低于指定的发送触发数，并且允许将发送数据写入FTDRHL。

[Setting conditions]

- 当SCR的TE位为0时
- 当写入FTDRHL的传输数据量等于或小于指定的传输触发数时。*1

[Clearing conditions]

- 当DTC或DMAC被激活时，在最后一次传输上执行写入FTDRHL
- 读取TDFE=1后将0写入TDFE标志时。
  当设置条件和清除条件同时出现时，TDFE标志为0。此后，当FTDRHL寄存器中存储的数据量等于或小于TTRG值时，在1个PCLK后TDFE设置为1。

注意：除非通信被中止，否则在写入发送数据之前不要通过访问SSR寄存器中的TDFE位来清除TDFE标志。注1.因为FTDRHL寄存器是16级FIFO寄存器，所以TDFE标志设置为1时可写入的最大数据量为16减去FDR.T[4:0]。如果写入更多数据，则丢弃数据。

29.2.15 Serial Status Register for Smart Card Interface Mode (SSR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SSR_SMCI 4007 0004h, SCI1.SSR_SMCI 4007 0024h, SCI4.SSR_SMCI 4007 0084h, SCI9.SSR_SMCI 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Set this bit to 0 in smart card interface mode	R/W
b1	MPB	Multi-Processor	Set this bit to 0 in smart card interface mode	R
b2	TEND	Transmit End Flag	0: A character is transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/(W)*1
b4	ERS	Error Signal Status Flag	0: Low error signal is not sampled 1: Low error signal is sampled.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error occurred.	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: No received data in RDR 1: Received data in RDR.	R/(W)*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data in TDR 1: No transmit data in TDR.	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR_SMCI register provides SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

With no error signal from the receiving side, the TEND flag is set to 1 when more data is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 to disable serial transmission. When the SCR_SMCI.TE bit changes from 0 to 1, the TEND flag is not affected and keeps the value 1.
- When a specified period elapses after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by the following register settings:
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETU after the start of transmission
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETU after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETU after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETU after the start of transmission.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR_SMCI.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurs during reception in asynchronous mode and the reception ends abnormally.

29.2.15 智能卡接口模式的串行状态寄存器(SSR_SMCI)(SCMR.SMIF=1)

Address(es): SCI0.SSR_SMCI 4007 0004h, SCI1.SSR_SMCI 4007 0024h, SCI4.SSR_SMCI 4007 0084h, SCI9.SSR_SMCI 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
重置后的值:	1	0	0	0	0	1	0	0

Bit	Symbol	位名称	Description	R/W
b0	MPBT	多处理器位传输	在智能卡接口模式下将此位设置为0	R/W
b1	MPB	Multi-Processor	在智能卡接口模式下将此位设置为0	R
b2	TEND	发送结束标志	0：传送一个字符1：字符传送完成。	R
b3	PER	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*1
b4	ERS	错误信号状态标志	0：不采样低误差信号1：采样低误差信号。	R/(W)*1
b5	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b6	RDRF	接收数据满标志	0：RDR中没有接收到数据1：RDR中接收到数据。	R/(W)*1
b7	TDRE	传输数据空标志	0：在TDR中发送数据1：在TDR中不发送数据。	R/(W)*1

Note 1. 读1后只能写0清除标志。

SSR_SMCI寄存器为SCI提供智能卡接口模式状态标志。

TEND标志（发送结束标志）

在接收端没有错误信号的情况下，当更多数据准备好传输到接收端时，TEND标志设置为1
TDR register.

[Setting conditions]

- 当SCR_SMCI.TE位=0时禁用串行传输。当SCR_SMCI.TE位由0变为1时，TEND标志不受影响，保持值为1。
- 在最后一次发送1个字节后经过指定时间后，ERS标志为0，并且不更新TDR寄存器。

  设置时序由以下寄存器设置确定：
  - 当SMR_SMCI.GM=0且SMR_SMCI.BLK=0时，传输开始后12.5ETU
  - 当SMR_SMCI.GM=0和SMR_SMCI.BLK=1时，传输开始后11.5ETU
  - 当SMR_SMCI.GM=1和SMR_SMCI.BLK=0时，传输开始后11.0ETU
  - 当SMR_SMCI.GM=1和SMR_SMCI.BLK=1时，11.0ETU后开始传输。

[Clearing conditions]

- 当SCR_SMCI.TE位为1时将发送数据写入TDR寄存器
- 读取TDRE=1后将0写入TDRE且SCR_SMCI.TE位为1。

PER标志（奇偶校验错误标志）

PER标志表示异步模式接收时发生奇偶校验错误，接收异常结束。

[Setting condition]

- When a parity error is detected during reception. Although receive data is transferred to RDR when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to the PER bit after reading PER = 1. After writing 0 to the PER bit, read the PER bit to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0 to disable serial reception, the PER flag is not affected and keeps its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurs during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error is read from the RDR register. In RDR, the data received before an overrun error occurred is saved, but data received after the overrun error is lost. When the ORER flag is set to 1, the received data is not forwarded to the RDR register.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read it to verify that its value is 0.

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and keeps its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in RDR.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after 1 is read
- When data is read from the RDR register.

Note: Do not clear RDRF flags by accessing RDRF bit in the SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When 0 is written to the TDRE after 1 is read
- When the SCR_SMCI.TE bit is 1 and data is forwarded to the TDR register.

Note: Do not clear TDRE flags by accessing TDRE bit in the SSR register unless communication is aborted.

[Setting condition]

- 在接收过程中检测到奇偶校验错误时。尽管发生奇偶校验错误时将接收数据传输到RDR，但不会发生SCIn_RXI中断请求。当PER标志设置为1时，后续接收数据不传输到RDR。

[Clearing condition]

- 当读取PER=1后将0写入PER位时。将0写入PER位后，读取PER位以检查它是否实际设置为0。

当SCR_SMCI中的RE位设置为0以禁用串行接收时，PER标志不受影响并保持其先前的值。

ERS标志（错误信号状态标志）

[Setting condition]

- 当对低误差信号进行采样时。

[Clearing condition]

- 在读取ERS =1后将0写入ERS 时。

ORER标志（溢出错误标志）

ORER标志表示接收过程中发生溢出错误，接收异常结束。

[Setting condition]

- 在从RDR寄存器读取没有奇偶校验错误的接收数据之前接收到下一个数据时。在RDR，溢出错误发生前接收的数据被保存，溢出错误后接收的数据丢失。
  当ORER标志设置为1时，接收到的数据不转发到RDR寄存器。

[Clearing condition]

- 当读取ORER=1后向ORER写入0。向ORER标志写入0后，读取它以验证其值为0。

当SCR_SMCI中的RE位设置为0时，ORER标志不受影响并保持其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR中存在接收数据。

[Setting condition]

- 当接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

- 读取1后向RDRF写入0时
- 从RDR寄存器读取数据时。

Note: 除非通信被中止，否则不要通过访问SSR寄存器中的RDRF位来清除RDRF标志。

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

- 当SCR_SMCI.TE位为0时
- 当数据从TDR寄存器传输到TSR寄存器时。

[Clearing conditions]

- 读取1后向TDRE写入0时
- 当SCR_SMCI.TE位为1并且数据被转发到TDR寄存器时。

Note: 除非通信被中止，否则不要通过访问SSR寄存器中的TDRE位来清除TDRE标志。

29.2.16 Smart Card Mode Register (SCMR)

Address(es): SCI0.SCMR 4007 0006h, SCI1.SCMR 4007 0026h, SCI4.SCMR 4007 0086h, SCI9.SCMR 4007 0126h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	SMIF	Smart Card Interface Mode Select	0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode.	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	SINV	Transmitted/Received Data Invert	0: TDR contents are transmitted as is. Receive data is stored as received in the RDR 1: TDR contents are inverted before transmitted. Receive data is stored in inverted form in the RDR. This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode. Set this bit to 0 for operation in simple IIC mode.	R/W*1
b3	SDIR	Transmitted/Received Data Transfer Direction	0: Transfer with LSB-first 1: Transfer with MSB-first. This bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode. Set this bit to 1 for operation in simple IIC mode.	R/W*1
b4	CHR1	Character Length 1	Only valid only in asynchronous mode*2. Selects the character length in combination with the CHR bit in SMR: CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3.	R/W*1
b6, b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	BCP2	Base Clock Pulse 2	Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 29.4 lists the combinations of the SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. Writable only when TE in SCR/SCR_SMCI = 0 and RE in SCR/SCR_SMCI = 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first should be selected and the value of MSB bit [7] in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects the smart card interface mode. Setting it to 0 selects all the other modes as follows:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode

29.2.16 智能卡模式寄存器(SCMR)

Address(es): SCI0.SCMR 4007 0006h, SCI1.SCMR 4007 0026h, SCI4.SCMR 4007 0086h, SCI9.SCMR 4007 0126h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
重置后的值:	1	1	1	1	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	SMIF	智能卡接口模式选择	0：非智能卡接口模式（异步模式，时钟同步模式、简单SPI模式或简单IIC模式）1：智能卡接口模式。	R/W*1
b1	—	Reserved	该位读取为1。写入值应为1。	R/W
b2	SINV	发送接收数据反转	0：TDR内容按原样发送。接收数据按接收方式存储在RDR1：TDR内容在发送前反转。接收数据以反转形式存储在RDR中。该位可用于以下模式： 智能卡接口模式 异步模式（多处理器模式） 时钟同步模式 简单SPI模式。将此位设置为0以在简单IIC模式下运行。	R/W*1
b3	SDIR	Transmitted/Received Data 转移方向	0：以LSB-first传输1：以MSB-first传输。该位可用于以下模式： 智能卡接口模式 异步模式（多处理器模式） 时钟同步模式 简单SPI模式。将该位设置为1以在简单IIC模式下运行。	R/W*1
b4	CHR1	字符长度1	仅在异步模式下有效*2。 结合SMR中的CHR位选择字符长度：CHR1CHR 0 0：以9位数据长度发送接收 0 1：以9位数据长度发送接收 10：发送接收8位数据长度（初始值）11：发送接收7位数据长度*3。	R/W*1
b6, b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b7	BCP2	基本时钟脉冲2	结合SMR_SMCI.BCP[1:0]位选择基本时钟周期数。表29.4列出了SCMR.BCP2位和 SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. 仅当SCRSCR_SMCI=0中的TE和SCRSCR_SMCI=0中的RE时才可写（串行传输和接收都被禁用）。
Note 2. 该设置无效，并且在非异步模式下使用了固定的8位数据长度。
Note 3. 应选择LSB-first，并且不能传输TDR中MSB位[7]的值。

SCMR寄存器选择智能卡接口和通信格式。

SMIF位（智能卡接口模式选择）

将SMIF位设置为1选择智能卡接口模式。将其设置为0会选择所有其他模式，如下所示：

- 异步模式，包括多处理器模式
- 时钟同步模式
- 简单SPI模式

- Simple IIC mode.

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit/receive data logic level. This bit does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit/receive data in combination with the CHR bit in SMR.

A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

Table 29.4 Combinations of SCMR.BCP2 bit and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00	93 clock cycles (S = 93)*1
0	01	128 clock cycles (S = 128)*1
0	10	186 clock cycles (S = 186)*1
0	11	512 clock cycles (S = 512)*1
1	00	32 clock cycles (S = 32)*1 (initial value)
1	01	64 clock cycles (S = 64)*1
1	10	372 clock cycles (S = 372)*1
1	11	256 clock cycles (S = 256)*1

Note 1. S is the value of S in the Bit Rate Register (BRR). See section 29.2.17, Bit Rate Register (BRR).

29.2.17 Bit Rate Register (BRR)

Address(es): SCI0.BRR 4007 0001h, SCI1.BRR 4007 0021h, SCI4.BRR 4007 0081h, SCI9.BRR 4007 0121h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each. Table 29.5 shows the relationship between the setting (N) and the bit rate (B) in the BRR for asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

The initial value of BRR is FFh. BRR can be read by the CPU, but can only be written to when the TE and RE bits in SCR/SCR_SMCI are 0.

- 简单的IIC模式。

SINV位（发送接收数据反转）

SINV位反转发送接收数据逻辑电平。该位不影响奇偶校验位的逻辑电平。要反转奇偶校验位，请反转SMR或SMR_SMCI中的PM位。

CHR1位（字符长度1）

CHR1位结合SMR中的CHR位选择发送接收数据的数据长度。

在异步模式以外的模式中使用8位的固定数据长度。

BCP2位（基本时钟脉冲2）

BCP2位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将该位与SMR_SMCI.BCP[1:0]位一起设置。

Table 29.4 SCMR.BCP2位和SMR_SMCI.BCP[1:0]位的组合

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
0	00	93个时钟周期(S=93)*1
0	01	128个时钟周期(S=128)*1
0	10	186个时钟周期(S=186)*1
0	11	512个时钟周期(S=512)*1
1	00	32个时钟周期(S=32)*1（初始值）
1	01	64个时钟周期(S=64)*1
1	10	372个时钟周期(S=372)*1
1	11	256个时钟周期(S=256)*1

Note 1. S是比特率寄存器(BRR)中S的值。请参阅第29.2.17节，比特率寄存器(BRR)。

29.2.17 比特率寄存器(BRR)

Address(es): SCI0.BRR 4007 0001h, SCI1.BRR 4007 0021h, SCI4.BRR 4007 0081h, SCI9.BRR 4007 0121h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

BRR是一个8位寄存器，用于调整比特率。

由于每个SCI通道都有独立的波特率发生器控制，因此可以为每个通道设置不同的比特率。表29.5显示了异步模式、多处理器传输、时钟同步模式、智能卡接口模式、简单SPI模式和简单IIC模式的BRR中的设置(N)和比特率(B)之间的关系。

BRR的初始值为FFh。BRR可以被CPU读取，但只有在TE和RE位在
SCR/SCR_SMCI are 0.

Table 29.5 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings BGDM bit	SEMR settings ABCS bit	SEMR settings ABCSE bit	BRR setting	Error
Asynchro-nous, multi-processor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	

B: Bit rate (bps).
N: BRR setting for on-chip baud rate generator ($0 \le N \le 255$).
PCLK: Operating frequency (MHz).
n and S: Determined by the settings of the SMR/SMR_SMCI and SCMR registers as listed in Table 29.7 and Table 29.8.
Note 1. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the I²C standard.

Table 29.6 Calculating widths at high and low level for SCL

Mode	SCL	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 29.7 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bits	Clock source	n
0 0	PCLK clock	0
0 1	PCLK/4 clock	1
1 0	PCLK/16 clock	2
1 1	PCLK/64 clock	3

Table 29.8 Base clock settings in smart card interface mode (1 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	0 0	93 clock cycles	93
0	0 1	128 clock cycles	128

Table 29.5 BRR中的N设置与比特率B的关系

Mode	SEMR settings BGDM bit	SEMR settings ABCS 位	SEMR settings ABCSE bit	BRR setting	Error
异步、多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
时钟同步，简单的SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	

B：比特率（bps）。
N：片内波特率发生器的BRR设置(0 N 255)。
PCLK：工作频率（MHz）。n和S：由表29.7和表29.8中列出的SMRSMR_SMCI和SCMR寄存器的设置决定。

Note 1. 调整码率，使简单IIC模式下SCLn输出的高低电平宽度满足I2C标准。

Table 29.6 计算SCL的高低电平宽度

Mode	SCL	公式（以秒为单位的结果）
IIC	高电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	低电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 29.7 时钟源设置

SMR或SMR_SMCI.CKS[1:0]位	时钟源	n
0 0	PCLK clock	0
0 1	PCLK/4 clock	1
1 0	PCLK/16 clock	2
1 1	PCLK/64 clock	3

Table 29.8 智能卡接口模式下的基本时钟设置（1of2）

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位周期的基本时钟周期	S
0	0 0	93个时钟周期	93
0	0 1	128个时钟周期	128

Table 29.8 Base clock settings in smart card interface mode (2 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	1 0	186 clock cycles	186
0	1 1	512 clock cycles	512
1	0 0	32 clock cycles	32
1	0 1	64 clock cycles	64
1	1 0	372 clock cycles	372
1	1 1	256 clock cycles	256

Table 29.9 and Table 29.10 list examples of BRR (N) settings in asynchronous mode. Table 29.11 lists the maximum bit rate selectable for each operating frequency. Table 29.14 lists the examples of BRR (N) settings in smart card interface mode.

Table 29.17 lists the examples of BRR (N) settings in simple IIC mode. In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 29.6.4, Receive Data Sampling Timing and Reception Margin. Table 29.12 and Table 29.14 list the maximum bit rates with external clock input.

When either the Asynchronous Mode Base Clock Select (ABCS) bit or the Baud Rate Generator Double-Speed Mode Select (BGDM) bit in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice the value listed in Table 29.16. When both of those bits are set to 1, the bit rate becomes four times the listed value.

Table 29.9 Examples of BRR settings for different bit rates in asynchronous mode (1)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

Bit rate (bps)	Operating frequency PCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Table 29.8 智能卡接口模式下的基本时钟设置（2个中的2个）

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位周期的基本时钟周期	S
0	1 0	186个时钟周期	186
0	1 1	512个时钟周期	512
1	0 0	32个时钟周期	32
1	0 1	64个时钟周期	64
1	1 0	372个时钟周期	372
1	1 1	256个时钟周期	256

表29.9和表29.10列出了异步模式下的BRR(N)设置示例。表29.11列出了每个工作频率可选择的最大比特率。表29.14列出了智能卡接口模式下的BRR(N)设置示例。

表29.17列出了简单IIC模式下的BRR(N)设置示例。在智能卡接口模式下，可以选择1位数据传输时间内的基本时钟周期数S。有关详细信息，请参阅第29.6.4节，接收数据采样时序和接收余量。表29.12和表29.14列出了外部时钟输入的最大比特率。

当异步模式基本时钟选择(ABCS)位或波特率发生器双速模式
串行扩展模式寄存器(SEMR)中的选择(BGDM)位在异步模式下设置为1，比特率变为表29.16中列出的值的两倍。当这两个位都设置为1时，比特率变为所列值的四倍。

Table 29.9 异步模式下不同比特率的BRR设置示例（一）

比特率(bps)	工作频率PCLK(MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

比特率(bps)	工作频率PCLK(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate quadruples.

Table 29.10 Examples of BRR settings for different bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.-
When either the ABCS bit or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate quadruples.

Table 29.11 Maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLK (MHz)	SEMR settings					Maximum bit rate (bps)	PCLK (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
8	0	0	0	0	0	250000	17.2032	0	0	0	0	0	537600
		1	0	0	0	500000			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2867200
9.8304	0	0	0	0	0	307200	18	0	0	0	0	0	562500
		1	0	0	0	614400			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	3000000
10	0	0	0	0	0	312500	19.6608	0	0	0	0	0	614400
		1	0	0	0	625000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3276800

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。当ABCS和BGDM都设置为1时，比特率翻四倍。

Table 29.10 异步模式下不同比特率的BRR设置示例（二）

比特率(bps)	工作频率PCLK(MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS位或BGDM位设置为1时，比特率加倍。
当ABCS和BGDM都设置为1时，比特率翻四倍。

Table 29.11 异步模式下每个工作频率的最大比特率（1of2）

PCLK (MHz)	SEMR settings					最大比特率(bps)	PCLK (MHz)	SEMR settings					最大比特率(bps)
	BGDM bit	ABCS 位	ABCSE bit	n	N			BGDM bit	ABCS 位	ABCSE bit	n	N	
8	0	0	0	0	0	250000	17.2032	0	0	0	0	0	537600
		1	0	0	0	500000			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2867200
9.8304	0	0	0	0	0	307200	18	0	0	0	0	0	562500
		1	0	0	0	614400			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	3000000
10	0	0	0	0	0	312500	19.6608	0	0	0	0	0	614400
		1	0	0	0	625000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3276800

Table 29.11 Maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLK (MHz)	SEMR settings					Maximum bit rate (bps)	PCLK (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
12	0	0	0	0	0	375000	20	0	0	0	0	0	625000
		1	0	0	0	750000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3333333
12.288	0	0	0	0	0	384000	25	0	0	0	0	0	781250
		1	0	0	0	768000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	4166666
14	0	0	0	0	0	437500	30	0	0	0	0	0	937500
		1	0	0	0	875000			1	0	0	0	1875000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3750000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	5000000
16	0	0	0	0	0	500000	33	0	0	0	0	0	1031250
		1	0	0	0	1000000			1	0	0	0	2062500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	2000000			1	0	0	0	4125000
	Don't care	Don't care	1	0	0	2666666		Don't care	Don't care	1	0	0	5500000
40	0	0	0	0	0	1250000							
		1	0	0	0	2500000							
	1	0	0	0	0								
		1	0	0	0	5000000							
	Don't care	Don't care	1	0	0	6666666							

Table 29.12 Maximum bit rate with external clock input in asynchronous mode (1 of 2)

		Maximum bit rate (bps)	
PCLK (MHz)	External input clock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 29.11 异步模式下每个工作频率的最大比特率（2之2）

PCLK (MHz)	SEMR settings					最大比特率(bps)	PCLK (MHz)	SEMR settings					最大比特率(bps)
	BGDM bit	ABCS 位	ABCSE bit	n	N			BGDM bit	ABCS 位	ABCSE bit	n	N	
12	0	0	0	0	0	375000	20	0	0	0	0	0	625000
		1	0	0	0	750000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3333333
12.288	0	0	0	0	0	384000	25	0	0	0	0	0	781250
		1	0	0	0	768000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	4166666
14	0	0	0	0	0	437500	30	0	0	0	0	0	937500
		1	0	0	0	875000			1	0	0	0	1875000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3750000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	5000000
16	0	0	0	0	0	500000	33	0	0	0	0	0	1031250
		1	0	0	0	1000000			1	0	0	0	2062500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	2000000			1	0	0	0	4125000
	Don't care	Don't care	1	0	0	2666666		Don't care	Don't care	1	0	0	5500000
40	0	0	0	0	0	1250000							
		1	0	0	0	2500000							
	1	0	0	0	0								
		1	0	0	0	5000000							
	Don't care	Don't care	1	0	0	6666666							

Table 29.12 异步模式下外部时钟输入的最大比特率（1of2）

		最大比特率(bps)	
PCLK (MHz)	外部输入时钟(MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 29.12 Maximum bit rate with external clock input in asynchronous mode (2 of 2)

		Maximum bit rate (bps)	
PCLK (MHz)	External input clock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
40	10.0000	625000	1250000

Table 29.13 BRR settings for different bit rates in clock synchronous and simple SPI modes

	Operating frequency PCLK (MHz)															
	8		10		16		20		25		30		33		40	
Bit rate (bps)	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																
250	3	124	—	—	3	249										
500	2	249	—	—	3	124	—	—			3	233				
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3
5 M							0	0*1	—	—	—	—	—	—	0	1
7.5 M											0	0*1				

Space: Setting prohibited.

—: Can be set, but an error will occur.

Note 1. Continuous transmission or reception is impossible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting to transmit or receive the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. Therefore, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate.

Table 29.14 Maximum bit rate with external clock input in clock synchronous and simple SPI modes

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667

Table 29.12 异步模式下外部时钟输入的最大比特率（2之2）

		最大比特率(bps)	
PCLK (MHz)	外部输入时钟(MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
40	10.0000	625000	1250000

Table 29.13 时钟同步和简单SPI模式下不同比特率的BRR设置

	工作频率PCLK(MHz)															
	8		10		16		20		25		30		33		40	
比特率(bps)	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																
250	3	124	—	—	3	249										
500	2	249	—	—	3	124	—	—			3	233				
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3
5 M							0	0*1	—	—	—	—	—	—	0	1
7.5 M											0	0*1				

空格：禁止设置。—：可以设置，但是会出错。注1。

连续发送或接收是不可能的。在发送或接收一帧数据后，在开始发送或接收下一帧数据之前会经过1位周期。同步时钟的输出停止1位周期。因此，传输一帧（8位）数据需要9位的时间，平均传输速率为89倍的位速率。

Table 29.14 时钟同步和简单SPI模式下外部时钟输入的最大比特率

PCLK (MHz)	外部输入时钟(MHz)	最大比特率(Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667

Table 29.15 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372

	Operating frequency PCLK (MHz)											
	7.1424			10.00			10.7136			13.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

	Operating frequency PCLK (MHz)											
	14.2848			16.00			18.00			20.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

	Operating frequency PCLK (MHz)											
	25.00			30.00			33.00			40.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	-12.49	0	3	5.01	0	4	-7.59	0	5	-6.66

Table 29.16 Maximum bit rate for each operating frequency in smart card interface mode, S = 32

PCLK (MHz)	Maximum bit rate (bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0
25.00	390625	0	0
30.00	468750	0	0
33.00	515625	0	0
40.00	625000	0	0

Table 29.17 BRR settings for different bit rates in simple IIC mode

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	5	4.2	1	7	-2.3
50 k	0	4	0.0	0	5	4.2	1	2	-16.7	1	2	4.2	1	3	-2.3
100 k*1	0	2	-16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	0	25	0	1	0.0	0	2	-16.7	0	2	4.2
350 k										0	1	-10.7	0	1	11.6*2
400 k*1										0	1	-21.9	0	1	-2.3*2

Bit rate (bps)	Operating frequency PCLK (MHz)								
	30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	22	1.9	1	25	-0.8	0	124	0.0
25 k	1	8	4.2	1	9	3.1	0	49	0.0
50 k	1	4	-6.3	1	4	3.1	0	24	0.0

Table 29.15 智能卡接口模式下不同比特率的BRR设置，n=0 S=372

	工作频率PCLK(MHz)											
	7.1424			10.00			10.7136			13.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

	工作频率PCLK(MHz)											
	14.2848			16.00			18.00			20.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

	工作频率PCLK(MHz)											
	25.00			30.00			33.00			40.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	-12.49	0	3	5.01	0	4	-7.59	0	5	-6.66

Table 29.16 智能卡接口模式下每个工作频率的最大比特率，S=32

PCLK (MHz)	最大比特率(bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0
25.00	390625	0	0
30.00	468750	0	0
33.00	515625	0	0
40.00	625000	0	0

Table 29.17 简单IIC模式下不同比特率的BRR设置

比特率(bps)	工作频率PCLK(MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	5	4.2	1	7	-2.3
50 k	0	4	0.0	0	5	4.2	1	2	-16.7	1	2	4.2	1	3	-2.3
100 k*1	0	2	-16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	0	25	0	1	0.0	0	2	-16.7	0	2	4.2
350 k										0	1	-10.7	0	1	11.6*2
400 k*1										0	1	-21.9	0	1	-2.3*2

比特率(bps)	工作频率PCLK(MHz)								
	30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	22	1.9	1	25	-0.8	0	124	0.0
25 k	1	8	4.2	1	9	3.1	0	49	0.0
50 k	1	4	-6.3	1	4	3.1	0	24	0.0

Bit rate (bps)	Operating frequency PCLK (MHz)								
	30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
100 k*1	1	2	-21.9	1	2	-14.1	0	12	-3.9
250 k	0	3	-6.3	0	3	3.1	0	4	0.0
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.7
400 k*1	0	2	-21.9	0	2	-14.1	0	3	-21.9

Note 1. The bit rate of 100 kbps and 400 kbps indicates the set value at which the error is on the minus side.
Note 2. The minimum value of low width is smaller than 1.3 μs which is the standard value of fast mode.

Table 29.18 Minimum widths at high and low level for SCL at different bit rates in simple IIC mode

Bit rate (bps)	Operating frequency PCLK (MHz)											
	8			10			16			20		
	n	N	Min. widths at high/low level for SCL (μs)	n	N	Min. widths at high/low level for SCL (μs)	n	N	Min. widths at high/low level for SCL (μs)	n	N	Min. widths at high/low level for SCL (μs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.38/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

Bit rate (bps)	Operating frequency PCLK (MHz)											
	25			30			33			40		
	n	N	Min. widths at high/low level for SCL (μs)	n	N	Min. widths at high/low level for SCL (μs)	n	N	Min. widths at high/low level for SCL (μs)	n	N	Min. widths at high/low level for SCL (μs)
10 k	1	19	44.80/51.20	1	22	42.93/49.60	1	25	44.12/50.42	0	124	43.75/50.00
25 k	1	7	17.92/20.48	1	8	16.80/19.20	1	9	16.97/19.39	0	49	17.50/20.00
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	4	8.48/9.70	0	24	8.75/10.00
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.82	0	12	4.55/5.20
250 k	0	2	1.68/1.92	0	3	1.86/2.13	0	3	1.70/1.94	0	4	1.75/2.00
350 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27 /1.45	0	3	1.40/1.60

Note 1. The minimum value of low width is smaller than 1.3 μs which is the standard value of fast mode. The setting values are the same as in Table 29.17.

29.2.18 Modulation Duty Register (MDDR)

Address(es): SCI0.MDDR 4007 0012h, SCI1.MDDR 4007 0032h, SCI4.MDDR 4007 0092h, SCI9.MDDR 4007 0132h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

MDDR corrects the bit rate adjusted by the BRR register.

When the BRME bit in SEMR is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected according to the settings in MDDR (M/256). Table 29.19 lists the relationship between the MDDR setting (M) and the bit rate (B).

比特率(bps)	工作频率PCLK(MHz)								
	30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
100 k*1	1	2	-21.9	1	2	-14.1	0	12	-3.9
250 k	0	3	-6.3	0	3	3.1	0	4	0.0
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.7
400 k*1	0	2	-21.9	0	2	-14.1	0	3	-21.9

注1.100kbps和400kbps的比特率表示误差在负侧的设定值。
注2.低宽度的最小值小于1.3 s，这是快速模式的标准值。

Table 29.18 简单IIC模式下不同比特率SCL的高低电平最小宽度

比特率(bps)	工作频率PCLK(MHz)											
	8			10			16			20		
	n	N	分钟。SCL高低电平宽度(μs)	n	N	分钟。SCL高低电平宽度(μs)	n	N	分钟。SCL高低电平宽度(μs)	n	N	分钟。SCL高低电平宽度(μs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.38/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

比特率(bps)	工作频率PCLK(MHz)											
	25			30			33			40		
	n	N	分钟。SCL高低电平宽度(μs)	n	N	分钟。SCL高低电平宽度(μs)	n	N	分钟。SCL高低电平宽度(μs)	n	N	分钟。SCL高低电平宽度(μs)
10 k	1	19	44.80/51.20	1	22	42.93/49.60	1	25	44.12/50.42	0	124	43.75/50.00
25 k	1	7	17.92/20.48	1	8	16.80/19.20	1	9	16.97/19.39	0	49	17.50/20.00
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	4	8.48/9.70	0	24	8.75/10.00
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.82	0	12	4.55/5.20
250 k	0	2	1.68/1.92	0	3	1.86/2.13	0	3	1.70/1.94	0	4	1.75/2.00
350 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27 /1.45	0	3	1.40/1.60

注1.低宽度的最小值小于1.3 s，这是快速模式的标准值。设定值与表29.17相同。

29.2.18 调制占空比寄存器(MDDR)

Address(es): SCI0.MDDR 4007 0012h, SCI1.MDDR 4007 0032h, SCI4.MDDR 4007 0092h, SCI9.MDDR 4007 0132h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1

MDDR校正由BRR寄存器调整的比特率。

当SEMR中的BRME位设置为1时，片内波特率发生器产生的比特率根据MDDR（M256）中的设置进行均匀校正。表29.19列出了MDDR设置(M)和比特率(B)之间的关系。

The initial value of MDDR is FFh. Bit [7] in this register is fixed to 1.

The CPU can read the MDDR register, but this register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 29.19 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

Mode	SEMR settings BGDM bit	ABCS bit	ABCSE bit	BRR setting	Error
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	

B: Bit rate (bps).
M: MDDR setting (128 ≤ MDDR ≤ 255).
N: BRR setting for baud rate generator (0 ≤ N ≤ 255).
PCLK: Operating frequency (MHz).
n and S: Determined by the settings of the SMR/SMR_SMCI and SCMR registers as listed in Table 29.7 and Table 29.8. See section 29.2.17, Bit Rate Register (BRR) for details.
Note 1. Do not use this function in clock synchronous mode or in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the I^2C standard.

Table 29.20 lists examples of N settings in BRR and M settings in MDDR in asynchronous mode.

Table 29.20 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (1)

Bit rate (bps)	Operating frequency PCLK (MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	–0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

MDDR的初始值为FFh。该寄存器中的位[7]固定为1。

CPU可以读取MDDR寄存器，但该寄存器只有在SCRSCR_SMCI中的TE和RE位为0时才可写。

Table 29.19 使用比特率调制功能时MDDR设置(M)和比特率(B)的关系

Mode	SEMR settings BGDM bit	ABCS 位	ABCSE bit	BRR setting	Error
异步、多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
时钟同步，简单SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error(\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	

B：比特率（bps）。
M: MDDR setting (128 ≤ MDDR ≤ 255).
N：波特率发生器的BRR设置(0≤N≤255)。
PCLK：工作频率（MHz）。n和S：由表29.7和表29.8中列出的SMRSMR_SMCI和SCMR寄存器的设置决定。有关详细信息，请参见第29.2.17节，比特率寄存器(BRR)。注1。

请勿在时钟同步模式或简单SPI模式的最高速度设置中使用此功能（SMR.CKS[1:0]=00b，SCR.CKE[1] = 0, and BRR = 0).
Note 2. 调整码率，使简单IIC模式下SCLn输出的高低电平宽度满足I2C标准。

表29.20列出了异步模式下BRR中的N设置和MDDR中的M设置的示例。

Table 29.20 异步模式下不同比特率的BRR和MDDR设置示例(1)

比特率(bps)	工作频率PCLK(MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	–0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Bit rate (bps)	Operating frequency PCLK (MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	–0.17	0	2	202	1	–0.11
460800	0	0	157	1	–0.18	0	0	154	1	–0.26	0	0	135	1	0.14

Bit rate (bps)	Operating frequency PCLK (MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	–0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	–0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	–0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	–0.20	0	0	210	0	0.14

Bit rate (bps)	Operating frequency PCLK (MHz)														
	19.6608					20					25				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	–0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

Bit rate (bps)	Operating frequency PCLK (MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	–0.01
57600	0	10	173	0	–0.01	0	9	143	0	0.01	0	38	230	1	–0.01
115200	0	10	173	1	–0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	–0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Note 1. In this example, the ABCS and ABCSE bits in SEMR are 0.
SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

29.2.19 Serial Extended Mode Register (SEMR)

Address(es): SCI0.SEMR 4007 0007h, SCI1.SEMR 4007 0027h, SCI4.SEMR 4007 0087h, SCI9.SEMR 4007 0127h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	BRME	Bit Rate Modulation Enable	0: Bit rate modulation function is disabled 1: Bit rate modulation function is enabled.	R/W*1

比特率(bps)	工作频率PCLK(MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	–0.17	0	2	202	1	–0.11
460800	0	0	157	1	–0.18	0	0	154	1	–0.26	0	0	135	1	0.14

比特率(bps)	工作频率PCLK(MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	–0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	–0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	–0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	–0.20	0	0	210	0	0.14

比特率(bps)	工作频率PCLK(MHz)														
	19.6608					20					25				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	–0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

比特率(bps)	工作频率PCLK(MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	–0.01
57600	0	10	173	0	–0.01	0	9	143	0	0.01	0	38	230	1	–0.01
115200	0	10	173	1	–0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	–0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Note 1. 在本例中，SEMR中的ABCS和ABCSE位为0。
SEMR.BRME=0(M=256)禁用比特率调制功能。

29.2.19 串行扩展模式寄存器(SEMR)

Address(es): SCI0.SEMR 4007 0007h, SCI1.SEMR 4007 0027h, SCI4.SEMR 4007 0087h, SCI9.SEMR 4007 0127h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	BRME	比特率调制 Enable	0：码率调制功能关闭1：码率调制功能开启。	R/W*1

Bit	Symbol	Bit name	Description	R/W
b3	ABCSE	Asynchronous Mode Extended Base Clock Select 1	Valid only in asynchronous mode with SCR.CKE[1] = 0: 0: Clock cycle number for 1-bit period is determined with combination of BGDM and ABCS in SEMR 1: Baud rate is 6 base clock cycles for 1-bit period.	R/W*1
b4	ABCS	Asynchronous Mode Base Clock Select	Valid only in asynchronous mode: 0: Selects 16 base clock cycles for 1-bit period 1: Selects 8 base clock cycles for 1-bit period.	R/W*1
b5	NFEN	Digital Noise Filter Function Enable	In asynchronous mode: 0: Noise cancellation function for the RXDn input signal is disabled 1: Noise cancellation function for the RXDn input signal is enabled. In simple IIC mode: 0: Noise cancellation function for the SCLn and SDAn input signals is disabled 1: Noise cancellation function for the SCLn and SDAn input signals is enabled. The NFEN bit must be 0 in all other modes.	R/W*1
b6	BGDM	Baud Rate Generator Double-Speed Mode Select	Valid only in asynchronous mode with SCR.CKE[1] = 0: 0: Baud rate generator outputs the clock with single frequency 1: Baud rate generator outputs the clock with double frequency.	R/W*1
b7	RXDESEL	Asynchronous Start Bit Edge Detection Select	Valid only in asynchronous mode: 0: A low level on the RXDn pin is detected as the start bit 1: A falling edge on the RXDn pin is detected as the start bit.	R/W*1

Note 1. Writable only when TE in SCR/SCR_SMCI = 0 and RE in SCR/SCR_SMCI = 0 (both serial transmission and reception are disabled).

SEMR selects the clock source for 1-bit period in asynchronous mode.

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables and disables the bit rate modulation function. The bit rate generated by on-chip baud rate generator is evenly corrected when this function is enabled.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The pulse number for a base clock at 1-bit period is 6 and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use the ABCSE bit and set SMR.CKS[1:0] = 00b and BRR = 0. Set this bit to 0 except in asynchronous mode.

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the clock cycles for a 1-bit period. Set this bit to 0 except in asynchronous mode.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the digital noise filter function is enabled:

- Noise cancellation is applied to the RXDn input signal in asynchronous mode
- Noise cancellation is applied to the SDAn and SCLn input signals in simple IIC mode.

In all other modes, set the NFEN bit to 0 to disable the digital noise filter function.

When the digital noise filter function is disabled, input signals are transferred as received.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects the cycle of output clock for the baud rate generator to be either single or double frequency.

The BGDM bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0). For the clock output from the baud rate generator, either normal or doubled frequency can be selected. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode.

Bit	Symbol	位名称	Description	R/W
b3	ABCSE	异步模式扩展基本时钟 Select 1	仅在SCR.CKE[1]=0的异步模式下有效：0：1位周期的时钟周期数由SEMR中的BGDM和ABCS组合确定1：波特率为1位周期的6个基本时钟周期。	R/W*1
b4	ABCS	异步模式 基本时钟选择	仅在异步模式下有效：0：为1位周期选择16个基本时钟周期1：为1位周期选择8个基本时钟周期。	R/W*1
b5	NFEN	数字噪声滤波器 功能启用	在异步模式下：0：禁用RXDn输入信号的噪声消除功能1：启用RXDn输入信号的噪声消除功能。在简单IIC模式下：0：禁用SCLn和SDAn输入信号的噪声消除功能1：启用SCLn和SDAn输入信号的噪声消除功能。在所有其他模式下，NFEN位必须为0。	R/W*1
b6	BGDM	波特率发生器双速模式 Select	仅在SCR.CKE[1]=0的异步模式下有效：0：波特率发生器输出单频时钟1：波特率发生器输出双频时钟。	R/W*1
b7	RXDESEL	异步起始位边沿检测选择	仅在异步模式下有效：0：RXDn引脚上的低电平被检测为起始位1：RXDn引脚上的下降沿被检测为起始位。	R/W*1

Note 1. 仅当SCRSCR_SMCI=0中的TE和SCRSCR_SMCI=0中的RE时才可写（串行传输和接收都被禁用）。

SEMR在异步模式下选择1位周期的时钟源。

BRME位（比特率调制使能）

BRME位启用和禁用比特率调制功能。该功能使能时，片内波特率发生器产生的比特率得到均匀校正。

ABCSE位（异步模式扩展基本时钟选择1）

1位周期的基本时钟脉冲数为6，双频时钟由波特率发生器输出。当比特率设置为6并同时分频总线时钟频率时，使用ABCSE位并设置SMR.CKS[1:0]=00b和BRR=0。除异步模式外，将此位设置为0。

ABCS位（异步模式基本时钟选择）

ABCS位选择1位周期的时钟周期。除异步模式外，将此位设置为0。

NFEN位（数字噪声滤波器功能使能）

NFEN位启用或禁用数字噪声滤波器功能。

启用数字噪声滤波器功能时：

- 噪声消除应用于异步模式下的RXDn输入信号
- 噪声消除应用于简单IIC模式下的SDAn和SCLn输入信号。

在所有其他模式下，将NFEN位设置为0以禁用数字噪声滤波器功能。

当数字噪声滤波器功能被禁用时，输入信号按接收到的方式传输。

BGDM位（波特率发生器双速模式选择）

BGDM位选择波特率发生器的输出时钟周期为单频或双频。

当在异步模式（SMR.CM=0）下选择片内波特率发生器作为时钟源（SCR.CKE[1]=0）时，BGDM位有效。对于波特率发生器的时钟输出，可选择正常频率或倍频。基本时钟由波特率发生器的时钟输出生成。当BGDM位设置为1时，基本时钟周期减半，比特率加倍。

在异步模式以外的模式下将此位设置为0。

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDESEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, set this bit to 1 to stop reception, or to start reception without retaining the RXDn pin input at high level for the period of one data frame or longer after completion of the break.

Set this bit to 0 in modes other than asynchronous mode.

29.2.20 Noise Filter Setting Register (SNFR)

Address(es): SCI0.SNFR 4007 0008h, SCI1.SNFR 4007 0028h, SCI4.SNFR 4007 0088h, SCI9.SNFR 4007 0128h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	NFCS[2:0]	Noise Filter Clock Select	In asynchronous mode, the standard setting for the base clock is as follows: b2 b0 0 0 0: The clock signal divided by 1 is used with the noise filter. In simple IIC mode, the standard settings for the clock source of the on-chip baud rate generator selected by the SMR.CKS[1:0] bits are as follows: b2 b0 0 0 1: The clock signal divided by 1 is used with the noise filter 0 1 0: The clock signal divided by 2 is used with the noise filter 0 1 1: The clock signal divided by 4 is used with the noise filter 1 0 0: The clock signal divided by 8 is used with the noise filter. Other settings are prohibited.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple IIC mode, set the bits to a value in the range from 001b to 100b.

29.2.21 I2C Mode Register 1 (SIMR1)

Address(es): SCI0.SIMR1 4007 0009h, SCI1.SIMR1 4007 0029h, SCI4.SIMR1 4007 0089h, SCI9.SIMR1 4007 0129h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICM	Simple IIC Mode Select	SMIF IICM 0 0: Asynchronous mode, multi-processor mode, clock synchronous mode, or simple SPI mode 0 1: Simple IIC mode 1 0: Smart card interface mode 1 1: Setting prohibited.	R/W*1

RXDESEL位（异步起始位边沿检测选择）

RXDESEL位选择异步模式下接收起始位的检测方法。当发生中断时，将该位设置为1以停止接收，或在中断完成后不将RXDn引脚输入保持高电平的情况下开始接收1个数据帧或更长时间。

在异步模式以外的模式下将此位设置为0。

29.2.20 噪声滤波器设置寄存器(SNFR)

Address(es): SCI0.SNFR 4007 0008h, SCI1.SNFR 4007 0028h, SCI4.SNFR 4007 0088h, SCI9.SNFR 4007 0128h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	NFCS[2:0]	噪声滤波器时钟选择	在异步模式下，基准时钟的标准设置如下：b2b0000：时钟信号除以1与噪声滤波器一起使用。 在简单IIC模式下，SMR.CKS[1:0]位选择的片内波特率发生器时钟源的标准设置如下：b2b0001：使用时钟信号除以1带噪声滤波器010：时钟信号除以2与噪声滤波器一起使用011：时钟信号除以4与噪声滤波器一起使用100：时钟信号除以8与噪声滤波器一起使用噪声滤波器。禁止其他设置。	R/W*1
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只有当SCRSCR_SMCI中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SNFR寄存器设置数字噪声滤波器时钟。

NFCS[2:0]位（噪声滤波器时钟选择）

NFCS[2:0]位选择数字噪声滤波器的采样时钟。要在异步模式下使用噪声滤波器，请将这些位设置为000b。在简单IIC模式下，将位设置为001b到100b范围内的值。

29.2.21 I2C模式寄存器1(SIMR1)

Address(es): SCI0.SIMR1 4007 0009h, SCI1.SIMR1 4007 0029h, SCI4.SIMR1 4007 0089h, SCI9.SIMR1 4007 0129h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IICM	简单IIC模式选择	SMIFIICM00：异步模式、多处理器模式、时钟同步模式或简单SPI模式01：简单IIC模式10：智能卡接口模式11：禁止设置。	R/W*1

Bit	Symbol	Bit name	Description	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b3	IICDL[4:0]	SDA Delay Output Select	The following cycles are of the clock signal from the on-chip baud rate generator: b7 b3 0 0 0 0 0: No output delay 0 0 0 0 1: 0 to 1 cycle 0 0 0 1 0: 1 to 2 cycles 0 0 0 1 1: 2 to 3 cycles 0 0 1 0 0: 3 to 4 cycles 0 0 1 0 1: 4 to 5 cycles : : 1 1 1 1 0: 29 to 30 cycles 1 1 1 1 1: 30 to 31 cycles.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

SIMR1 selects simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SMIF bit in SCMR, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDA Delay Output Select)

The IICDL[4:0] bits set a delay for output on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLK by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set these bits to 00000b unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

29.2.22 I²C Mode Register 2 (SIMR2)

Address(es): SCI0.SIMR2 4007 000Ah, SCI1.SIMR2 4007 002Ah, SCI4.SIMR2 4007 008Ah, SCI9.SIMR2 4007 012Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICINTM	I²C Interrupt Mode Select	0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts.	R/W*1
b1	IICCSC	Clock Synchronization	0: No synchronization with the clock signal 1: Synchronization with the clock signal.	R/W*1
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	IICACKT	ACK Transmission Data	0: ACK transmission 1: NACK transmission and reception of ACK/NACK.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (serial reception and transmission disabled).

SIMR2 selects how reception and transmission are controlled in simple IIC mode.

IICINTM bit (I²C Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 to synchronize the internally generated SCLn clock signal when the SCLn pin is driven low

Bit	Symbol	位名称	Description	R/W
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7 to b3	IICDL[4:0]	SDA延迟输出选择	以下周期是来自片内波特率发生器的时钟信号：b7b300000：无输出延迟00001：0到1个周期00010：1到2个周期00011：2到3个循环00100：3到4个循环00101：4到5个循环::11110：29到30个循环11111：30到31个循环.	R/W*1

Note 1. 只有当SCR中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

SIMR1选择简单IIC模式和SDAn输出的延迟级数。

IICM位（简单IIC模式选择）

IICM位结合SCMR中的SMIF位选择工作模式。

IICDL[4:0]位（SDA延迟输出选择）

IICDL[4:0]位设置SDAn引脚输出相对于SCLn引脚输出下降沿的延迟。

可用的延迟设置范围从无延迟到31个周期，以来自片上波特率发生器的时钟信号为基准。通过在SMR.CKS[1:0]中设置的除数对PCLK进行分频获得的信号作为来自片上波特率发生器的时钟信号提供。除非在简单IIC模式下操作，否则将这些位设置为00000b。在简单IIC模式下，将位设置为00001b到11111b范围内的值。

29.2.22 I2C模式寄存器2(SIMR2)

Address(es): SCI0.SIMR2 4007 000Ah, SCI1.SIMR2 4007 002Ah, SCI4.SIMR2 4007 008Ah, SCI9.SIMR2 4007 012Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IICINTM	I2C中断模式选择	0：使用ACKNACK中断1：使用接收和发送中断。	R/W*1
b1	IICCSC	时钟同步	0：与时钟信号不同步1：与时钟信号同步。	R/W*1
b4 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	IICACKT	ACK传输数据	0：ACK发送1：NACK发送和接收ACKNACK。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只有当SCR中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SIMR2选择在简单IIC模式下如何控制接收和发送。

IIICTM位（I2C中断模式选择）

IICINTM位选择简单IIC模式下的中断请求源。

IICCSC位（时钟同步）

当SCLn引脚驱动为低电平时，将IICCSC位设置为1以同步内部生成的SCLn时钟信号

because of a wait inserted by another device, for example.

The SCLn clock signal is not synchronized if this bit is 0. The SCLn clock signal is generated according to the rate selected in the BRR regardless of the level input on the SCLn pin.

Set this bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

The IICACKT bit transmits data that contains ACK bits. Set this bit to 1 when ACK and NACK bits are received.

29.2.23 I²C Mode Register 3 (SIMR3)

Address(es): SCI0.SIMR3 4007 000Bh, SCI1.SIMR3 4007 002Bh, SCI4.SIMR3 4007 008Bh, SCI9.SIMR3 4007 012Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTP REQ	IICRST AREQ	IICSTA REQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICSTAREQ	Start Condition Generation	0: A start condition is not generated 1: A start condition is generated.*1, *3, *5, *6	R/W
b1	IICRSTAREQ	Restart Condition Generation	0: A restart condition is not generated 1: A restart condition is generated.*2, *3, *5, *6	R/W
b2	IICSTPREQ	Stop Condition Generation	0: A stop condition is not generated 1: A stop condition is generated.*2, *3, *5, *6	R/W
b3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag	0: There are no requests for generating conditions or a condition is being generated 1: A start, restart, or stop condition is completely generated. When 0 is written to IICSTIF, it is set to 0.*4	R/W*4
b5, b4	IICSDAS[1:0]	SDA Output Select	b5 b4 0 0: Serial data output 0 1: Generate start, restart, or stop condition 1 0: Output low level on SDAn pin 1 1: Drive SDAn pin to high-impedance state.	R/W
b7, b6	IICSCLS[1:0]	SCL Output Select	b7 b6 0 0: Serial clock output 0 1: Generate a start, restart, or stop condition 1 0: Output low level on SCLn pin 1 1: Drive SCLn pin to high-impedance state.	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that it is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that it is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- When generation of a start condition is complete.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b and set the

例如，由于另一个设备插入了等待。

如果该位为0，则SCLn时钟信号不同步。SCLn时钟信号根据BRR中选择的速率生成，与SCLn引脚上的输入电平无关。

除调试期间外，将此位设置为1。

IICACKT位（ACK传输数据）

IICACKT位发送包含ACK位的数据。当收到ACK和NACK位时，将该位设置为1。

29.2.23 I2C模式寄存器3(SIMR3)

Address(es): SCI0.SIMR3 4007 000Bh, SCI1.SIMR3 4007 002Bh, SCI4.SIMR3 4007 008Bh, SCI9.SIMR3 4007 012Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTP REQ	IICRST AREQ	IICSTA REQ
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IICSTAREQ	开始条件生成	0：不产生启动条件1：产生启动条件。 1、*3、*5、*6	R/W
b1	IICRSTAREQ	重启条件 Generation	0：不产生重启条件1：产生重启条件。*2，*3，*5，*6	R/W
b2	IICSTPREQ	停止条件生成	0：不产生停止条件1：产生停止条件。*2、*3、*5、*6	R/W
b3	IICSTIF	发出启动、重启或停止条件已完成 Flag	0：没有条件生成请求或正在生成条件1：启动、重新启动或停止条件已完全生成。当0写入IICSTIF时，设置为0.*4	R/W*4
b5, b4	IICSDAS[1:0]	SDA输出选择	b5b400：串行数据输出01：产生启动、重启或停止条件10：SDAn引脚1输出低电平1：驱动SDAn引脚为高阻抗状态。	R/W
b7, b6	IICSCLS[1:0]	SCL输出选择	b7b600：串行时钟输出01：产生启动、重启或停止条件10：在SCLn引脚1上输出低电平1：驱动SCLn引脚为高阻状态。	R/W

Note 1. 仅在检查总线状态并确认其空闲后才生成启动条件。
Note 2. 在检查总线状态并确认其繁忙后生成重新启动或停止条件。
Note 3. 在给定时间，不要将IICSTAREQ、IICRSTAREQ和IICSTPREQ位中的一个以上设置为1。
Note 4. 仅写入0。写入1时，忽略该值。
Note 5. 在IICSTIF标志的值为0后执行条件的生成。
Note 6. 请勿在该位为1时向其写入0。当该位为1时，向该位写入0可暂停条件的生成。

IICSTAREQ位（开始条件生成）

当要生成启动条件时，除了将IICSTAREQ位设置为1之外，将IICSDAS[1:0]和IICSCLS[1:0]位都设置为01b。

[Setting condition]

- 向该位写入1。

[Clearing condition]

- 当开始条件的生成完成时。

IICRSTAREQ位（重启条件生成）

当要产生重启条件时，将IICSDAS[1:0]和IICSCLS[1:0]位都设置为01b并将

IICRSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- When generation of a restart condition is complete.

IICSTPREQ bit (Stop Condition Generation

When a stop condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b and set the IICSTPREQ bit to 1.

[Setting condition]

- Writing 1 to the bit.

[Clearing condition]

- When generation of a stop condition is complete.

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 when an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- When generation of a start, restart, or stop condition completes. If this conflicts with any of the clearing conditions for the flag, the clearing condition takes precedence.

[Clearing conditions]

- Writing 0 to the bit then, confirm that the IICSTIF flag is 0
- Writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode
- Writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDA Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin.

Set the IICSDAS[1:0] and IICSCLS[1:0] bits to the same value.

IICSCLS[1:0] bits (SCL Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin.

Set the IICSCLS[1:0] and IICSDAS[1:0] bits to the same value.

29.2.24 I²C Status Register (SISR)

Address(es): SCI0.SISR 4007 000Ch, SCI1.SISR 4007 002Ch, SCI4.SISR 4007 008Ch, SCI9.SISR 4007 012Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IICACKR	ACK Reception Data Flag	0: ACK received 1: NACK received.	R
b1	—	Reserved	This bit is read as 0	R

IICRSTAREQ位为1。

[Setting condition]

- 向该位写入1。

[Clearing condition]

- 当重新启动条件的生成完成时。

IICSTPREQ位（停止条件生成

当要产生停止条件时，将IICSDAS[1:0]和IICSCLS[1:0]位都设置为01b并将IICSTPREQ位为1。

[Setting condition]

- 向该位写入1。

[Clearing condition]

- 当停止条件的生成完成时。

IICSTIF标志（发出启动、重启或停止条件完成标志）

生成条件后，IICSTIF标志指示生成完成。使用IICSTAREQ时，IICRSTAREQ或IICSTPREQ位会导致条件生成，在将IICSTIF标志设置为0后执行此操作。

当通过设置SCR.TEIE位使能中断请求时IICSTIF标志为1时，输出STI请求。

[Setting condition]

- 当启动、重新启动或停止条件的生成完成时。如果这与标志的任何清除条件相冲突，则清除条件优先。

[Clearing conditions]

- 然后将0写入该位，确认IICSTIF标志为0
- 非简单IIC模式下向SIMR1.IICM位写入0
- 将0写入SCR.TE位。

IICSDAS[1:0]位（SDA输出选择）

IICSDAS[1:0]位控制SDAn引脚的输出。

将IICSDAS[1:0]和IICSCLS[1:0]位设置为相同的值。

IICSCLS[1:0]位（SCL输出选择）

IICSCLS[1:0]位控制SCLn引脚的输出。

将IICSCLS[1:0]和IICSDAS[1:0]位设置为相同的值。

29.2.24 I2C状态寄存器(SISR)

Address(es): SCI0.SISR 4007 000Ch, SCI1.SISR 4007 002Ch, SCI4.SISR 4007 008Ch, SCI9.SISR 4007 012Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
重置后的值：	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	IICACKR	ACK接收数据标志	0：收到ACK1：收到NACK。	R
b1	—	Reserved	该位读为0	R

Bit	Symbol	Bit name	Description	R/W
b2	—	Reserved	The read value is undefined	R
b3	—	Reserved	This bit is read as 0	R
b5, b4	—	Reserved	The read values are undefined	R
b7, b6	—	Reserved	These bits are read as 0	R

SISR monitors the state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. This flag is updated on the rising edge of the SCLn clock for the ACK/NACK receiving bit.

29.2.25 SPI Mode Register (SPMR)

Address(es): SCI0.SPMR 4007 000Dh, SCI1.SPMR 4007 002Dh, SCI4.SPMR 4007 008Dh, SCI9.SPMR 4007 012Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSE	SSn Pin Function Enable	0: SSn pin function is disabled 1: SSn pin function is enabled.	R/W*1
b1	CTSE	CTS Enable	0: CTS function is disabled (RTS output function is enabled) 1: CTS function is enabled.	R/W*1
b2	MSS	Master Slave Select	0: Transmission is through the TXDn pin and reception is through the RXDn pin (master mode) 1: Reception is through the TXDn pin and transmission is through the RXDn pin (slave mode).	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MFF	Mode Fault Flag	0: No mode fault error 1: Mode fault error.	R/W*2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CKPOL	Clock Polarity Select	0: Clock polarity is not inverted 1: Clock polarity is inverted.	R/W*1
b7	CKPH	Clock Phase Select	0: Clock is not delayed 1: Clock is delayed.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).
Note 2. Only 0 can be written to these bits, to clear the flag.

SPMR selects the extension settings in asynchronous and clock synchronous modes.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 to use the SSn pin to control transmission and reception in simple SPI mode. Set this bit to 0 in all other modes. When master mode (SCR.CKE[1:0] = 00b and MSS = 0) is selected and there is a single master, the SSn pin on the master side is not required to control reception and transmission. In such a case, set the SSE bit to 0. Do not enable both the SSE and CTSE bits as the operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 to use the SSn pin to input the CTS control signal to control transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to 1 as the operation is the same as that when these bits are set to 0.

Bit	Symbol	位名称	Description	R/W
b2	—	Reserved	读取值未定义	R
b3	—	Reserved	该位读为0	R
b5, b4	—	Reserved	读取的值未定义	R
b7, b6	—	Reserved	这些位被读为0	R

SISR在简单IIC模式下监控状态。

IICACKR标志（ACK接收数据标志）

接收到的ACK和NACK位可以从IICACKR标志中读取。该标志在ACKNACK接收位的SCLn时钟的上升沿更新。

29.2.25 SPI模式寄存器(SPMR)

Address(es): SCI0.SPMR 4007 000Dh, SCI1.SPMR 4007 002Dh, SCI4.SPMR 4007 008Dh, SCI9.SPMR 4007 012Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SSE	SSn引脚功能使能	0：禁用SSn引脚功能1：启用SSn引脚功能。	R/W*1
b1	CTSE	CTS Enable	0：CTS功能无效（RTS输出功能有效）1：CTS功能有效。	R/W*1
b2	MSS	主从选择	0：通过TXDn引脚发送，通过RXDn引脚接收（主模式）1：通过TXDn引脚接收，通过RXDn引脚发送（从模式）。	R/W*1
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	MFF	模式故障标志	0：无模式故障错误1：模式故障错误。	R/W*2
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	CKPOL	时钟极性选择	0：时钟极性不反转1：时钟极性反转。	R/W*1
b7	CKPH	时钟相位选择	0：时钟不延迟1：时钟延迟。	R/W*1

Note 1. 只有当SCR中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

Note 2. 只能将0写入这些位，以清除标志。

SPMR在异步和时钟同步模式下选择扩展设置。

SSE位（SSn引脚功能使能）

将SSE位设置为1以使用SSn引脚控制简单SPI模式下的发送和接收。在所有其他模式下将此位设置为0。Whenmastermode(SCR.CKE[1:0]=00bandMSS=0)isselectedandthereisasinglemaster theSSnpinonthemastersideisnotrequiredtocontrolreceptionandtransmission.在这种情况下，请将SSE位设置为0。不要同时启用SSE和CTSE位，因为这些位设置为0时的操作相同。

CTSE位（CTS使能）

将CTSE位设置为1以使用SSn引脚输入CTS控制信号来控制发送和接收。当该位设置为0时输出RTS信号。在智能卡接口模式、简单SPI模式和简单IIC模式下将该位设置为0。不要将CTSE和SSE位都设置为1，因为操作与将这些位设置为0时的操作相同。

MSS bit (Master Slave Select)

The MSS bit selects between master and slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when the MSS bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin. Set this bit to 0 in modes other than simple SPI mode.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading this flag.

[Setting condition]

- When input on the SSn pin is low during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- Writing 0 to the flag after it is read as 1.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 29.70 for details.

Set the bit to 0 in modes other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 29.70 for details.

Set the bit to 0 in modes other than simple SPI and clock synchronous modes.

29.2.26 FIFO Control Register (FCR)

Address(es): SCI0.FCR 4007 0014h, SCI1.FCR 4007 0034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FM	FIFO Mode Select	Valid only in asynchronous mode, including multi-processor, or clock synchronous mode: 0: Non-FIFO mode Selects TDR/RDR or TDRHL/RDRHL for communication 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1
b1	RFRST	Receive FIFO Data Register Reset	Valid only when FCR.FM = 1: 0: Do not reset FRDRHL 1: Reset FRDRHL.	R/W
b2	TFRST	Transmit FIFO Data Register Reset	Valid only when FCR.FM = 1: 0: Do not reset FTDRHL 1: Reset FTDRHL.	R/W
b3	DRES	Receive Data Ready Error Select Bit	When detecting a receive data ready, the interrupt request is selected: 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI).	R/W
b7 to b4	TTRG[3:0]	Transmit FIFO Data Trigger Number	Valid only in asynchronous mode, including multi-processor, or clock synchronous mode: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W

MSS位（主从选择）

MSS位在简单SPI模式下选择主从操作。当MSS位设置为1时，TXDn和RXDn引脚的功能相反，因此数据通过TXDn引脚接收并通过RXDn引脚发送。在简单SPI模式以外的模式下将此位设置为0。

MFF标志（模式故障标志）

MFF标志指示模式故障错误。在多主机配置中，通过读取该标志确定模式故障错误发生。

[Setting condition]

- 在简单SPI模式（SSE位=1和MSS位=0）下主机操作期间SSn引脚上的输入为低电平时。

[Clearing condition]

- 读为1后将0写入标志。

CKPOL位（时钟极性选择）

CKPOL位选择通过SCKn引脚输出的时钟信号的极性。详见图29.70。

在简单SPI模式和时钟同步模式以外的模式下将该位设置为0。

CKPH位（时钟相位选择）

CKPH位选择通过SCKn引脚输出的时钟信号的相位。详见图29.70。

在简单SPI和时钟同步模式以外的模式下将该位设置为0。

29.2.26 先进先出控制寄存器(FCR)

Address(es): SCI0.FCR 4007 0014h, SCI1.FCR 4007 0034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
重置后的值：	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FM	先进先出模式选择	仅在异步模式下有效，包括多处理器，或时钟同步模式：0：非FIFO模式 选择TDRRDR或TDRHLRDRHL进行通信1：FIFO模式。 选择FTDRHLFRDRHL进行通信。	R/W*1
b1	RFRST	接收FIFO数据寄存器Reset	仅在FCR.FM=1时有效：0： 不复位FRDRHL1：复位FRDRHL。	R/W
b2	TFRST	发送FIFO数据注册重置	仅当FCR.FM=1时有效：0： 不复位FTDRHL1：复位FTDRHL。	R/W
b3	DRES	接收数据就绪错误选择位	当检测到接收数据就绪时，选择中断请求：0：接收数据满中断（SCIn_RXI）1：接收错误中断（SCIn_ERI）。	R/W
b7 to b4	TTRG[3:0]	发送FIFO数据触发Number	仅在异步模式（包括多处理器）或时钟同步模式下有效：0000：触发编号0:1111：触发编号15。	R/W

Bit	Symbol	Bit name	Description	R/W
b11 to b8	RTRG[3:0]	Receive FIFO Data Trigger Number	Valid only in asynchronous mode, including multi-processor, or clock synchronous mode: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W
b15 to b12	RSTRG[3:0]	RTS Output Active Trigger Number Select	Valid only in asynchronous mode, including multi-processor, or clock synchronous mode, while FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

FCR selects FIFO mode, resets FTDRHL/FRDRHL, selects the FIFO data trigger number of transmission or reception, and selects the RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR, or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

The FRDRHL register is reset when the RFRST bit is set to 1, and the receive data count is reset to 0. After writing 1, this bit is set to 0 after 1 PCLK.

TFRST bit (Transmit FIFO Data Register Reset)

The FTDRHL register is reset when the TFRST bit is set to 1, and the transmit data count is reset to 0. After writing 1, this bit is set to 0 after 1 PCLK.

DRES bit (Receive Data Ready Error Select Bit)

On detecting a receive data ready error, the DRES bit selects the interrupt request from an SCIn_RXI interrupt request or an SCIn_ERI interrupt request. Set the DRES bit to 1 when starting the DMAC or DTC and reading the FRDRH and FRDRL registers.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in the Transmit FIFO Data Register (FTDRHL) is equal to or less than the specified transmit triggering number, and software can write data to FTDRHL. If SCR.TIE = 1, SCIn_TXI interrupt request occurred.

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in the Receive FIFO Data Register (FRDRHL) is equal to or greater than the specified receive triggering number, and software can read data from FRDRHL. If SCR.RIE = 1, SCIn_RXI interrupt request occurred. When RTRG[3:0] is set to 0, the RDF flag is not set even when the amount of the data in the receive FIFO is equal to 0. Additionally, an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in the Receive FIFO Data Register (FRDRHL) is equal to or greater than the specified receive triggering number, the RTS signal goes high. When RSTRG[3:0] is set to 0, the RTS signal does not go high even when the amount of data in the receive FIFO is equal to 0.

Bit	Symbol	位名称	Description	R/W
b11 to b8	RTRG[3:0]	接收FIFO数据触发Number	仅在异步模式（包括多处理器）或时钟同步模式下有效：0000：触发编号0:1111：触发编号15。	R/W
b15 to b12	RSTRG[3:0]	RTS输出有源触发号码选择	仅在异步模式下有效，包括多处理器或时钟同步模式，同时FCR.FM=1，SPMR.CTSE=0，和SPMR.SSE=0：0000：触发编号0：1111：触发编号15。	R/W

Note 1. 仅当TE=0且RE=0时可写。

FCR选择FIFO模式，复位FTDRHLFRDRHL，选择发送或接收的FIFO数据触发数，选择RTS输出激活触发数。

FM位（FIFO模式选择）

当FM位设置为1时，选择FTDRHL和FRDRHL进行通信。当FM位设置为0时，选择TDR和RDR，或TDRHL和RDRHL进行通信。

RFRST位（接收FIFO数据寄存器复位）

当RFRST位设置为1时，FRDRHL寄存器复位，接收数据计数复位为0。写入1后，该位在1个PCLK后设置为0。

TFRST位（发送FIFO数据寄存器复位）

当TFRST位设置为1时，FTDRHL寄存器复位，发送数据计数复位为0。写入1后，该位在1个PCLK后设置为0。

DRES位（接收数据就绪错误选择位）

检测到接收数据就绪错误时，DRES位从SCIn_RXI中断请求或SCIn_ERI中断请求中选择中断请求。启动DMAC或DTC并读取FRDRH和FRDRL寄存器时，将DRES位设置为1。

TTRG[3:0]位（发送FIFO数据触发数）

当发送FIFO数据寄存器(FTDRHL)中的发送数据量等于或小于指定的发送触发数时，TDFE标志设置为1，并且软件可以将数据写入FTDRHL。如果SCR.TIE=1，则发生SCIn_TXI中断请求。

RTRG[3:0]位（接收FIFO数据触发数）

当接收FIFO数据寄存器(FRDRHL)中的接收数据量等于或大于指定的接收触发数时，RDF标志设置为1，并且软件可以从FRDRHL中读取数据。如果SCR.RIE=1，则发生SCIn_RXI中断请求。当RTRG[3:0]设置为0时，即使接收FIFO中的数据量等于0，RDF标志也不会设置。此外，不会发生SCIn_RXI中断。

RSTRG[3:0]位（RTS输出有效触发数选择）

当接收FIFO数据寄存器(FRDRHL)中存储的接收数据量等于或大于指定的接收触发数时，RTS信号变为高电平。当RSTRG[3:0]设置为0时，即使接收FIFO中的数据量等于0，RTS信号也不会变高。

29.2.27 FIFO Data Count Register (FDR)

Address(es): SCI0.FDR 4007 0016h, SCI1.FDR 4007 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	R[4:0]	Receive FIFO Data Count	Indicates the amount of receive data stored in FRDRHL. Valid only in asynchronous mode, including multi-processor or clock synchronous mode, when FCR.FM = 1.	R
b7 to b5	—	Reserved	These bits are read as 0	R
b12 to b8	T[4:0]	Transmit FIFO Data Count	Indicates the amount of non-transmit data stored in FTDRHL. Valid only in asynchronous mode, including multi-processor or clock synchronous mode, when FCR.FM = 1.	R
b15 to b13	—	Reserved	These bits are read as 0	R

This register indicates the amount of data stored in FRDRHL/FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. A value of 00h means no receive data, and 10h means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. A value of 00h means no transmit data, and 10h means that all (maximum count) of the data to be transmitted is stored in FTDRHL.

29.2.28 Line Status Register (LSR)

Address(es): SCI0.LSR 4007 0018h, SCI1.LSR 4007 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ORER	Overrun Error Flag	Valid only in asynchronous mode, including multi-processor, or clock synchronous mode, with FIFO selected: 0: No overrun error occurred 1: An overrun error occurred.	R*1
b1	—	Reserved	This bit is read as 0	R
b6 to b2	FNUM[4:0]	Framing Error Count	Indicates the amount of data with a framing error in the receive data stored in the Receive FIFO Data Register (FRDRHL)	R
b7	—	Reserved	This bit is read as 0	R
b12 to b8	PNUM[4:0]	Parity Error Count	Indicates the amount of data with a parity error among the receive data stored in the Receive FIFO Data Register (FRDRHL)	R
b15 to b13	—	Reserved	These bits are read as 0	R

Note 1. If this flag is 1, write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the status of receive error.

29.2.27 FIFO数据计数寄存器(FDR)

Address(es): SCI0.FDR 4007 0016h, SCI1.FDR 4007 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	R[4:0]	接收FIFO数据计数	表示FRDRHL中存储的接收数据量。当FCR.FM=1时，仅在异步模式下有效，包括多处理器或时钟同步模式。	R
b7 to b5	—	Reserved	这些位被读为0	R
b12 to b8	T[4:0]	发送FIFO数据计数	指示存储在FTDRHL中的非传输数据量。当FCR.FM=1时，仅在异步模式下有效，包括多处理器或时钟同步模式。	R
b15 to b13	—	Reserved	这些位被读为0	R

该寄存器指示存储在FRDRHLFTDRHL中的数据量。

R[4:0]位（接收FIFO数据计数）

R[4:0]位指示存储在FRDRHL中的接收数据量。值为00h表示没有接收数据，10h表示最大接收数据存储在FRDRHL中。

T[4:0]位（发送FIFO数据计数）

T[4:0]位指示存储在FTDRHL中的未传输数据量。值00h表示没有发送数据，而10h表示要发送的所有数据（最大计数）都存储在FTDRHL中。

29.2.28 线路状态寄存器(LSR)

Address(es): SCI0.LSR 4007 0018h, SCI1.LSR 4007 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ORER	溢出错误标志	仅在异步模式下有效，包括多处理器，或时钟同步模式，选择FIFO：0：未发生溢出错误1：发生溢出错误。	R*1
b1	—	Reserved	该位读为0	R
b6 to b2	FNUM[4:0]	帧错误计数	指示存储在接收FIFO数据寄存器(FRDRHL)中的接收数据中存在帧错误的数据量	R
b7	—	Reserved	该位读为0	R
b12 to b8	PNUM[4:0]	奇偶错误计数	表示存储在接收FIFO数据寄存器(FRDRHL)中的接收数据中有奇偶校验错误的数据量	R
b15 to b13	—	Reserved	这些位被读为0	R

Note 1. 如果该标志为1，则向SSR_FIFO.ORER写入0以清除该标志。

LSR寄存器指示接收错误的状态。

ORER bit (Overrun Error Flag)

The ORER bit reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The value in the FNUM[4:0] bits indicates the amount of data stored in the FRDRHL register with a framing error.

PNUM[4:0] bits (Parity Error Count)

The value in the PNUM[4:0] bits indicates the amount of data stored in the FRDRHL register with a parity error.

29.2.29 Compare Match Data Register (CDR)

Address(es): SCI0.CDR 4007 001Ah, SCI1.CDR 4007 003Ah, SCI4.CDR 4007 009Ah, SCI9.CDR 4007 013Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	CMPD[8:0]	Compare Match Data	Compare data pattern for address match wakeup function	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function when the address match function is enabled (DCCR.DCME = 1).

Three bit lengths are available:

- CMPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length.

29.2.30 Data Compare Match Control Register (DCCR)

Address(es): SCI0.DCCR 4007 0013h, SCI1.DCCR 4007 0033h, SCI4.DCCR 4007 0093h, SCI9.DCCR 4007 0133h

	b7	b6	b5	b4	b3	b2	b1	b0
	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DCMF	Data Compare Match Flag	0: Not matched 1: Matched.	R/(W)*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DPER	Data Compare Match Parity Error Flag	0: No parity error occurred 1: A parity error occurred.	R/(W)*1
b4	DFER	Data Compare Match Framing Error Flag	0: No framing error occurred 1: A framing error occurred.	R/(W)*1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

ORER位（溢出错误标志）

ORER位反映了SSR_FIFO.ORER中的值。

FNUM[4:0]位（帧错误计数）

FNUM[4:0]位中的值表示存储在FRDRHL寄存器中的具有帧错误的数据量。

PNUM[4:0]位（奇偶错误计数）

PNUM[4:0]位中的值表示存储在FRDRHL寄存器中的具有奇偶校验错误的数据量。

29.2.29 比较匹配数据寄存器(CDR)

Address(es): SCI0.CDR 4007 001Ah, SCI1.CDR 4007 003Ah, SCI4.CDR 4007 009Ah, SCI9.CDR 4007 013Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPD[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	CMPD[8:0]	比较匹配数据	比较地址匹配唤醒功能的数据模式	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CDR寄存器设置地址匹配功能。

CMPD[8:0]位（比较匹配数据）

当地址匹配功能使能（DCCR.DCME=1）时，CMPD[8:0]位设置要比较的数据以接收地址匹配功能的数据。

提供三种位长：

- 7位长度的CMPD[6:0]
- CMPD[7:0]8位长度
- CMPD[8:0]，长度为9位。

29.2.30 数据比较匹配控制寄存器(DCCR)

Address(es): SCI0.DCCR 4007 0013h, SCI1.DCCR 4007 0033h, SCI4.DCCR 4007 0093h, SCI9.DCCR 4007 0133h

	b7	b6	b5	b4	b3	b2	b1	b0
	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
重置后的值：	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DCMF	数据比较匹配标志	0：不匹配1： 匹配。	R/(W)*1
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	DPER	数据比较匹配奇偶校验 错误标志	0：未发生奇偶校验错误1 ：发生奇偶校验错误。	R/(W)*1
b4	DFER	数据比较匹配 成帧错误标志	0：未发生帧错误1：发生帧 错误。	R/(W)*1
b5	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	IDSEL	ID Frame Select	Valid only in asynchronous mode, including multi-processor: 0: Always compare data regardless of the MPB bit value 1: Compare data when the MPB bit is 1 (ID frame).	R/W
b7	DCME	Data Compare Match Enable	Valid only in asynchronous mode, including multi-processor: 0: Address match function is disabled 1: Address match function is enabled.	R/W

Note 1. Only 0 can be written to clear the flag after reading 1.

DCCR sets control of the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detects a match of the comparison data (CDR.CMPD) with receive data.

[Setting condition]

- When comparison data (CDR.CMPD) matches the receive data, when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the RE bit to 0 in the Serial Control Register (SCR) does not affect the DCMF flag, which keeps its previous state.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred at address match detection (reception data match detection).

[Setting condition]

- When a parity error is detected in the frame in which an address match was detected.

[Clearing conditions]

- When 0 is written after 1 is read from DPER.

Clearing the RE bit in SCR to 0 (serial reception is disabled) does not affect the DPER flag, which keeps its previous value.

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurred at address match detection (reception data match detection).

[Setting conditions]

- When a stop bit is 0 in the frame in which an address match is detected.
- When in 2-stop mode, only the first stop bit is checked for a value of 1 while the second bit is not checked.

[Clearing conditions]

- When 0 is written after 1 is read from DFER.

When the RE bit in SCR is set to 0 (serial reception is disabled), the DFER flag is not affected and keeps its previous value.

IDSEL bit (ID Frame Select)

The IDSEL bit selects whether to compare data regardless of the value of the MPB bit or to compare data only when MPB = 1 (ID frame), when the address match function is enabled.

DCME bit (Data Compare Match Enable)

The DCME bit selects whether the address match function (data compare match function) is used or not.

If SCI detects a match between the comparison data (CDR.CMPD) and receive data, DCME is cleared automatically and the SCI operates in receive mode without data compare match function. See section 29.3.6, Address Match (Receive Data Match Detection) Function.

Bit	Symbol	位名称	Description	R/W
b6	IDSEL	ID帧选择	仅在异步模式下有效，包括多处理器：0：无论MPB位值如何，始终比较数据1：当MPB位为1（ID帧）时比较数据。	R/W
b7	DCME	数据比较匹配 Enable	仅在异步模式下有效，包括多处理器：0：禁用地址匹配功能 1：启用地址匹配功能。	R/W

Note 1. 读1后只能写0清除标志。

DCCR设置地址匹配功能的控制。

DCMF标志（数据比较匹配标志）

DCMF标志表示SCI检测到比较数据(CDR.CMPD)与接收数据的匹配。

[Setting condition]

- 当比较数据(CDR.CMPD)与接收数据匹配时，当DCCR.DCME=1。

[Clearing condition]

- 从DCMF读取1后写入0时。

将串行控制寄存器(SCR)中的RE位清除为0不会影响DCMF标志，它保持其先前的状态。

DPER标志（数据比较匹配奇偶校验错误标志）

DPER标志表示在地址匹配检测（接收数据匹配检测）时发生奇偶校验错误。

[Setting condition]

- 在检测到地址匹配的帧中检测到奇偶校验错误时。

[Clearing conditions]

- 当从DPER读取1后写入0。

将SCR中的RE位清为0（禁用串行接收）不会影响DPER标志，它保持其先前的值。

DFER标志（数据比较匹配成帧错误标志）

DFER标志表示在地址匹配检测（接收数据匹配检测）时发生了帧错误。

[Setting conditions]

- 当检测到地址匹配的帧中停止位为0时。
- 在2停止模式下，仅检查第一个停止位的值是否为1，而不检查第二个停止位。

[Clearing conditions]

- 从DFER读取1后写入0。

当SCR中的RE位设置为0（禁用串行接收）时，DFER标志不受影响并保持其先前的值。

IDSEL位（ID帧选择）

IDSEL位选择不管MPB位的值是比较数据还是只比较数据
MPB=1（ID帧），当地址匹配功能启用时。

DCME位（数据比较匹配使能）

DCME位选择是否使用地址匹配功能（数据比较匹配功能）。

如果SCI检测到比较数据（CDR.CMPD）与接收数据匹配，则DCME自动清零，SCI在接收模式下运行，没有数据比较匹配功能。请参见第29.3.6节，地址匹配（接收数据匹配检测）功能。

The write value should be 0 for any mode other than asynchronous mode.

29.2.31 Serial Port Register (SPTR)

Address(es): SCI0.SPTR 4007 001Ch, SCI1.SPTR 4007 003Ch, SCI4.SPTR 4007 009Ch, SCI9.SPTR 4007 013Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	RXDMON	Serial Input Data Monitor	The state of the RXDn pin: 0: RXDn pin is low 1: RXDn pin is high.	R
b1	SPB2DT	Serial Port Break Data Select	The output level of TXDn pin when SCR.TE = 0: 0: Output low on TXDn pin 1: Output high on TXDn pin.	R/W
b2	SPB2IO	Serial Port Break I/O	Selects whether the value of SPB2DT is output to TXDn pin: 0: The value of SPB2DT bit is not output to TXDn pin 1: The value of SPB2DT bit is output to TXDn pin.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPTR register provides confirmation of serial reception pin (RXDn pin) status and sets transmission pin (TXDn pin) status.

This register can only be used in asynchronous mode.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO and SPTR.SPB2DT bit settings as shown in Table 29.21.

Table 29.21 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	x	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	x	x	Serial transmission data is output

x: Don't care.
Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

29.3 Operation in Asynchronous Mode

Figure 29.2 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit/receive data, a parity bit, and stop bits (high level).

In asynchronous serial communications, the communications line is held in the mark state (high level) when not communicating.

The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and the receiver have a double-buffered structure in addition to FIFO mode, so that the data can be read or written during transmission or reception, enabling continuous data transmission and reception.

对于异步模式以外的任何模式，写入值都应为0。

29.2.31 串行端口寄存器(SPTR)

Address(es): SCI0.SPTR 4007 001Ch, SCI1.SPTR 4007 003Ch, SCI4.SPTR 4007 009Ch, SCI9.SPTR 4007 013Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
重置后的值：	0	0	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b0	RXDMON	串行输入数据监视器	RXDn引脚的状态：0：RXDn引脚为低电平1：RXDn引脚为高电平。	R
b1	SPB2DT	串口中断数据Select	SCR.TE=0时TXDn引脚的输出电平：0：TXDn引脚输出低电平1：TXDn引脚输出高电平。	R/W
b2	SPB2IO	串口中断IO	选择是否将SPB2DT的值输出到TXDn引脚：0：SPB2DT位的值不输出到TXDn引脚1：SPB2DT位的值输出到TXDn引脚。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SPTR寄存器提供串行接收引脚（RXDn引脚）状态的确认并设置发送引脚（TXDn引脚）状态。

该寄存器只能在异步模式下使用。

TXDn引脚状态由SCR.TE、SPTR.SPB2IO和SPTR.SPB2DT位设置的组合决定，如表29.21所示。

Table 29.21 TXDn引脚状态

SCR.TE的价值	SPTR.SPB2IO的值	SPTR.SPB2DT的值	TXDn引脚状态
0	0	x	Hi-Z (initial value)
0	1	0	低电平输出
0	1	1	高电平输出
1	x	x	串行传输数据输出

x: Don't care.
Note: 仅在异步模式下使用SPTR寄存器。不保证在任何其他模式下使用该寄存器。

29.3 异步模式下的操作

图29.2显示了异步串行通信的一般格式。一帧由起始位（低电平）、发送接收数据、奇偶校验位和停止位（高电平）组成。

在异步串行通信中，通信线在不通信时保持在标记状态（高电平）。

SCI监控通信线路。当SCI检测到低电平时，将其视为起始位并开始串行通信。

在SCI内部，发射器和接收器是独立的单元，可实现全双工通信。发送器和接收器除了FIFO模式外，都具有双缓冲结构，使数据在发送或接收过程中都可以进行读写，实现数据的连续发送和接收。

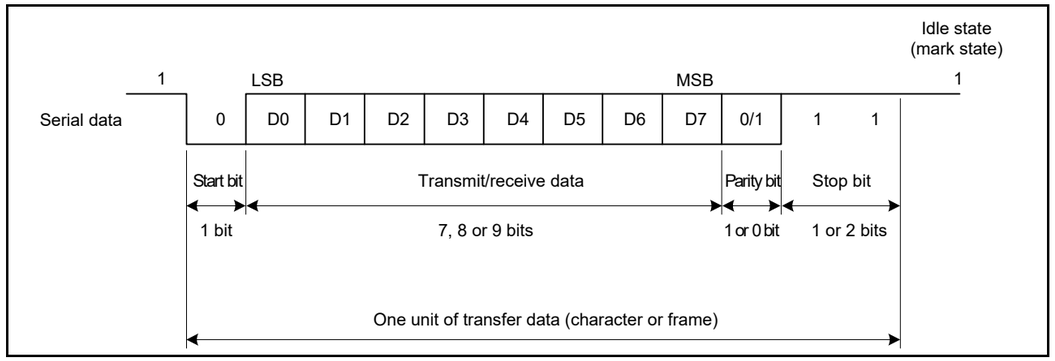


Figure 29.2 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

29.3.1 Serial Data Transfer Format

Table 29.22 lists the serial data transfer formats that can be used in asynchronous mode. Any of the 18 transfer formats can be selected with the SMR and SCMR settings. For details on the multi-processor function, see section 29.4, Multi-Processor Communications Function.

Table 29.22 Serial transfer formats (asynchronous mode) (1 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
					1 2 3 4 5 6 7 8 9 10 11 12 13
CHR1	CHR	PE	MP	STOP	
0	0	0	0	0	S 9-bit data STOP
0	0	0	0	1	S 9-bit data STOP STOP
0	0	1	0	0	S 9-bit data P STOP
0	0	1	0	1	S 9-bit data P STOP STOP
1	0	0	0	0	S 8-bit data STOP
1	0	0	0	1	S 8-bit data STOP STOP
1	0	1	0	0	S 8-bit data P STOP

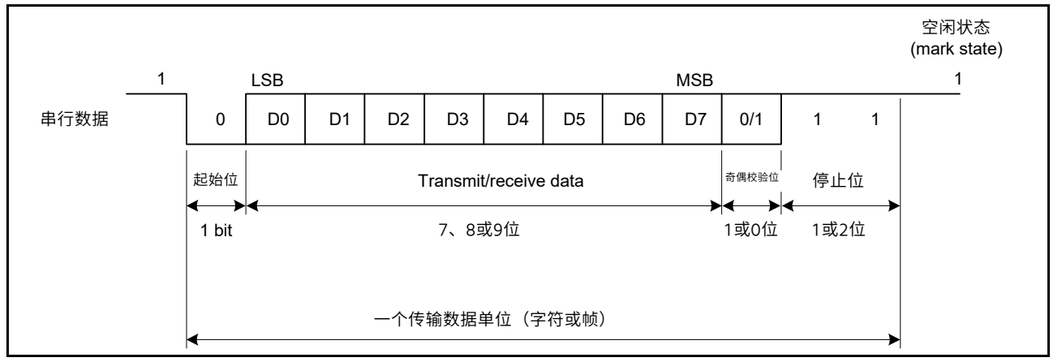


Figure 29.2 异步串行通信中的数据格式，包含8位数据、奇偶校验位和2个停止位

29.3.1 串行数据传输格式

表29.22列出了可以在异步模式下使用的串行数据传输格式。可以使用SMR和SCMR设置选择18种传输格式中的任何一种。有关多处理器功能的详细信息，请参阅第29.4节，多处理器通信功能。

Table 29.22 串行传输格式（异步模式）（1of2）

SCMR setting	SMR setting				串行传输格式和帧长
					1 2 3 4 5 6 7 8 9 10 11 12 13
CHR1	CHR	PE	MP	STOP	
0	0	0	0	0	S 9-bit data STOP
0	0	0	0	1	S 9-bit data STOP STOP
0	0	1	0	0	S 9-bit data P STOP
0	0	1	0	1	S 9-bit data P STOP STOP
1	0	0	0	0	S 8-bit data STOP
1	0	0	0	1	S 8-bit data STOP STOP
1	0	1	0	0	S 8-bit data P STOP

Table 29.22 Serial transfer formats (asynchronous mode) (2 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length (1 2 3 4 5 6 7 8 9 10 11 12 13)
CHR1	CHR	PE	MP	STOP	
1	0	1	0	1	S | 8-bit data | P | STOP | STOP
1	1	0	0	0	S | 7-bit data | STOP
1	1	0	0	1	S | 7-bit data | STOP | STOP
1	1	1	0	0	S | 7-bit data | P | STOP
1	1	1	0	1	S | 7-bit data | P | STOP | STOP
0	0	—	1	0	S | 9-bit data | MPB | STOP
0	0	—	1	1	S | 9-bit data | MPB | STOP | STOP
1	0	—	1	0	S | 8-bit data | MPB | STOP
1	0	—	1	1	S | 8-bit data | MPB | STOP | STOP
1	1	—	1	0	S | 7-bit data | MPB | STOP
1	1	—	1	1	S | 7-bit data | MPB | STOP | STOP

S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multi-processor bit

Table 29.22 串行传输格式（异步模式）（2之2）

SCMR setting	SMR setting				串行传输格式和帧长 (1 2 3 4 5 6 7 8 9 10 11 12 13)
CHR1	CHR	PE	MP	STOP	
1	0	1	0	1	S | 8-bit data | P | STOP | STOP
1	1	0	0	0	S | 7-bit data | STOP
1	1	0	0	1	S | 7-bit data | STOP | STOP
1	1	1	0	0	S | 7-bit data | P | STOP
1	1	1	0	1	S | 7-bit data | P | STOP | STOP
0	0	—	1	0	S | 9-bit data | MPB | STOP
0	0	—	1	1	S | 9-bit data | MPB | STOP | STOP
1	0	—	1	0	S | 8-bit data | MPB | STOP
1	0	—	1	1	S | 8-bit data | MPB | STOP | STOP
1	1	—	1	0	S | 7-bit data | MPB | STOP
1	1	—	1	1	S | 7-bit data | MPB | STOP | STOP

S: 起始位
STOP: 停止位
P: 奇偶校验位
MPB: Multi-processor bit

29.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 29.3. The reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\left| D - 0.5 \right|}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M: Reception margin
N: Ratio of bit rate to clock
N = 16 when ABCSE in SEMR = 0 and ABCS in SEMR = 0,
N = 8 when ABCS in SEMR = 1, N = 6 when ABCSE in SEMR = 1
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined by the following formula:

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed in system design.

Note 1. In this example, the ABCS bit in SEMR is 0 and ABCSE bit in SEMR is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.
When the ABCSE bit is 1, a frequency of 6 times the bit rate is used as a base clock and the receive data is sampled on the rising edge of the 3rd pulse of the base clock.

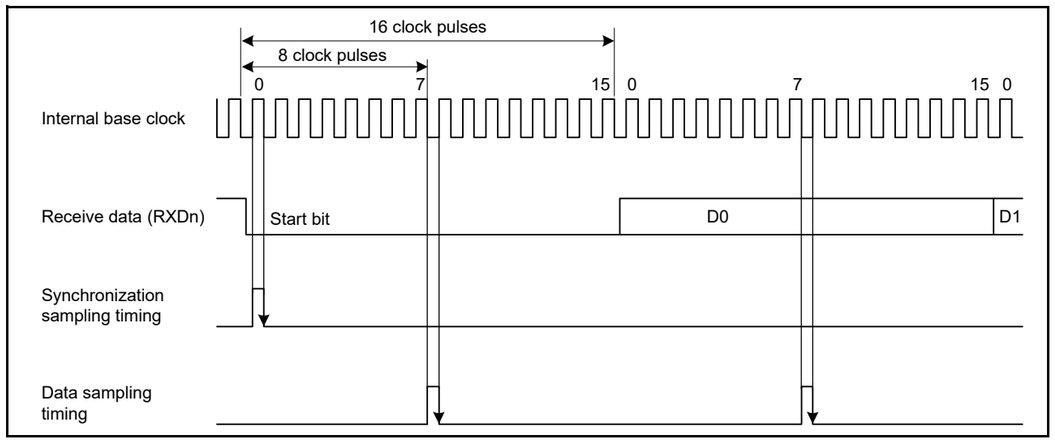


Figure 29.3 Receive data sampling timing in asynchronous mode

29.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the SCI transfer clock based on the CM setting in SMR and the CKE[1:0] setting in SCR.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when ABCS in SEMR = 0) or 8 times the bit rate (when ABCS in SEMR = 1).

29.3.2 异步模式下接收数据采样时序和接收余量

在异步模式下，SCI在频率为16倍*1比特率的基本时钟上运行。

在接收时，SCI使用基本时钟对起始位的下降沿进行采样，并执行内部同步。

由于接收数据是在基本时钟的第8个脉冲*1的上升沿采样的，因此数据在每个位的中间锁存，如图29.3所示。
异步模式下的接收余量由以下公式（1）确定：

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\left| D - 0.5 \right|}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M：接收余量
N：比特率与时钟的比率
当SEMR中的ABCSE=0和SEMR中的ABCS=0时，N=16，
当SEMR中的ABCS=1时N=8，当SEMR中的ABCSE=1时N=6
D:时钟占空比(D=0.5to1.0)
L：帧长（L=9到13）
F：时钟频率偏差的绝对值

假设公式（1）中F=0，D=0.5，接收裕量由下式确定：

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$$

但是，这只是计算值，在系统设计中应允许有20%到30%的余量。

注1.本例中，SEMR中的ABCS位为0，SEMR中的ABCSE位为0。当ABCS位为1，ABCSE位为0时，使用8倍比特率的频率作为基准时钟，并在基本时钟的第4个脉冲的上升沿对接收数据进行采样。当ABCSE位为1时，使用6倍比特率的频率作为基准时钟，在基准时钟的第3个脉冲的上升沿对接收数据进行采样。

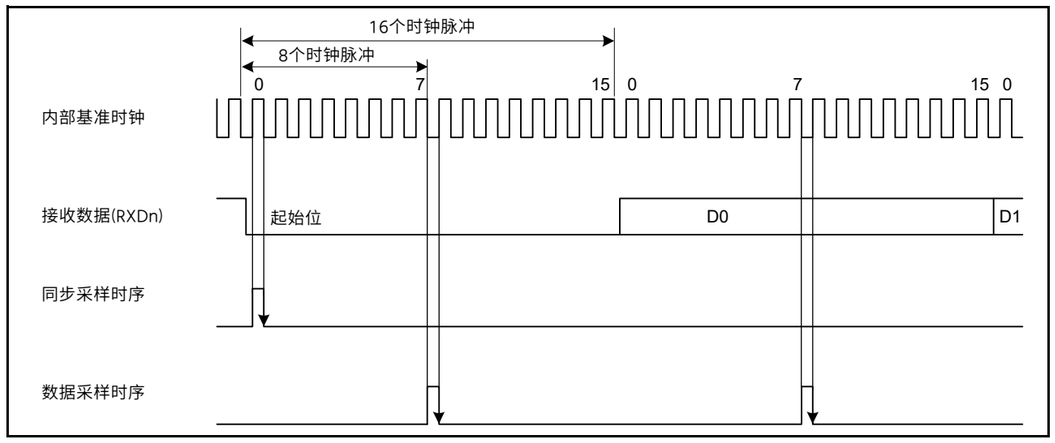


Figure 29.3 异步模式下接收数据采样时序

29.3.3 Clock

根据SMR中的CM设置和SCR中的CKE[1:0]设置，可以选择片内波特率发生器产生的内部时钟或输入到SCKn引脚的外部时钟作为SCI传输时钟。

当外部时钟输入到SCKn引脚时，时钟频率必须是比特率的16倍（当ABCS在SEMR=0）或比特率的8倍（当SEMR中的ABCS=1时）。

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as Figure 29.4 shows.

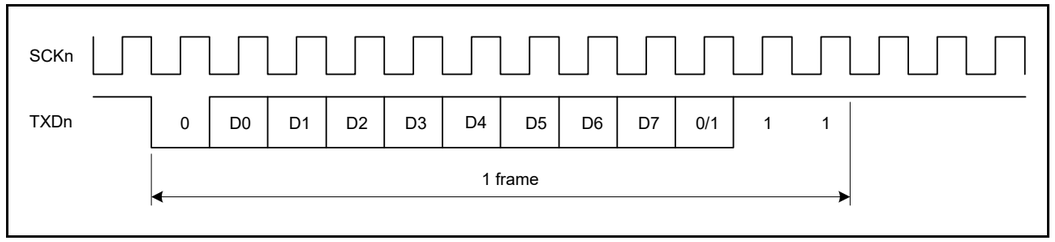


Figure 29.4 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, and STOP = 1

29.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the ABCS bit in SEMR is set to 1 and 8 pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that when ABCS is set to 0. When the BGDM bit in SEMR is set to 1, the cycle of the base clock is halved and the bit rate is double that when BGDM is set to 0. When the CKE[1] bit in SCR is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate on a bit rate four times that when the ABCS and BGDM bits are set to 0. When the ABCSE bit in SEMR is set to 1, the number of basic clock pulses are 6 during a period of 1 bit, and SCI operates at a bit rate 16/3 times that when SEMR.ABCS = 0, SEMR.BGDM = 0 and SMER.ABCSE = 0.

As shown by Formula (1) in section 29.3.2, Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the ABCS or ABCSE in SEMR is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

29.3.5 CTS and RTS Functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the CTSE bit in SPMR to 1 enables the CTS function. When the CTS function is enabled, driving the CTSn_RTSn pin low causes transmission to start.

Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function that uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for low level and high level output are shown in this section.

[Conditions for low-level output]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the RE bit in SCR is 1
- Reception is not in progress
- There is no received data yet to be read
- The ORER, FER, and PER flags in SSR are all 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the RE bit in SCR is 1
- When the amount of receive data written in FRDRHL is equal to or less than the specified receive triggering number
- The ORER flag in SSR_FIFO (ORER in the FRDRH) is 0.

[Condition for high-level output]

(a) Non-FIFO selected

- The conditions for low-level output are not satisfied

当SCI使用其内部时钟时，时钟可以从SCKn引脚输出。在这种情况下，时钟输出的频率等于比特率，并且相位使得时钟的上升沿位于传输数据的中间，如图29.4所示。

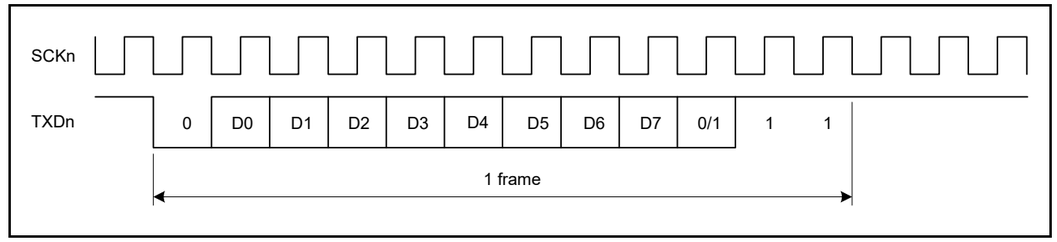


Figure 29.4 异步模式下输出时钟与传输数据的相位关系 SMR.CHR=0，PE=1，MP=0，STOP=1

29.3.4 双倍速操作和6倍比特率的频率

当SEMR中的ABCS位设置为1并选择1位周期的8个基本时钟脉冲时，SCI以ABCS设置为0时的两倍比特率运行。当SEMR中的BGDM位被设置时为1时，基本时钟周期减半，比特率是BGDM设置为0时的两倍。当SCR中的CKE[1]位设置为0且选择片内波特率发生器时，设置ABCS和BGDM位为1允许SCI以四倍于ABCS和BGDM位设置为0时的比特率运行。当SEMR中的ABCSE位设置为1时，基本时钟脉冲数为6周期为1位，SCI以16的比特率运行，是SEMR.ABCS=0、SEMR.BGDM=0和SMER.ABCSE=0时的3倍。

如第29.3.2节"异步模式下的接收数据采样时序和接收裕量"中的公式（1）所示，当SEMR中的ABCS或ABCSE设置为1时，接收裕量会减小。因此，如果可以得到目标码率ABCS或ABCSE设置为0时，建议您使用ABCS和ABCSE设置为0的SCI。

29.3.5 CTS和RTS函数

CTS功能在传输控制中使用CTSn_RTSn引脚上的输入。将SPMR中的CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚驱动为低电平会导致传输开始。

在传输过程中将CTSn_RTSn引脚驱动为高电平不会影响当前帧的传输。

在使用CTSn_RTSn引脚输出的RTS功能中，当可以接收时输出低电平。
本节显示低电平和高电平输出的条件。

[Conditions for low-level output]

(a) 满足以下所有条件时选择非FIFO

- SCR中RE位的值为1
- 接收未进行
- 没有接收到的数据尚未读取
- SSR中的ORER、FER和PER标志均为0。

(b) 满足以下所有条件时选择FIFO

- SCR中RE位的值为1
- 当FRDRHL中写入的接收数据量等于或小于指定的接收触发数时
- SSR_FIFO中的ORER标志（FRRDH中的ORER）为0。

[Condition for high-level output]

(a) Non-FIFO selected

- 不满足低电平输出的条件

- After reception is complete, if it is terminated with SCR.RE = 0 without reading the RDR register, then RTS remains high. Read the SCR register for dummy after writing SCR.RE = 0.

(b) FIFO selected

- The conditions for low-level output are not satisfied.

29.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the DCCR.DCME bit is set to 1*4, when one frame of data is received, the SCI compares that received data with the data set in CDR.CMPD. If SCI detects a match to the comparison data (CDR.CMPD*3) with the received data, the SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP = 1), if the DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match. Receive data where the MPB bit is 0 is always treated as a mismatch.

If DCCR.IDSEL is set to 0, the SCI performs address match or mismatch regardless of the MPB bit value of the received data. Until the SCI detects a match between the comparison data (CDR.CMPD*3) and receive data, the received data is skipped (discarded), and the SCI cannot detect parity error or framing error. When the SCI detects a match, DCCR.DCME is automatically cleared, and DCCR.DCMF is set to 1.

If DCCR.IDSEL is set to 1, the SCR.MPIE bit is automatically cleared. If DCCR.IDSEL is set to 0, the value of SCR.MPIE bit is retained. If SCR.RIE is set to 1, the SCI issues an SCIn_RXI interrupt request. If the SCI detects a framing error in the receive data for which a match is detected, DCCR.DFER is set to 1, and if the SCI detects a parity error in that frame, DCCR.DPER is set to 1. The compared receive data is not stored in RDR*1, and SSR.RDRF remains at 0.*2

After the SCI detects a match, and DCCR.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the DCCR.DFER or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

An example of the address match function is shown in Figure 29.5 and Figure 29.6.

Note 1. When FCR.FM = 1, this refers to the FRDRHL register.
Note 2. When FCR.FM = 1, this refers to the SSR_FIFO.RDF flag.
Note 3. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, or CMPD[8:0] with 9-bit length.
Note 4. Set the DCCR.DCME bit to 1 before receiving the start bit of the received frame that performs address matching.

- 接收完成后，如果在没有读取RDR寄存器的情况下以SCR.RE=0终止，则RTS保持高电平。写入SCR.RE=0后，读取SCR寄存器的虚拟寄存器。

(b) FIFO selected

- 不满足低电平输出的条件。

29.3.6 地址匹配（接收数据匹配检测）功能

地址匹配功能只能在异步模式下使用。

如果DCCR.DCME位设置为1*4，当接收到一帧数据时，SCI会将接收到的数据与CDR.CMPD中设置的数据进行比较。如果SCI检测到比较数据(CDR.CMPD*3)与接收到的数据匹配，则SCI可以发出SCIn_RXI中断请求。

如果SMR.MP位设置为0，则仅对接收格式的有效数据进行比较。在多处理器模式下（SMR.MP=1），如果DCCR.IDSEL位设置为1，则接收MPB位为1的数据将进行地址匹配比较。MPB位为0的接收数据始终被视为不匹配。

如果DCCR.IDSEL设置为0，则SCI执行地址匹配或不匹配，无论接收数据的MPB位值如何。直到SCI检测到比较数据（CDR.CMPD*3）与接收数据匹配，接收数据被跳过（丢弃），SCI无法检测奇偶校验错误或成帧错误。当SCI检测到匹配时，自动清除DCCR.DCME，并将DCCR.DCMF设置为1。

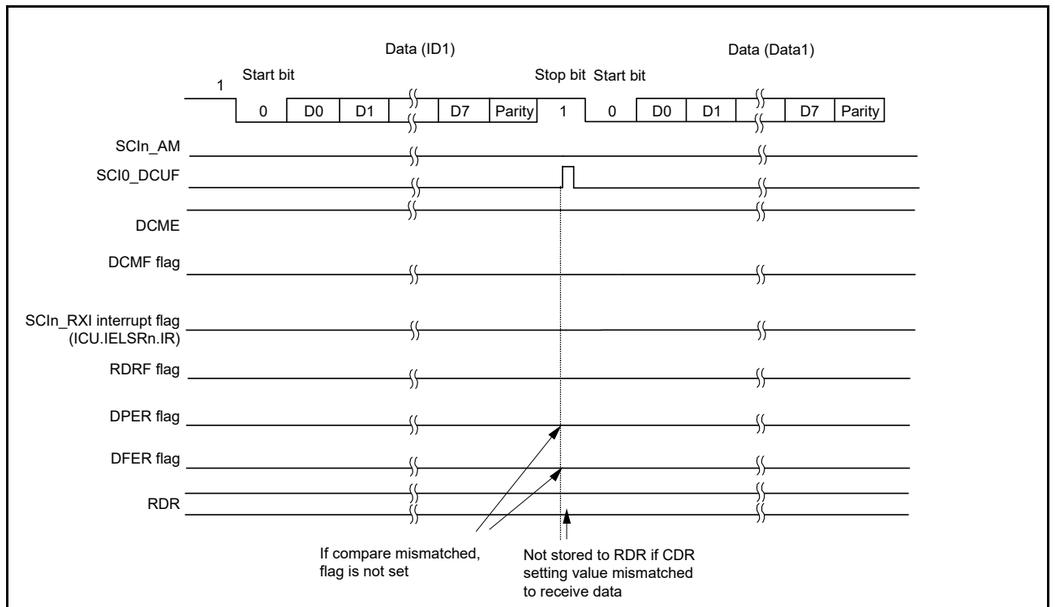
如果DCCR.IDSEL设置为1，则SCR.MPIE位自动清零。如果DCCR.IDSEL设置为0，则SCR.MPIE位被保留。如果SCR.RIE设置为1，则SCI发出SCIn_RXI中断请求。如果SCI在检测到匹配的接收数据中检测到帧错误，则DCCR.DFER设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER设置为1。比较接收数据不存储在RDR*1中，并且SSR.RDRF保持在0.*2

SCI检测到匹配后，DCCR.DCME自动清零，SCI根据当前寄存器设置连续接收下一个数据。

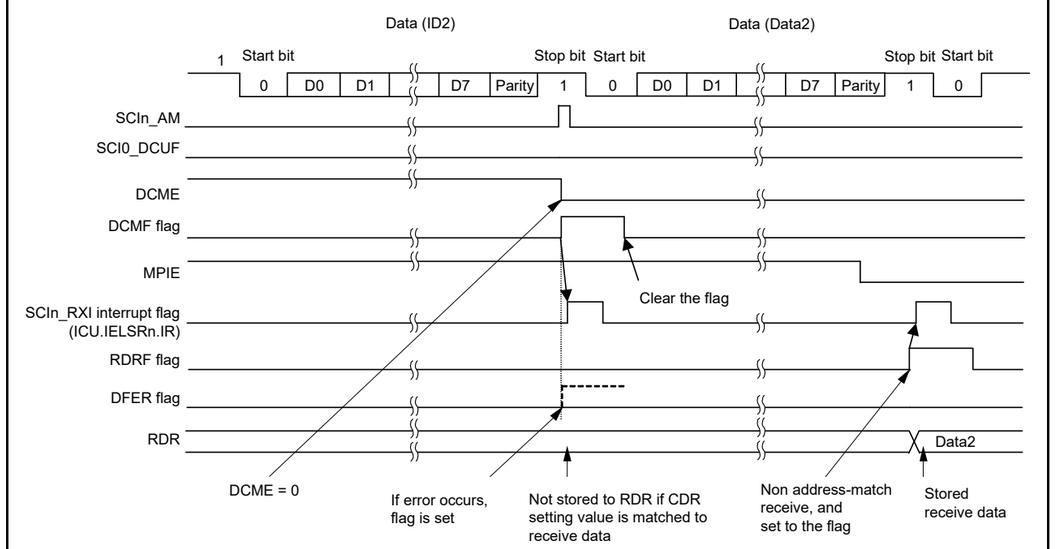
当设置DCCR.DFER或DCCR.DPER标志时，不执行地址匹配。在启用地址匹配功能之前，将DCCR.DFER和DCCR.DPER标志设置为0。

地址匹配函数的示例如图29.5和图29.6所示。

注1.当FCR.FM=1时，指的是FRDRHL寄存器。
注2.当FCR.FM=1时，这指的是SSR_FIFO.RDF标志。
注3.此比较目标可以选择3种长度中的一种：7位长度的CMPD[6:0]、8位长度的CMPD[7:0]或9位长度的CMPD[8:0].注4.在接收到执行地址匹配的接收帧的起始位之前，将DCCR.DCME位设置为1。

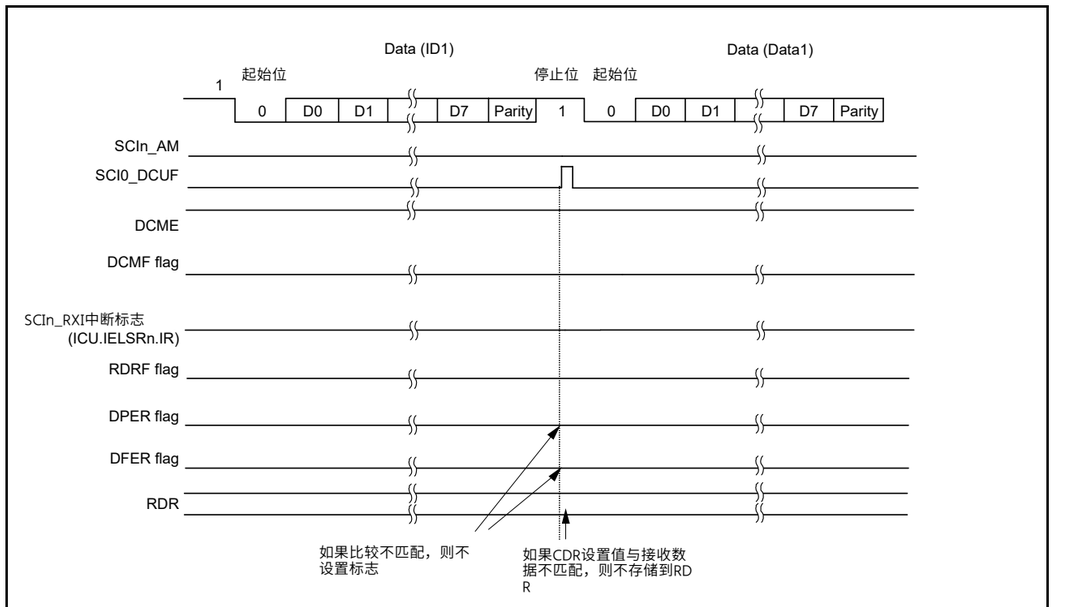


(a) Example of compare mismatched between receive data and CDR (8-bit length/parity/non multi-processor mode)

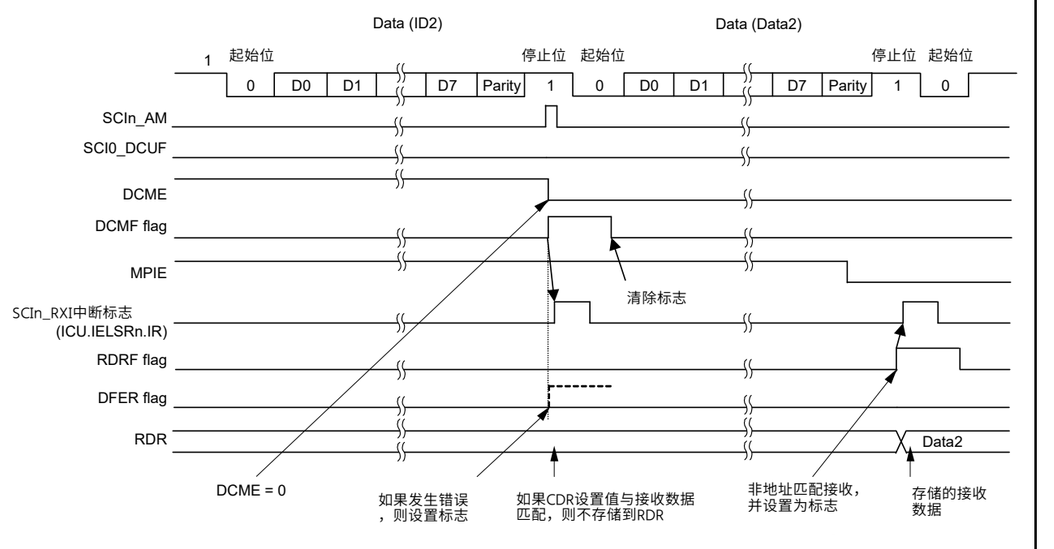


(b) Example of compare matched between receive data and CDR (8-bit length/parity/non multi-processor mode)

Figure 29.5 Example of address match (1) in non Multi-processor mode

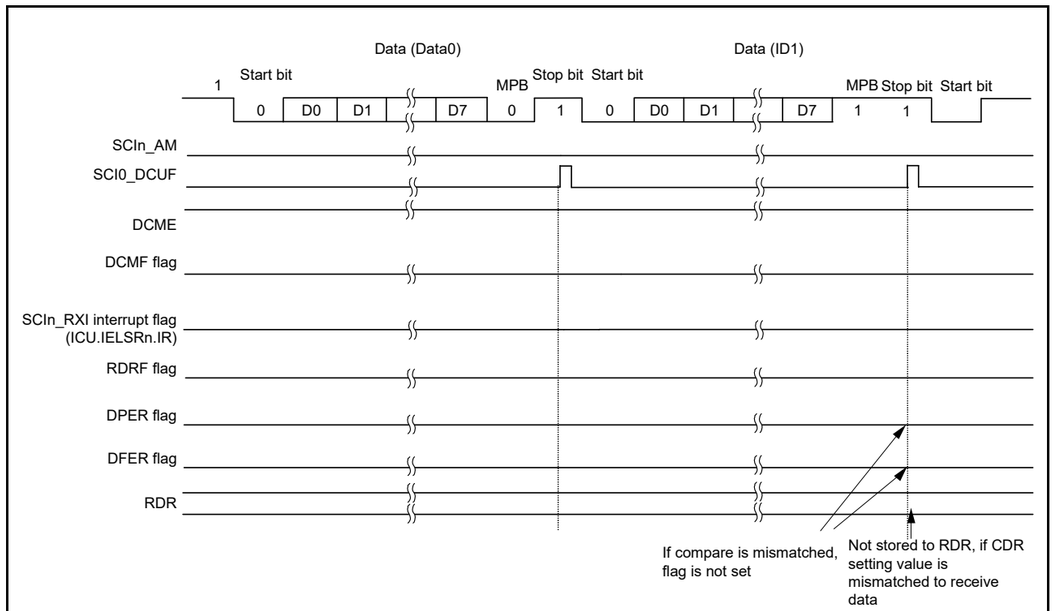


(a)接收数据和CDR比较不匹配的示例（8位长度奇偶校验非多处理器模式）

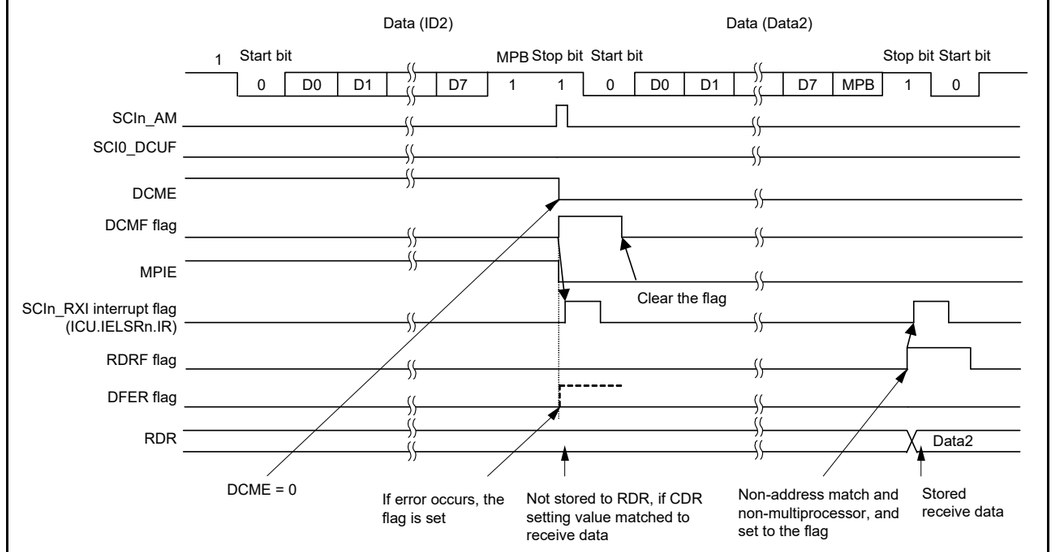


(b)接收数据与CDR比较匹配示例（8位长度奇偶校验非多处理器模式）

Figure 29.5 非多处理器模式下的地址匹配示例(1)

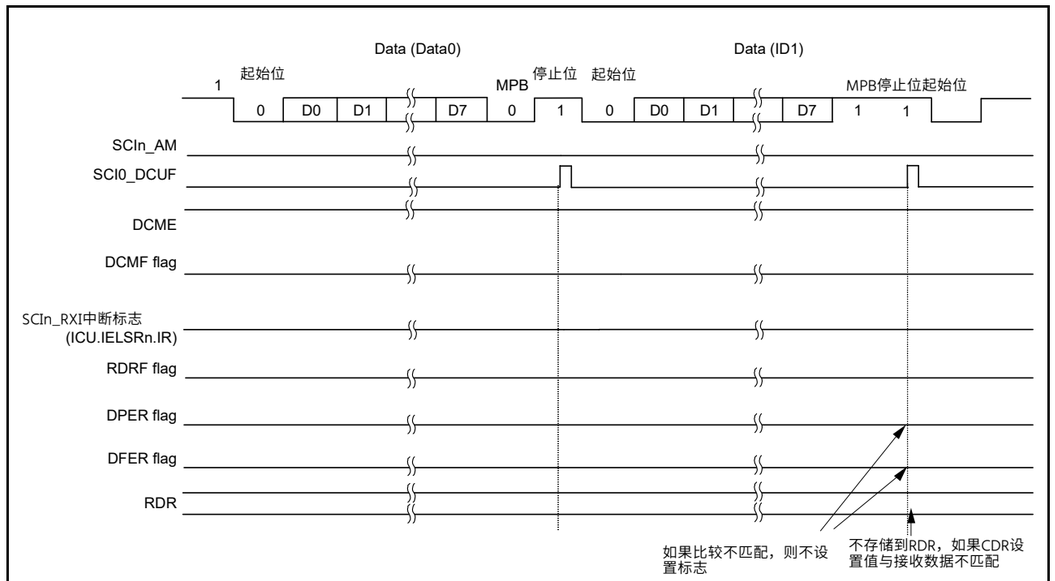


(a) Example of compare mismatched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

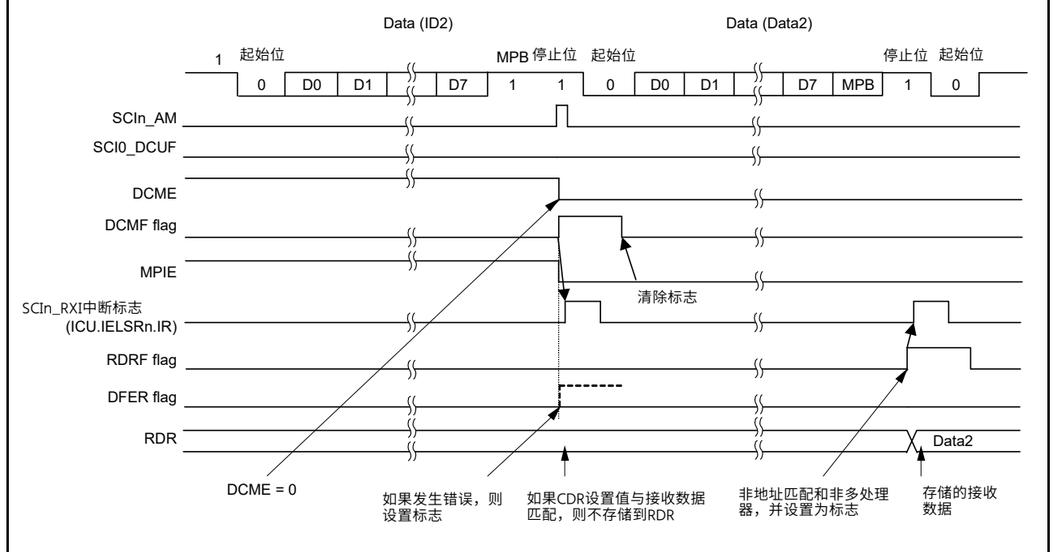


(b) Example of compare matched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

Figure 29.6 Example of address match (2) in multi-processor mode



(a)接收数据和CDR比较不匹配的示例（8位长度IDSEL=1多处理器模式）



(b)接收数据和CDR比较匹配的示例（8位长度IDSEL=1多处理器模式）

Figure 29.6 多处理器模式下的地址匹配示例（2）

29.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to SCR, and then continue through the SCI procedure (select non-FIFO or FIFO) shown in Figure 29.7 and Figure 29.8. Whenever the operating mode or transfer format is to be changed, the SCR must be initialized before a change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.

Note: When the SCR.RE bit is set to 0, the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO, and the RDR and RDRHL registers are not initialized. When the SCR.TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

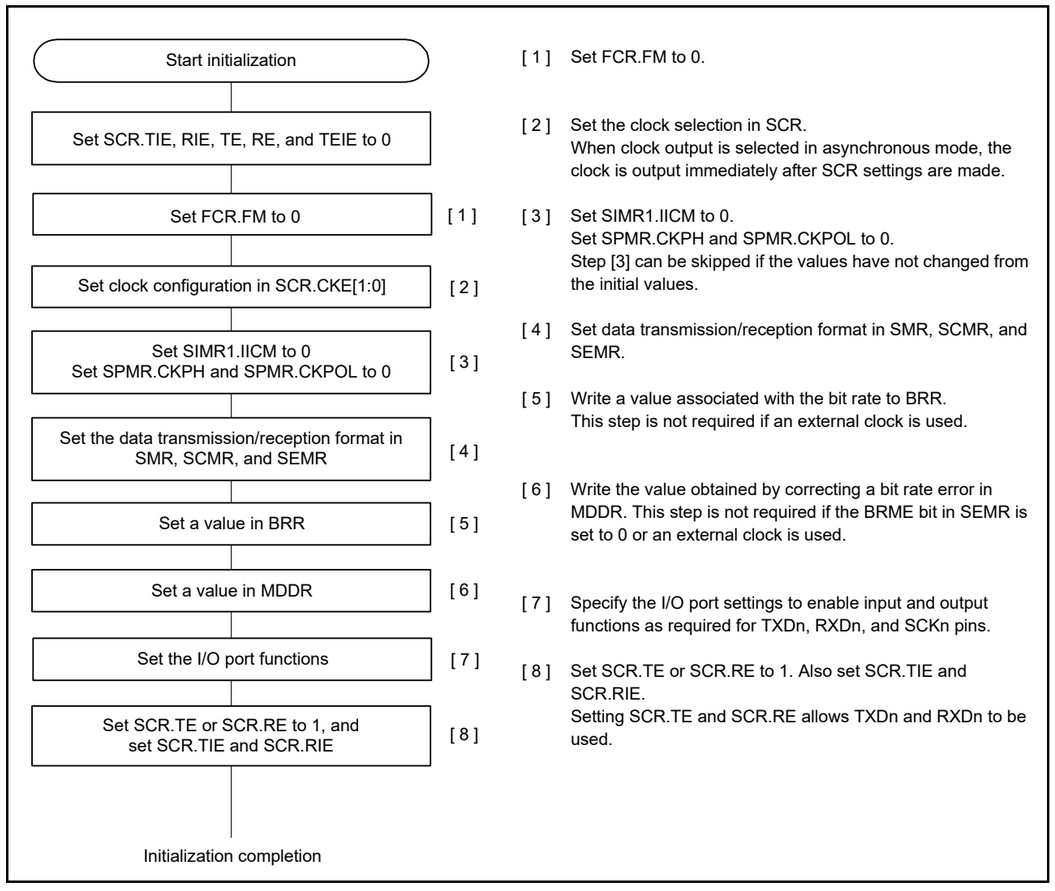


Figure 29.7 Example SCI initialization flow in asynchronous mode with non-FIFO selected

29.3.7 异步模式下的SCI初始化

在发送和接收数据之前，首先将初始值00h写入SCR，然后继续执行图29.7和图29.8所示的SCI程序（选择非FIFO或FIFO）。每当要更改操作模式或传输格式时，必须在进行更改之前初始化SCR。

在异步模式下使用外部时钟时，请确保在初始化期间提供时钟信号。

Note: 当SCR.RE位设置为0时，SSRSSR_FIFO中的ORER、FER、RDRF、RDF、PER和DR标志，以及RDR和RDRHL寄存器未初始化。当SCR.TE位设置为0时，选择的TEND标志FIFO缓冲区未初始化。

Note: 当SCR.TIE位为1时，将SCR.TE位的值从1切换到0或0到1会导致生成SCIn_TXI中断请求。

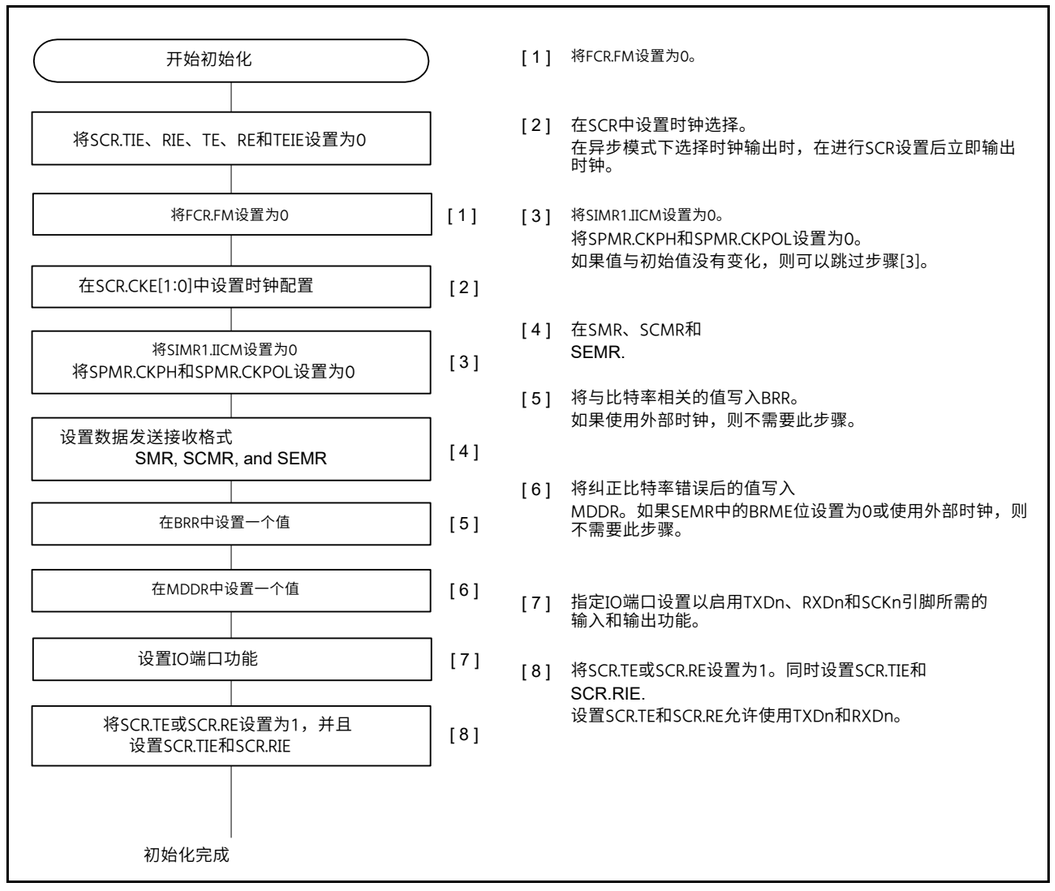


Figure 29.7 选择非FIFO的异步模式下的示例SCI初始化流程

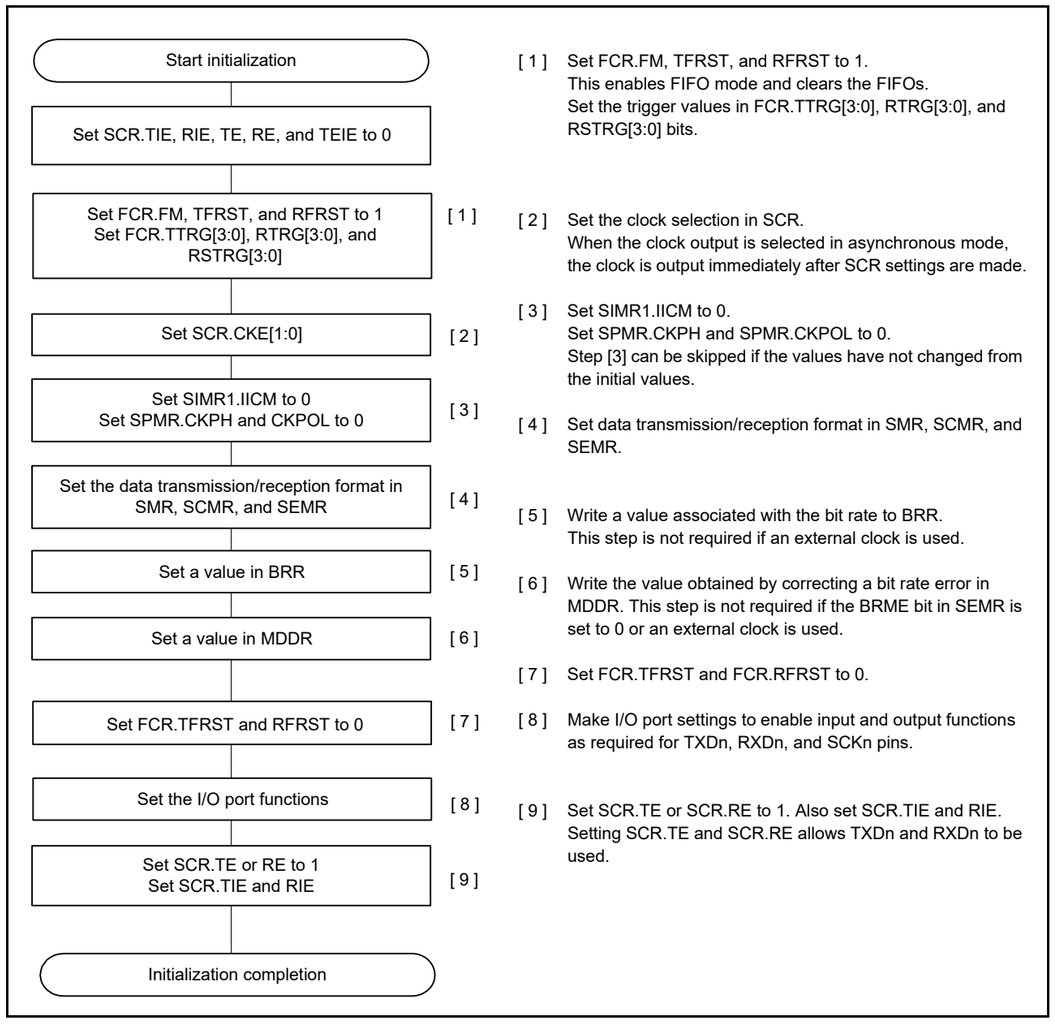


Figure 29.8 Example SCI initialization flow in synchronous mode with FIFO selected

29.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 29.9, Figure 29.10, and Figure 29.11 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the SCR.TE bit is set to 1, the high level for one frame (preamble) is output to TXD.

1. The SCI transfers data from TDR*1 to TSR when data is written to TDR*1 in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in SCR are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CTSE bit in SPMR is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from TDR*1 to TSR. If the TIE bit in SCR is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to TDR*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt

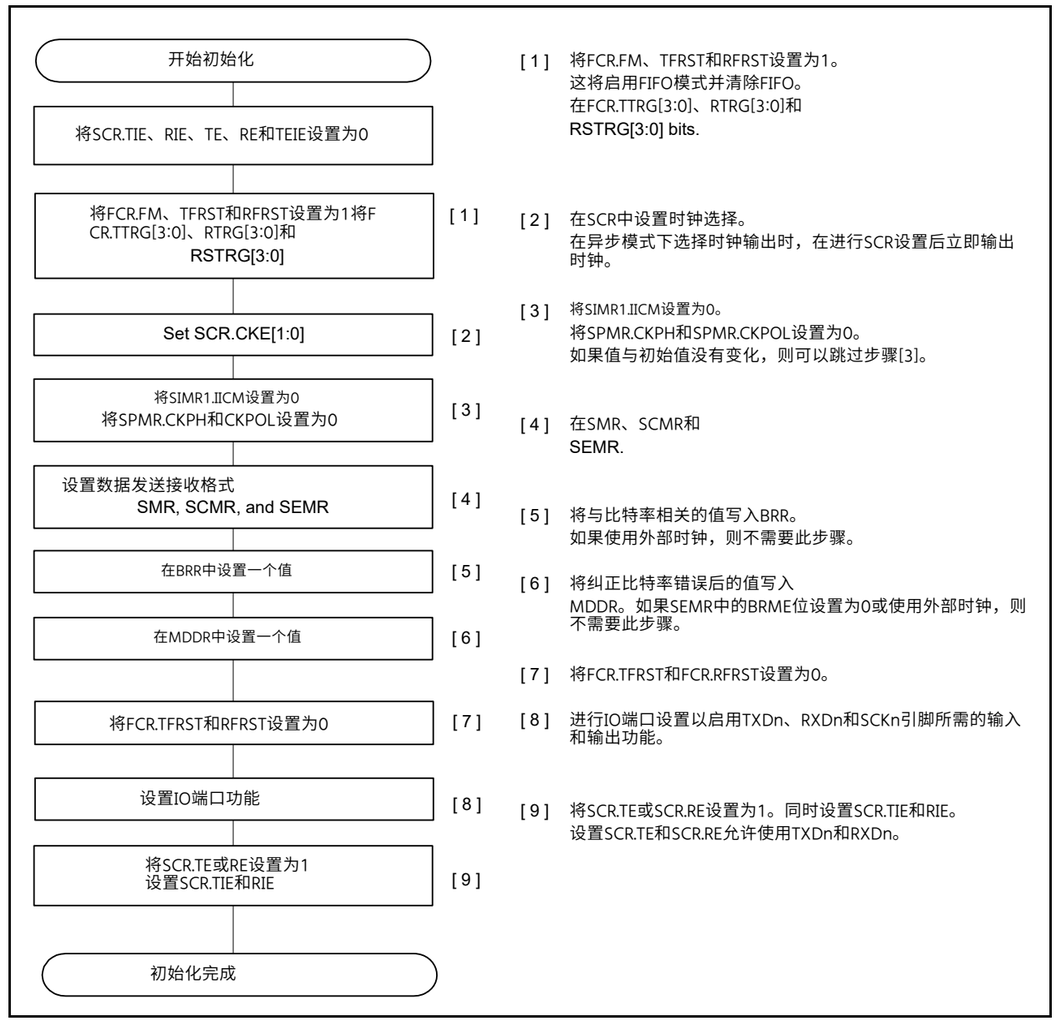


Figure 29.8 选择FIFO的同步模式下的SCI初始化流程示例

29.3.8 异步模式下的串行数据传输

(1) Non-FIFO selected

图29.9、图29.10和图29.11显示了异步模式下的串行传输示例。

在串行传输中，SCI的操作如本节所述。当SCR.TE位设置为1时，一帧（前导码）的高电平输出到TXD。

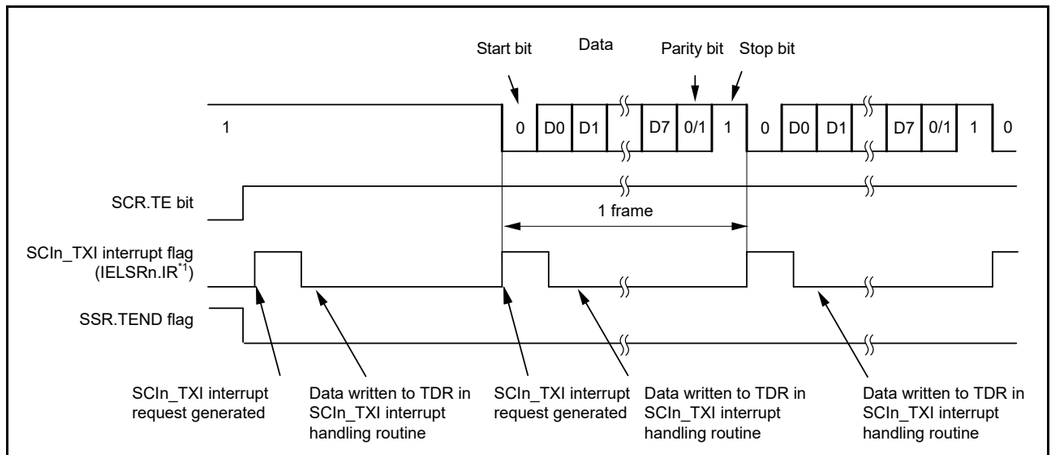
1. 当在SCIn_TXI中断处理程序中将数据写入TDR*1时，SCI将数据从TDR*1传输到TSR。当一条指令同时将SCR中的TE和TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。
2. SPMR中的CTSE位设置为0（禁用CTS功能）或在CTSn_RTSn引脚导致数据从TDR*1传输到TSR。如果SCR中的TIE位为1，则产生SCIn_TXI中断请求。在当前传输数据传输完成之前，通过在SCIn_TXI中断处理例程中将下一个传输数据写入TDR*1，可以实现连续传输。当SCIn_TEI中断

requests are in use, set TIE to 0 (an SCIn_TXI interrupt request is disabled) and TEIE to 1 (an SCIn_TEI interrupt request is enabled) in the SCR register after the last of the data to be transmitted is written to the TDR*1 from the handling routine for SCIn_TXI requests.

3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. The SCI checks for update of the TDR on output of the stop bit.
5. When TDR is updated, setting the CTSE bit in SPMR to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from TDR*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If TDR is not updated, the TEND flag in SSR is set to 1, the stop bit is sent, and the mark state is entered where 1 is output. If the TEIE bit in SCR is 1, the TEND flag in SSR is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Only write data to TDRHL when 9-bit data length is selected.

Figure 29.9, Figure 29.10, and Figure 29.11 show an example flow of serial transmission in asynchronous mode.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

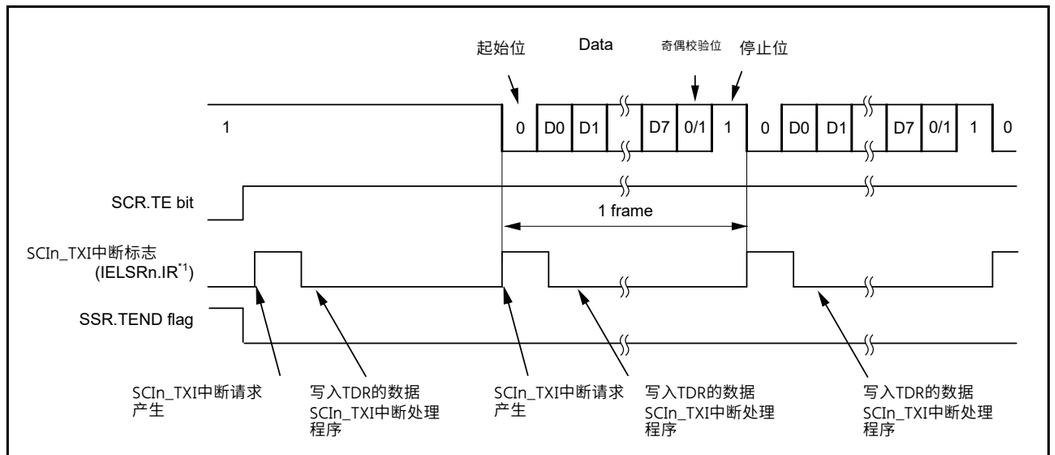
Figure 29.9 Example operation of serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission

在将要发送的最后一个数据写入TDR*1之后，在SCR寄存器中将TIE设置为0（禁用SCIn_TXI中断请求）并将TEIE设置为1（启用SCIn_TEI中断请求）SCIn_TXI请求的处理例程。

3. 数据按以下顺序从TXDn引脚发送：
   - 起始位
   - 传输数据
   - 奇偶校验位或多处理器位（可根据格式省略）
   - 停止位。
4. SCI在停止位的输出上检查TDR的更新。
5. 更新TDR时，将SPMR中的CTSE位设置为0（禁用CTS功能）或在CTSn_RTSn管脚将下一个传输数据从TDR*1传输到TSR并传输停止位，然后开始下一帧的串行传输。
6. 如果不更新TDR，则SSR中的TEND标志设置为1，发送停止位，并进入标记状态，输出1。如果SCR中的TEIE位为1，则SSR中的TEND标志设置为1，并产生SCIn_TEI中断请求。

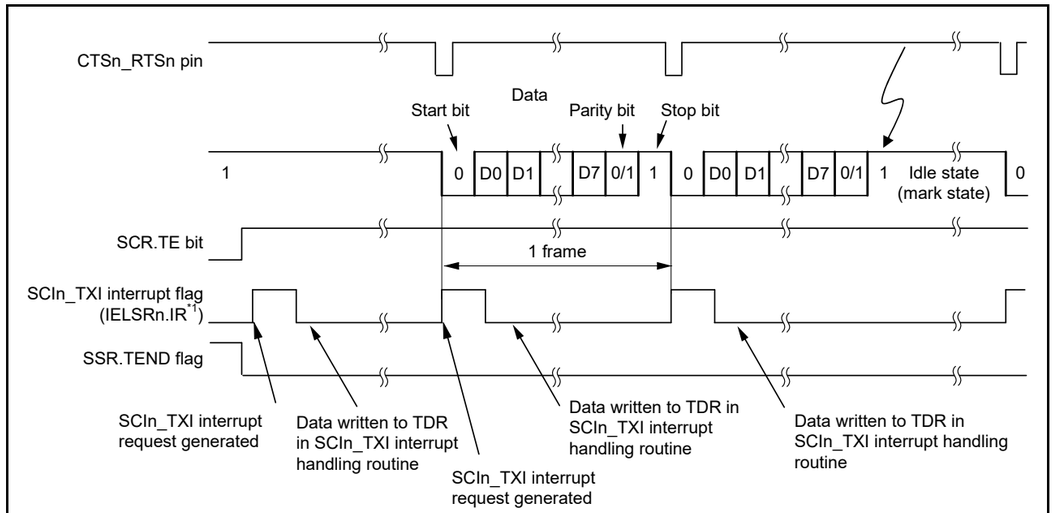
注意1.选择9位数据长度时，仅将数据写入TDRHL。

图29.9、图29.10和图29.11显示了异步模式下串行传输的示例流程。



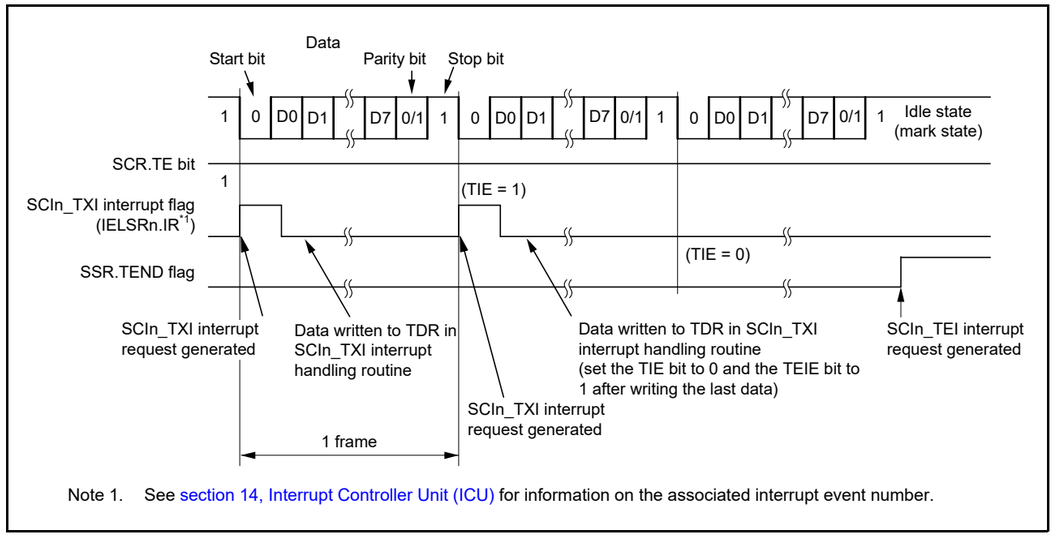
Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.9 异步模式下串行传输的示例操作(1)使用8位数据、奇偶校验位、1个停止位、未使用CTS功能以及传输开始时



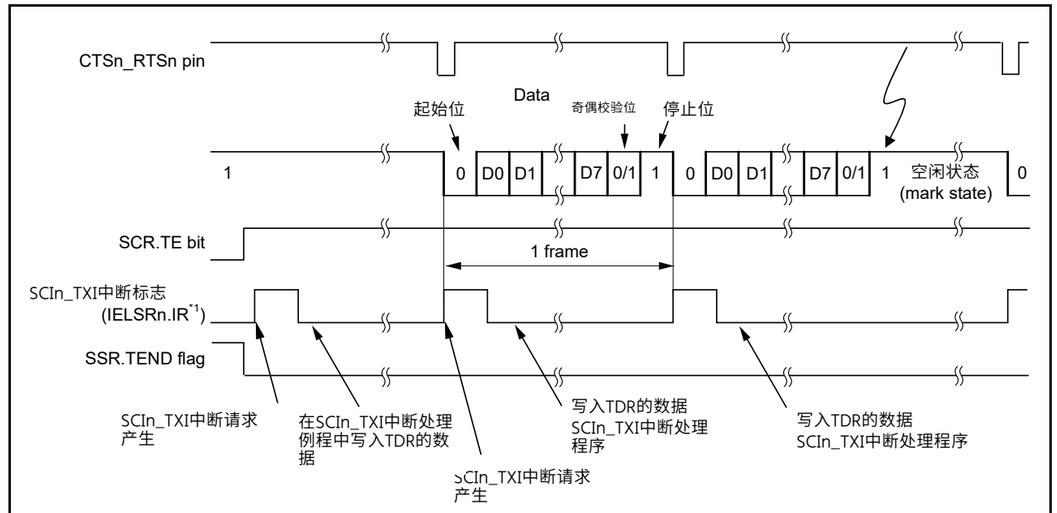
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.10 Example operation of serial transmission in asynchronous mode (2) with 8-bit data, parity bit, 1 stop bit, CTS function used, and at the beginning of transmission



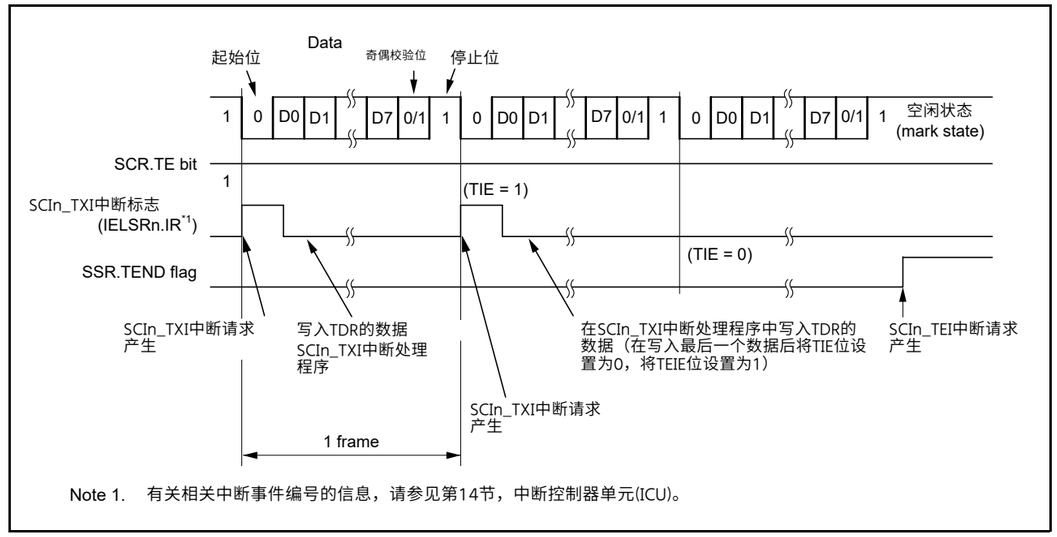
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.11 Example operation of serial transmission in asynchronous mode (3) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and from the middle of transmission until transmission completion



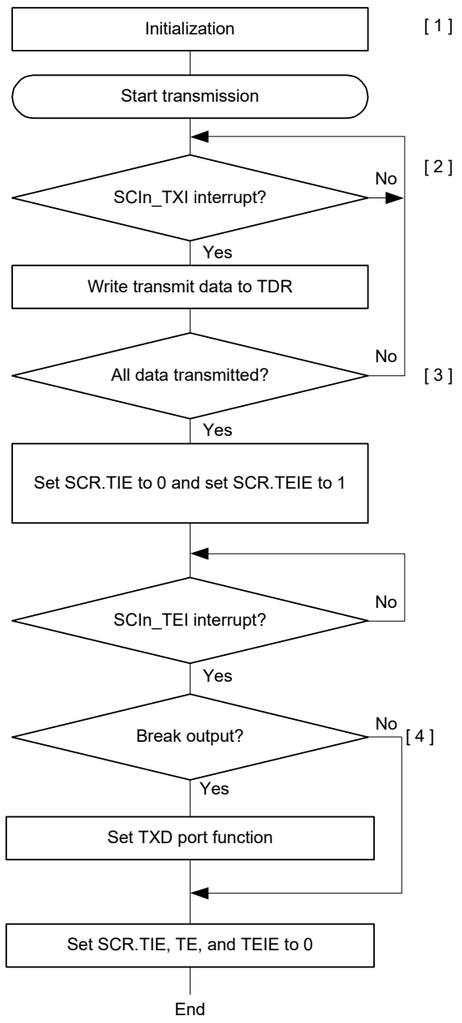
Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.10 异步模式下串行传输的示例操作(2)使用8位数据、奇偶校验位、1个停止位、使用CTS功能以及在传输开始时



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.11 异步模式下串行传输的示例操作(3)8位数据、奇偶校验位、1个停止位、未使用CTS功能，以及从传输中间到传输完成



[1] SCI Initialization:
Set data transmission.
After SCR.TE is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Write transmit data to TDR while in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request. Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set SCR.TIE to 0 and SCR.TEIE to 1 after the last of the data to be transmitted are written to TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low level output) of TXDn pin using SPTR.SPB2IO and SPTR.SPB2DT bits, set SCR.TE to 0.

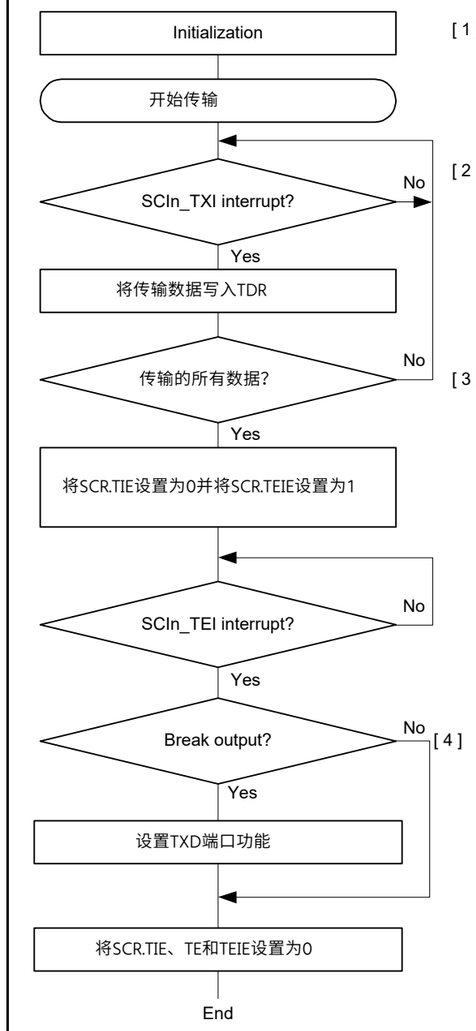
Note: TDR becomes TDRHL when 9-bit data length is selected.

Figure 29.12 Example of serial transmission flow in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 29.13 shows an example of a data format that is written to FTDRH and FTDRL in asynchronous mode.

Data that corresponds to the correct data length is set to FTDRH and FTDRL. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI Initialization:
设置数据传输。
SCR.TE设置为1后，对于一个帧（前导码）输出1，并启用传输。

[2] 通过SCIn_TXI中断请求将发送数据写入TDR：当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。在SCIn_TXI中断处理程序中将发送数据写入TDR。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据写入TDR一次。也可以通过激活DMAC或DTC将传输数据写入TDR。当SCIn_TEI中断请求正在使用时，设置

在要传输的最后一个数据写入TDR后，SCR.TIE为0，SCR.TEIE为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，在使用SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE设置为0。

Note: 选择9位数据长度时，TDR变为TDRHL。

Figure 29.12 选择非FIFO的异步模式下串行传输流示例

(2) FIFO selected

图29.13显示了以异步模式写入FTDRH和FTDRL的数据格式示例。

对应于正确数据长度的数据设置为FTDRH和FTDRL。为未使用的位写入0。从FTDRH到FTDRL的顺序写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

—: Invalid. The write value should be 0.

Figure 29.13 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit in SCR is set to 1, the high level for one frame (preamble) is output to TXD.

1. The SCI transfers data from FTDRL*1 to TSR when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine.
   The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in SCR are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CTSE bit in SPMR is set to 0 (CTS function is disabled) and a low level on the CTSn_RTSn pin causes data transfer from FTDRL*1 to TSR. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, TDFE bit in SSR_FIFO is set to 1. If the TIE bit in SCR is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set TIE to 0 (an SCIn_TXI interrupt request is disabled) and TEIE to 1 (an SCIn_TEI interrupt request is enabled) in the SCR register after the last of the data to be transmitted is written to the FTDRL*1, *2 from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. The SCI checks whether the non-transmitted data remains in FTDRL*3 on the output of the stop bit.
5. When data is set to FTDRL*3, setting of CTSE to 0 (CTS function is disabled) in the SPMR register or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered where 1 is output. If the TEIE bit in SCR is 1, the TEND flag in SSR_FIFO is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data to the FTDRH and FTDRL registers when 9-bit data length is selected.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FTDRL register and not the FTDRH register, when 9-bit data length is selected.

Figure 29.14 shows an example flow of serial transmission in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	—	—	8位传输数据							
9 bits	0	不在乎	—	—	—	—	—	—	—	9位传输数据								

-：无效的。写入值应为0。

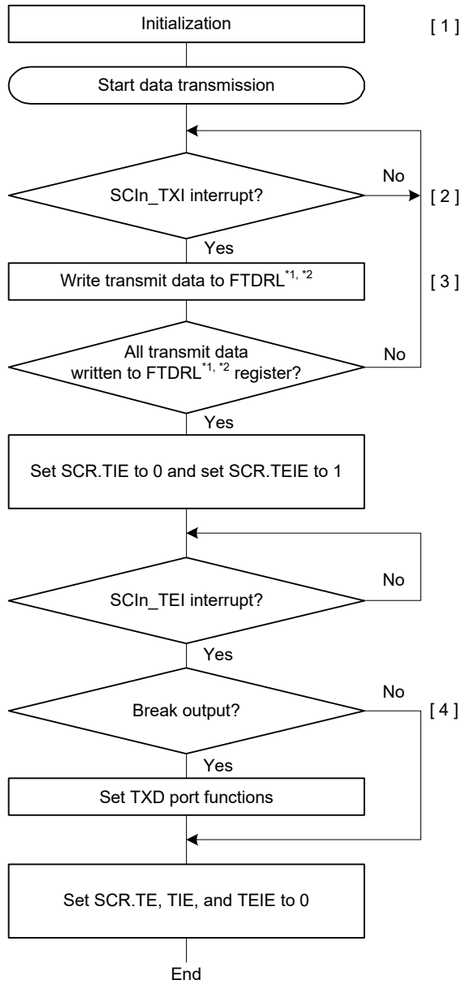
Figure 29.13 选择FIFO写入FTDRH和FTDRL的数据格式

在串行传输中，SCI的操作如本节所述。当SCR中的TE位设置为1时，一帧（前导码）的高电平输出到TXD。

1. 在SCIn_TXI中断处理例程中将数据写入FTDRL*1时，SCI将数据从FTDRL*1传输到TSR。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。当SCR中的TE和TIE位通过一条指令同时设置为1时，会在传输开始时产生SCIn_TXI中断请求。
2. SPMR中的CTSE位设置为0（禁用CTS功能）并且在CTSn_RTSn引脚导致数据从FTDRL*1传输到TSR。当写入FTDRL的发送数据量等于或小于指定的发送触发次数时，SSR_FIFO中的TDFE位设置为1。如果SCR中的TIE位为1，则产生SCIn_TXI中断请求。在当前传输数据传输完成之前，通过在SCIn_TXI中断处理例程中将下一个传输数据写入FTDRL*1可以实现连续传输。使用SCIn_TEI中断请求时，在将要传输的最后一个数据写入FTDRL后，在SCR寄存器中将TIE设置为0（禁用SCIn_TXI中断请求）并将TEIE设置为1（启用SCIn_TEI中断请求）*1 *2来自SCIn_TXI请求的处理例程。
3. 数据按以下顺序从TXDn引脚发送：
   - 起始位
   - 传输数据
   - 奇偶校验位或多处理器位（可根据格式省略）
   - 停止位。
4. SCI在停止位的输出上检查未传输的数据是否保留在FTDRL*3中。
5. 当数据设置为FTDRL*3时，将SPMR寄存器中的CTSE设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平输入会导致下一个传输数据从FTDRL*1传输到TSR并传输停止位，之后开始下一帧的串行传输。
6. 如果FTDRL*3中未设置数据，则将SSR_FIFO中的TEND标志设置为1，发送停止位，并在输出1时进入标记状态。如果SCR中的TEIE位为1，则SSR_FIFO中的TEND标志设置为1，并产生SCIn_TEI中断请求。

注意1.选择9位数据长度时，将数据写入FTDRH和FTDRL寄存器。
注2.选择9位数据长度时，按从FTDRH到FTDRL的顺序写入数据。
Note3.TheSCIonlychecksforupdatetotheFTDRLregisterandnottheFTDRHregister when9-bitdatalengthisselected.

图29.14显示了选择FIFO的异步模式下串行传输的示例流程。



[1] SCI initialization:
Set data transmission.
After SCR.TE is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
For data transmission from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1, *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and set the SSR_FIFO.TDFE flag to 0. It is possible to write 16 bits of transmit data, which is also the amount of data stored in the transmit FIFO.
Transmit data can also be written to FTDRL by activating the DMAC or DTC. When data is written to FTDRL by the DMAC or DTC, the TDFE flag is cleared automatically. Therefore, do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set SCR.TIE to 0 and SCR.TEIE to 1 after the last of the data to be transmitted is written to the FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low level output) of TXDn pin using SPTR.SPB2IO and SPTR.SPB2DT, set SCR.TE to 0.

Note 1. When data length is 9 bits, FTDRH and FTDRL registers are used.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 29.14 Example flow of serial transmission in asynchronous mode with FIFO selected

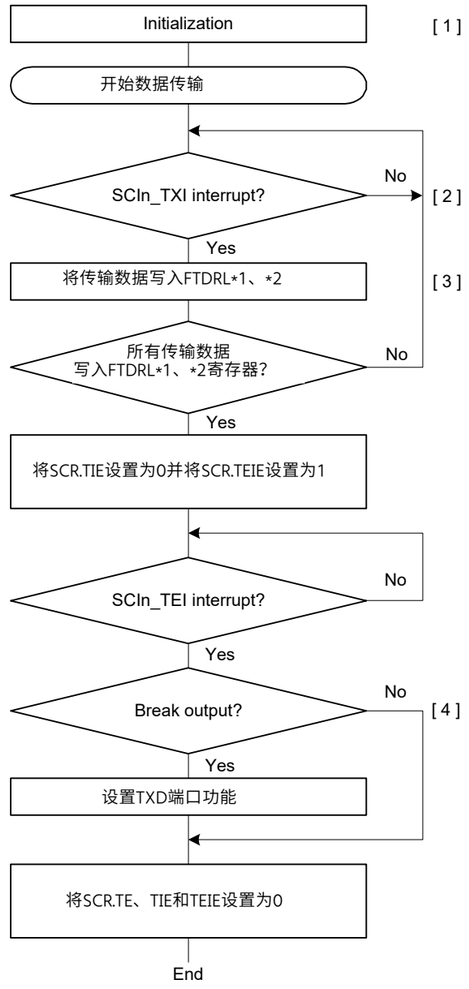
29.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

Figure 29.15 and Figure 29.16 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the RE bit in SCR becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the ORER flag in SSR is set to 1. If the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to RDR*1.
4. If a parity error is detected, the PER flag in SSR is set to 1 and receive data is transferred to RDR*1. If the RIE bit in



[1] SCI initialization:
设置数据传输。
SCR.TE设置为1后，对于一个帧（前导码）输出1，并启用传输。

[2] 通过SCIn_TXI中断请求将数据写入FTDRL*1：对于从FTDRL到TSR的数据传输，当写入FTDRL的发送数据量等于或小于指定的发送触发数时，发送数据FIFO空中断（SCIn_TXI）请求生成。在SCIn_TXI中断处理例程中将发送数据写入FTDRL*1、*2一次。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将所有传输数据写入FTDRL，并将SSR_FIFO.TDFE标志设置为0。可以写入16位传输数据，这也是传输FIFO中存储的数据量。也可以通过激活DMAC或DTC将传输数据写入FTDRL。当DMAC或DTC将数据写入FTDRL时，TDFE标志会自动清除。

因此，不要写入TDFE标志。
当SCIn_TEI中断请求正在使用时，设置
在要传输的最后一个数据写入FTDRL后，SCR.TIE为0，SCR.TEIE为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，请在使用SPTR.SPB2IO和SPTR.SPB2DT设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE设置为0。

Note 1. 当数据长度为9位时，使用FTDRH和FTDRL寄存器。
Note 2. 当数据长度为9位时，按照FTDRH到FTDRL的顺序写入。

Figure 29.14 选择FIFO的异步模式下串行传输示例流程

29.3.9 异步模式下的串行数据接收

(1) Non-FIFO selected

图29.15和图29.16显示了异步模式下串行数据接收操作的示例。

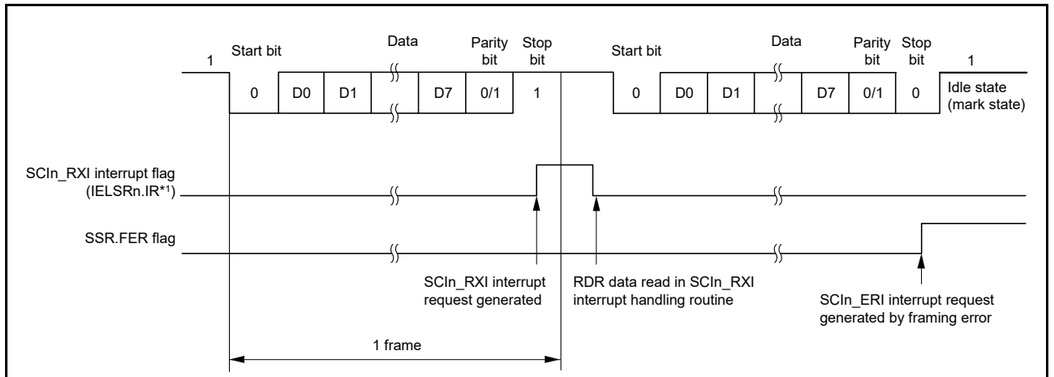
在串行数据接收中，SCI操作如下：

1. 当SCR中RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。
2. 当SCI监视通信线路并检测到起始位时，它会执行内部同步，将接收数据存储在RSR中，并检查奇偶校验位和停止位。
3. 如果发生溢出错误，则SSR中的ORER标志设置为1。如果SCR中的RIE位为1，则产生SCIn_ERI中断请求。接收数据不传输到RDR*1。
4. 如果检测到奇偶校验错误，则将SSR中的PER标志设置为1，并将接收数据传输到RDR*1。如果RIE位在

SCR is 1, an SCIn_ERI interrupt request is generated.

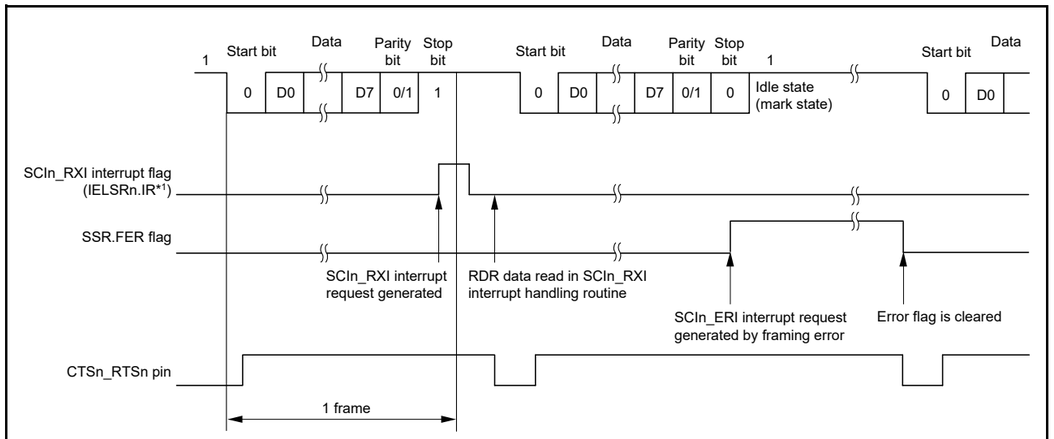
5. If a frame error is detected, the FER flag in the SSR is set to 1 and receive data is transferred to RDR*1. If the RIE bit in the SCR is 1, an SCIn_ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to RDR*1. If the RIE bit in the SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that was transferred to RDR causes the CTSn_RTSn pin to output low.

Note 1. Only read data in RDRHL when 9-bit data length is selected.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.15 Example of SCI operation for serial reception in asynchronous mode (1) when RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.16 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

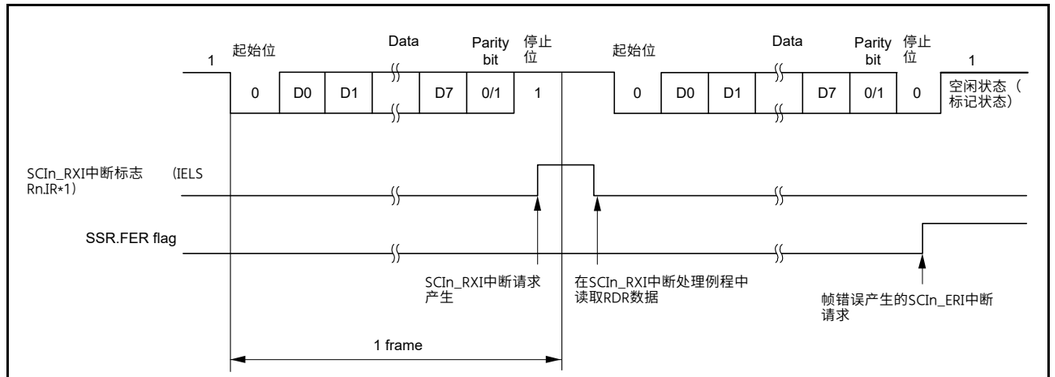
Table 29.23 lists the states of the flags in the SSR register and the receive data handling when a receive error is detected.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed when the receive error flag is 1. Also, set the ORER, FER, and PER flags to

SCR为1，产生SCIn_ERI中断请求。

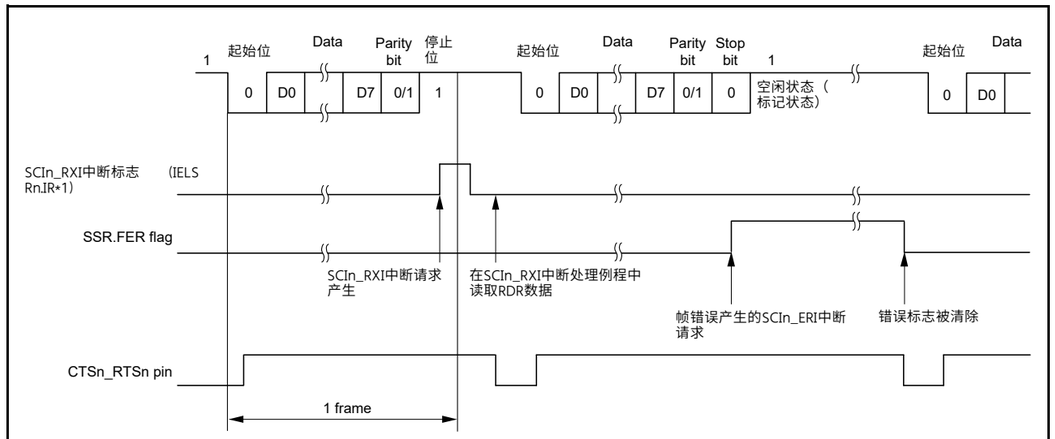
5. 如果检测到帧错误，则将SSR中的FER标志设置为1，并将接收数据传输到RDR*1。如果SCR中的RIE位为1，则产生SCIn_ERI中断请求。
6. 当接收成功完成时，接收数据被传输到RDR*1。如果SCR中的RIE位为1，则SCIn_RXI中断请求产生。在接收下一个接收数据完成之前，通过在SCIn_RXI中断处理例程中读取传输到RDR的接收数据来启用连续接收。读取传输到RDR的接收数据会导致CTSn_RTSn引脚输出低电平。

注1.选择9位数据长度时，仅读取RDRHL中的数据。



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.15 异步模式下串行接收的SCI操作示例(1)不使用RTS功能，8位数据、奇偶校验位和1个停止位



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.16 使用RTS功能，8位数据、奇偶校验位和1个停止位时，异步模式下串行接收的SCI操作示例(2)

表29.23列出了SSR寄存器中标志的状态以及检测到接收错误时的接收数据处理。

如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。接收错误标志为1时无法恢复数据接收。另外，请将ORER、FER和PER标志设置为

0 before resuming reception. In addition, be sure to read RDR or RDRHL during overrun error processing. When reception is forcibly terminated by setting the RE bit in SCR to 0 during operation, read RDR or RDRHL because the received data that is not read might be left in RDR or RDRHL.

Figure 29.17 and Figure 29.18 show example flows for serial data reception.

Table 29.23 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register				
ORER	**FER**	**PER**	**Received data**	**Receive error type**
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR	Framing error
0	0	1	Transferred to RDR	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note: Only read data in the RDRHL register when 9-bit data length is selected.

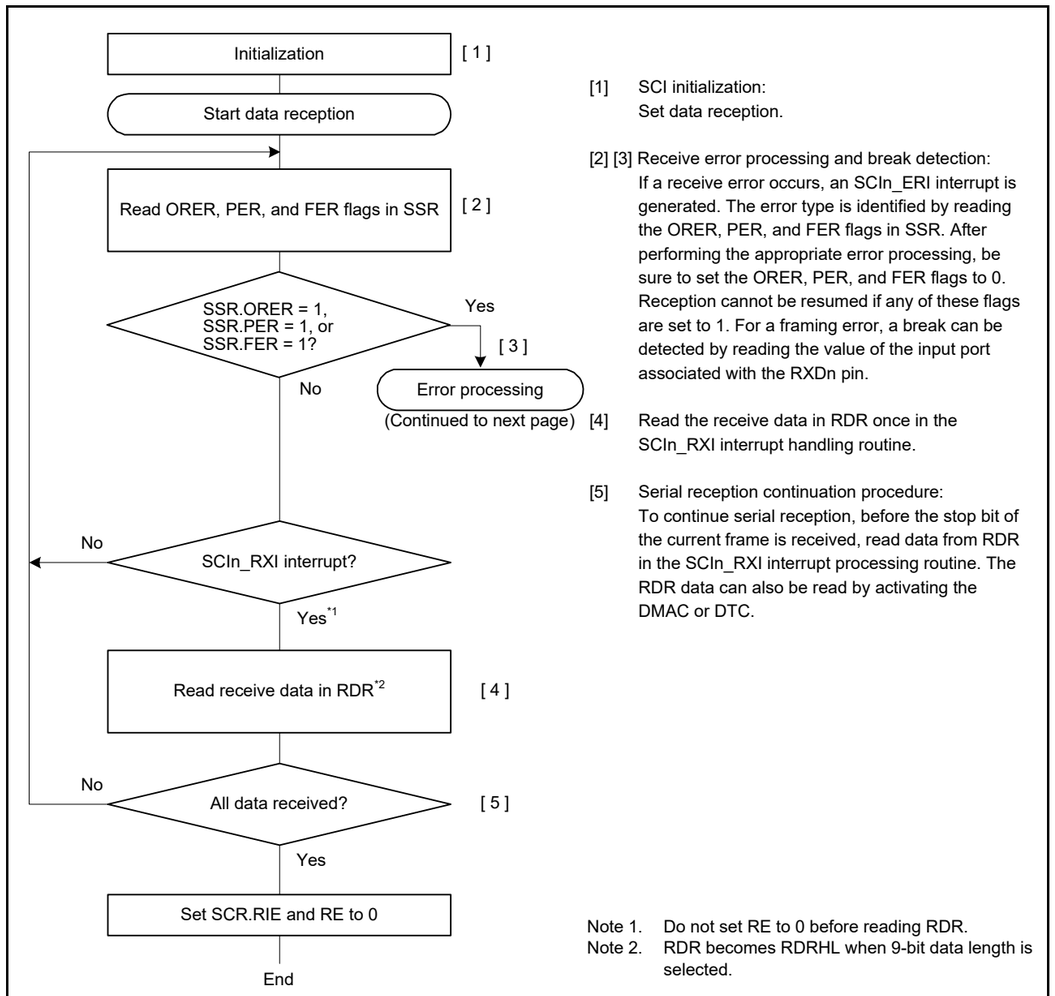
0恢复接收前。此外，请务必在溢出错误处理期间读取RDR或RDRHL。如果在操作期间通过将SCR中的RE位设置为0来强制终止接收，请读取RDR或RDRHL，因为未读取的接收数据可能会留在RDR或RDRHL中。

图29.17和图29.18显示了串行数据接收的示例流程。

Table 29.23 SSR状态寄存器中的标志和接收数据处理

SSR状态寄存器中的标志				
ORER	**FER**	**PER**	**接收数据**	**接收错误类型**
1	0	0	Lost	溢出错误
0	1	0	转移到RDR	构图错误
0	0	1	转移到RDR	奇偶校验错误
1	1	0	Lost	溢出错误+成帧错误
1	0	1	Lost	溢出错误+奇偶校验错误
0	1	1	转移到RDR	成帧错误+奇偶校验错误
1	1	1	Lost	溢出错误+帧错误+奇偶校验错误

Note: 仅在选择9位数据长度时读取RDRHL寄存器中的数据。



[1] SCI initialization:
Set data reception.

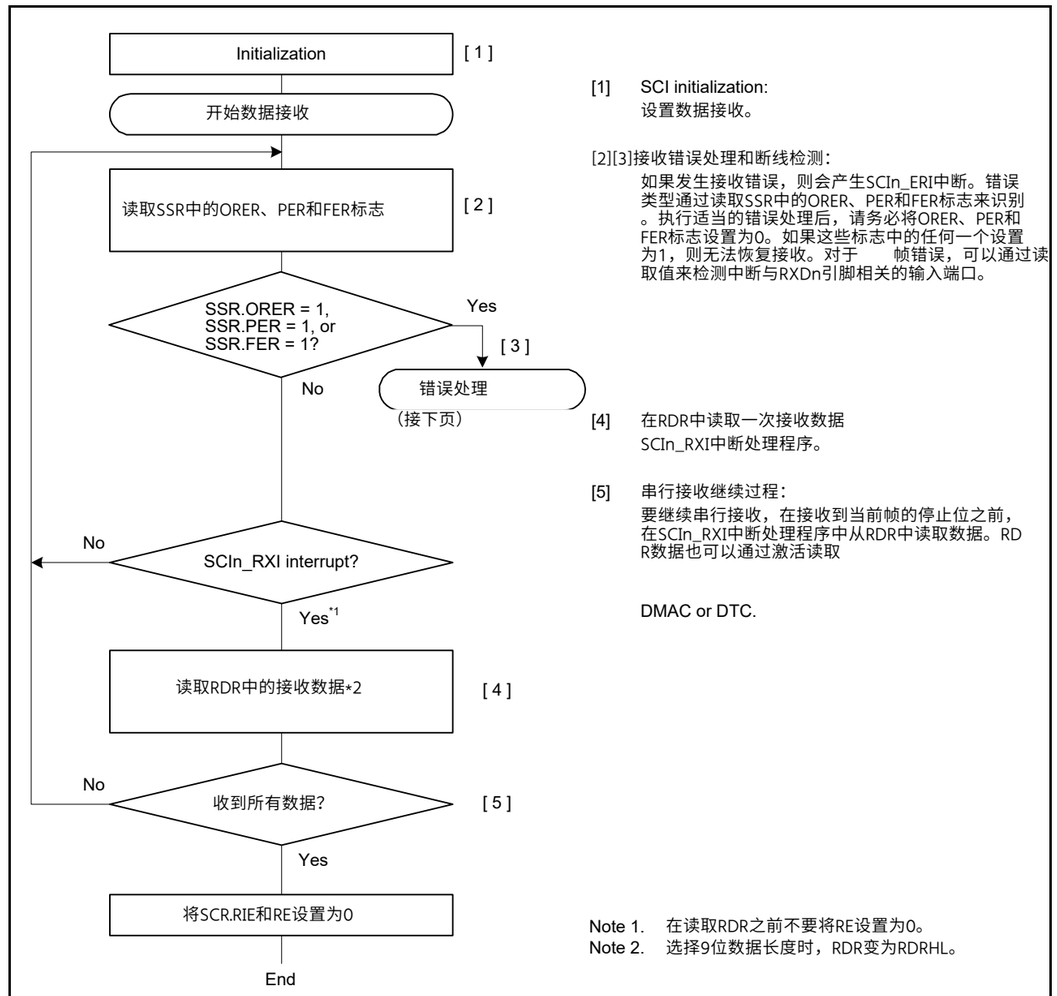
[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. The error type is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags are set to 1. For a framing error, a break can be detected by reading the value of the input port associated with the RXDn pin.

[4] Read the receive data in RDR once in the SCIn_RXI interrupt handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the SCIn_RXI interrupt processing routine. The RDR data can also be read by activating the DMAC or DTC.

Note 1. Do not set RE to 0 before reading RDR.
Note 2. RDR becomes RDRHL when 9-bit data length is selected.

Figure 29.17 Example flow of serial reception in asynchronous mode with non-FIFO selected (1)



[1] SCI initialization:
设置数据接收。

[2][3]接收错误处理和断线检测：
如果发生接收错误，则会产生SCIn_ERI中断。错误类型通过读取SSR中的ORER、PER和FER标志来识别。执行适当的错误处理后，请务必将ORER、PER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。对于 帧错误，可以通过读取值来检测中断与RXDn引脚相关的输入端口。

[4] 在RDR中读取一次接收数据
SCIn_RXI中断处理程序。

[5] 串行接收继续过程：
要继续串行接收，在接收到当前帧的停止位之前，在SCIn_RXI中断处理程序中从RDR中读取数据。RDR数据也可以通过激活读取

DMAC or DTC.

Note 1. 在读取RDR之前不要将RE设置为0。
Note 2. 选择9位数据长度时，RDR变为RDRHL。

Figure 29.17 选择非FIFO的异步模式下串行接收示例流程(1)

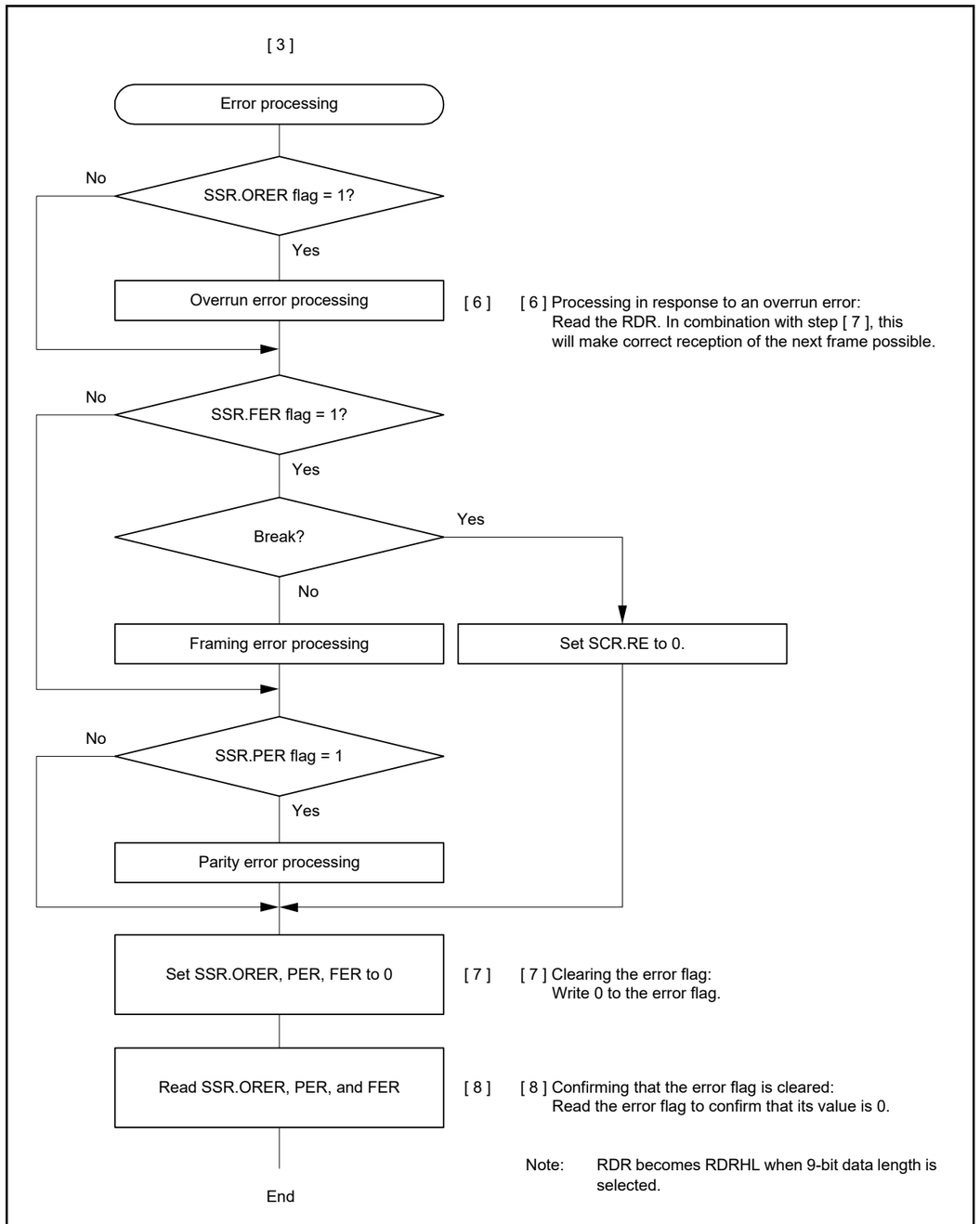


Figure 29.18 Example flow of serial reception in asynchronous mode with non-FIFO selected (2)

(2) FIFO selected

Figure 29.19 shows an example of a data format that is written to FRDRH and FRDRL in asynchronous mode.

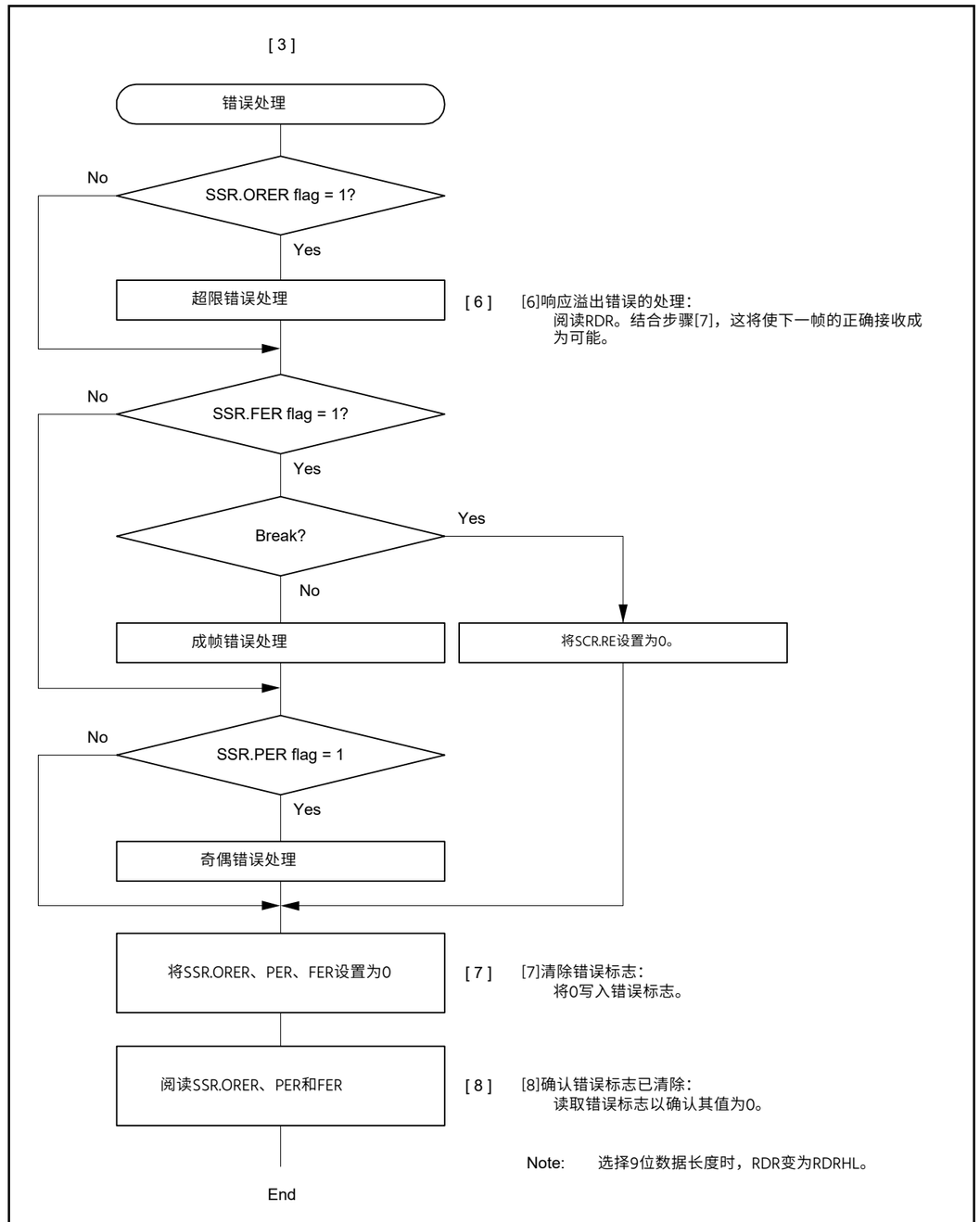


Figure 29.18 选择非FIFO的异步模式下串行接收示例流程(2)

(2) FIFO selected

图29.19显示了以异步模式写入FRDRH和FRDRL的数据格式示例。

In asynchronous mode, 0 is written to the MPB flag bit in the FRDRH register. Data that corresponds to the data length is written to FRDRH and FRDRL. Unused bits are written as 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, SCI updates FER, PER and receive data (RDAT[8:0]) in the FRDRL register with the next data. The RDF, ORER, and DR flags in FRDRH always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL														
			FRDRHL														
			FRDRH								FRDRL						
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

Note: 0 is always read for MPB flag (FRDRH[1]).
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7].
When data length is 8 bits, 0 is always read for FRDRH[0].
FRDRH[7] bit is read as an indefinite value.

Figure 29.19 Data format stored to FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the RE bit in SCR becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. When the FRDRL register is full, an overrun error occurs. If an overrun error occurs, the ORER flag in SSR_FIFO is set to 1. When the RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to FRDRL*1.
4. If a parity error is detected, the PER flag and receive data are transferred to FRDRL*1. When RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
5. If a frame error is detected, the FER flag and receive data are transferred to FRDRL*1. When RIE is set to 1, an SCIn_ERI interrupt request is generated.
6. After a frame error is detected and when SCI detects that the continuous receive data is for one frame, reception stops.
7. When the amount of data stored in the receive FIFO data register (FRDRL) falls below the specified receive triggering number, and the next data is not received after 15 ETUs from the last stop bit in asynchronous mode, the DR bit in SSR_FIFO is set to 1. When RIE is 1 and the DRES bit in FCR register is 0, SCI generates an SCIn_RXI interrupt request. When the DRES bit is 1, SCI generates an SCIn_ERI interrupt request.
8. When reception finishes successfully, receive data is transferred to FRDRL*1. RDF is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. When the RIE is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*3 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. Only read the data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 2. Read the data in order from FRDRH to FRDRL when 9-bit data length is selected.
Note 3. The SCI only checks for updates to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.

在异步模式下，将0写入FRDRH寄存器中的MPB标志位。对应于数据长度的数据被写入FRDRH和FRDRL。未使用的位写为0。按从FRDRH到FRDRL的顺序读取。如果软件读取FRDRL，SCI会用下一个数据更新FER、PER和FRDRL寄存器中的接收数据（RDAT[8:0]）。RDF，

FRDRH中的ORER和DR标志始终反映SSR_FIFO寄存器中的相关标志。

数据长度	寄存器设置		在FRDRH、FRRDL中接收数据														
			FRDRHL														
			FRDRH								FRDRL						
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8位接收数据							
9 bits	0	不在乎	—	RDF	ORER	FER	PER	DR	0	9位接收数据								

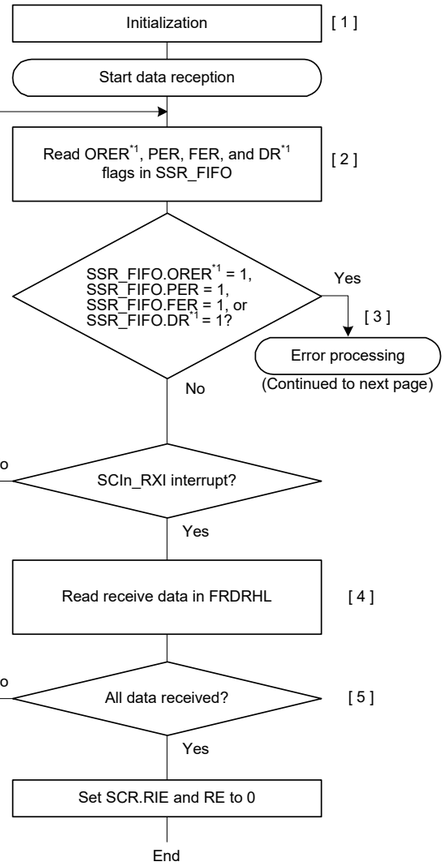
Note: MPB标志(FRDRH[1])总是读取0。当数据长度为7位时，FRRDH[0]和FRDRL[7]总是读取0。
当数据长度为8位时，FRRDH[0]总是读取0。
FRDRH[7]位被读取为不定值。

Figure 29.19 选择FIFO时存储到FRDRH和FRDRL的数据格式

在串行数据接收中，SCI操作如下：

1. 当SCR中RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。
2. 当SCI监视通信线路并检测到起始位时，它会执行内部同步，将接收数据存储在RSR中，并检查奇偶校验位和停止位。
3. 当FRDRL寄存器已满时，会发生溢出错误。如果发生溢出错误，则SSR_FIFO中的ORER标志设置为1。当RIE位为1时，将产生SCIn_ERI中断请求。接收数据不传输到FRDRL*1。
4. 如果检测到奇偶校验错误，则将PER标志和接收数据传输到FRDRL*1。当RIE位设置为1时，一个SCIn_ERI中断请求产生。
5. 如果检测到帧错误，则将FER标志和接收数据传输到FRDRL*1。当RIE设置为1时，SCIn_ERI中断请求产生。
6. 检测到帧错误后，当SCI检测到连续接收数据为一帧时，接收停止。
7. 当接收FIFO数据寄存器(FRDRL)中存储的数据量低于指定的接收触发数，并且在异步模式下距最后一个停止位15个ETU后没有接收到下一个数据时，SSR_FIFO中的DR位设置为1.当RIE为1且FCR寄存器中的DRES位为0时，SCI产生一个SCIn_RXI中断请求。当DRES位为1时，SCI产生一个SCIn_ERI中断请求。
8. 当接收成功完成时，接收数据被传输到FRDRL*1。当写入FRDRHL的接收数据量等于或大于指定的接收触发数时，RDF设置为1。当RIE为1时，产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理程序中读取传输到FRDRL*2的接收数据来启用连续接收。如果传送到FRDRL*3的接收数据小于RTS触发数，CTSn_RTSn引脚输出低电平。

注1.选择9位数据长度时，仅读取FRDRH和FRDRL寄存器中的数据。
注2.选择9位数据长度时，按从FRDRH到FRDRL的顺序读取数据。
Note3.TheSCIonlychecksforupdatestotheFRDRLregisterandnottotheFRDRHregisterwhen9-bitdatalengthisselected.



[1] SCI initialization:
Set data reception.

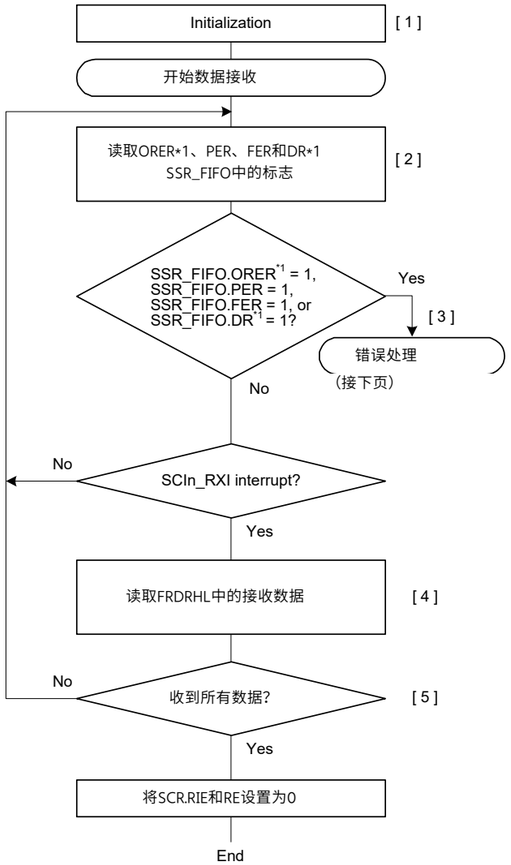
[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON bit. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if the ORER*1 flag is set to 1. The reception operation is continuous, even if the FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The receive data stored in the FRDRHL register is read until the amount of stored data is below the FCR.RTRG value. Confirm the number of the receive data bits in the FIFO by FDR.R bits.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF and DR flags to 0.
The FRDRHL data can also be read by activating the DMAC or DTC. The RDF flag is cleared automatically in this case. Therefore, do not write to the RDF flag.

Note 1. Can be read by the FRDRHL.ORER and DR flags.

Figure 29.20 Example flow of serial reception in asynchronous mode with FIFO selected (1)



[1] SCI initialization:
设置数据接收。

[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。可以通过读取SPTR.RXDMON位来检测中断。通过读取SSR_FIFO中的ORER*1、PER、DR*1和FER标志来识别错误。执行适当的错误处理后，请务必将ORER*1标志设置为0。如果ORER*1标志设置为1，则无法恢复接收。接收操作是连续的，即使FER=1或PER=1或DR*1=1。

[4] 在FRDRHL中读取接收数据
SCIn_RXI中断处理程序。读取存储在FRDRHL寄存器中的接收数据，直到存储的数据量低于FCR.RTRG值。通过FDR.R位确认FIFO中接收数据的位数。

[5] 串行接收继续过程：
要继续串行接收，在发生溢出错误之前，在SCIn_RXI中断处理程序中从FRDRHL读取数据并清除

RDF和DR标志为0。
也可以通过激活DMAC或DTC来读取FRDRHL数据。在这种情况下，RDF标志会自动清除。因此，不要写入RDF标志。

Note 1. 可以通过FRDRHL.ORER和DR标志读取。

Figure 29.20 选择FIFO的异步模式下串行接收示例流程(1)

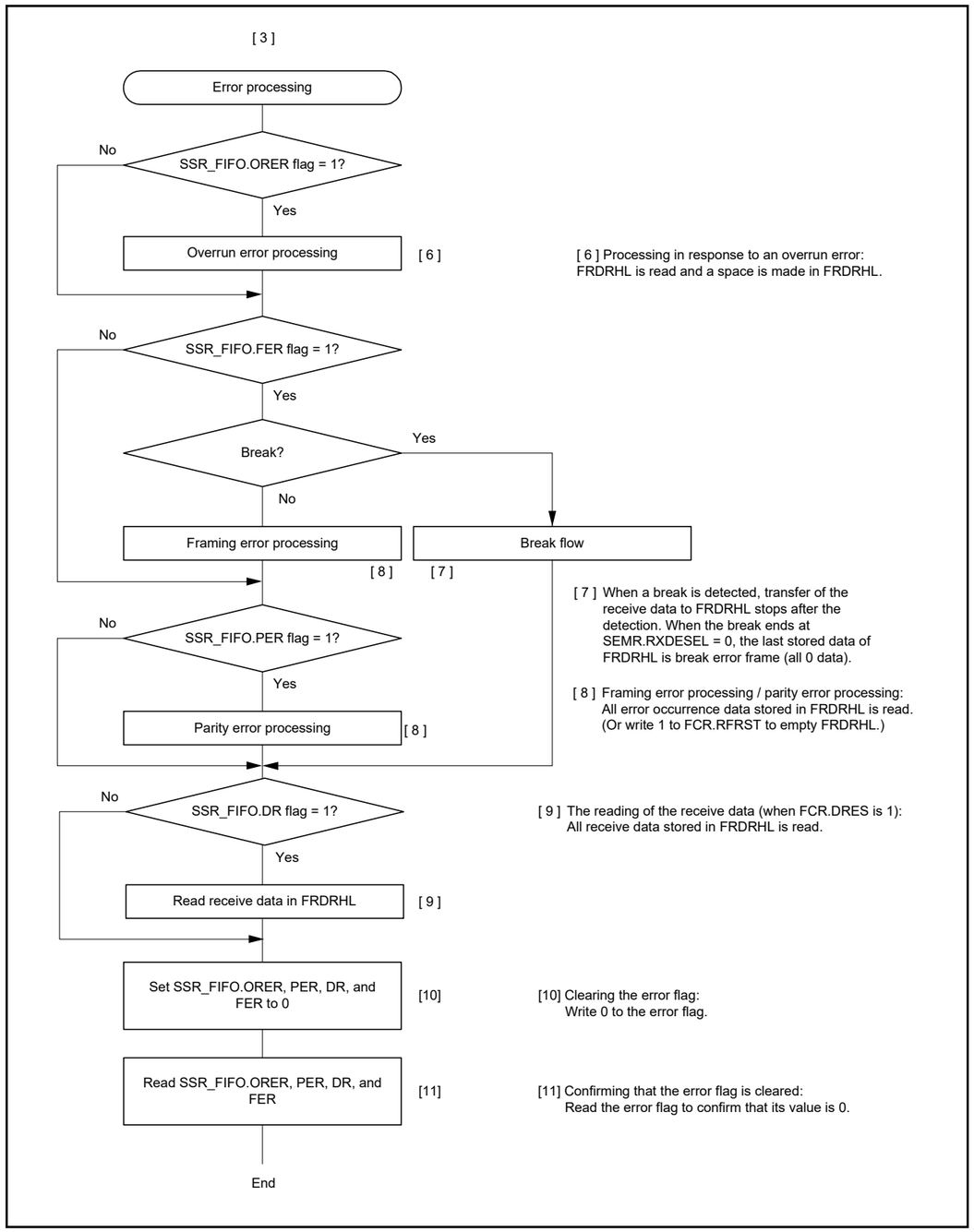


Figure 29.21 Example flow of serial reception in asynchronous mode with FIFO selected (2)

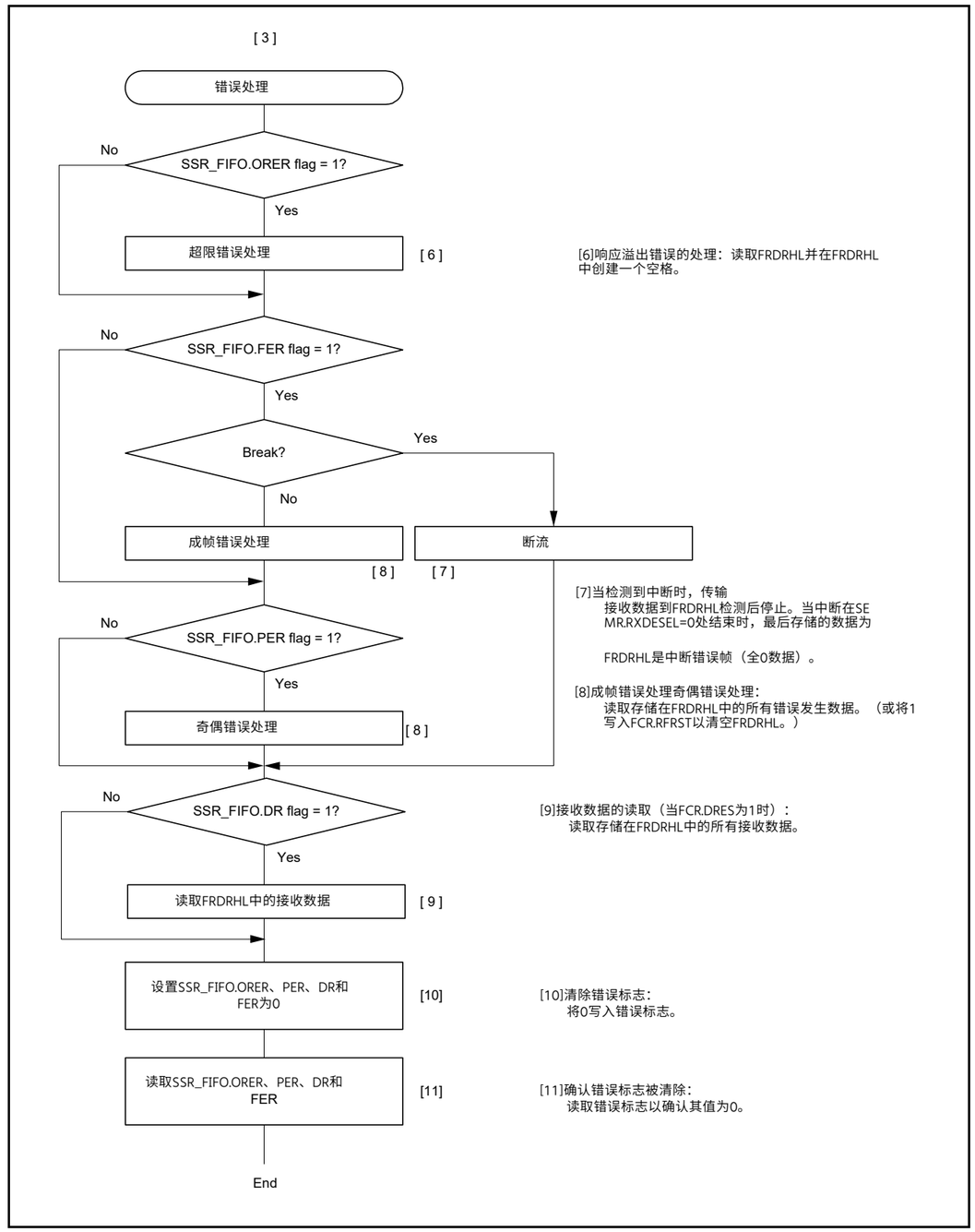


Figure 29.21 选择FIFO的异步模式下串行接收示例流程(2)

29.4 Multi-Processor Communications Function

The multi-processor communication function enables the SCI to transmit and receive data by sharing a communication line between multiple processors, using asynchronous serial communication in which the multi-processor bit is added. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle.

Figure 29.22 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1, is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0, is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives the data again in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the MPIE bit in SCR. When MPIE is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from RSR to RDR (RDRHL when 9-bit data length is selected)
- Detection of a receive error
- Setting the respective status flags RDRF, ORER, and FER in SSR

On receiving a character in which the multi-processor bit is set to 1, the MPBT bit in SSR is set to 1 and the MPIE bit in SCR is automatically cleared, returning the SCI to a non multi-processor reception operation. An SCIn_RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in non multi-processor asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in non multi-processor asynchronous mode.

29.4 多处理器通信功能

多处理器通信功能使SCI通过在多个处理器之间共享一条通信线路，使用添加了多处理器位的异步串行通信来发送和接收数据。在多处理器通信中，为每个接收站分配一个唯一的ID代码。串行通信周期由指定接收站的ID传输周期和向指定接收站传输数据的数据传输周期组成。

多处理器位用于区分ID传输周期和数据传输周期：

- 当多处理器位设置为1时，发送周期为ID发送周期
- 当多处理器位设置为0时，传输周期为数据传输周期。

图29.22显示了使用多处理器格式的处理器之间的通信示例。首先，发送站发送将多处理器位设置为1的通信数据，该通信数据被添加到接收站的ID码。接着，发送站发送将多处理器位设置为0的通信数据被添加到发送数据。接收站接收到多处理器位设置为1的通信数据后，将接收到的ID与接收站自身的ID进行比较。如果两者匹配，则接收站接收随后发送的通信数据。如果接收到的ID与接收站的ID不匹配，则接收站跳过通信数据，直到再次接收到多处理器位设置为1的数据。

(1) Non-FIFO selected

为了支持这个功能，SCI在SCR中提供了MPIE位。当MPIE设置为1时，将禁用以下操作，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR传输到RDR（选择9位数据长度时为RDRHL）
- 检测接收错误
- 在SSR中设置相应的状态标志RDRF、ORER和FER

接收到多处理器位设置为1的字符时，SSR中的MPBT位设置为1，并且SCR中的MPIE位自动清零，将SCI返回到非多处理器接收操作。如果SCR中的RIE位置位，则会产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与非多处理器异步模式下的操作没有区别。多处理器通信使用的时钟与非多处理器异步模式使用的时钟相同。

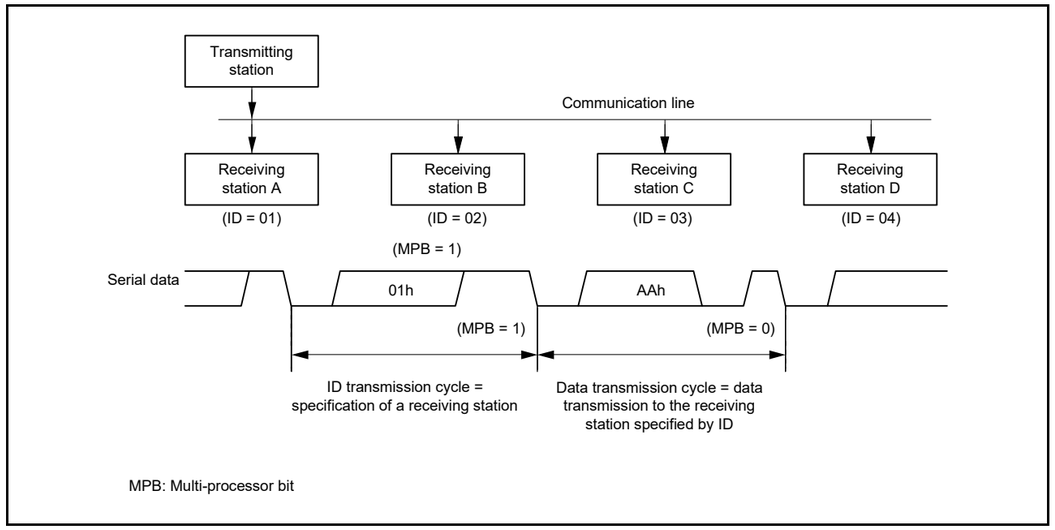


Figure 29.22 Example of communication using multi-processor format with transmission of data AAh to receiving station A

(2) FIFO selected

For data transmission, software must write data to the MPBT bit in FTDRHL register that corresponds to transmit data in the TDAT bit in FTDRHL register. For data reception, the multi-processor bit that is part of the receive data is written to the MPB bit in FRDRHL register and receive data is written to FRDRL register.

When the MPIE bit is set to 1, the following functions are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from RSR to FRDRHL register
- Detection of a receive error
- Break
- Setting of the respective status flags RDF, ORER, and FER in SSR_FIFO register.

On receiving an 8-bit character in which the multi-processor bit is set to 1, the MPB bit in FRDRHL is set to 1 and receive data is written to the RDAT bit in FRDRHL. The MPIE bit in SCR is automatically cleared, therefore returning the SCI to non multi-processor reception operation. An SCIn_RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference in operation from non multi-processor asynchronous mode with FIFO selected.

29.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 29.23 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the MPBT bit in SSR set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as in asynchronous mode.

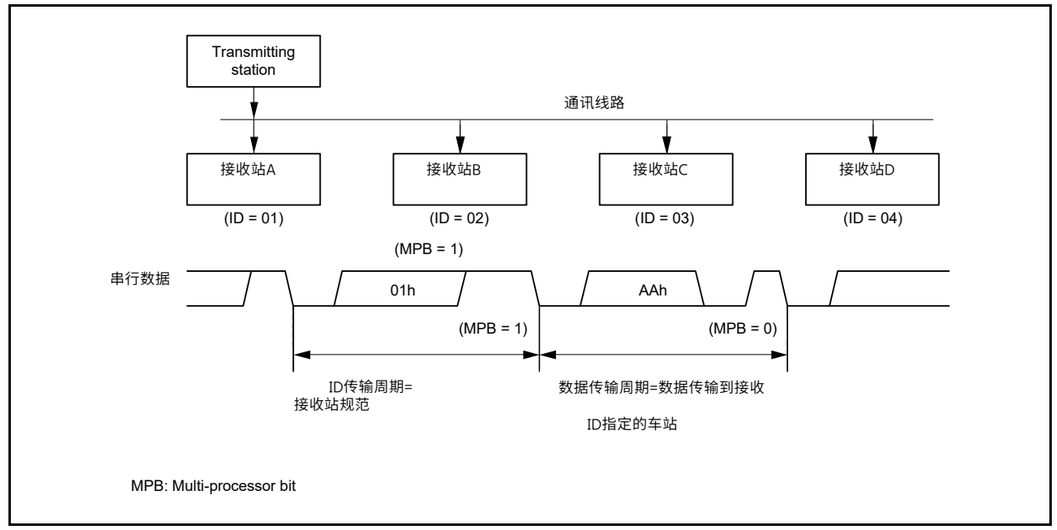


Figure 29.22 使用多处理器格式的通信示例，将数据AAh传输到接收站A

(2) FIFO selected

对于数据传输，软件必须将数据写入FTDRHL寄存器中的MPBT位，该位对应于FTDRHL寄存器中的TDAT位中的传输数据。对于数据接收，作为接收数据一部分的多处理器位被写入FRDRHL寄存器的MPB位，接收数据被写入FRDRL寄存器。

当MPIE位设置为1时，以下功能将被禁用，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR传送到FRDRHL寄存器
- 检测接收错误
- Break
- 在SSR_FIFO寄存器中设置相应的状态标志RDF、ORER和FER。

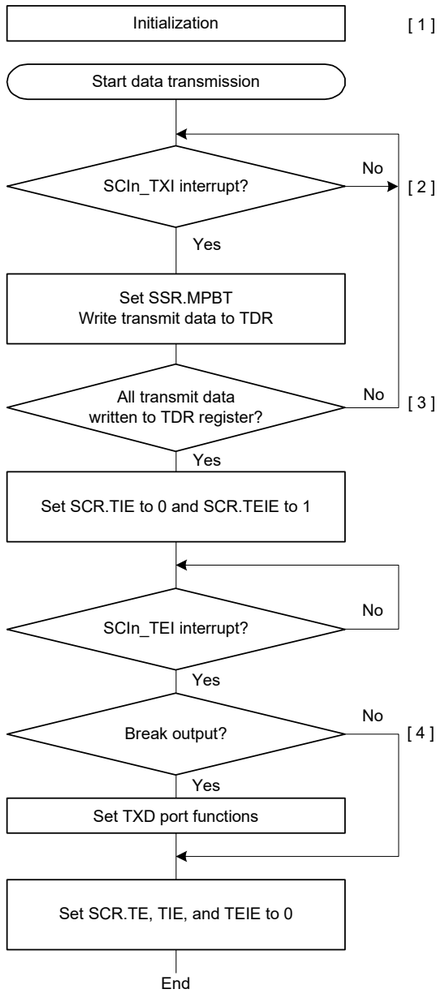
接收到多处理器位设置为1的8位字符时，FRDRHL中的MPB位设置为1，接收数据写入FRDRHL中的RDAT位。SCR中的MPIE位自动清零，因此SCI将返回到非多处理器接收操作。如果SCR中的RIE位置位，则会产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与选择FIFO的非多处理器异步模式的操作没有区别。

29.4.1 多处理器串行数据传输

(1) Non-FIFO selected

图29.23显示了一个多处理器数据传输的示例流程。在ID传输周期，ID必须在SSR中的MPBT位设置为1的情况下传输。在数据传输周期，数据必须在MPBT位设置为0的情况下传输。其余操作与中相同异步模式。



[1] SCI initialization:
Set data transmission.
After SCR.TE is set to 1, 1 is output for a frame, and transmission is enabled.

[2] SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Set SSR.MPBT to 0 or 1, and write transmit data to TDR in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request.
Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set SCR.TIE to 0 and SCR.TEIE to 1 after the last of the data to be transmitted is written to TDR.

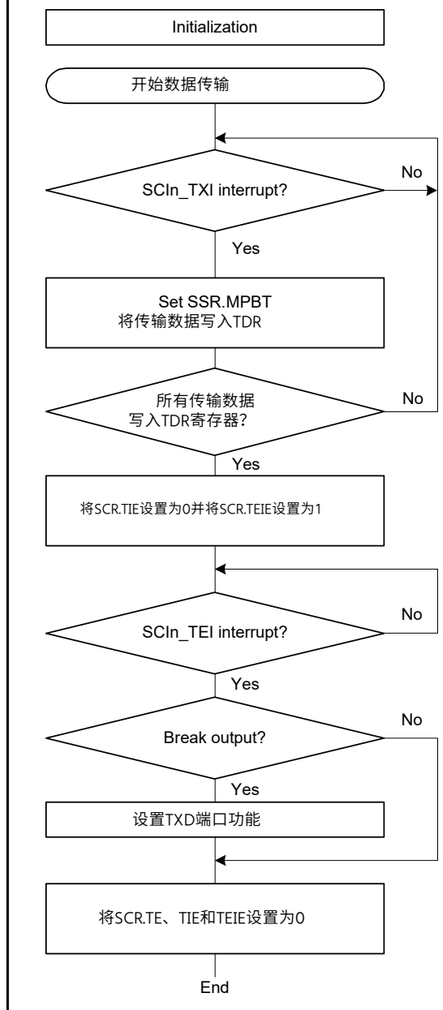
[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set SCR.TE to 0.

Figure 29.23 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 29.24 shows an example of data format that is written to FTDRH and FTDRL in multi-processor mode.

MPBT is set to 1 in FTDRH register. Data is set to FTDRH and FTDRL with the correct data length. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI initialization:
设置数据传输。
SCR.TE置1后，每帧输出1，使能传输。

[2] SCIn_TXI interrupt request:
当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。将SSR.MPBT设置为0或1，并在SCIn_TXI中断处理程序中将发送数据写入TDR。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据写入TDR一次。也可以通过激活DMAC或DTC将传输数据写入TDR。

使用SCIn_TEI中断请求时，将要传输的最后一个数据写入TDR后，将SCR.TIE设置为0，并将SCR.TEIE设置为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE设置为0。

Figure 29.23 选择非FIFO的多处理器串行传输示例流程

(2) FIFO selected

图29.24显示了在多处理器模式下写入FTDRH和FTDRL的数据格式示例。

MPBT在FTDRH寄存器中设置为1。数据设置为具有正确数据长度的FTDRH和FTDRL。为未使用的位写入0。从FTDRH到FTDRL的顺序写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL													
			FTDRHL													
			FTDRH								FTDRL					
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

—: Invalid. The write value should be 0.

Figure 29.24 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

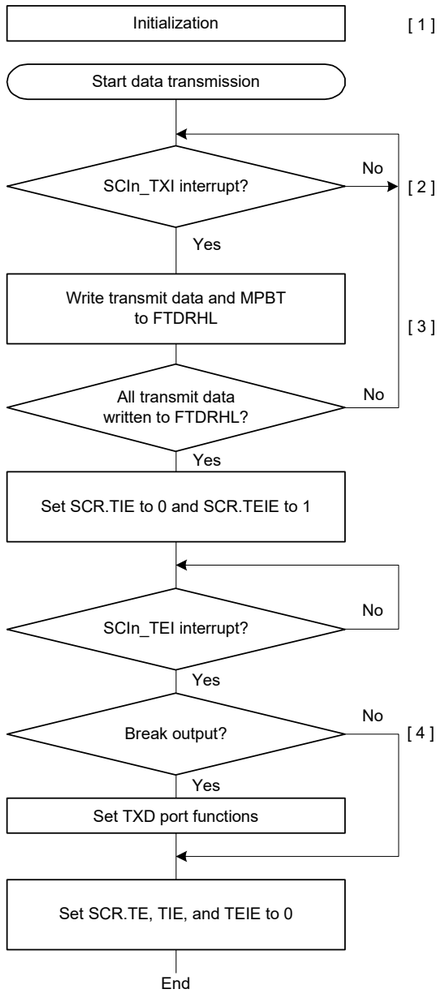
Figure 29.25 shows an example flow of multi-processor data transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the MPBT bit in FTDRH set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据													
			FTDRHL													
			FTDRH								FTDRL					
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8位传输数据							
9 bits	0	不在乎	—	—	—	—	—	—	MPBT	9位传输数据								

-：无效的。写入值应为0。

Figure 29.24 在选择FIFO的多处理器模式下写入FTDRH和FTDRL的数据格式

图29.25显示了选择FIFO的多处理器数据传输示例流程。在ID传输周期中，必须在FTDRH中的MPBT位设置为1的情况下传输ID。在数据传输周期中，必须在MPBT位设置为0的情况下传输数据。其余操作与操作相同在异步模式下选择FIFO。



[1] SCI initialization:
Set data transmission.
After SCR.TE is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRHL by an SCIn_TXI interrupt request:
For data transmission from FTDRHL to TSR, when the amount of receive data written in FTDRHL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data and MPBT to FTDRHL once using an SCIn_TXI interrupt request.
Transmit data can also be written to FTDRHL by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set SCR.TIE to 0 and SCR.TEIE to 1 after the last of the data to be transmitted is written to the FTDRHL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (low level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set SCR.TE to 0.

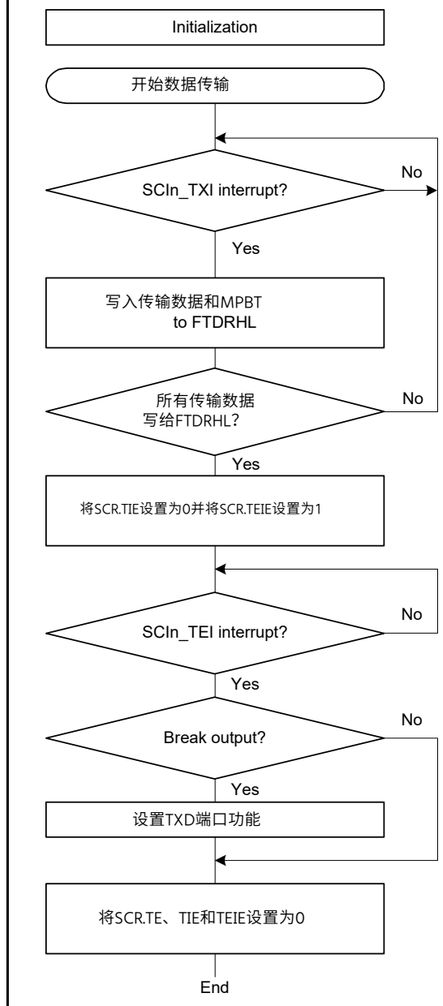
Figure 29.25 Example flow of serial transmission in multi-processor mode with FIFO selected

29.4.2 Multi-Processor Serial Data Reception

(1) Non-FIFO selected

Figure 29.26 and Figure 29.27 show example flows of multi-processor data reception. When the MPIE bit in SCR is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to RDR, or RDRHL when 9-bit data length is selected, and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as in asynchronous mode.

Figure 29.26 shows an example operation for data reception.



[1] SCI initialization:
设置数据传输。
SCR.TE置1后，每帧输出1，使能传输。

[2] 通过SCIn_TXI中断请求将数据写入FTDRHL：对于从FTDRHL到TSR的数据传输，当写入FTDRHL的接收数据量等于或小于指定的发送触发数时，发送数据FIFO空中断（SCIn_TXI）请求生成。

[3] 串行传输继续程序：
要继续串行传输，写入传输数据和MPBT到FTDRHL一次使用SCIn_TXI中断请求。也可以通过激活DMAC或DTC将传输数据写入FTDRHL。使用SCIn_TEI中断请求时，在将要传输的最后一个数据写入FTDRHL后，将SCR.TIE设置为0，并将SCR.TEIE设置为1。

[4] 串行传输结束时中断输出：要在串行传输中输出中断，通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE设置为0。

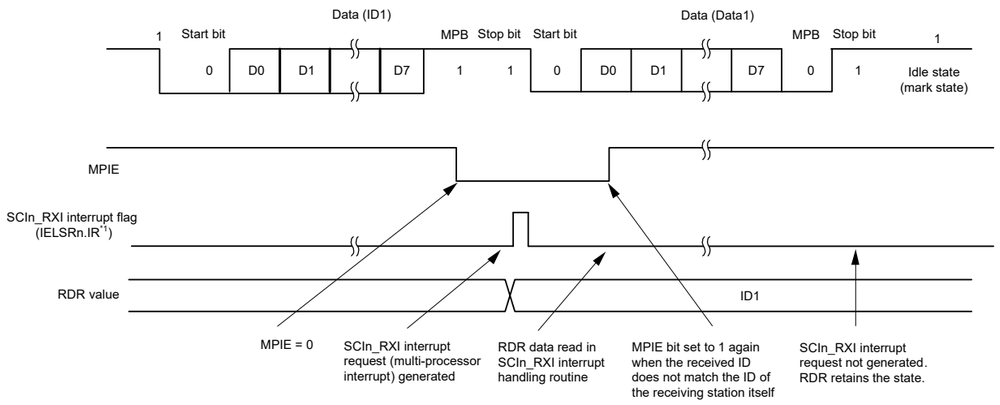
Figure 29.25 选择FIFO的多处理器模式下的串行传输示例流程

29.4.2 多处理器串行数据接收

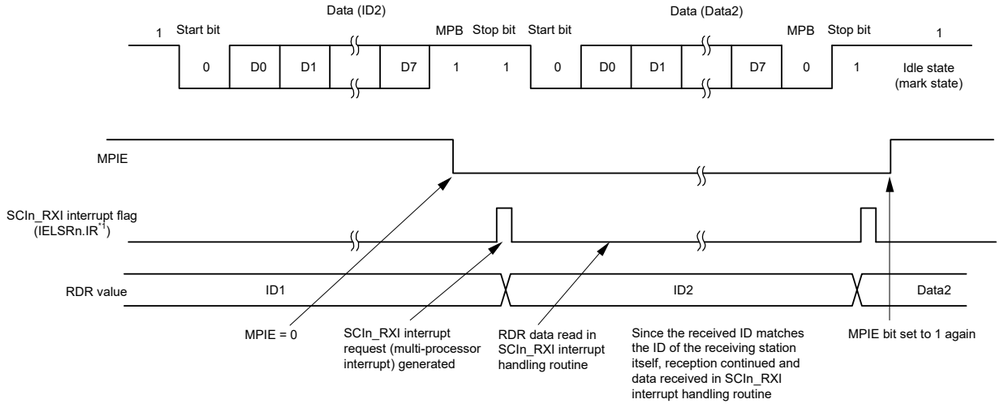
(1) Non-FIFO selected

图29.26和图29.27显示了多处理器数据接收的示例流程。当SCR中的MPIE位设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，选择9位数据长度并生成SCIN_RXI中断请求时，接收到的数据将传输到RDR或RDRHL。其余操作与异步模式相同。

图29.26显示了数据接收的示例操作。



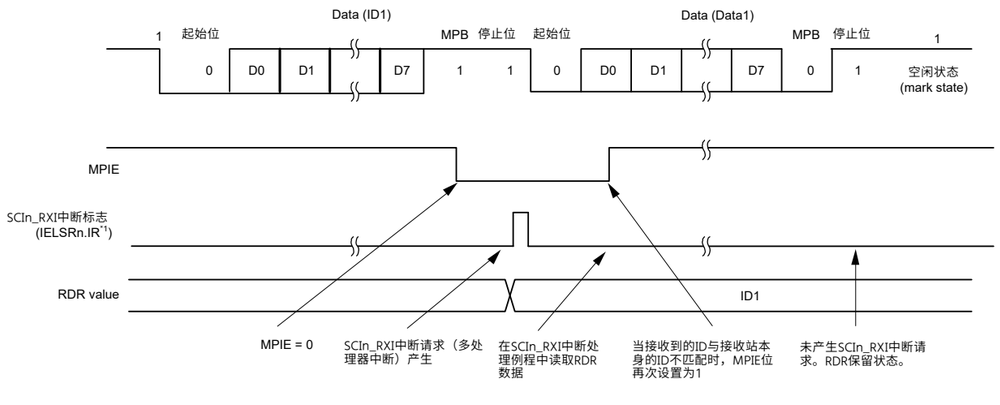
(a) When the received ID does not match the ID of the receiving station itself



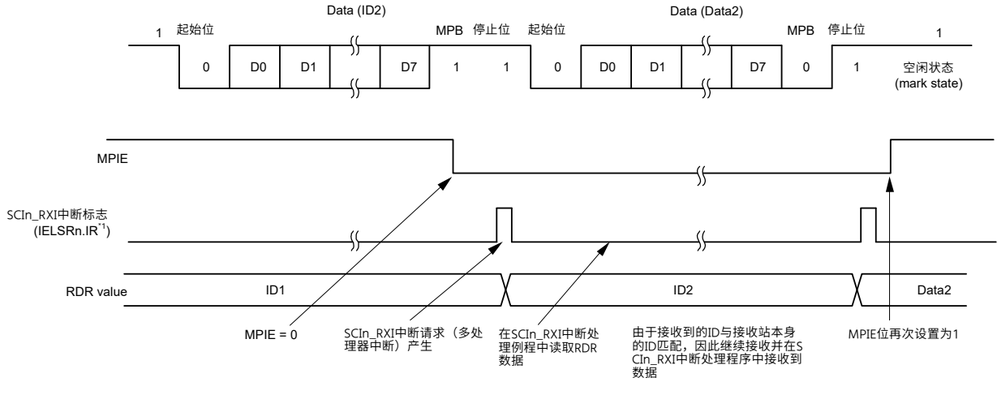
(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.26 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



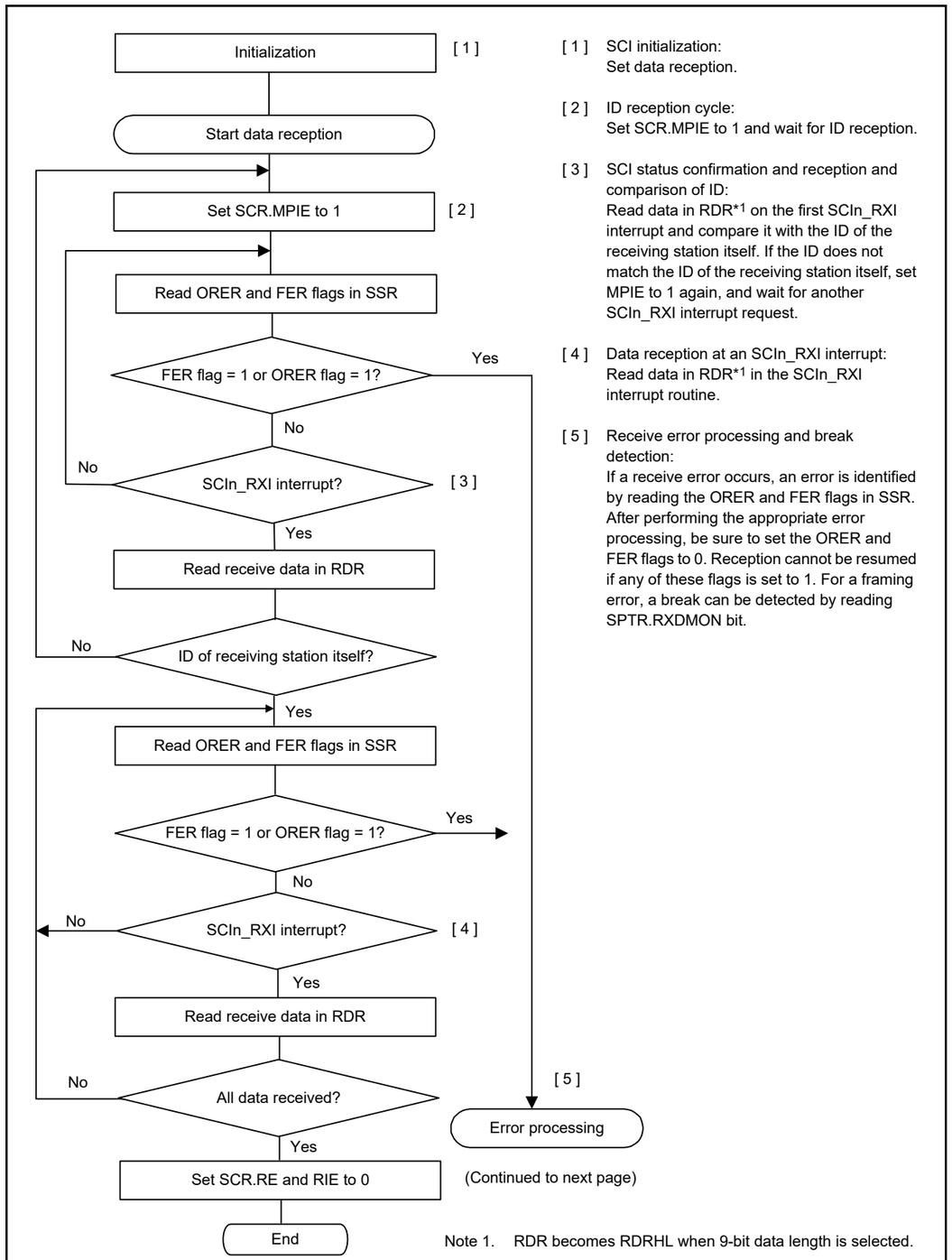
(a)当接收到的ID与接收站本身的ID不匹配时



(b)当接收到的ID与接收站本身的ID匹配时

Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.26 使用8位数据、多处理器位和1个停止位的SCI接收示例



[1] SCI initialization:
Set data reception.

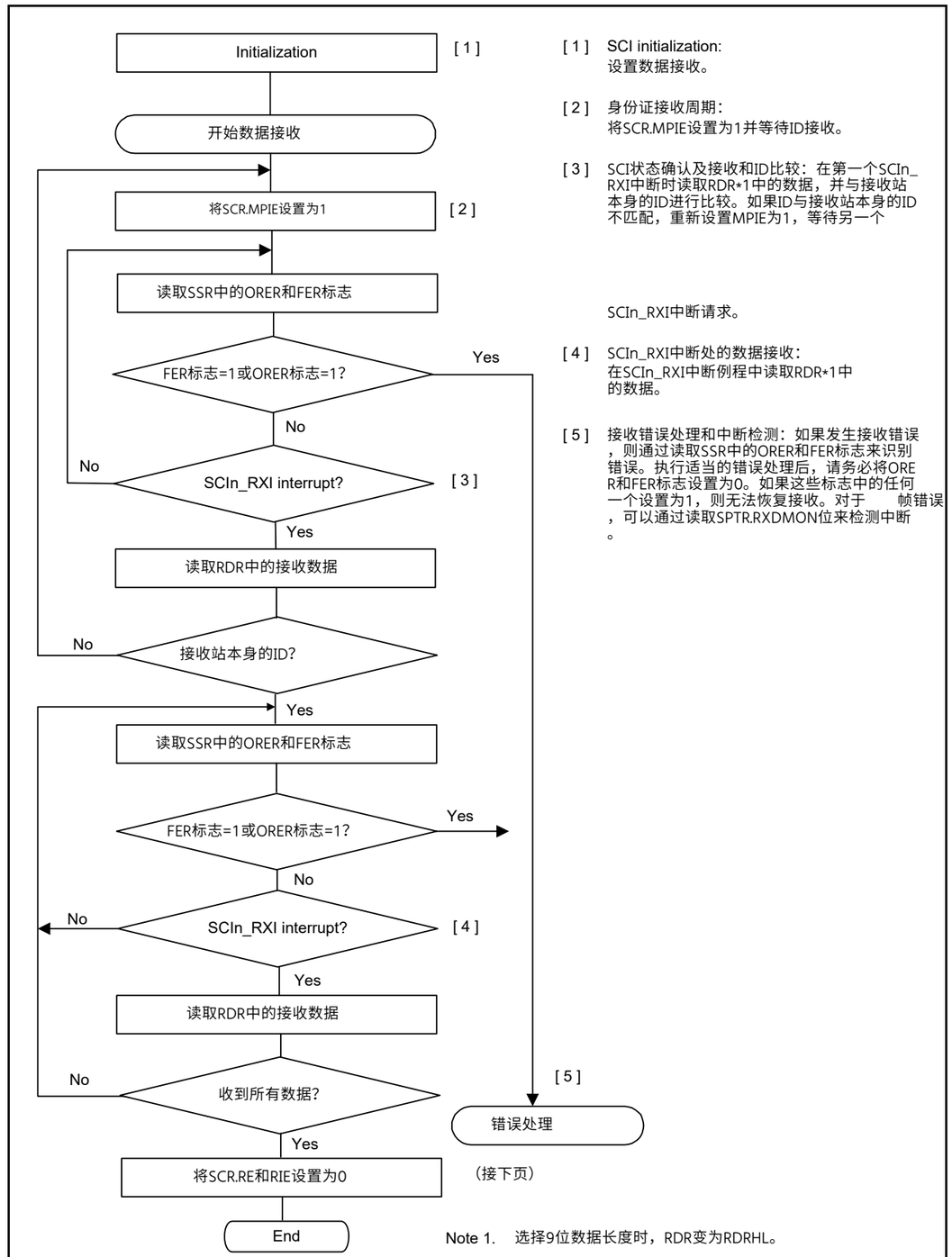
[2] ID reception cycle:
Set SCR.MPIE to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
Read data in RDR*1 on the first SCIn_RXI interrupt and compare it with the ID of the receiving station itself. If the ID does not match the ID of the receiving station itself, set MPIE to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR*1 in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. For a framing error, a break can be detected by reading SPTR.RXDMON bit.

Figure 29.27 Example flow of multi-processor serial reception(1) with non-FIFO selected



[1] SCI initialization:
设置数据接收。

[2] 身份证接收周期：
将SCR.MPIE设置为1并等待ID接收。

[3] SCI状态确认及接收和ID比较：在第一个SCIn_RXI中断时读取RDR*1中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，重新设置MPIE为1，等待另一个

SCIn_RXI中断请求。

[4] SCIn_RXI中断处的数据接收：
在SCIn_RXI中断例程中读取RDR*1中的数据。

[5] 接收错误处理和中断检测：如果发生接收错误，则通过读取SSR中的ORER和FER标志来识别错误。执行适当的错误处理后，请务必将ORER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。对于 帧错误，可以通过读取SPTR.RXDMON位来检测中断。

Figure 29.27 选择非FIFO的多处理器串行接收示例流程(1)

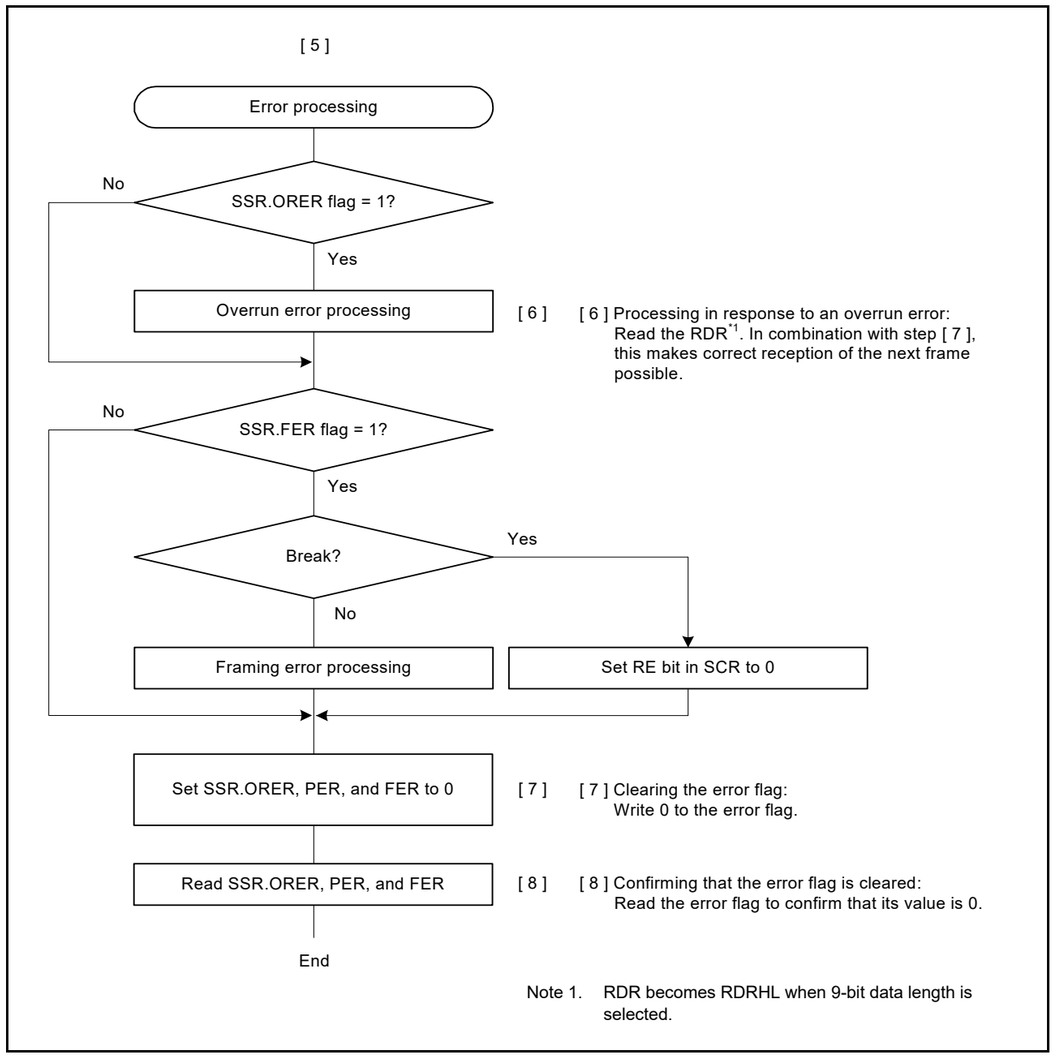


Figure 29.28 Example flow of multi-processor serial reception (2) with non-FIFO selected

(2) FIFO selected

Figure 29.29 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the MPB flag in FRDRH. A value of 0 is written to the PER flag in FRDRH. Data is written to FRDRH and FRDRL with the correct data length. Unused bits are written with 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, the SCI updates FER, MPB and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER, and DR flags in FRDRH always reflect the associated flags in the SSR_FIFO register.

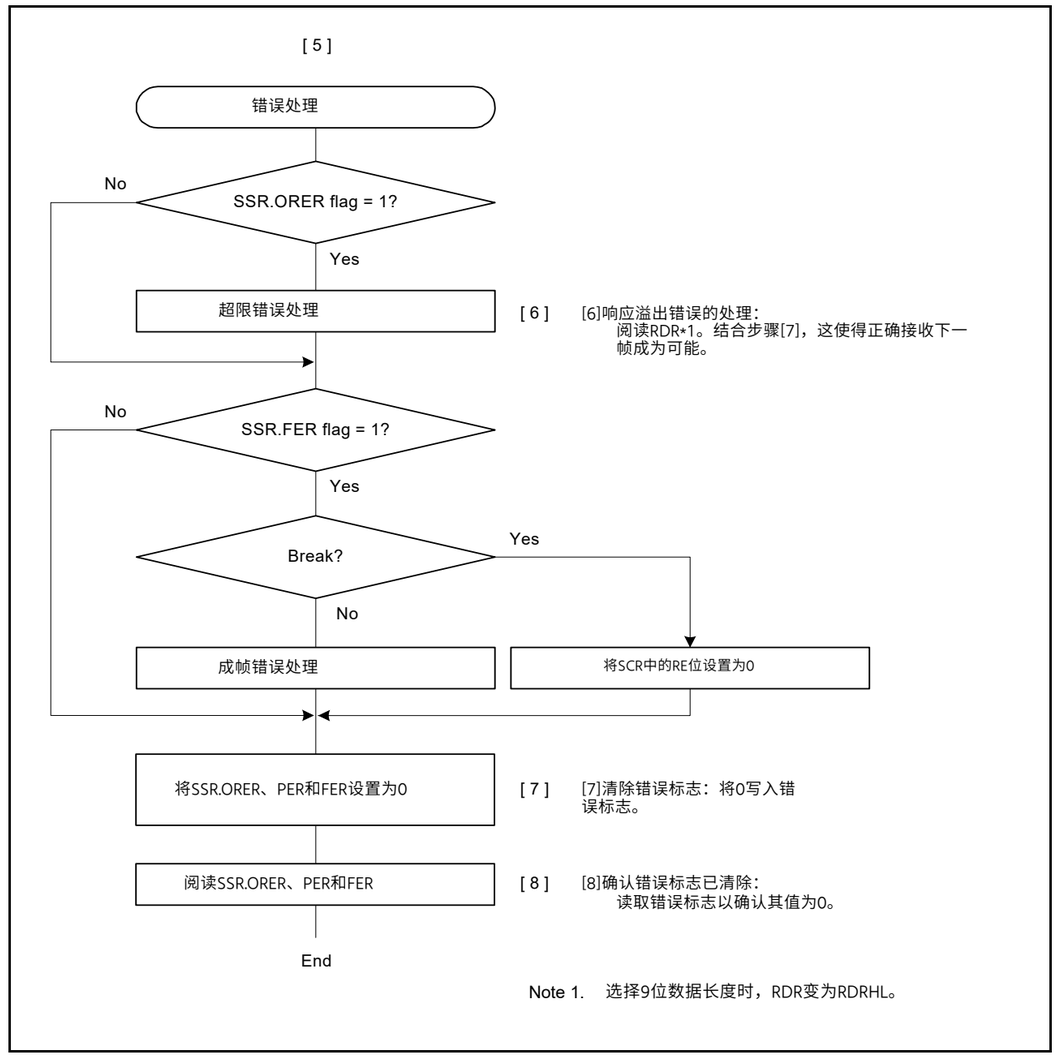


Figure 29.28 选择非FIFO的多处理器串行接收示例流程(2)

(2) FIFO selected

图29.29显示了在多处理器模式下写入FRDRH和FRDRL的数据格式示例。

在多处理器模式下，作为接收数据一部分的MPB值被写入FRDRH中的MPB标志。值0写入FRDRH中的PER标志。数据以正确的数据长度写入FRDRH和FRDRL。未使用的位写入0。按从FRDRH到FRDRL的顺序读取。如果软件读取FRDRL，SCI会用下一个数据更新FER、MPB和FRDRL中的接收数据（RDAT[8:0]）。FRDRH中的RDF、ORER和DR标志始终反映SSR_FIFO寄存器中的相关标志。

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR. CHR1	SMR. CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRH[7] bit is read as an indefinite value.

Figure 29.29 Data format stored to FRDRH and FRDRL in multi-processor mode with FIFO selected

Figure 29.30 shows an example flow of multi-processor data reception with FIFO selected. When the MPIE bit in SCR is set to 1, reading communication data is skipped until the reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB, and the associated errors are transferred to FRDRHL. The MPIE bit in SCR register is automatically cleared and non multi-processor reception continues.

If a frame error occurs and the FER flag in SSR_FIFO is set to 1, the SCI continues data reception. The rest of the operations are the same as in asynchronous mode with FIFO selected.

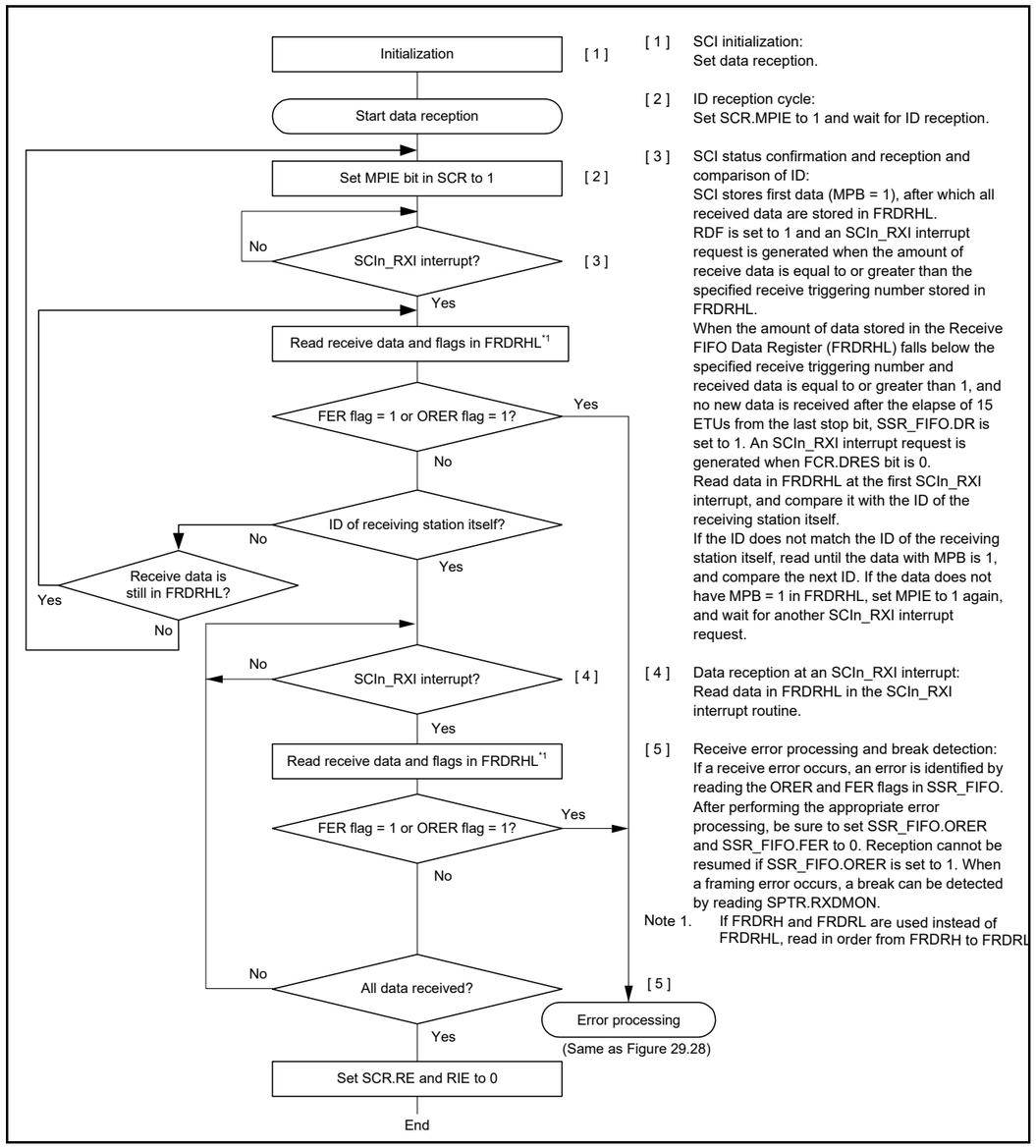
数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR. CHR1	SMR. CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8位接收数据							
9 bits	0	不在乎	—	RDF	ORER	FER	0	DR	MPB	9位接收数据								

Note: 当数据长度为7位时，FRRDH[0]和FRDRL[7]总是读取0
当数据长度为8位时，FRRDH[0]总是读取0
FRDRH[7]位被读取为不定值。

Figure 29.29 在选择FIFO的多处理器模式下存储到FRDRH和FRDRL的数据格式

图29.30显示了选择FIFO的多处理器数据接收示例流程。当SCR的MPIE位设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据、MPB和相关的错误被传输到FRDRHL。SCR寄存器中的MPIE位自动清零，继续非多处理器接收。

如果发生帧错误并且SSR_FIFO中的FER标志设置为1，则SCI继续数据接收。其余操作与选择FIFO的异步模式相同。



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set SCR.MPIE to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
SCI stores first data (MPB = 1), after which all received data are stored in FRDRHL.
RDF is set to 1 and an SCIn_RXI interrupt request is generated when the amount of receive data is equal to or greater than the specified receive triggering number stored in FRDRHL.
When the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number and received data is equal to or greater than 1, and no new data is received after the elapse of 15 ETUs from the last stop bit, SSR_FIFO.DR is set to 1. An SCIn_RXI interrupt request is generated when FCR.DRES bit is 0.
Read data in FRDRHL at the first SCIn_RXI interrupt, and compare it with the ID of the receiving station itself.
If the ID does not match the ID of the receiving station itself, read until the data with MPB is 1, and compare the next ID. If the data does not have MPB = 1 in FRDRHL, set MPIE to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in FRDRHL in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set SSR_FIFO.ORER and SSR_FIFO.FER to 0. Reception cannot be resumed if SSR_FIFO.ORER is set to 1. When a framing error occurs, a break can be detected by reading SPTR.RXDMON.

Note 1. If FRDRH and FRDRL are used instead of FRDRHL, read in order from FRDRH to FRDRL

Figure 29.30 Example flow of serial reception in multi-processor mode with FIFO selected

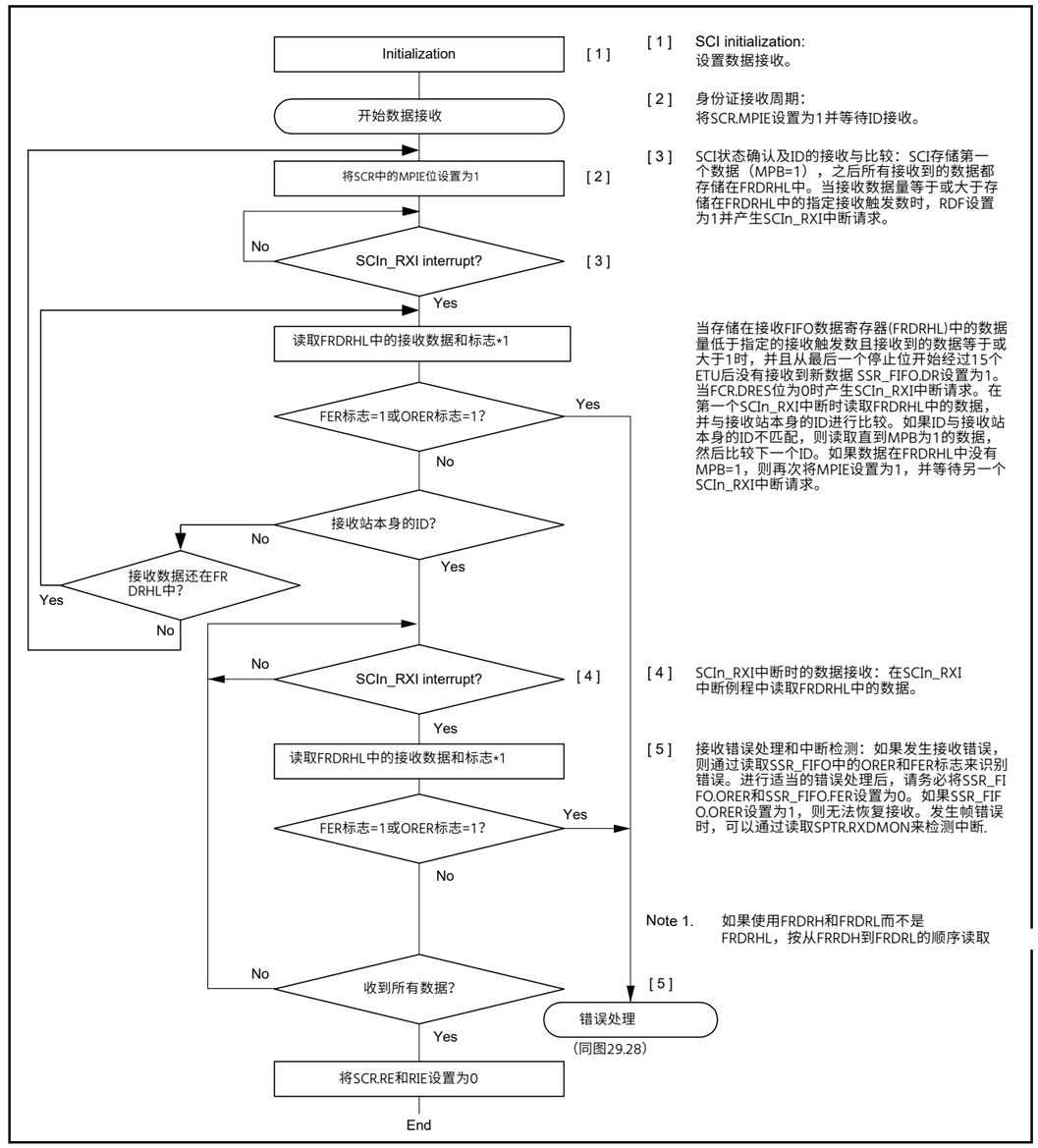
29.5 Operation in Clock Synchronous Mode

Figure 29.31 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock.

After 8-bit data is output, the transmission line holds the last bit as the output state. When the CKPH bit in SPMR register is 1 in slave mode, the SCI holds the first bit output state.



[1] SCI initialization:
设置数据接收。

[2] 身份证接收周期：
将SCR.MPIE设置为1并等待ID接收。

[3] SCI状态确认及ID的接收与比较：SCI存储第一个数据（MPB=1），之后所有接收到的数据都存储在FRDRHL中。当接收数据量等于或大于存储在FRDRHL中的指定接收触发数时，RDF设置为1并产生SCIn_RXI中断请求。

当存储在接收FIFO数据寄存器(FRDRHL)中的数据量低于指定的接收触发数且接收到的数据等于或大于1时，并且从最后一个停止位开始经过15个ETU后没有接收到新数据 SSR_FIFO.DR设置为1。当FCR.DRES位为0时产生SCIn_RXI中断请求。在第一个SCIn_RXI中断时读取FRDRHL中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，则读取直到MPB为1的数据，然后比较下一个ID。如果数据在FRDRHL中没有MPB=1，则再次将MPIE设置为1，并等待另一个SCIn_RXI中断请求。

[4] SCIn_RXI中断时的数据接收：在SCIn_RXI中断例程中读取FRDRHL中的数据。

[5] 接收错误处理和中断检测：如果发生接收错误，则通过读取SSR_FIFO中的ORER和FER标志来识别错误。进行适当的错误处理后，请务必将SSR_FIFO.ORER和SSR_FIFO.FER设置为0。如果SSR_FIFO.ORER设置为1，则无法恢复接收。发生帧错误时，可以通过读取SPTR.RXDMON来检测中断.

Note 1. 如果使用FRDRH和FRDRL而不是FRDRHL，按从FRRDH到FRDRL的顺序读取

Figure 29.30 选择FIFO的多处理器模式下的串行接收示例流程

29.5 时钟同步模式下的操作

图29.31显示了时钟同步串行数据通信的数据格式。

在时钟同步模式下，数据的发送或接收与时钟脉冲同步。传输数据中的一个字符由8位数据组成。在时钟同步模式下，不能添加奇偶校验位。

在数据传输中，SCI从同步时钟的一个下降沿输出数据到下一个下降沿。在数据接收中，SCI与同步时钟的上升沿同步接收数据。

8位数据输出后，传输线保持最后一位作为输出状态。在从机模式下，当SPMR寄存器中的CKPH位为1时，SCI保持第一位输出状态。

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a common clock. Both the transmitter and the receiver have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to perform continuous transfer in the fastest bit rate setting (BRR = 00h and SMR.CKS[1:0] = 00b). Therefore, when the FIFO is selected, this setting (BRR = 00h and SMR.CKS[1:0] = 00b) is not available.

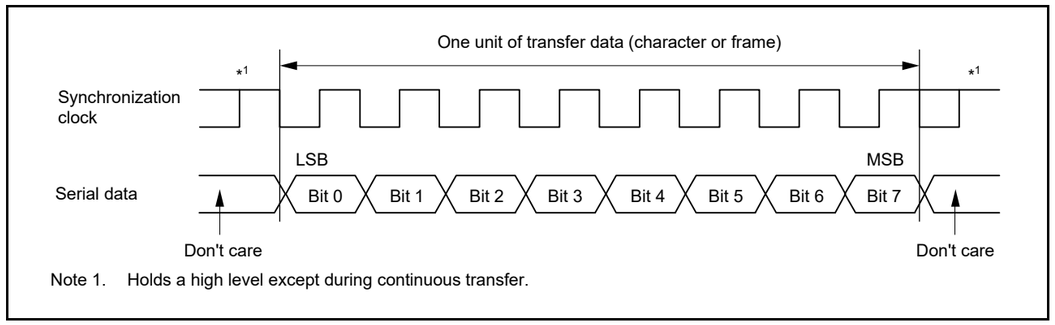


Figure 29.31 Data format in clock synchronous serial communications with LSB-first

29.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected based on the setting of the CKE[1:0] bits in the SCR register.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed, the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts when the RE bit in SCR is set to 1. The synchronization clock stops when it is held high*1 and when an overrun error occurs, or when the RE bit is set to 0.

When only data reception is performed and the CTS function is enabled, the clock output does not start when the RE is set to 1 and the CTSn_RTSn input is high. The synchronization clock output starts when the RE bit is set to 1 and the CTSn_RTSn input is low. When the CTSn_RTSn input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn input continues to be low, the synchronization clock stops when it is held high*1 and when an overrun error occurs, or when the RE bit is set to 0.

Note 1. The signal is held high when SPMR.CKPH bit is 0 and SPMR.CKPOL bit is 0, or when SPMR.CKPH bit is 1 and SPMR.CKPOL bit is 1.
It is held low when SPMR.CKPH bit is 0 and SPMR.CKPOL bit is 1, or when SPMR.CKPH bit is 1 and SPMR.CKPOL bit is 0.

29.5.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn input controls the start of data reception or transmission when the clock source is the internal clock. Setting the CTSE bit in SPMR register to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication becomes possible. Conditions for output of CTSn_RTSn low and high are as follows:

[Conditions for low output]

在SCI中，发送器和接收器是独立的单元，通过使用公共时钟实现全双工通信。发送器和接收器都具有双缓冲结构，因此可以在发送过程中写入下一个发送数据或在接收过程中读取上一个接收数据，从而实现数据的连续传输。

但是，不可能以最快的比特率设置（BRR=00h和SMR.CKS[1:0]=00b）执行连续传输。Therefore whentheFIFOis selected thissetting(BRR=00handSMR.CKS[1:0]=00b)isnotavailable.

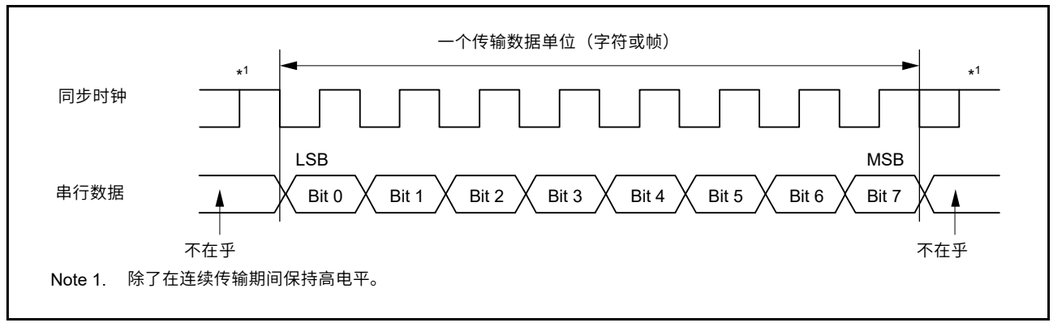


Figure 29.31 LSB优先时钟同步串行通信中的数据格式

29.5.1 Clock

由片内波特率发生器产生的内部时钟或外部同步时钟输入
SCKn引脚可以根据SCR寄存器中CKE[1:0]位的设置来选择。

当SCI在内部时钟上运行时，同步时钟从SCKn引脚输出。在一个字符的传输中输出八个同步时钟脉冲。当不执行传输时，时钟保持高电平。但是，当CTS功能禁用时仅执行数据接收时，当SCR中的RE位设置为1时，同步时钟输出开始。当同步时钟保持为高*1和发生溢出错误时，同步时钟停止，或者当RE位设置为0时。

当仅执行数据接收并启用CTS功能时，当RE设置为1且CTSn_RTSn输入为高电平时，时钟输出不会启动。当RE位设置为1且CTSn_RTSn输入为低电平时，同步时钟输出开始。当帧接收完成时CTSn_RTSn输入为高电平时，同步时钟输出在其变为高电平时停止。如果CTSn_RTSn输入持续为低电平，则同步时钟在保持高电平*1并且发生溢出错误或RE位设置为0时停止。

注1.当SPMR.CKPH位为0且SPMR.CKPOL位为0或SPMR.CKPH位为1且
SPMR.CKPOL位为1。当SPMR.CKPH位为0且SPMR.CKPOL位为1或SPMR.CKPH位为1且

SPMR.CKPOL位为0。

29.5.2 CTS和RTS函数

在CTS功能中，当时钟源为内部时钟时，CTSn_RTSn输入控制数据接收或发送的开始。将SPMR寄存器中的CTSE位设置为1启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚设置为低电平会导致数据接收或发送开始。

在数据发送或接收过程中将CTSn_RTSn引脚设置为高电平不会影响当前帧的发送或接收。

在RTS功能中，当时钟源为外部同步时钟时，CTSn_RTSn输出用于请求开始数据接收或发送。当串行通信成为可能时，CTSn_RTSn输出变为低电平。CTSn_RTSn低电平和高电平的输出条件如下：

[低输出的条件]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the RE or TE bit in SCR is 1
- When serial communication is enabled
- There is no received data available to be read (when SCR.RE is 1)
- Data is available for transmission in TSR (when SCR.TE is 1)
- The SSR.ORER flag is 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the RE or TE bit in the SCR is 1
- When serial communication is enabled
- When the amount of receive data written in FRDRHL is less than the specified CTSn_RTSn output triggering number (when SCR.RE = 1)
- Data that has not been transmitted is available in FTDRHL (when SCR.TE is 1 and SCR.CKE[1] is 0)
- Data is available for transmission in TSR (when SCR.TE is 1 and SCR.CKE[1] is 1)
- The SSR_FIFO.ORER flag is 0.

[Condition for high output]

(a) Non-FIFO selected

- The conditions for low output are not satisfied
- After reception is complete, if it is terminated with SCR.RE = 0 without reading the RDR register, then RTS remains high. Read the SCR register for dummy after writing SCR.RE = 0.

(b) FIFO selected

The conditions for low output are not satisfied.

29.5.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to SCR, then continue through the SCI procedure in 29.5.2 CTS and RTS Functions. Any time the operating mode or transfer format is to be changed, SCR must be initialized before the change can be made.

Note: When the SCR.RE bit is set to 0, the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO, and the RDR and RDRHL registers are not initialized. When the TE bit in the SCR register is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the TIE bit is 1 generates an SCIn_TXI interrupt request.

(a) 满足以下所有条件时选择非FIFO

- SCR中RE或TE位的值为1
- 启用串行通信时
- 没有可读取的接收数据（当SCR.RE为1时）
- 数据可用于在TSR中传输（当SCR.TE为1时）
- SSR.ORER标志为0。

(b) 满足以下所有条件时选择FIFO

- SCR中RE或TE位的值为1
- 启用串行通信时
- 当FRDRHL写入的接收数据量小于指定的CTSn_RTSn输出触发数时（当SCR.RE=1时）
- 未传输的数据在FTDRHL中可用（当SCR.TE为1且SCR.CKE[1]为0时）
- 数据可用于TSR中的传输（当SCR.TE为1且SCR.CKE[1]为1时）
- SSR_FIFO.ORER标志为0。

【高输出条件】

(a) Non-FIFO selected

- 不满足低输出条件
- 接收完成后，如果在没有读取RDR寄存器的情况下以SCR.RE=0终止，则RTS保持高电平。写入SCR.RE=0后，读取SCR寄存器的虚拟寄存器。

(b) FIFO selected

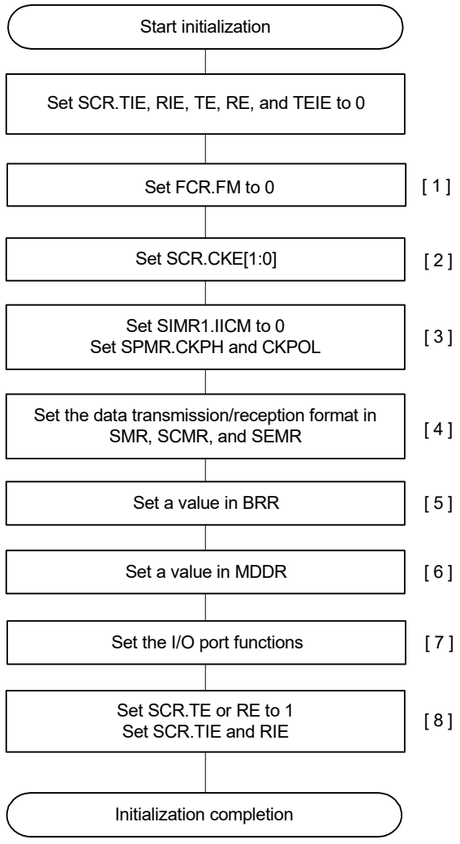
不满足低输出的条件。

29.5.3 时钟同步模式下的SCI初始化

在发送和接收数据之前，首先将初始值00h写入SCR，然后继续执行29.5.2CTS和RTS功能中的SCI程序。每当要更改操作模式或传输格式时，必须先初始化SCR，然后才能进行更改。

Note: 当SCR.RE位设置为0时，SSRSSR_FIFO中的ORER、FER、RDRF、RDF、PER和DR标志以及RDR和RDRHL寄存器不会被初始化。当SCR寄存器中的TE位设置为0时，所选FIFO缓冲区的TEND标志不会被初始化。

Note: 当TIE位为1时，将SCR.TE位的值从1切换为0或从0切换为1会产生SCIn_TXI中断请求。



[1] Set FCR.FM to 0.

[2] Set the clock selection in SCR.

[3] Set SIMR1.IICM to 0.
Set SPMR.CKPH and CKPOL.
Step [3] can be skipped if the values have not changed from the initial values.

[4] Set data transmission/reception format in SMR, SCMR, and SEMR.

[5] Write a value associated with the bit rate to BRR.
This step is not required if an external clock is used.

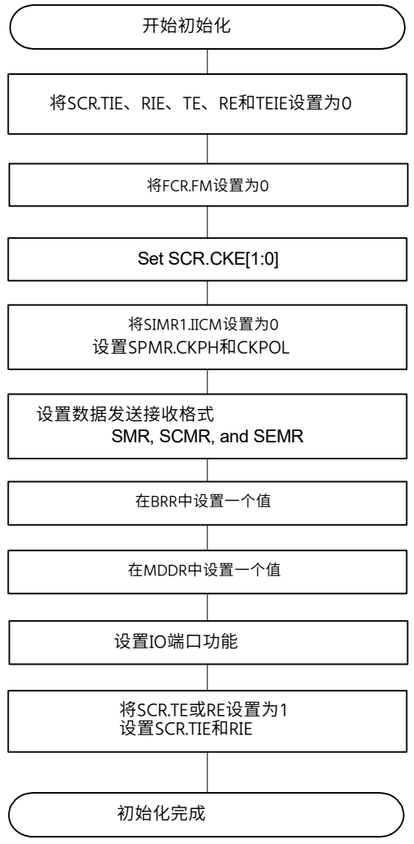
[6] Write the value obtained by correcting a bit rate error in MDDR. This step is not required if SEMR.BRME is set to 0 or an external clock is used.

[7] Specify the I/O port settings to enable input and output functions as required for the TXDn, RXDn, and SCKn pins.

[8] Set SCR.TE or RE to 1. Also set SCR.TIE and RIE.
Setting TE and RE allows TXDn and RXDn to be used.

Note: In simultaneous transmit and receive operations, the SCR.TE and SCR.RE must both be set to 0 or set to 1 simultaneously.

Figure 29.32 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected



[1] 将FCR.FM设置为0。

[2] 在SCR中设置时钟选择。

[3] 将SIMR1.IICM设置为0。
设置SPMR.CKPH和CKPOL。
如果值与初始值没有变化，则可以跳过步骤[3]。

[4] 在SMR、SCMR和
SEMR.

[5] 将与比特率相关的值写入BRR。
如果使用外部时钟，则不需要此步骤。

[6] 将纠正比特率错误后的值写入
MDDR。如果SEMR.BRME设置为0或使用外部时钟，则不需要此步骤。

[7] 指定IO端口设置以启用TXDn、RXDn和SCKn引脚所需的输入和输出功能。

[8] 将SCR.TE或RE设置为1。同时设置SCR.TIE和RIE。
设置TE和RE允许使用TXDn和RXDn。

Note: 在同时发送和接收操作中，
SCR.TE和SCR.RE必须都设置为0或同时设置为1。

Figure 29.32 在时钟同步模式下选择非FIFO的SCI初始化示例流程

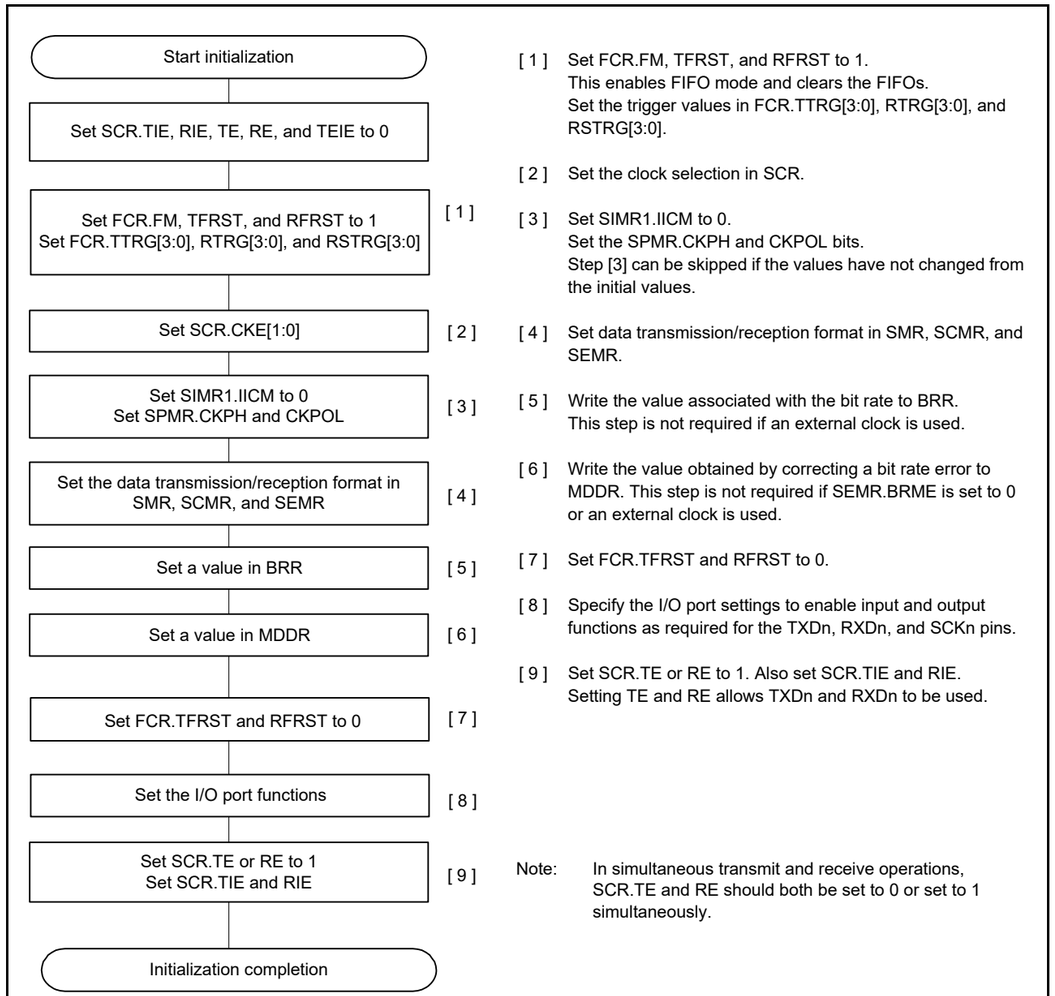


Figure 29.33 Example flow of SCI initialization in clock synchronous mode with FIFO selected

29.5.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 29.34, Figure 29.35, and Figure 29.36 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from TDR to TSR when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit in SCR is set to 1 but only after SCR.TIE is also set to 1, or when SCR.TE and SCR.TIE are both set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the TIE bit in SCR is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the TIE bit in SCR to 0 and the TEIE bit in SCR to 1 after the last of the

Figure 29.33 选择FIFO的时钟同步模式下的SCI初始化示例流程

29.5.4 时钟同步模式下的串行数据传输

(1) Non-FIFO selected

图29.34、图29.35和图29.36显示了时钟同步模式下的串行传输示例。

在串行数据传输中，SCI操作如下：

1. 当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR传输到TSR。当SCR中的TE位设置为1但仅在SCR.TIE也设置为1之后，或者当SCR.TE和SCR.TIE同时设置为1时，会在传输开始时产生SCIn_TXI中断请求单指令。
2. 将数据从TDR传输到TSR后，SCI开始传输。当SCR中的TIE位设置为1时，SCIn_TXI中断请求产生。在当前发送数据发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入TDR来启用连续发送。什么时候
SCIn_TEI中断请求正在使用中，将SCR中的TIE位设置为0，并将SCR中的TEIE位设置为1

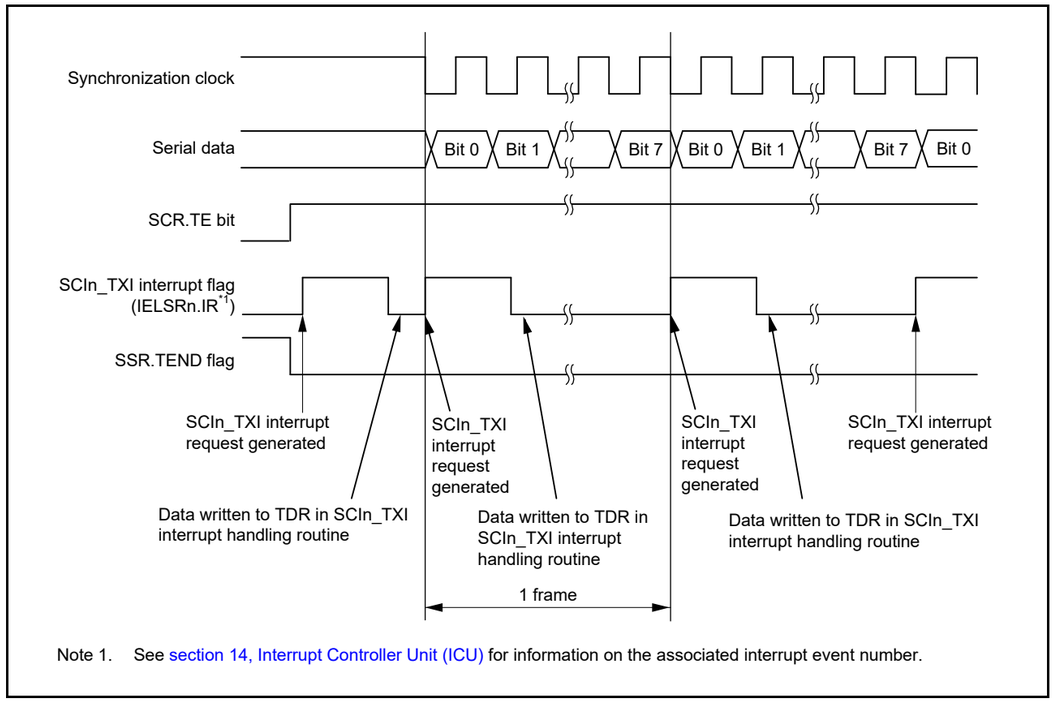
data to be transmitted is written to TDR.

3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified, and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTSn_RTSn signal is low while the CTSE bit in SPMR register is 1.
4. The SCI checks for updates to TDR on output of the last bit.
5. When TDR is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the TEND flag in SSR register is set to 1. The TXDn pin keeps the output state of the last bit. If the TEIE bit in SCR register is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 29.34, Figure 29.35, and Figure 29.36 show example flows of serial data transmission.

Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Be sure to set the receive error flags to 0 before starting transmission.

Note: Setting the RE bit in SCR register to 0 does not clear the receive error flags.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.34 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission

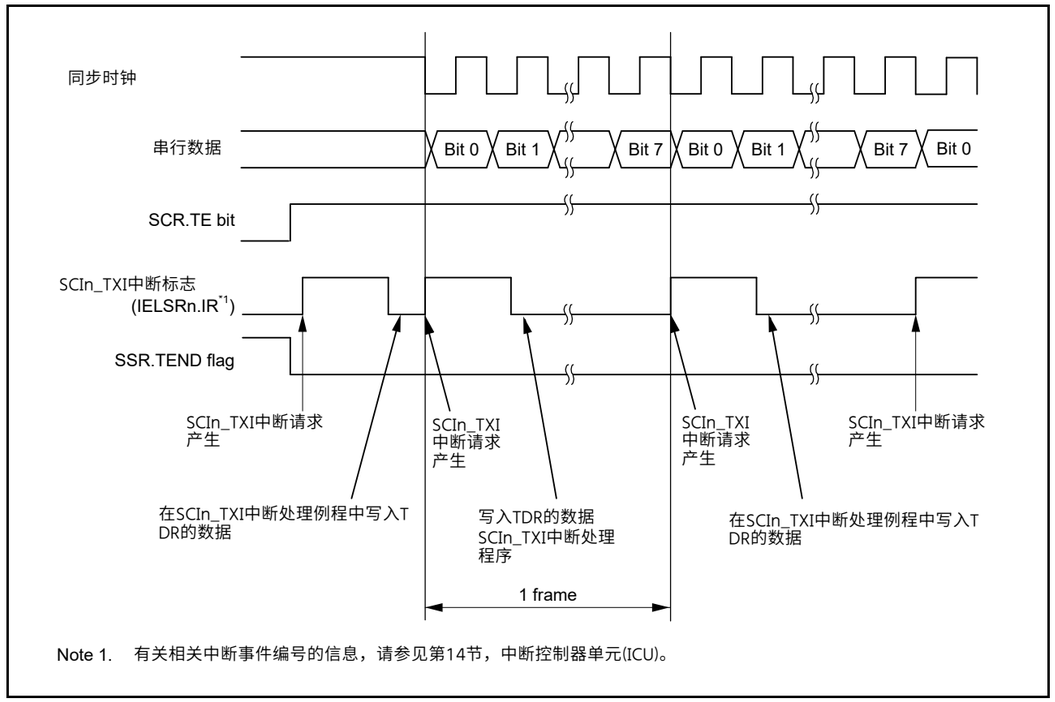
要传输的数据被写入TDR。

3. 8位数据从TXDn引脚发送，当指定时钟输出模式时与输出时钟同步，当指定使用外部时钟时与输入时钟同步。时钟信号的输出暂停，直到输入CTSn_RTSn信号为低电平，同时SPMR寄存器中的CTSE位为1。
4. SCI在最后一位的输出上检查TDR的更新。
5. 当TDR更新时，下一个发送数据从TDR传输到TSR，并开始下一帧的串行传输。
6. 如果TDR未更新，则SSR寄存器中的TEND标志设置为1。TXDn引脚保持最后一位的输出状态。
   如果SCR寄存器中的TEIE位为1，则产生SCIn_TEI中断请求并且SCKn引脚保持高电平。

图29.34、图29.35和图29.36显示了串行数据传输的示例流程。

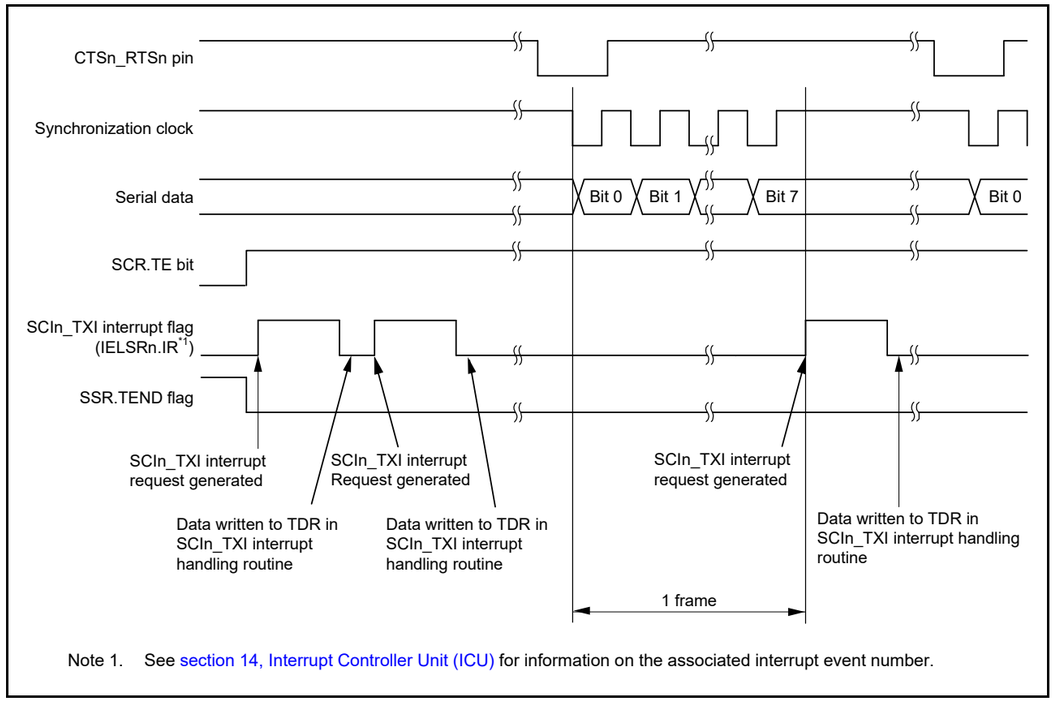
当接收错误标志（SSR中的ORER、FER或PER）设置为1时，发送不会开始。请务必在开始发送之前将接收错误标志设置为0。

Note: 将SCR寄存器中的RE位设置为0不会清除接收错误标志。



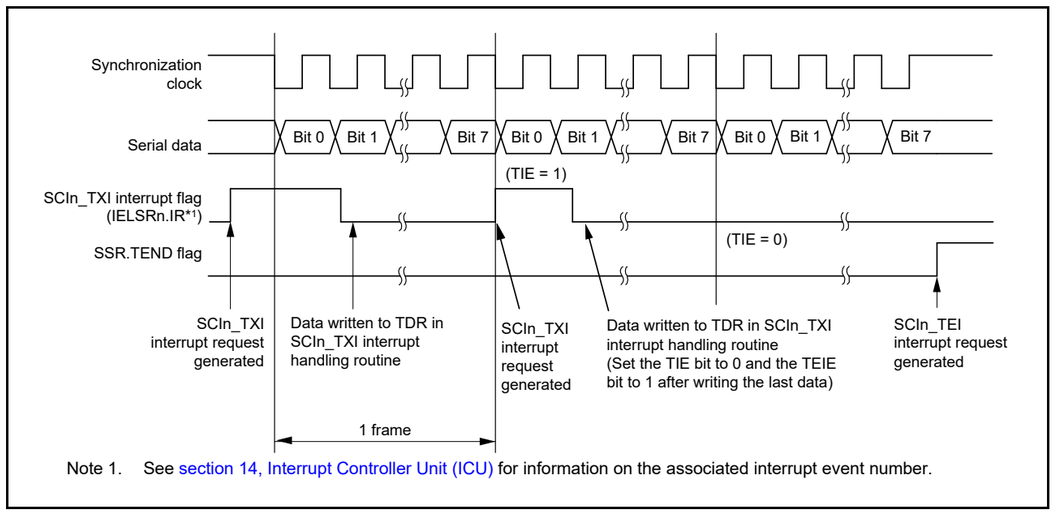
Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.34 传输开始时未使用CTS功能时时钟同步模式下的串行数据传输示例



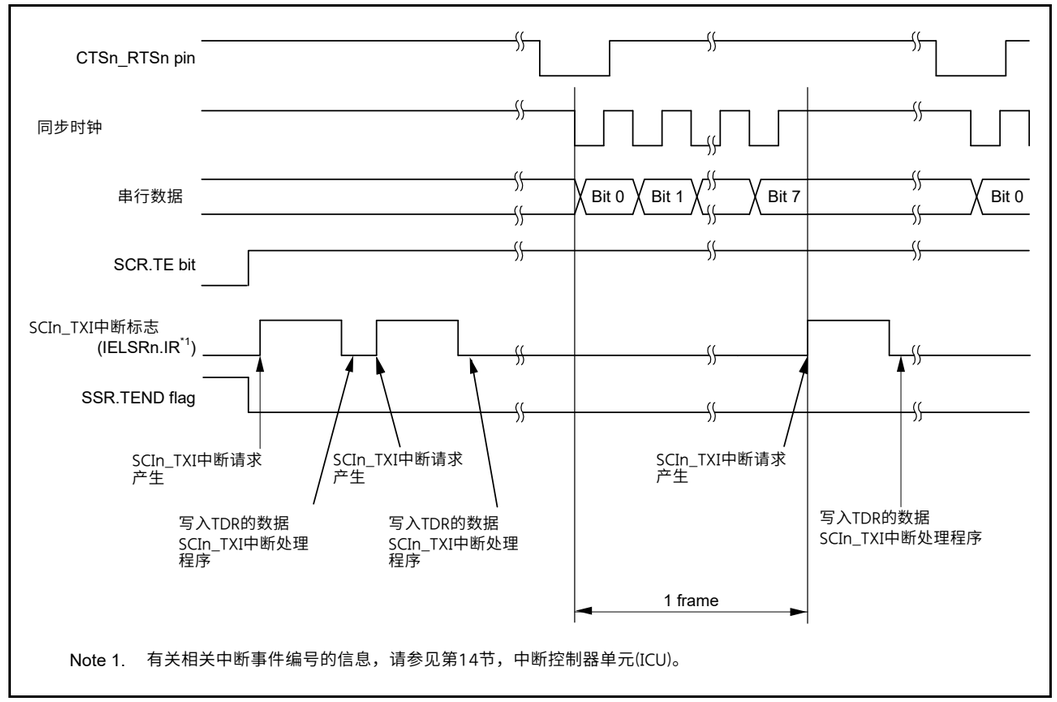
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.35 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



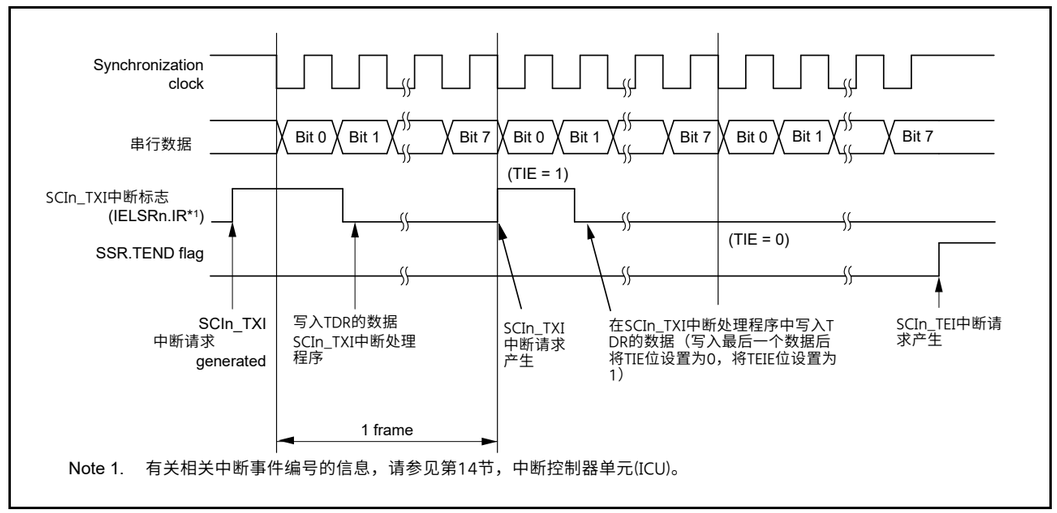
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.36 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



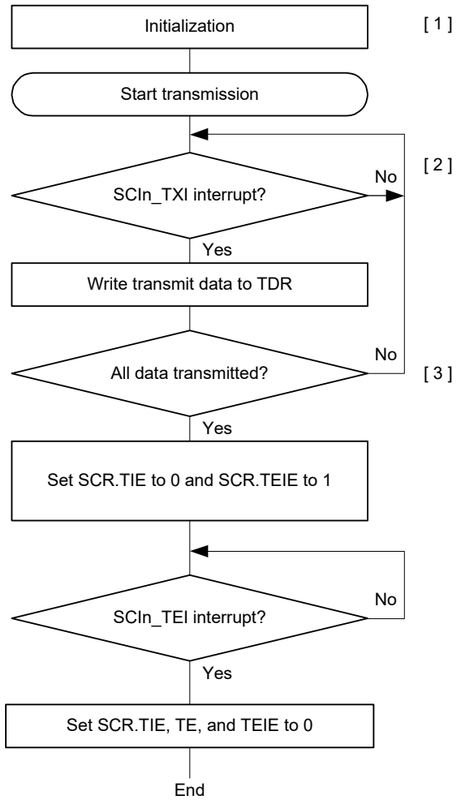
Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.35 传输开始时使用CTS功能时时钟同步模式下的串行数据传输示例



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.36 从传输中间到传输完成的时钟同步模式下的串行数据传输示例



[1] SCI initialization:
Set data transmission.

[2] Writing transmit data to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (SCIn_TXI) request. Transmit data can also be written to TDR by activating the DMAC or DTC by the SCIn_TXI interrupt request.
When SCIn_TEI interrupt requests are in use, set SCR.TIE to 0 and SCR.TEIE to 1 after the last of the data to be transmitted is written to TDR.

Note: When the external clock is in use (the value of SCR.CKE[1:0] is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR.TEND flag to 1. Setting SCR.TE to 0 immediately after this might lead to insufficient hold time for received data on the receiver side.

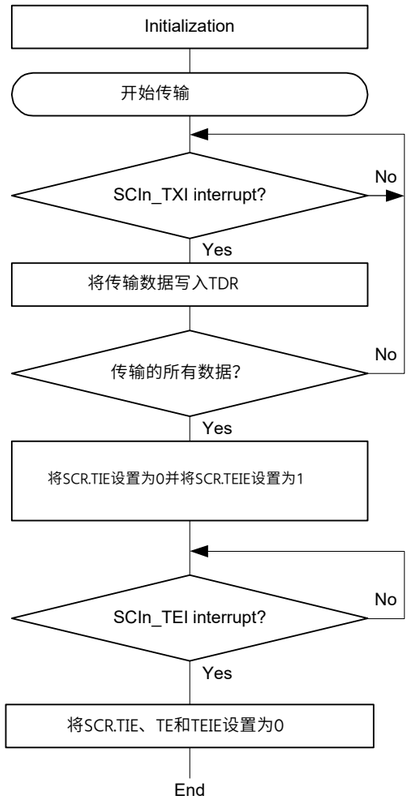
Figure 29.37 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 29.38 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from FTDRL*1 to TSR when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when SCR.TE is set to 1, but only after SCR.TIE is also set to 1, or when SCR.TE and SCR.TIE are both set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the TDFE flag in SSR_FIFO is set to 1. When the TIE bit in SCR is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the TIE bit in SCR to 0 and the TEIE bit in SCR to 1 after the last of the data to be transmitted is written to FTDRL.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified, and in synchronization with the input clock when use of an external clock is specified. Output of the clock



[1] SCI initialization:
设置数据传输。

[2] 通过SCIn_TXI中断请求将发送数据写入TDR：当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。传输数据从SCIn_TXI请求的处理例程中写入一次TDR。

[3] 串行传输继续程序：
要继续串行传输，请将传输数据写入
接受发送数据空中断(SCIn_TXI)请求时的TDR。发送数据也可以通过SCIn_TXI中断请求激活DMAC或DTC写入TDR。当SCIn_TEI中断请求正在使用时，设置

在要传输的最后一个数据写入TDR后，SCR.TIE为0，SCR.TEIE为1。

Note: 当使用外部时钟时（SCR.CKE[1:0]的值为10b或11b），SCK引脚上最后一位的上升沿将SSR.TEND标志设置为1。将SCR.TE设置为紧随其后的0可能会导致接收方接收数据的保持时间不足。

Figure 29.37 选择非FIFO的时钟同步模式下的串行传输示例流程

(2) FIFO selected

图29.38显示了选择FIFO的时钟同步模式下的串行传输示例。

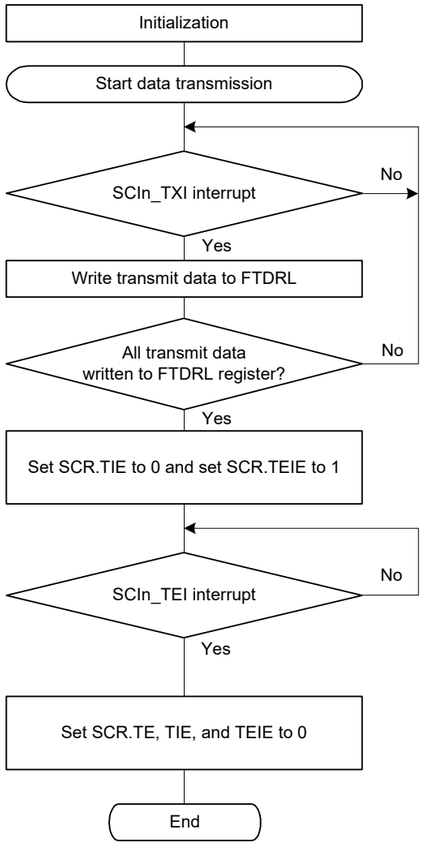
在串行数据传输中，SCI操作如下：

1. 在SCIn_TXI中断处理例程中将数据写入FTDRL*1时，SCI将数据从FTDRL*1传输到TSR。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。发送开始时的SCIn_TXI中断请求在SCR.TE设置为1时产生，但仅在SCR.TIE也设置为1之后，或者当SCR.TE和SCR.TIE同时设置为1时操作说明。
2. 将数据从FTDRL传输到TSR后，SCI开始传输。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO中的TDFE标志设置为1。当SCR中的TIE位设置为1时，产生SCIn_TXI中断请求。在当前传输数据传输完成之前，通过在SCIn_TXI中断处理例程中将下一个传输数据写入FTDRL来启用连续传输。使用SCIn_TEI中断请求时，将要发送的最后一个数据写入FTDRL后，将SCR中的TIE位设置为0，并将SCR中的TEIE位设置为1。
3. 8位数据从TXDn引脚发送，当指定时钟输出模式时与输出时钟同步，当指定使用外部时钟时与输入时钟同步。时钟输出

signal is suspended until the CTSn_RTSn input signal is low and while the CTSE bit in SPMR is 1.

4. The SCI checks whether non-transmitted data remains in FTDRL on the output of the stop bit.
5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, the TEND flag in SSR_FIFO is set to 1. The TXDn pin keeps the output state of the last bit. If the EIE bit in SCR is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In clock synchronous mode, FTDRH is not used.



[1] SCI initialization:
Set data transmission.
After SCR.TE is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRL by an SCIn_TXI interrupt request:
For transmission data from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit FIFO data empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0 before transmission of the current transmit data finishes. Transmit data can also be written to FTDRL by activating the DMAC or DTC. The TDFE flag is cleared automatically in this case. Do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set SCR.TIE to 0 and SCR.TEIE to 1 after the last of the data to be transmitted is written to FTDRL.

Note: When the external clock is in use (the value of SCR.CKE[1:0] is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting SCR.TE to 0 immediately after this might lead to insufficient hold time for receive data on the receiver side.

Figure 29.38 Example flow of serial transmission in clock synchronous mode with FIFO selected

29.5.5 Serial Data Reception in Clock Synchronous Mode

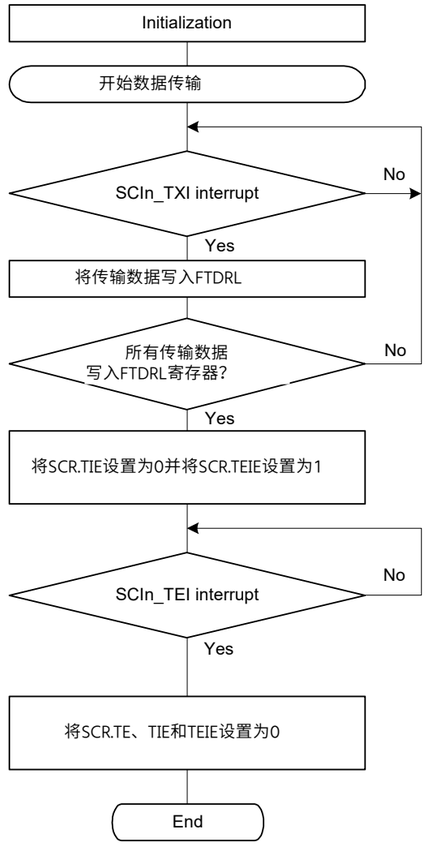
(1) Non-FIFO selected

Figure 29.39 and Figure 29.40 show examples of SCI operation for serial reception in clock synchronous mode.

信号暂停，直到CTSn_RTSn输入信号为低并且SPMR中的CTSE位为1。

4. SCI在停止位的输出上检查未传输的数据是否保留在FTDRL中。
5. 当FTDRL被更新时，下一个传输数据从FTDRL传输到TSR并开始下一帧的串行传输。
6. 如果FTDRL未更新，则SSR_FIFO中的TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR中的EIE位为1，则产生SCIn_TEI中断请求，并且SCKn引脚保持高电平。

注1.在时钟同步模式下，不使用FTDRH。



[1] SCI initialization:
设置数据传输。
SCR.TE置1后，每帧输出1，使能传输。

[2] 通过SCIn_TXI中断请求向FTDRL写入发送数据：对于从FTDRL到TSR的发送数据，当写入FTDRL的发送数据量等于或小于指定发送触发次数时，发送FIFO数据空中断（SCIn_TXI）请求生成。在SCIn_TXI中断处理例程中将发送数据写入FTDRL一次。

[3] 串行传输继续程序：
要继续串行传输，请在SCIn_TXI中断处理例程中将下一个传输数据写入FTDRL，并在当前传输数据传输完成之前将SSR_FIFO.TDFE标志清除为0。也可以通过激活DMAC或DTC将传输数据写入FTDRL。在这种情况下，TDFE标志会自动清除。不要写入TDFE标志。使用SCIn_TEI中断请求时，将要传输的最后一个数据写入FTDRL后，将SCR.TIE设置为0，并将SCR.TEIE设置为1。

Note: 当使用外部时钟时（SCR.CKE[1:0]的值为10b或11b），SCK引脚上最后一位的上升沿将SSR_FIFO.TEND标志设置为1。将SCR.TE设置为在此之后立即为0可能会导致接收方接收数据的保持时间不足。

Figure 29.38 选择FIFO的时钟同步模式下的串行传输示例流程

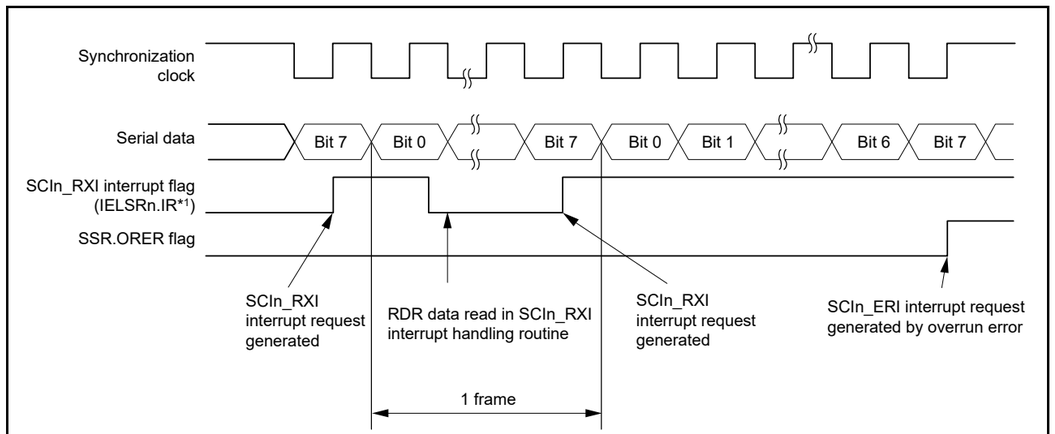
29.5.5 时钟同步模式下的串行数据接收

(1) Non-FIFO selected

图29.39和图29.40显示了时钟同步模式下串行接收的SCI操作示例。

In serial data reception, the SCI operates as follows:

1. When the value of SCR.RE becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in RSR.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If SCR.RIE is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to RDR.
4. When reception completes successfully, receive data is transferred to RDR. If SCR.RIE is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data from RDR causes the CTSn_RTSn pin to output low.

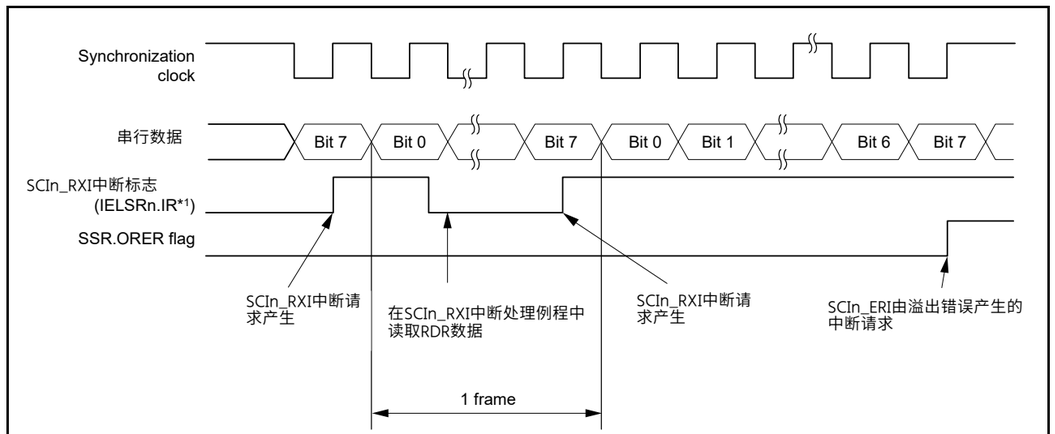


Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.39 Example operation of serial reception in clock synchronous mode (1) when RTS function is not used

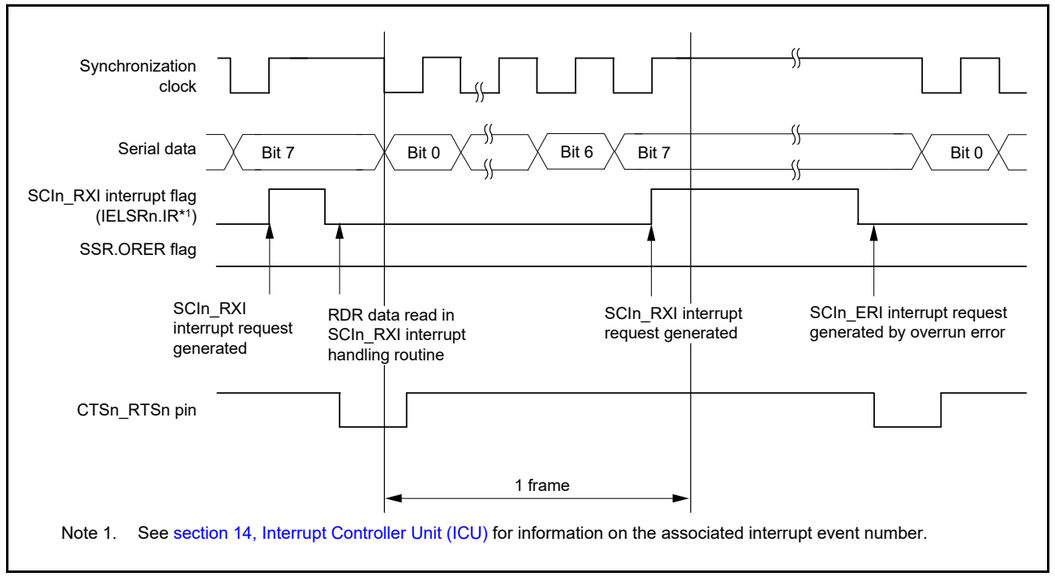
在串行数据接收中，SCI操作如下：

1. 当SCR.RE的值变为1时，CTSn_RTSn引脚变为低电平。
2. SCI执行内部初始化并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR中。
3. 如果发生溢出错误，则SSR.ORER标志设置为1。如果SCR.RIE为1，则生成SCIn_ERI中断请求。接收数据不传输到RDR。
4. 当接收成功完成时，接收数据被传送到RDR。如果SCR.RIE为1，则产生SCIn_RXI中断请求。在接收下一个接收数据完成之前，通过在SCIn_RXI中断处理例程中读取传输到RDR的接收数据来启用连续接收。从RDR读取接收到的数据会导致CTSn_RTSn引脚输出低电平。



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.39 不使用RTS功能时时钟同步模式下串行接收的示例操作(1)

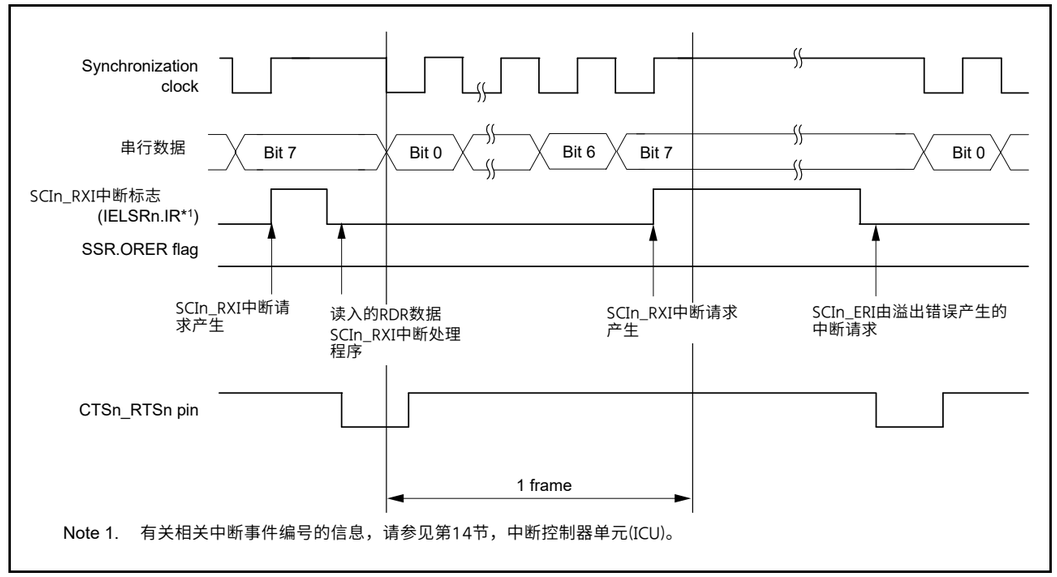


Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

Figure 29.40 Example operation of serial reception in clock synchronous mode (2) when RTS function is used

Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER flags in SSR to 0 before resuming data reception. Additionally, be sure to read the RDR during overrun error processing. When a data reception is forcibly terminated by setting the RE bit in SCR to 0 during operation, read the RDR because the received data that is not read yet might be left in the RDR.

Figure 29.41 shows an example flow of serial data reception.

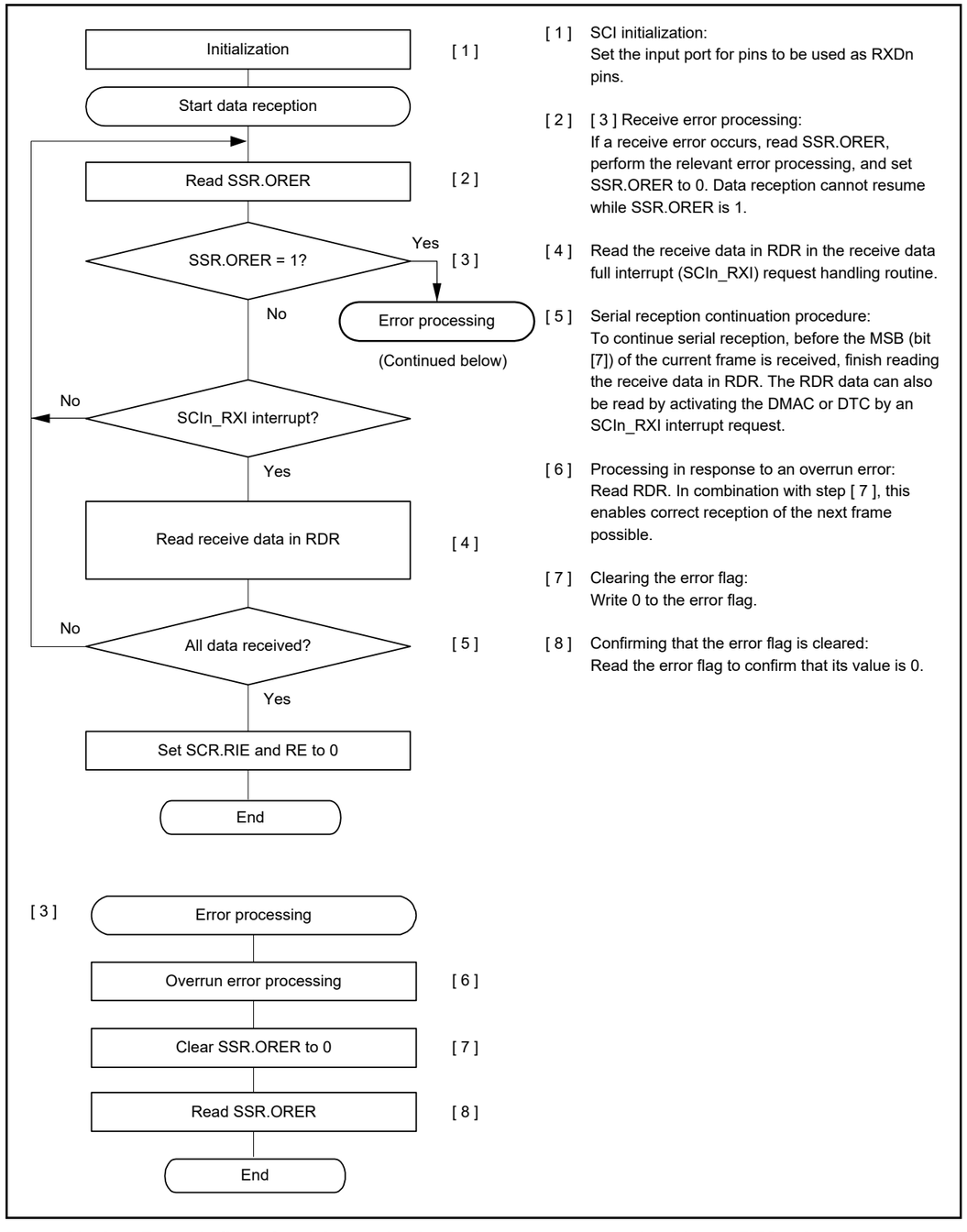


Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.40 使用RTS功能时时钟同步模式下串行接收的示例操作(2)

接收错误标志为1时无法恢复数据传输。因此，在恢复数据接收之前，将SSR中的ORER、FER和PER标志清除为0。此外，请务必在溢出错误处理期间读取RDR。如果在操作期间通过将SCR中的RE位设置为0来强制终止数据接收，请读取RDR，因为尚未读取的接收数据可能会留在RDR中。

图29.41显示了串行数据接收的示例流程。



[1] SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read SSR.ORER, perform the relevant error processing, and set SSR.ORER to 0. Data reception cannot resume while SSR.ORER is 1.

[4] Read the receive data in RDR in the receive data full interrupt (SCIn_RXI) request handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit [7]) of the current frame is received, finish reading the receive data in RDR. The RDR data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request.

[6] Processing in response to an overrun error:
Read RDR. In combination with step [7], this enables correct reception of the next frame possible.

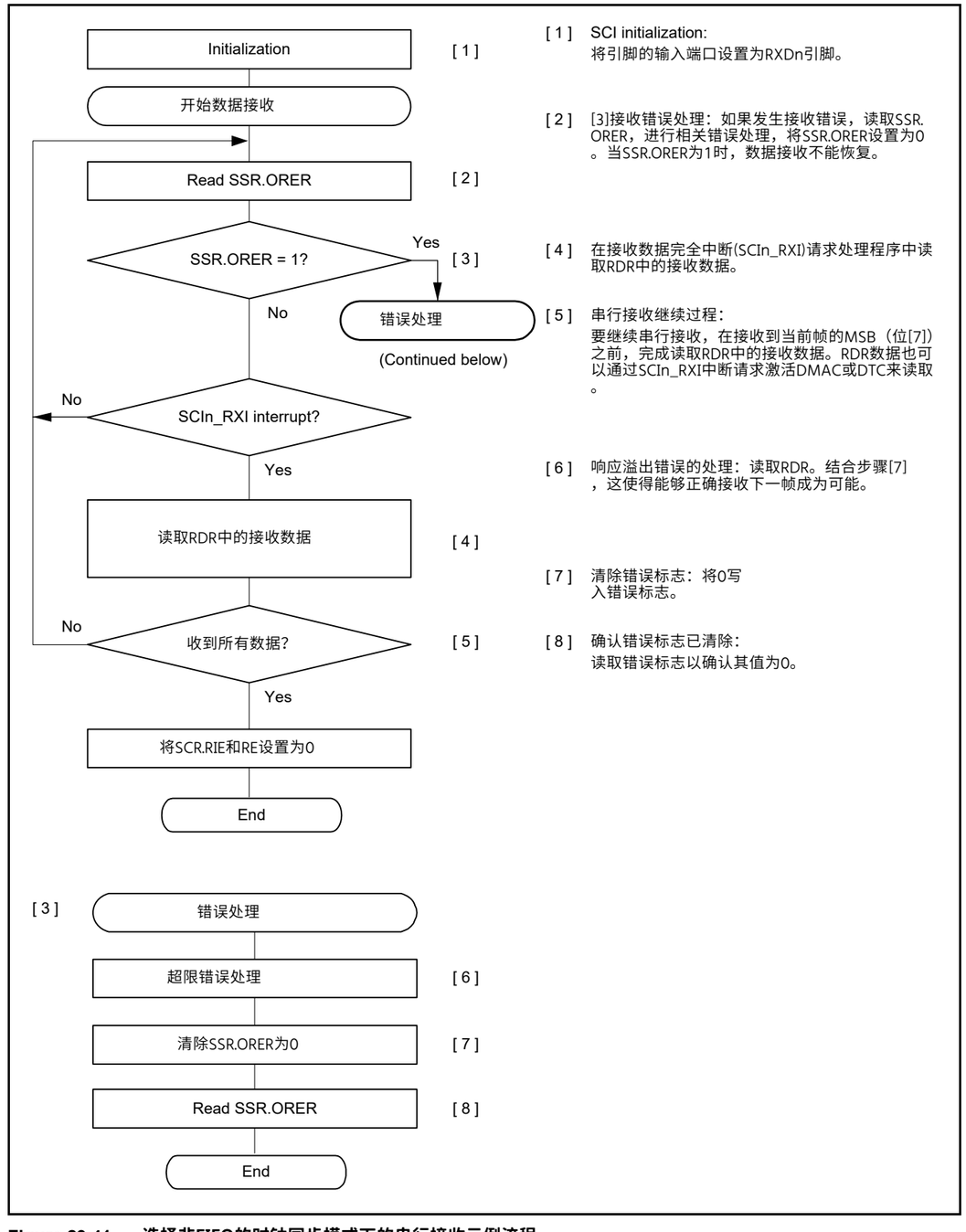
[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 29.41 Example flow of serial reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 29.42 shows an example of serial reception in clock synchronous mode with FIFO selected.



[1] SCI initialization:
将引脚的输入端口设置为RXDn引脚。

[2] [3]接收错误处理：如果发生接收错误，读取SSR.ORER，进行相关错误处理，将SSR.ORER设置为0。当SSR.ORER为1时，数据接收不能恢复。

[4] 在接收数据完全中断(SCIn_RXI)请求处理程序中读取RDR中的接收数据。

[5] 串行接收继续过程：
要继续串行接收，在接收到当前帧的MSB（位[7]）之前，完成读取RDR中的接收数据。RDR数据也可以通过SCIn_RXI中断请求激活DMAC或DTC来读取。

[6] 响应溢出错误的处理：读取RDR。结合步骤[7]，这使得能够正确接收下一帧成为可能。

[7] 清除错误标志：将0写入错误标志。

[8] 确认错误标志已清除：
读取错误标志以确认其值为0。

Figure 29.41 选择非FIFO的时钟同步模式下的串行接收示例流程

(2) FIFO selected

图29.42显示了选择FIFO的时钟同步模式下的串行接收示例。

In serial data reception, the SCI operates as follows:

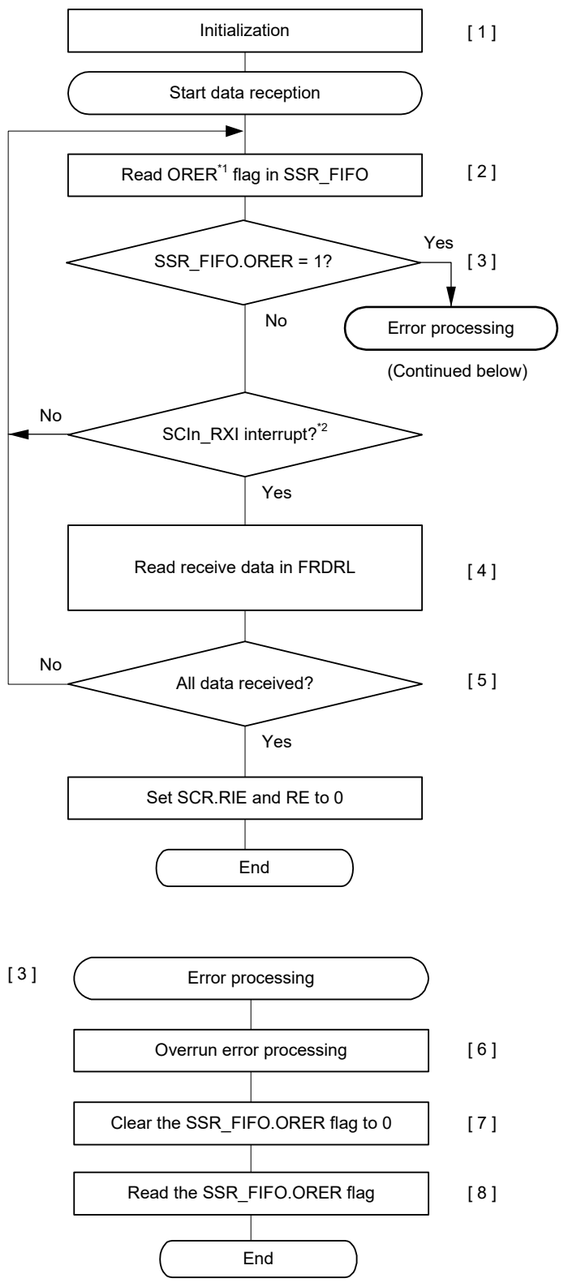
1. When the value of SCR.RE becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in RSR.
3. If an overrun error occurs, the ORER flag in SSR_FIFO is set to 1. If the RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to FRDRL*1.
4. When data reception completes successfully, the receive data is transferred to FRDRL*1. The RDF in SSR_FIFO is set to 1 when the amount of the receive data is equal to or greater than the specified receive triggering number stored in FRDRHL. If the RIE bit in SCR register is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the RTS trigger number, the CTSn_RTSn pin goes low.

Note 1. In clock synchronous mode, FRDRH is not used.
Note 2. Read data in order from FRDRH to FRDRL when RDF and ORER are read with receive data.

在串行数据接收中，SCI操作如下：

1. 当SCR.RE的值变为1时，CTSn_RTSn引脚变为低电平。
2. SCI执行内部初始化并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR中。
3. 如果发生溢出错误，则SSR_FIFO中的ORER标志设置为1。如果SCR中的RIE位为1，则产生SCIn_ERI中断请求。接收数据不传输到FRDRL*1。
4. 当数据接收成功完成时，接收数据被传输到FRDRL*1。当接收数据量等于或大于存储在FRDRHL中的指定接收触发数时，SSR_FIFO中的RDF设置为1。如果SCR寄存器的RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理例程中读取传输到FRDRL*2的接收数据来启用连续数据接收。如果传输到FRDRL的接收数据量小于RTS触发数，则CTSn_RTSn引脚变为低电平。

注1.在时钟同步模式下，不使用FRDRH。
注2.RDF和ORER与接收数据一起读取时，按FRDRH到FRDRL的顺序读取数据。



[1] SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the SSR_FIFO.ORER flag, perform the relevant error processing, then set SSR_FIFO.ORER to 0. Data reception cannot be resumed while SSR_FIFO.ORER is 1.

[4] The receive data stored in FRDRL is read until the amount of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial reception continuation procedure:
To continue serial reception before overrun error occurs, finish reading the receive data in FRDRL and clear SSR_FIFO.RDF to 0. The FRDRL data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.

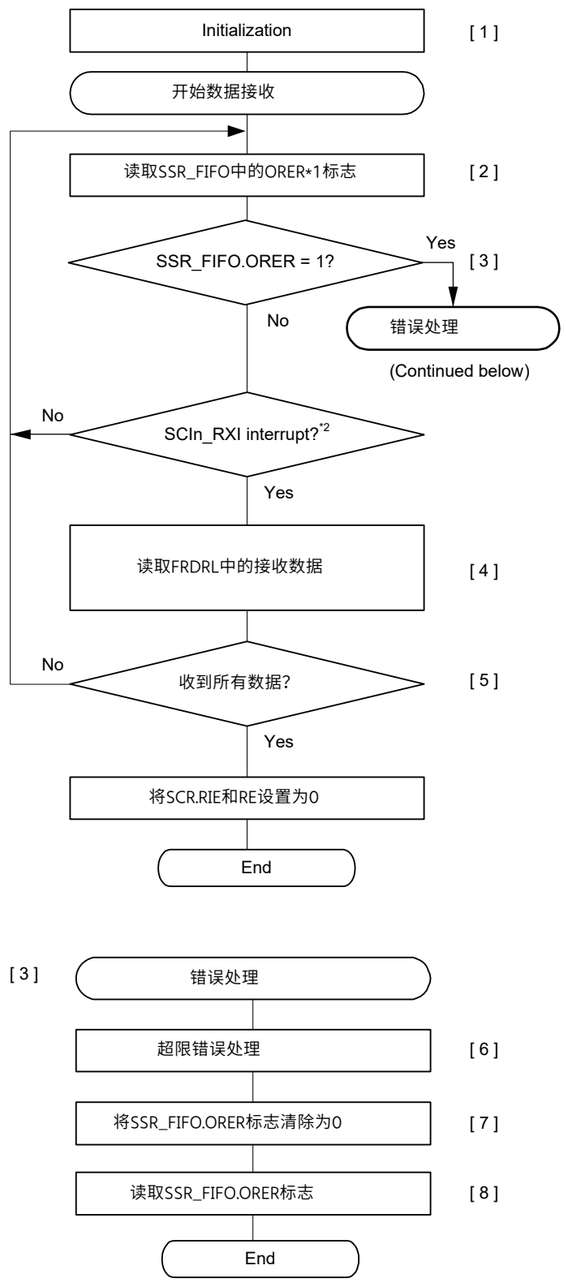
[6] Processing in response to an overrun error:
Read FRDRL. In combination with step [7], this enables correct reception of the next frame possible.

[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. ORER can also be read from FRDRH.ORER. However, to clear the ORER flag, write 0 to SSR_FIFO.ORER.
Note 2. All receive data is an integer multiple of the FIFO triggering number.

Figure 29.42 Example flow of serial reception in clock synchronous mode with FIFO selected



[1] SCI initialization:
将引脚的输入端口设置为RXDn引脚。

[2] [3]接收错误处理：如果发生接收错误，读取
SSR_FIFO.ORER标志位，进行相关错误处理，然后设置SSR_FIFO.ORER为0。当SSR_FIFO.ORER为1时，不能恢复数据接收。

[4] 读取存储在FRDRL中的接收数据，直到存储的数据量小于FCR.RTRG值。软件可以检查FDR.R[4:0]中的可读数据。

[5] 串行接收继续过程：
要在溢出错误发生之前继续串行接收，请完成读取FRDRL中的接收数据并将SSR_FIFO.RDF清除为0。也可以通过SCIn_RXI中断请求激活DMAC或DTC来读取FRDRL数据。在这种情况下，RDF标志会自动清除。不要写入RDF标志。

[6] 响应溢出错误的处理：读取FRDRL。结合步骤[7]，这使得能够正确接收下一帧成为可能。

[7] 清除错误标志：将0写入错误标志。

[8] 确认错误标志已清除：
读取错误标志以确认其值为0。

Note 1. ORER也可以从FRDRH.ORER中读取。但是，要清除ORER标志，请将0写入SSR_FIFO.ORER.
Note 2. 所有接收数据是整数倍FIFO触发数。

Figure 29.42 选择FIFO的时钟同步模式下的串行接收示例流程

29.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 29.43 shows an example flow for simultaneous serial transmission and reception operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmission and reception operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the TEND flag in the SSR register is set to 1.
2. Initialize the SCR register and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously using a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the RIE and RE bits to 0 in the SCR register, then check that the receive error flag ORER in SSR is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously using a single instruction.

29.5.6 时钟同步的同时串行数据发送和接收 Mode

(1) Non-FIFO selected

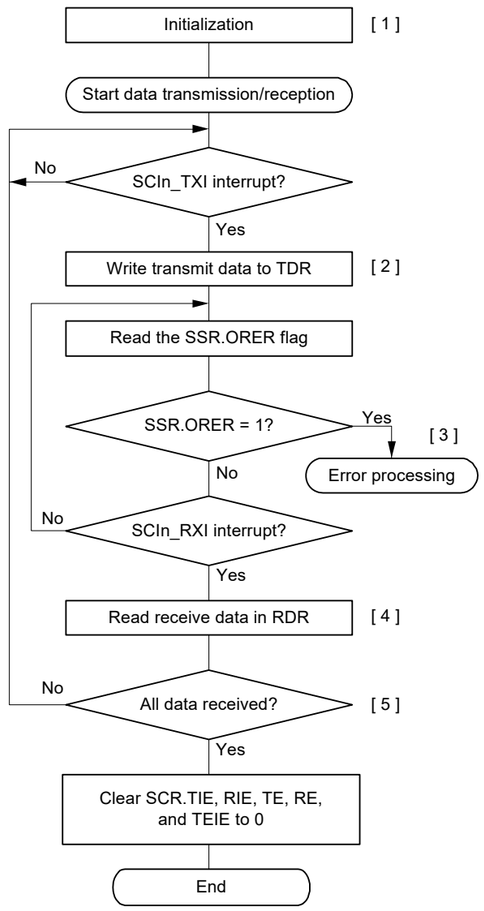
图29.43显示了在时钟同步模式下同时进行串行发送和接收操作的示例流程。初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

1. 通过验证SSR寄存器中的TEND标志是否设置为1来检查SCI是否完成了数据传输。
2. 初始化SCR寄存器，然后使用一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1. 检查SCI是否完成数据接收。
2. 将SCR寄存器中的RIE和RE位设置为0，然后检查SSR中的接收错误标志ORER是否为0。
3. 使用一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR in the SCIn_TXI interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, read the SSR.ORER flag, perform the relevant error processing, then set SSR.ORER to 0. Data reception cannot resume while SSR.ORER is 1.

[4] Reading receive data:
Read the receive data in RDR in the SCIn_RXI interrupt request handling routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB (bit [7]) of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB (bit [7]) of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data can also be written to TDR by activating the DMAC or DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DMAC or DTC by a receive data full interrupt (SCIn_RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 29.43 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 29.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

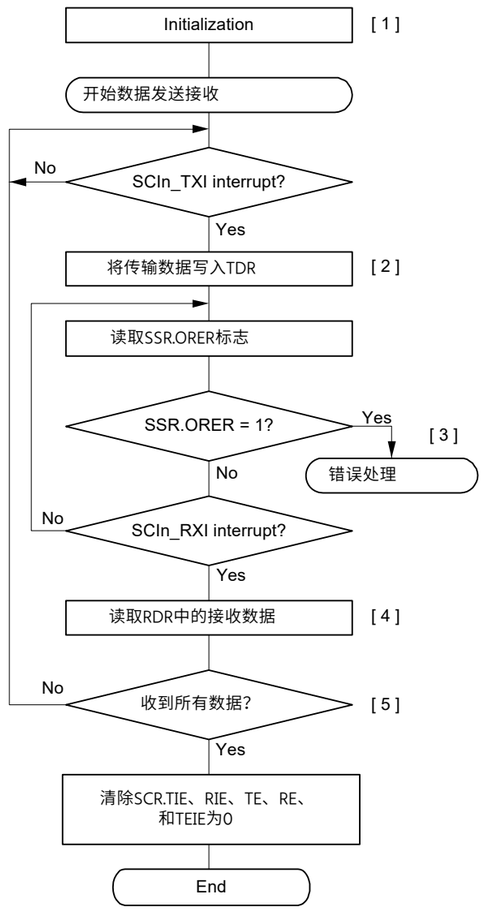
After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the TEND flag in SSR_FIFO is set to 1.
2. Initialize SCR, then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously using a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.
2. Set the RIE and RE bits in SCR to 0 and then check that the receive error flag ORER in SSR_FIFO is 0.



[1] SCI initialization:
TXDn引脚可以作为发送数据的输出引脚，RXDn引脚可以同时作为接收数据的输入引脚。

[2] 发送数据写入：
在SCIn_TXI中断请求处理例程中将发送数据写入TDR。

[3] 接收错误处理：
如果发生接收错误，读取SSR.ORER标志，进行相关错误处理，然后将SSR.ORER设置为0。当SSR.ORER为1时，数据接收不能恢复。

[4] 读取接收数据：
在SCIn_RXI中断请求处理程序中读取RDR中的接收数据。

[5] 串口发送接收继续流程：要继续串口发送和接收，在接收到当前帧的MSB（bit[7]）之前，通过SCIn_RXI中断读完RDR中的接收数据。此外，在发送当前帧的MSB（位[7]）之前，通过SCIn_TXI中断将数据写入TDR。

发送数据也可以通过发送数据空中断(SCIn_TXI)请求激活DMAC或DTC写入TDR。同样，也可以通过接收数据完全中断(SCIn_RXI)请求激活DMAC或DTC来读取RDR数据。

Note: 从发送或接收操作切换到同时发送和接收操作时，首先设置TIE，SCR中的RIE、TE、RE和TEIE位为0，然后将TIE、RIE、TE和RE位同时设置为1。

Figure 29.43 选择非FIFO的时钟同步模式下同时串行发送和接收的示例流程

(2) FIFO selected

图29.44显示了在时钟同步模式下同时串行发送和接收操作的示例流程，并选择了FIFO。

初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

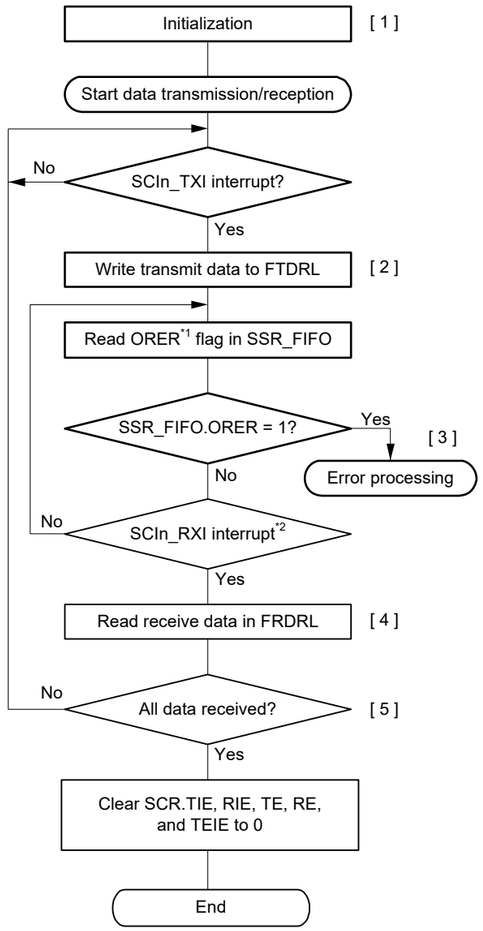
从发送模式切换到同时发送和接收模式：

1. 通过验证SSR_FIFO中的TEND标志是否设置为1来检查SCI是否完成了传输。
2. 初始化SCR，然后使用一条指令同时将SCR中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1. 检查SCI是否完成接收。
2. 将SCR中的RIE和RE位设置为0，然后检查SSR_FIFO中的接收错误标志ORER是否为0。

3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously using a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI interrupt request handling routine. The number of transmission data that can be written is 16 bits, which is the number of stored transmit data in the FIFO.

[3] Receive error processing:
If a receive error occurs, read the SSR_FIFO.ORER flag, perform the relevant error processing, then set SSR_FIFO.ORER to 0. Data reception cannot be resumed while SSR_FIFO.ORER is 1.

[4] Reading receive data:
The received data stored in FRDRL register is read until the amount of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial transmission/reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data is finished, write the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DMAC or DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DMAC or DTC by a receive FIFO data full interrupt (SCIn_RXI) request. The RDF and TDFE flags are cleared automatically in this case.
Do not write to the RDF and TDFE flags.

Note 1. ORER can also read from FRDRH.ORER. To clear the ORER flag, write 0 to SSR_FIFO.ORER.
Note 2. All receive data must be an integer multiple of the FIFO triggering number.

Figure 29.44 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

29.6 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

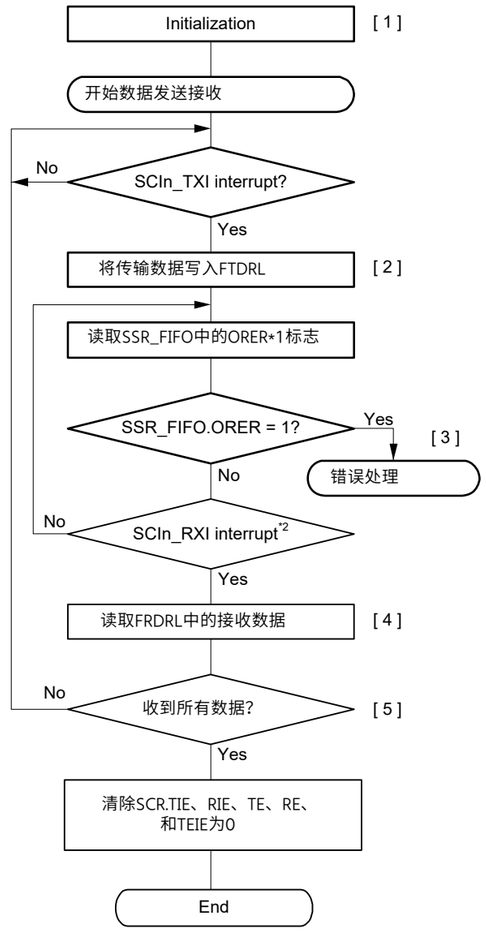
Smart card interface mode can be selected using the appropriate register.

29.6.1 Example Connection

Figure 29.45 shows an example connection between a smart card (IC card) and the MCU.

As shown in Figure 29.45, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

3. 使用一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。



[1] SCI initialization:
TXDn引脚可以作为发送数据的输出引脚，RXDn引脚可以同时作为接收数据的输入引脚。

[2] 发送数据写入：
在SCIn_TXI中断请求处理例程中将发送数据写入FTDRL。可写入的发送数据个数为16位，即FIFO中存储的发送数据个数。

[3] 接收错误处理：
如果发生接收错误，读取SSR_FIFO.ORER标志位，进行相应的错误处理，然后将SSR_FIFO.ORER设置为0。当SSR_FIFO.ORER为1时，不能恢复数据接收。

[4] 读取接收数据：
读取存储在FRDRL寄存器中的接收数据，直到存储的数据量小于FCR.RTRG值。软件可以检查FDR.R[4:0]中的可读数据。

[5] 串口发送接收继续流程：继续串口接收，在溢出错误发生前，完成FRRDL中接收数据的读取并将SSR_FIFO.RDF标志清0。要继续串口发送，在当前发送数据发送完成之前，写入接下来在SCIn_TXI中断处理例程中将数据发送到FTDRL，并将SSR_FIFO.TDFE标志清除为0。发送数据也可以通过发送FIFO数据空中断(SCIn_TXI)请求激活DMAC或DTC写入FTDRL。同样，也可以通过接收FIFO数据满中断(SCIn_RXI)请求激活DMAC或DTC来读取FRDRL数据。在这种情况下，RDF和TDFE标志会自动清除。不要写入RDF和TDFE标志。

Note 1. ORER也可以从FRDRH.ORER中读取。要清除ORER标志，请将0写入SSR_FIFO.ORER。
Note 2. 所有接收数据必须是整数倍FIFO触发数。

Figure 29.44 时钟同步模式下同时串行发送和接收的示例流程 FIFO selected

29.6 智能卡接口模式下的操作

SCI支持符合ISOIEC7816-3（识别卡标准）的智能卡（IC卡）接口，作为SCI的扩展功能。

可以使用适当的寄存器选择智能卡接口模式。

29.6.1 示例连接

图29.45显示了智能卡（IC卡）和MCU之间的示例连接。

如图29.45所示，由于MCU使用单条传输线与IC卡通信，因此将TXDn和RXDn引脚互连，并使用电阻将数据传输线上拉到VCC。

Setting the TE and RE bits in SCR_SMCI to 1 with an IC card disconnected enables closed-loop transmission or reception allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

The output port of the MCU can be used to output a reset signal.

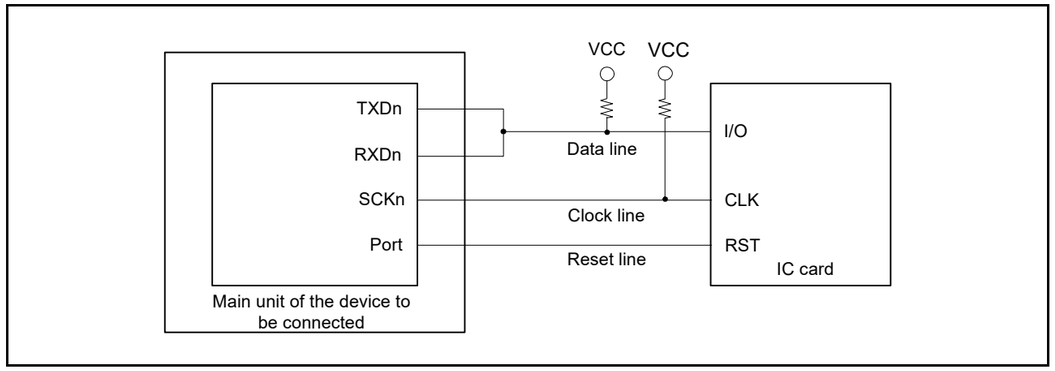


Figure 29.45 Example connection with a smart card (IC card)

29.6.2 Data Format (Except in Block Transfer Mode)

Figure 29.46 shows the data transfer formats in smart card interface mode.

The data transfer format is as follows:

- One frame consists of 8-bit data and a parity bit in asynchronous mode
- During transmission, a guard time of at least 2 ETUs (elementary time unit – the time required to transfer 1 bit) is set from the end of the parity bit until the start of the next frame
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

在断开IC卡的情况下将SCR_SMCI中的TE和RE位设置为1可启用闭环发送或接收，从而实现自诊断。要将SCI产生的时钟脉冲提供给IC卡，请将SCKn引脚输出输入到IC卡的CLK引脚。

MCU的输出端口可用于输出复位信号。

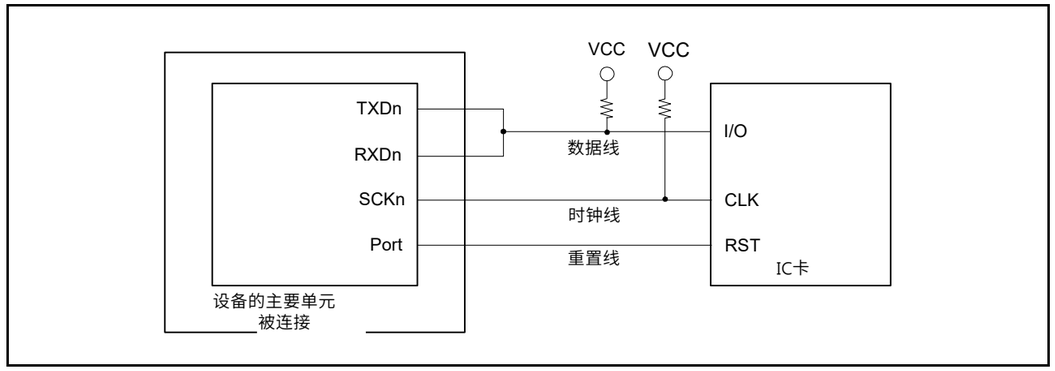


Figure 29.45 与智能卡（IC卡）的连接示例

29.6.2 数据格式（块传输模式除外）

图29.46显示了智能卡接口模式下的数据传输格式。

数据传输格式如下：

- 一帧由异步模式下的8位数据和一个奇偶校验位组成
- 在传输过程中，从奇偶校验位结束到下一帧开始，设置至少2个ETU（基本时间单位–传输1位所需的时间）的保护时间
- 如果在接收期间检测到奇偶校验错误，则在从起始位经过10.5ETU后输出1ETU的低错误信号
- 如果在传输过程中对错误信号进行采样，则在至少2个ETU后会自动重新传输相同的数据。

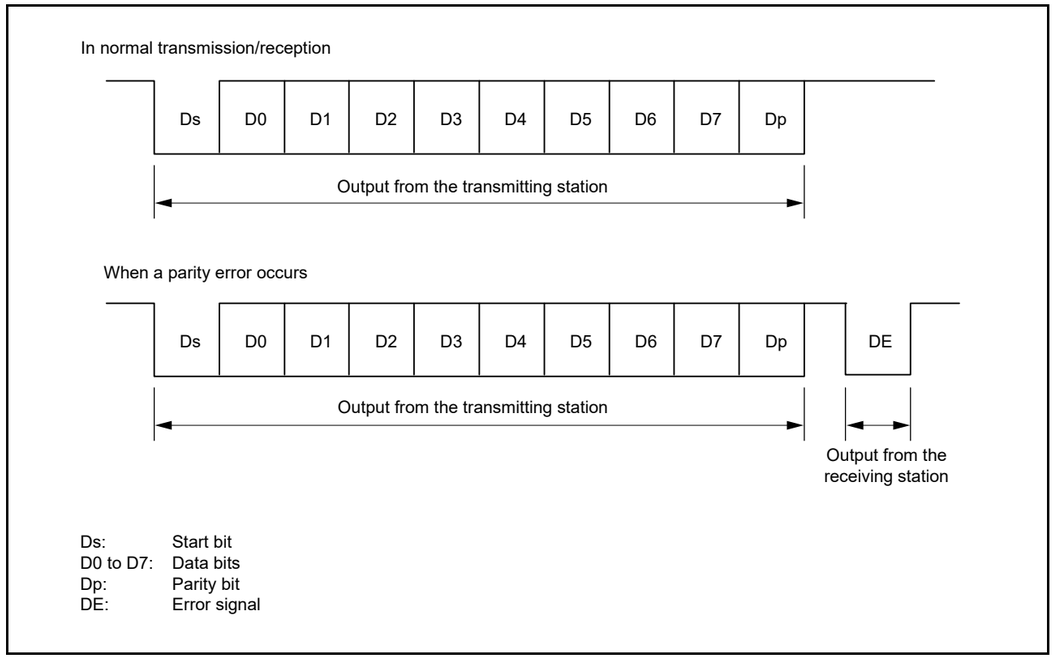


Figure 29.46 Data formats in smart card interface mode

For communication with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct convention type

For the direct convention type, logic levels 1 and 0 correspond to the Z and A states, respectively, and data is transferred with LSB-first as the start character, as shown in Figure 29.47. Therefore, data in the start character in Figure 29.47 is 3Bh.

When using the direct convention type, write 0 to both the SDIR and SINV bits in SCMR. Write 0 to the PM bit in SMR_SMCI to use even parity, which is described by the smart card standard.

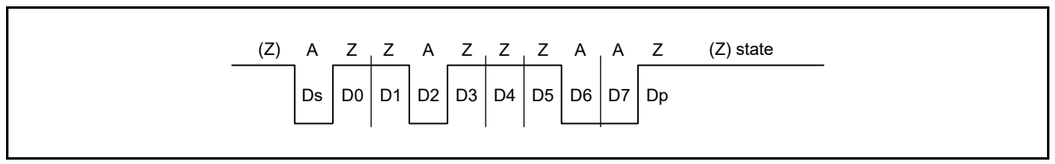


Figure 29.47 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse convention type

For the inverse convention type, logic levels 1 and 0 correspond to the A and Z states, respectively and data is transferred with MSB-first as the start character, as shown in Figure 29.48. Therefore, data in the start character in Figure 29.48 is 3Fh.

When using the inverse convention type, write 1 to both the SDIR and SINV bits in SCMR. The parity bit is at logic level 0 to produce even parity, which is described by the smart card standard, and corresponds to state Z. Because the SINV bit only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

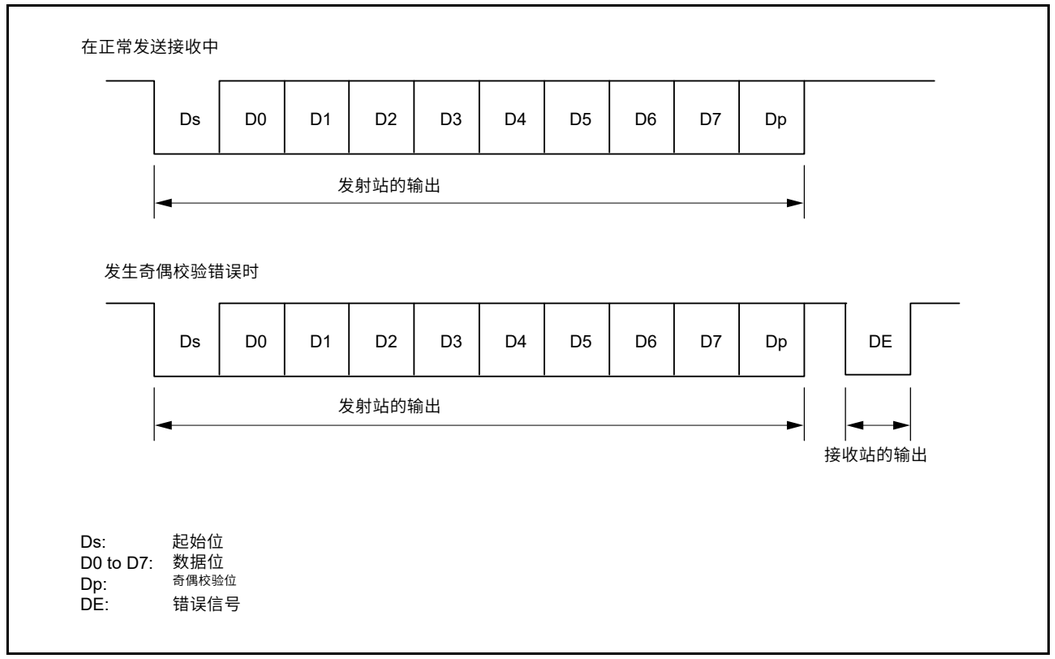


Figure 29.46 智能卡接口模式下的数据格式

与直接约定型和逆约定型的IC卡进行通信时，请按照本节的步骤进行。

(1) 直接约定型

对于直接约定类型，逻辑电平1和0分别对应于Z和A状态，数据以LSB-first作为起始字符进行传输，如图29.47所示。因此，图29.47中起始字符中的数据为3Bh。

使用直接约定类型时，将0写入SCMR中的SDIR和SINV位。将0写入PM位SMR_SMCI使用偶校验，由智能卡标准描述。

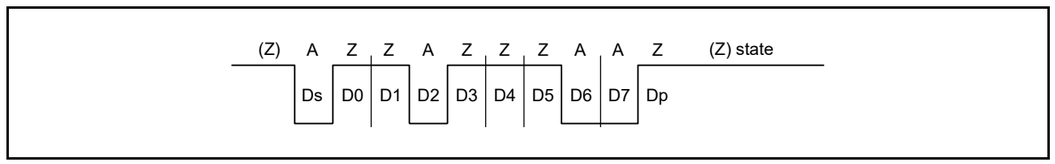


Figure 29.47 与SCMR=0中的SDIR、SCMR=0中的SINV和SMR_SMCI=0中的PM的直接约定

(2) 逆约定型

对于逆约定类型，逻辑电平1和0分别对应于A和Z状态，数据以MSB-first作为起始字符进行传输，如图29.48所示。因此，图29.48中起始字符中的数据为3Fh。

使用逆约定类型时，将1写入SCMR中的SDIR和SINV位。奇偶校验位为逻辑电平0，产生偶校验，由智能卡标准描述，对应状态Z。由于SINV位仅将数据位D7反转为D0，因此向SMR_SMCI中的PM位写入1以反转发送和接收的奇偶校验位。

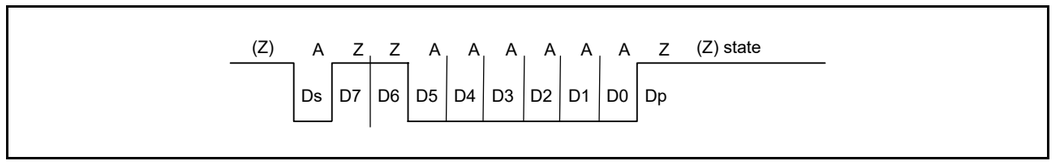


Figure 29.48 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

29.6.3 Block Transfer Mode

Block transfer mode differs from non-block transfer mode of the smart card interface mode in the following respects:

- If a parity error is detected during reception, no error signal is output. Because the PER bit in SSR_SMCI is set by error detection, clear the PER bit before receiving the parity bit of the next frame.
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in non-block transfer mode of the smart card interface mode, but the flag is read as 0 because no error signal is transferred.

29.6.4 Receive Data Sampling Timing and Reception Margin

Only the clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate based on the BCP2 settings in SCMR and the BCP[1:0] bits in SMR_SMCI.

For data reception, the falling edge of the start bit is sampled with the base clock to perform synchronization.

Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as Figure 29.49 shows. The reception margin is determined by the following formula:

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5) F - \frac{\left| D - 0.5 \right|}{N} (1 + F) \right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock (N = 32, 64, 372, 256)

D: Duty cycle of clock (D = 0 to 1.0)

L: Frame length (L = 10)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined by the following formula:

$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\%$

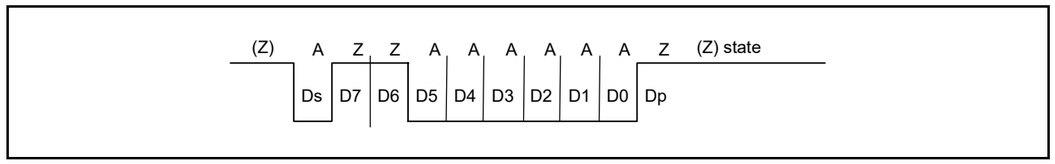


Figure 29.48 SCMR=1中的SDIR、SCMR=1中的SINV和SMR_SMCI=1中的PM的逆约定

29.6.3 块传输模式

块传输模式与智能卡接口模式的非块传输模式有以下几个方面的不同：

- 如果在接收期间检测到奇偶校验错误，则不输出错误信号。因为SSR_SMCI中的PER位是通过错误检测设置的，所以在接收下一帧的奇偶校验位之前清除PER位。
- 在传输过程中，从奇偶校验位结束到下一帧开始至少设置1个ETU作为保护时间
- 因为没有重传相同的数据，所以在传输开始后SSR_SMCI中的TEND标志设置为11.5ETU
- 在块传输模式下，SSR_SMCI中的ERS 标志指示错误信号状态，与智能卡接口模式的非块传输模式一样，但该标志被读取为0，因为没有传输错误信号。

29.6.4 接收数据采样时序和接收裕量

只有片内波特率发生器产生的时钟可以用作智能卡接口模式下的传输时钟。

在此模式下，SCI可以在频率为32、64、372、256、93、128、186或512倍比特率的基础时钟上运行，具体取决于SCMR中的BCP2设置和BCP[1:0]SMR_SMCI中的位。

对于数据接收，起始位的下降沿与基本时钟一起采样以执行同步。

接收数据在基本时钟的第16、32、186、128、46、64、93和256个上升沿采样，以便可以在每个位的中间锁存，如图29.49所示。接收余量由以下公式确定：

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5) F - \frac{\left| D - 0.5 \right|}{N} (1 + F) \right| \times 100\ [\%]$$

M：接收余量（%）

N：比特率与时钟的比率（N=32、64、372、256）

D：时钟的占空比（D=0到1.0）

L：帧长（L=10）

F：时钟频率偏差的绝对值

假设指定公式中的F=0、D=0.5和N=372的值，则接收裕度由以下公式确定：

$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\%$

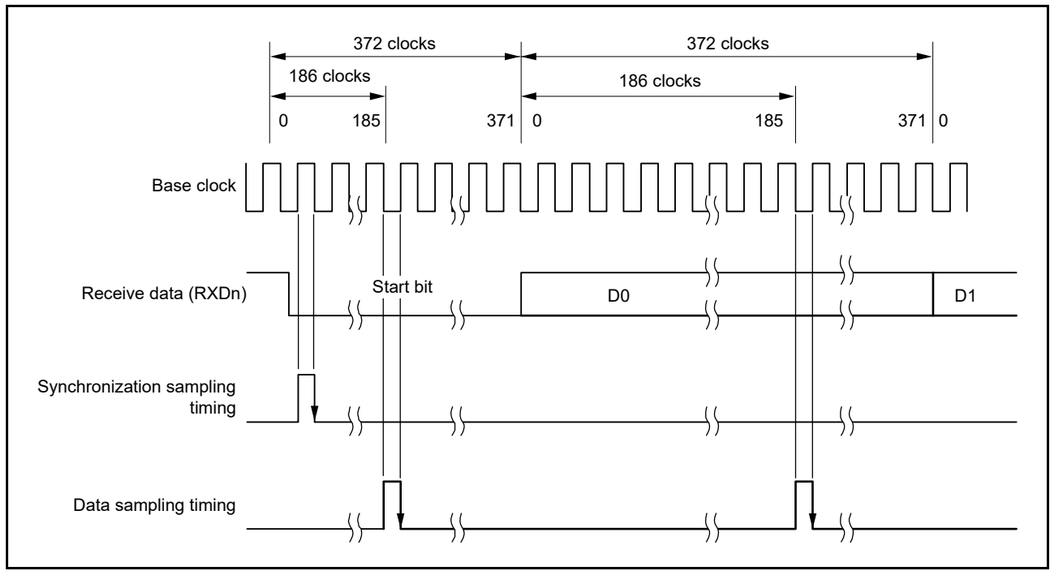


Figure 29.49 Receive data sampling timing in smart card interface mode for clock frequency 372 times the bit rate

29.6.5 SCI Initialization

Before transmitting and receiving data, write the initial value 00h to SCR_SMCI and initialize the SCI as shown in the example in Figure 29.50.

Be sure to set the initial value in the TIE, RIE, TE, RE, TEIE bits in SCR_SMCI before switching from transmission to reception mode, or from reception to transmission mode. When the RE bit in SCR_SMCI is set to 0, the RDR register is not initialized.

To change from reception to transmission mode, first check that reception is complete, and then initialize the SCI. At the end of initialization, set the TE bit to 1 and the RE bit to 0 in the SCR_SMCI register. Reception completion can be verified by reading the SCIn_RXI request, or ORER or PER flag in SSR_SMCI.

To change from transmission to reception mode, first check that transmission is complete, and then initialize the SCI. At the end of initialization, set the TE bit to 0 and the RE bit to 1 in the SCR_SMCI register. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

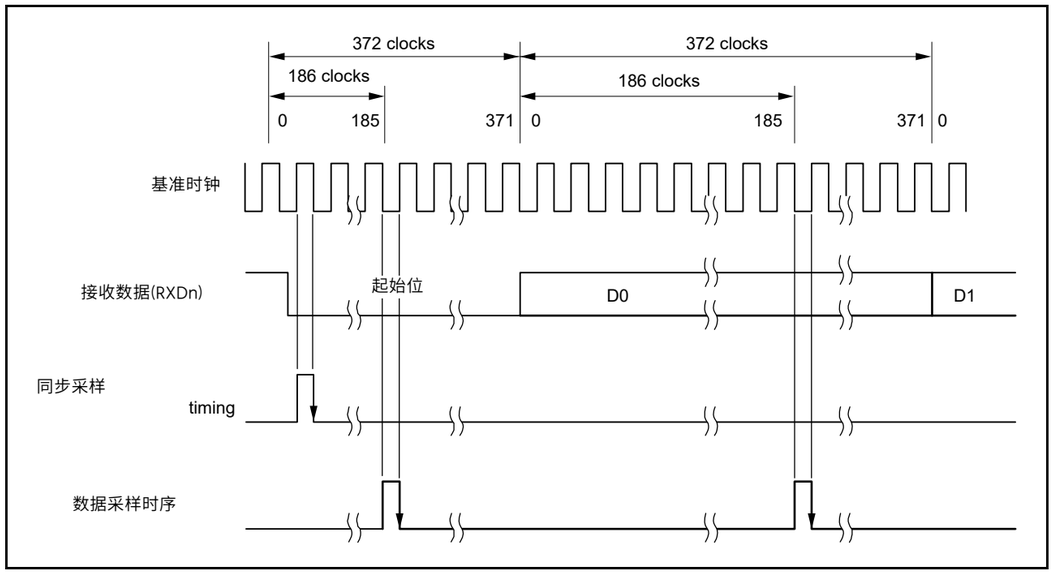


Figure 29.49 智能卡接口模式下接收数据采样时序，时钟频率为比特率的372倍

29.6.5 SCI初始化

在发送和接收数据之前，将初始值00h写入SCR_SMCI并初始化SCI，如图29.50中的示例所示。

在从发送模式切换到接收模式或从接收模式切换到发送模式之前，请务必在SCR_SMCI的TIE、RIE、TE、RE、TEIE位中设置初始值。当SCR_SMCI中的RE位设置为0时，RDR寄存器未初始化。

要从接收模式更改为发送模式，首先检查接收是否完成，然后初始化SCI。初始化结束时，将SCR_SMCI寄存器中的TE位设置为1，将RE位设置为0。可以通过读取SCIn_RXI请求或SSR_SMCI中的ORER或PER标志来验证接收完成。

要从发送模式更改为接收模式，首先检查发送是否完成，然后初始化SCI。初始化结束时，将SCR_SMCI寄存器中的TE位设置为0，将RE位设置为1。可以通过读取SSR_SMCI中的TEND标志来验证传输完成。

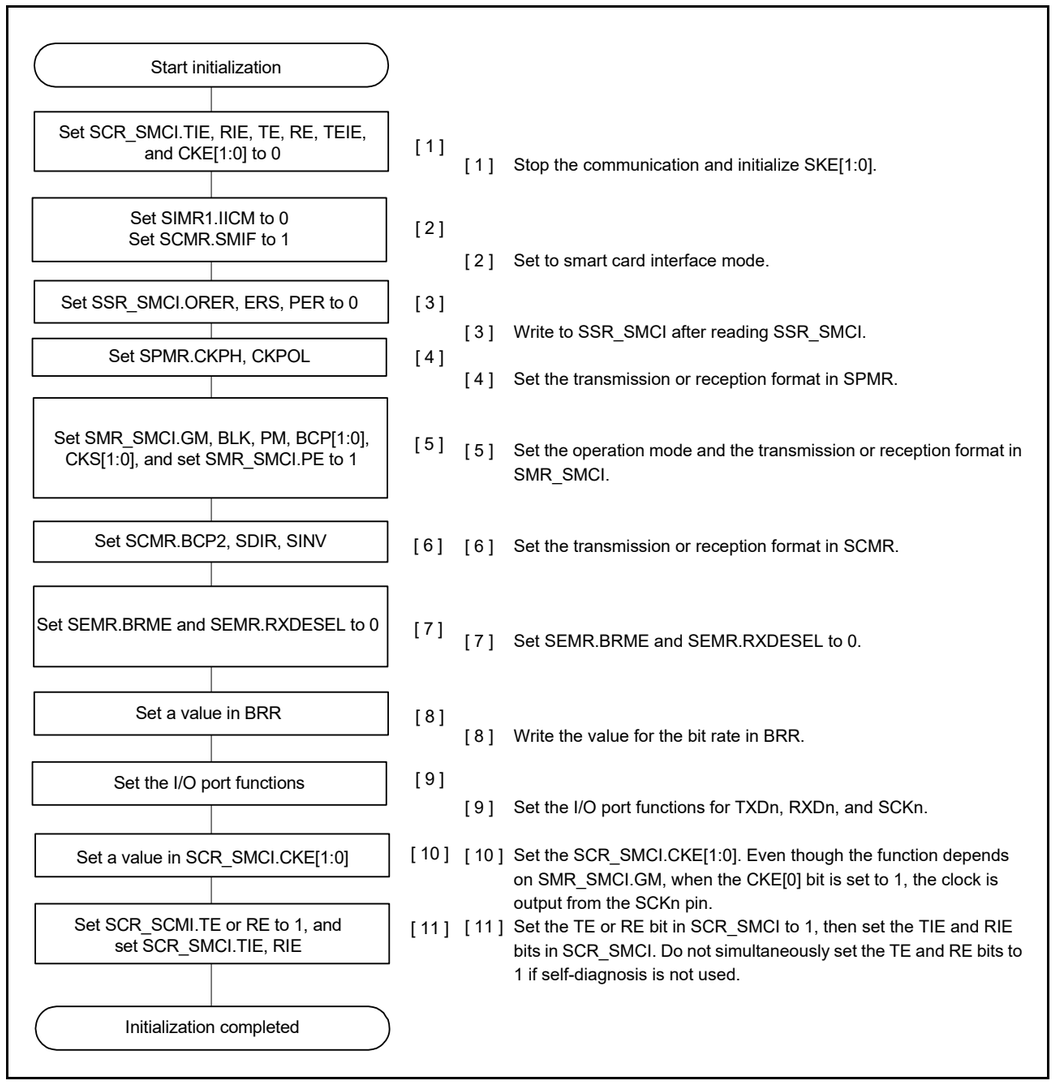


Figure 29.50 Example flow of SCI initialization in smart card interface mode

Figure 29.51 shows a timing diagram when data transmission is performed by transitioning to smart card interface mode according to the flow in Figure 29.50. Figure 29.51 shows when the GM bit in SMR_SMCI is set to 0. The timing in Figure 29.51 shows when the port is connected as SCKn and TXDn, the pins are Hi-Z because CKE[0] bit in SCR_SMCI is 0.

Start the clock output to the SCK pin by setting CKE[0] bit in SCR_SMCI to 1, then start data transmission by writing transmit data after setting TE bit in SCR_SMCI to 1. When TE bit in SCR_SMCI changes from 0 to 1, there is a preamble period for one frame before data transmission starts. In smart card interface mode, the TXDn pin is Hi-Z during a preamble period. Pull-up or pull-down for the SCKn and TXDn pins is required outside the MCU.

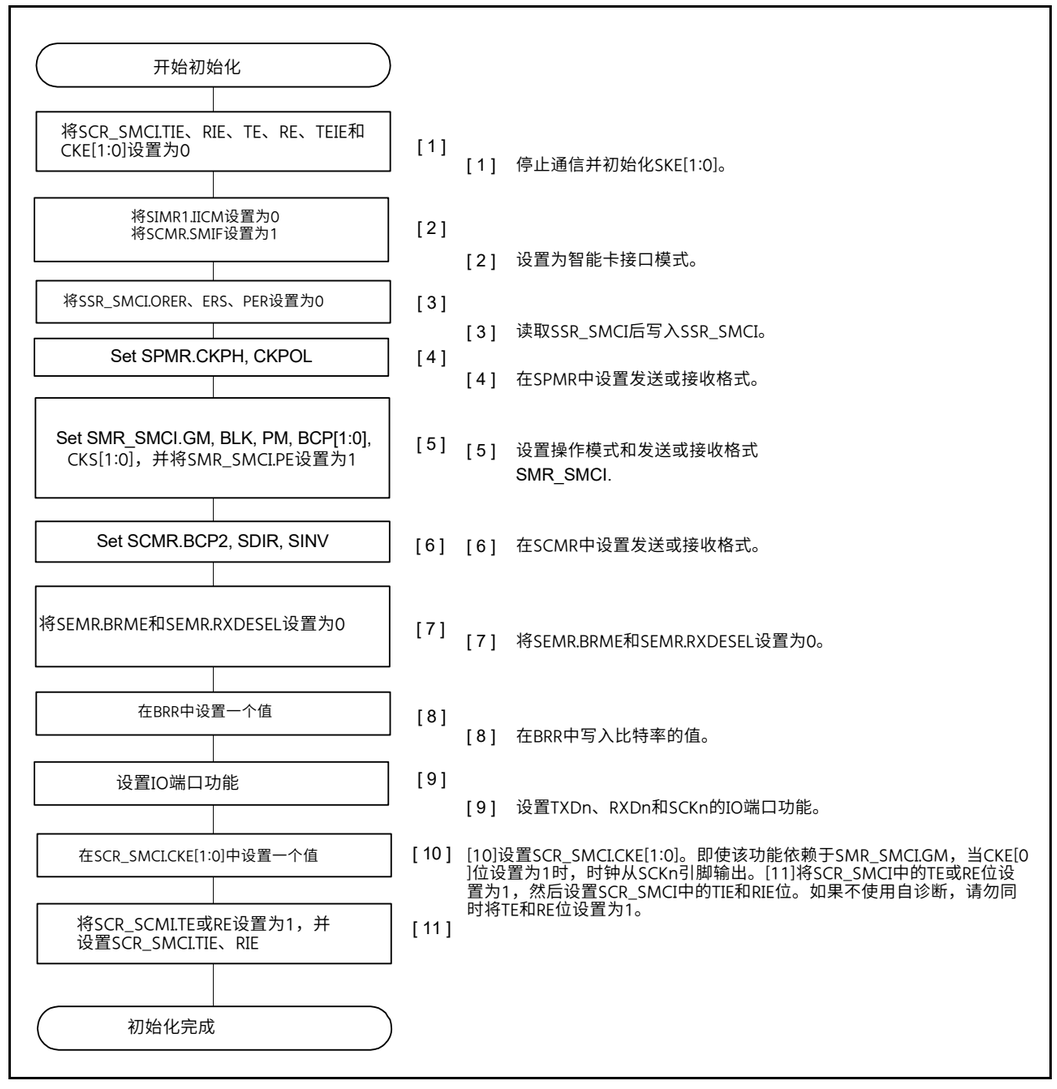


Figure 29.50 智能卡接口模式下SCI初始化流程示例

图29.51显示了当按照图29.50中的流程通过转换到智能卡接口模式来执行数据传输时的时序图。图29.51显示了SMR_SMCI中的GM位设置为0时。图29.51中的时序显示了当端口连接为SCKn和TXDn时，引脚为Hi-Z，因为SCR_SMCI中的CKE[0]位为0。

通过设置SCR_SMCI中的CKE[0]位为1，开始向SCK引脚输出时钟，然后在设置SCR_SMCI中的TE位为1后，通过写入发送数据开始数据传输。当SCR_SMCI中的TE位从0变为1时，有数据传输开始前一帧的前导周期。在智能卡接口模式下，TXDn引脚在前导期间为Hi-Z。SCKn和TXDn引脚的上拉或下拉需要在MCU外部进行。

In smart card interface mode, even when the TE and RE bits in SCR_SMCI are 0, the clock is continuously output if the clock output setting is used.

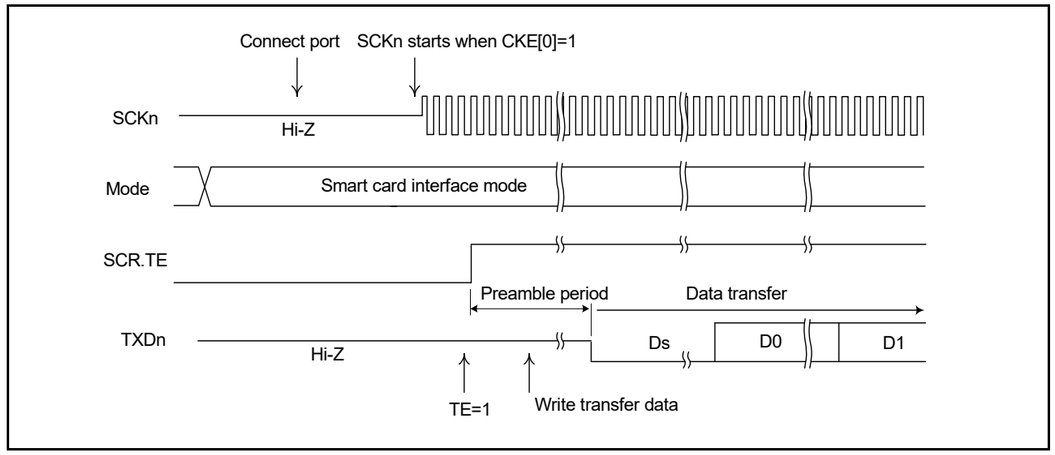


Figure 29.51 Example timing of data transmission in smart card interface mode

29.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be retransmitted in smart card mode. Figure 29.52 shows the data retransfer operation during transmission.

In Figure 29.52:

- [1] indicates when an error signal from the receiver end is sampled after 1-frame data is transmitted, the ERS flag in SSR_SMCI is set to 1. If the RIE bit is 1 in SCR_SMCI, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
- [2] indicates for a frame in which an error signal is received, the TEND flag in SSR_SMCI is not set. Data is retransferred from TDR to TSR allowing automatic data retransmission.
- [3] indicates if no error signal is returned from the receiver, the ERS flag is not set to 1.
- [4] indicates the SCI determines that the transmission of 1-frame data including the retransfer is complete, and the TEND flag is set. If the TIE bit in SCR_SMCI is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 29.54 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DMAC or DTC.

When the TEND flag in SSR_SMCI is set to 1 in transmission and when the TIE bit in SCR_SMCI is 1, an SCIn_TXI interrupt request is generated.

The DMAC or DTC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is specified as a source of DMAC or DTC activation beforehand, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DMAC or DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DMAC or DTC is not activated. Therefore, the SCI and DMAC or DTC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 to enable an SCIn_ERI interrupt request generation when an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DMAC or DTC, be sure to enable the DMAC or DTC before setting the SCI.

For DMAC or DTC settings, see section 17, DMA Controller (DMAC) and section 18, Data Transfer Controller (DTC).

在智能卡接口模式下，即使SCR_SMCI中的TE和RE位为0，如果使用时钟输出设置，时钟也会持续输出。

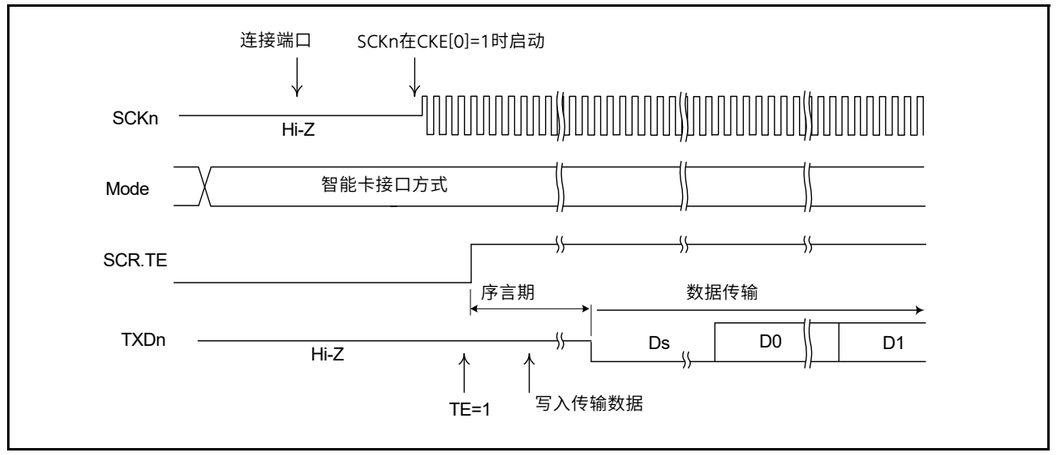


Figure 29.51 智能卡接口模式下数据传输时序示例

29.6.6 串行数据传输（块传输模式除外）

智能卡接口模式下的串行数据传输（块传输模式除外）与非智能卡接口模式下的串行数据传输不同之处在于，在智能卡模式下对错误信号进行采样，数据可以重传。图29.52显示了传输过程中的数据重传操作。

在图29.52中：

- [1]表示当发送1帧数据后，对接收端的错误信号进行采样时，SSR_SMCI中的ERS标志置1。如果SCR_SMCI中的RIE位为1，则产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将ERS 标志清零。
- [2]表示对于接收到错误信号的帧，SSR_SMCI中的TEND标志未设置。数据从TDR重新传输到TSR，允许自动数据重新传输。
- [3]表示如果接收器没有返回错误信号，则ERS 标志不设置为1。
- [4]表示SCI确定包括重传在内的1帧数据的传输完成，并且设置了TEND标志。如果SCR_SMCI中的TIE位为1，则产生SCIn_TXI中断请求。将传输数据写入TDR以开始传输下一个数据。

图29.54显示了串行传输的示例流程。所有处理步骤都使用SCIn_TXI中断请求自动执行以激活DMAC或DTC。

当SSR_SMCI中的TEND标志在传输中设置为1并且SCR_SMCI中的TIE位为1时，将产生SCIn_TXI中断请求。

如果事先将SCIn_TXI中断请求指定为DMAC或DTC激活源，则DMAC或DTC由SCIn_TXI中断请求激活，从而允许传输数据。当DMAC或DTC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在此重传期间，TEND标志保持为0，并且不激活DMAC或DTC。因此，SCI和DMAC或DTC会自动传输指定的字节数，包括发生错误时的重传。因为ERS 标志不会自动清除，所以将RIE位设置为1以在发生错误时启用SCIn_ERI中断请求生成，并将ERS 标志清除为0。

使用DMAC或DTC发送或接收数据时，请务必在设置DMAC或DTC之前启用DMAC或DTC
SCI.

对于DMAC或DTC设置，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

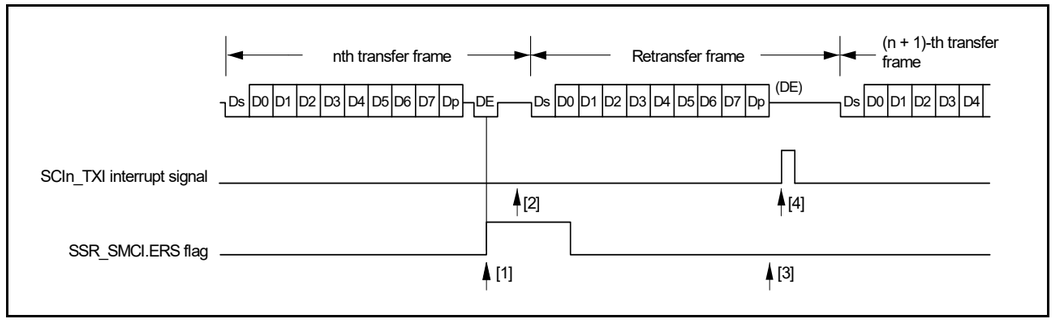


Figure 29.52 Data retransfer operation in SCI transmission mode

Note: The TEND flag in SSR_SMCI is set at different timings depending on the GM bit setting in SMR_SMCI.

Figure 29.53 shows the TEND flag generation timing.

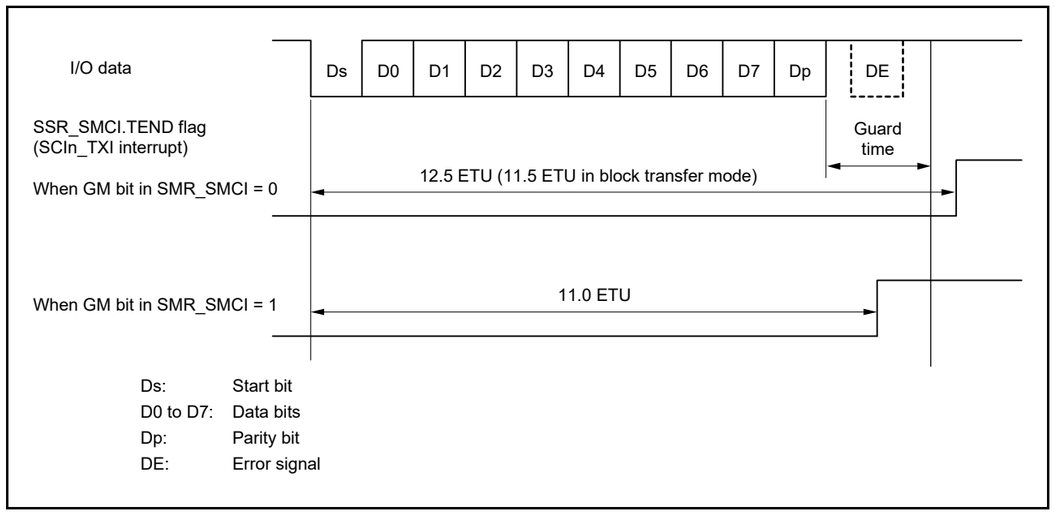


Figure 29.53 SSR.TEND flag generation timing during transmission

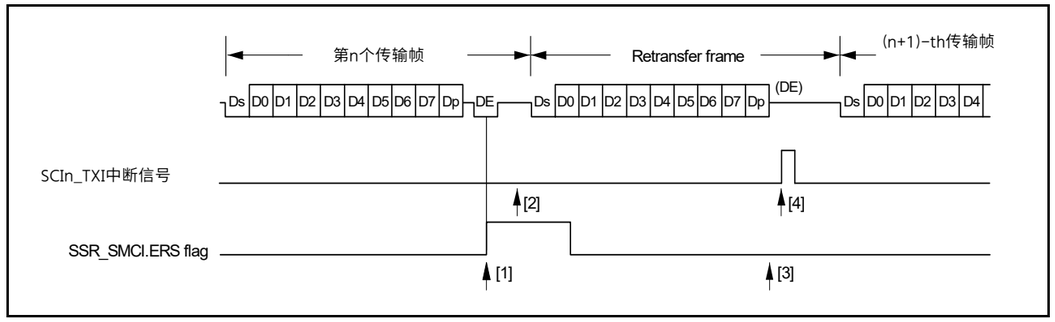


Figure 29.52 SCI传输模式下的数据重传操作

Note: SSR_SMCI中的TEND标志根据SMR_SMCI中的GM位设置在不同的时间设置。

图29.53显示了TEND标志生成时序。

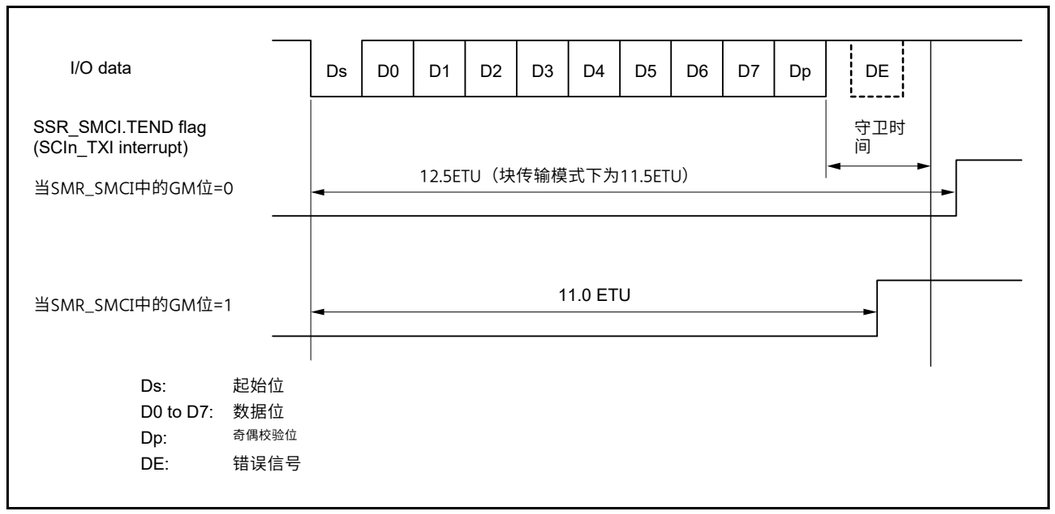


Figure 29.53 发送期间的SSR.TEND标志生成时序

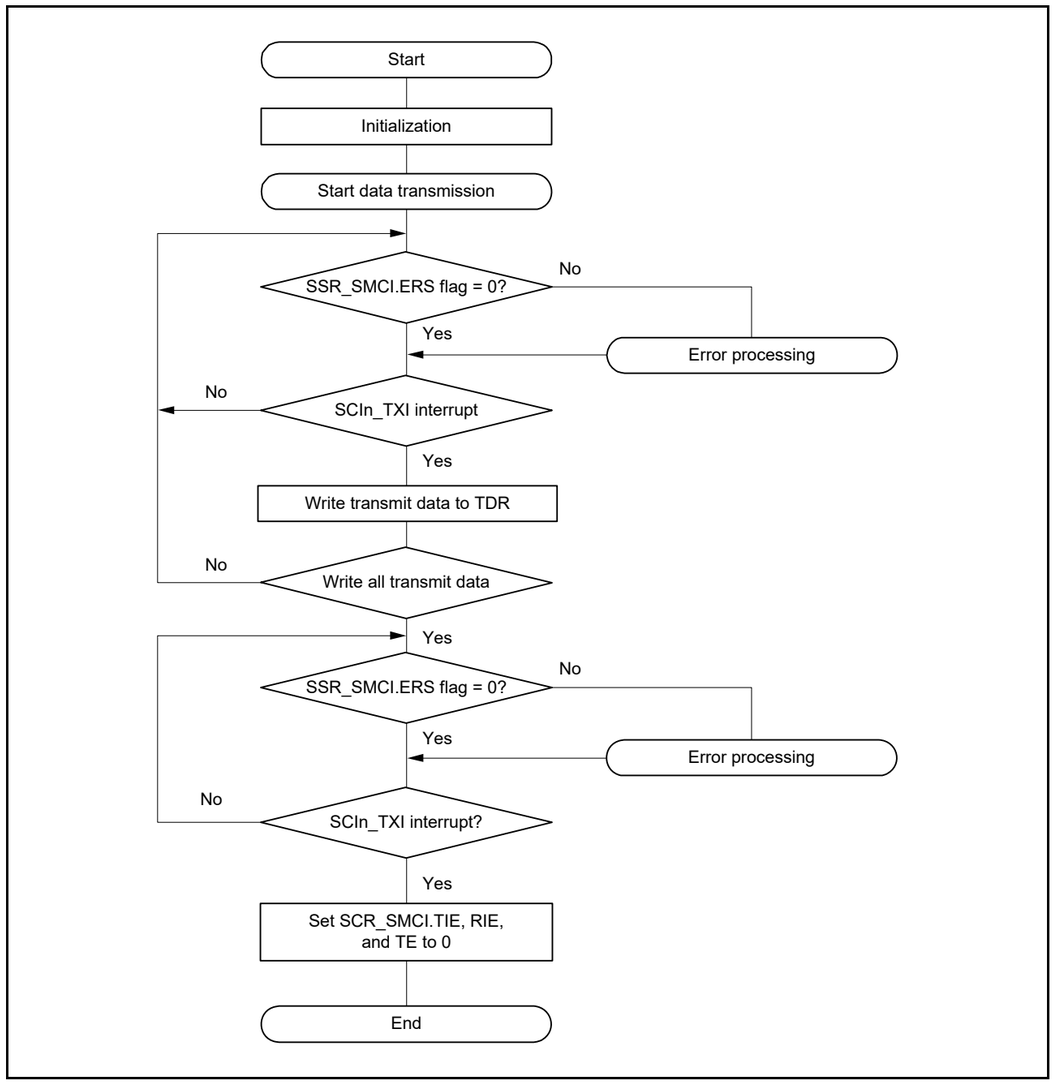


Figure 29.54 Example flow of smart card interface transmission

29.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 29.55 shows the data retransfer operation in reception mode.

- [1] indicates if a parity error is detected in the receive data, the PER flag in SSR_SMCI is set to 1. When the RIE bit in SCR_SMCI is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
- [2] indicates for a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
- [3] indicates when no parity error is detected, the PER flag in SSR_SMCI is not set to 1.
- [4] indicates the data is determined to be received successfully. When the RIE bit in SCR_SMCI is 1, an SCIn_RXI interrupt request is generated.

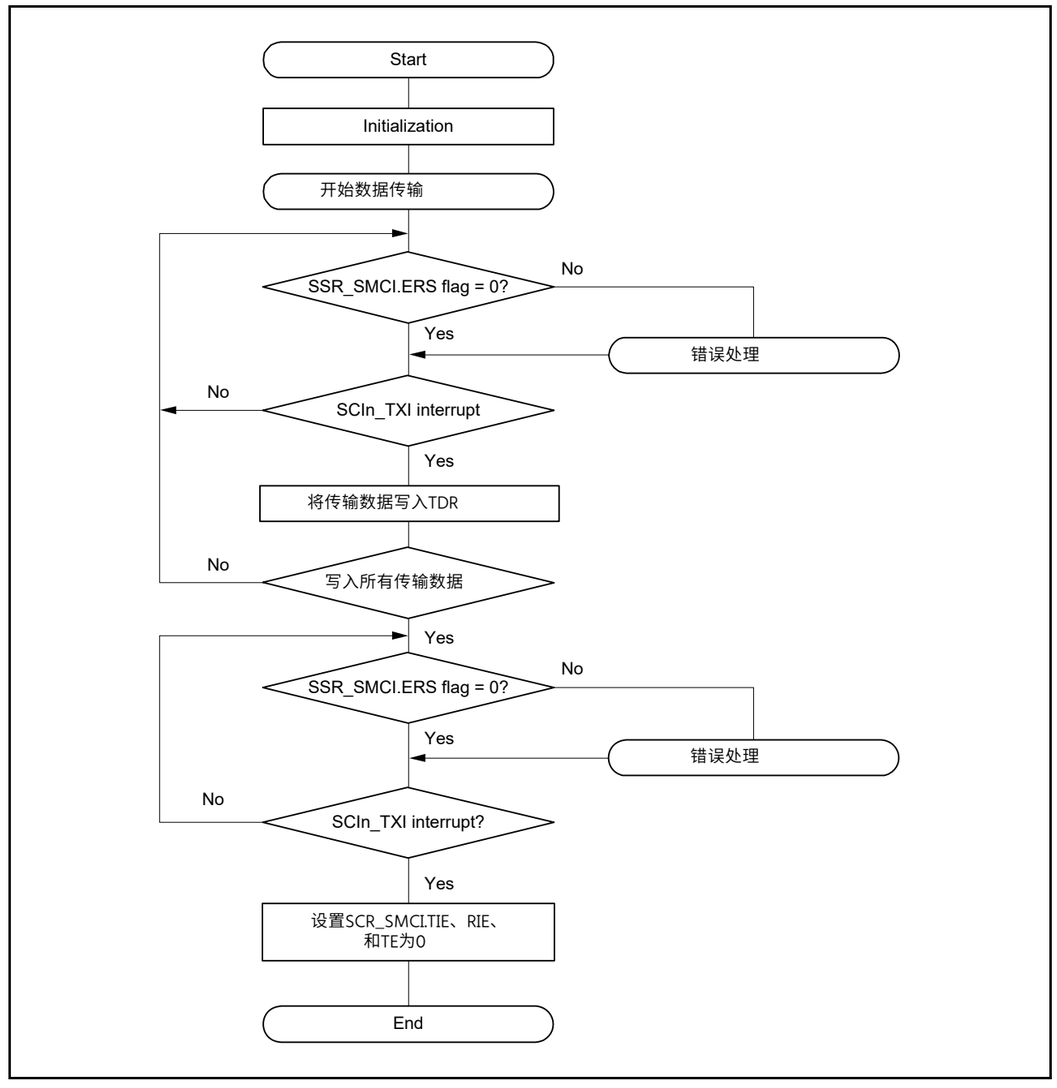


Figure 29.54 智能卡接口传输示例流程

29.6.7 串行数据接收（块传输模式除外）

智能卡接口模式下的串行数据接收与非智能卡接口模式下的串行数据接收类似。图29.55显示了接收模式下的数据重传操作。

- [1]表示如果在接收数据中检测到奇偶校验错误，则将SSR_SMCI中的PER标志设置为1。当SCR_SMCI中的RIE位为1时，产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将PER标志清零。
- [2]表示对于检测到奇偶校验错误的帧，不产生SCIn_RXI中断。
- [3]表示当没有检测到奇偶校验错误时，SSR_SMCI中的PER标志不设置为1。
- [4]表示确定数据接收成功。当SCR_SMCI的RIE位为1时，产生SCIn_RXI中断请求。

Figure 29.56 shows an example flow of serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DMAC or DTC.

In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DMAC or DTC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is specified as a source of DMAC or DTC activation beforehand, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DMAC or DTC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DMAC or DTC are transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, therefore allowing the data to be read.

When a reception is forced to terminate by setting the RE bit in SCR_SMCI to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 29.3.9, Serial Data Reception in Asynchronous Mode.

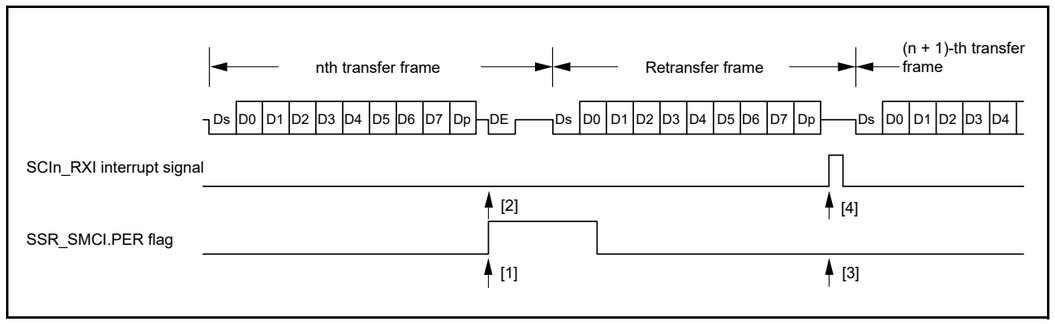


Figure 29.55 Data retransfer operation in SCI reception mode with data retransfer operation during reception

图29.56显示了串行数据接收的示例流程。所有处理步骤都使用SCIn_RXI中断请求自动执行以激活DMAC或DTC。

在接收时，将RIE位设置为1允许产生SCIn_RXI中断请求。如果事先将SCIn_RXI中断请求指定为DMAC或DTC激活源，则DMAC或DTC由SCIn_RXI中断请求激活，从而允许传输接收数据。

如果接收期间发生错误并且SSR_SMCI中的ORER或PER标志设置为1，则会生成接收错误中断(SCIn_ERI)请求。错误发生后清除错误标志。如果发生错误，则不激活DMAC或DTC并跳过接收数据。因此，将传输在DMAC或DTC中指定的接收数据字节数。

如果在接收过程中发生奇偶校验错误并且PER标志设置为1，则接收数据将传输到RDR，因此可以读取数据。

如果在操作期间通过将SCR_SMCI中的RE位设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的已接收数据可能留在RDR中。

Note: 有关块传输模式下的操作，请参见第29.3.9节，异步模式下的串行数据接收。

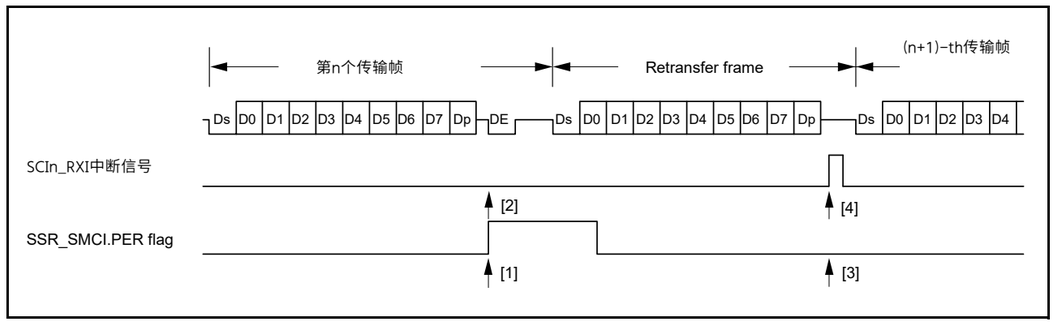


Figure 29.55 SCI接收模式下的数据重传操作与接收期间的数据重传操作

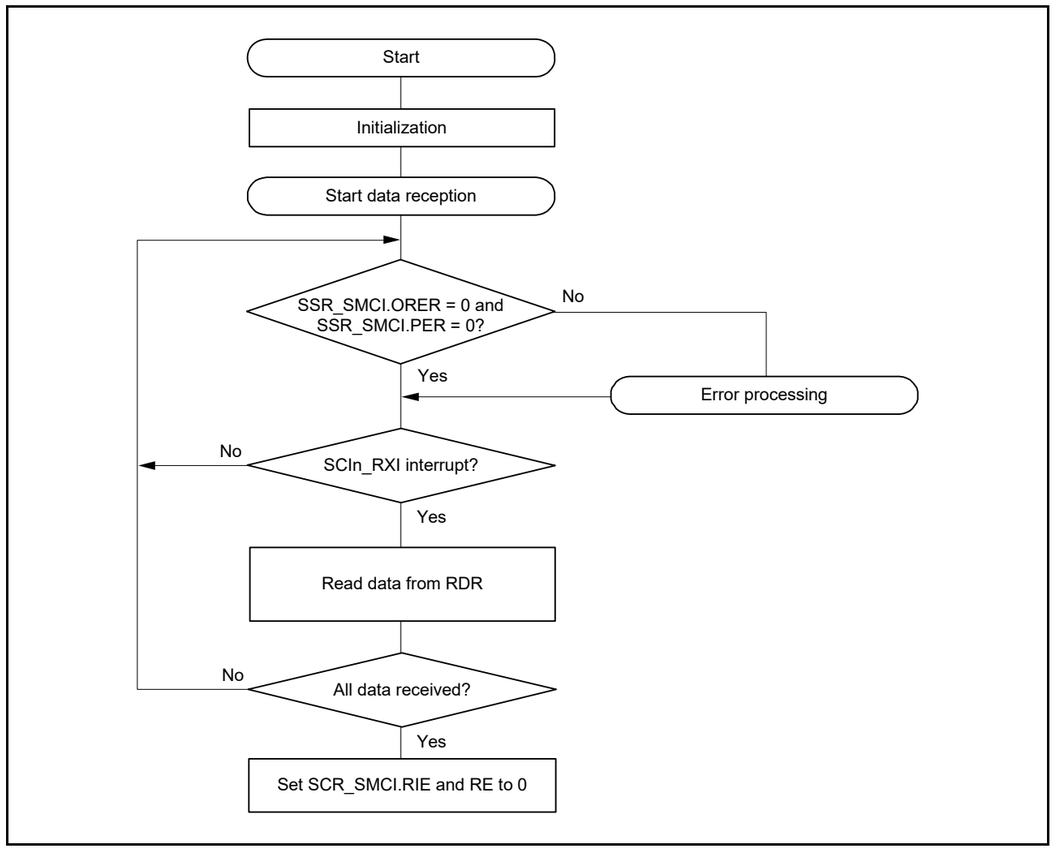


Figure 29.56 Example flow of smart card interface reception

29.6.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1: 0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 29.2.12, Serial Control Register for Smart Card Interface Mode (SCR_SMCI)(SCMR.SMIF = 1). When setting the clock output, the base clock described in section 29.6.4, Receive Data Sampling Timing and Reception Margin is output.

Figure 29.57 shows an example timing for the clock output control when the CKE[1] bit in SCR_SMCI is set to 0 and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected on the SCK pin, so there is a possibility that pulses with an unintended width might be output from the SCK pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

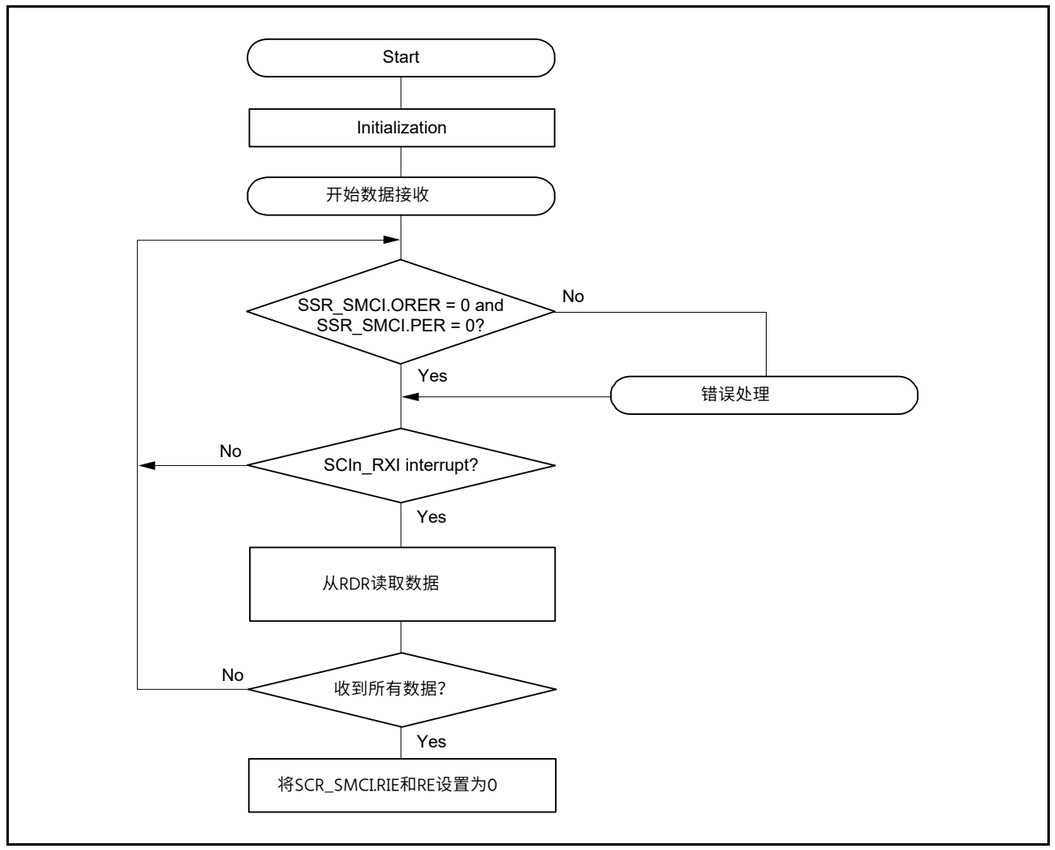


Figure 29.56 智能卡接口接收示例流程

29.6.8 时钟输出控制

当SMR_SMCI中的GM位设置为1时，时钟输出可由SCR_SMCI中的CKE[1:0]位控制。有关CKE[1:0]位的详细信息，请参见第29.2.12节，智能卡接口模式的串行控制寄存器(SCR_SMCI)(SCMR.SMIF=1)。设置时钟输出时，输出第29.6.4节"接收数据采样时序和接收裕量"中描述的基本时钟。

图29.57显示了当SCR_SMCI中的CKE[1]位设置为0且控制SCR_SMCI中的CKE[0]位。

当SMR_SMCI中的GM位为0时，SCR_SMCI中CKE[0]位的输出控制立即反映在SCK引脚，因此有可能会从SCK引脚输出具有意外宽度的脉冲。

当SMR_SMCI中的GM位为1时，即使SCR_SMCI中的CKE[0]位发生变化，也会输出与基本时钟脉冲宽度相同的时钟。

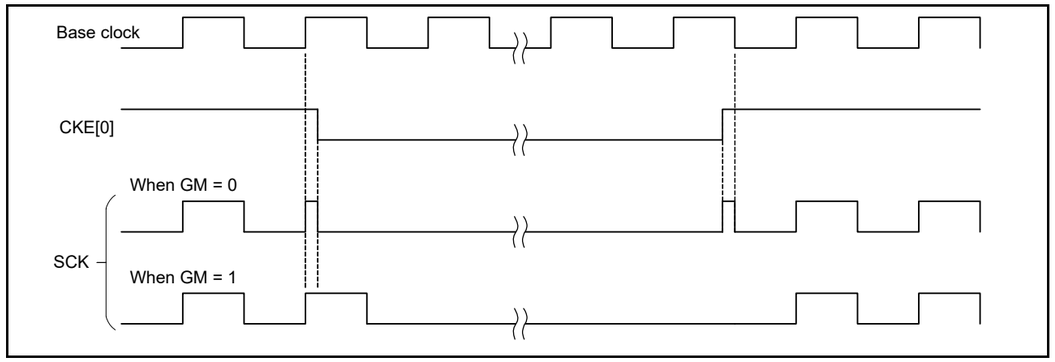


Figure 29.57 Clock output control

29.7 Operation in Simple IIC Mode

Simple I²C bus format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as a partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I²C bus format and timing are shown in Figure 29.58 and Figure 29.59.

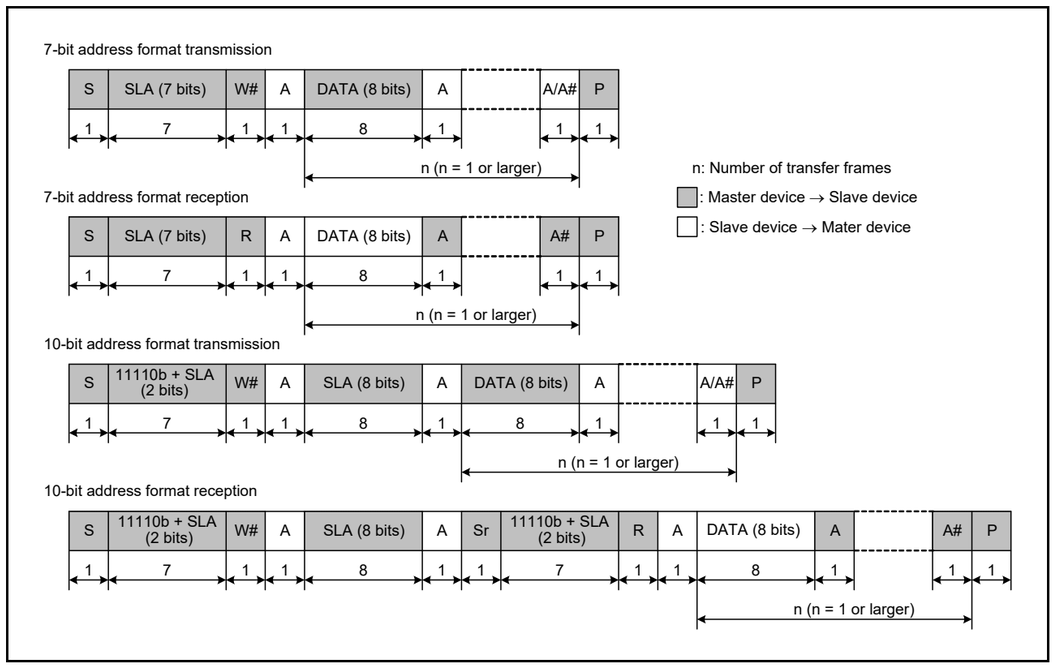


Figure 29.58 I²C bus format

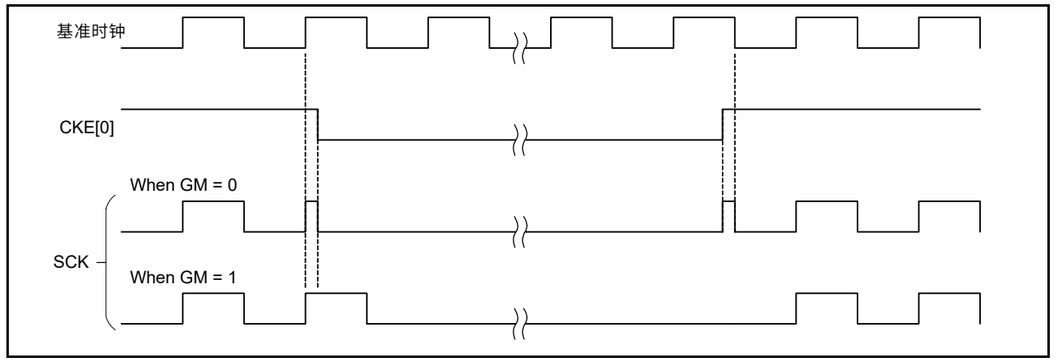


Figure 29.57 时钟输出控制

29.7 简单IIC模式下的操作

简单I2C总线格式由8个数据位和一个确认位组成。通过在启动条件或重启条件之后继续进入从地址帧，主设备可以指定从设备作为通信伙伴。当前指定的从设备保持有效，直到指定新的从设备或满足停止条件。所有帧中的8个数据位从MSB开始按顺序传输。

I2C总线格式和时序如图29.58和图29.59所示。

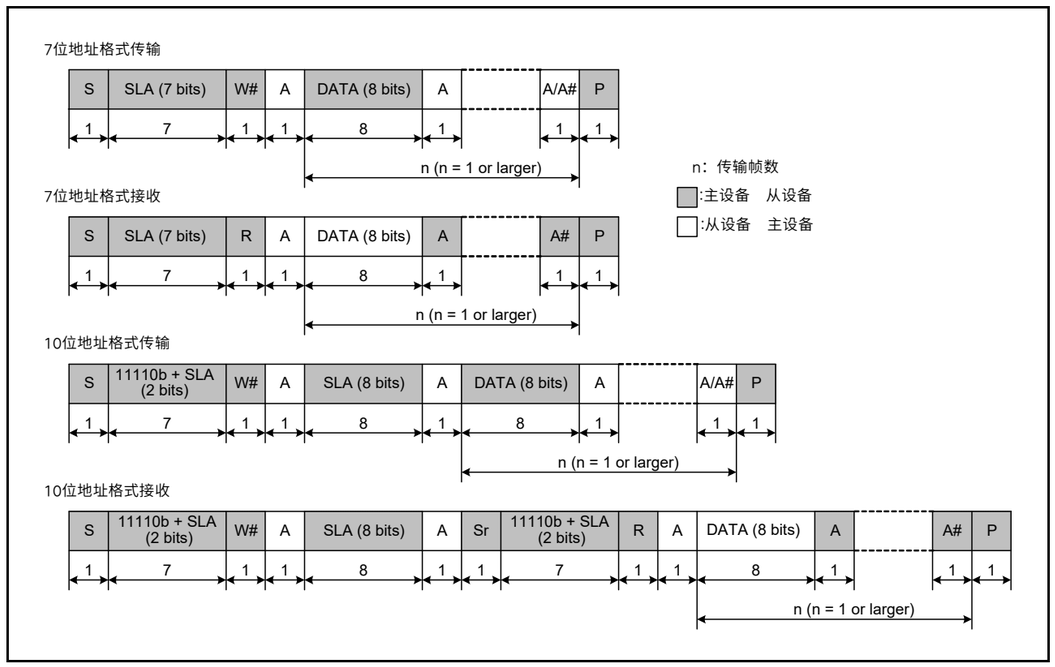


Figure 29.58 I2C总线格式

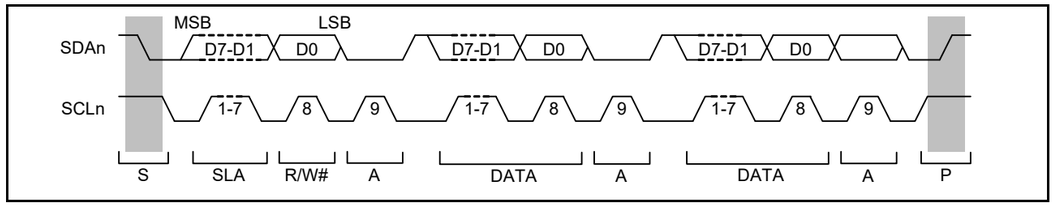


Figure 29.59 I²C bus timing when SLA is 7 bits

S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high.

SLA: Indicates a slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.

A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return to low indicates ACK and return to high indicates NACK.

Sr: Indicates a restart condition when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses.

DATA: Indicates the data being received or transmitted.

P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high level when the SCLn line is high.

29.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the IICSTAREQ bit in SIMR3 causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

- The level on the SDAn line falls (from high level to low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from high level to low level), the IICSTAREQ bit is set to 0, and a start-condition generated interrupt is output.

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at a low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from low to high level)
- When the high level on the SCLn line is detected, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from high level to low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from high level to low level), the IICRSTAREQ bit in SIMR3 is set to 0, and a restart-condition generated interrupt is output.

Writing 1 to the IICSTPREQ bit in SIMR3 causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from high level to low level) and the SCLn line is kept at a low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from low to high level)

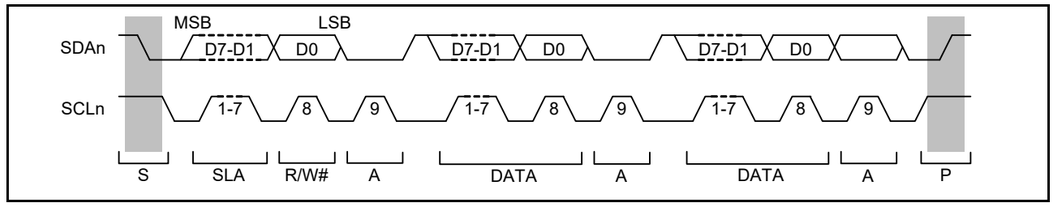


Figure 29.59 SLA为7位时的I2C总线时序

S：表示启动条件，当主设备将SDAn线上的电平从高电平变为低电平而SCLn线为高电平时。

SLA: 指示从地址，主设备通过该地址选择从设备。

RW#：指示传输方向（接收或传输）。值1表示从从设备传输到主设备，0表示从主设备传输到从设备。

AA#：表示确认位。这由从设备返回用于主传输，并由主设备返回用于主接收。返回低电平表示ACK，返回高电平表示NACK。

Sr：当主设备将SDAn线上的电平从高电平变为低电平而SCLn线为高电平且经过设置时间后，表示重启条件。

DATA: 表示正在接收或发送的数据。

P：表示停止条件，当SCLn线为高电平时，主设备将SDAn线上的电平从低电平变为高电平。

29.7.1 启动、重启和停止条件的生成

将1写入SIMR3中的IICSTAREQ位会导致产生启动条件。开始条件的生成通过以下操作进行：

- SDAn线上的电平下降（从高电平到低电平），SCLn线保持在释放状态
- 开始条件的保持时间设置为比特周期的一半，比特率由BRR设置确定
- SCLn线上的电平下降（从高电平变为低电平），IICSTAREQ位设置为0，并输出起始条件产生的中断。

将1写入SIMR3中的IICRSTAREQ位会导致产生重启条件。重新启动条件的生成通过以下操作进行：

- SDAn线被释放，SCLn线保持低电平
- SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定
- SCLn线被释放（从低电平过渡到高电平）
- 当检测到SCLn线上的高电平时，重启条件的建立时间设置为比特周期的一半，比特率由BRR设置确定
- SDAn线上的电平下降（从高电平到低电平）
- 重启条件的保持时间设置为比特周期的一半，比特率由BRR设置确定
- SCLn线上的电平下降（从高电平变为低电平），SIMR3中的IICRSTAREQ位设置为0，并输出重启条件产生的中断。

将1写入SIMR3中的IICSTPREQ位会导致产生停止条件。停止条件的生成通过以下操作进行：

- SDAn线上的电平下降（从高电平到低电平），SCLn线保持在低电平
- SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定
- SCLn线被释放（从低电平过渡到高电平）

- When the high level on the SCLn line is detected, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn is released (transition from low to high level), the IICSTPREQ bit in SIMR3 is set to 0, and a stop-condition generated interrupt is output.

Figure 29.60 shows the timing of operations in the generation of start, restart, and stop conditions.

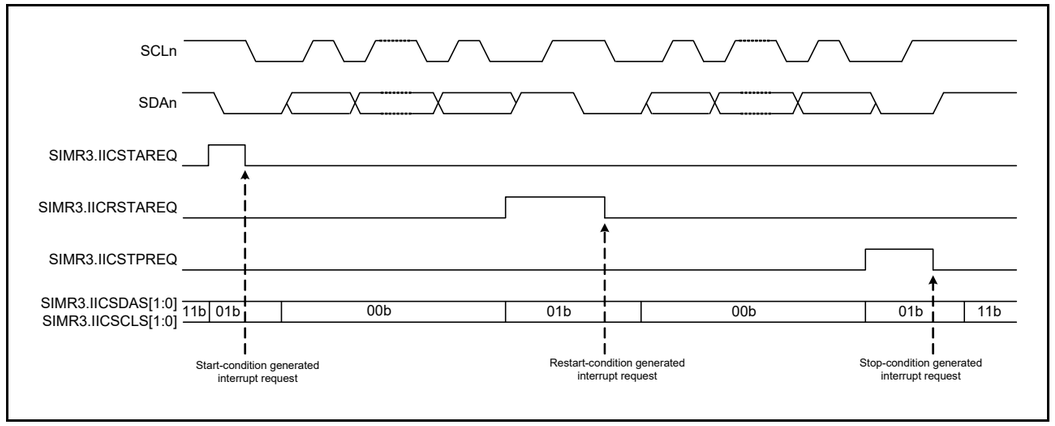


Figure 29.60 Timing of operations to generate start, restart, and stop conditions

29.7.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the IICCSC bit in SIMR2 to 1 allows clock synchronization control when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is input on the SCLn pin. Counting to determine the period at a high level starts after the input on the SCLn pin transitions to the high level.

The interval from the time until counting, to determine the period at high level that starts on the transition of the SCLn pin to the high level, is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 PCLK cycles). The period at high level of the internal SCLn clock is extended even when other devices are not placing the low level on the SCLn line.

If the ICCSC bit in SIMR2 register is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the IICCSC bit in SIMR2 is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed. Figure 29.61 shows an example operation to synchronize the clocks.

- 当检测到SCLn线上的高电平时，停止条件的建立时间设置为比特周期的一半，比特率由BRR设置确定
- SDAn被释放（从低电平转换为高电平），SIMR3中的IICSTPREQ位设置为0，并输出停止条件产生的中断。

图29.60显示了生成启动、重新启动和停止条件的操作时序。

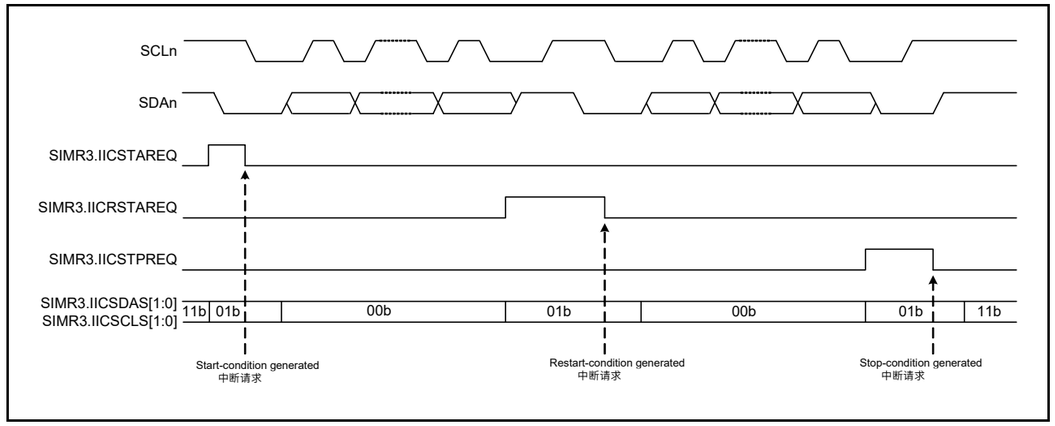


Figure 29.60 生成启动、重启和停止条件的操作时序

29.7.2 时钟同步

如果从设备在传输的另一侧插入等待，则可以将SCLn线驱动为低电平。将SIMR2中的IICCSC位设置为1，当内部SCLn时钟信号的电平与输入到SCLn引脚的电平之间出现差异时，可以进行时钟同步控制。

当IICCSC位设置为1时，内部SCLn时钟信号的电平由低变为高。当SCLn引脚输入低电平时，停止计数以确定高电平的周期。在SCLn引脚上的输入转换为高电平后，开始计数以确定高电平的周期。

从时间到计数的时间间隔，确定从SCLn引脚转换为高电平开始的高电平周期，是SCLn输出延迟的总和，SCLn引脚输入的噪声过滤延迟（噪声滤波器的采样时钟为2或3个周期），内部处理的延迟（1或2个PCLK周期）。即使其他设备没有将低电平置于SCLn线上，内部SCLn时钟的高电平周期也会延长。

如果SIMR2寄存器中的ICCSC位为1，则通过对SCLn引脚上的输入和内部SCLn时钟进行逻辑与来获得数据发送和接收的同步。如果SIMR2中的IICCSC位为0，则与内部SCLn时钟同步，用于数据的发送和接收。

如果从设备在发出启动、重新启动或停止条件的生成请求后，在内部SCLn时钟信号从低电平转变为高电平之前的间隔中插入一个等待周期，则直到生成的时间为延长了那个时期。

如果从设备在内部SCLn时钟信号从低电平转变为高电平之后插入等待周期，尽管在不停止等待周期的情况下发出生成完成中断，但不能保证条件本身的生成。图29.61显示了同步时钟的示例操作。

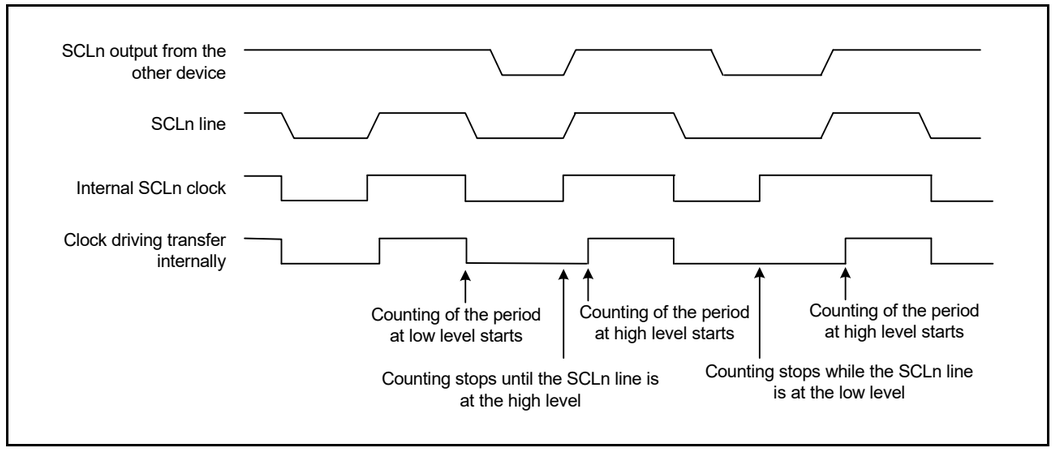


Figure 29.61 Example operation for clock synchronization

29.7.3 SDA Output Delay

The IICDL[4:0] bits in SIMR1 can be used to set a delay for output on the SDAn pin relative to the falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable. The delay settings represent periods of the associated numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLK, by the divisor selected in the CKS[1:0] bit in the SMR register). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and an acknowledge bit.

If the SDAn output delay is shorter than the time required for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility for erroneous operation of slave devices. Ensure that the settings for the output delay on the SDAn pin specify a time period greater than the time that the output on the SCLn pin takes to fall (300 ns for IIC in standard mode and fast mode).

Figure 29.62 shows the timing of delays in SDAn output.

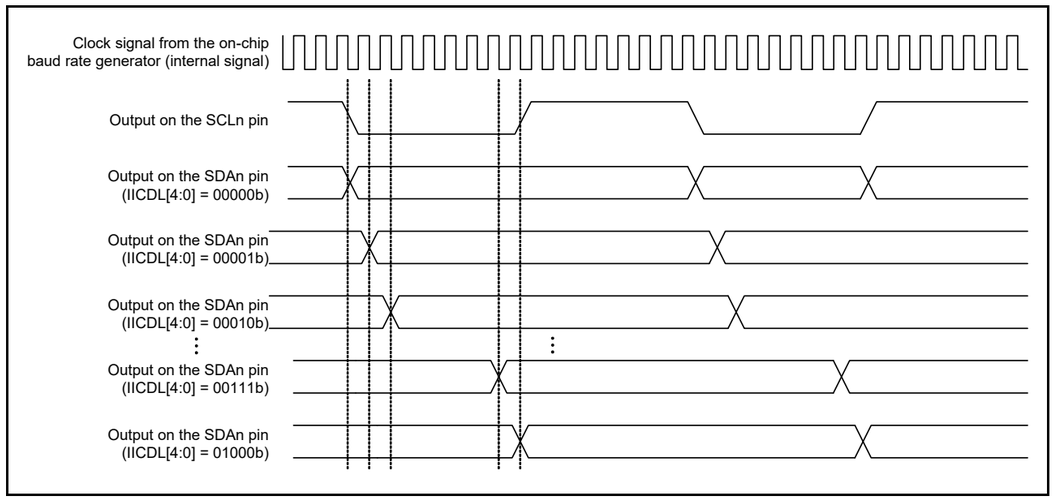


Figure 29.62 Timing of delays in SDAn output

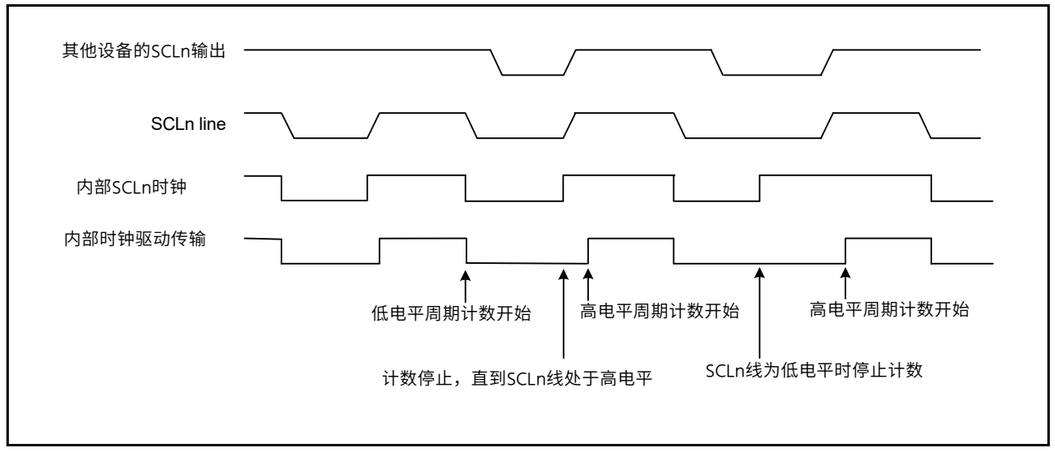


Figure 29.61 时钟同步的示例操作

29.7.3 SDA输出延迟

SIMR1中的IICDL[4:0]位可用于设置SDAn引脚输出相对于SCLn引脚输出下降沿的延迟。可选择从0到31的延迟设置。延迟设置表示来自片上波特率发生器的时钟信号的相关周期数的周期（通过将基本时钟PCLK除以在SMR寄存器）。SDAn引脚上的输出延迟适用于启动条件重启条件停止条件信号、8位发送数据和确认位。

如果SDAn输出延迟小于SCLn引脚电平下降所需的时间，则SDAn引脚上的输出变化会在SCLn引脚上的输出电平下降时开始，从而产生从机错误操作的可能性设备。确保SDAn引脚上的输出延迟设置指定的时间段大于SCLn引脚上的输出下降所需的时间（标准模式和快速模式下的IIC为300ns）。

图29.62显示了SDAn输出中的延迟时间。

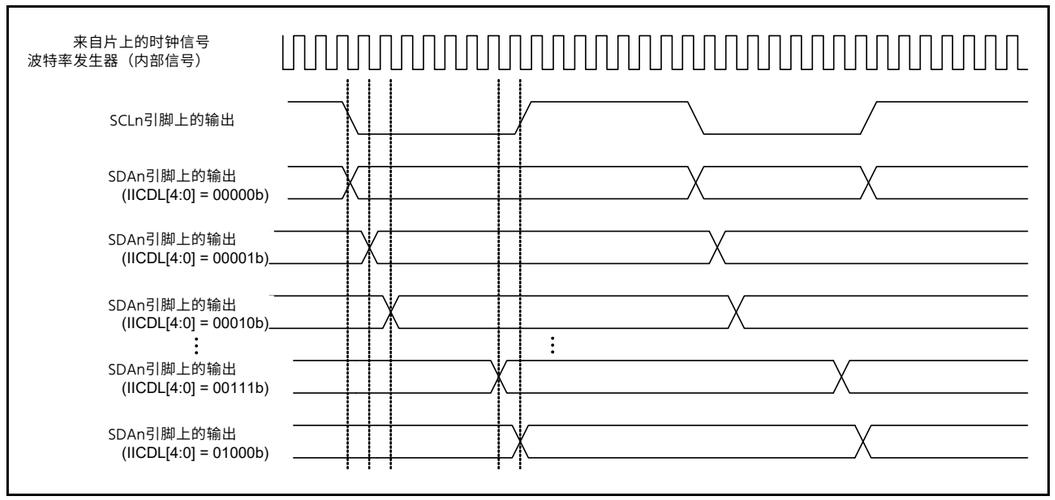


Figure 29.62 SDAn输出中的延迟时间

29.7.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value of 00h to SCR and initialize the interface as shown in the example in Figure 29.63.

Before making any changes to the operating mode or transfer format, be sure to set SCR to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

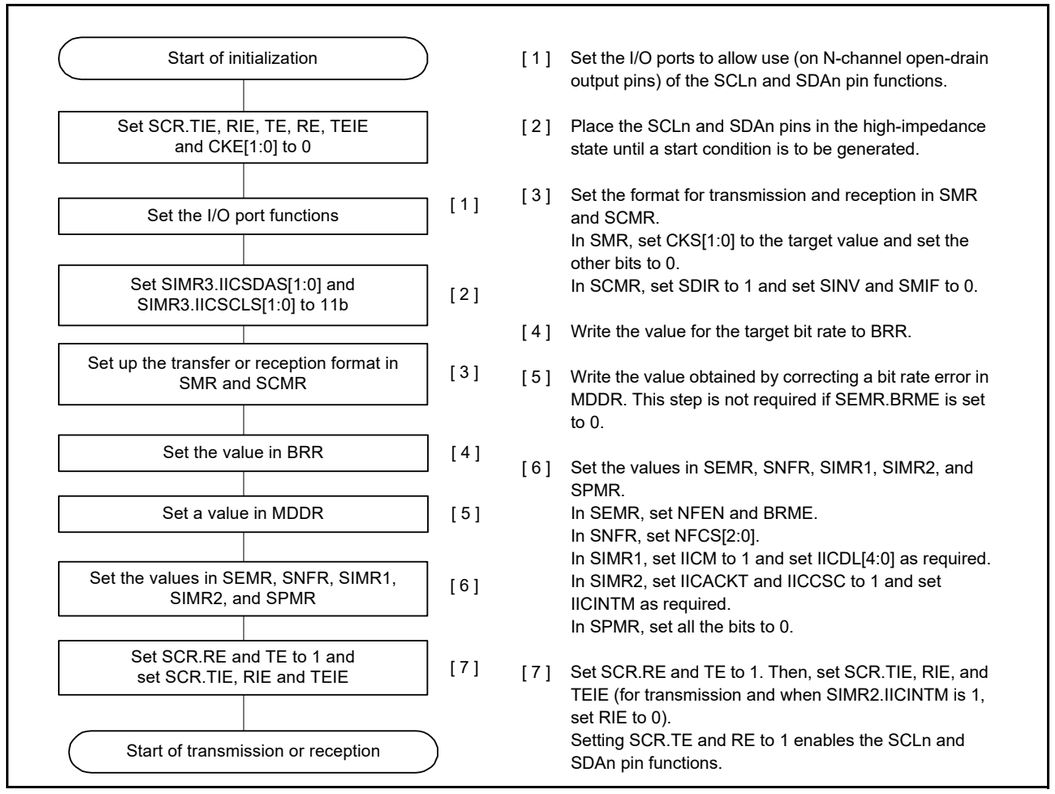


Figure 29.63 Example flow of SCI initialization in simple IIC mode

29.7.5 Operation in Master Transmission (Simple IIC Mode)

Figure 29.64 and Figure 29.65 show examples of master transmission and Figure 29.66 shows an example flow of data transmission. The value of the IICINTM bit in the SIMR2 register is assumed to be 1 (use reception and transmission interrupts) and the value of the RIE bit in the SCR register is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled). See Table 29.28 for more information on the STI interrupt.

When 10-bit slave addresses are used, steps [3] and [4] in Figure 29.66 are repeated twice.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the timing of generation of the SCIn_TXI interrupt request during clock synchronous transmission.

29.7.4 简单IIC模式下的SCI初始化

在传输数据之前，将初始值00h写入SCR并初始化接口，如示例中所示
Figure 29.63.

在对操作模式或传输格式进行任何更改之前，请务必将SCR设置为其初始值。在简单IIC模式下，通信端口的开漏设置应在端口侧进行。

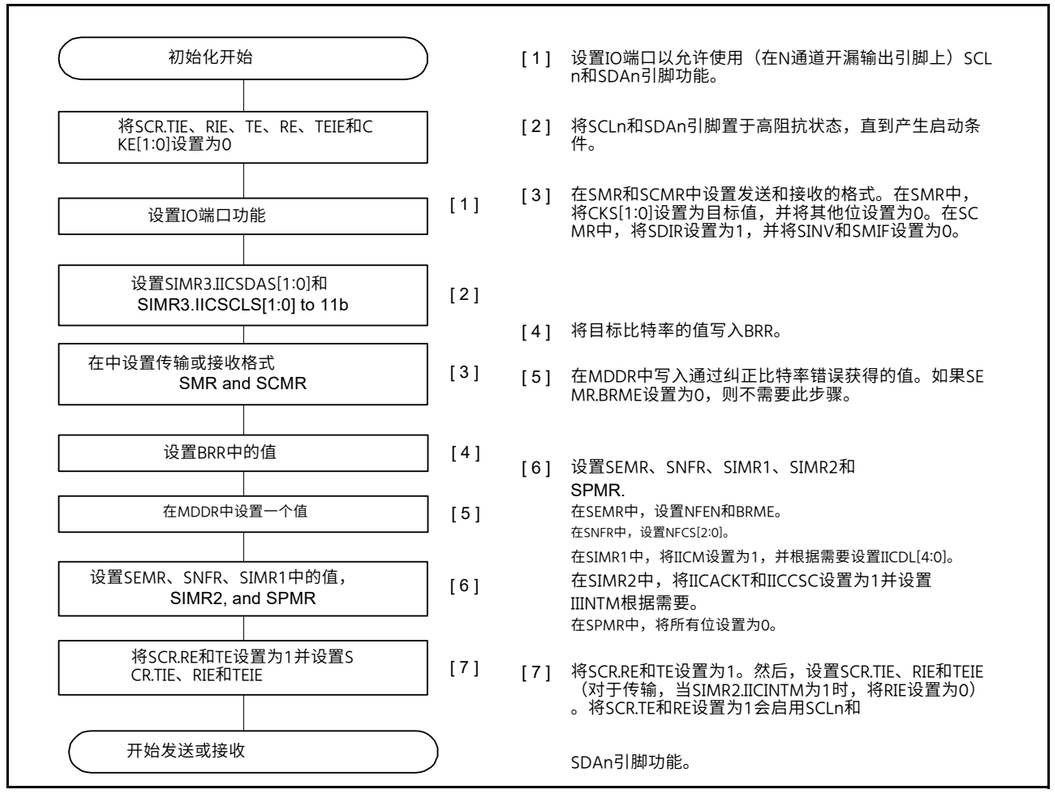


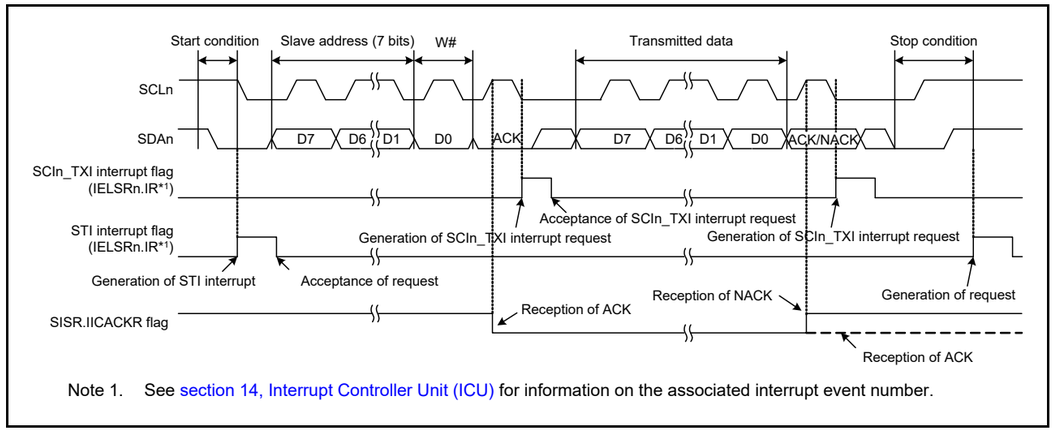
Figure 29.63 简单IIC模式下SCI初始化示例流程

29.7.5 主传输操作（简单IIC模式）

图29.64和图29.65显示了主机传输的示例，图29.66显示了数据传输的示例流程。SIMR2寄存器中的IICINTM位的值假定为1（使用接收和发送中断），SCR寄存器中的RIE位的值假定为0（禁止SCIn_RXI和SCIn_ERI中断请求）。有关STI中断的更多信息，请参见表29.28。

当使用10位从地址时，图29.66中的步骤[3]和[4]重复两次。

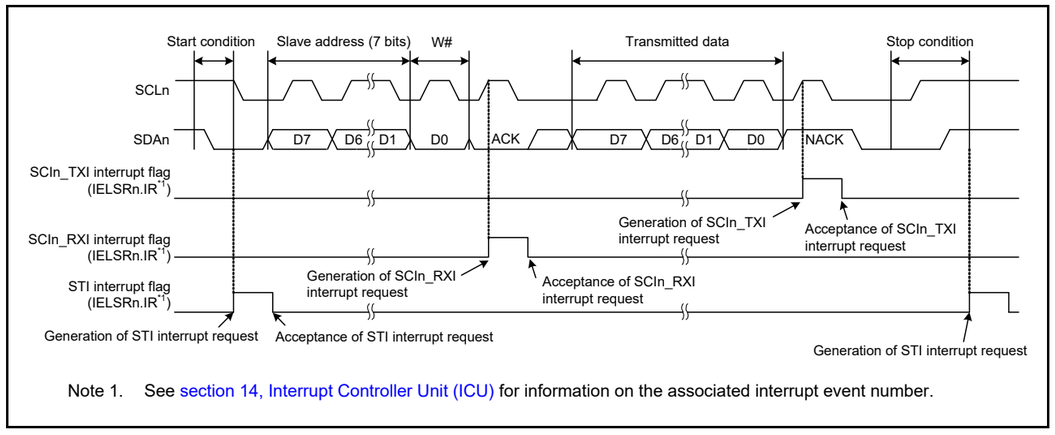
在简单IIC模式下，发送数据空中断(SCIn_TXI)在一帧通信完成时产生，与时钟同步传输期间产生SCIn_TXI中断请求的时序不同。



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

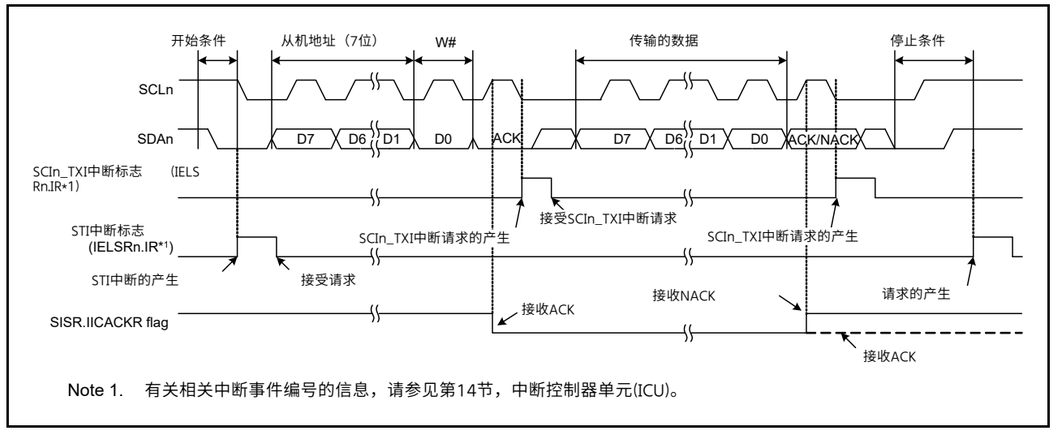
Figure 29.64 Example 1 operation for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the IICINTM bit in SIMR2 register is set to 0, using ACK/NACK interrupts during master transmission, the DMAC or DTC is activated by the ACK interrupt as the trigger and the required number of data bytes are transmitted. When a NACK is received, error processing, such as transmission stop and retransmission, is performed using the NACK interrupt as the trigger.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

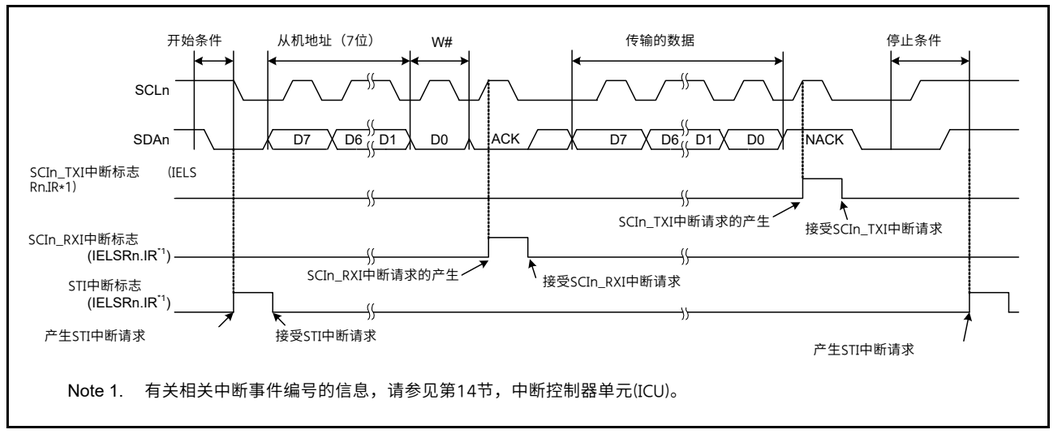
Figure 29.65 Example 2 operation for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.64 示例1简单IIC模式下的主机发送操作，具有7位从机地址、发送中断和接收中断

当SIMR2寄存器中的IICINTM位设置为0时，在主机传输期间使用ACKNACK中断，DMAC或DTC由ACK中断作为触发器激活，并发送所需的数据字节数。
接收到NACK时，使用
NACK中断作为触发。



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.65 示例2简单IIC模式下的主机传输操作，具有7位从机地址、ACK中断和NACK中断

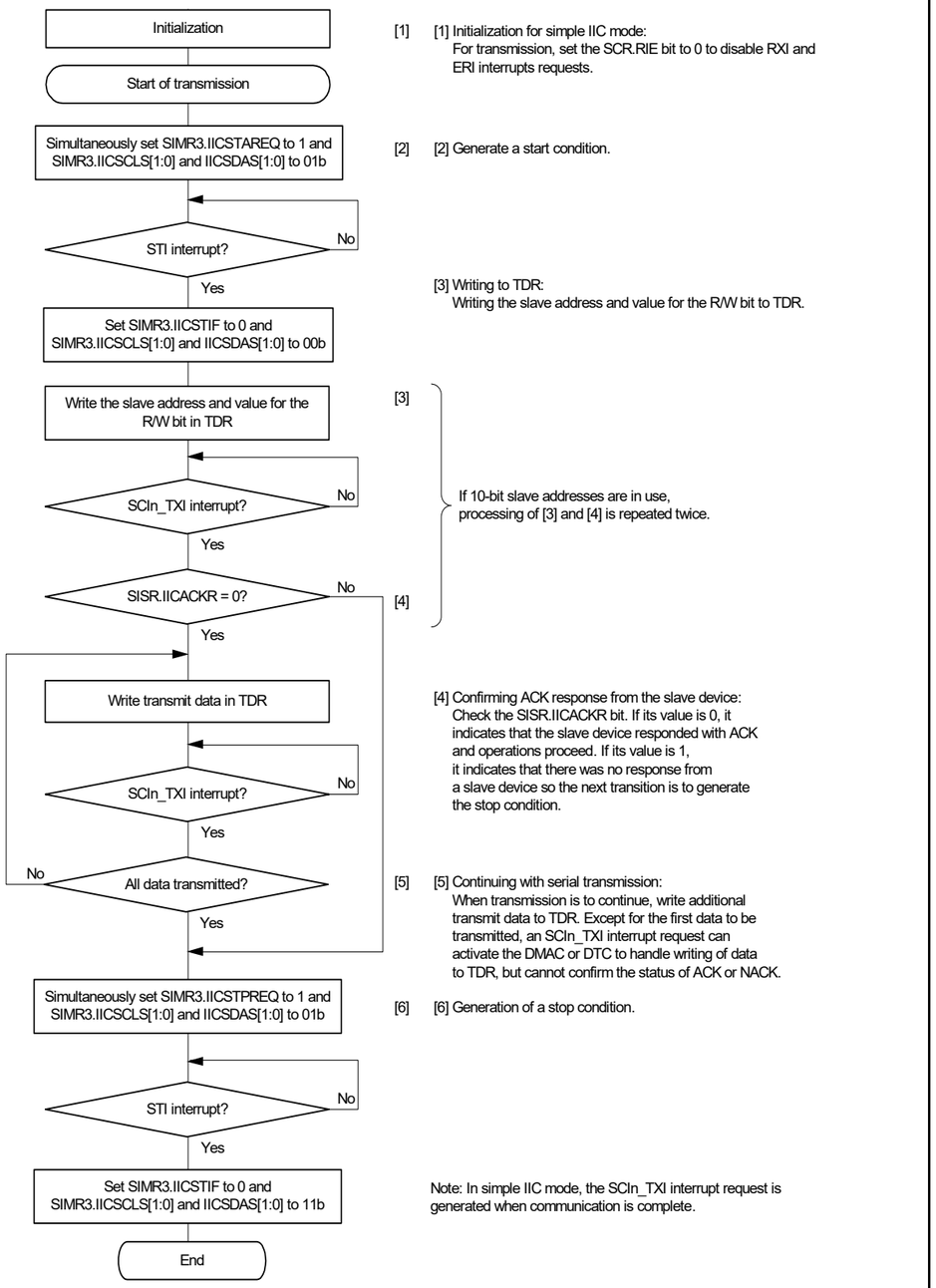


Figure 29.66 Example procedure for master transmission in simple IIC mode with transmission interrupts and reception interrupts

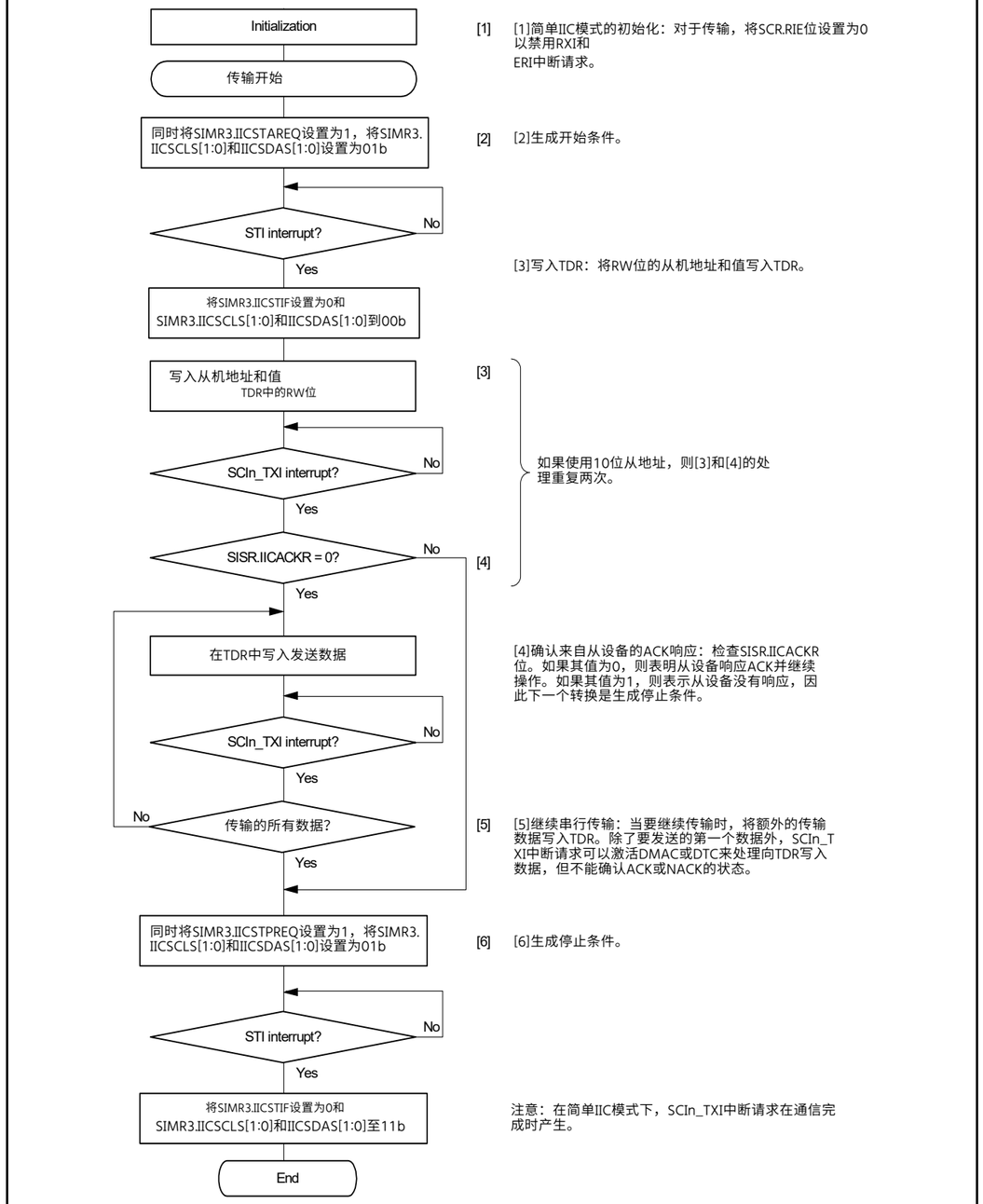


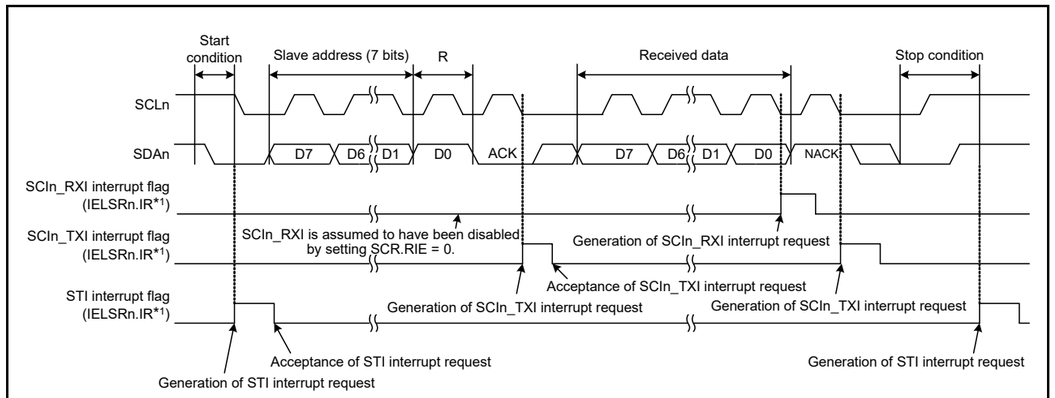
Figure 29.66 带有发送中断和接收中断的简单IIC模式下主机发送的示例程序

29.7.6 Master Reception in Simple IIC Mode

Figure 29.67 shows an example of master reception operation in simple IIC mode and Figure 29.68 shows an example flow of master reception.

The value of the IICINTM bit in SIMR2 register is assumed to be 1 using reception and transmission interrupts.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame completes, unlike the timing of the SCIn_TXI interrupt request generation during clock synchronous transmission.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the associated interrupt event number.

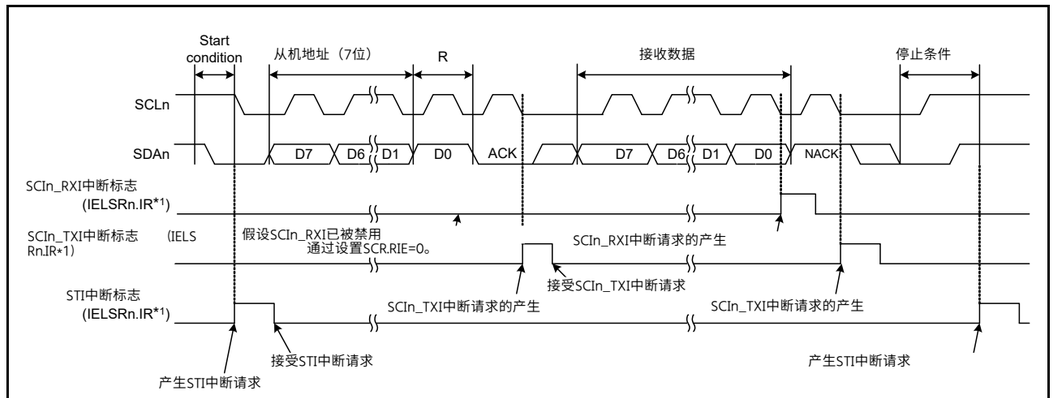
Figure 29.67 Example operation for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

29.7.6 简单IIC模式下的主接收

图29.67显示了简单IIC模式下的主机接收操作示例，图29.68显示了主机接收的示例流程。

SIMR2寄存器中IICINTM位的值假定为1使用接收和发送中断。

在简单IIC模式下，发送数据空中断(SCIn_TXI)在一帧通信完成时产生，与时钟同步传输期间SCIn_TXI中断请求产生的时序不同。



Note 1. 有关相关中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 29.67 简单IIC模式下主机接收的示例操作，具有7位从机地址、发送中断和接收中断

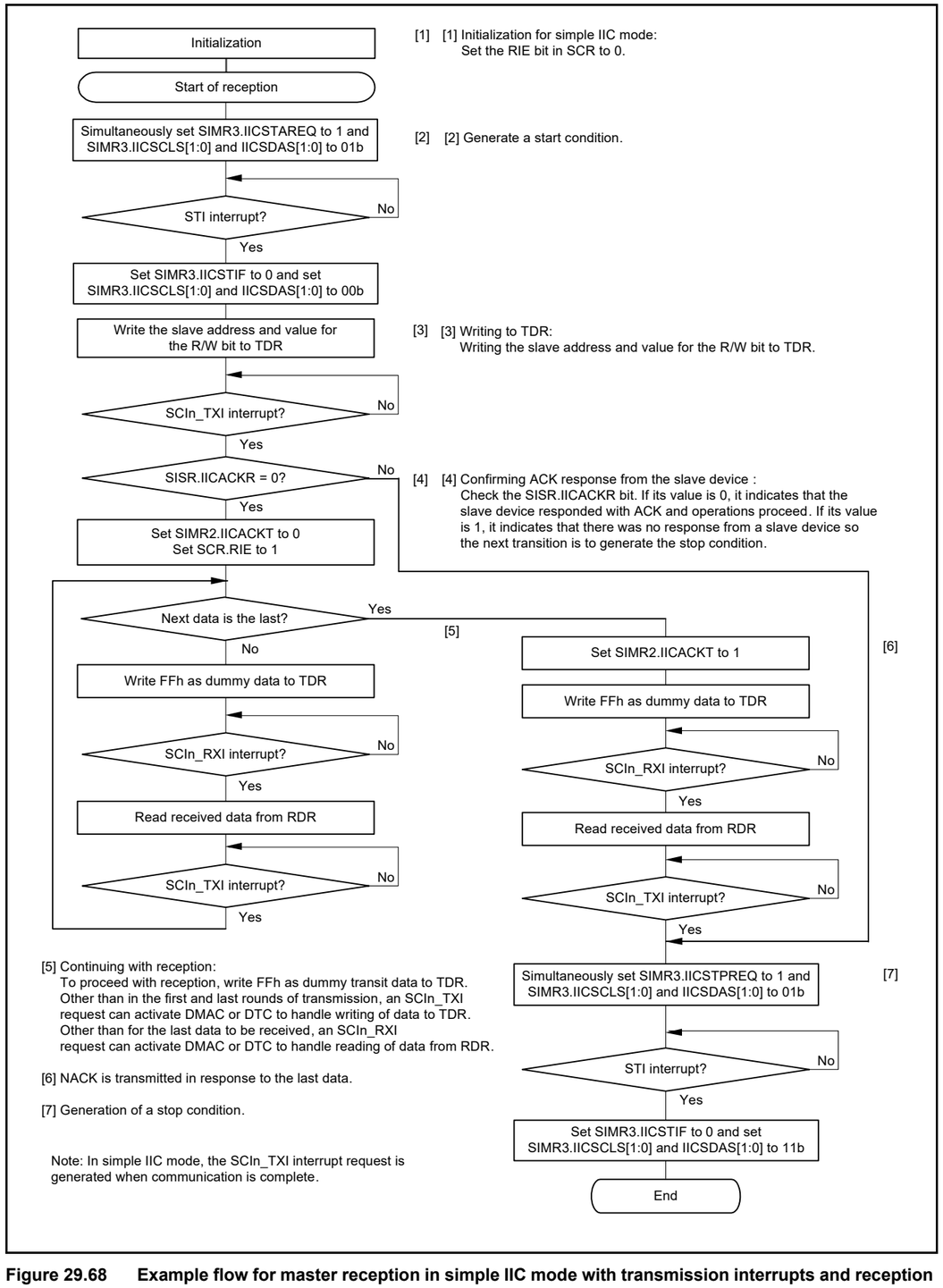


Figure 29.68 Example flow for master reception in simple IIC mode with transmission interrupts and reception interrupts

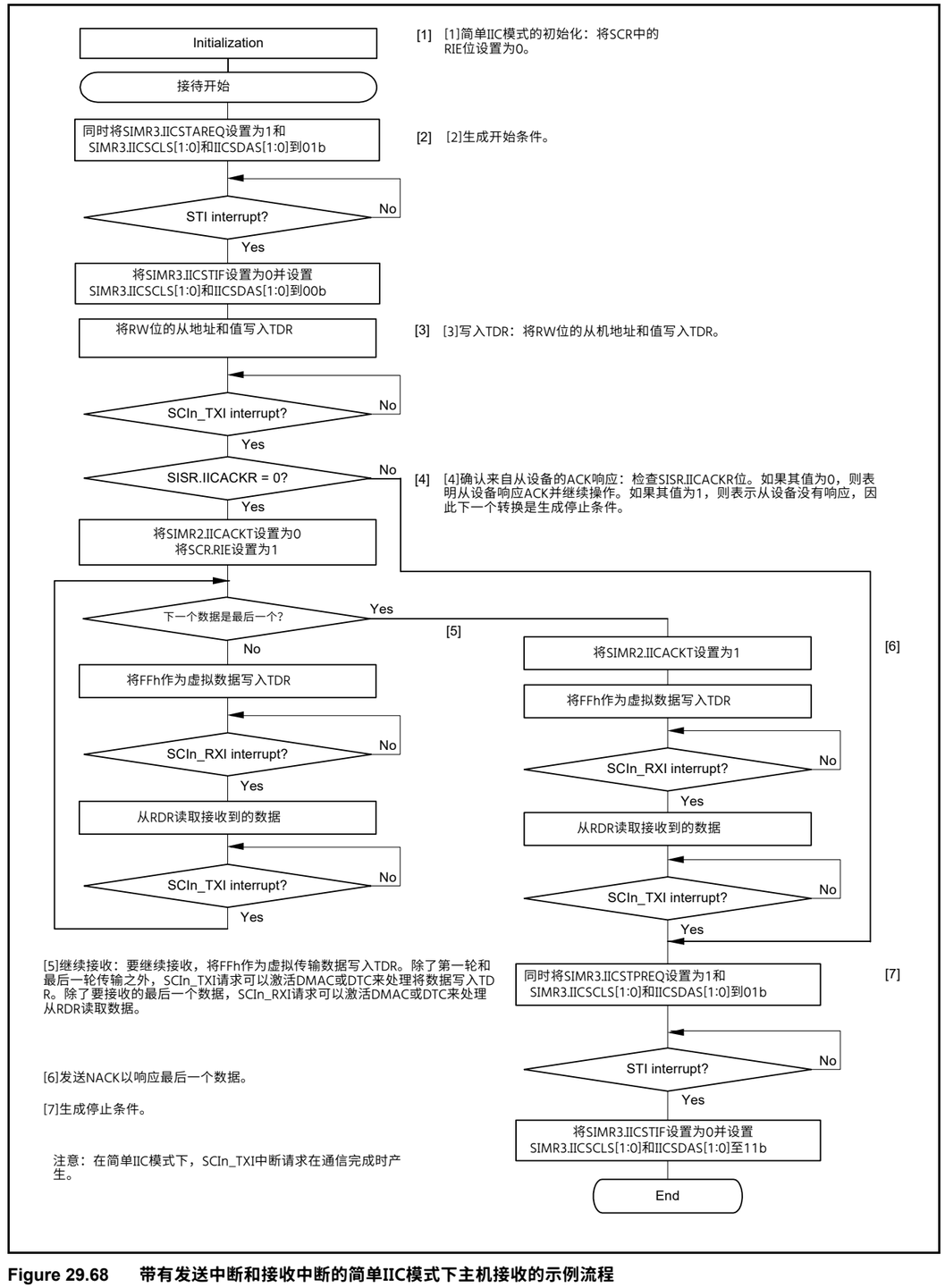


Figure 29.68 带有发送中断和接收中断的简单IIC模式下主机接收的示例流程

29.8 Operation in Simple SPI Mode

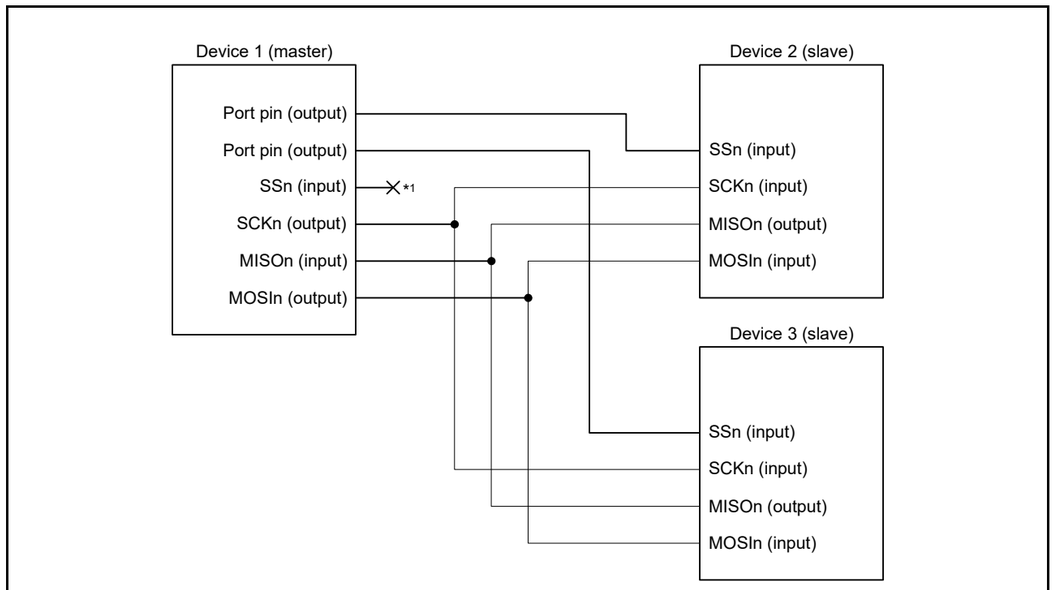
As an extended function, the SCI supports a simple SPI mode that handles transfer in one or multiple master devices and multiple slave devices.

To place the SCI in simple SPI mode, use the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) and set the SSE bit in SPMR register to 1. When the configuration only has a single master, the SSn pin function is not required to connect the device used as the master in simple SPI mode. Therefore, set the SSE bit in the SPMR register to 0.

Figure 29.69 shows an example of connections in simple SPI mode. Use a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of transfer data consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the SINV bit in SCMR to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a common clock signal. Additionally, because both the transmitter and receiver have a buffered structure, it is possible to both write the next transmit data while transmission is in progress and read previously received data while reception is in progress. This enables continuous transfer.



Note 1. The SSn input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 29.69 Example connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

29.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1).

Table 29.24 lists the relationship between the pin states, mode, and the input level on the SSn pin.

29.8 简单SPI模式下的操作

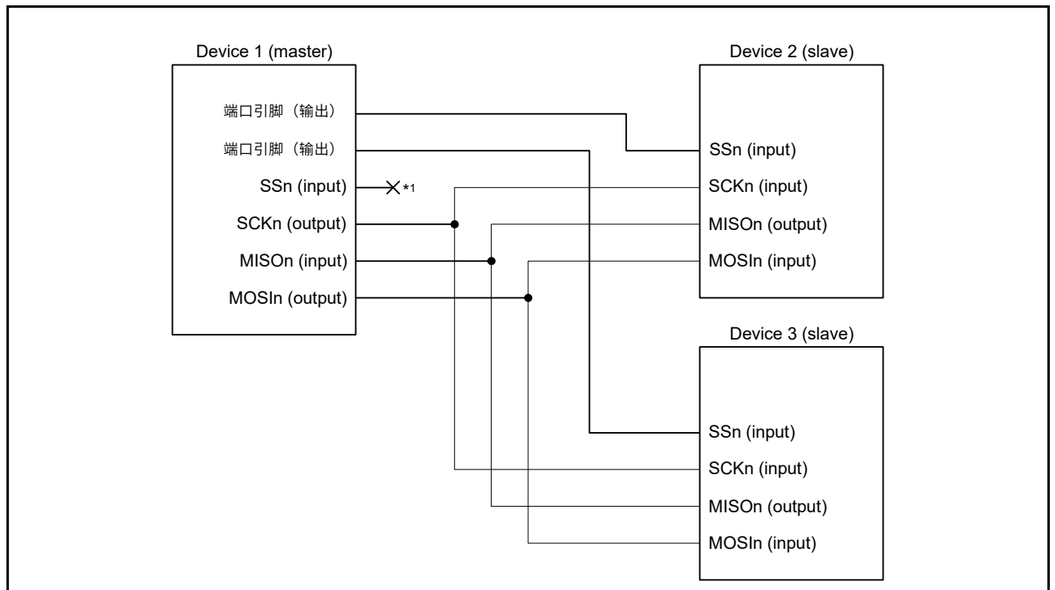
作为一项扩展功能，SCI支持简单的SPI模式，可处理一个或多个主设备和多个从设备中的传输。

要将SCI置于简单SPI模式，请使用时钟同步模式的设置（SCMR.SMIF=0，SIMR1.IICM=0，SMR.CM=1）并将SPMR寄存器中的SSE位设置为1。当仅配置单主控，在简单SPI模式下连接作为主控的设备不需要SSn引脚功能。因此，将SPMR寄存器中的SSE位设置为0。

图29.69显示了简单SPI模式下的连接示例。使用通用端口引脚从主机产生SSn输出信号。

在简单SPI模式下，数据与时钟脉冲同步传输，方式与时钟同步模式相同。1个字符的传输数据由8位数据组成，不能附加奇偶校验位。可以通过将SCMR中的SINV位设置为1来反转数据。

由于接收器和发送器在SCI模块中相互独立，因此可以使用公共时钟信号进行全双工通信。此外，由于发送器和接收器都具有缓冲结构，因此可以在发送过程中写入下一个发送数据，并在接收过程中读取先前接收到的数据。这使得连续传输成为可能。



Note 1. 在单主机系统中不需要SSn输入（接口与设置SPMR.SSE=0一起使用）。

Figure 29.69 在SPMR.SSE位=0的单主模式下使用简单SPI模式的示例连接

29.8.1 主从模式下的引脚状态

简单SPI模式接口的引脚方向（输入或输出）根据设备是主设备（SCR.CKE[1:0]=00b或01b且SPMR.MSS=0）还是从设备（SCR.CKE）而不同[1:0]=10b或11b且SPMR.MSS=1)。

表29.24列出了SSn引脚上引脚状态、模式和输入电平之间的关系。

Table 29.24 Pin states by mode and input level on SSn pin

Mode	Input on SSn pin	State of TXDn pin	State of RXDn pin	State of SCKn pin
Master mode*1	High (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin. Because the SSn pin function is not required, the pin is available for other purposes.
Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE and RE bits = 00b) in a multi-master configuration (SPMR.SSE = 1).

29.8.2 SS Function in Master Mode

Setting the SCR.CKE[1:0] bits to 00b and the SPMR.MSS bit to 0 selects master operation. The SSn pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and a transmission or reception is in progress. The MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. In addition, the value of the MFF bit in SPMR is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading the MFF flag in SPMR. If a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn outputs are in the high-impedance state after the completion of the transfer. Use a general port pin to produce the SS output signal from the master.

29.8.3 SS Function in Slave Mode

Setting the SCR.CKE[1:0] bits to 10b and the SPMR.MSS bit to 1 selects slave operation. When the level on the SSn pin is high, the MISOn output pin is in a high-impedance state and clock input through the SCKn pin is ignored. When the level on the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high level during transmission or reception, the MISOn output pin is placed in a high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the current transmitted or received character is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, or SCIn_TEI) is then generated.

29.8.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in SPMR can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 29.70. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

Table 29.24 SSn引脚上的模式和输入电平的引脚状态

Mode	SSn引脚上的输入	TXDn引脚状态	RXDn引脚状态	SCKn引脚状态
Master mode*1	高（转移可以继续）	数据传输输出*2	接收数据的输入	Clock output*3
	低（转移无法进行）	High-impedance	接收数据的输入（但禁用）	High-impedance
从机模式	高（传输无法进行）	接收数据的输入（但禁用）	High-impedance	时钟输入（但禁用）
	低（转移可以继续）	接收数据的输入	数据传输输出	时钟输入

Note 1. 当只有一个主机(SPMR.SSE=0)时，无论SSn引脚上的输入电平如何，都可以进行传输。这相当于在SSn引脚上输入高电平。由于不需要SSn引脚功能，因此该引脚可用于其他用途。
Note 2. 当串行传输被禁用（SCR.TE位=0）时，MOSIn引脚输出处于高阻抗状态。
Note 3. 在多主机配置（SPMR.SSE=1）中禁用串行传输（SCR.TE和RE位=00b）时，SCKn引脚输出处于高阻抗状态。

29.8.2 主控模式下的SS功能

将SCR.CKE[1:0]位设置为00b并将SPMR.MSS位设置为0选择主机操作。SSn引脚不用于单主机配置(SPMR.SSE=0)，因此无论SSn引脚的值如何，都可以进行发送或接收。

在多主机配置（SPMR.SSE=1）中，当SSn引脚上的电平为高电平时，主机设备在开始发送或接收之前从SCKn引脚输出时钟信号，以指示没有其他主机或另一个主机在进行接收或发送。

在多主机配置中，当SSn引脚上的电平为低电平时，存在其他主机，并且正在进行发送或接收。MOSIn输出和SCKn引脚处于高阻状态，无法开始发送或接收。此外，SPMR中MFF位的值为1，表示模式故障错误。在多主机配置中，通过读取SPMR中的MFF标志开始错误处理。如果在发送或接收过程中发生模式故障错误，则发送或接收不会停止，但MOSIn和SCKn输出在传输完成后处于高阻抗状态。使用通用端口引脚从主机产生SS输出信号。

29.8.3 从模式下的SS功能

将SCR.CKE[1:0]位设置为10b并将SPMR.MSS位设置为1选择从机操作。当SSn引脚上的电平为高电平时，MISOn输出引脚处于高阻抗状态，并且通过SCKn引脚输入的时钟被忽略。当SSn引脚为低电平时，通过SCKn引脚输入的时钟有效，可以进行发送或接收。

如果SSn引脚上的输入在发送或接收过程中从低电平变为高电平，则MISOn输出引脚处于高阻抗状态。同时，发送或接收的内部处理以通过SCKn引脚输入的时钟速率继续，直到对当前发送或接收字符的处理完成，之后它停止，并且适当的中断（SCIn_TXI、SCIn_RXI或SCIn_TEI）然后生成。

29.8.4 时钟与发送接收数据的关系

SPMR中的CKPOL和CKPH位可用于以四种不同的方式设置用于发送和接收的时钟。时钟信号与数据收发的关系如图29.70所示。主从操作的关系是相同的。这与SSn引脚上的电平为高电平时相同。

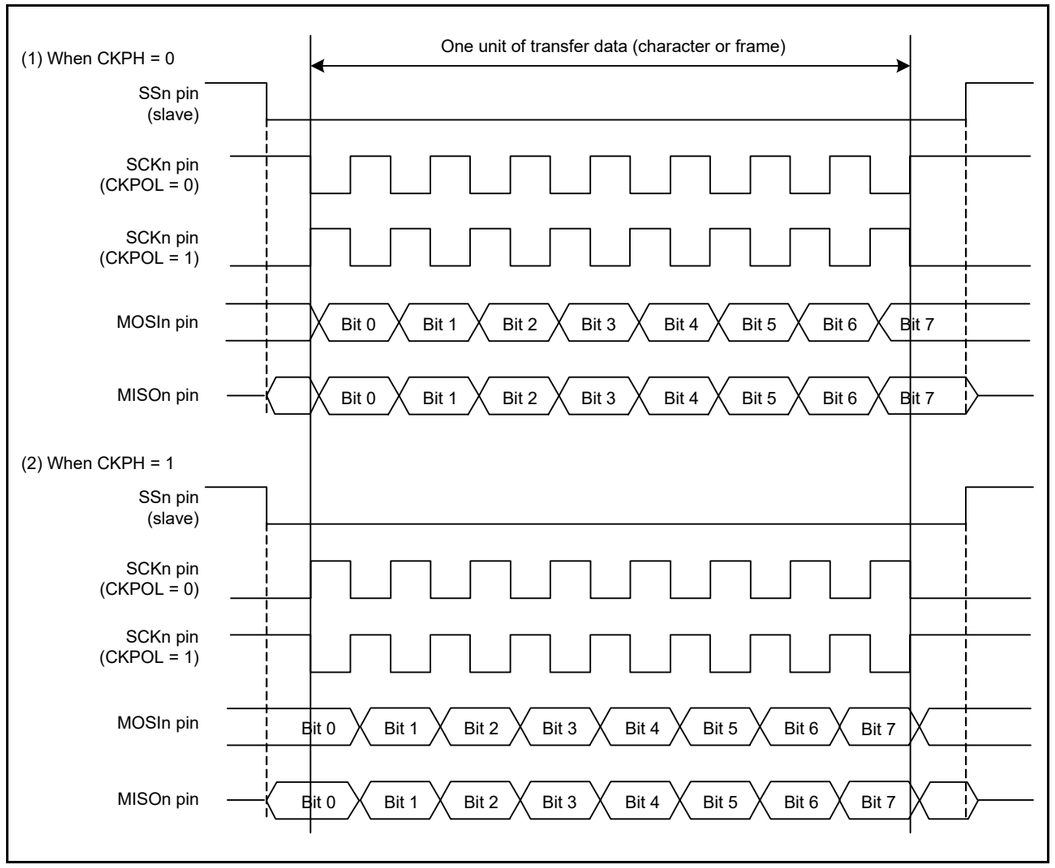


Figure 29.70 Relation between clock signal and transmit or receive data in simple SPI mode

29.8.5 SCI Initialization in Simple SPI Mode

SCI initialization in simple SPI mode is the same as in clock synchronous mode. See Figure 29.32 for an example of initialization flow. The CKPOL and CKPH bits in SPMR must be set to ensure that the selected clock signal configuration is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note: Only the SCR.RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.

Changing the value of the TE bit in the SCR register from 1 to 0 or from 0 to 1 when the TIE bit in the SCR register is 1 at the same time, leads to the generation of a transmit data empty interrupt (SCIn_TXI).

29.8.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at a low level before starting the transfer and at a high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

29.9 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in MDDR when PCLK is selected with the CKS[1:0] bits in SMR/SMR_SMCI.

Figure 29.71 shows an example where PCLK is selected in the CKS[1:0] bits in SMR/SMR_SMCI and BRR and MDDR

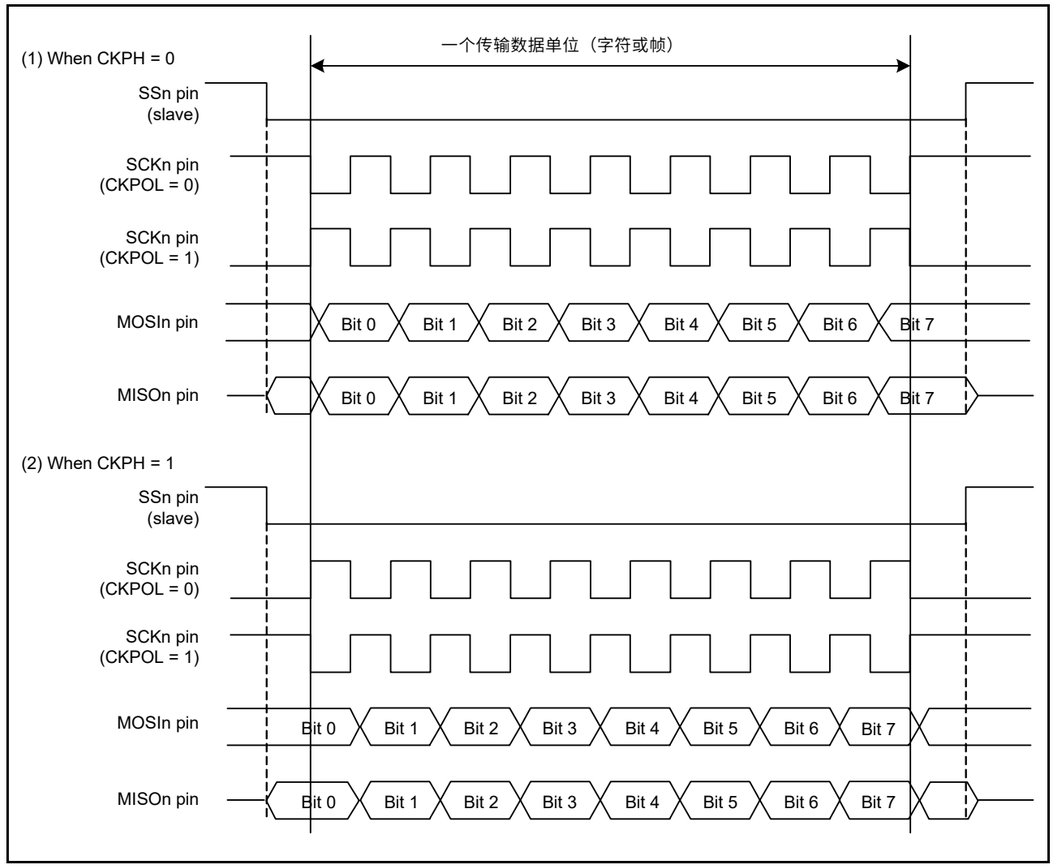


Figure 29.70 简单SPI模式下时钟信号与发送或接收数据的关系

29.8.5 简单SPI模式下的SCI初始化

简单SPI模式下的SCI初始化与时钟同步模式下相同。有关初始化流程的示例，请参见图29.32。必须设置SPMR中的CKPOL和CKPH位，以确保所选时钟信号配置适用于主器件和从器件。

在对操作模式或传输格式进行任何更改之前，始终初始化SCR寄存器。

Note: 只有SCR.RE位设置为0。SSR.ORER、FER、PER和RDR标志未初始化。

当SCR寄存器中的TIE位同时为1时，将SCR寄存器中的TE位的值从1更改为0或从0更改为1，会导致产生发送数据空中断（SCIn_TXI）。

29.8.6 简单SPI模式下串行数据的发送和接收

在主机操作中，确保传输另一侧的从设备的SSn引脚在开始传输之前为低电平，在传输完成时为高电平。否则，过程与时钟同步模式相同。

29.9 比特率调制功能

使用比特率调制功能，当
PCLK由SMRSMR_SMCI中的CKS[1:0]位选择。

图29.71显示了在SMRSMR_SMCI和BRR和MDDR的CKS[1:0]位中选择PCLK的示例

are set to 0 and 160 respectively, in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias and expansion. Contraction is generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

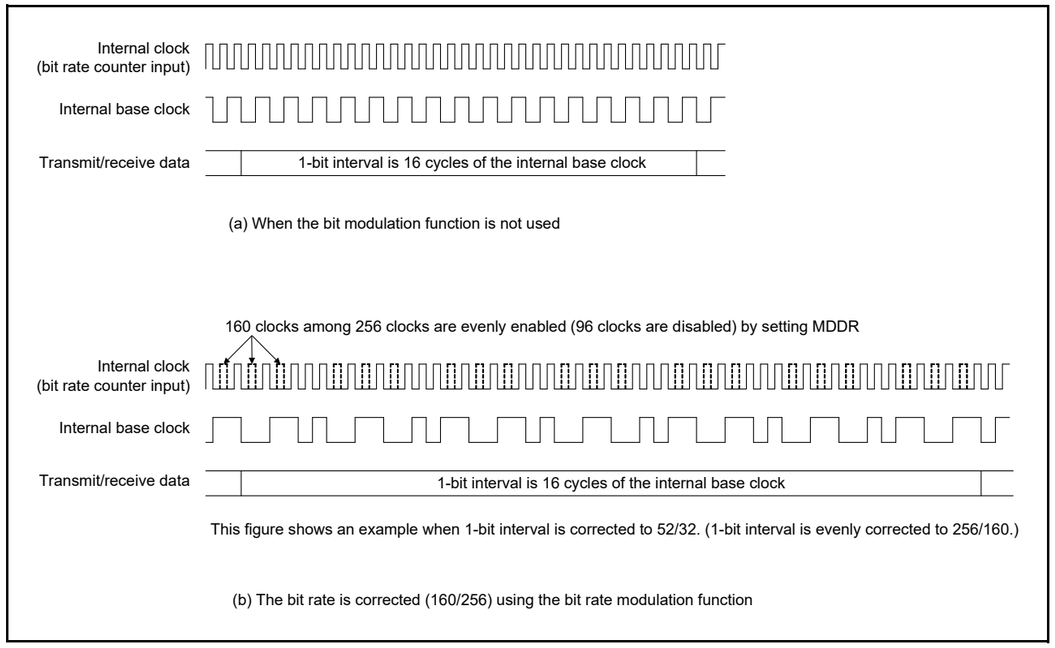


Figure 29.71 Example internal base clock using bit rate modulation function

29.10 Interrupt Sources

29.10.1 Buffer Operations for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the ICU is 1, the ICU does not output the interrupt request but saves it internally with a capacity for retention of one request per source.

When the value of the interrupt status flag in the ICU becomes 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

29.10.2 Buffer Operations for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected)

When an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the ICU is set to 0, and if the conditions for an SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

29.10.3 Interrupts in Asynchronous, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

Table 29.25 lists interrupt sources in asynchronous mode, clock synchronous mode, and simple SPI mode. A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in SCR.

在异步模式下分别设置为0和160。在这个例子中，基本时钟的周期被均匀地校正（256160）并且比特率也被校正（160256）。

Note: 启用内部时钟会导致偏差和扩展。内部基准时钟的脉冲宽度产生收缩。

不要在时钟同步模式和简单SPI模式的最高速度设置（SMR.CKS[1:0]=00b，SCR.CKE[1]=0和BRR=0）中使用此功能。

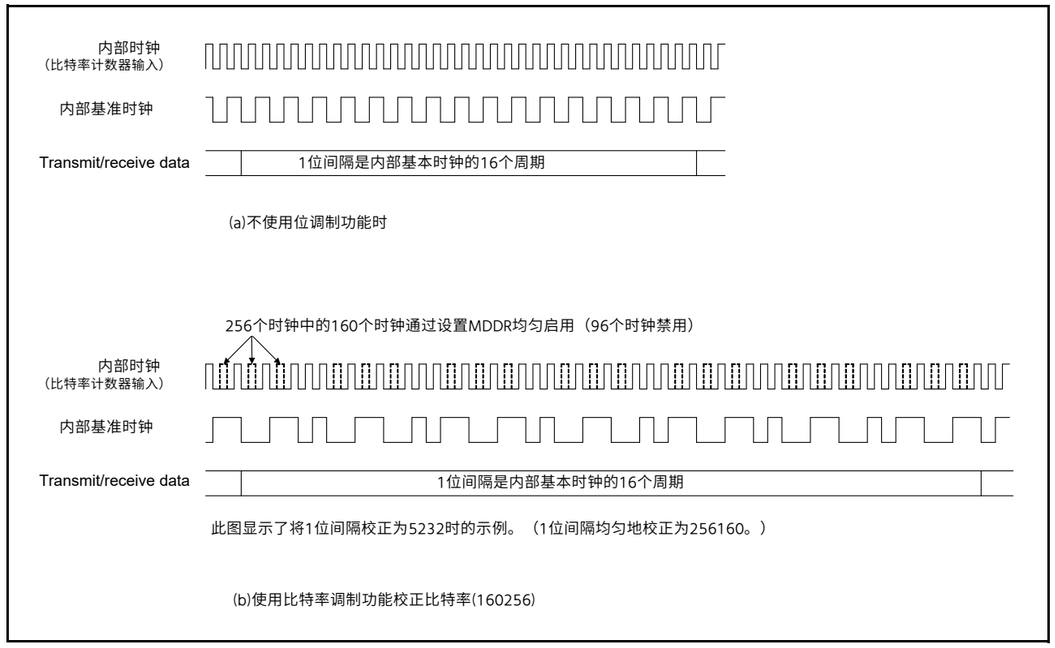


Figure 29.71 使用比特率调制功能的示例内部基本时钟

29.10 中断源

29.10.1 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择非FIFO）

如果在ICU中的中断状态标志为1时满足SCIn_TXI和SCIn_RXI中断的条件，则ICU不输出中断请求，而是将其保存在内部，每个源可以保留一个请求。

当ICU中的中断状态标志的值变为0时，输出ICU中保留的中断请求。
当实际中断输出时，内部保留的中断请求会被自动丢弃。清除相关中断使能位（SCRSCR_SMCI中的TIE或RIE位）也可用于丢弃内部保留的中断请求。

29.10.2 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择FIFO）

当ICU中的中断状态标志设置为1时，SCIn_TXI和SCIn_RXI中断不会向ICU输出中断请求。当ICU的中断状态标志设置为0，并且满足SCIn_TXI和SCIn_RXI中断的条件时，将产生中断请求。

29.10.3 异步、时钟同步和简单SPI模式下的中断

(1) Non-FIFO selected

表29.25列出了异步模式、时钟同步模式和简单SPI模式下的中断源。可以为每个中断源分配不同的中断向量。可以使用SCR中的启用位启用或禁用各个中断源。

If the TIE bit in SCR register is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from TDR or TDRHL*1 to the TSR. An SCIn_TXI interrupt request can also be generated using a single instruction to set the TE and TIE bits to 1 in the SCR simultaneously. An SCIn_TXI interrupt request can activate the DMAC or DTC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting TE to 1 when the TIE bit is 0 or by setting TIE to 1 when TE is 1*2 in the SCR register.

When new data is not written by the time of transmission of the last bit of the current transmit data and the TEIE bit is 1 in SCR, the TEND flag in SSR becomes 1 and an SCIn_TEI interrupt request is generated. Additionally, when the TE bit is 1 in SCR, the TEND flag in SSR saves the value 1 until more transmit data are written to the TDR or TDRHL*1, and setting the TEIE bit in SCR to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL*1 leads to clearing of the TEND flag in SSR and, after a certain time, discarding of the SCIn_TEI interrupt request.

If RIE is 1 in SCR, an SCIn_RXI interrupt request is generated when received data is stored in RDR. An SCIn_RXI interrupt request can activate the DMAC or DTC to handle data transfer.

Setting any of the ORER, FER, and PER flags in SSR to 1 when the RIE bit in SCR is 1 leads to the generation of an SCIn_ERI interrupt request. An SCIn_RXI interrupt request is not generated at this time. Clearing all three flags (ORER, FER, and PER) leads to discarding of the SCIn_ERI interrupt request.

(2) FIFO selected

Table 29.26 lists interrupt sources in FIFO selected mode.

If the TIE bit in the SCR register is 1, an SCIn_TXI interrupt request is generated when the amount of stored data in the FTDRL register is equal to or less than the threshold value indicated in the TTRG bit in FCR register. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the TE and TIE bits in SCR to 1 simultaneously.

An SCIn_TXI interrupt request is not generated by setting the TE bit in the SCR register to 1 when TIE bit in the SCR register is 0 or by setting TIE to 1 when TE is 1.

If the TEIE bit in SCR register is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmission data is sent, the TEND flag in SSR_FIFO register is set to 1 and the SCIn_TEI interrupt request is generated.

If the RIE bit in the SCR register is 1, an SCIn_RXI interrupt request is generated when the amount of stored data in the FRDRL becomes equal to or greater than the threshold value indicated in the RTRG bit in the FCR register. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the RIE bit in the SCR register is 1, when the ORER flag in the SSR_FIFO register is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, an SCIn_ERI interrupt request is generated. When the amount of data stored in the FRDRL register is at the threshold value or above, an SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case the ORER, FER, and PER flags in the SSR_FIFO register are all cleared.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt using the Interrupt Request Enable bit in the ICU rather than using the TIE bit in the SCR register. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.

Table 29.25 SCI interrupt sources with non-FIFO selected (1 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible	Possible
	Address match	DCMF	RIE	Possible	Possible

如果SCR寄存器中的TIE位为1，当发送数据从TDR或TDRHL*1到TSR。也可以使用一条指令生成SCIn_TXI中断请求来设置SCR中的TE和TIE位同时为1。SCIn_TXI中断请求可以激活DMAC或DTC来处理数据传输。

当TIE位为0时将TE设置为1，或者当SCR寄存器中的TE为1*2时将TIE设置为1，不会产生SCIn_TXI中断请求。

当当前发送数据的最后一位发送时没有写入新数据且SCR中的TEIE位为1时，SSR中的TEND标志变为1，并产生SCIn_TEI中断请求。此外，当SCR中的TE位为1时，SSR中的TEND标志保存值1，直到有更多发送数据写入TDR或TDRHL*1，并且将SCR中的TEIE位设置为1会导致产生SCIn_TEI中断请求。

将数据写入TDR或TDRHL*1会导致SSR中的TEND标志清零，并在一定时间后丢弃SCIn_TEI中断请求。

如果SCR中的RIE为1，则当接收到的数据存储在RDR中时会产生SCIn_RXI中断请求。SCIn_RXI中断请求可以激活DMAC或DTC来处理数据传输。

当SCR中的RIE位为1时，将SSR中的任何ORER、FER和PER标志设置为1会导致生成SCIn_ERI中断请求。此时不产生SCIn_RXI中断请求。清除所有三个标志（ORER、FER和PER）导致丢弃SCIn_ERI中断请求。

(2) FIFO selected

表29.26列出了FIFO选择模式下的中断源。

如果SCR寄存器中的TIE位为1，当存储器中存储的数据量达到FTDRL寄存器等于或小于FCR寄存器中TTRG位指示的阈值。SCIn_TXI中断请求也可以通过使用一条指令同时将SCR中的TE和TIE位设置为1来产生。

当SCR寄存器的TIE位为0时将SCR寄存器的TE位设置为1，或者当TE为1时将TIE设置为1，不会产生SCIn_TXI中断请求。

如果SCR寄存器中的TEIE位为1，并且如果在发送数据的最后一位时下一个数据没有写入FTDRL寄存器，则SSR_FIFO寄存器中的TEND标志设置为1，并且SCIn_TEI中断请求为生成。

如果SCR寄存器中的RIE位为1，则当FRDRL中存储的数据量等于或大于FCR寄存器中RTRG位指示的阈值时，将产生SCIn_RXI中断请求。当RTRG为0时，即使接收FIFO中的数据量等于0，也不会发生SCIn_RXI中断。

如果SCR寄存器中的RIE位为1，当SSR_FIFO寄存器中的ORER标志设置为1或帧错误或奇偶校验错误的数据存储在FRDRL寄存器中时，将产生SCIn_ERI中断请求。当FRDRL寄存器中存储的数据量在阈值或以上时，也会产生SCIn_RXI中断请求。SCIn_ERI中断请求可以取消，此时SSR_FIFO寄存器中的ORER、FER和PER标志全部清零。

注意1.选择异步模式和9位数据长度时。
注2.当要开始新一轮传输时，为了在传输最后一个数据时暂时禁止SCIn_TXI中断，在处理完传输完成的中断后，使用ICU中的中断请求使能位控制中断的激活，而不是而不是使用SCR寄存器中的TIE位。这种方法可以防止在传输新数据时抑制SCIn_TXI中断请求。

Table 29.25 选择了非FIFO的SCI中断源（2个中的1个）

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER、FER、PER、DFER, DPER	RIE	不可能	不可能
SCIn_RXI	接收数据已满	RDRF	RIE	Possible	Possible
	地址匹配	DCMF	RIE	Possible	Possible

Table 29.25 SCI interrupt sources with non-FIFO selected (2 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_AM	Address match	DCMF	—	Possible	Possible
SCIn_TXI	Transmit data empty	TDRE	TIE	Possible	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI modes.

Table 29.26 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible	Not possible
		DR (when FCR.DRES = 1)	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDF	RIE	Possible	Possible
	Receive data ready	DR (when FCR.DRES = 0)	RIE	Possible	Possible
	Address match	DCMF	RIE	Possible	Possible
SCIn_AM	Address match	DCMF	—	Possible	Possible
SCIn_TXI	Transmit data empty	TDFE	TIE	Possible	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI modes.

29.10.4 Interrupts in Smart Card Interface Mode

Table 29.27 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 29.27 SCI interrupt sources in smart card interface mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error or error signal detection	ORER, FER, ERS	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible	Possible
SCIn_TXI	Transmit end	TEND	TIE	Possible	Possible

Data transmission or reception using the DMAC or DTC is also possible in smart card interface mode. In transmission, when the TEND flag in SSR_SMCI is set to 1, an SCIn_TXI interrupt request is generated. The SCIn_TXI interrupt request activates the DMAC or DTC allowing transfer of transmit data if the SCIn_TXI request is specified beforehand as a source of DMAC or DTC activation. The TEND flag is automatically set to 0 when the DMAC or DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DMAC or DTC is not activated. Therefore, the SCI and DMAC or DTC automatically transmit the specified number of bytes, including retransmission when errors occur. However, the ERS flag in SSR_SMCI is not automatically set to 0 at error occurrence. Therefore, the ERS flag must be cleared by setting the RIE bit in SCR_SMCI to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DMAC or DTC, be sure to enable the DMAC or DTC before setting the SCI. For DMAC or DTC settings, see section 17, DMA Controller (DMAC) and section 18, Data Transfer Controller (DTC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to RDR. This SCIn_RXI interrupt request activates the DMAC or DTC allowing transfer of receive data if the SCIn_RXI request is specified as a source of DMAC or DTC activation. If an error occurs, the error flag is set. Therefore, the DMAC or DTC is not activated and an

Table 29.25 选择非FIFO的SCI中断源（2个中的2个）

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_AM	地址匹配	DCMF	—	Possible	Possible
SCIn_TXI	传输数据为空	TDRE	TIE	Possible	Possible
SCIn_TEI	发射端	TEND	TEIE	不可能	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

Table 29.26 选择了FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER、FER、PER、DFER, DPER	RIE	不可能	不可能
		DR (when FCR.DRES = 1)	RIE	不可能	不可能
SCIn_RXI	接收数据已满	RDF	RIE	Possible	Possible
	接收数据就绪	DR (when FCR.DRES = 0)	RIE	Possible	Possible
	地址匹配	DCMF	RIE	Possible	Possible
SCIn_AM	地址匹配	DCMF	—	Possible	Possible
SCIn_TXI	传输数据为空	TDFE	TIE	Possible	Possible
SCIn_TEI	发射端	TEND	TEIE	不可能	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

29.10.4 智能卡接口模式中的中断

表29.27列出了智能卡接口模式下的中断源。在此模式下不能使用发送结束中断(SCIn_TEI)请求和地址匹配(SCIn_AM)请求。

Table 29.27 智能卡接口模式下的SCI中断源

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_ERI	接收错误或错误信号检测	ORER、FER、ERS	RIE	不可能	不可能
SCIn_RXI	接收数据已满	RDRF	RIE	Possible	Possible
SCIn_TXI	发射端	TEND	TIE	Possible	Possible

在智能卡接口模式下也可以使用DMAC或DTC进行数据传输或接收。在发送过程中，当SSR_SMCI中的TEND标志设置为1时，会产生一个SCIn_TXI中断请求。如果事先将SCIn_TXI请求指定为DMAC或DTC激活源，则SCIn_TXI中断请求将激活DMAC或DTC，从而允许传输数据。当DMAC或DTC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在重传期间，TEND标志保持为0，并且不激活DMAC或DTC。因此，SCI和DMAC或DTC会自动传输指定的字节数，包括发生错误时的重传。但是，发生错误时，SSR_SMCI中的ERS 标志不会自动设置为0。因此，必须通过将SCR_SMCI中的RIE位设置为1来清除ERS 标志，以便在发生错误时产生SCIn_ERI中断请求。

使用DMAC或DTC发送或接收数据时，请务必在设置SCI之前启用DMAC或DTC。对于DMAC或DTC设置，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

在接收中，当接收数据设置为RDR时会产生SCIn_RXI中断请求。如果SCIn_RXI请求被指定为DMAC或DTC激活源，则此SCIn_RXI中断请求将激活DMAC或DTC，从而允许传输接收数据。如果发生错误，则设置错误标志。因此，DMAC或DTC未激活，并且

SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

29.10.5 Interrupts in Simple IIC Mode

Table 29.28 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DMAC or DTC can also be used to handle transfer in simple IIC mode.

When the IICINTM bit in SIMR2 register is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously set up as an activation source for the DMAC or DTC, the SCIn_RXI request activates the DMAC or DTC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DMAC or DTC, the SCIn_TXI request activates the DMAC or DTC to handle transfer of the transmit data.

When the IICINTM bit in SIMR2 register is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is at the low level on the rising edge of the SCLn signal for the 9th bit (acknowledge bit). If the SCIn_RXI was set up as an activation source for the DMAC or DTC beforehand, the SCIn_RXI request activates the DMAC or DTC to handle transfer of the received data.
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is at the high level on the rising edge of the SCLn signal for the 9th bit (acknowledge bit).

If the DMAC or DTC is used for data transfer in reception or transmission, be sure to set up and enable the DMAC or DTC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 29.28 SCI interrupt sources in simple IIC mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_RXI	Reception, ACK detection	—	RIE	Possible	Possible
SCIn_TXI	Transmission, NACK detection	—	TIE	Possible	Possible
STIn	Completion of generation of a start, restart, or stop condition	IICSTIF	TEIE	Not possible	Not possible

Note: Activation of the DTC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts).

29.11 Event Linking

By using interrupt request signals as event signals, the SCI can provide linked operation through the Event Link Controller (ELC) for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- Indicates that when SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger

而是向CPU发出SCIn_ERI中断请求。必须清除错误标志。

29.10.5 简单IIC模式下的中断

表29.28列出了简单IIC模式下的中断源。STI中断分配给发送结束中断(SCIn_TEI)请求。不能使用接收错误中断(SCIn_ERI)和地址匹配(SCIn_AM)请求。

DMAC或DTC也可用于处理简单IIC模式下的传输。

当SIMR2寄存器中的IIINTM位为1时：

- SCIn_RXI请求在第8位的SCLn信号的下降沿产生。如果SCIn_RXI先前设置为DMAC或DTC的激活源，则SCIn_RXI请求将激活DMAC或DTC以处理接收数据的传输。
- SCIn_TXI请求在第9位（确认位）的SCLn信号的下降沿生成。如果SCIn_TXI先前设置为DMAC或DTC的激活源，SCIn_TXI请求激活DMAC或DTC来处理传输数据的传输。

SIMR2寄存器中的IIINTM位为0时：

- 如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿上处于低电平，则生成SCIn_RXI请求（ACK检测）。如果事先将SCIn_RXI设置为DMAC或DTC的激活源，则SCIn_RXI请求将激活DMAC或DTC以处理接收数据的传输。
- 如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿处于高电平，则生成SCIn_TXI请求（NACK检测）。

如果DMAC或DTC用于接收或传输中的数据传输，请务必设置并启用DMAC或设置SCI之前的DTC。

当SIMR3中的IICSTAREQ、IICRSTAREQ和IICSTPREQ位用于生成开始条件、重新启动条件或停止条件时，生成完成时会发出STI请求。

Table 29.28 简单IIC模式下的SCI中断源

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_RXI	接收、ACK检测	—	RIE	Possible	Possible
SCIn_TXI	传输、NACK检测	—	TIE	Possible	Possible
STIn	完成启动、重新启动或停止条件的生成	IICSTIF	TEIE	不可能	不可能

Note: 只有当SIMR2.IICINTM位为1（使用接收和发送中断）时，才能激活DTC。

29.11 事件链接

通过使用中断请求信号作为事件信号，SCI可以通过EventLink提供链接操作预先选择的模块的控制器(ELC)。

无论相关中断请求使能位的值如何，都可以输出事件信号。

(1) 错误事件输出（接收错误或检测到错误信号）

- 表示在异步模式下接收期间由于奇偶校验错误而异常终止
- 指示在异步模式下接收期间由于帧错误而异常终止
- 表示接收期间由于溢出错误而异常终止
- 指示在智能卡接口模式下传输期间检测到错误信号
- 表示当SSR_FIFO.FER和PER标志为0，且接收数据少于接收FIFO数据时触发

number is in the receive FIFO buffer, 15 ETUs elapse when FIFO is selected and FCR.DRES is 1.

(2) Receive data full event output

- Indicates that ACK is detected if the IICINTM bit in SIMR2 register is 0 in simple IIC mode
- Indicates that the 8th-bit SCLn falling edge is detected if the IICINTM bit in SIMR2 register is 1 in simple IIC mode.
- When the IICINTM bit in SIMR2 register bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used.

(a) Non-FIFO selected

- Indicates that received data is in the Receive Data Register (RDR or RDRHL).

(b) FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output

- Indicates that the SCR/SCR_SMCI.TE bit changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the IICINTM bit in SIMR2 register is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the IICINTM bit in SIMR2 register is 1 in simple IIC mode.

(a) Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

(b) FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output

- Indicates the completion of transmission
- Indicates that the starting condition, restart condition, or stop condition is generated in simple IIC mode.

Note: When FIFO is selected, using this event output is prohibited.

(5) Address match event output

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is 1 in asynchronous mode, including multi-processor mode.

29.12 Address mismatch event output (SCI0_DCUF)

SCI0_DCUF indicates a mismatch of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is 1 in asynchronous mode, including multi-processor mode. This event can be used for snooze end request only.

29.13 Noise Cancellation Function

Figure 29.72 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2-stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless a match occurs, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

数字在接收FIFO缓冲液中，选择FIFO时15ETUSETALES，而FCR.DRES为1。

(2) 接收数据满事件输出

- 表示在simpleIIC模式下SIMR2寄存器的IICINTM位为0则检测到ACK
- 表示在简单IIC模式下，如果SIMR2寄存器中的IICINTM位为1，则检测到第8位SCLn下降沿。
- 当SIMR2寄存器位中的IICINTM位在简单IIC模式下主机发送期间为1时，设置ELC以便不使用接收数据满事件。

(a) Non-FIFO selected

- 表示接收到的数据在接收数据寄存器（RDR或RDRHL）中。

(b) FIFO selected

- 禁止使用此事件输出。

(3) 传输数据空事件输出

- 表示SCRSCR_SMCI.TE位由0变为1
- 表示在智能卡接口模式下传输完成
- 表示在simpleIIC模式下SIMR2寄存器的IICINTM位为0则检测到NACK
- 表示在简单IIC模式下，如果SIMR2寄存器中的IICINTM位为1，则检测到第9位SCLn下降沿。

(a) Non-FIFO selected

- 表示发送数据从发送数据寄存器（TDR或TDRHL）传输到发送移位 Register (TSR).

(b) FIFO selected

- 禁止使用此事件输出。

(4) 发送结束事件输出

- 表示传输完成
- 指示在简单IIC模式下生成启动条件、重启条件或停止条件。

Note: 选择FIFO时，禁止使用该事件输出。

(5) 地址匹配事件输出

- 在异步模式下，包括多处理器模式，当DCCR.DCME为1时，表示比较数据(CDR.CMPD)与一帧接收数据的匹配。

29.12 地址不匹配事件输出(SCI0_DCUF)

SCI0_DCUF表示比较数据(CDR.CMPD)与一帧接收数据不匹配时
DCCR.DCME在异步模式下为1，包括多处理器模式。此事件仅可用于贪睡结束请求。

29.13 降噪功能

图29.72显示了用于噪声消除的噪声滤波器的配置。噪声滤波器由一个2级触发器电路和一个匹配检测电路组成。当噪声滤波器的输入信号和2级触发器电路的输出信号完全匹配时，匹配的电平作为内部信号传送。除非发生匹配，否则将保留先前的值。当相同电平在噪声滤波器的采样时钟上保持3个周期或更长时间时，它被认为是有效的接收信号。3个周期或更短的脉冲变化被认为是噪声，而不是接收信号。

When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 the period of 1 transfer bit.

When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 the period of 1 transfer bit.

When SEMR.ABCSE = 1, the cycle is 1/6 the period of 1 transfer bit.

In asynchronous mode, the noise cancellation function can be applied to the receive signal input on the RXDn pin. The receive level of RXDn is sampled in the flip-flop circuit of the noise filter on the base clock of asynchronous mode.

In simple IIC mode, this function can be used for each input on SDAn and SCLn. The sampling clock for the noise cancellation function is selected in the SNFR.NFCS bit by dividing the baud rate generator source clock by 1, 2, 4, or 8.

If the base clock is stopped with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When TE and RE in SCR are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is considered as an internal signal. When the input level corresponds to 0, the initial output of the noise filter is retained until the level matches in 3 consecutive sampling cycles.

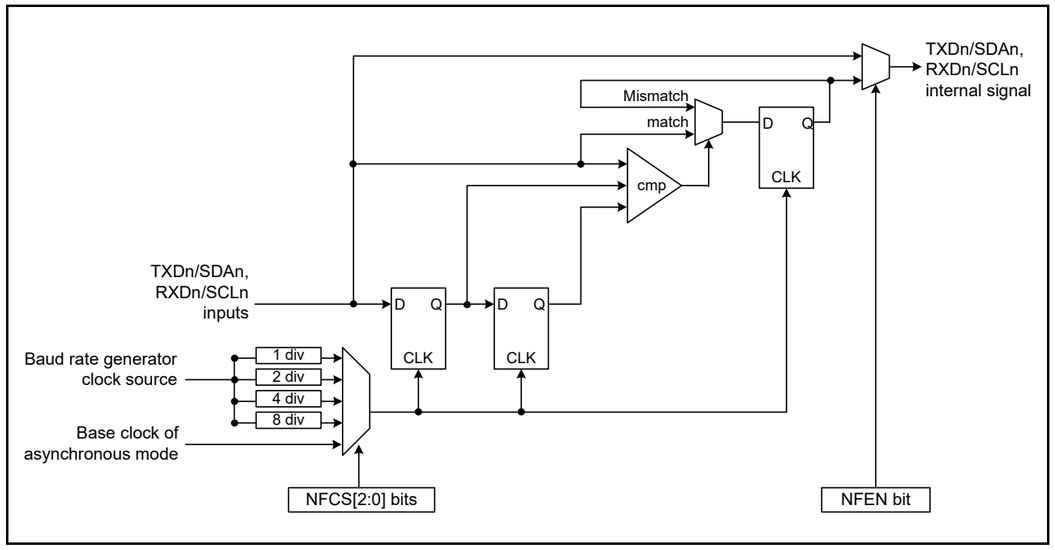


Figure 29.72 Digital noise filter circuit block diagram

29.14 Usage Notes

29.14.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

29.14.2 SCI Operations during Low Power State

(1) Transmission

When setting the module to the stopped state or in transition to Software Standby mode, stop the operation (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting the I/O port as an SCI function, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes TSR. The TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected. The value is kept with FIFO selected. Depending on the port settings and the SPTR register settings, output pins might output the level before a transition to the low power state is made after release from the module-stop state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

当SEMR.ABCS=0且SEMR.ABCSE=0时，周期为1161个传输位的周期。

当SEMR.ABCS=1和SEMR.ABCSE=0时，周期为181个传输位的周期。

当SEMR.ABCSE=1时，周期为161个传输位的周期。

在异步模式下，可以对RXDn引脚上的接收信号输入应用噪声消除功能。RXDn的接收电平在异步模式的基本时钟上在噪声滤波器的触发器电路中被采样。

在简单IIC模式下，该功能可用于SDAn和SCLn上的每个输入。通过将波特率发生器源时钟除以1、2、4或8，在SNFR.NFCS位中选择噪声消除功能的采样时钟。

如果在启用噪声滤波器的情况下停止基本时钟，然后再次重新启动基本时钟输入，则噪声滤波器操作将从时钟停止的状态恢复。当SCR中的TE和RE在基本时钟输入期间设置为0时，所有噪声滤波器触发器值都被初始化为1。因此，如果在接收操作恢复时输入数据为1，则该函数确定电平匹配为检测到并且结果被认为是内部信号。当输入电平对应于0时，保留噪声滤波器的初始输出，直到电平在3个连续采样周期内匹配。

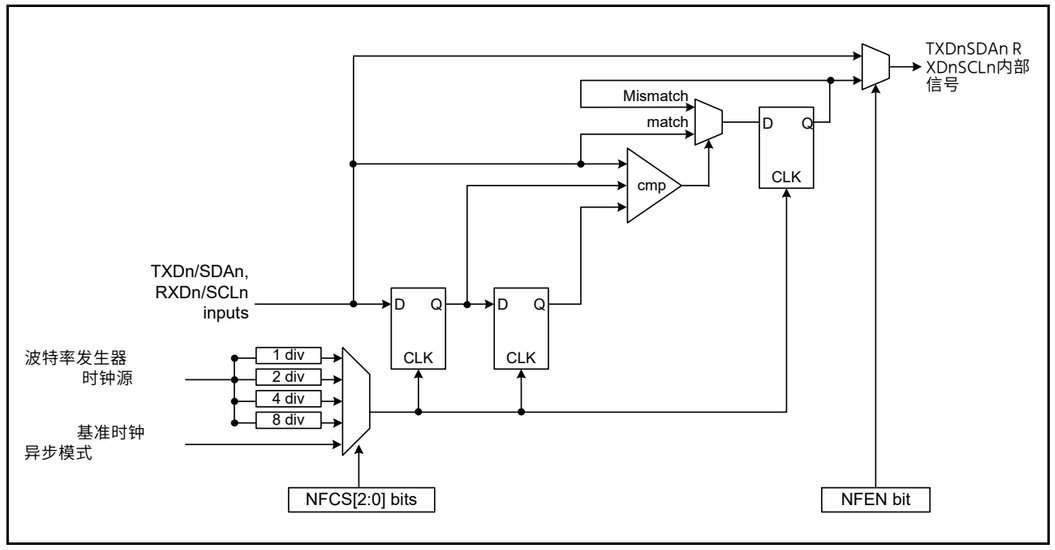


Figure 29.72 数字噪声滤波器电路框图

29.14 使用说明

29.14.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SCI操作。SCI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

29.14.2 低功耗状态下的SCI操作

(1) Transmission

将模块设置为停止状态或转换到软件待机模式时，在将TXDn引脚切换到通用IO端口引脚功能后停止操作（通过将SCRSCR_SMCI中的TIE、TE和TEIE位设置为0）。当设置IO口为SCI功能时，SPTR寄存器可以控制TXDn引脚的状态。将TE位设置为0初始化TSR。SSRSSR_SMCI中的TEND位在选择非FIFO时初始化为1。该值在选择FIFO的情况下保持不变。根据端口设置和SPTR寄存器设置，输出引脚可能会在从模块停止状态或软件待机模式释放后转换到低功耗状态之前输出电平。在传输过程中转换到这些状态时，传输的数据变得不确定。

To transmit data in the same transmission mode after cancellation of the low power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

To transmit data with a different transmission mode, initialize the SCI first.

Figure 29.73 shows an example flow of transition to Software Standby mode during transmission. Figure 29.74 and Figure 29.75 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or transitioning to Software Standby mode from the transmission mode using DTC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC.

(2) Reception

(a) When address match function is not used as wakeup condition

Before specifying the module-stop state or transitioning to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the data being received is invalid.

Figure 29.76 shows an example flow of transition to Software Standby mode during reception.

(b) When address match function is used as condition of resumption (wakeup)

Before specifying the module-stop state or transitioning to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When the SCI transfers to the low power mode, if the receive data pin (RXD) is at the low level, set the RXDESEL bit in SEMR to 0. If RXDESEL is set to 1, there is a possibility that a start bit (falling edge of RXDn pin) cannot be detected on release of the low power mode.

Figure 29.77 shows an example flow of transition to Software Standby mode during reception with address match.

(c) When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions, including the maximum bit rates, exist. For details, see section 11, Low Power Modes.

在取消低功耗状态后以相同的传输模式传输数据：

1. 将TE位设置为1。
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. 将数据顺序写入TDR以开始数据传输。

要以不同的传输模式传输数据，请先初始化SCI。

图29.73显示了传输期间转换到软件待机模式的示例流程。图29.74和
图29.75显示了转换到软件待机模式期间的端口引脚状态。

在指定模块停止状态或从传输模式转换到软件待机模式之前，使用
DTC传输，停止传输操作（TE=0）。要在使用DTC取消后开始发送，请将TE位设置为1。SCIn_TXI中断标志 设置为1并使用DTC开始发送。

(2) Reception

(a) 当地址匹配功能不用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前，停止接收操作（SCRSCR_SMCI中的RE=0）。如果在数据接收期间进行转换，则正在接收的数据无效。

图29.76显示了接收期间转换到软件待机模式的示例流程。

(b) 当地址匹配功能用作恢复条件时（唤醒）

在指定模块停止状态或转换到软件待机模式之前：

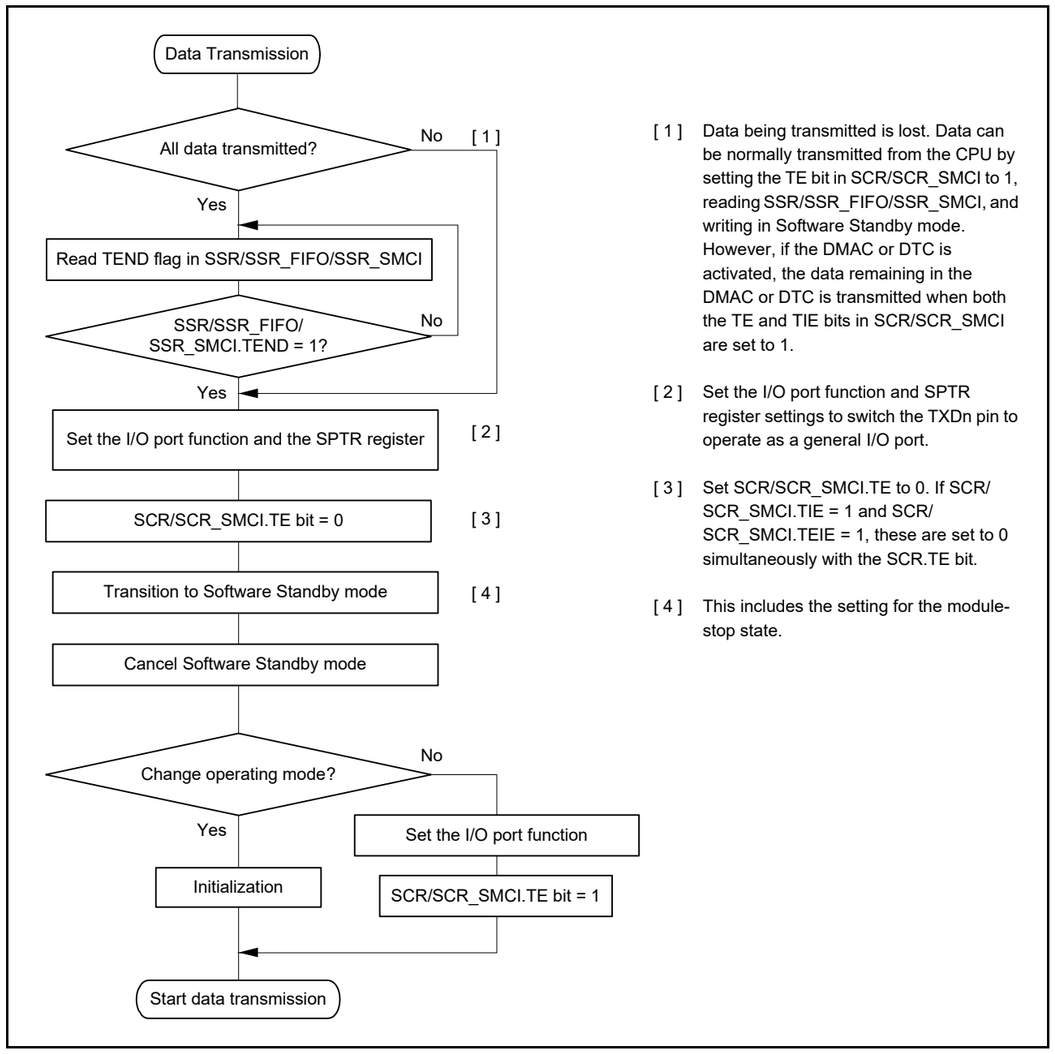
1. 设置取消低功耗状态后的操作。
2. 将CDR.CMPD和DCCR.DCME设置为1。
3. 设置接收操作（在SCRSCR_SMCI中RE=1）。
4. 设置模块停止状态或软件待机模式。

当SCI转移到低功耗模式时，如果接收数据引脚(RXD)处于低电平，则将SEMR中的RXDESEL位设置为0。如果RXDESEL设置为1，则可能会出现起始位（下降RXDn引脚的边沿）无法在低功耗模式释放时检测到。

图29.77显示了在地址匹配的接收期间转换到软件待机模式的示例流程。

(c) 在贪睡模式下使用SCI0时

在贪睡模式下使用SCI0时，存在一些限制，包括最大比特率。有关详细信息，请参阅第11节，低功耗模式。



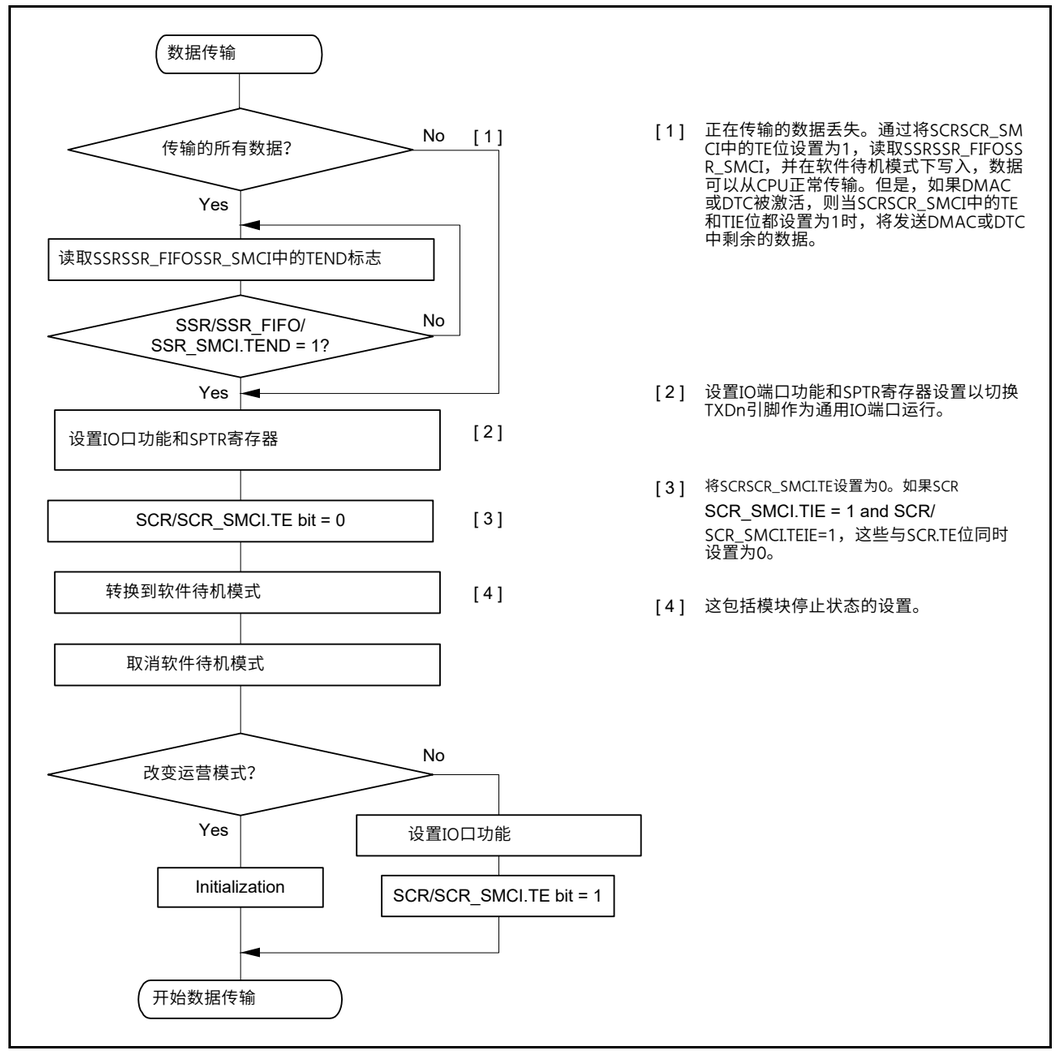
[1] Data being transmitted is lost. Data can be normally transmitted from the CPU by setting the TE bit in SCR/SCR_SMCI to 1, reading SSR/SSR_FIFO/SSR_SMCI, and writing in Software Standby mode. However, if the DMAC or DTC is activated, the data remaining in the DMAC or DTC is transmitted when both the TE and TIE bits in SCR/SCR_SMCI are set to 1.

[2] Set the I/O port function and SPTR register settings to switch the TXDn pin to operate as a general I/O port.

[3] Set SCR/SCR_SMCI.TE to 0. If SCR/SCR_SMCI.TIE = 1 and SCR/SCR_SMCI.TEIE = 1, these are set to 0 simultaneously with the SCR.TE bit.

[4] This includes the setting for the module-stop state.

Figure 29.73 Example flow of transition to Software Standby mode during transmission



[1] 正在传输的数据丢失。通过将SCRSCR_SMCI中的TE位设置为1，读取SSRSSR_FIFOSSR_SMCI，并在软件待机模式下写入，数据可以从CPU正常传输。但是，如果DMAC或DTC被激活，则当SCRSCR_SMCI中的TE和TIE位都设置为1时，将发送DMAC或DTC中剩余的数据。

[2] 设置IO端口功能和SPTR寄存器设置以切换TXDn引脚作为通用IO端口运行。

[3] 将SCRSCR_SMCI.TE设置为0。如果SCR SCR_SMCI.TIE = 1 and SCR/ SCR_SMCI.TEIE=1，这些与SCR.TE位同时设置为0。

[4] 这包括模块停止状态的设置。

Figure 29.73 传输期间转换到软件待机模式的示例流程

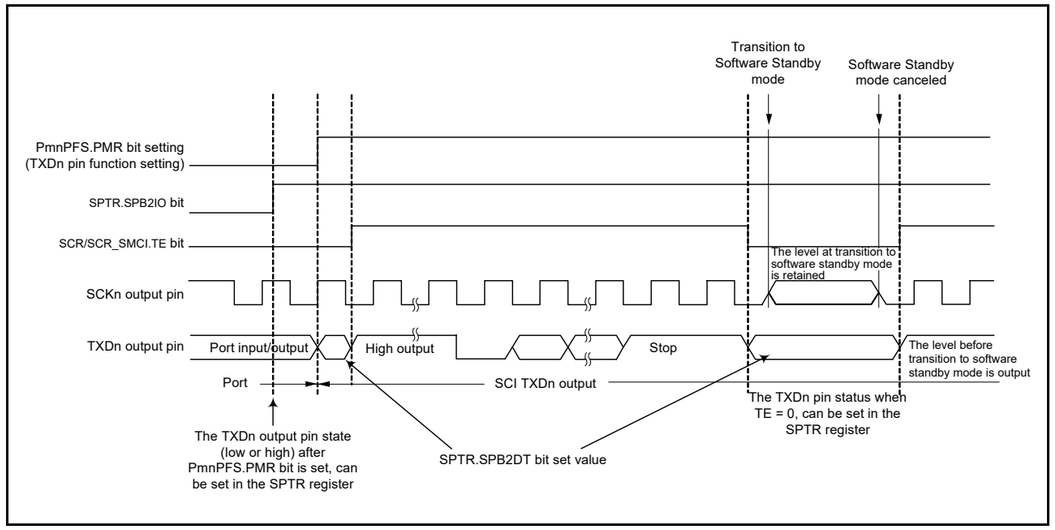


Figure 29.74 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

Figure 29.75 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

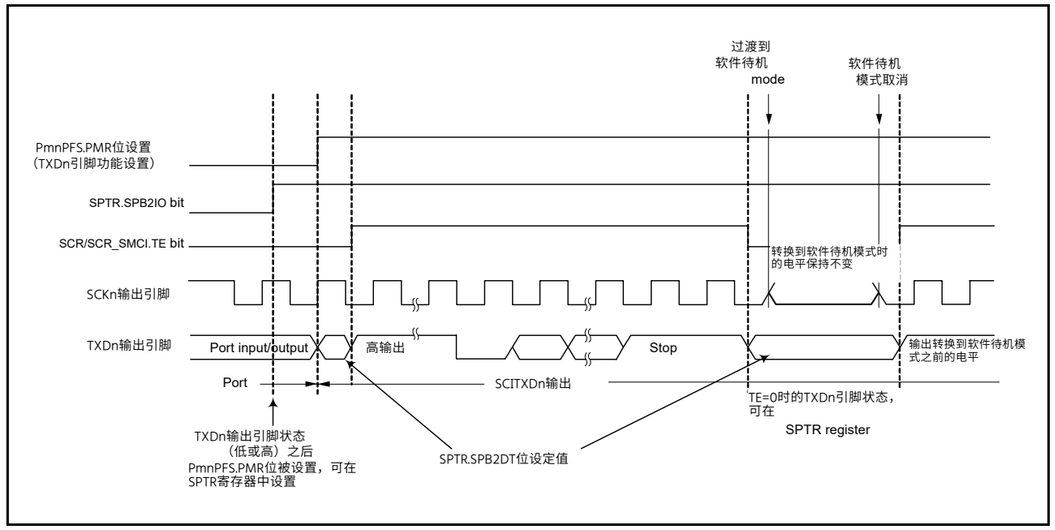


Figure 29.74 转换到内部时钟和异步传输的软件待机模式期间的端口引脚状态

Figure 29.75 通过内部时钟和时钟同步传输转换到软件待机模式期间的端口引脚状态

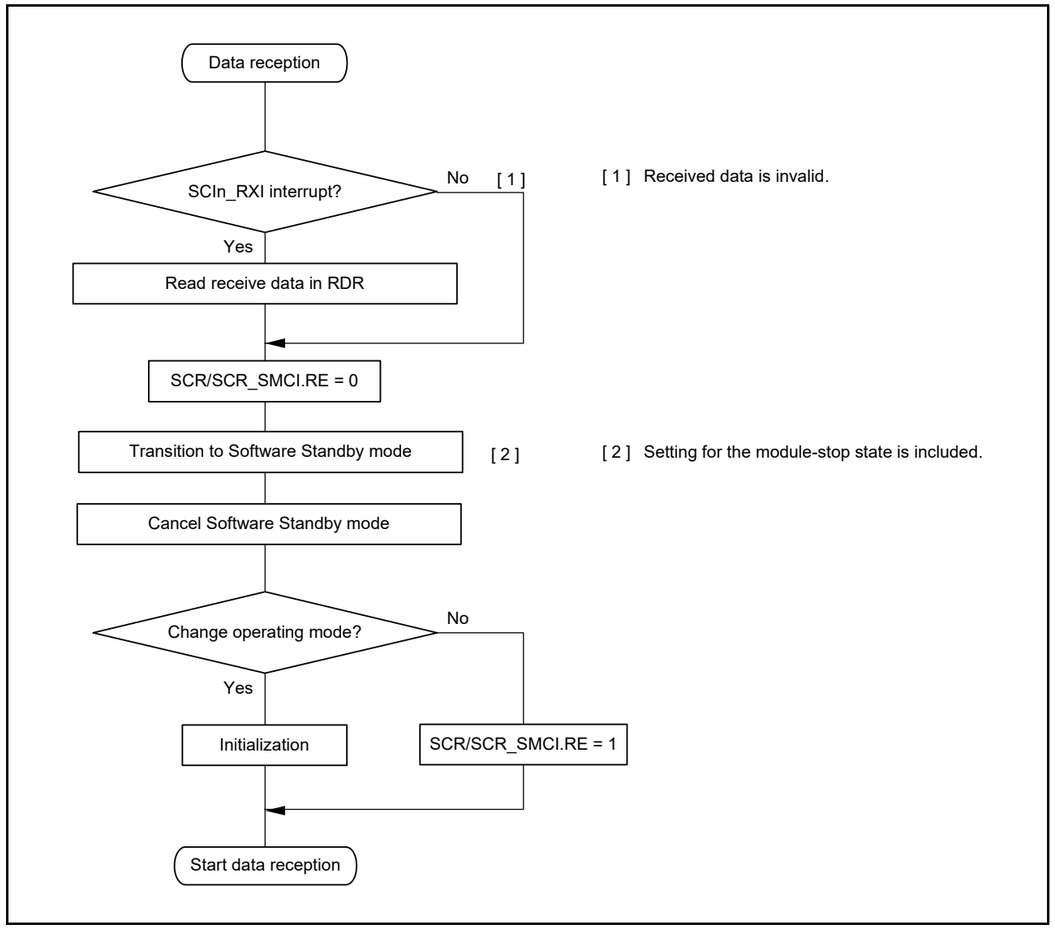


Figure 29.76 Example flow of transition to Software Standby mode during reception

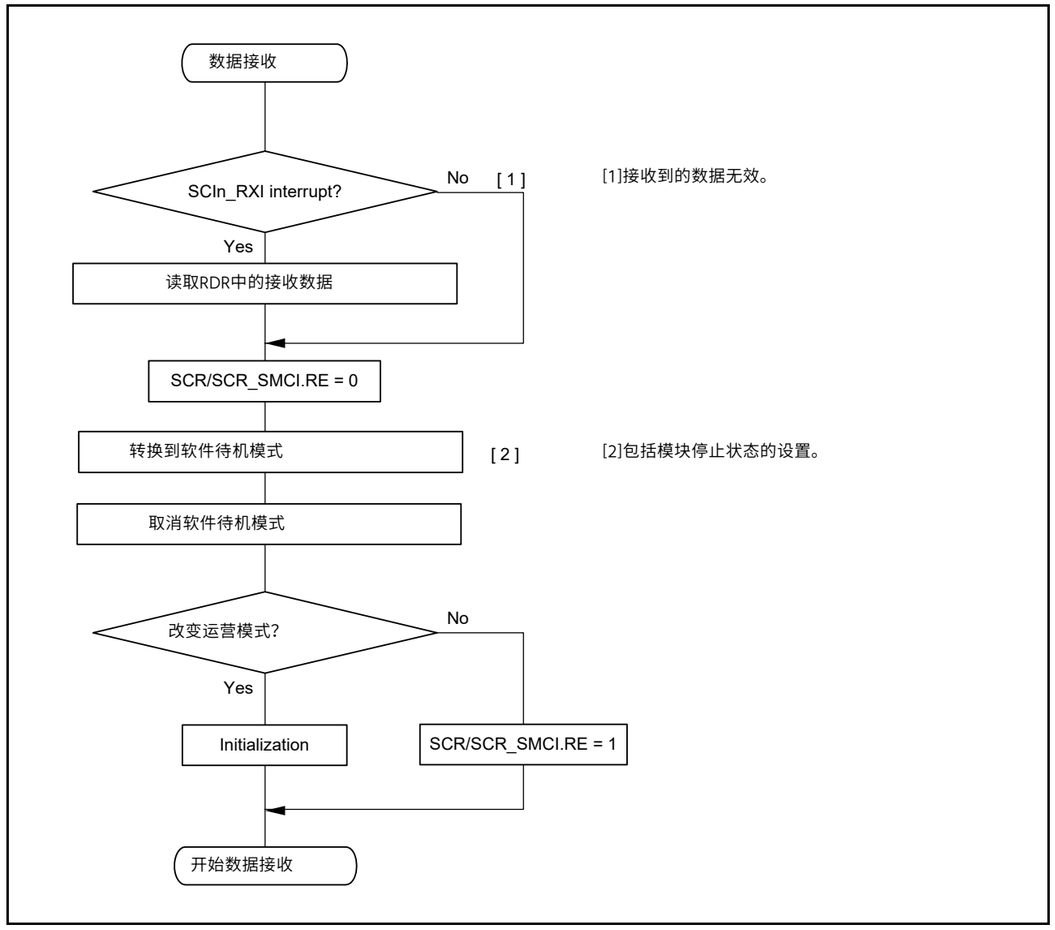
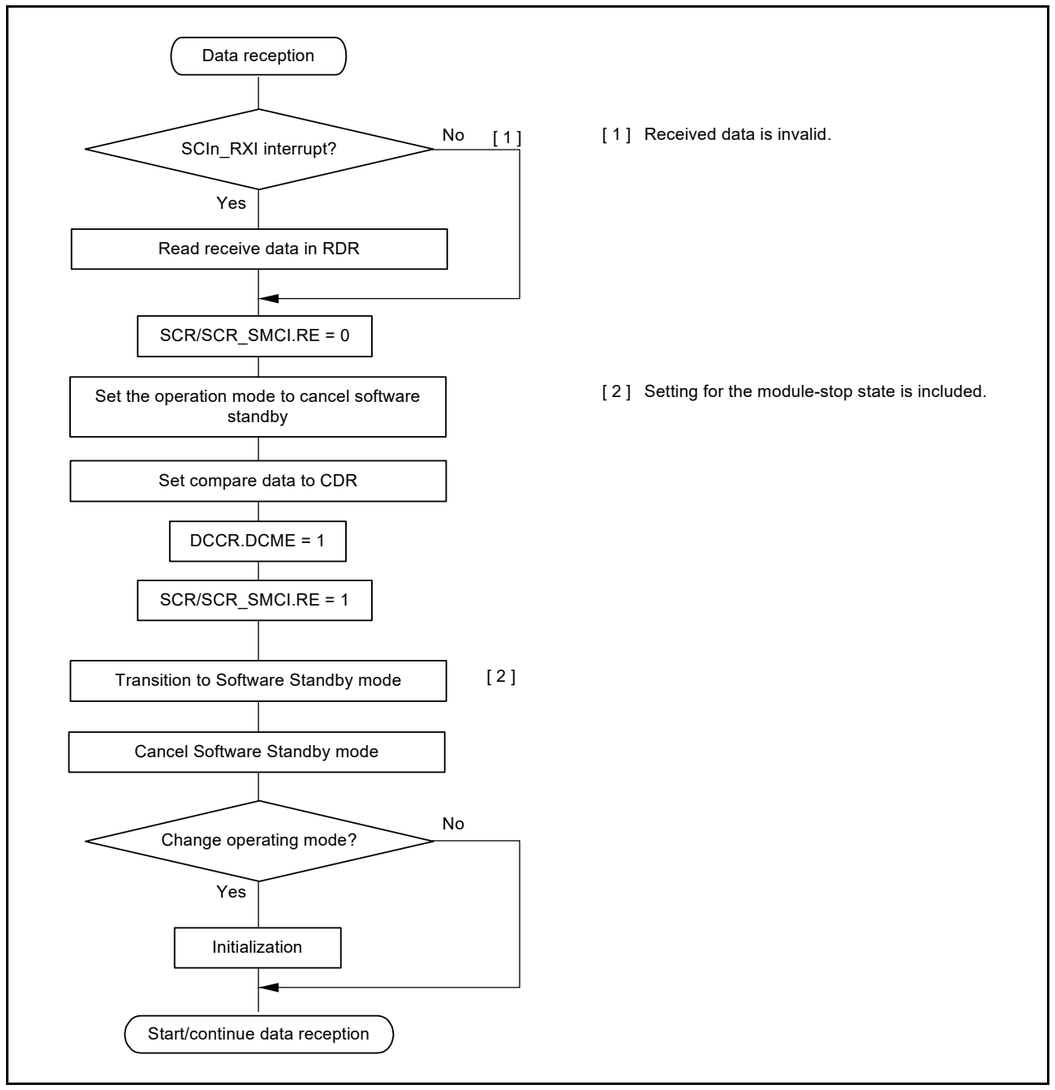


Figure 29.76 接收期间转换到软件待机模式的示例流程



[1] Received data is invalid.

[2] Setting for the module-stop state is included.

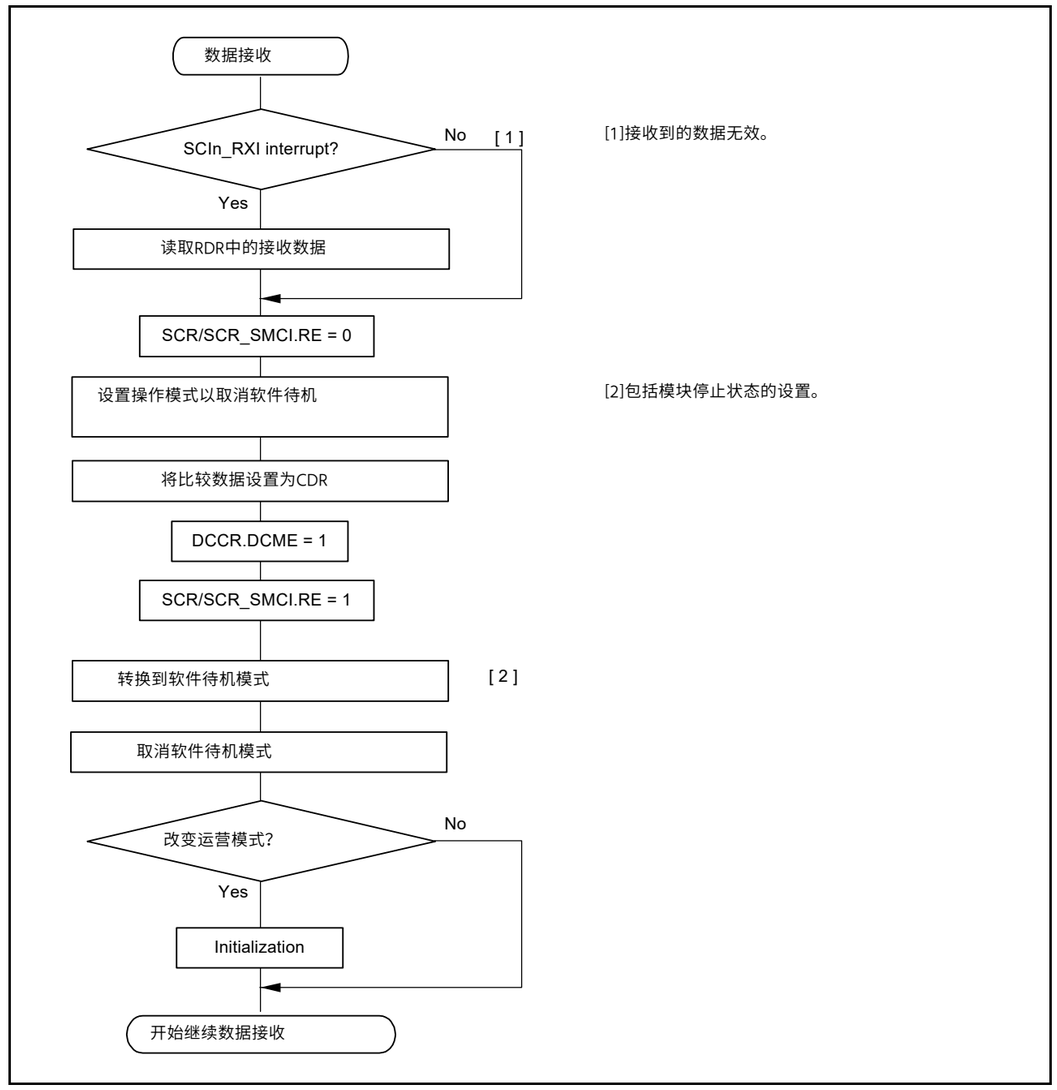
Figure 29.77 Example flow of transition to Software Standby mode during reception with address match

29.14.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and the FER flag in SSR is set to 1 to indicate a framing error. The PER flag in SSR might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, if the FER flag is set to 0, indicating that no framing error occurred, it is set to 1 again. When the RXDESEL bit in SEMR is 1, the SCI sets the FER flag in SSR to 1 and stops receiving operations until a start bit of the next data frame is detected. If the FER flag in SSR is 0, the FER flag in SSR retains 0 during the break.

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.



[1]接收到的数据无效。

[2]包括模块停止状态的设置。

Figure 29.77 在地址匹配的接收期间转换到软件待机模式的示例流程

29.14.3 断裂检测和处理

(1) Non-FIFO selected

当检测到帧错误时，可以通过直接读取RXDn引脚值来检测中断。在中断时，来自RXDn引脚的输入变为全0，并且SSR中的FER标志设置为1以指示帧错误。SSR中的PER标志也可能设置为1以指示奇偶校验错误。即使在收到中断后，SCI仍继续接收操作。因此，如果FER标志设置为0，表示没有发生帧错误，则再次设置为1。当SEMR中的RXDESEL位为1时，SCI将SSR中的FER标志设置为1，并停止接收操作，直到检测到下一个数据帧的起始位。如果SSR中的FER标志为0，则SSR中的FER标志在中断期间保持为0。

当RXDn引脚设置为1且中断结束时，在第一个下降沿检测起始位的开始
RXDn引脚允许SCI开始接收操作。

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for one frame, reception stops. When a framing error is detected, a break can be detected by reading the RXDMON bit value in SPTR. After the RXD signal is in the mark state and the break ends, reception of data to FRDRHL resumes.

29.14.4 Mark State and Production of Breaks

When the TE bit is 0 in SCR/SCR_SMCI, disabling serial transmission, the state of the TXDn pin can be set using the SPB2IO bit in SPTR and the SPB2DT bit in SPTR. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the TE bit in SCR/SCR_SMCI to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put a communication line in the mark state (the state of 1), and change the TxDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the TE bit in SCR/SCR_SMCI to 0. When the TE bit in SCR/SCR_SMCI is set to 0, the transmitter is initialized regardless of the current state of transmission.

29.14.5 Receive Error Flags and Transmit Operations in Clock Synchronous and Simple SPI Modes

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even when data is written to the TDR or FTDRL*1 registers. Be sure to set the receive error flags to 0 before starting transmission.

Note: The receive error flags cannot be set to 0 if serial reception is disabled by setting the RE bit in SCR/SCR_SMCI to 0.

Note 1. Do not use the FTDRH register in simple SPI mode.

29.14.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous and Simple SPI Modes

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLK cycle + data output delay time for the slave + setup time for the master (tSU).

See Figure 29.78.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock, bit [7]. See Figure 29.78.

When updating TDR after bit [7] starts to transmit, update TDR when the synchronization clock is in the low-level period, and set the high-level width of the transmit clock bit [7] to 4 PCLK cycles or longer. See Figure 29.78.

(2) FIFO selected

检测到帧错误后，当SCI检测到一帧连续接收数据为0时，接收停止。当检测到帧错误时，可以通过读取SPTR中的RXDMON位值来检测中断。在RXD信号处于标记状态并且中断结束后，重新接收到FRDRHL的数据。

29.14.4 标记状态和产生的中断

当SCRSCR_SMCI中的TE位为0时，禁止串行传输，TXDn引脚的状态可以使用SPTR中的SPB2IO位和SPTR中的SPB2DT位来设置。使用这种方法，可以将TXDn引脚置于标记状态以发送中断。

在将SCRSCR_SMCI中的TE位设置为1之前，启用串行传输，设置SPB2IO和SPB2DT位以将通信线置于标记状态（状态为1），并使用IO端口功能更改TxDn引脚。要输出数据传输中断，通过设置SPB2IO和SPB2DT位将TXDn引脚设置为输出0后，使用IO端口功能更改TXDn引脚并将SCRSCR_SMCI中的TE位设置为0。当SCR中的TE位SCR_SMCI设置为0，无论当前的传输状态如何，都会初始化发送器。

29.14.5 以时钟同步和简单的方式接收错误标志和发送操作 SPI模式

当SSRSSR_FIFO中的接收错误标志(ORER)设置为1时，发送无法开始，即使数据已写入TDR或FTDRL*1寄存器。确保在开始传输之前将接收错误标志设置为0。

Note: 如果通过将SCRSCR_SMCI中的RE位设置为0来禁用串行接收，则接收错误标志不能设置为0。

注1.不要在简单SPI模式下使用FTDRH寄存器。

29.14.6 时钟同步和时钟同步传输的限制 简单的SPI模式

当外部时钟源用作同步时钟时，有以下限制。

(1) 传输开始

从将发送数据写入TDR到外部时钟输入开始，至少等待以下时间：

1个PCLK周期+从设备的数据输出延迟时间+主设备的建立时间(tSU)。

请参见图29.78。

(2) 连续传输

在发送时钟下降沿之前将下一个发送数据写入TDR或TDRHL，位[7]。请参见图29.78。

在bit[7]开始发送后更新TDR时，同步时钟处于低电平周期时更新TDR，并将发送时钟bit[7]的高电平宽度设置为4个PCLK周期或更长。请参见图29.78。

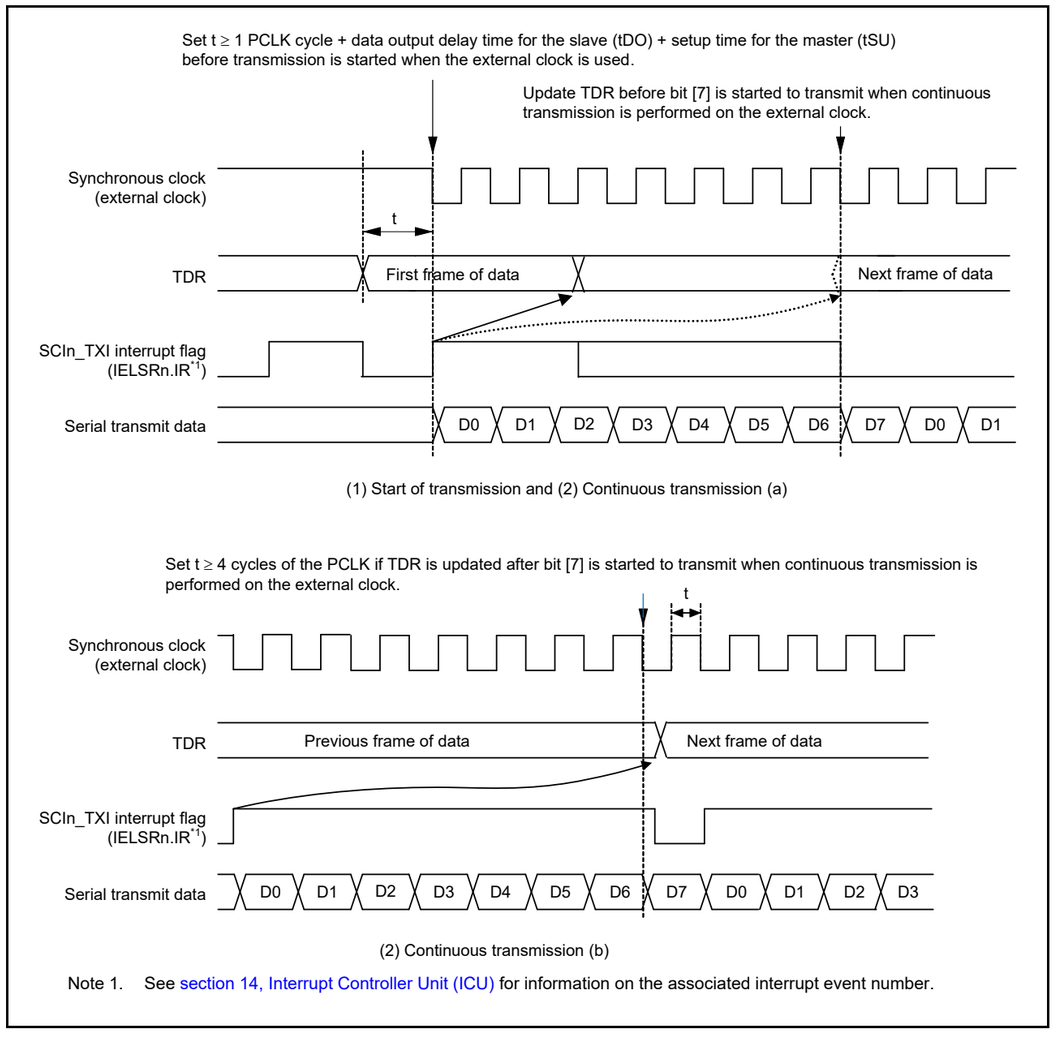


Figure 29.78 Restrictions on the use of external clock in clock synchronous transmission

29.14.7 Restrictions on Using DMAC or DTC

During transmission or reception operations using the DMAC or DTC, do not set the transfer information for the DMAC or DTC.

(1) Writing data to TDR (FTDRHL)

(a) Non-FIFO selected

Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not transferred to TSR yet. When using DMAC or DTC, be sure to write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

(b) FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when the TE bit is 1 in SCR register. Confirm the amount of writable data using the FDR.T[4:0] bits.

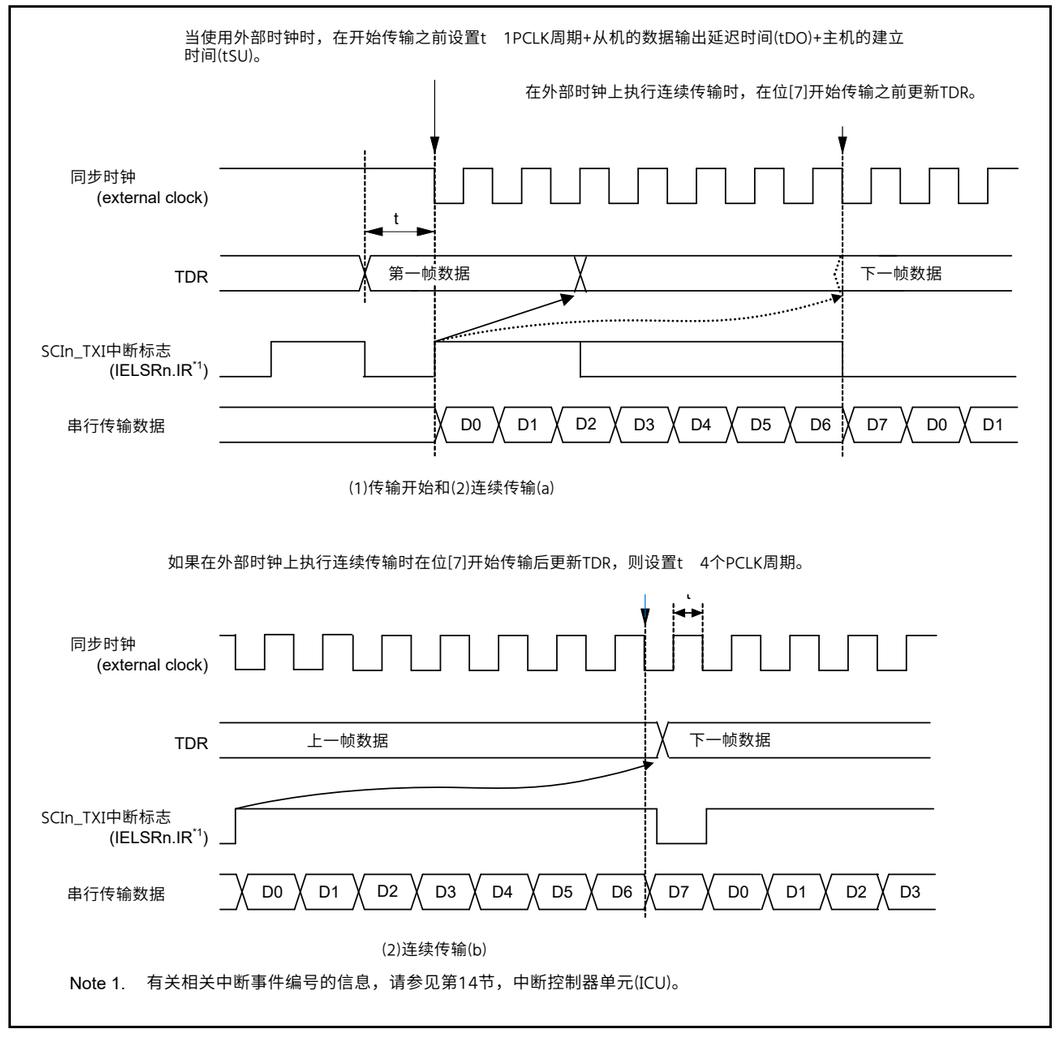


Figure 29.78 时钟同步传输中使用外部时钟的限制

29.14.7 使用DMAC或DTC的限制

在使用DMAC或DTC进行发送或接收操作期间，请勿设置DMAC或DTC的传输信息。

(1) 将数据写入TDR(FTDRHL)

(a) Non-FIFO selected

数据可以写入TDR和TDRHL。但是，如果在发送数据保留在TDR或TDRHL中时将新数据写入TDR或TDRHL，则TDR和TDRHL中的先前数据将丢失，因为它尚未传输到TSR。使用DMAC或DTC时，请务必在SCIn_TXI中断请求处理程序中将发送数据写入TDR或TDRHL。

(b) FIFO selected

当SCR寄存器中的TE位为1时，可以将数据写入FTDRH和FTDRL寄存器。使用FDR.T[4:0]位确认可写数据量。

(2) Reading data from RDR (FRDRHL)

When using the DMAC or DTC to read RDR and RDRHL, be sure to set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI channel.

29.14.8 Notes on Starting Transfer

At the point where transfer starts when the Interrupt Status flag, IELSRn.IR, in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1). For details on the interrupt status flag, see section 14, Interrupt Controller Unit (ICU).

1. Confirm that transfer stopped (the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0).
2. Set the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE) to 0.
3. Read the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to check that it is 0.
4. Set the Interrupt Status flag, IELSRn.IR, in the ICU to 0.

29.14.9 External Clock Input in Clock Synchronous and Simple SPI Modes

In clock synchronous mode and simple SPI mode, the external clock (SCKn) must be input as follows:

High-pulse period, low-pulse period = 2 PCLK cycles or more, period = 6 PCLK cycles or more.

29.14.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set by the CKPH and CKPOL bits when the SSE bit is 1 in the SPMR register. This prevents the clock line from being placed in the high-impedance state when the TE bit is set to 0 or unexpected edges from being generated on the clock line when the TE bit changes from 0 to 1 in the SCR register. When the SSE bit is 0 in single-master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the TE bit is set to 0.
- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin, as indicated in Figure 29.79. If the TE and RE bits in the SCR become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while the current character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

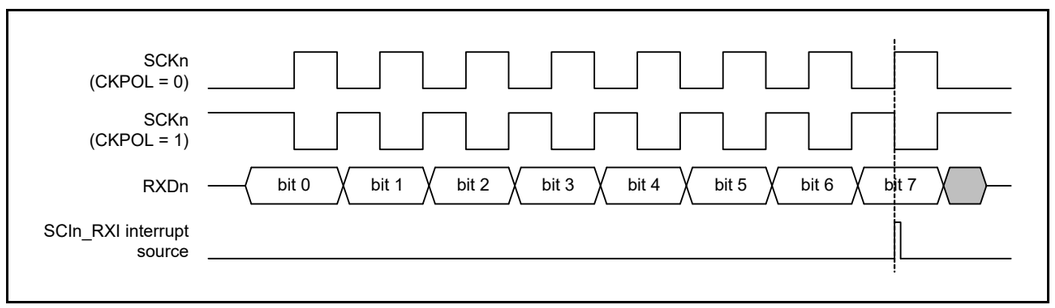


Figure 29.79 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) Slave mode

- Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

(2) 从RDR(FRDRHL)读取数据

使用DMAC或DTC读取RDR和RDRHL时，务必将接收数据满中断（SCIn_RXI）设置为相关SCI通道的激活源。

29.14.8 开始转移注意事项

在ICU中的中断状态标志IELSRn.IR为1时开始传输的点，按照本节中的程序在允许操作之前清除中断请求（通过将SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位设置为1）。有关中断状态标志的详细信息，请参见第14节，中断控制器单元(ICU)。

1. 确认传输已停止（SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位为0）。
2. 将相关的中断使能位（SCRSCR_SMCI.TIE或SCRSCR_SMCI.RIE）设置为0。
3. 读取相关的中断使能位（SCRSCR_SMCI.TIE或SCRSCR_SMCI.RIE位）以检查它是否为0。
4. 将ICU中的中断状态标志IELSRn.IR设置为0。

29.14.9 时钟同步和简单SPI模式下的外部时钟输入

在时钟同步模式和简单SPI模式下，外部时钟（SCKn）必须输入如下：

高脉冲周期，低脉冲周期=2个PCLK周期或更多，周期=6个PCLK周期或更多。

29.14.10 简单SPI模式的限制

(1) 主模式

- 使用电阻上拉或下拉与传输时钟初始设置相匹配的时钟线
  SPMR寄存器中SSE位为1时的CKPH和CKPOL位。这可以防止在TE位设置为0时将时钟线置于高阻抗状态，或者当SCR寄存器中的TE位从0变为1时在时钟线上产生意外边沿。当SSE位在单主机模式下为0时，不需要上拉或下拉时钟线，因为即使将TE位设置为0，时钟线也不会处于高阻状态。
- 对于时钟延迟设置（SPMR.CKPH位为1），接收数据满中断（SCIn_RXI）在SCKn引脚上的最后一个时钟沿之前产生，如图29.79所示。如果SCR中的TE和RE位在SCKn引脚上的时钟信号的最后一个边沿之前变为0，则SCKn引脚处于高阻状态，因此传输时钟的最后一个时钟脉冲的宽度被缩短.此外，SCIn_RXI中断可能会导致所连接从机的SSn引脚上的输入信号在SCKn引脚上的时钟信号的最后一个边沿之前变为高电平，从而导致从机的错误操作。
- 在多主机配置中，如果在传输当前字符时发生模式故障错误，则SCKn引脚输出变为高阻态，而SSn引脚上的输入处于低电平，从而停止将时钟信号提供给连接的奴隶。重新启动传输时，重置连接的从机以避免未对齐的位。

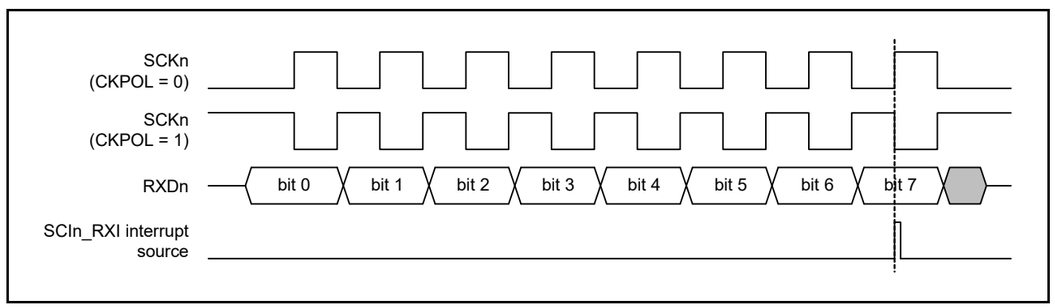


Figure 29.79 带时钟延迟的简单SPI模式下SCIn_RXI中断的时序

(2) 从机模式

- 从将发送数据写入TDR到外部时钟输入开始，至少等待以下时间：

1 PCLK cycle + data output delay time for the slave (tDO) + setup time for the master (tSU)
Also, wait at least 5 PCLK cycles from the input of the low level on the SSn pin to the start of the external clock input.

- Provide an external clock signal to the master for the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin changes from low to high while a character is being transferred, set the TE and RE bits in SCR to 0 and, after restoring the settings, restart transfer of the first byte.

1个PCLK周期+从机的数据输出延迟时间(tDO)+主机的建立时间(tSU)另外，从SSn引脚输入低电平到外部时钟输入开始，至少等待5个PCLK周期.

- 向主机提供外部时钟信号，用于传输数据长度
- 在数据传输开始之前和结束之后控制SSn引脚上的输入
- 当SSn引脚上的输入电平从低电平变为高电平而字符正在传输时，设置TE和SCR中的RE位为0，并在恢复设置后重新开始传输第一个字节。

30. I2C Bus Interface (IIC)

30.1 Overview

The MCU has a 2-channel I2C Bus Interface (IIC). The IIC module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions.

Table 30.1 lists the IIC specifications, Figure 30.1 shows a block diagram, and Figure 30.2 shows an example of I/O pin connections to external circuits, with an I2C bus configuration example. Table 30.2 lists the I/O pins.

Table 30.1 IIC specifications (1 of 2)

Parameter	Description
Communications format	• I2C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the setup times, hold times, and bus-free times for the transfer rate.
Transfer rate	Fast-mode supported up to 400 kbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Configurable for up to three different slave addresses • 7-bit and 10-bit address formats supported, including simultaneous use • General call addresses, device ID addresses, and SMBus host addresses detectable.
Acknowledgment	• For transmission, automatic loading of the acknowledge bit. Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatic transmission of the acknowledge bit. If a wait between the 8th and 9th clock cycles is selected, software can control the value in the acknowledge field in response to the received value.
Wait function	During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the 8th and 9th clock cycles • Waiting between the 9th clock cycle and the 1st clock cycle of the next transfer.
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed
Arbitration	• For multi-master operation: - SCL clock synchronization is possible when conflict occurs with the SCL signal from another master - When issuing the start condition can create conflict on the bus, loss of arbitration is detected by testing for a mismatch between the internal signal for the SDA line and the level on the SDA line - In master operation, loss of arbitration is detected by testing for a mismatch between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration because the start condition occurs while the bus is busy is detectable, to prevent the issuing of double start conditions • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match • Loss of arbitration because mismatching of internal and line levels for data is detectable in slave transmission.
Timeout function	Internal detection of long-interval stops of the SCL clock
Noise cancellation	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters.
Interrupt sources	• Transfer error or occurrence of events (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end.
Module-stop function	Module-stop state can be set
IIC operating modes	• Master transmit • Master receive • Slave transmit • Slave receive.

30. I2C总线接口(IIC)

30.1 Overview

MCU有一个2通道I2C总线接口(IIC)。IIC模块符合并提供NXPI2C（内部集成电路）总线接口功能的子集。

表30.1列出了IIC规范，图30.1显示了框图，图30.2显示了IO引脚连接到外部电路的示例，以及I2C总线配置示例。表30.2列出了IO引脚。

Table 30.1 IIC规格(1of2)

Parameter	Description
通讯格式	I2C总线格式或SMBus格式 可选择主模式或从模式 自动保护传输速率的设置时间、保持时间和无总线时间。
传输率	支持高达400kbps的快速模式
SCL clock	对于主机操作，SCL时钟的占空比可在4%至96%的范围内选择
发布和检测条件	自动生成启动、重新启动和停止条件。 可检测启动条件（包括重启条件）和停止条件。
从机地址	最多可配置三个不同的从属地址 支持7位和10位地址格式，包括同时使用 可检测到广播呼叫地址、设备ID地址和SMBus主机地址。
Acknowledgment	对于传输，自动加载确认位。 检测到未确认位时，可以自动暂停下一个发送数据的传输。 对于接收，确认位的自动传输。 如果选择了第8和第9个时钟周期之间的等待，软件可以控制确认字段中的值以响应接收到的值。
等待功能	在接收期间，通过将SCL时钟保持为低电平可获得以下等待周期： 在第8个和第9个时钟周期之间等待 在第9个时钟周期和下一次传输的第一个时钟周期之间等待。
SDA输出延迟功能	传输数据的输出时序，包括确认位，可以延迟
Arbitration	• For multi-master operation: 当与来自另一个主机的SCL信号发生冲突时，SCL时钟同步是可能的当发出启动条件可能会在总线上产生冲突时，通过测试SDA线的内部信号与上的电平之间的不匹配来检测仲裁丢失SDA线在主机操作中，通过测试SDA线上的信号与SDA线的内部信号之间的不匹配来检测仲裁丢失。 可检测到由于在总线繁忙时出现启动条件而导致的仲裁丢失，以防止发出双重启动条件SDA线路上的不匹配 仲裁丢失，因为在从传输中可检测到数据的内部和线路电平不匹配。
超时功能	内部检测SCL时钟的长间隔停止
噪音消除	用于SCL和SDA信号的数字噪声滤波器 用于通过滤波器消除噪声的可编程窗口。
中断源	传输错误或事件发生（仲裁检测、NACK、超时、启动或重启条件或停止条件） 接收数据已满，包括与从地址匹配 传输数据为空，包括与从地址匹配 传输结束。
Module-stop function	模块停止状态可设置
IIC操作模式	主机发送 主机接收 从机发送 从机接收。

Table 30.1 IIC specifications (2 of 2)

Parameter	Description
Event link function (output)	• Transfer error or event occurrences (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end.
Wakeup function*1	• CPU can return from a Software Standby mode using a wakeup event

Note 1. This function is only available for IIC channel IIC0.

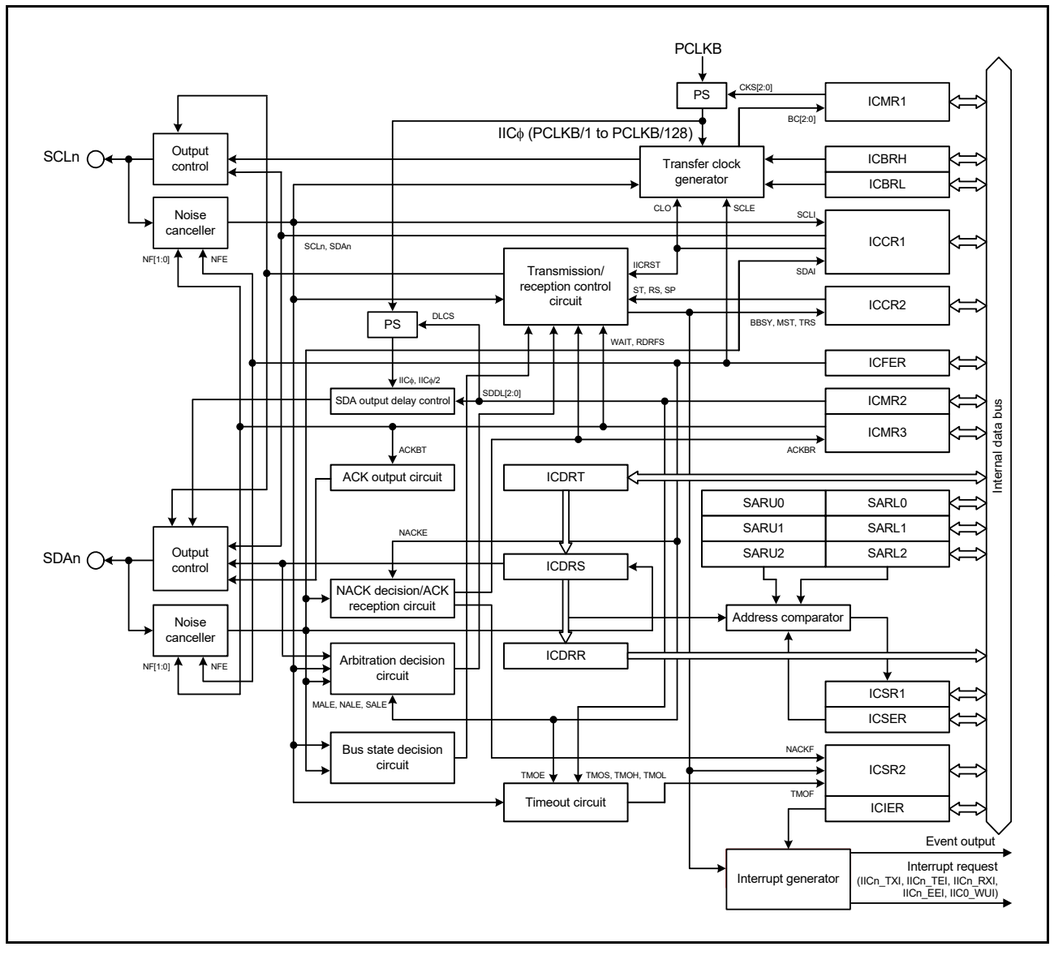


Figure 30.1 IIC block diagram

Table 30.1 IIC规格（2个中的2个）

Parameter	Description
事件链接功能（输出）	传输错误或事件发生（仲裁检测、NACK、超时、启动或重启条件或停止条件） 接收数据已满，包括与从地址匹配 传输数据为空，包括与从地址匹配 传输结束。
Wakeup function*1	CPU可以使用唤醒事件从软件待机模式返回

Note 1. 该功能仅适用于IIC通道IIC0。

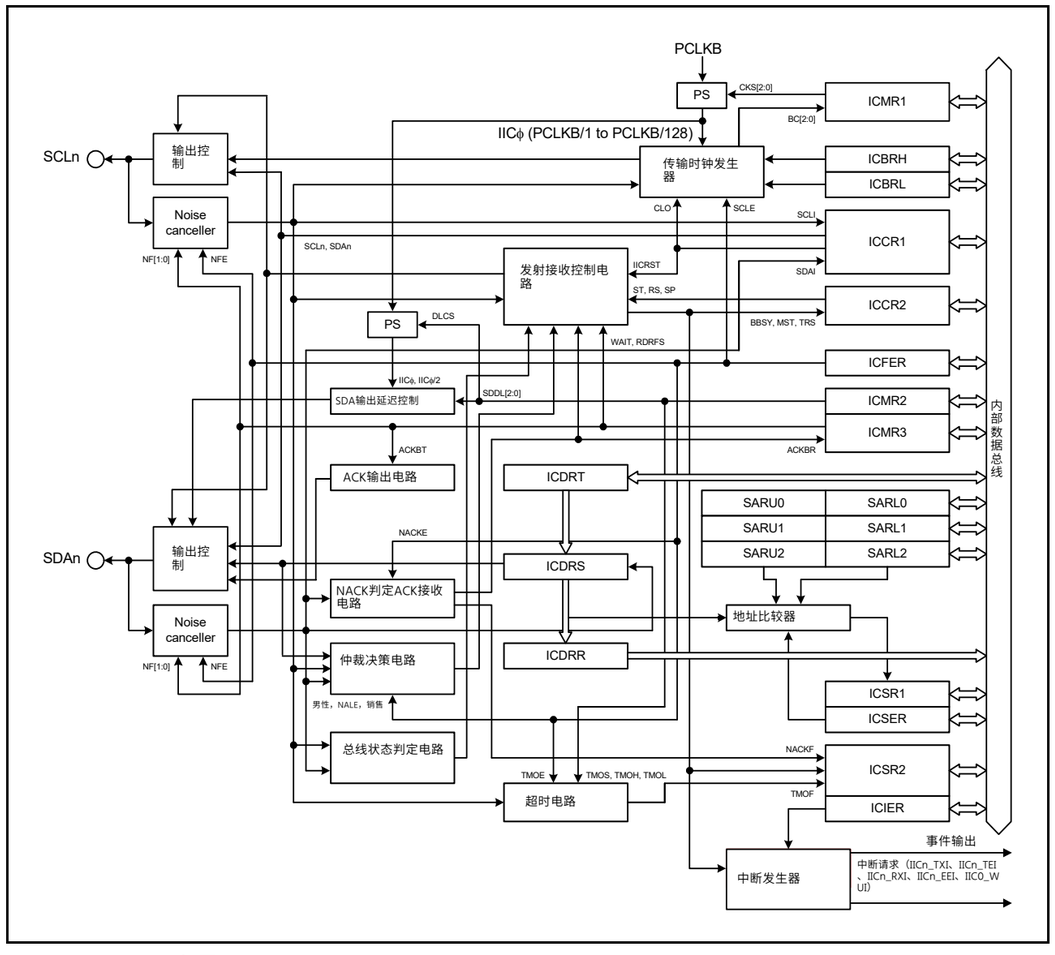


Figure 30.1 IIC框图

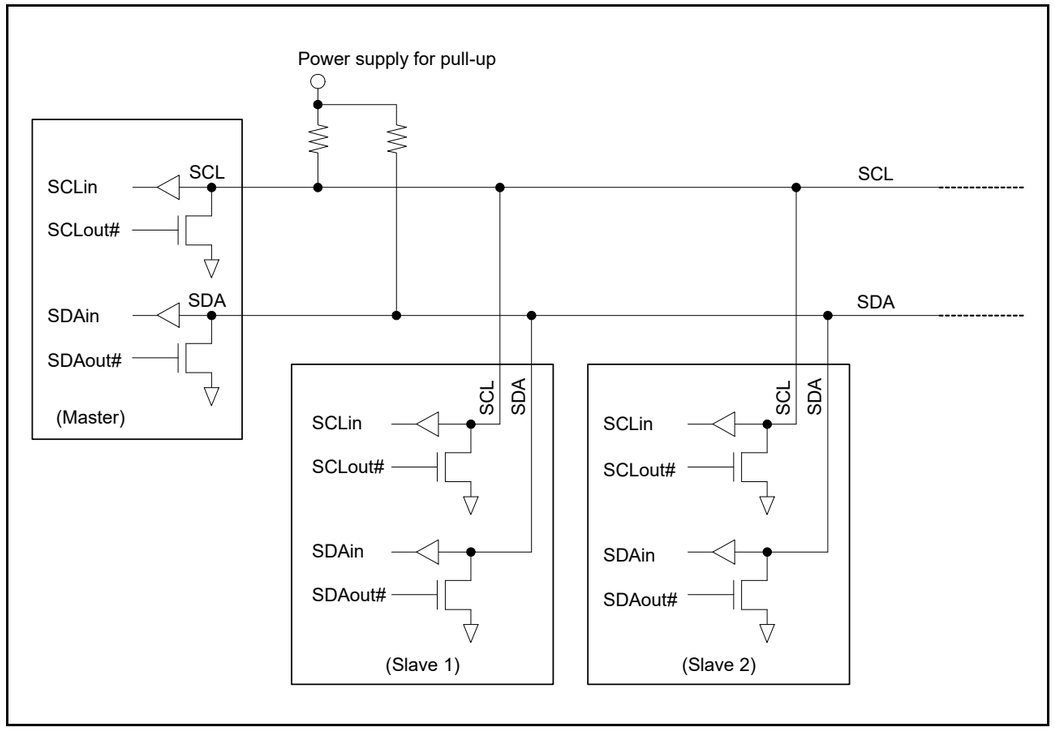


Figure 30.2 I/O pin connection to the external circuit (I2C bus configuration example)

The input level of the signals for IIC is CMOS when I2C bus is selected (ICMR3.SMBS = 0), or TTL when SMBus is selected (ICMR3.SMBS = 1).

Table 30.2 IIC pin configuration

Channel	Pin name	I/O	Function
IIC0	SCL0	I/O	IIC0 serial clock I/O pin
	SDA0	I/O	IIC0 serial data I/O pin
IIC1	SCL1	I/O	IIC1 serial clock I/O pin
	SDA1	I/O	IIC1 serial data I/O pin

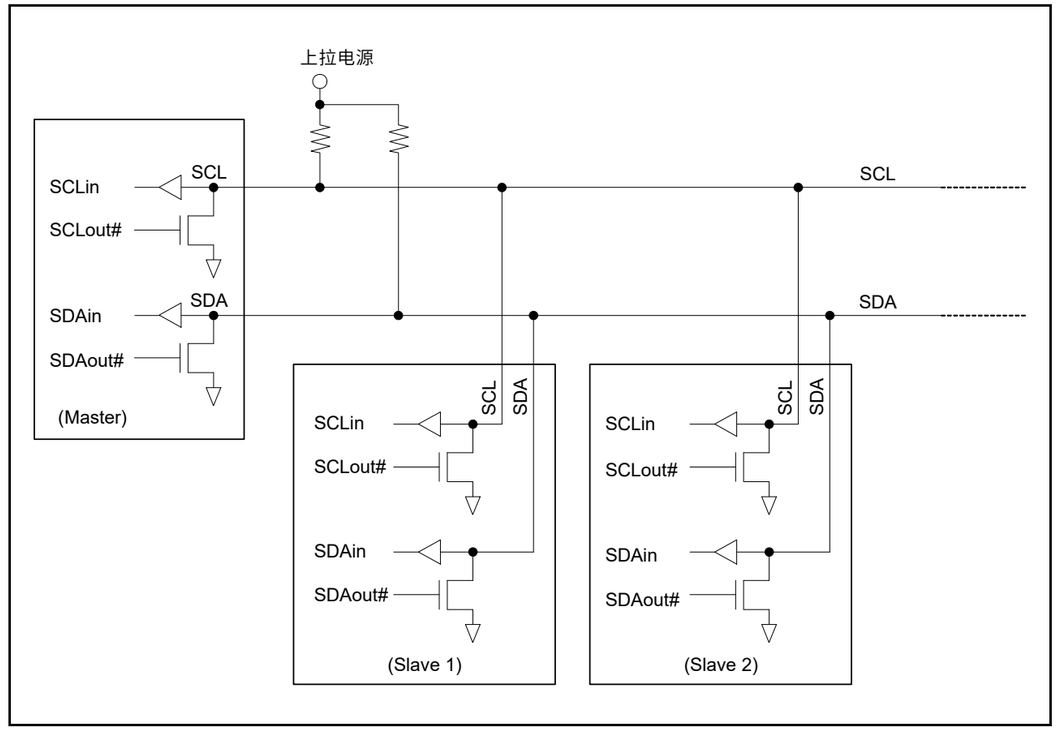


Figure 30.2 IO引脚连接到外部电路（I2C总线配置示例）

TheinputlevelofthesignalsforIICisCMOSwhenI2Cbusisselected(ICMR3.SMBS=0) orTTLwhenSMBusisselected(ICMR3.SMBS=1).

Table 30.2 IIC引脚配置

Channel	引脚名称	I/O	Function
IIC0	SCL0	I/O	IIC0串行时钟IO引脚
	SDA0	I/O	IIC0串行数据IO引脚
IIC1	SCL1	I/O	IIC1串行时钟IO引脚
	SDA1	I/O	IIC1串行数据IO引脚

30.2 Register Descriptions

30.2.1 I2C Bus Control Register 1 (ICCR1)

Address(es): IIC0.ICCR1 4005 3000h, IIC1.ICCR1 4005 3100h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is low 1: SDAn line is high.	R
b1	SCLI	SCL Line Monitor	0: SCLn line is low 1: SCLn line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: IIC drives the SDAn pin low 1: IIC releases the SDAn pin. • Write: 0: IIC drives SDAn pin low 1: IIC releases SDAn pin.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: IIC drives the SCLn pin low 1: IIC releases the SCLn pin. • Write: 0: IIC drives SCLn pin low 1: IIC releases SCLn pin. Use an external pull-up resistor to drive the signal high.	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Write enable SCLO and SDAO bits 1: Write protect SCLO and SDAO bits. This bit is read as 1.	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Do not output extra SCL clock cycle (default) 1: Output extra SCL clock cycle. This bit clears automatically after 1 clock cycle is output.	R/W
b6	IICRST	IIC Bus Interface Internal Reset	0: Release IIC reset or internal reset 1: Initiate IIC reset or internal reset. This clears the bit counter and the SCLn/SDAn output latch.	R/W
b7	ICE	IIC Bus Interface Enable	0: Disable (SCLn and SDAn pins in inactive state) 1: Enable (SCLn and SDAn pins in active state). Used in combination with the IICRST bit to select either IIC or internal reset.	R/W

SDAO bit (SDA Output Control/Monitor) and SCLO bit (SCL Output Control/Monitor)

The SDAO and SCLO bits directly control the SDAn and SCLn signals output from the IIC.

When writing to these bits, also write 0 to the SOWP bit. Setting these bits results in input to the IIC by the input buffer. When slave mode is selected, a start condition might be detected and the bus might be released depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, or during transmission or reception. Operation after rewriting under the specified conditions is not guaranteed. When reading these bits, the state of signals output from the IIC can be read.

CLO bit (Extra SCL Clock Cycle Output)

The CLO bit allows output of an extra SCL clock cycle for debugging or error processing.

Normally, set this bit to 0. Setting this bit to 1 in a normal communication state causes a communication error. For details on this function, see section 30.12.2, Extra SCL Clock Cycle Output Function.

30.2 注册说明

30.2.1 I2C总线控制寄存器1(ICCR1)

Address(es): IIC0.ICCR1 4005 3000h, IIC1.ICCR1 4005 3100h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
重置后的值:	0	0	0	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	SDAI	SDA线路监视器	0：SDAn线为低电平1 ：SDAn线为高电平。	R
b1	SCLI	SCL线路监视器	0：SCLn线低1：SC Ln线高。	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0：IIC将SDAn引脚驱动为低电 平1：IIC释放SDAn引脚。 写： 0：IIC驱动SDAn引脚为低电平 1：IIC释放SDAn引脚。	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0：IIC将SCLn引脚驱动为低电平 1：IIC释放SCLn引脚。 写： 0：IIC驱动SCLn引脚为低电平1：IIC释放SCLn引脚。使 用外部上拉电阻将信号驱动为高电平。	R/W
b4	SOWP	SCLOSDAO写保护	0：写使能SCLO和SDAO位1：写保护S CLO和SDAO位。该位读为1。	R/W
b5	CLO	额外的SCL时钟周期输出	0：不输出额外的SCL时钟周期（默认）1：输出额外的S CL时钟周期。该位在输出1个时钟周期后自动清零。	R/W
b6	IICRST	IIC总线接口内部复位	0：释放IIC复位或内部复位1：启动IIC复位或内部复位。这 将清除位计数器和SCLnSDAn输出锁存器。	R/W
b7	ICE	IIC总线接口使能	0：禁用（SCLn和SDAn引脚处于非活动状态）1：启用（SCLn 和SDAn引脚处于活动状态）。与IICRST位结合使用来选择IIC或 内部复位。	R/W

SDAO位（SDA输出控制监视器）和SCLO位（SCL输出控制监视器）

SDAO和SCLO位直接控制IIC输出的SDAn和SCLn信号。

写入这些位时，还要向SOWP位写入0。设置这些位会导致输入缓冲器向IIC输入。
选择从模式时，可能会检测到启动条件，并且可能会根据位设置释放总线。

请勿在开始条件、停止条件、重启条件或发送或接收期间重写这些位。不保证在指定条件下重写后的操作。
读取这些位时，可以读取IIC输出的信号状态。

CLO位（额外SCL时钟周期输出）

CLO位允许输出额外的SCL时钟周期用于调试或错误处理。

通常，将此位设置为0。在正常通信状态下将此位设置为1会导致通信错误。有关此功能的详细信息，请参见第30.12.2节，额外SCL时钟周期输出功能。

IICRST bit (IIC Bus Interface Internal Reset)

The IICRST bit initiates an internal state reset of the IIC. Setting this bit to 1 initiates an IIC reset or internal reset. Whether an IIC reset or internal reset is initiated is determined by setting this bit in combination with the ICE bit. Table 30.3 lists the IIC resets.

The IIC reset initializes all registers except ICCR1.ICE and ICCR1.ICCRST bits and internal states of the IIC.

The internal reset initializes the following:

- Bit counter (ICMR1.BC[2:0] bits)
- I2C Bus Shift Register (ICDRS)
- I2C Bus Status Registers (ICSR1 and ICSR2)
- SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits)
- I2C Bus Control Register 2 (except ICCR2.BBSY bit).

For the reset conditions of each register, see section 30.15, State of Registers when Issuing each Condition.

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the IIC without initializing the port settings and the control and setting registers of the IIC. If the IIC hangs up in a low-level output state, resetting the internal states cancels the low-level output state and releases the bus with the SCLn pin and SDAn pin at high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up that occurs during communication with the master device in slave mode, the slave and the master devices might enter different states, because the bit counter information differs. For this reason, do not initiate an internal reset in slave mode. Initiate recovery processing from the master device. If an internal reset is required because the IIC hangs with the SCLn line in a low-level output state in slave mode, initiate an internal reset, and then issue a restart condition from the master device or issue a stop condition and resume communication from the start condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start condition or restart condition from the master device, synchronization is lost because the master and slave devices operate asynchronously.

Table 30.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	Resets all registers except ICCR1.ICE and ICCR1.ICCRST bits, and internal states of the IIC
	1	Internal reset	Resets the following: • ICMR1.BC[2:0] bits • ICSR1 register • ICSR2 register • ICDRS register • ICCR1.SCLO bit • ICCR1.SDAO bit • ICCR2 register (except ICCR2.BBSY bit) • internal states of the IIC.

ICE bit (IIC Bus Interface Enable)

The ICE bit selects the active or inactive state of the SCLn and SDAn pins. It can also be combined with the IICRST bit to initiate one of the two resets. See Table 30.3 for the reset types.

Set the ICE bit to 1 when using the IIC. The SCLn and SDAn pins are placed in the active state when the ICE bit is set to 1. Set the ICE bit to 0 when the IIC is not used. The SCLn and SDAn pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCLn or SDAn pin to the IIC when setting up the pin function control. Slave address comparison is performed if the pins are assigned to the IIC.

IICRST位（IIC总线接口内部复位）

IICRST位启动IIC的内部状态复位。将此位设置为1会启动IIC复位或内部复位。
是否启动IIC复位或内部复位由设置该位和ICE位共同决定。表30.3列出了IIC复位。

IIC复位初始化除ICCR1.ICE和ICCR1.ICCRST位和IIC内部状态之外的所有寄存器。

内部复位初始化以下内容：

- 位计数器（ICMR1.BC[2:0]位）
- I2C总线移位寄存器(ICDRS)
- I2C总线状态寄存器（ICSR1和ICSR2）
- SDAO和SCLO输出控制监视器（ICCR1.SCLO和ICCR1.SDAO位）
- I2C总线控制寄存器2（ICCR2.BBSY位除外）。

有关每个寄存器的复位条件，请参阅第30.15节，发出每个条件时的寄存器状态。

在操作期间将IICRST位设置为1（ICE位设置为1）启动的内部复位会复位IIC的内部状态，而无需初始化IIC的端口设置以及控制和设置寄存器。如果IIC在低电平输出状态下挂起，复位内部状态会取消低电平输出状态并释放总线，同时SCLn引脚和SDAn引脚处于高阻抗状态。

Note: 如果在从模式下与主设备通信期间发生的总线挂断使用IICRST位启动内部复位，则从设备和主设备可能进入不同的状态，因为位计数器信息不同。因此，不要在从模式下启动内部复位。从主设备启动恢复处理。如果由于IIC在从模式下挂起且SCLn线处于低电平输出状态而需要内部复位，则启动内部复位，然后从主设备发出重启条件或发出停止条件并从主设备恢复通信开始条件。如果在没有从主设备发出启动条件或重新启动条件的情况下，通过仅在从设备中启动复位来重新启动通信，则由于主设备和从设备异步操作而失去同步。

Table 30.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	复位除ICCR1.ICE和ICCR1.ICCRST位之外的所有寄存器，以及内部状态IIC
	1	内部复位	复位以下内容： ICMR1.BC[2:0]位 ICSR1寄存器 ICSR2寄存器 ICDRS寄存器 ICCR1.SCLO位 ICCR1.SDAO位 ICCR2寄存器（ICCR2.BBSY位除外） IIC的内部状态。

ICE位（IIC总线接口使能）

ICE位选择SCLn和SDAn引脚的有效或无效状态。它也可以与IICRST位组合以启动两个复位之一。复位类型见表30.3。

使用IIC时将ICE位设置为1。当ICE位设置为1时，SCLn和SDAn引脚处于活动状态。不使用IIC时，将ICE位设置为0。当ICE位设置为0时，SCLn和SDAn引脚处于无效状态。在设置引脚功能控制时，不要将SCLn或SDAn引脚分配给IIC。如果引脚分配给IIC，则执行从地址比较。

30.2.2 I2C Bus Control Register 2 (ICCR2)

Address(es): IIC0.ICCR2 4005 3001h, IIC1.ICCR2 4005 3101h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Do not issue a start condition request 1: Issue a start condition request.	R/W
b2	RS	Restart Condition Issuance Request	0: Do not issue a restart condition request 1: Issue a restart condition request.	R/W
b3	SP	Stop Condition Issuance Request	0: Do not issue a stop condition request 1: Issue a stop condition request.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	TRS	Transmit/Receive Mode	0: Receive mode 1: Transmit mode.	R/W*1
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode.	R/W*1
b7	BBSY	Bus Busy Detection Flag	0: I2C bus released (bus free state) 1: I2C bus occupied (bus busy state).	R

Note 1. The MST and TRS bits can be written to when the ICMR1.MTWP bit is set to 1.

ST bit (Start Condition Issuance Request)

The ST bit requests transition to master mode and issues a start condition.

When this bit is set to 1, a start condition is issued when the BBSY flag is set to 0 (bus free state). For details on issuing a start condition, see section 30.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit.

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Only set the ST bit to 1 (start condition request) when the BBSY flag is set to 0 (bus free state). Arbitration might be lost if the ST bit is set to 1 (start condition request) when the BBSY flag is 1 (bus busy state).

RS bit (Restart Condition Issuance Request)

The RS bit requests that a restart condition be issued in master mode.

When this bit is set to 1 to request a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on issuing a restart condition, see section 30.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1.

30.2.2 I2C总线控制寄存器2(ICCR2)

Address(es): IIC0.ICCR2 4005 3001h, IIC1.ICCR2 4005 3101h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	ST	开始条件签发 Request	0：不发出启动条件请求1：发出启动条件请求。	R/W
b2	RS	重启条件发布 Request	0：不发出重启条件请求1：发出重启条件请求。	R/W
b3	SP	停止条件发布 Request	0：不发出停止条件请求1：发出停止条件请求。	R/W
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	TRS	Transmit/Receive Mode	0：接收模式1：发送模式。	R/W*1
b6	MST	Master/Slave Mode	0：从模式1：主模式。	R/W*1
b7	BBSY	总线忙检测标志	0：I2C总线释放（总线空闲状态）1：I2C总线占用（总线忙状态）。	R

Note 1. 当ICMR1.MTWP位设置为1时，可以写入MST和TRS位。

ST位（开始条件发布请求）

ST位请求转换到主机模式并发出启动条件。

当该位设置为1时，当BBSY标志设置为0（总线空闲状态）时发出启动条件。有关发出启动条件的详细信息，请参阅第30.11节，启动、重启和停止条件发出功能。

[Setting condition]

- 当1写入ST位时。

[Clearing conditions]

- 当0写入ST位时
- 发出启动条件时（检测到启动条件）
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Note: 仅当BBSY标志设置为0（总线空闲状态）时，才将ST位设置为1（启动条件请求）。如果在BBSY标志为1（总线繁忙状态）时将ST位设置为1（开始条件请求），则仲裁可能会丢失。

RS位（重启条件发布请求）

RS位请求在主机模式下发出重启条件。

当该位设置为1以请求重新启动条件时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出重新启动条件。有关发出重启条件的详细信息，请参阅第30.11节"启动、重启和停止条件发出功能"。

[Setting condition]

- 当ICCR2中的BBSY标志设置为1时，将1写入RS位。

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (restart condition request) is written to the RS bit in slave mode, the restart condition is not issued but the RS bit remains set to 1. If the operating mode changes to master mode without the RS bit being cleared, the restart condition might be issued.

SP bit (Stop Condition Issuance Request)

The SP bit requests that a stop condition be issued in master mode.

When this bit is set to 1, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on issuing a stop condition, see section 30.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition is issued (a stop condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Note: Writing to the SP bit is not possible while the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 while a restart condition is being issued.

TRS bit (Transmit/Receive Mode)

The TRS bit indicates transmit or receive mode.

The IIC is in receive mode when the TRS bit is set to 0 and in transmit mode when the TRS bit is set to 1. The combination of the TRS bit and the MST bit indicates the IIC operating mode.

The value of the TRS bit automatically changes to 1 for transmit mode or 0 for receive mode when a start condition is issued or detected and the R/W# bit is set. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to the TRS bit is not required during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally because of a restart condition request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit appended to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected

[Clearing conditions]

- 当0写入RS位时
- 发出重新启动条件时（检测到启动条件）
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

Note: 发出停止条件时不要将RS位设置为1。
Note: 如果在从模式下将1（重新启动条件请求）写入RS位，则不发出重新启动条件，但RS位保持设置为1。如果在RS位未清除的情况下工作模式变为主模式，则重新启动条件可能会发出。

SP位（停止条件发出请求）

SP位请求在主机模式下发出停止条件。

当该位设置为1时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出停止条件。有关发出停止条件的详细信息，请参阅第30.11节"启动、重启和停止条件发出功能"。

[Setting condition]

- 当1写入SP位时，且ICCR2中的BBSY标志和MST位都设置为1。

[Clearing conditions]

- 当0写入SP位时
- 发出停止条件时（检测到停止条件）
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当检测到启动条件和重新启动条件时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

Note: 当BBSY标志为0（总线空闲状态）时，不能写入SP位。
Note: 发出重启条件时不要将SP位设置为1。

TRS位（发送接收模式）

TRS位指示发送或接收模式。

当TRS位设置为0时，IIC处于接收模式；当TRS位设置为1时，IIC处于发送模式。TRS位和MST位的组合表示IIC工作模式。

当发出或检测到启动条件并且设置RW#位时，TRS位的值自动更改为1（发送模式）或0（接收模式）。虽然当ICMR1的MTWP位设置为1时可以写入TRS位，但在正常使用期间不需要写入TRS位。

[Setting conditions]

- 由于启动条件请求而正常发出启动条件时（在ST位设置为1的情况下检测到启动条件时）
- 由于重新启动条件请求而正常发出重新启动条件时（在RS位设置为1的情况下检测到重新启动条件时）
- 当附加到从地址的RW#位在主模式下设置为0时
- 当从机模式接收到的地址与ICSER中使能的地址匹配时，RW#位设置为1
- 当将1写入TRS位且ICMR1中的MTWP位设置为1时。

[Clearing conditions]

- 检测到停止条件时

- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When the R/W# bit appended to the slave address is set to 1 in master mode
- In slave mode, on a match between the received address and the address enabled in ICSER when the value of the received R/W# bit is 0, including when the received address is the general call address
- In slave mode, when a restart condition is detected (a start condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

MST bit (Master/Slave Mode)

The MST bit indicates master or slave mode.

The IIC is in slave mode when the MST bit is set to 0 and is in master mode when the MST bit is set to 1. The combination of the MST bit and the TRS bit indicates the operating mode of the IIC.

The value of the MST bit automatically changes to 1 for master mode or 0 for slave mode when a start condition is issued or when a stop condition is issued or detected. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to the MST bit is not required during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

BBSY flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I2C bus is occupied (bus busy state) or released (bus free state).

This flag is set to 1 when the SDAn line changes from high to low with the SCLn line high, assuming that a start condition was issued.

This flag is set to 0 when the SDAn line changes from low to high with the SCLn line high, if the bus free time (ICBRL setting) start condition is not detected, assuming that a stop condition was issued.

[Setting condition]

- When a start condition is detected.

[Clearing conditions]

- When the bus free time (ICBRL setting) start condition is not detected after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (IIC reset).

- ICSR2中的AL（仲裁失败）标志设置为1时
- 当附加到从地址的RW#位在主模式下设置为1时
- 在从机模式下，当接收到的RW#位的值为0时，接收到的地址与ICSER中使能的地址匹配，包括接收到的地址是广播地址时
- 在从模式下，当检测到重启条件时（检测到ICCR2.BBSY=1和ICCR2.MST = 0)
- 当将0写入TRS位且ICMR1中的MTWP位设置为1时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

MST位（主从模式）

MST位指示主机或从机模式。

当MST位设置为0时，IIC处于从机模式，当MST位设置为1时，IIC处于主机模式。MST位和TRS位的组合指示IIC的工作模式。

当发出启动条件或发出或检测到停止条件时，MST位的值自动变为1（主机模式）或0（从机模式）。虽然当ICMR1的MTWP位设置为1时可以写入MST位，但在正常使用期间不需要写入MST位。

[Setting conditions]

- 由于启动条件请求而正常发出启动条件时（在ST位设置为1的情况下检测到启动条件时）
- 当ICMR1中的MTWP位设置为1时，将1写入MST位。

[Clearing conditions]

- 检测到停止条件时
- ICSR2中的AL（仲裁失败）标志设置为1时
- 将0写入MST位且ICMR1中的MTWP位设置为1时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

BBSY标志（总线忙检测标志）

BBSY标志指示I2C总线是被占用（总线繁忙状态）还是被释放（总线空闲状态）。

当SDAn线从高电平变为低电平且SCLn线为高电平时，该标志设置为1，假设发出了启动条件。

如果未检测到总线空闲时间（ICBRL设置）启动条件，假设发出了停止条件，则当SDAn线从低电平变为高电平且SCLn线为高电平时，该标志设置为0。

[Setting condition]

- 当检测到启动条件时。

[Clearing conditions]

- 检测到停止条件后未检测到总线空闲时间（ICBRL设置）启动条件时
- 当ICCR1中的IICRST位写入1且ICCR1中的ICE位设置为0时（IIC复位）。

30.2.3 I2C Bus Mode Register 1 (ICMR1)

Address(es): IIC0.ICMR1 4005 3002h, IIC1.ICMR1 4005 3102h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits.	R/W*1
b3	BCWP	BC Write Protect	0: Write enable BC[2:0] bits. 1: Write protect BC[2:0] bits. This bit is read as 1.	R/W*1
b6 to b4	CKS[2:0]	Internal Reference Clock Select	Select the internal reference clock source (IICϕ) for the IIC. b6 b4 0 0 0: PCLKB clock 0 0 1: PCLKB/2 clock 0 1 0: PCLKB/4 clock 0 1 1: PCLKB/8 clock 1 0 0: PCLKB/16 clock 1 0 1: PCLKB/32 clock 1 1 0: PCLKB/64 clock 1 1 1: PCLKB/128 clock.	R/W
b7	MTWP	MST/TRS Write Protect	0: Write protect MST and TRS bits in ICCR2 1: Write enable MST and TRS bits in ICCR2.	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

BC[2:0] bits (Bit Counter)

The BC[2:0] bits function as a counter that indicates the number of bits remaining to be transferred on detection of a rising edge on the SCLn line. Although the BC[2:0] bits are writable and readable, it is not required to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one for an additional acknowledge bit, between transferred frames when the SCLn line is at a low level.

The values of the BC[2:0] bits return to 000b at the end of a data transfer, including the acknowledge bit, or when a start or restart condition is detected.

30.2.3 I2C总线模式寄存器1(ICMR1)

Address(es): IIC0.ICMR1 4005 3002h, IIC1.ICMR1 4005 3102h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
重置后的值:	0	0	0	0	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	BC[2:0]	位计数器	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits.	R/W*1
b3	BCWP	BC写保护	0：写使能BC[2:0]位。1：写保护BC[2:0]位。该位读为1。	R/W*1
b6 to b4	CKS[2:0]	内部参考时钟选择	选择IIC的内部参考时钟源(IIC)。b6b4000：PCLKB时钟001：PCLKB2时钟010：PCLKB4时钟011：PCLKB8时钟100：PCLKB16时钟101：PCLKB32时钟110：PCLKB64时钟111：PCLKB128时钟。	R/W
b7	MTWP	MSTTRS写保护	0：写保护ICCR2中的MST和TRS位1：写使能ICCR2中的MST和TRS位。	R/W

Note 1. 重写BC[2:0]位，同时将BCWP位设置为0。

BC[2:0]位（位计数器）

BC[2:0]位用作计数器，指示在检测到SCLn线上的上升沿时要传输的剩余位数。虽然BC[2:0]位是可写和可读的，但在正常情况下不需要访问这些位。

要写入这些位，当SCLn线处于低电平时，在传输的帧之间指定要传输的位数加一作为附加确认位。

BC[2:0]位的值在数据传输结束时返回到000b，包括确认位，或者当检测到启动或重启条件时。

30.2.4 I2C Bus Mode Register 2 (ICMR2)

Address(es): IIC0.ICMR2 4005 3003h, IIC1.ICMR2 4005 3103h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOS	Timeout Detection Time Select	0: Select long mode 1: Select short mode.	R/W
b1	TMOL	Timeout L Count Control	0: Disable count while the SCLn line is low 1: Enable count while the SCLn line is low.	R/W
b2	TMOH	Timeout H Count Control	0: Disable count while the SCLn line is high 1: Enable count while the SCLn line is high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS = 0 (IICϕ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICϕ cycle 0 1 0: 2 IICϕ cycles 0 1 1: 3 IICϕ cycles 1 0 0: 4 IICϕ cycles 1 0 1: 5 IICϕ cycles 1 1 0: 6 IICϕ cycles 1 1 1: 7 IICϕ cycles. • When ICMR2.DLCS = 1 (IICϕ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICϕ cycles 0 1 0: 3 or 4 IICϕ cycles 0 1 1: 5 or 6 IICϕ cycles 1 0 0: 7 or 8 IICϕ cycles 1 0 1: 9 or 10 IICϕ cycles 1 1 0: 11 or 12 IICϕ cycles 1 1 1: 13 or 14 IICϕ cycles.	R/W
b7	DLCS	SDA Output Delay Clock Source Select	0: Internal reference clock (IICϕ) selected as the clock source for the SDA output delay counter 1: Internal reference clock divided by 2 (IICϕ/2) selected as the clock source for the SDA output delay counter.*1	R/W

Note 1. The setting DLCS = 1 (IICϕ/2) is only valid when SCL is low. When SCL is high, the setting DLCS = 1 is invalid and the clock source becomes the internal reference clock (IICϕ).

TMOS bit (Timeout Detection Time Select)

The TMOS bit selects long mode or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE bit = 1). When this bit is set to 0, long mode is selected. When the TMOS bit is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16-bit counter. In short mode, the counter functions as a 14-bit counter. While the SCLn line is in the state that enables this counter as specified in the TMOH and TMOL bits, the counter counts up in synchronization with the internal reference clock (IICϕ) as a count source.

For details on the timeout function, see section 30.12.1, Timeout Function.

TMOL bit (Timeout L Count Control)

The TMOL bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held low and the timeout function is enabled (ICFER.TMOE bit = 1).

TMOH bit (Timeout H Count Control)

The TMOH bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is

30.2.4 I2C总线模式寄存器2(ICMR2)

Address(es): IIC0.ICMR2 4005 3003h, IIC1.ICMR2 4005 3103h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
重置后的值:	0	0	0	0	0	1	1	0

Bit	Symbol	位名称	Description	R/W
b0	TMOS	超时检测时间选择	0：选择长模式1：选择短模式。	R/W
b1	TMOL	超时L计数控制	0：SCLn线为低电平时禁止计数1：SCLn线为低电平时使能计数。	R/W
b2	TMOH	超时H计数控制	0：SCLn线为高电平时禁止计数1：SCLn线为高电平时使能计数。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	SDDL[2:0]	SDA输出延迟计数器	当ICMR2.DLCS=0(IIC)b6b4000：无输出延迟001：1IIC 周期010：2IIC 周期011：3IIC 周期100：4IIC 周期101：5IIC 周期110：6IIC 周期111：7IIC 周期。 当ICMR2.DLCS=1(IIC 2)b6b4000：无输出延迟001：1或2个IIC 周期010：3或4个IIC 周期011：5或6个IIC 周期100：7或8个IIC 周期101：9或10个IIC 周期110：11或12个IIC 周期111：13或14个IIC 周期。	R/W
b7	DLCS	SDA输出延迟时钟源Select	0：选择内部参考时钟(IIC)作为SDA输出延迟计数器的时钟源1：选择内部参考时钟除以2(IIC 2)作为SDA输出延迟计数器的时钟源。*1	R/W

Note 1. 设置DLCS=1(IIC 2)仅在SCL为低电平时有效。当SCL为高电平时，设置DLCS=1无效，时钟源变为内部参考时钟(IIC)。

TMOS位（超时检测时间选择）

当使能超时功能（ICFER.TMOE位=1）时，TMOS位为超时检测时间选择长模式或短模式。当该位设置为0时，选择长模式。当TMOS位设置为1时，选择短模式。在长模式下，超时检测内部计数器用作16位计数器。在短模式下，计数器用作14位计数器。当SCLn线处于启用TMOH和TMOL位中指定的计数器的状态时，计数器与作为计数源的内部参考时钟(IIC)同步递增计数。

关于超时功能的详细信息，请参见第30.12.1节，超时功能。

TMOL位（超时L计数控制）

TMOL位启用或禁用超时功能内部计数器的递增计数，同时SCLn线保持低电平且启用超时功能（ICFER.TMOE位=1）。

TMOH位（超时H计数控制）

TMOH位启用或禁用超时功能的内部计数器的向上计数，而SCLn线是

held high and the timeout function is enabled (ICFER.TMOE bit = 1).

SDDL[2:0] bits (SDA Output Delay Counter)

The SDDL[2:0] bits can be used to delay the SDA output. This counter works with the clock source selected by the DLCS bit. The SDDL[2:0] setting can be used for all types of SDA output, including the transmission of the acknowledge bit.

Set the SDA output delay time to meet the I2C bus standard for the data enable time/acknowledge enable time*1, or the SMBus standard, within [data hold time (300 ns or more + the SCL clock low-level period) - the data setup time (250 ns)]. If a value outside the standard is set, communication between devices might malfunction or falsely indicate a start or stop condition, depending on the bus state.

For details on this function, see section 30.5, SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time
3,450 ns for up to 100 kbps: Standard-mode (Sm)
900 ns for up to 400 kbps: Fast-mode (Fm)

30.2.5 I2C Bus Mode Register 3 (ICMR3)

Address(es): IIC0.ICMR3 4005 3004h, IIC1.ICMR3 4005 3104h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Select	b1 b0 0 0: Noise of up to 1 IICϕ cycle filtered out (single-stage filter) 0 1: Noise of up to 2 IICϕ cycles filtered out (2-stage filter) 1 0: Noise of up to 3 IICϕ cycles filtered out (3-stage filter) 1 1: Noise of up to 4 IICϕ cycles filtered out (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: 0 Received as the acknowledge bit (ACK reception) 1: 1 Received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: 0 Sent as the acknowledge bit (ACK transmission) 1: 1 Sent as the acknowledge bit (NACK transmission).	R/W*1
b4	ACKWP	ACKBT Write Protect	0: Write protect the ACKBT bit 1: Write enable the ACKBT bit.	R/W*1
b5	RDRFS	RDRF Flag Set Timing Select	0: Set the RDRF flag on the rising edge of the 9th SCL clock cycle. The SCLn line is not held low on the falling edge of the 8th clock cycle. 1: Set the RDRF flag on the rising edge of the 8th SCL clock cycle. The SCLn line is held low on the falling edge of the 8th clock cycle. Low-hold is released by writing to ACKBT.	R/W*2
b6	WAIT	WAIT	0: No WAIT SCLn is not held low during the period between 9th clock cycle and 1st clock cycle 1: WAIT SCLn is held low during the period between 9th clock cycle and 1st clock cycle. Low-hold is released by reading ICDRR.	R/W*2
b7	SMBS	SMBus/I2C Bus Select	0: I2C bus is selected 1: SMBus is selected.	R/W

Note 1. Write to the ACKBT bit only when the ACKWP bit is already 1. If software writes 1 to both the ACKWP and ACKBT bits at the same time, the ACKBT bit is not set to 1.
Note 2. The WAIT and RDRFS bits are valid only in receive mode (invalid in transmit mode).

保持高电平并启用超时功能（ICFER.TMOE位=1）。

SDDL[2:0]位（SDA输出延迟计数器）

SDDL[2:0]位可用于延迟SDA输出。该计数器使用由选择的时钟源
DLCS位。SDDL[2:0]设置可用于所有类型的SDA输出，包括确认位的传输。

设置SDA输出延迟时间以满足I2C总线标准为数据使能时间确认使能时间*1，或SMBus标准，在[数据保持时间（300ns或更长+SCL时钟低电平周期）内数据建立时间（250ns）]。如果设置了超出标准的值，则设备之间的通信可能会发生故障或错误地指示开始或停止条件，具体取决于总线状态。

有关此功能的详细信息，请参阅第30.5节，SDA输出延迟功能。

注1.数据使能时间确认使能时间
3 450ns，最高100kbps：标准模式(Sm)900ns，
最高400kbps：快速模式(Fm)

30.2.5 I2C总线模式寄存器3(ICMR3)

Address(es): IIC0.ICMR3 4005 3004h, IIC1.ICMR3 4005 3104h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	NF[1:0]	噪声过滤级选择	b1b000：最多过滤掉1个IIC 周期的噪声（单级滤波器）01：最多过滤掉2个IIC 周期的噪声（2级滤波器）10：最多3个IIC 的噪声过滤掉的周期（3级滤波器）11：过滤掉最多4个IIC 周期的噪声（4级滤波器）。	R/W
b2	ACKBR	接收确认	0：0作为确认位接收（ACK接收）1：1作为确认位接收（NACK接收）。	R
b3	ACKBT	发送确认	0：0作为确认位发送（ACK发送）1：1作为确认位发送（NACK发送）。	R/W*1
b4	ACKWP	ACKBT写保护	0：ACKBT位写保护1：ACKBT位写使能。	R/W*1
b5	RDRFS	RDRF标志设置时序Select	0：在第9个SCL时钟周期的上升沿设置RDRF标志。SCLn线在第8个时钟周期的下降沿不保持低电平。1：在第8个SCL时钟周期的上升沿设置RDRF标志。SCLn线在第8个时钟周期的下降沿保持低电平。 通过写入ACKBT释放低保持。	R/W*2
b6	WAIT	WAIT	0：不等待 SCLn在第9个时钟周期和第1个时钟周期之间不保持低电平1：WAIT SCLn在第9个时钟周期和第1个时钟周期之间保持低电平。通过读取ICDRR释放低保持。	R/W*2
b7	SMBS	SMBusI2C总线选择	0：选择I2C总线1：选择SMBus。	R/W

Note 1. 仅当ACKWP位已经为1时才写入ACKBT位。如果软件同时向ACKWP和ACKBT位写入1，则ACKBT位不会设置为1。

Note 2. WAIT和RDRFS位仅在接收模式下有效（在发送模式下无效）。

NF[1:0] bits (Noise Filter Stage Select)

The NF[1:0] bits select the number of stages in the digital noise filter.

For details on the digital noise filter function, see section 30.6, Digital Noise Filter Circuits.

Note: Set the noise range to be filtered within a range less than the SCLn line high-level period or low-level period. If the noise range is set to a value of [SCL clock width: high-level period or low-level period, whichever is shorter] - [1.5 internal reference clock (IICϕ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise by the noise filter function of the IIC, which might prevent the IIC from operating normally.

ACKBR bit (Receive Acknowledge)

The ACKBR bit stores the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKBT bit (Transmit Acknowledge)

The ACKBT bit controls the value of the acknowledge bit to be sent in receive mode.

[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1.

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition issue is detected with the SP bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKWP bit (ACKBT Write Protect)

The ACKWP bit controls write enabling of the ACKBT bit.

RDRFS bit (RDRF Flag Set Timing Select)

The RDRFS bit selects the RDRF flag set timing in receive mode and also selects whether to hold the SCLn line low on the falling edge of the 8th SCL clock cycle.

When the RDRFS bit is 0, the SCLn line is not held low on the falling edge of the 8th SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

When the RDRFS bit is 1, the SCLn line is held low on the falling edge of the 8th SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the 8th SCL clock cycle. The low-hold of the SCLn line is released by a write to the ACKBT bit.

After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1), based on the receive data.

WAIT bit (WAIT)

The WAIT bit controls whether to hold the period between the 9th SCL clock cycle and the 1st SCL clock cycle low until the receive data buffer (ICDRR) is completely read each time a single-byte of data is received in receive mode.

When the WAIT is 0, the receive operation continues without holding the period between the 9th and the 1st SCL clock cycle low. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.

When the WAIT is 1, the SCLn line is held low from the falling edge of the 9th clock cycle until the ICDRR value is read each time a single-byte of data is received. This enables receive operation in byte units.

NF[1:0]位（噪声滤波器级选择）

NF[1:0]位选择数字噪声滤波器的级数。

有关数字噪声滤波器功能的详细信息，请参见第30.6节"数字噪声滤波器电路"。

Note: 将要过滤的噪声范围设置在小于SCLn线高电平周期或低电平周期的范围内。如果噪声范围设置为[SCL时钟宽度：高电平周期或低电平周期，以较短者为准][1.5内部参考时钟(IIC)周期+模拟噪声滤波器：120ns（参考值）]或以上，SCL时钟会被IIC的噪声过滤功能视为噪声，这可能会导致IIC无法正常工作。

ACKBR位（接收确认）

ACKBR位存储在发送模式下从接收设备接收到的确认位信息。

[Setting condition]

- 当ICCR2中的TRS位设置为1接收到1作为确认位时。

[Clearing conditions]

- 当ICCR2中的TRS位设置为1接收到0作为确认位时
- 当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKBT位（发送确认）

ACKBT位控制要在接收模式下发送的确认位的值。

[Setting condition]

- 当1写入该位且ACKWP位设置为1时。

[Clearing conditions]

- 当0写入该位且ACKWP位设置为1时
- 当ICCR2中的SP位设置为1时检测到停止条件问题
- 当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKWP位（ACKBT写保护）

ACKWP位控制ACKBT位的写使能。

RDRFS位（RDRF标志设置时序选择）

RDRFS位选择接收模式下的RDRF标志设置时序，并选择是否在第8个SCL时钟周期的下降沿保持SCLn线为低电平。

当RDRFS位为0时，SCLn线在第8个SCL时钟周期的下降沿不保持低电平，并且RDRF标志在第9个SCL时钟周期的上升沿设置为1。

当RDRFS位为1时，SCLn线在第8个SCL时钟周期的下降沿保持低电平，并且RDRF标志在第8个SCL时钟周期的上升沿设置为1。SCLn线的低保持通过写ACKBT位来释放。

使用此设置接收数据后，SCLn线在发送确认位之前自动保持低电平。这使处理能够根据接收数据发送ACK(ACKBT=0)或NACK(ACKBT=1)。

等待位（等待）

WAIT位控制是否将第9个SCL时钟周期和第1个SCL时钟周期之间的周期保持为低电平，直到在接收模式下每次接收到一个单字节数据时，接收数据缓冲区(ICDRR)被完全读取。

当WAIT为0时，接收操作继续，而不会将第9个和第1个SCL时钟周期之间的周期保持为低电平。当RDRFS和WAIT位都为0时，双缓冲器使能连续接收操作。

当WAIT为1时，SCLn线从第9个时钟周期的下降沿保持低电平，直到每次接收到一个单字节数据时读取ICDRR值。这启用了以字节为单位的接收操作。

Note: When the WAIT bit value is to be read, be sure to first read the ICDRR.

SMBS bit (SMBus/I2C Bus Select)

Setting the SMBS bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

30.2.6 I2C Bus Function Enable Register (ICFER)

Address(es): IIC0.ICFER 4005 3005h, IIC1.ICFER 4005 3105h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOE	Timeout Function Enable	0: Timeout function disabled 1: Timeout function enabled.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Master arbitration-lost detection disabled. Also disables automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost. 1: Master arbitration-lost detection enabled. Also enables automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost.	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: NACK transmission arbitration-lost detection disabled 1: NACK transmission arbitration-lost detection enabled.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Slave arbitration-lost detection disabled 1: Slave arbitration-lost detection enabled.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Transfer operation not suspended during NACK reception (transfer suspension disabled) 1: Transfer operation suspended during NACK reception (transfer suspension enabled).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: No digital noise filter circuit used 1: A digital noise filter circuit used.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: No SCL synchronous circuit used 1: An SCL synchronous circuit used.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

TMOE bit (Timeout Function Enable)

The TMOE bit enables or disables the timeout function.

For details on the timeout function, see section 30.12.1, Timeout Function.

MALE bit (Master Arbitration-Lost Detection Enable)

The MALE bit specifies whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

The NALE bit specifies whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode, for instance when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with different number of receive bytes.

SALE bit (Slave Arbitration-Lost Detection Enable)

The SALE bit specifies whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode, for example, when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs because of noise.

Note: 当要读取WAIT位值时，请务必先读取ICDRR。

SMBS位（SMBusI2C总线选择）

将SMBS位设置为1可选择SMBus并启用ICSER中的HOAE位。

30.2.6 I2C总线功能使能寄存器(ICFER)

Address(es): IIC0.ICFER 4005 3005h, IIC1.ICFER 4005 3105h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
重置后的值：	0	1	1	1	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	TMOE	超时功能启用	0：禁用超时功能1：启用超时功能。	R/W
b1	MALE	Master Arbitration-Lost检测启用	0：禁用主机仲裁丢失检测。当仲裁丢失时，还禁止自动清除ICCR2中的MST和TRS位。1：使能主机仲裁丢失检测。 当仲裁丢失时，还可以自动清除ICCR2中的MST和TRS位。	R/W
b2	NALE	NACK传输Arbitration-Lost Detection Enable	0：NACK传输仲裁丢失检测禁用1：NACK传输仲裁丢失检测启用。	R/W
b3	SALE	Slave Arbitration-Lost检测启用	0：禁止从机仲裁丢失检测1：使能从机仲裁丢失检测。	R/W
b4	NACKE	NACK接收传输暂停启用	0：NACK接收期间传输操作不暂停（传输暂停禁用）1：NACK接收期间传输操作暂停（传输暂停启用）。	R/W
b5	NFE	数字噪声滤波电路Enable	0：不使用数字噪声滤波电路1：使用数字噪声滤波电路。	R/W
b6	SCLE	SCL同步电路Enable	0：不使用SCL同步电路1：使用SCL同步电路。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

TMOE位（超时功能使能）

TMOE位启用或禁用超时功能。

关于超时功能的详细信息，请参见第30.12.1节，超时功能。

MALE位（主仲裁丢失检测使能）

MALE位指定是否在主机模式下使用仲裁丢失检测功能。通常，将此位设置为1。

NALE位（NACK传输仲裁丢失检测使能）

NALE位指定在接收模式下发送NACK期间检测到ACK时是否导致仲裁丢失，例如，当总线上存在具有相同地址的从设备时，或者当两个或多个主设备同时选择同一个不同编号的从设备时接收字节数。

SALE位（从设备仲裁丢失检测使能）

SALE位指定当在从机发送模式下在总线上检测到与正在发送的值不同的值时，是否导致仲裁丢失，例如，当总线上存在具有相同地址的从机或与发送不匹配时数据的出现是因为噪声。

NACKE bit (NACK Reception Transfer Suspension Enable)

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.

When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended. When the NACKE bit is 0, the next transfer operation continues regardless of the received acknowledge content.

For details on the NACK reception transfer suspension function, see section 30.9.2, NACK Reception Transfer Suspension Function.

SCLE bit (SCL Synchronous Circuit Enable)

The SCLE bit specifies whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCLE bit is set to 0 (no SCL synchronous circuit used), the IIC does not synchronize the SCL clock with the SCL input clock. In this setting, the IIC outputs the SCL clock with the transfer rate set in ICBRH and ICBRL regardless of the SCLn line state. For this reason, if the bus load of the I2C bus line is much larger than the specification value or if the SCL clock output overlaps in multiple masters, a short-cycle SCL clock that does not meet the specification might be output. When no SCL synchronous circuit is used, it also affects the issuing of the start, restart, and stop conditions, and the continuous output of extra SCL clock cycles.

The SCLE bit must not be set to 0 except for checking the output of the set transfer rate.

30.2.7 I2C Bus Status Enable Register (ICSER)

Address(es): IIC0.ICSER 4005 3006h, IIC1.ICSER 4005 3106h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Slave address in SARL0 and SARU0 disabled 1: Slave address in SARL0 and SARU0 enabled.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Slave address in SARL1 and SARU1 disabled 1: Slave address in SARL1 and SARU1 enabled.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Slave address in SARL2 and SARU2 disabled 1: Slave address in SARL2 and SARU2 enabled.	R/W
b3	GCAE	General Call Address Enable	0: General call address detection disabled 1: General call address detection enabled.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device ID Address Detection Enable	0: Device ID address detection disabled 1: Device ID address detection enabled.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOAE	Host Address Enable	0: Host address detection disabled 1: Host address detection enabled.	R/W

SARyE bit (Slave Address Register y Enable) (y = 0 to 2)

The SARyE bit enables or disables the received slave address and the slave address set in SARLy and SARUy.

When the SARyE bit is set to 1, the slave address set in SARLy and SARUy is enabled and is compared with the received slave address. When the SARyE bit is set to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE bit (General Call Address Enable)

The GCAE bit specifies whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

NACKE位（NACK接收传输暂停使能）

NACKE位指定在发送模式下从从设备接收到NACK时是继续还是停止传输操作。通常，将此位设置为1。

当在NACKE位设置为1的情况下接收到NACK时，暂停下一个传输操作。当NACKE位为0时，无论接收到的确认内容如何，　　下一次传输操作都会继续进行。

有关NACK接收传输暂停功能的详细信息，请参阅第30.9.2节，NACK接收传输悬浮功能。

SCLE位（SCL同步电路使能）

SCLE位指定是否将SCL时钟与SCL输入时钟同步。通常，将此位设置为1。

当SCLE位设置为0（不使用SCL同步电路）时，IIC不会将SCL时钟与SCL输入时钟同步。在此设置中，无论SCLn线路状态如何，IIC都以ICBRH和ICBRL中设置的传输速率输出SCL时钟。因此，如果I2C总线的总线负载远大于规格值，或者SCL时钟输出在多个主机中重叠，则可能会输出不符合规格的短周期SCL时钟。当不使用SCL同步电路时，也会影响启动、重启和停止条件的发出，以及额外SCL时钟周期的连续输出。

SCLE位不得设置为0，除非检查设置的传输速率的输出。

30.2.7 I2C总线状态使能寄存器(ICSER)

Address(es): IIC0.ICSER 4005 3006h, IIC1.ICSER 4005 3106h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
重置后的值：	0	0	0	0	1	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	SAR0E	从地址寄存器0使能	0：禁用SARL0和SARU0中的从地址1：启用SARL0和SARU0中的从地址。	R/W
b1	SAR1E	从地址寄存器1使能	0：禁用SARL1和SARU1中的从地址1：启用SARL1和SARU1中的从地址。	R/W
b2	SAR2E	从地址寄存器2使能	0：禁用SARL2和SARU2中的从地址1：启用SARL2和SARU2中的从地址。	R/W
b3	GCAE	广播呼叫地址启用	0：禁止广播呼叫地址检测1：使能广播呼叫地址检测。	R/W
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	DIDE	设备ID地址检测 Enable	0：禁用设备ID地址检测1：启用设备ID地址检测。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	HOAE	主机地址启用	0：禁止主机地址检测1：使能主机地址检测。	R/W

SARyE位（从地址寄存器y使能）（y=0到2）

SARyE位启用或禁用接收到的从机地址和设置在SARLy和SARUy中的从机地址。

当SARyE位设置为1时，设置在SARLy和SARUy中的从机地址被启用，并与接收到的从机地址进行比较。当SARyE位设置为0时，设置在SARLy和SARUy中的从机地址被禁用并被忽略，即使它与接收到的从机地址匹配。

GCAE位（广播呼叫地址使能）

GCAE位指定接收到的广播调用地址（0000000b+0[W]：全0）是否忽略。

When this bit is set to 1, if the received slave address matches the general call address, the IIC recognizes the received slave address as the general call address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs data receive operation. When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE bit (Device ID Address Detection Enable)

The DIDE bit specifies whether to recognize and execute the device ID address when a device ID (1111 100b) is received in the first frame after a start condition or restart condition is detected.

When the DIDE bit is set to 1, if the received first frame matches the device ID, the IIC recognizes that the device ID address was received. When the subsequent R/W# bit is 0 [W], the IIC recognizes the second and the subsequent frames as slave addresses and continues the receive operation. When the DIDE bit is set to 0, the IIC ignores the received first frame even if it matches the device ID address and recognizes the first frame as a normal slave address.

For details on the device ID address detection, see section 30.7.3, Device ID Address Detection.

HOAE bit (Host Address Enable)

The HOAE bit specifies whether to ignore received host address (0001 000b) when the SMBS bit in ICMR3 is 1.

When this bit is set to 1 while the SMBS bit in ICMR3 is 1, if the received slave address matches the host address, the IIC recognizes the received slave address as the host address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the receive operation.

When the SMBS bit in ICMR3 or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

30.2.8 I2C Bus Interrupt Enable Register (ICIER)

Address(es): IIC0.ICIER 4005 3007h, IIC1.ICIER 4005 3107h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOIE	Timeout Interrupt Request Enable	0: Timeout interrupt (TMOIn) request disabled 1: Timeout interrupt (TMOIn) request enabled.	R/W
b1	ALIE	Arbitration-Lost Interrupt Request Enable	0: Arbitration-lost interrupt (ALIn) request disabled 1: Arbitration-lost interrupt (ALIn) request enabled.	R/W
b2	STIE	Start Condition Detection Interrupt Request Enable	0: Start condition detection interrupt (STIn) request disabled 1: Start condition detection interrupt (STIn) request enabled.	R/W
b3	SPIE	Stop Condition Detection Interrupt Request Enable	0: Stop condition detection interrupt (SPIn) request disabled 1: Stop condition detection interrupt (SPIn) request enabled.	R/W
b4	NAKIE	NACK Reception Interrupt Request Enable	0: NACK reception interrupt (NAKIn) request disabled 1: NACK reception interrupt (NAKIn) request enabled.	R/W
b5	RIE	Receive Data Full Interrupt Request Enable	0: Receive data full interrupt (IICn_RXI) request disabled 1: Receive data full interrupt (IICn_RXI) request enabled.	R/W
b6	TEIE	Transmit End Interrupt Request Enable	0: Transmit end interrupt (IICn_TEI) request disabled 1: Transmit end interrupt (IICn_TEI) request enabled.	R/W
b7	TIE	Transmit Data Empty Interrupt Request Enable	0: Transmit data empty interrupt (IICn_TXI) request disabled 1: Transmit data empty interrupt (IICn_TXI) request enabled.	R/W

TMOIE bit (Timeout Interrupt Request Enable)

The TMOIE bit enables or disables timeout interrupt (TMOIn) requests when the TMOF flag in ICSR2 is set to 1. To cancel a TMOI interrupt request, set the TMOF flag or the TMOIE bit to 0.

当该位设置为1时，如果接收到的从机地址与广播呼叫地址匹配，则IIC将接收到的从机地址识别为广播呼叫地址，而与在SARLy和SARUy中设置的从机地址（y=0到2）无关，并执行数据接收操作。当该位设置为0时，即使接收到的从机地址与广播呼叫地址匹配，也会忽略它。

DIDE位（设备ID地址检测使能）

DIDE位指定当在检测到开始条件或重新启动条件后的第一帧中接收到设备ID(1111100b)时是否识别和执行设备ID地址。

当DIDE位设置为1时，如果接收到的第一帧与设备ID匹配，则IIC识别出设备ID地址已收到。当随后的RW#位为0[W]时，IIC将第二个和后续帧识别为从地址并继续接收操作。当DIDE位设置为0时，IIC忽略接收到的第一帧，即使它与设备ID地址匹配，并将第一帧识别为正常的从机地址。

有关设备ID地址检测的详细信息，请参阅第30.7.3节，设备ID地址检测。

HOAE位（主机地址使能）

HOAE位指定当ICMR3中的SMBS位为1时是否忽略接收到的主机地址（0001000b）。

当该位设置为1且ICMR3中的SMBS位为1时，如果接收到的从机地址与主机地址匹配，则IIC将接收到的从地址识别为主机地址，与SARLy中设置的从地址无关，并且SARUy（y=0到2）并执行接收操作。

当ICMR3中的SMBS位或HOAE位设置为0时，即使接收到的从机地址与主机地址匹配，也会忽略它。

30.2.8 I2C总线中断使能寄存器(ICIER)

Address(es): IIC0.ICIER 4005 3007h, IIC1.ICIER 4005 3107h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TMOIE	超时中断请求使能	0：禁止超时中断（TMOIn）请求1：允许超时中断（TMOIn）请求。	R/W
b1	ALIE	仲裁失败中断请求Enable	0：禁用仲裁丢失中断(ALIn)请求1：启用仲裁丢失中断(ALIn)请求。	R/W
b2	STIE	启动条件检测中断请求启用	0：禁止启动条件检测中断（STIn）请求1：允许启动条件检测中断（STIn）请求。	R/W
b3	SPIE	停止条件检测中断请求启用	0：停止条件检测中断（SPIn）请求禁止1：停止条件检测中断（SPIn）请求允许。	R/W
b4	NAKIE	NACK接收中断请求Enable	0：禁止NACK接收中断（NAKIn）请求1：允许NACK接收中断（NAKIn）请求。	R/W
b5	RIE	接收数据完整中断请求Enable	0：禁止接收数据完整中断（IICn_RXI）请求1：使能接收数据完整中断（IICn_RXI）请求。	R/W
b6	TEIE	发送结束中断请求Enable	0：禁止发送结束中断（IICn_TEI）请求1：允许发送结束中断（IICn_TEI）请求。	R/W
b7	TIE	发送数据空中断请求启用	0：禁止发送数据空中断（IICn_TXI）请求1：允许发送数据空中断（IICn_TXI）请求。	R/W

TMOIE位（超时中断请求使能）

当ICSR2中的TMOF标志设置为1时，TMOIE位启用或禁用超时中断(TMOIn)请求。要取消TMOI中断请求，请将TMOF标志或TMOIE位设置为0。

ALIE bit (Arbitration-Lost Interrupt Request Enable)

The ALIE bit enables or disables arbitration-lost interrupt (ALIn) requests when the AL flag in ICSR2 is set to 1. To cancel an ALI interrupt request, set the AL flag or the ALIE bit to 0.

STIE bit (Start Condition Detection Interrupt Request Enable)

The STIE bit enables or disables start condition detection interrupt (STIn) requests when the START flag in ICSR2 is set to 1. To cancel an STI interrupt request, set the START flag or the STIE bit to 0.

SPIE bit (Stop Condition Detection Interrupt Request Enable)

The SPIE bit enables or disables stop condition detection interrupt (SPIn) requests when the STOP flag in ICSR2 is set to 1. To cancel an SPI interrupt request, set the STOP flag or the SPIE bit to 0.

NAKIE bit (NACK Reception Interrupt Request Enable)

The NAKIE bit enables or disables NACK reception interrupt (NAKIn) requests when the NACKF flag in ICSR2 is set to 1. To cancel an NAKI interrupt request, set the NACKF flag or the NAKIE bit to 0.

RIE bit (Receive Data Full Interrupt Request Enable)

The RIE bit enables or disables receive data full interrupt (IICn_RXI) requests when the RDRF flag in ICSR2 is set to 1.

TEIE bit (Transmit End Interrupt Request Enable)

The TEIE bit enables or disables transmit end interrupt (IICn_TEI) requests when the TEND flag in ICSR2 is set to 1. To cancel an IICn_TEI interrupt request, set the TEND flag or the TEIE bit to 0.

TIE bit (Transmit Data Empty Interrupt Request Enable)

The TIE bit enables or disables transmit data empty interrupt (IICn_TXI) requests when the TDRE flag in ICSR2 is set to 1.

30.2.9 I²C Bus Status Register 1 (ICSR1)

Address(es): IIC0.ICSR1 4005 3008h, IIC1.ICSR1 4005 3108h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 not detected 1: Slave address 0 detected.	R/(W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 not detected 1: Slave address 1 detected.	R/(W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 not detected 1: Slave address 2 detected.	R/(W) *1
b3	GCA	General Call Address Detection Flag	0: General call address not detected 1: General call address detected.	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device ID Address Detection Flag	0: Device ID command not detected 1: Device ID command detected. This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0[W]).	R/(W) *1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

ALIE位（仲裁丢失中断请求使能）

当ICSR2中的AL标志设置为1时，ALIE位启用或禁用仲裁丢失中断(ALIn)请求。要取消ALI中断请求，请将AL标志或ALIE位设置为0。

STIE位（启动条件检测中断请求使能）

当ICSR2中的START标志设置为1时，STIE位启用或禁用启动条件检测中断(STIn)请求。要取消STI中断请求，请将START标志或STIE位设置为0。

SPIE位（停止条件检测中断请求使能）

当ICSR2中的STOP标志设置为1时，SPIE位启用或禁用停止条件检测中断(SPIn)请求。要取消SPI中断请求，请将STOP标志或SPIE位设置为0。

NAKIE位（NACK接收中断请求使能）

当ICSR2中的NACKF标志设置为1时，NAKIE位启用或禁用NACK接收中断(NAKIn)请求。要取消NAKI中断请求，请将NACKF标志或NAKIE位设置为0。

RIE位（接收数据满中断请求使能）

当ICSR2中的RDRF标志设置为1时，RIE位启用或禁用接收数据完整中断(IICn_RXI)请求。

TEIE位（发送结束中断请求使能）

当ICSR2中的TEND标志设置为1时，TEIE位启用或禁用发送结束中断(IICn_TEI)请求。要取消IICn_TEI中断请求，请将TEND标志或TEIE位设置为0。

TIE位（发送数据空中断请求使能）

当ICSR2中的TDRE标志设置为1时，TIE位启用或禁用发送数据空中断(IICn_TXI)请求。

30.2.9 I2C总线状态寄存器1(ICSR1)

Address(es): IIC0.ICSR1 4005 3008h, IIC1.ICSR1 4005 3108h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	AAS0	从地址0检测标志	0：未检测到从地址01：检测到从地址0。	R/(W) *1
b1	AAS1	从地址1检测标志	0：未检测到从地址11：检测到从地址1。	R/(W) *1
b2	AAS2	从地址2检测标志	0：未检测到从地址21：检测到从地址2。	R/(W) *1
b3	GCA	广播呼叫地址检测Flag	0：未检测到广播呼叫地址1：检测到广播呼叫地址。	R/(W) *1
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	DID	设备ID地址检测标志	0：未检测到设备ID命令1：检测到设备ID命令。当检测到开始条件后立即接收到的第一个帧与(设备ID(1111100b)+0[W])的值匹配时，该位设置为1。	R/(W) *1
b6	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	HOA	Host Address Detection Flag	0: Host address not detected 1: Host address detected. This bit is set to 1 when the received slave address matches the host address (0001 000b).	R/(W) *1

Note 1. Only 0 can be written to clear the flag.

AASy flag (Slave Address y Detection Flag) (y = 0 to 2)

[Setting conditions]

For 7-bit address format (SARUy.FS = 0):

- When the received slave address matches the SVA[6:0] value in SARLy with the SARyE bit in ICSER set to 1 (slave address y detection enabled). This flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address matches a value of 11110b + SVA[1:0] in SARUy and the subsequent address matches the SARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled). This flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy bit after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or internal reset.

For 7-bit address format (SARUy.FS = 0):

- When the received slave address does not match the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address does not match a value of 11110b + SVA[1:0] in SARUy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When the received slave address matches a value of 11110b + SVA[1:0] in SARUy, and the subsequent address does not match the SARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.

GCA flag (General Call Address Detection Flag)

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection is enabled). This flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA bit after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection is enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

DID flag (Device ID Address Detection Flag)

[Setting condition]

Bit	Symbol	位名称	Description	R/W
b7	HOA	主机地址检测标志	0：未检测到主机地址1：检测到主机地址。当接收到的从机地址与主机地址(0001000b)匹配时，该位设置为1。	R/(W) *1

Note 1. 只能写入0来清除标志。

AASy标志（从机地址y检测标志）（y=0到2）

[Setting conditions]

对于7位地址格式(SARUy.FS=0)：

- 当接收到的从地址与SARLy中的SVA[6:0]值匹配且ICSER中的SARyE位设置为1（从地址y检测启用）时。该标志在帧中第9个SCL时钟周期的上升沿设置为1。

对于10位地址格式(SARUy.FS=1)：

- 当接收到的从地址与SARUy中的值11110b+SVA[1:0]匹配且后续地址与SARLy值匹配且ICSER中的SARyE位设置为1（启用从地址y检测）时。该标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取AASy=1后将0写入AASy位时
- 检测到停止条件时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

对于7位地址格式(SARUy.FS=0)：

- 当接收到的从地址与SARLy中的SVA[6:0]值不匹配时，ICSER中的SARyE位设置为1（从地址y检测使能）。该标志在帧中第9个SCL时钟周期的上升沿设置为0。

对于10位地址格式(SARUy.FS=1)：

- 当接收到的从地址与SARUy中的值11110b+SVA[1:0]不匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当接收到的从地址与SARUy中的值11110b+SVA[1:0]匹配，并且后续地址与SARLy值不匹配且ICSER中的SARyE位设置为1（启用从地址y检测）时。该标志在帧中第9个SCL时钟周期的上升沿设置为0。

GCA标志（广播呼叫地址检测标志）

[Setting condition]

- 当接收到的从机地址与广播地址（0000000b+0[W]）匹配时，GCAE位在ICSER设置为1（启用广播呼叫地址检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取GCA=1后将0写入GCA位时
- 检测到停止条件时
- 当接收到的从机地址与广播地址（0000000b+0[W]）不匹配时，GCAE位在ICSER设置为1（启用广播呼叫地址检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

DID标志（设备ID地址检测标志）

[Setting condition]

- When the first frame received immediately after a start condition or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), with the DIDE bit in ICSER set to 1 (device ID address detection is enabled). This flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID bit after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start condition or restart condition is detected does not match a value of (device ID (1111 100b)), with the DIDE bit in ICSER set to 1 (device ID address detection is enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When the first frame received immediately after a start condition or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]) and the second frame does not match any slave address from 0 to 2 with the DIDE bit in ICSER set to 1 (device ID address detection is enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

HOA flag (Host Address Detection Flag)

[Setting condition]

- When the received slave address matches the host address (0001 000b) with the HOAE bit in ICSER set to 1 (host address detection is enabled). This flag is set to 1 on the rising edge of the 9th SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA bit after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection is enabled). This flag is set to 0 on the rising edge of the 9th SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

30.2.10 I2C Bus Status Register 2 (ICSR2)

Address(es): IIC0.ICSR2 4005 3009h, IIC1.ICSR2 4005 3109h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout not detected 1: Timeout detected.	R/(W) *1
b1	AL	Arbitration-Lost Flag	0: Arbitration not lost 1: Arbitration lost.	R/(W) *1
b2	START	Start Condition Detection Flag	0: Start condition not detected 1: Start condition detected.	R/(W) *1
b3	STOP	Stop Condition Detection Flag	0: Stop condition not detected 1: Stop condition detected.	R/(W) *1
b4	NACKF	NACK Detection Flag	0: NACK not detected 1: NACK detected.	R/(W) *1
b5	RDRF	Receive Data Full Flag	0: ICDRR contains no receive data 1: ICDRR contains receive data.	R/(W) *1

- 当检测到开始条件或重新启动条件后立即接收到的第一帧与（设备ID(1111100b)+0[W]）的值匹配，且ICSER中的DIDE位设置为1（启用设备ID地址检测）.该标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取DID=1后向DID位写入0时
- 检测到停止条件时
- 当检测到开始条件或重新启动条件后立即接收的第一帧与(设备ID(1111100b))的值不匹配时，ICSER中的DIDE位设置为1（启用设备ID地址检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当检测到启动条件或重新启动条件后立即接收到的第一帧与（设备ID(1111100b)+0[W]）的值匹配，并且第二帧与DIDE位不匹配从0到2的任何从机地址在ICSER中设置为1（启用设备ID地址检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

HOA标志（主机地址检测标志）

[Setting condition]

- 当接收到的从机地址与主机地址(0001000b)匹配且ICSER中的HOAE位设置为1时（启用主机地址检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取HOA=1后将0写入HOA位时
- 检测到停止条件时
- 当接收到的从机地址与主机地址（0001000b）不匹配时，将ICSER中的HOAE位设置为1（启用主机地址检测）。该标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

30.2.10 I2C总线状态寄存器2(ICSR2)

Address(es): IIC0.ICSR2 4005 3009h, IIC1.ICSR2 4005 3109h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TMOF	超时检测标志	0：未检测到超时1：检测到超时。	R/(W) *1
b1	AL	Arbitration-Lost Flag	0：仲裁未失败1：仲裁失败。	R/(W) *1
b2	START	启动条件检测标志	0：未检测到启动条件1：检测到启动条件。	R/(W) *1
b3	STOP	停止条件检测标志	0：未检测到停止条件1：检测到停止条件。	R/(W) *1
b4	NACKF	NACK检测标志	0：未检测到NACK1：检测到NACK。	R/(W) *1
b5	RDRF	接收数据满标志	0：ICDRR不包含接收数据1：ICDRR包含接收数据。	R/(W) *1

Bit	Symbol	Bit name	Description	R/W
b6	TEND	Transmit End Flag	0: Data being transmitted 1: Data transmission complete.	R/(W) *1
b7	TDRE	Transmit Data Empty Flag	0: ICDRT contains transmit data 1: ICDRT contains no transmit data.	R

Note 1. Only 0 can be written to clear the flag.

TMOF flag (Timeout Detection Flag)

The TMOF flag is set to 1 when the IIC detects a timeout after the SCLn line state remains unchanged for the set period.

[Setting condition]

- When the SCLn line state remains unchanged for the period specified in the TMOH, TMOL, and TMOS bits in ICMR2, while the TMOE bit in ICFER is 1 (the timeout function is enabled) in master mode or in slave mode, and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF bit after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

AL flag (Arbitration-Lost Flag)

The AL flag indicates that bus mastership is lost in arbitration because of a bus conflict or some other reason when a start condition is issued or an address and data is transmitted. The IIC monitors the level on the SDAn line during transmission and, if the level on the line does not match the value of the bit being output, sets the value of the AL flag to 1 to indicate that the bus is occupied by another device.

The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission in master mode or during data transmission in slave mode.

[Setting conditions]

When master arbitration-lost detection is enabled (ICFER.MALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of SCL clock, except for the ACK period during data transmission in master transmit mode
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition issue requested) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is set to 1 (start condition issue requested), with the BBSY flag in ICCR2 set to 1.

When NACK arbitration-lost detection is enabled (ICFER.NALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled (ICFER.SALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of SCL clock, except for the ACK period during data transmission in slave transmit mode.

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Bit	Symbol	位名称	Description	R/W
b6	TEND	发送结束标志	0：数据传输中1：数据传输完成。	R/(W) *1
b7	TDRE	传输数据空标志	0：ICDRT包含发送数据1：ICDRT不包含发送数据。	R

Note 1. 只能写入0来清除标志。

TMOF标志（超时检测标志）

当IIC在SCLn线路状态在设定的时间段内保持不变后检测到超时时，TMOF标志设置为1。

[Setting condition]

- 当SCLn线状态在TMOH、TMOL和TMOS位中指定的周期内保持不变时ICMR2，而在主模式或从模式下，ICFER中的TMOE位为1（使能超时功能），并且接收到的从地址匹配。

[Clearing conditions]

- 读取TMOF=1后向TMOF位写入0时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

AL标志（仲裁失败标志）

AL标志表示在发出启动条件或发送地址和数据时，由于总线冲突或其他原因，总线控制权在仲裁中丢失。IIC在传输过程中监视SDAn线上的电平，如果线上的电平与正在输出的位的值不匹配，则将AL标志的值设置为1，以指示总线被另一个设备占用。

IIC还可以设置AL标志，以指示在主机模式下的NACK传输期间或从机模式下的数据传输期间检测到仲裁丢失。

[Setting conditions]

当启用主机仲裁丢失检测时(ICFER.MALE=1)：

- 当内部SDA输出状态与SCL时钟上升沿上的SDAn线电平不匹配时，除了主机发送模式下数据传输期间的ACK周期
- 当ICCR2中的ST位为1（请求启动条件发出）或内部检测到启动条件时SDA输出状态与SDAn线路电平不匹配
- 当ICCR2中的ST位设置为1（请求启动条件发出）时，ICCR2中的BBSY标志设置为1。

当启用NACK仲裁丢失检测时(ICFER.NALE=1)：

- 在接收模式下的NACK传输期间，当内部SDA输出状态与ACK周期内SCL时钟上升沿上的SDAn线电平不匹配时。

当启用从设备仲裁丢失检测时(ICFER.SALE=1)：

- 当内部SDA输出状态与SCL时钟上升沿上的SDAn线电平不匹配时，除了从机传输模式下数据传输期间的ACK周期。

[Clearing conditions]

- 读取AL=1后向AL标志写入0时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

Table 30.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 and BBSY in ICCR2 set to 1
			1	Transmit data mismatch	When transmit data including slave address does not match the bus state in master transmit mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master or slave receive mode
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

×: Don't care

START flag (Start Condition Detection Flag)

[Setting condition]

- When a start condition or a restart condition is detected.

[Clearing conditions]

- When 0 is written to the START bit after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

STOP flag (Stop Condition Detection Flag)

[Setting condition]

- When a stop condition is detected.

[Clearing conditions]

- When 0 is written to the STOP bit after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

NACKF flag (NACK Detection Flag)

[Setting condition]

- When an acknowledge is not received (NACK is received) from the receive device in transmit mode, with the NACKE bit in ICFER set to 1 (transfer suspension enabled).

[Clearing conditions]

- When 0 is written to the NACKF bit after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1, the IIC suspends data transmission or reception. Writing to ICDRT in transmit mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit or receive operation. To restart data transmission or reception, set the NACKF flag to 0.

RDRF flag (Receive Data Full Flag)

[Setting conditions]

- When receive data is transferred from ICDRS to ICDRR. The RDRF flag is set to 1 on the rising edge of the 8th or 9th SCL clock cycle (selected by the RDRFS bit in ICMR3).
- When the received slave address matches, after a start condition or a restart condition is detected, with the TRS bit

Table 30.4 仲裁丢失生成源和仲裁丢失使能函数之间的关系

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	仲裁失败的生成源
1	×	×	1	开始条件发布错误	当ICCR2中的ST位为1时检测到启动条件时，当内部SDA输出状态与SDAn线电平不匹配时
					当ICCR2中的ST设置为1且ICCR2中的BBSY设置为1时
			1	传输数据不匹配	当发送数据包括从机地址与主机发送模式下的总线状态不匹配时
×	1	×	1	NACK传输不匹配	在主机或从机接收模式下发送NACK期间检测到ACK时
×	×	1	1	传输数据不匹配	当发送数据与从发送模式下的总线状态不匹配时

×: Don't care

START标志（开始条件检测标志）

[Setting condition]

- 当检测到启动条件或重新启动条件时。

[Clearing conditions]

- 读取START=1后向START位写入0时
- 检测到停止条件时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

停止标志（停止条件检测标志）

[Setting condition]

- 当检测到停止条件时。

[Clearing conditions]

- 在读取STOP=1后将0写入STOP位时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

NACKF标志（NACK检测标志）

[Setting condition]

- 在发送模式下，当没有从接收设备接收到确认（接收到NACK）时，使用ICFER中的NACKE位设置为1（启用传输暂停）。

[Clearing conditions]

- 读取NACKF=1后向NACKF位写入0时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

Note: 当NACKF标志设置为1时，IIC暂停数据发送或接收。在NACKF标志设置为1的情况下，在发送模式下写入ICDRT或在接收模式下从ICDRR读取不会启用数据发送或接收操作。要重新开始数据发送或接收，请将NACKF标志设置为0。

RDRF标志（接收数据满标志）

[Setting conditions]

- 当接收数据从ICDRS传输到ICDRR。RDRF标志在第8个或第9个SCL时钟周期的上升沿设置为1（由ICMR3中的RDRFS位选择）。
- 当接收到的从机地址匹配时，在检测到启动条件或重启条件后，与TRS位

in ICCR2 set to 0.

[Clearing conditions]

- When 0 is written to the RDRF bit after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

TEND flag (Transmit End Flag)

[Setting condition]

- On the rising edge of the 9th SCL clock cycle while the TDRE flag is 1.

[Clearing conditions]

- When 0 is written to the TEND bit after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

TDRE flag (Transmit Data Empty Flag)

[Setting conditions]

- When data is transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1.

[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0
- When 1 is written to the IICRST bit in ICCR1 to initiate an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the IIC suspends data transmission or reception. In this case, if the TDRE flag is 0 (next transmit data written), data is transferred to the ICDRS register and the ICDRT register becomes empty on the rising edge of the 9th clock cycle, but the TDRE flag is not set to 1.

30.2.11 I2C Bus Wakeup Unit Register (ICWUR)

Address(es): IIC0.ICWUR 4005 3016h

	b7	b6	b5	b4	b3	b2	b1	b0
	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
Value after reset:	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WUAFA	Wakeup Analog Filter Additional Selection	0: Do not add the wakeup analog filter 1: Add the wakeup analog filter.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	WUACK	ACK bit for Wakeup Mode	Choice of four response modes in combination with ICCR1.IICRST and WUACK. See Table 30.5.	R/W
b5	WUF	Wakeup Event Occurrence Flag	0: Slave address not matching during wakeup 1: Slave address matching during wakeup.	R/W

在ICCR2中设置为0。

[Clearing conditions]

- 读取RDRF=1后向RDRF位写入0时
- 从ICDRR读取数据时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

TEND标志（发送结束标志）

[Setting condition]

- 在第9个SCL时钟周期的上升沿，同时TDRE标志为1。

[Clearing conditions]

- 读取TEND=1后向TEND位写入0时
- 数据写入ICDRT时
- 检测到停止条件时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

TDRE标志（传输数据空标志）

[Setting conditions]

- 当数据从ICDRT传输到ICDRS并且ICDRT变为空时
- ICCR2中的TRS位设置为1时
- 当TRS位为1时接收到的从机地址匹配。

[Clearing conditions]

- 数据写入ICDRT时
- ICCR2中的TRS位设置为0时
- 当向ICCR1中的IICRST位写入1以启动IIC复位或内部复位。

Note: 当ICFER中的NACKE位为1时NACKF标志设置为1，则IIC暂停数据发送或接收。在这种情况下，如果TDRE标志为0（写入下一个发送数据），则数据被传送到ICDRS寄存器
并且ICDRT寄存器在第9个时钟周期的上升沿变空，但TDRE标志不设置为1。

30.2.11 I2C总线唤醒单元寄存器(ICWUR)

Address(es): IIC0.ICWUR 4005 3016h

	b7	b6	b5	b4	b3	b2	b1	b0
	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
重置后的值:	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	WUAFA	唤醒模拟滤波器附加选择	0：不加唤醒模拟滤波器1：加唤醒模拟滤波器。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	WUACK	唤醒模式的ACK位	四种响应模式的选择结合ICCR1.IICRST和WUACK。见表30.5。	R/W
b5	WUF	唤醒事件发生标志	0：唤醒期间从机地址不匹配1：唤醒期间从机地址匹配。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	WUIE	Wakeup Interrupt Request Enable	0: Wakeup Interrupt Request (IIC0_WUI) disabled 1: Wakeup Interrupt Request (IIC0_WUI) enabled.	R/W
b7	WUE	Wakeup Function Enable	0: Wakeup function disabled 1: Wakeup function enabled.	R/W

Table 30.5 Wakeup mode

IICRST	WUACK	Operation mode	Description
0	0	Normal wakeup mode 1	ACK response at 9th SCL and SCL low hold after 9th SCL
0	1	Normal wakeup mode 2	No ACK response immediately and SCL low hold between 8th and 9th SCL. SCL low hold release and ACK response on 9th SCL.
1	0	Command recovery mode	ACK response on 9th SCL and no SCL low hold
1	1	EEP response mode	NACK response on 9th SCL and no SCL low hold

WUF flag (Wakeup Event Occurrence Flag)

[Setting condition]

- When PCLKB is supplied after a slave-address match in the first 8th SCL low during wakeup mode.

[Clearing conditions]

- When 0 is written to the WUF bit after reading WUF = 1
- ICE = 0, IICRST = 1.

30.2.12 I2C Bus Wakeup Unit Register 2 (ICWUR2)

Address(es): IIC0.ICWUR2 4005 3017h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WUSYF	WUASYF	WUSEN
Value after reset:	1	1	1	1	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	WUSEN	Wakeup Function Synchronous Enable	0: IIC asynchronous operation enabled 1: IIC synchronous operation enabled.	R/W
b1	WUASYF	Wakeup Function Asynchronous Operation Status Flag	0: IIC synchronous operation enabled 1: IIC asynchronous operation enabled.	R
b2	WUSYF	Wakeup Function Synchronous Operation Status Flag	0: IIC asynchronous operation enabled 1: IIC synchronous operation enabled.	R
b7 to b3	—	Reserved	These bits are read as1. The write value should be 1.	R/W

WUSEN bit (Wakeup Function Synchronous Enable)

The WUSEN bit is used in combination with the WUASYF flag (or WUSYF flag) to switch between PCLKB synchronous and asynchronous operation, when the wakeup function is enabled (ICWUR.WUE = 1).

The PCLKB operation switches from synchronous to asynchronous operation:

- When the ICCR2.BBSY flag is 0 (bus free state) if 0 is written to the WUSEN bit while the WUASYF flag is 0.
- The reception occurs independently of the operation of PCLKB (with PCLKB stopped) after it switches to the PCLKB asynchronous operation, on wakeup event detection.

The PCLKB operation switches asynchronous to synchronous operation:

- When 1 is written to the WUSEN bit with the WUASYF flag at 1, when a wakeup event is detected. After writing 1, the WUASYF flag immediately becomes 0.

Bit	Symbol	位名称	Description	R/W
b6	WUIE	唤醒中断请求使能	0：唤醒中断请求（IIC0_WUI）禁用1：唤醒中断请求（IIC0_WUI）启用。	R/W
b7	WUE	唤醒功能启用	0：禁用唤醒功能1：启用唤醒功能。	R/W

Table 30.5 唤醒模式

IICRST	WUACK	操作模式	Description
0	0	正常唤醒模式1	第9个SCL的ACK响应和第9个SCL后的SCL低保持
0	1	正常唤醒模式2	没有ACK立即响应，并且SCL在第8和第9SCL之间保持低电平。SCL低保持释放和第9个SCL的ACK响应。
1	0	命令恢复模式	在第9个SCL上的ACK响应并且没有SCL低保持
1	1	EEP响应模式	第9个SCL的NACK响应和无SCL低保持

WUF标志（唤醒事件发生标志）

[Setting condition]

- 当PCLKB在唤醒模式下的前8个SCL低电平的从地址匹配后提供时。

[Clearing conditions]

- 读取WUF=1后向WUF位写入0时
- ICE = 0, IICRST = 1.

30.2.12 I2C总线唤醒单元寄存器2(ICWUR2)

Address(es): IIC0.ICWUR2 4005 3017h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WUSYF	WUASYF	WUSEN
重置后的值：	1	1	1	1	1	1	0	1

Bit	Symbol	位名称	Description	R/W
b0	WUSEN	唤醒功能同步Enable	0：IIC异步操作使能1：IIC同步操作使能。	R/W
b1	WUASYF	唤醒功能异步操作状态标志	0：IIC同步操作使能1：IIC异步操作使能。	R
b2	WUSYF	唤醒功能同步操作状态标志	0：IIC异步操作使能1：IIC同步操作使能。	R
b7 to b3	—	Reserved	这些位被读取为1。写入值应为1。	R/W

WUSEN位（唤醒功能同步使能）

WUSEN位与WUASYF标志（或WUSYF标志）结合使用，在启用唤醒功能时（ICWUR.WUE=1）在PCLKB同步和异步操作之间切换。

PCLKB操作从同步操作切换到异步操作：

- 如果在WUASYF标志为0时将0写入WUSEN位，则ICCR2.BBSY标志为0（总线空闲状态）。
- 接收发生独立于PCLKB的操作（PCLKB停止）后，PCLKB异步操作，唤醒事件检测。

PCLKB操作将异步操作切换为同步操作：

- 当WUASYF标志为1的情况下向WUSEN位写入1时，检测到唤醒事件。写入1后，WUASYF标志立即变为0。

- When a stop condition is detected with a wakeup event undetected.

WUASYF flag (Wakeup Function Asynchronous Operation Status Flag)

This flag can place the IIC in PCLKB asynchronous operation when the wakeup function is enabled (ICWUR.WUE = 1).

[Setting condition]

- When the ICCR2.BBSY flag is 0, and WUSEN bit is set to 0, with the ICWUR.WUE bit set to 1.

[Clearing conditions]

- When 1 is written to the WUSEN bit, after detecting a wakeup event with ICWUR.WUE bit set to 1
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wakeup event, with WUASY flag set to 1 and ICWUR.WUE bit set to 1
- When 1 is written to the WUSEN bit with the WUASYF flag set to 1, and a wakeup event is detected with ICWUR.WUE set to 1
- When ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- When ICWUR.WUE = 0.

WUSYF flag (Wakeup Function Synchronous Operation Status Flag)

This flag can place the IIC in PCLKB synchronous operation when the wakeup function is enabled (ICWUR.WUE = 1). When this flag is used, the WUASYF flag is reserved.

[Setting conditions]

- When 1 is written to the WUSEN bit after detecting a wakeup event with ICWUR.WUE bit set to 1, and WUSYF flag set to 0
- When a stop condition is detected with WUSEN bit set to 1, before detecting a wakeup event with the WUSYF flag set to 0 and the ICWUR.WUE bit set to 1
- When ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- When ICWUR.WUE = 0.

[Clearing condition]

- When the ICCR2.BBSY flag is 0 with the ICWUR.WUE bit set to 1, after writing 0 to the WUSEN bit.

30.2.13 Slave Address Register Ly (SARLy) (y = 0 to 2)

Address(es): IIC0.SARL0 4005 300Ah, IIC1.SARL0 4005 310Ah, IIC0.SARL1 4005 300Ch, IIC1.SARL1 4005 310Ch, IIC0.SARL2 4005 300Eh, IIC1.SARL2 4005 310Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	SVA[6:0]							SVA0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SVA0	10-Bit Address LSB	Slave address setting	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	Slave address setting	R/W

SVA0 bit (10-Bit Address LSB)

When the 10-bit address format is selected (SARUy.FS = 1), the SVA0 bit functions as the LSB of a 10-bit address and is combined with the SVA[6:0] bits to form the lower 8 bits of a 10-bit address.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, this bit is valid. When the SARUy.FS bit or SARyE bit is 0, the setting of this bit is ignored.

- 当检测到停止条件且未检测到唤醒事件时。

WUASYF标志（唤醒功能异步操作状态标志）

当启用唤醒功能（ICWUR.WUE=1）时，该标志可以将IIC置于PCLKB异步操作中。

[Setting condition]

- 当ICCR2.BBSY标志为0且WUSEN位设置为0时，ICWUR.WUE位设置为1。

[Clearing conditions]

- 当WUSEN位写入1时，检测到唤醒事件后ICWUR.WUE位设置为1
- 在检测到唤醒事件之前检测到停止条件且WUSEN位设置为1且WUASY标志设置为1且ICWUR.WUE位设置为1
- 当WUASYF标志设置为1的情况下将1写入WUSEN位时，检测到唤醒事件ICWUR.WUE设置为1
- 当ICCR1.ICE=0且ICCRST=1时（ICC复位）
- When ICWUR.WUE = 0.

WUSYF标志（唤醒功能同步操作状态标志）

当启用唤醒功能（ICWUR.WUE=1）时，该标志可以将IIC置于PCLKB同步操作中。
使用此标志时，保留WUASYF标志。

[Setting conditions]

- 当检测到唤醒事件后将1写入WUSEN位时，ICWUR.WUE位设置为1，WUSYF标志设置为0
- 当WUSEN位设置为1检测到停止条件时，在检测到WUSYF标志设置为0且ICWUR.WUE位设置为1的唤醒事件之前
- 当ICCR1.ICE=0且ICCRST=1时（ICC复位）
- When ICWUR.WUE = 0.

[Clearing condition]

- 当ICCR2.BBSY标志为0且ICWUR.WUE位设置为1时，将0写入WUSEN位。

30.2.13 从地址寄存器Ly(SARLy)(y=0to2)

Address(es): IIC0.SARL0 4005 300Ah, IIC1.SARL0 4005 310Ah, IIC0.SARL1 4005 300Ch, IIC1.SARL1 4005 310Ch, IIC0.SARL2 4005 300Eh, IIC1.SARL2 4005 310Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	SVA[6:0]							SVA0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SVA0	10-Bit Address LSB	从机地址设置	R/W
b7 to b1	SVA[6:0]	7位地址10位地址低位	从机地址设置	R/W

SVA0位（10位地址LSB）

Whenthe10-bitaddressformatisselected(SARUy.FS=1) theSVA0bitfunctionsastheLSBofa10-bitaddressandiscombinedwiththeSVA[6:0]bitstoformthelower8bitsofa10位地址。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，该位有效。
当SARUy.FS位或SARyE位为0时，忽略该位的设置。

SVA[6:0] bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), the SVA[6:0] bits function as a 7-bit address. When the 10-bit address format is selected (SARUy.FS = 1), these bits combined with the SVA0 bit to form the lower 8 bits of a 10-bit address. When the SARyE bit in ICSER is 0, the setting of these bits is ignored.

30.2.14 Slave Address Register Uy (SARUy) (y = 0 to 2)

Address(es): IIC0.SARU0 4005 300Bh, IIC1.SARU0 4005 310Bh, IIC0.SARU1 4005 300Dh, IIC1.SARU1 4005 310Dh, IIC0.SARU2 4005 300Fh, IIC1.SARU2 4005 310Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Select	0: Select 7-bit address format 1: Select 10-bit address format.	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	Slave address setting	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS bit (7-Bit/10-Bit Address Format Select)

The FS bit selects the 7-bit address or 10-bit address for the slave address y in SARLy and SARUy.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the settings of the SVA[1:0] bits and the SVA0 bit in SARLy are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the settings of the SVA[1:0] bits and SARLy are valid.

When the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the setting in the SARUy.FS bit is invalid.

SVA[1:0] bits (10-Bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), the SVA[1:0] bits function as the upper 2 bits of a 10-bit address.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, these bits are valid. When the SARUy.FS bit or SARyE bit is 0, the setting of these bits is ignored.

30.2.15 I2C Bus Bit Rate Low-Level Register (ICBRL)

Address(es): IIC0.ICBRL 4005 3010h, IIC1.ICBRL 4005 3110h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

BRL[4:0] bits (Bit Rate Low-Level Period)

The BRL[4:0] bits set the low-level period of the SCL clock. ICBRL counts the low-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1. ICBRL also generates the data setup time for

SVA[6:0]位（7位地址10位地址低位）

Whenthe7-bitaddressformatisselected(SARUy.FS=0) theSVA[6:0]bitsfunctionasa7-bitaddress.Whenthe10-bitaddressformatisselected(SARUy.FS=1) thesebitscombinedwiththeSVA0bittoformthelower8bitsofa10-bitaddress.当ICSER中的SARyE位为0时，这些位的设置被忽略。

30.2.14 从地址寄存器Uy(SARUy)(y=0to2)

Address(es): IIC0.SARU0 4005 300Bh, IIC1.SARU0 4005 310Bh, IIC0.SARU1 4005 300Dh, IIC1.SARU1 4005 310Dh, IIC0.SARU2 4005 300Fh, IIC1.SARU2 4005 310Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FS	7位10位地址格式选择	0：选择7位地址格式1：选择10位地址格式。	R/W
b2, b1	SVA[1:0]	10位地址高位	从机地址设置	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FS位（7位10位地址格式选择）

FS位为SARLy和SARUy中的从机地址y选择7位地址或10位地址。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为0时，从机地址y选择7位地址格式，SARLy中的SVA[6:0]设置有效 SARLy中的SVA[1:0]位和SVA0位的设置被忽略。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，从机地址y和SVA[1:0]位的设置选择10位地址格式和SARLy是有效的。

当ICSER中的SARyE位为0（SARLy和SARUy禁用）时，SARUy.FS位中的设置无效。

SVA[1:0]位（10位地址高位）

Whenthe10-bitaddressformatisselected(FS=1) theSVA[1:0]bitsfunctionastheupper2bitsofa10-bitaddress.

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，这些位有效。
当SARUy.FS位或SARyE位为0时，这些位的设置被忽略。

30.2.15 I2C总线比特率低电平寄存器(ICBRL)

Address(es): IIC0.ICBRL 4005 3010h, IIC1.ICBRL 4005 3110h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	BRL[4:0]	比特率低电平周期	SCL时钟低电平周期	R/W
b7 to b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W

BRL[4:0]位（比特率低电平周期）

BRL[4:0]位设置SCL时钟的低电平周期。ICBRL使用ICMR1的CKS[2:0]位中指定的内部参考时钟源(IIC)对低电平周期进行计数。ICBRL还生成数据建立时间

automatic SCL low-hold operation (see section 30.9, Automatic Low-Hold Function for SCL). When the IIC is used only in slave mode, the BRL[4:0] bits must be set to a value longer than the data setup time*1.

If the digital noise filter is enabled (the NFE bit in ICFER is 1), set the ICBRL register to a value at least one greater than the number of stages in the noise filter. For details on the number of stages, see the description of the ICMR3.NF[1:0] bits.

Note 1. Data setup time (tSU: DAT)
250 ns for up to 100 kbps: Standard-mode (Sm)
100 ns for up to 400 kbps: Fast-mode (Fm)

30.2.16 I2C Bus Bit Rate High-Level Register (ICBRH)

Address(es): IIC0.ICBRH 4005 3011h, IIC1.ICBRH 4005 3111h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

BRH[4:0] bits (Bit Rate High-Level Period)

The BRH[4:0] bits set the high-level period of the SCL clock. BRH[4:0] bits are valid in master mode. If the IIC is used only in slave mode, do not set the BRH[4:0] bits.

ICBRH counts the high-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1.

If the digital noise filter is enabled (the NFE bit in ICFER is 1), set these bits to a value at least one greater than the number of stages in the noise filter. For the number of stages in the noise filter, see the description of the ICMR3.NF[1:0] bits.

The IIC transfer rate and the SCL clock duty are calculated using the following expression.

1) ICFER.SCLE = 0
Transfer rate = 1/{[(BRH + 1) + (BRL + 1)]/IICφ*1 + tr*2 + tf*2}
Duty cycle = {tr + [(BRH + 1)/IICφ]}/{tr + tf + [(BRH + 1) + (BRL + 1)]/IICφ}

2) ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
Transfer rate = 1/{[(BRH + 3) + (BRL+ 3)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 3)/IICφ]}/{tr + tf + [(BRH + 3) + (BRL + 3)]/IICφ}

3) ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
Transfer rate = 1/{[(BRH + 3 + nf*3) + (BRL + 3 + nf)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 3 + nf)/IICφ]}/{tr + tf + [(BRH + 3 + nf) + (BRL + 3 + nf)]/IICφ}

4) ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
Transfer rate = 1/{[(BRH + 2) + (BRL + 2)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 2)/IICφ]}/{tr + tf + [(BRH + 2) + (BRL + 2)]/IICφ}

5) ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
Transfer rate = 1/{[(BRH + 2 + nf) + (BRL + 2 + nf)]/IICφ + tr + tf}
Duty cycle = {tr + [(BRH + 2 + nf)/IICφ]}/{tr + tf + [(BRH + 2 + nf) + (BRL + 2 + nf)]/IICφ}

Note 1. IICφ = PCLKB × Division ratio.
Note 2. The SCLn line rising time [tr] and SCLn line falling time [tf] depend on the total bus line capacitance [Cb] and the pull-up resistor [Rp]. For details, see the I2C bus standard from NXP Semiconductors.
Note 3. nf = Number of digital noise filter stages selected in the ICMR3.NF bits.

自动SCL低保持操作（参见第30.9节，SCL的自动低保持功能）。当IIC仅用于从机模式时，BRL[4:0]位必须设置为比数据建立时间*1更长的值。

如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将ICBRL寄存器设置为至少比噪声滤波器中的级数大1的值。有关级数的详细信息，请参见ICMR3.NF[1:0]位的说明。

注1.数据建立时间(tSU:DAT)
250ns，最高100kbps：标准模式(Sm)100ns，
最高400kbps：快速模式(Fm)

30.2.16 I2C总线比特率高级寄存器(ICBRH)

Address(es): IIC0.ICBRH 4005 3011h, IIC1.ICBRH 4005 3111h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	BRH[4:0]	比特率高级期	SCL时钟高电平周期	R/W
b7 to b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W

BRH[4:0]位（比特率高电平周期）

BRH[4:0]位设置SCL时钟的高电平周期。BRH[4:0]位在主机模式下有效。如果IIC仅用于从机模式，则不要设置BRH[4:0]位。

ICBRH使用CKS[2:0]位中指定的内部参考时钟源(IIC)计算高电平周期
ICMR1.

如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将这些位设置为至少比噪声滤波器中的级数大1的值。有关噪声滤波器的级数，请参见ICMR3.NF[1:0]位的说明。

IIC传输速率和SCL时钟占空比使用以下表达式计算。

1) ICFER.SCLE = 0
传输率=1{[(BRH+1)+(BRL+1)]IICφ*1+tr*2+tf*2
占空比={tr+[(BRH+1)IICφ] {tr+tf+[(BRH+1)+(BRL+1)]IICφ

2) ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
传输率=1{[(BRH+3)+(BRL+3)]IICφ+tr+tf
占空比={tr+[(BRH+3)IICφ] {tr+tf+[(BRH+3)+(BRL+3)]IICφ

3) ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
传输率=1{[(BRH+3+nf*3)+(BRL+3+nf)]IICφ+tr+tf
占空比={tr+[(BRH+3+nf)IICφ] {tr+tf+[(BRH+3+nf)+(BRL+3+nf)]IICφ

4) ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
传输率=1{[(BRH+2)+(BRL+2)]IICφ+tr+tf
占空比={tr+[(BRH+2)IICφ] {tr+tf+[(BRH+2)+(BRL+2)]IICφ

5) ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
传输率=1{[(BRH+2+nf)+(BRL+2+nf)]IICφ+tr+tf
占空比={tr+[(BRH+2+nf)IICφ] {tr+tf+[(BRH+2+nf)+(BRL+2+nf)]IICφ

Note 1. IICφ=PCLKB×分频比。
Note 2. SCLn线上升时间[tr]和SCLn线下降时间[tf]取决于总总线电容[Cb]和上拉电阻器[Rp]。有关详细信息，请参阅NXPSemiconductors的I2C总线标准。
Note 3. nf=在ICMR3.NF位中选择的数字噪声滤波器级数。

Table 30.6 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011	15 (EFh)	18 (F2h)	32	-	1)
400	001	9 (E9h)	20 (F4h)	32	-	1)

Table 30.7 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011	14 (EEh)	17 (F1h)	32	-	4)
400	001	8 (E8h)	19 (F3h)	32	-	4)

Table 30.8 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 1

Transfer rate (kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011	12 (ECh)	15 (EFh)	32	01b	5)
400	001	6 (E6h)	17 (F1h)	32	01b	5)

Note: SCLn line rising time (tr): ≤ 100 kbps, Sm: 1000 ns, ≤ 400 kbps, Fm: ≤ 300 ns
SCLn line falling time (tf): ≤ 400 kbps, Sm/Fm: ≤ 300 ns

30.2.17 I2C Bus Transmit Data Register (ICDRT)

Address(es): IIC0.ICDRT 4005 3012h, IIC1.ICDRT 4005 3112h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the I2C Bus Shift Register (ICDRS), it transfers the transmit data that is written to ICDRT to ICDRS and starts transmitting data in transmit mode.

The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data is written to ICDRT while the ICDRS data is being transmitted.

ICDRT can always be read from and written to. Write transmit data to ICDRT once when a transmit data empty interrupt (IICn_TXI) request is generated.

30.2.18 I2C Bus Receive Data Register (ICDRR)

Address(es): IIC0.ICDRR 4005 3013h, IIC1.ICDRR 4005 3113h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data is received, the received data is transferred from the I2C Bus Shift Register (ICDRS) to ICDRR to enable the next data to be received.

The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data is read from ICDRR while ICDRS is receiving data. ICDRR cannot be written to. Read data from ICDRR once when a receive data full interrupt (IICn_RXI) request is generated.

If ICDRR receives the next receive data before the current data is read from ICDRR while the RDRF flag in ICSR2 is 1, the IIC automatically holds the SCL clock low for 1 cycle before the RDRF flag is set to 1 again.

Table 30.6 SCLE=0时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011	15 (EFh)	18 (F2h)	32	-	1)
400	001	9 (E9h)	20 (F4h)	32	-	1)

Table 30.7 SCLE=1和NFE=0时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011	14 (EEh)	17 (F1h)	32	-	4)
400	001	8 (E8h)	19 (F3h)	32	-	4)

Table 30.8 SCLE=1和NFE=1时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0]	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011	12 (ECh)	15 (EFh)	32	01b	5)
400	001	6 (E6h)	17 (F1h)	32	01b	5)

Note: SCLn线路上升时间(tr): 100kbps，Sm：1000ns， 400kbps，Fm： 300ns
SCLn线下降时间(tf): 400kbps，SmFm： 300ns

30.2.17 I2C总线发送数据寄存器(ICDRT)

Address(es): IIC0.ICDRT 4005 3012h, IIC1.ICDRT 4005 3112h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1

当ICDRT在I2C总线移位寄存器(ICDRS)中检测到一个空间时，它会将写入的发送数据传输到ICDRT到ICDRS并开始在传输模式下传输数据。

ICDRT和ICDRS的双缓冲结构允许在传输ICDRS数据的同时将下一个传输数据写入ICDRT的连续传输操作。

ICDRT始终可以被读取和写入。当产生发送数据空中断（IICn_TXI）请求时，将发送数据写入ICDRT。

30.2.18 I2C总线接收数据寄存器(ICDRR)

Address(es): IIC0.ICDRR 4005 3013h, IIC1.ICDRR 4005 3113h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0

当接收到1个字节的数据时，接收到的数据会从I2C总线移位寄存器(ICDRS)传输到ICDRR，以便接收下一个数据。

如果在ICDRS正在接收数据时从ICDRR读取接收到的数据，ICDRS和ICDRR的双缓冲结构允许连续接收操作。无法写入ICDRR。当产生接收数据完全中断(IICn_RXI)请求时，从ICDRR读取数据一次。

如果ICDRR在从ICDRR读取当前数据之前接收到下一个接收数据，而ICSR2中的RDRF标志为1，则IIC在RDRF标志再次设置为1之前自动将SCL时钟保持低1个周期。

30.2.19 I2C Bus Shift Register (ICDRS)

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—

ICDRS is an 8-bit shift register to transmit and receive data. During transmission, transmit data is transferred from ICDRT to ICDRS and is sent from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data is received. ICDRS cannot be accessed directly.

30.3 Operation

30.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start or restart condition is an address frame that specifies a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.

Figure 30.3 shows the I2C bus format and Figure 30.4 shows the I2C bus timing.

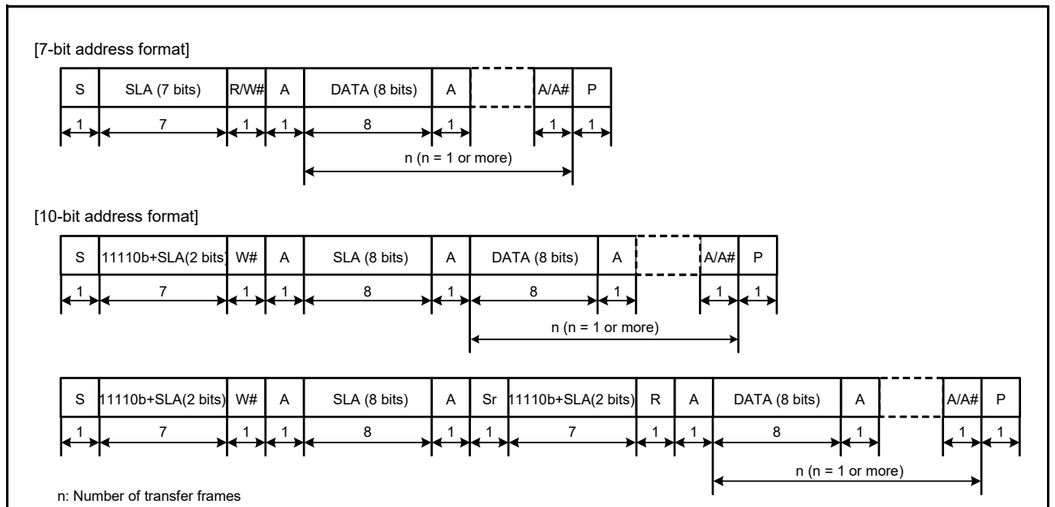


Figure 30.3 I2C bus format

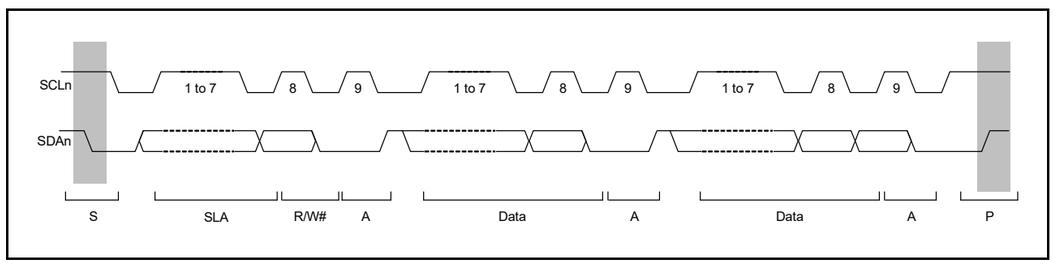


Figure 30.4 I2C bus timing (SLA = 7 bits)

30.2.19 I2C总线移位寄存器(ICDRS)

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	—	—	—	—	—	—	—	—

ICDRS是一个8位移位寄存器，用于发送和接收数据。在传输过程中，传输数据从ICDRT到ICDRS并从SDAn引脚发送。在接收过程中，接收到1个字节的数据后，数据从ICDRS传输到ICDRR。ICDRS不能直接访问。

30.3 Operation

30.3.1 通讯数据格式

I2C总线格式由8位数据和1位确认组成。开始或重启条件之后的帧是地址帧，它指定与主设备通信的从设备。指定的从站有效，直到指定新的从站或发出停止条件。

图30.3显示了I2C总线格式，图30.4显示了I2C总线时序。

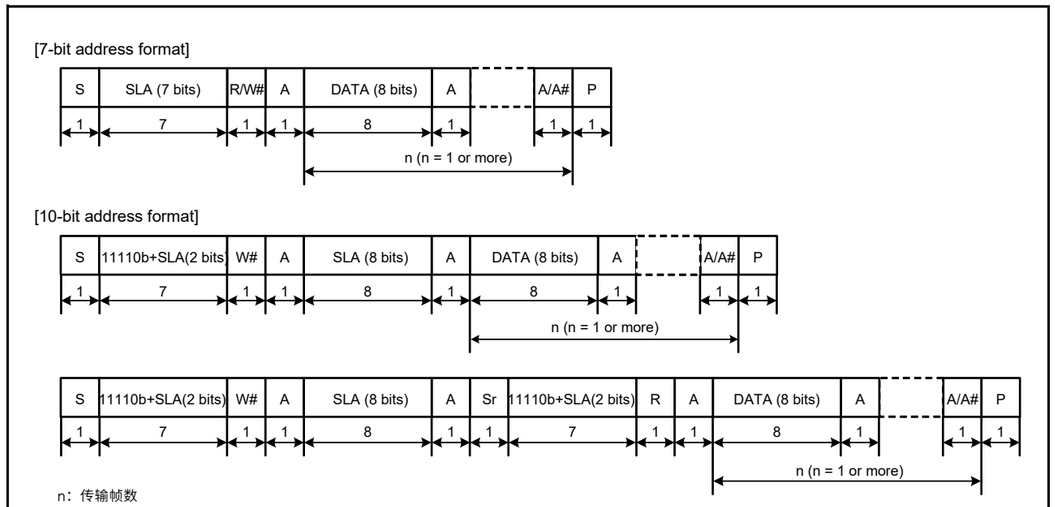


Figure 30.3 I2C总线格式

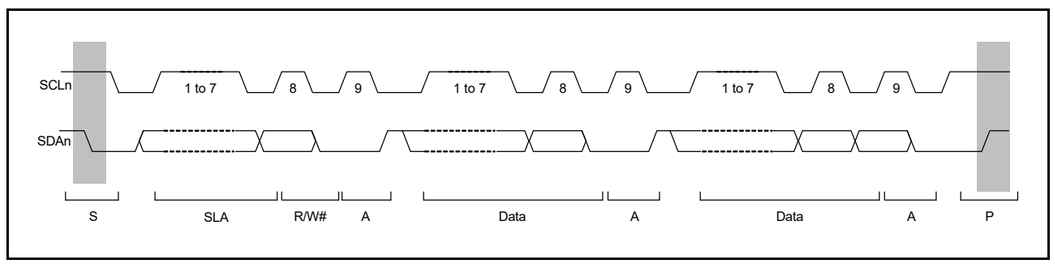


Figure 30.4 I2C总线时序（SLA=7位）

S: Start condition. The master device drives the SDAn line low from high while the SCLn line is high.

SLA: Slave address, by which the master device selects a slave device

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0

A: Acknowledge. The receive device drives the SDAn line low. In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.

A#: Not Acknowledge. The receive device drives the SDAn line high.

Sr: Restart condition. The master device drives the SDAn line low from high after the setup time elapses with the SCLn line high.

DATA: Transmitted or received data

P: Stop condition. The master device drives the SDAn line high from low while the SCLn line is high.

30.3.2 Initial Settings

Before starting data transmission or reception, initialize the IIC using the procedure shown in Figure 30.5.

1. Set the ICCR1.ICE bit to 0 to set the SCLn and SDAn pins to the inactive state.
2. Set the ICCR1.IICRST bit to 1 to initiate IIC reset.
3. Set the ICCR1.ICE bit to 1 to initiate internal reset.
4. Set the SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL registers (y = 0 to 2), and set the other registers as required. For initial settings of the IIC, see Figure 30.5.
5. When the required register settings are complete, set the ICCR1.IICRST bit to 0 to release the IIC reset.

Note: This procedure is not required if the IIC initialization is already complete.

S: 启动条件。主设备将SDAn线从高电平驱动为低电平，而SCLn线为高电平。

SLA: 从地址，主设备通过该地址选择从设备

R/W#: 指示数据传输的方向：当RW#为1时从从设备到主设备，或者当RW#为0时从主设备到从设备

A: 承认。接收设备将SDAn线驱动为低电平。在主发送模式下，从设备返回确认。
在主接收模式下，主设备返回确认。

A#: 不承认。接收设备将SDAn线驱动为高电平。

Sr: 重启条件。建立时间过后，主器件将SDAn线从高电平驱动为低电平，SCLn线为高电平。

DATA: 传输或接收的数据

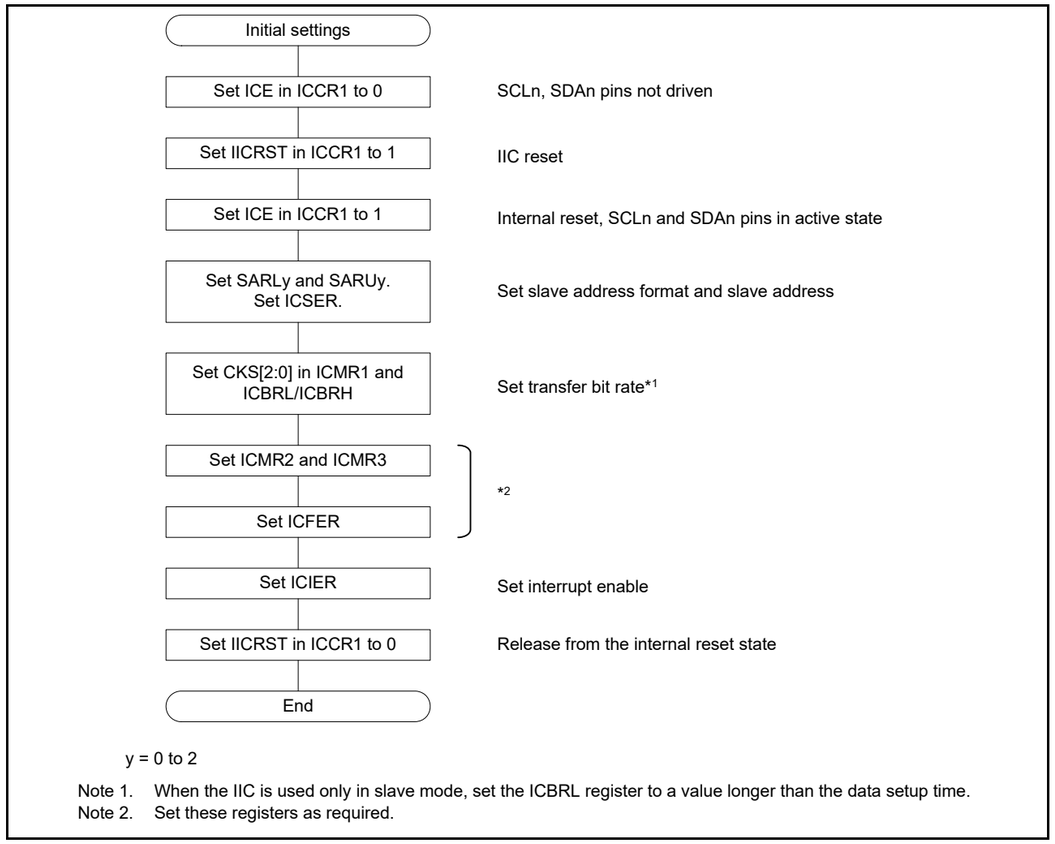
P: 停止条件。主设备将SDAn线从低电平驱动至高电平，而SCLn线为高电平。

30.3.2 初始设置

在开始数据发送或接收之前，使用图30.5所示的过程初始化IIC。

1. 将ICCR1.ICE位设置为0，将SCLn和SDAn引脚设置为无效状态。
2. 将ICCR1.IICRST位设置为1以启动IIC复位。
3. 将ICCR1.ICE位设置为1以启动内部复位。
4. 设置SARLy、SARUy、ICSER、ICMR1、ICBRH和ICBRL寄存器（y=0到2），并根据需要设置其他寄存器。IIC的初始设置见图30.5。
5. 当所需的寄存器设置完成后，将ICCR1.IICRST位设置为0以释放IIC复位。

Note: 如果IIC初始化已经完成，则不需要此过程。



Note 1. When the IIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.
Note 2. Set these registers as required.

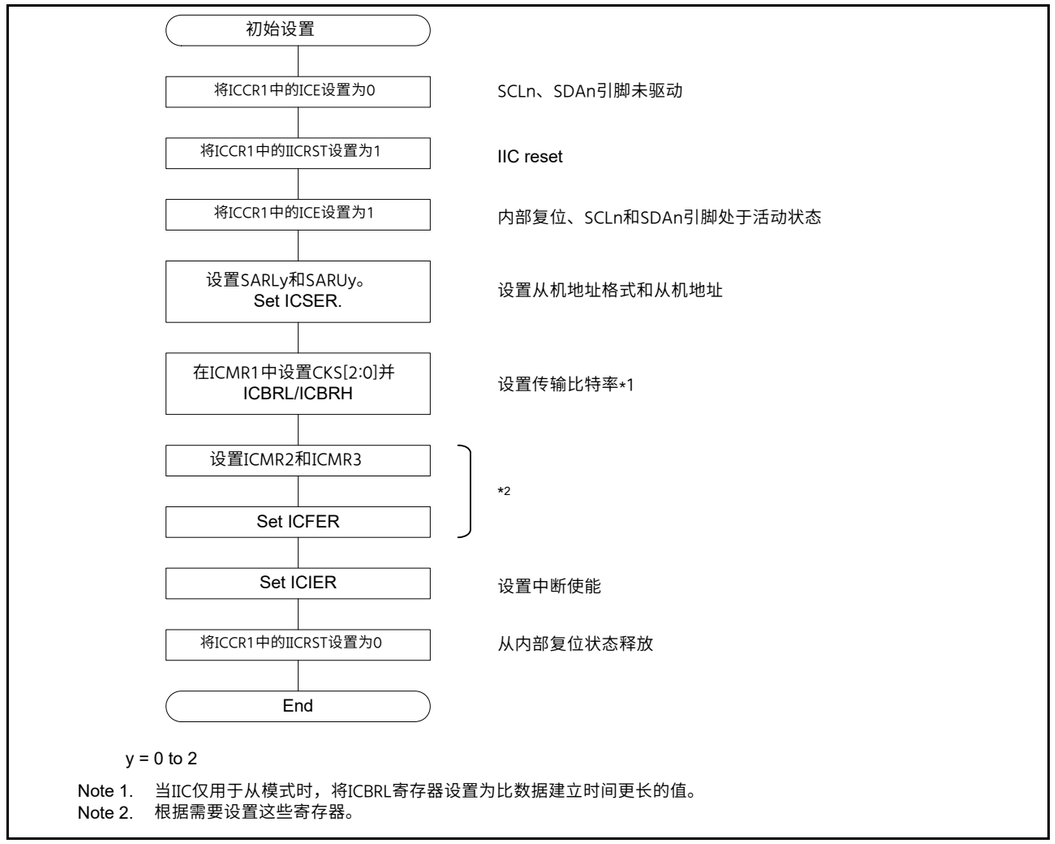
Figure 30.5 Example of IIC initialization flow

30.3.3 Master Transmit Operation

In master transmit operation, the IIC outputs the SCL clock and transmit data signals as the master device, and the slave device returns acknowledgments. Figure 30.6 shows an example of master transmission. Figure 30.7 to Figure 30.9 show the timing of operations in master transmission.

To set up and perform master transmission:

1. Initialize the IIC using the procedure described in section 30.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and START flags in ICSR2 automatically set to 1, and the ST bit is automatically set to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that the start condition requested by the ST bit has successfully completed, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is automatically set to 1 in response to setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. After the byte containing the slave address and R/W# bit is transmitted, the value of the TRS bit automatically updates to select master transmit or master receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the IIC continues in master transmit mode.
   If the ICSR2.NACKF flag is 1, indicating that no slave device recognized the address or there was an error in



Note 1. 当IIC仅用于从模式时，将ICBRL寄存器设置为比数据建立时间更长的值。
Note 2. 根据需要设置这些寄存器。

Figure 30.5 IIC初始化流程示例

30.3.3 主发送操作

在主发送操作中，IIC作为主设备输出SCL时钟和发送数据信号，从设备返回确认。图30.6显示了主传输的示例。图30.7至图30.9显示了主传输中的操作时序。

设置和执行主传输：

1. 使用第30.3.2节，初始设置中描述的程序初始化IIC。
2. 读取ICCR2中的BBSY标志以检查总线是否打开，然后将ICCR2中的ST位设置为1（启动条件请求）。收到请求后，IIC发出一个开始条件。同时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。如果检测到启动条件且SDA输出状态的内部电平与SDAn线上的电平匹配当ST位为1时，IIC识别到ST位请求的启动条件已成功完成，并且ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志自动设置为1，以响应将TRS位设置为1。
3. 检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。在发送包含从机地址和RW#位的字节后，TRS位的值会根据发送的RW#位的值自动更新以选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。如果ICSR2.NACKF标志为1，表示没有从设备识别该地址或存在错误

communications, write 1 to the ICCR2.SP bit to issue a stop condition.
To transmit data with an address in the 10-bit format, start by writing 1111 0b, the 2 upper bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower bits of the slave address to ICDRT.

4. After confirming that the TDRE flag in ICSR2 is 1, write the transmit data to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready or a stop condition is issued.
5. After all bytes of transmit data are written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1, and then set the SP bit in ICCR2 to 1 (stop condition requested). On receiving a stop condition request, the IIC issues the stop condition. For details, see section 30.11.3, Issuing a Stop Condition.
6. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. In addition, the IIC automatically sets the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
7. After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

通信，向ICCR2.SP位写入1以发出停止条件。要使用10位格式的地址传输数据，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。然后，作为第二次地址传输，将从地址的低8位写入ICDRT。

4. 确认ICSR2中的TDRE标志为1后，将发送数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到发送数据准备好或发出停止条件。
5. 将发送数据的所有字节写入ICDRT寄存器后，等待ICSR2中的TEND标志的值返回1，然后将ICCR2中的SP位设置为1（请求停止条件）。在收到停止条件请求时，IIC发出停止条件。有关详细信息，请参阅第30.11.3节，发出停止条件。
6. 在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机接收模式。此外，IIC自动将TDRE和TEND标志设置为0，并将ICSR2中的STOP标志设置为1。
7. 检查ICSR2.STOP标志为1后，将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

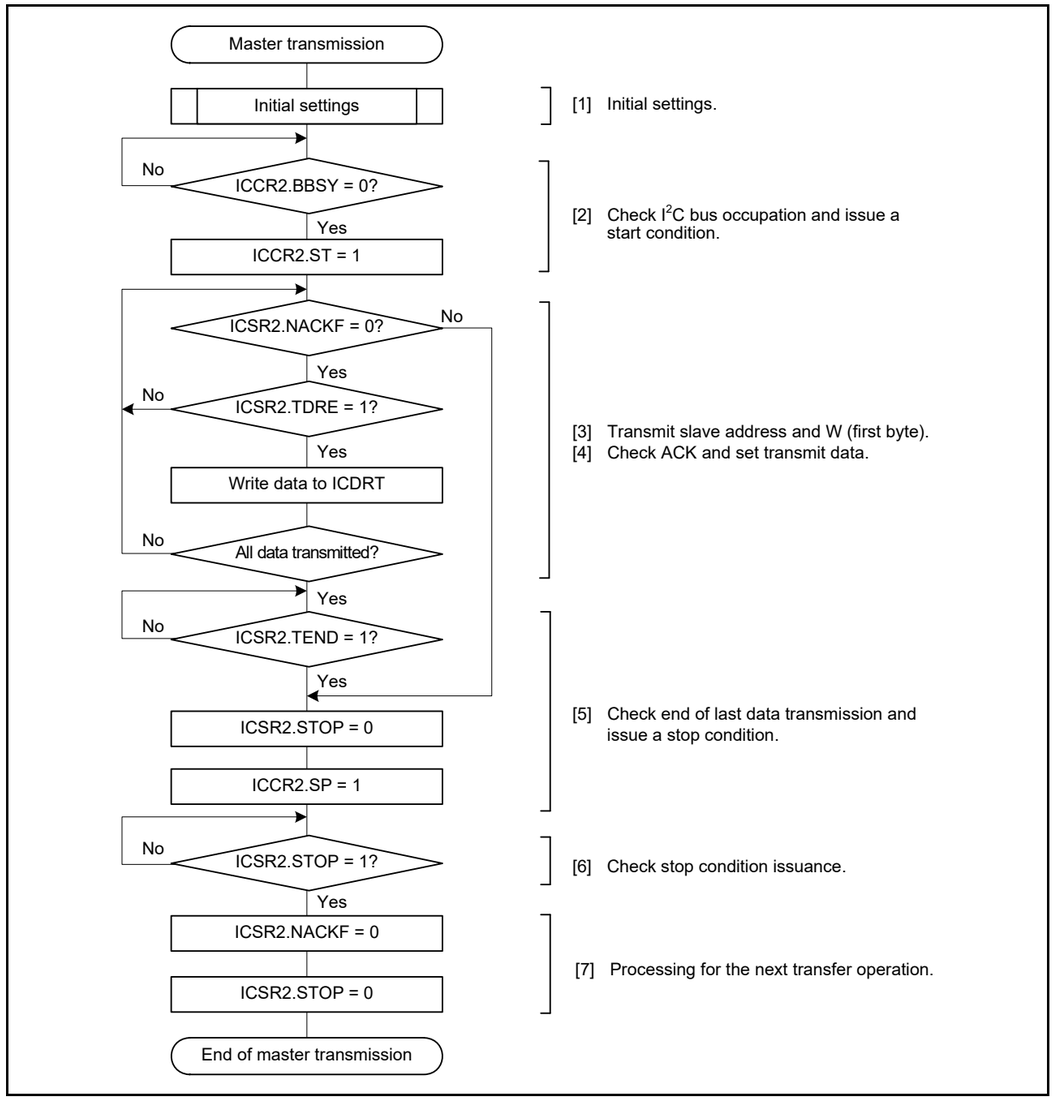


Figure 30.6 Example of master transmission flow

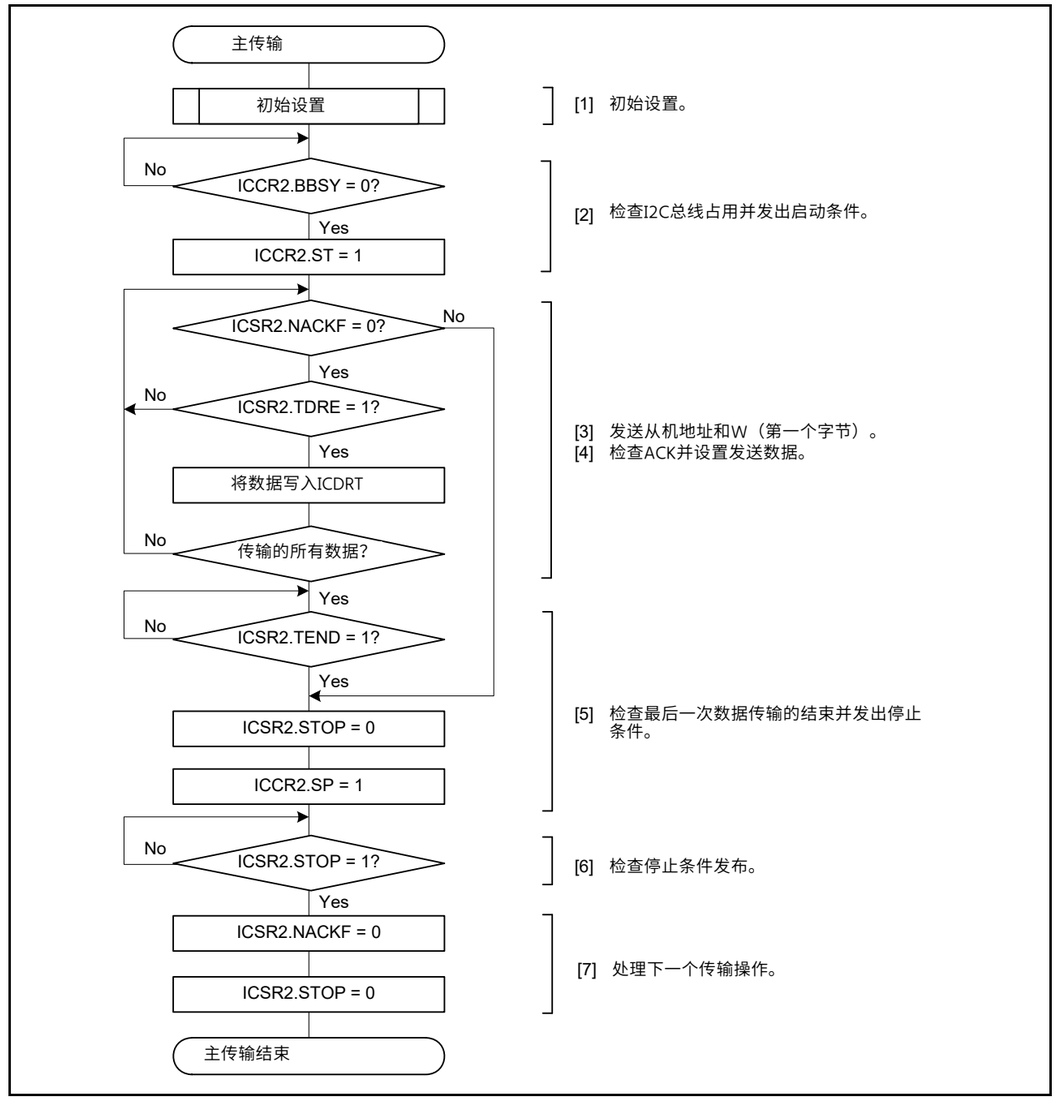


Figure 30.6 主传输流程示例

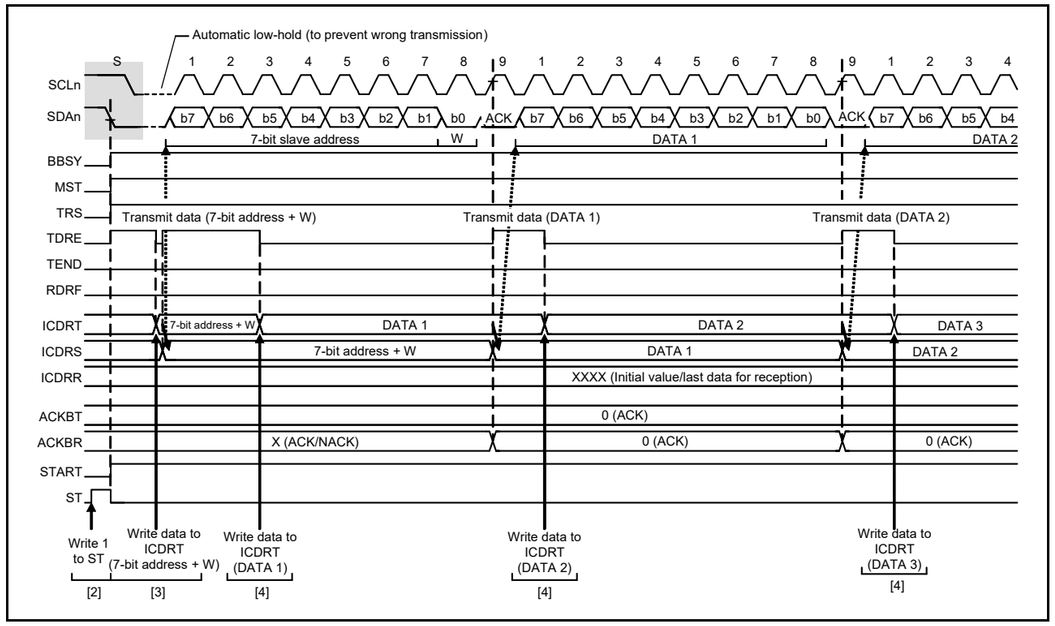


Figure 30.7 Master transmit operation timing (1) (7-bit address format)

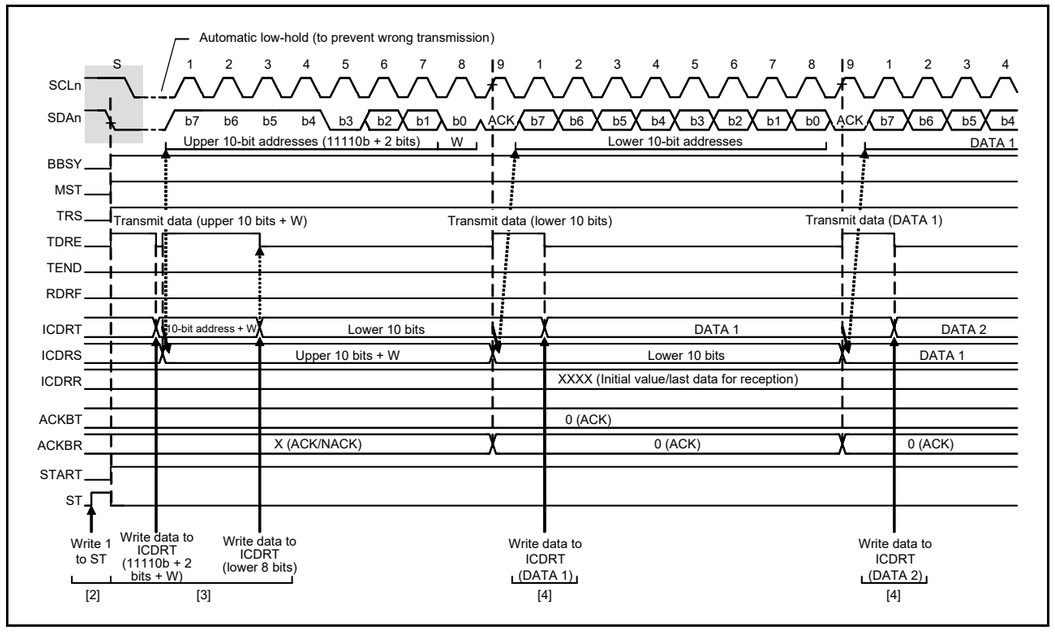


Figure 30.8 Master transmit operation timing (2) (10-bit address format)

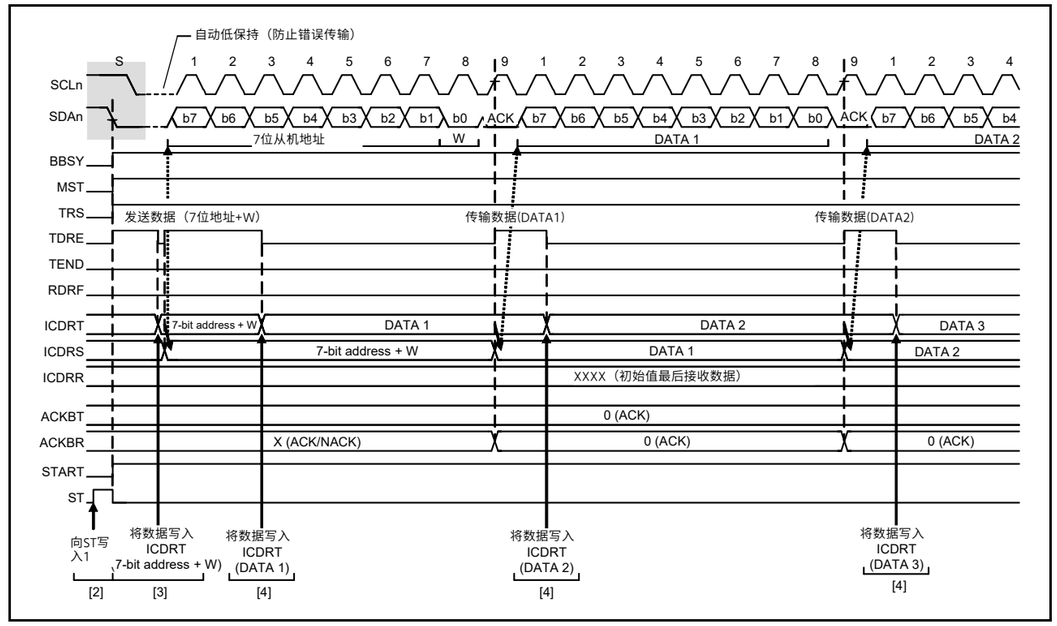


Figure 30.7 主机发送操作时序（1）（7位地址格式）

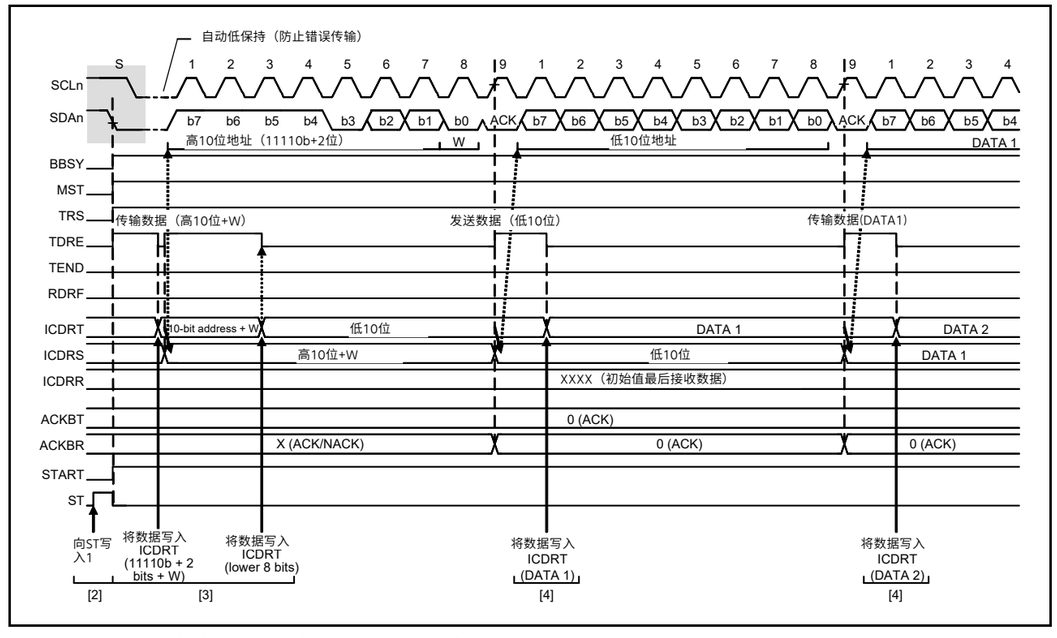


Figure 30.8 主机发送操作时序（2）（10位地址格式）

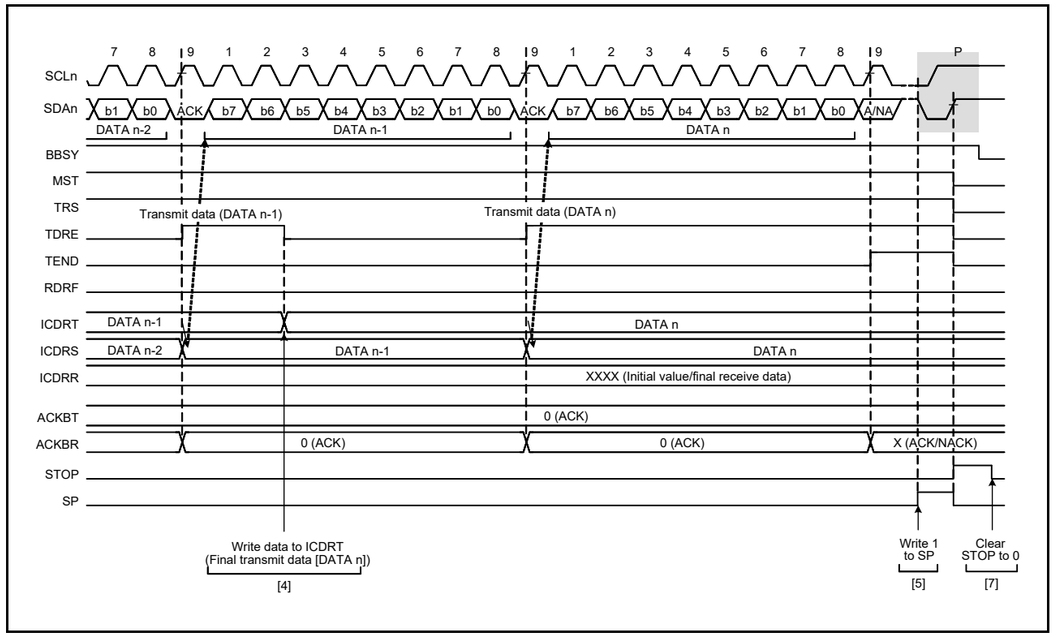


Figure 30.9 Master transmit operation timing (3)

30.3.4 Master Receive Operation

In master receive operation, the IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the IIC must start by sending a slave address to the associated slave device, the slave address phase of the procedure is performed in master transmit mode, and the subsequent steps are performed in master receive mode.

Figure 30.10 and Figure 30.11 show examples of master reception (7-bit address format). Figure 30.12 to Figure 30.14 show the timing of operations in master reception.

To set up and perform master reception:

1. Initialize the IIC using the procedure in section 30.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, and then set the ST bit in ICCR2 to 1 to request issue of a start condition. On receiving the request, the IIC issues a start condition. When the IIC detects the start condition, the BBSY flag and the START flag in ICSR2 automatically set to 1 and the ST bit is automatically set to 0. If the start condition is detected and the levels for the SDA output and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that the start condition issue is successful as requested by the ST bit, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag is set to 1. When the byte containing the slave address and R/W# bit is transmitted, the value of the ICCR2.TRS bit automatically updates to select transmit or receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 1, the TRS bit is set to 0 on the rising edge of the 9th cycle of SCL clock, placing the IIC in master receive mode. The TDRE flag is set to 0 and the ICSR2.RDRF flag is automatically set to 1.
   If the ICSR2.NACKF flag is 1, indicating that no slave device recognized the address or that there is an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmit 1111 0b, the two upper bits of the slave address, and

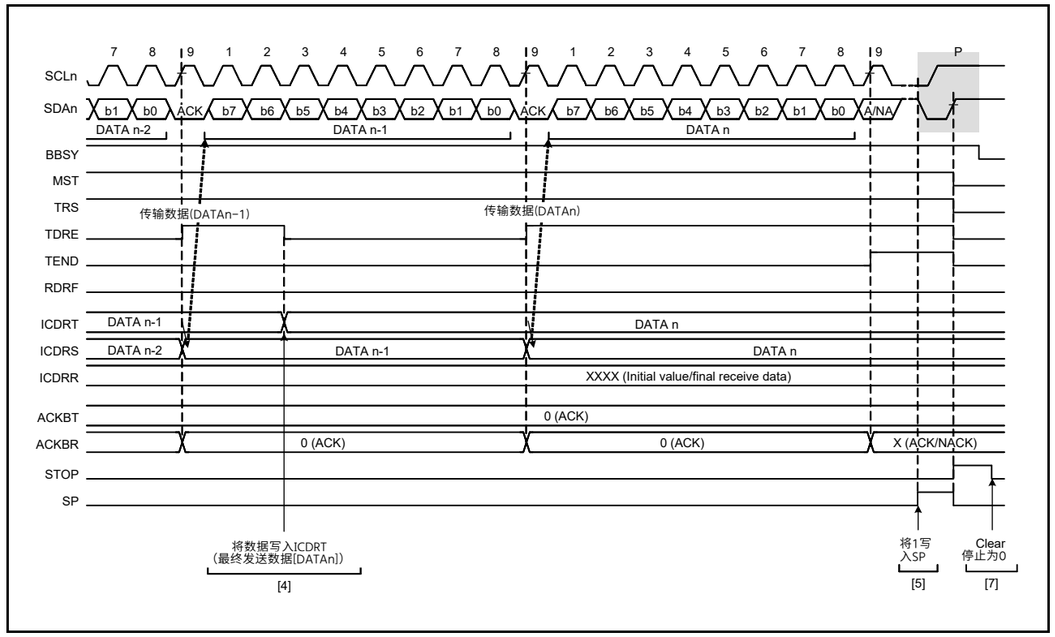


Figure 30.9 主机发送操作时序（3）

30.3.4 主接收操作

在主设备接收操作中，作为主设备的IIC输出SCL时钟，从从设备接收数据，并返回确认。因为IIC必须首先向相关的从设备发送一个从地址，所以该过程的从地址阶段在主发送模式下执行，随后的步骤在主接收模式下执行。

图30.10和图30.11显示了主机接收示例（7位地址格式）。图30.12至图30.14显示了主机接收中的操作时序。

设置和执行主接收：

1. 使用第30.3.2节，初始设置中的过程初始化IIC。
2. 读取ICCR2中的BBSY标志以检查总线是否打开，然后将ICCR2中的ST位设置为1以请求发出启动条件。收到请求后，IIC发出一个开始条件。当IIC检测到启动条件时，ICSR2中的BBSY标志和START标志自动置1，ST位自动置0。如果检测到启动条件，则SDA输出的电平和SDAn上的电平当ST位为1时，IIC识别出启动条件发出成功，ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。
3. 检查ICSR2中的TDRE标志是否为1，然后将要发送的值（第一个字节表示从机地址和RW#位的值）写入ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志设置为1。当发送包含从机地址和RW#位的字节时，ICCR2.TRS位的值会根据发送的RW#位的值自动更新以选择发送或接收模式。如果RW#位的值为1，则在SCL时钟的第9个周期的上升沿将TRS位设置为0，将IIC置于主机接收模式。TDRE标志设置为0，ICSR2.RDRF标志自动设置为1。

   如果ICSR2.NACKF标志为1，表示没有从设备识别该地址或通信中存在错误，则向ICCR2.SP位写入1以发出停止条件。对于来自具有10位地址的设备的主机接收，首先使用主机发送来发出10位地址，然后发出重启条件。之后，发送11110b，即从机地址的高两位，然后

the R bit to place the IIC in master receive mode.

4. Dummy read ICDRR after confirming that the RDRF flag in ICSR2 is 1. Doing so causes the IIC to start output of the SCL clock and start data reception.
5. After 1 byte of data is received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the 8th or 9th cycle of SCL clock, as selected by the RDRFS bit in ICMR3. Reading the ICDRR register produces the received data and automatically sets the RDRF flag to 0. The value of the acknowledgment field received during the 9th cycle of the SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 for wait insertion before reading the ICDRR register, containing the second byte from the last. In addition to enabling NACK output, even when interrupts or other operations result in delays in setting the ICMR3.ACKBT bit to 1 (NACK) in step (6), this fixes the SCLn line to low on the rising edge of the 9th clock cycle in reception of the last byte, which enables the issue of a stop condition.
6. When the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next and final byte, set the ICMR3.ACKBT bit to 1 (NACK).
7. After reading the second-to-last byte from the ICDRR register, if the value of the ICSR2.RDRF flag is 1, write 1 to the SP bit in ICCR2 (to request stop condition), and then read the last byte from ICDRR. When ICDRR is read, the IIC is released from the wait state and issues the stop condition after low-level output in the 9th clock cycle is complete or the SCLn line is released from the low-hold state.
8. On detecting the stop condition, the IIC automatically sets the ICCR2.MST and ICCR2.TRS bits to 00b and enters slave receive mode. Additionally, detection of the stop condition sets the ICSR2.STOP flag to 1.
9. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and ICSR2.STOP flags to 0 for the next transfer operation.

R位将IIC置于主机接收模式。

4. 确认ICSR2中的RDRF标志为1后虚拟读取ICDRR。这样做会导致IIC开始输出SCL时钟并开始数据接收。
5. 接收到1个字节的数据后，ICSR2中的RDRF标志在SCL时钟的第8或第9个周期的上升沿设置为1，由ICMR3中的RDRFS位选择。读取ICDRR寄存器会产生接收到的数据并自动将RDRF标志设置为0。在SCL时钟的第9个周期内接收到的确认字段的值作为ICMR3.ACKBT位中设置的值返回。如果要接收的下一个字节是倒数第二个字节，则将ICMR3.WAIT位设置为1以等待插入，然后再读取包含倒数第二个字节的ICDRR寄存器。除了启用NACK输出之外，即使在中断或其他操作导致在步骤(6)中将ICMR3.ACKBT位设置为1(NACK)时出现延迟，这也会在第9个时钟的上升沿将SCLn线固定为低循环接收最后一个字节，这使得发出停止条件。
6. 当ICMR3.RDRFS位为0且必须通知从设备在传输下一个和最后一个字节后结束数据接收传输时，将ICMR3.ACKBT位设置为1(NACK)。
7. 从ICDRR寄存器读取倒数第二个字节后，如果ICSR2.RDRF标志的值为1，则将1写入ICCR2中的SP位（请求停止条件），然后从ICDRR读取最后一个字节。当读取ICDRR时，IIC从等待状态中释放，并在第9个时钟周期的低电平输出完成或SCLn线从低保持状态释放后发出停止条件。
8. 在检测到停止条件时，IIC自动将ICCR2.MST和ICCR2.TRS位设置为00b并进入从机接收模式。此外，检测到停止条件会将ICSR2.STOP标志设置为1。
9. 检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和ICSR2.STOP标志设置为0以进行下一次传输操作。

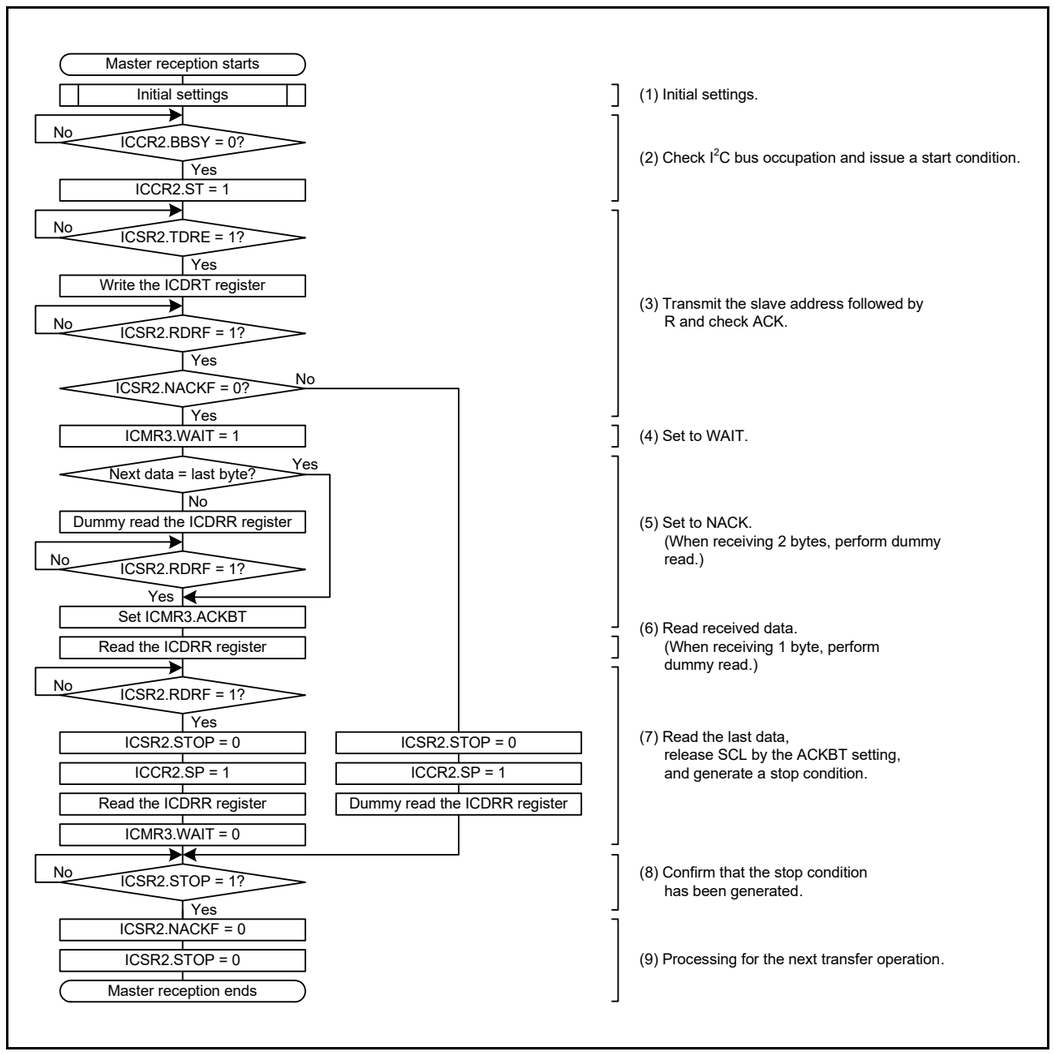


Figure 30.10 Example of master reception flow with 7-bit address format, and 1 or 2 bytes

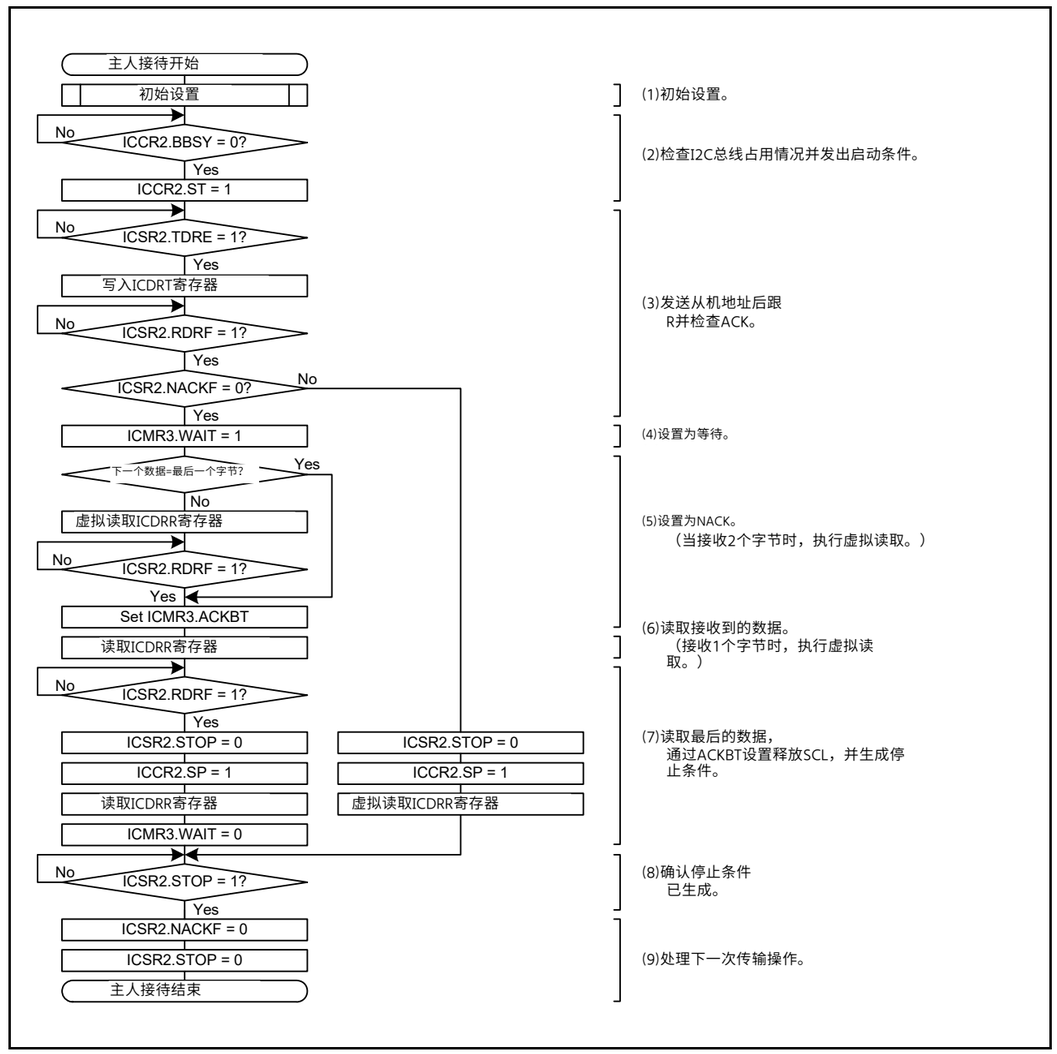


Figure 30.10 具有7位地址格式和1或2字节的主机接收流程示例

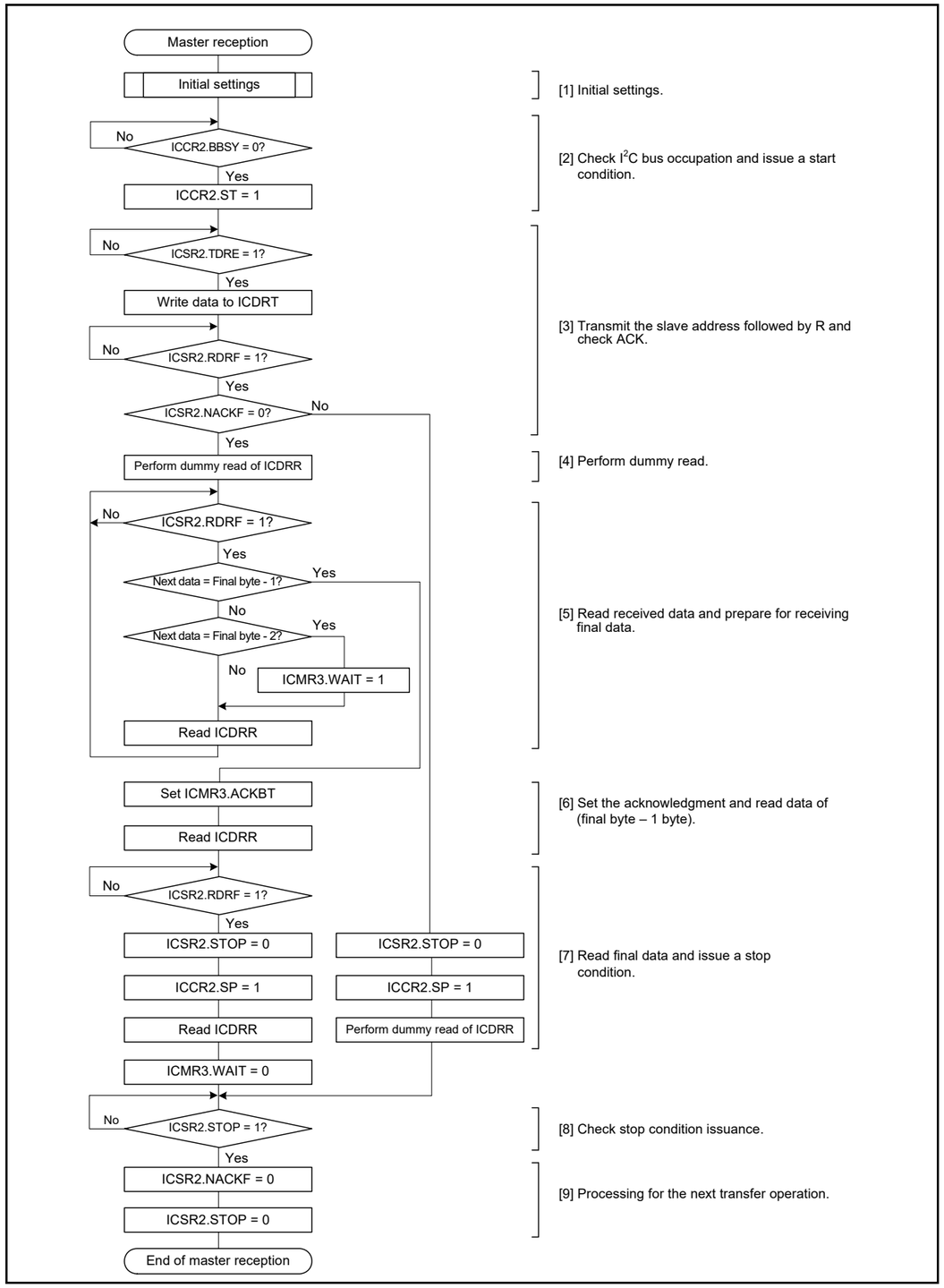


Figure 30.11 Example of master reception flow with 7-bit address format, and 3 bytes or more

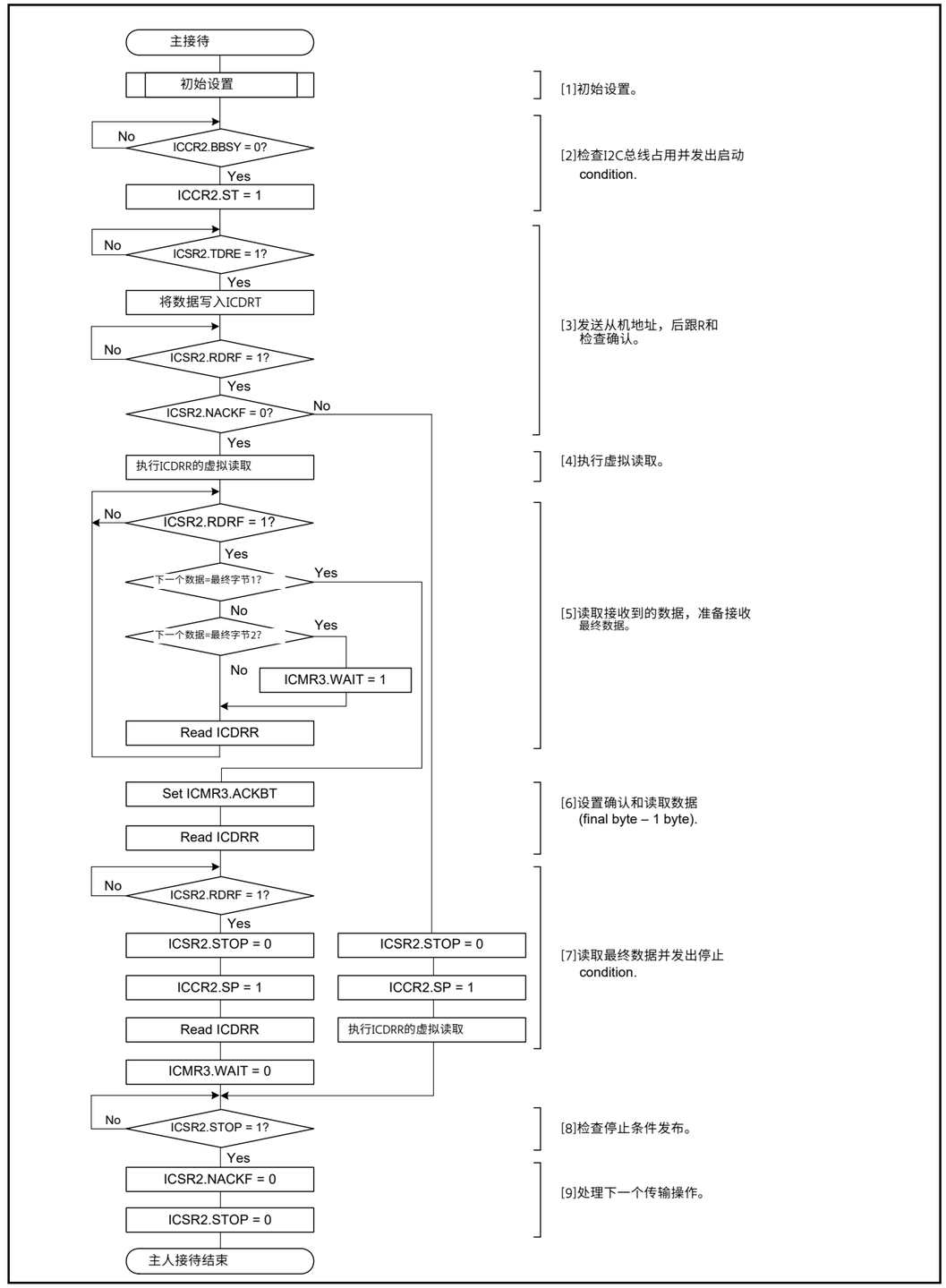


Figure 30.11 具有7位地址格式和3字节或更多字节的主机接收流程示例

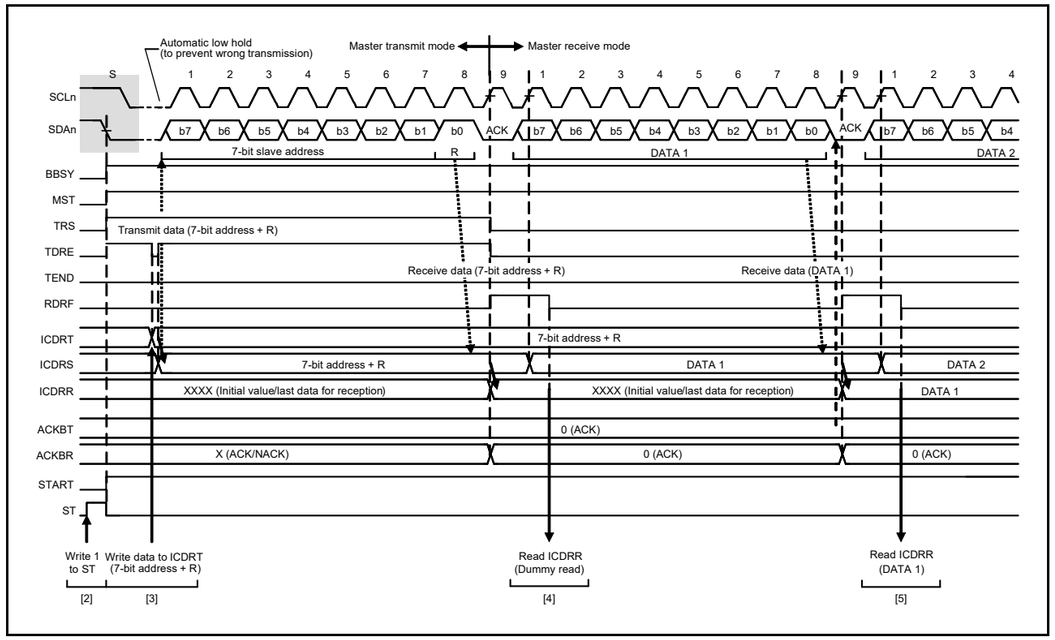


Figure 30.12 Master receive operation timing (1) with 7-bit address format when RDRFS = 0

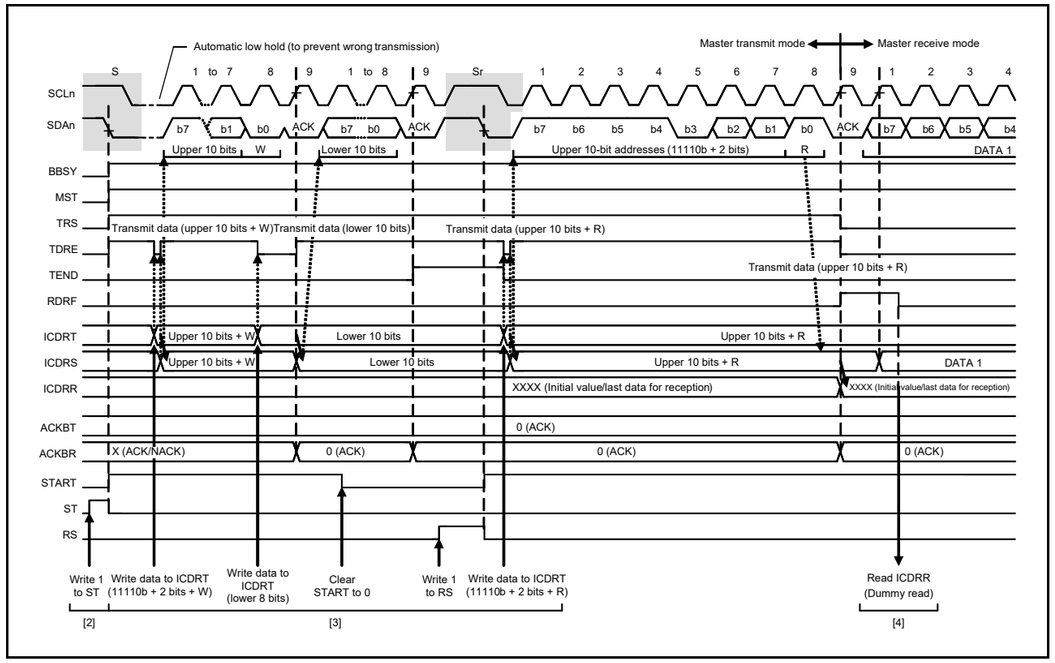


Figure 30.13 Master receive operation timing (2) with 10-bit address format when RDRFS = 0

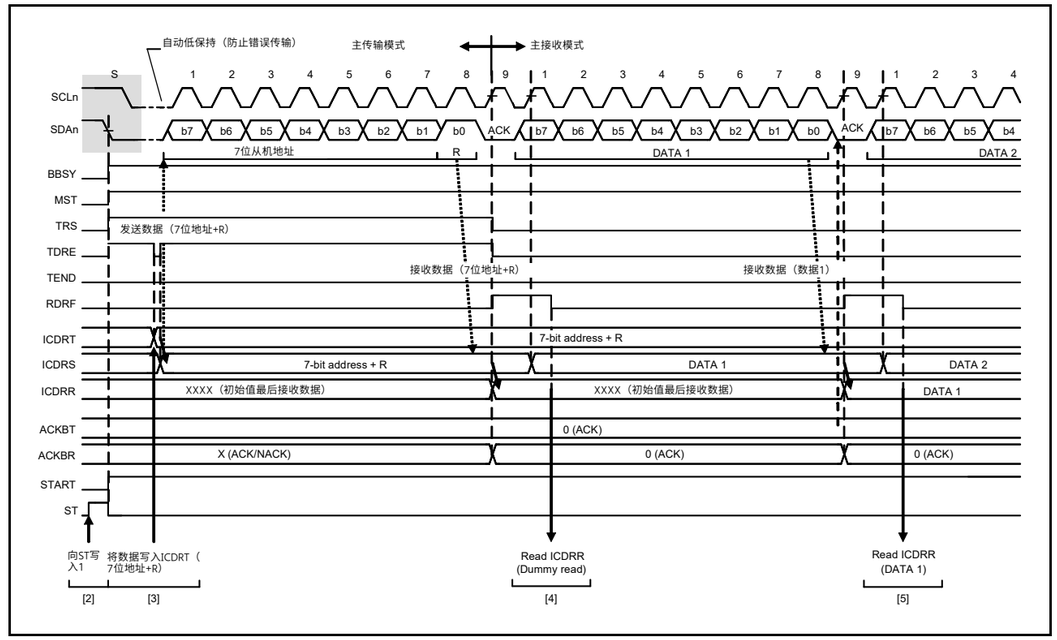


Figure 30.12 RDRFS=0时采用7位地址格式的主机接收操作时序(1)

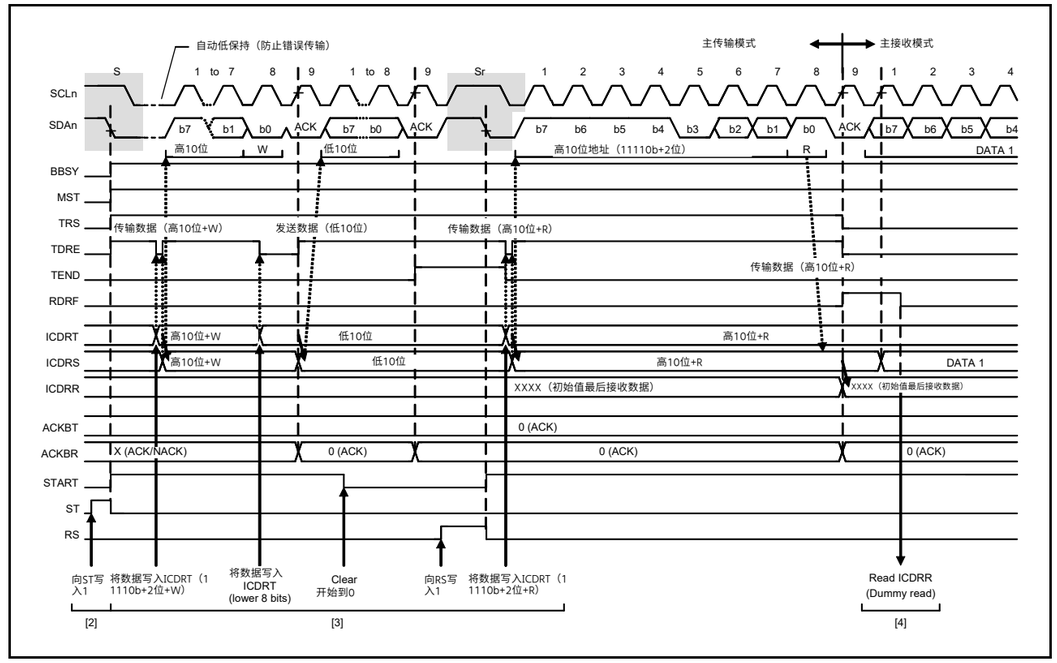


Figure 30.13 RDRFS=0时10位地址格式的主机接收操作时序(2)

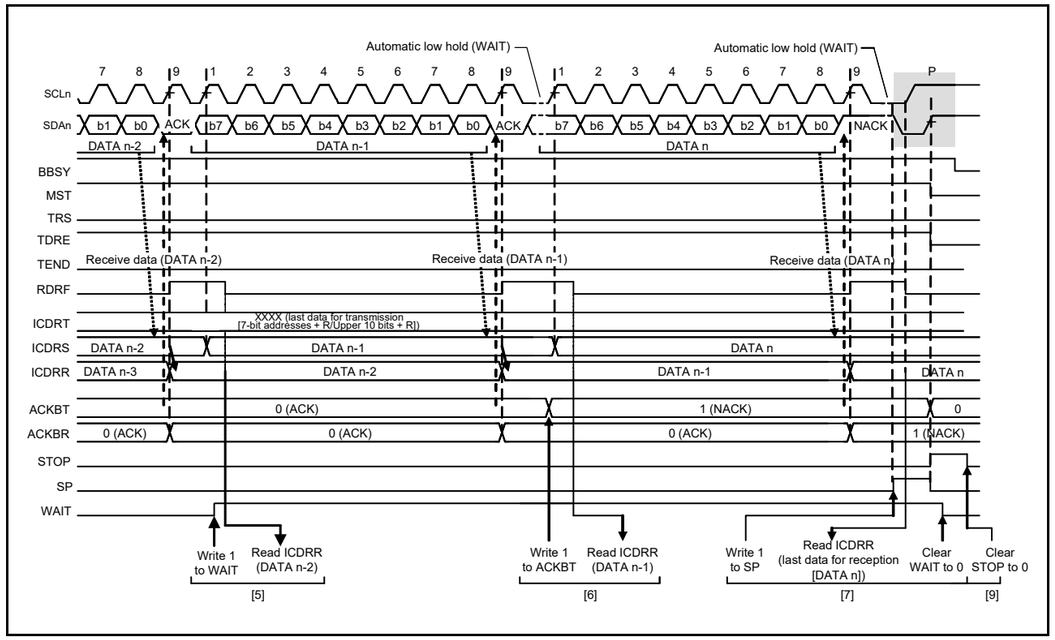


Figure 30.14 Master receive operation timing (3) when RDRFS = 0

30.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the IIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 30.15 shows an example of slave transmission. Figure 30.16 and Figure 30.17 show the operation timing in slave transmission.

To set up and perform slave transmission:

1. To initialize the IIC, follow the procedure in section 30.3.2, Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, the IIC sets one of the associated bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 1 on the rising edge of the 9th cycle of SCL clock and outputs the value set in the ICMR3.ACKBT bit as the acknowledge bit on the 9th cycle of SCL clock. If the value of the received R/W# bit is 1, the IIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.
3. Check that the ICSR2.TEND flag is 1, and write the transmit data to the ICDRT register. If the IIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the IIC suspends transfer of the next data.
4. Wait unit the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the IIC drives the SCLn line low on the 9th falling edge of SCL clock.
5. When the ICSR2.NACKF flag or the ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.
6. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy (y = 0 to 2) bits, the ICSR2.TDRE and TEND flags, and the ICCR2.TRS bit to 0, and enters slave receive mode.
7. Check that the ICSR2.STOP flag is 1, and set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

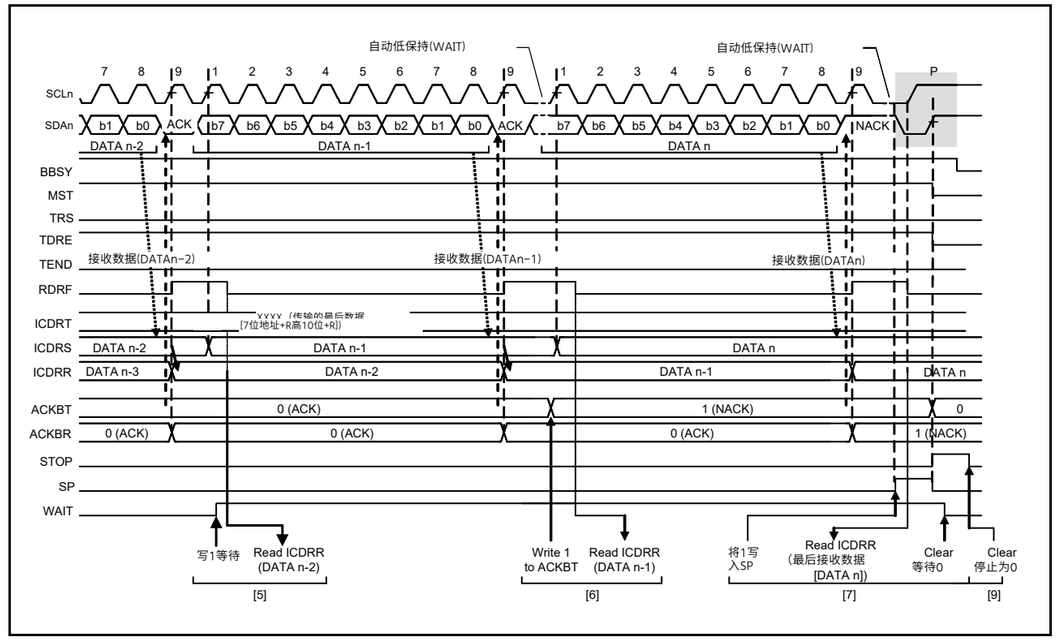


Figure 30.14 RDRFS=0时的主机接收操作时序(3)

30.3.5 从机发送操作

在从发送操作中，主设备输出SCL时钟，IIC作为从设备发送数据，主设备返回确认。

图30.15显示了从机传输的示例。图30.16和图30.17显示了从机传输中的操作时序。

设置和执行从属传输：

1. 要初始化IIC，请按照第30.3.2节，初始设置中的程序进行操作。
   初始化后，IIC一直处于待机状态，直到收到匹配的从机地址。
2. 接收到匹配的从地址后，IIC在SCL时钟的第9个周期的上升沿将相关位ICSR1.HOA、GCA和AASy（y=0到2）之一设置为1，并输出设置的值ICMR3.ACKBT位作为SCL时钟第9个周期的确认位。如果接收到的RW#位的值为1，则IIC通过将ICCR2.TRS位和ICSR2.TDRE标志都设置为1自动将自己置于从发送模式。
3. 检查ICSR2.TEND标志是否为1，并将发送数据写入ICDRT寄存器。如果IIC在ICFER.NACKE位为1时没有收到来自主设备的确认（接收到NACK信号），则IIC暂停下一个数据的传输。
4. 等待单元ICSR2.TEND标志设置为1，而ICSR2.TDRE标志为1，在ICSR2.NACKF标志设置为1或发送的最后一个字节写入ICDRT寄存器之后。当ICSR2.NACKF标志或TEND标志为1时，IIC在SCL时钟的第9个下降沿将SCLn线驱动为低电平。
5. 当ICSR2.NACKF标志或ICSR2.TEND标志为1时，假读ICDRR以完成处理。这将释放SCLn线。
6. 在检测到停止条件时，IIC自动设置ICSR1.HOA、GCA和AASy（y=0到2）位，即ICSR2.TDRE和TEND标志位，且ICCR2.TRS位为0，进入从机接收模式。
7. 检查ICSR2.STOP标志是否为1，并将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

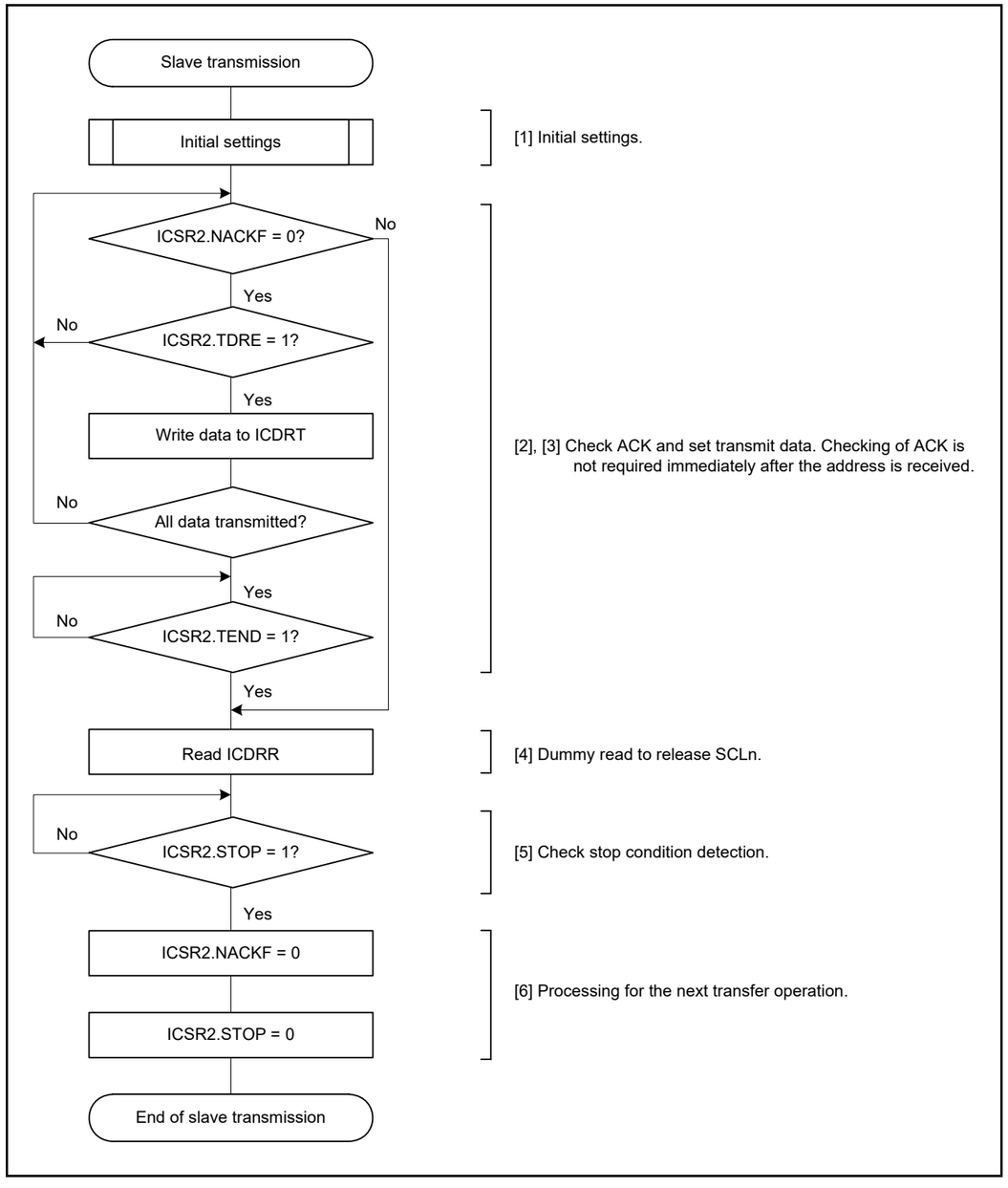


Figure 30.15 Example of slave transmission flow

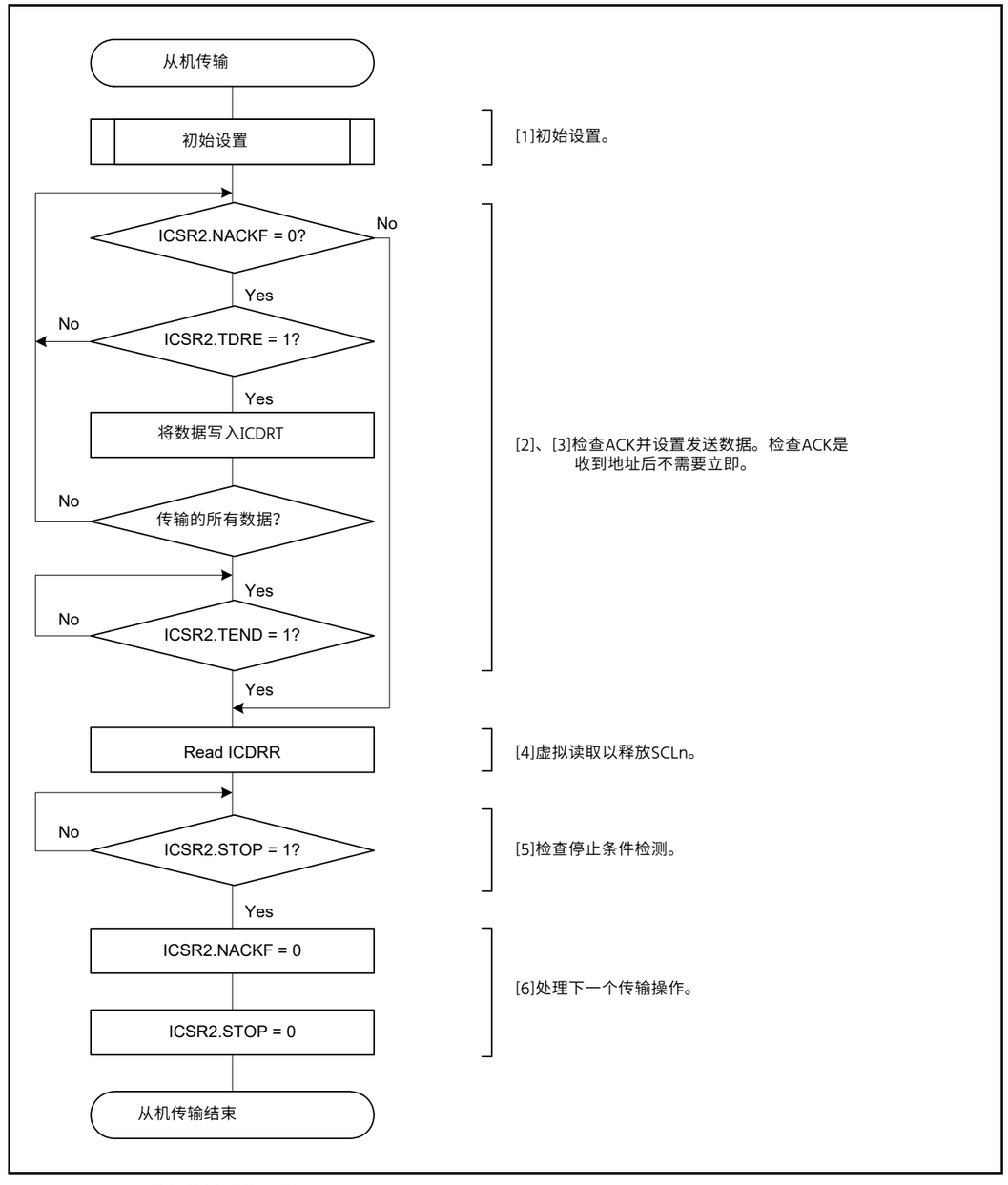


Figure 30.15 从机传输流程示例

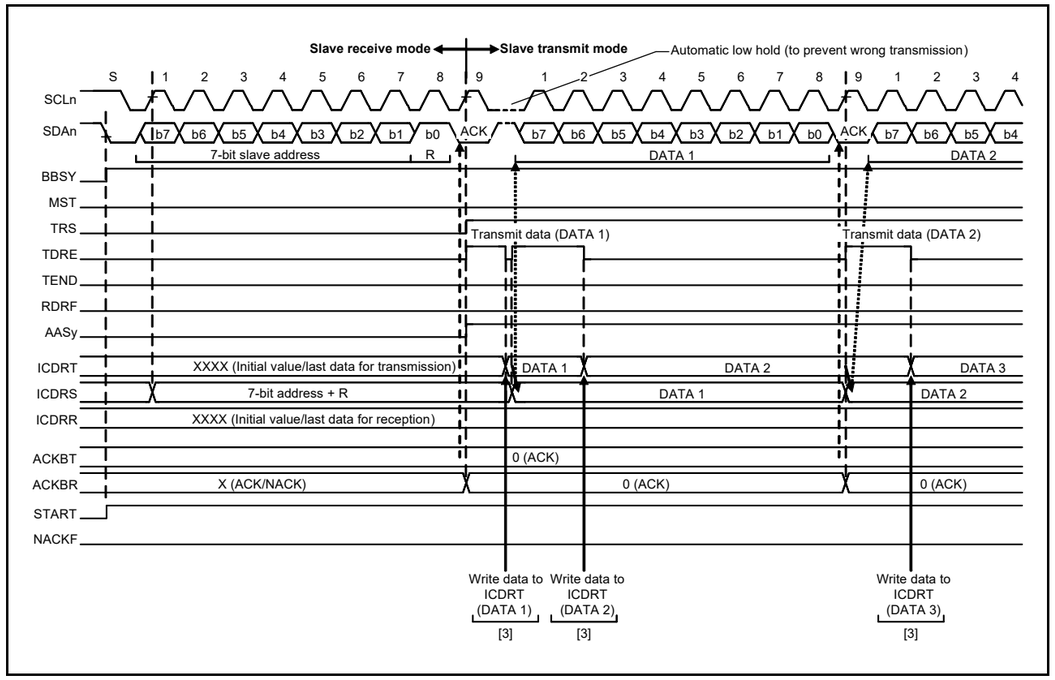


Figure 30.16 Slave transmit operation timing (1) with 7-bit address format

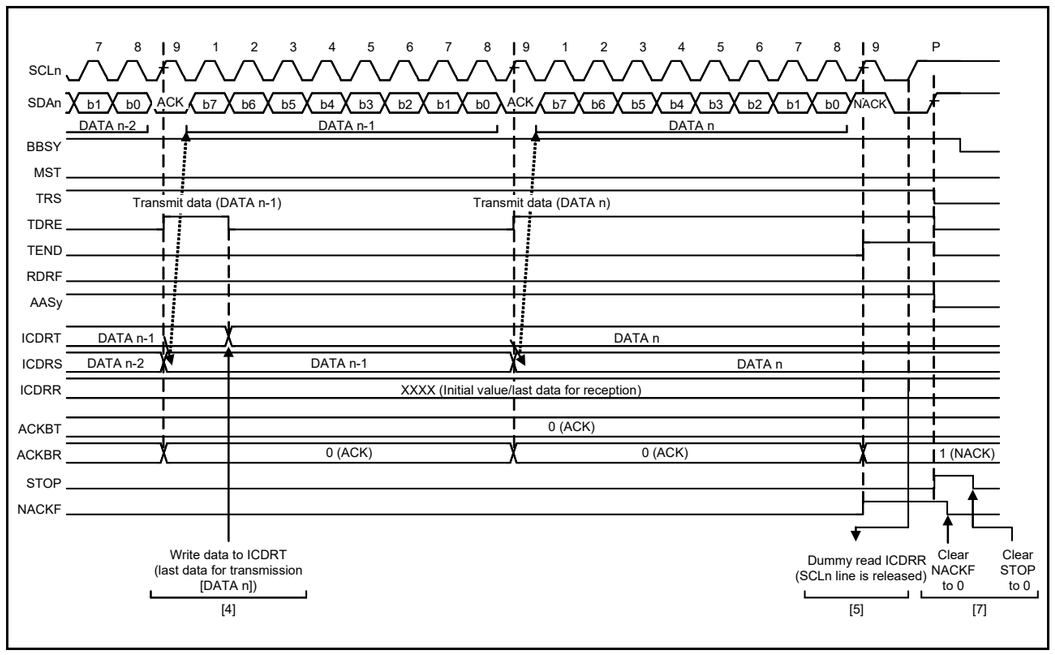


Figure 30.17 Slave transmit operation timing (2)

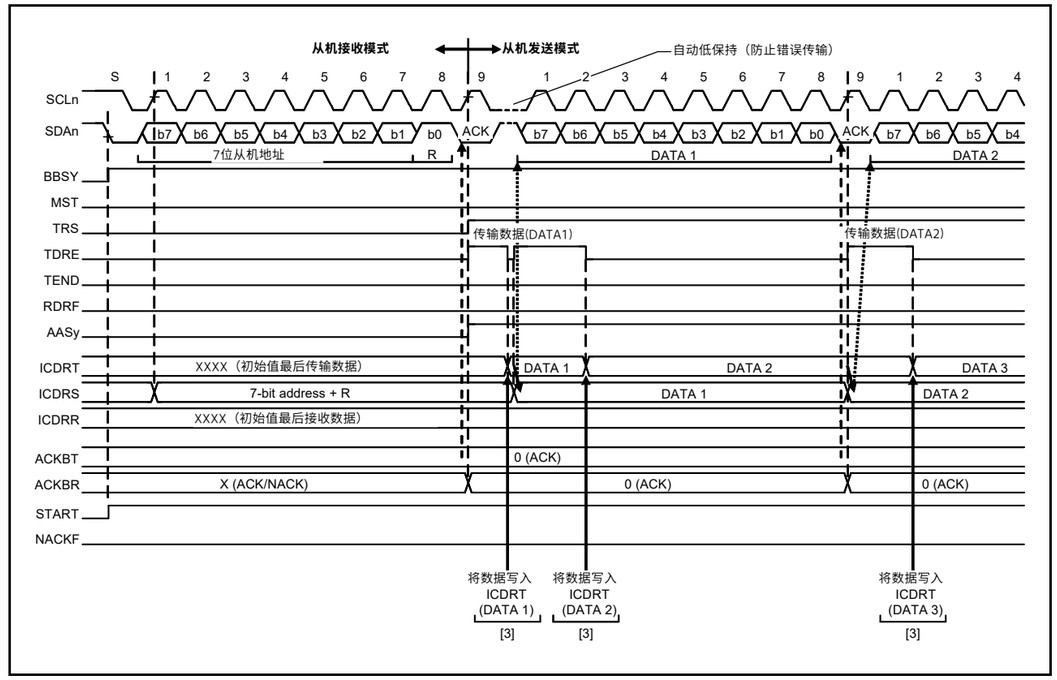


Figure 30.16 7位地址格式的从机发送操作时序(1)

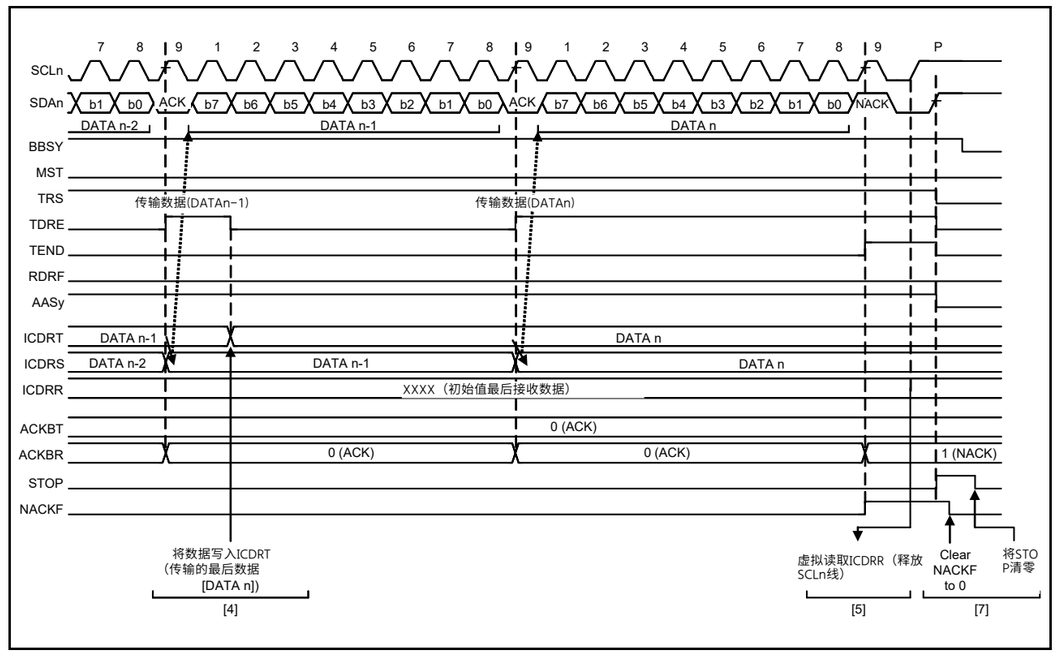


Figure 30.17 从机发送操作时序（2）

30.3.6 Slave Receive Operation

In a slave receive operation, the master device outputs the SCL clock and transmit data, and the IIC returns acknowledgments as a slave device.

Figure 30.18 shows an example of slave reception. Figure 30.19 and Figure 30.20 show the timing of operations in slave reception.

To set up and perform slave reception:

1. To initialize the IIC, follow the procedure in section 30.3.2, Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy (y = 0 to 2) bits to 1 on the rising edge of the 9th cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the 9th cycle of the SCL clock. If the value of the received R/W# bit is 0, the IIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.
3. Check that the ICSR2.STOP flag is 0 and the ICSR2.RDRF flag is 1, and then dummy read the ICDRR register. The dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected.
4. When ICDRR is read, the IIC automatically sets the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and the next byte is received while the RDRF flag is still set to 1, the IIC holds the SCLn line low until 1 SCL cycle before the point where RDRF must be set. In this case, reading the ICDRR register releases the SCLn line from being held low.
   When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read the ICDRR register until all the data is completely received.
5. On detecting the stop condition, the IIC automatically clears the ICSR1.HOA, GCA, and AASy (y = 0 to 2) bits to 0.
6. Check that the ICSR2.STOP flag is 1, then set the ICSR2.STOP flag to 0 for the next transfer operation.

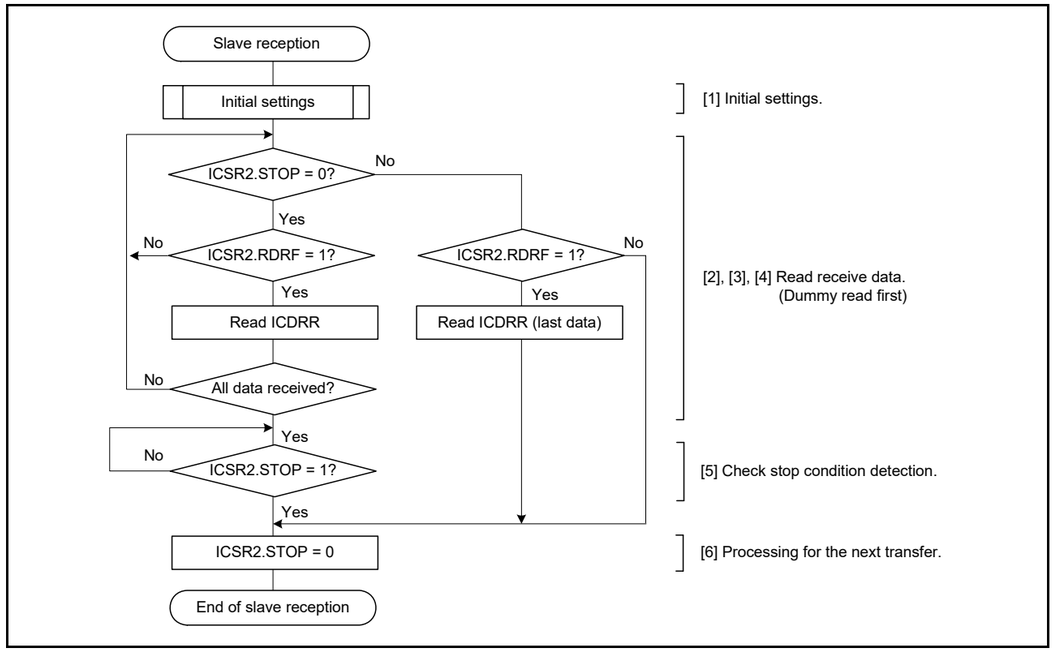


Figure 30.18 Example slave reception flow

30.3.6 从机接收操作

在从机接收操作中，主设备输出SCL时钟并发送数据，IIC作为从设备返回确认。

图30.18显示了从机接收的示例。图30.19和图30.20显示了从机接收中的操作时序。

设置和执行从属接收：

1. 要初始化IIC，请按照第30.3.2节，初始设置中的程序进行操作。
   初始化后，IIC一直处于待机状态，直到收到匹配的从机地址。
2. 接收到匹配的从地址后，IIC在SCL时钟的第9个周期的上升沿将相关的ICSR1.HOA、GCA和AASy（y=0到2）位之一设置为1，并输出设置的值在ICMR3.ACKBT位到SCL时钟的第9个周期的确认位。如果接收到的RW#位的值为0，则IIC继续将自身置于从接收模式并将ICSR2中的RDRF标志设置为1。
3. 检查ICSR2.STOP标志为0且ICSR2.RDRF标志为1，然后伪读取ICDRR寄存器。Thedummyvalueconsistsofthe slaveaddressandRW#bitwhenthe7-bitaddressformatisselected orthelower8bitswhenthe10-bitaddressformatisselected.
4. 读取ICDRR时，IIC自动将ICSR2.RDRF标志设置为0。如果ICDRR的读取延迟并且在RDRF标志仍设置为1时接收到下一个字节，则IIC将SCLn线保持为低电平直到1个SCL周期在必须设置RDRF之前。在这种情况下，读取ICDRR寄存器会释放SCLn线的低电平。当ICSR2.STOP标志为1且ICSR2.RDRF标志也为1时，读取ICDRR寄存器，直到完全接收到所有数据。
5. 在检测到停止条件时，IIC自动将ICSR1.HOA、GCA和AASy（y=0到2）位清零。
6. 检查ICSR2.STOP标志是否为1，然后将ICSR2.STOP标志设置为0以进行下一次传输操作。

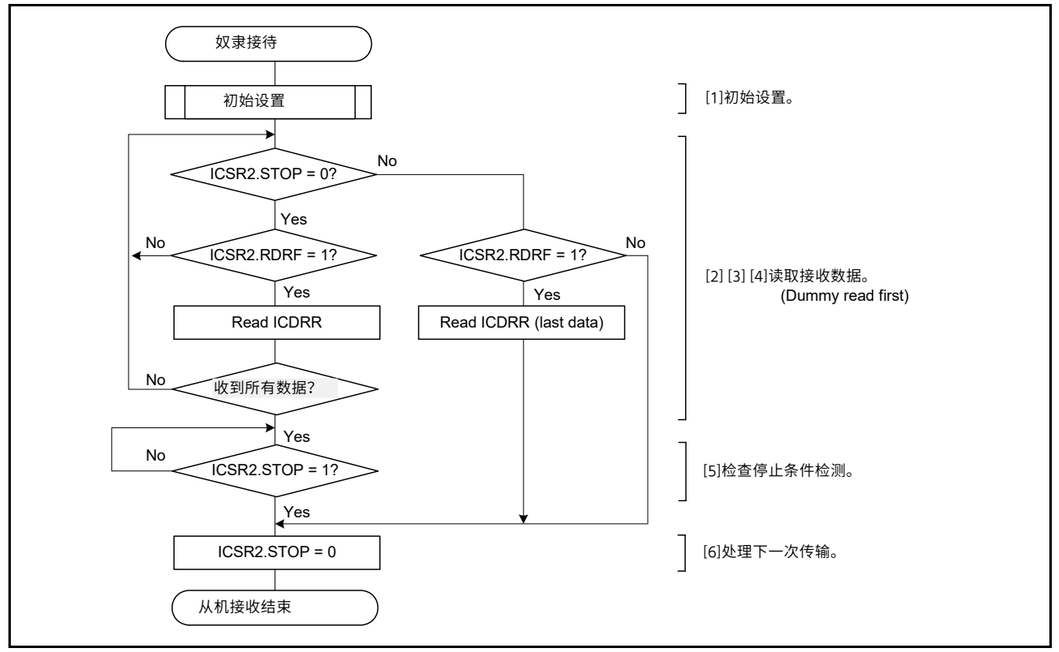


Figure 30.18 从机接收流程示例

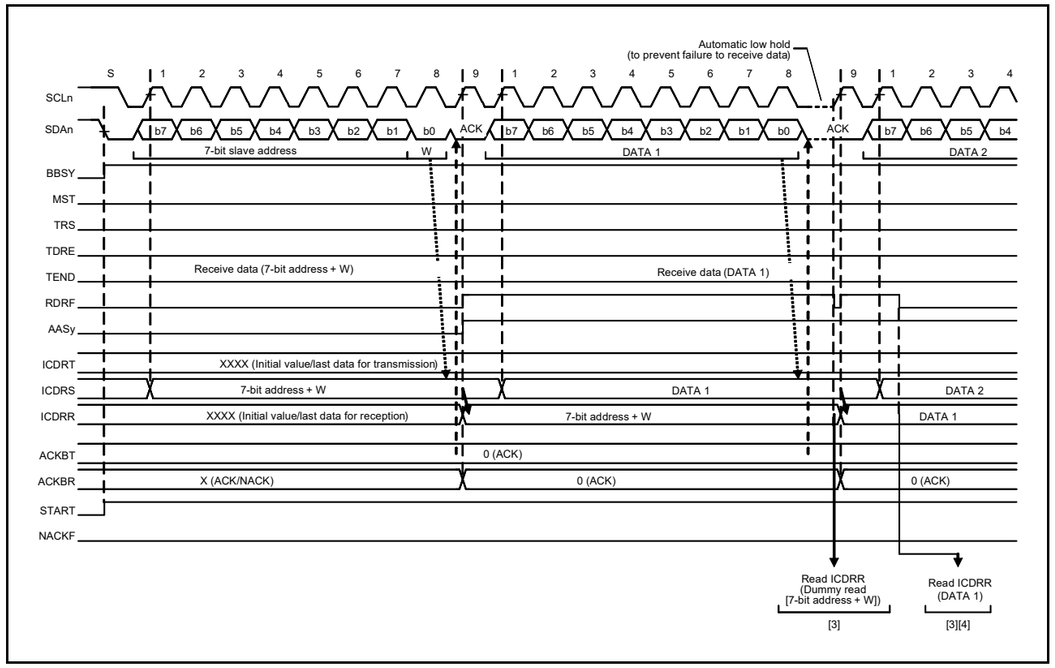


Figure 30.19 Slave receive operation timing (1) with 7-bit address format when RDRFS = 0

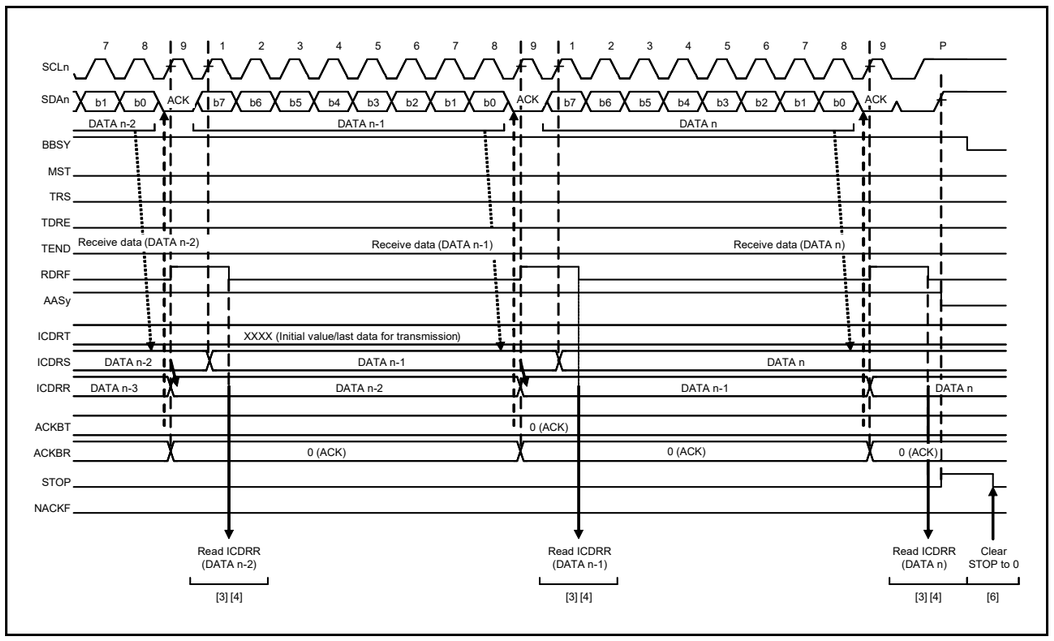


Figure 30.20 Slave receive operation timing (2) when RDRFS = 0

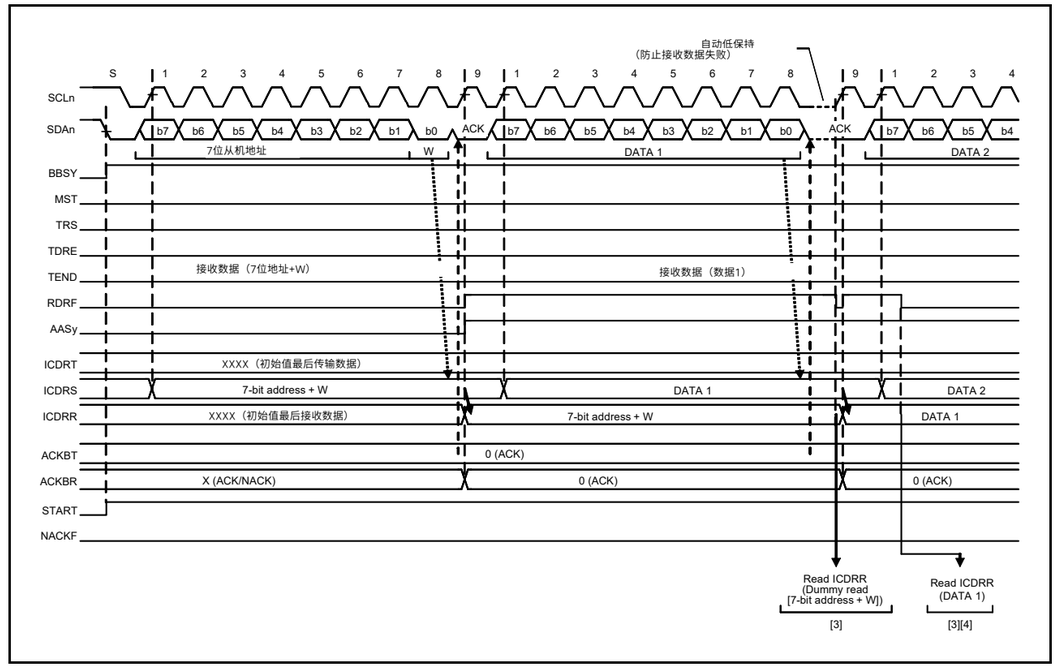


Figure 30.19 RDRFS=0时7位地址格式的从机接收操作时序(1)

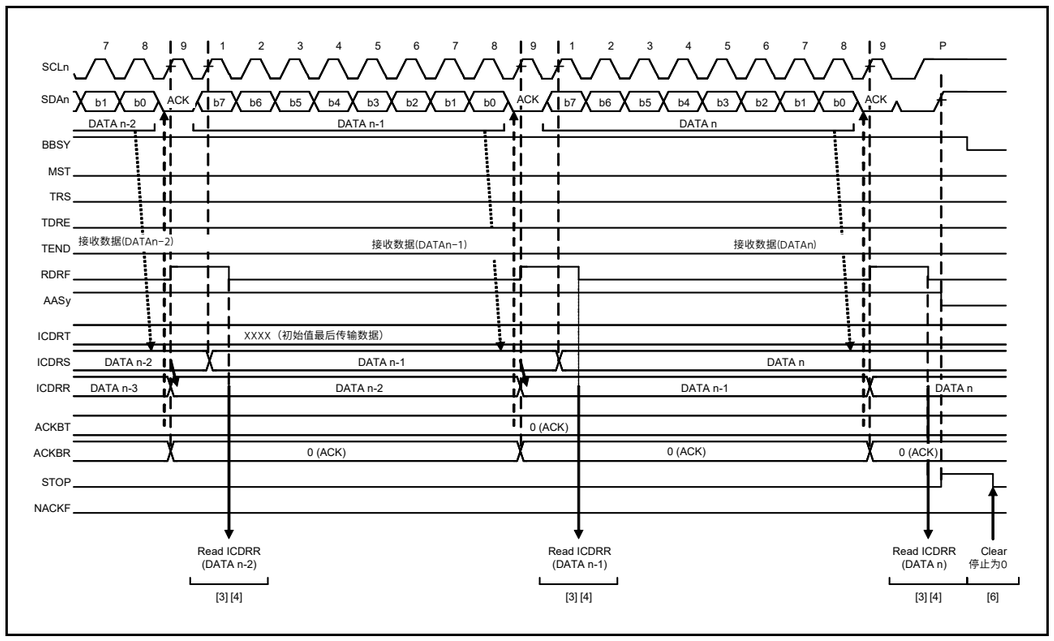


Figure 30.20 RDRFS=0时的从机接收操作时序(2)

30.4 SCL Synchronization Circuit

To generate the SCL clock, the IIC starts counting the value for the high-level period specified in ICBRH when it detects a rising edge on the SCLn line and drives the SCLn line low when it completes counting. When the IIC detects the falling edge of the SCLn line, it starts counting the value for the low-level period specified in ICBRL, and then stops driving the SCLn line (releases the line) when it completes counting. The IIC repeats this process to generate the SCL clock.

If multiple master devices are connected to the I2C bus, a collision of SCL signals might arise because of contention with another master device. In such cases, the master devices must synchronize their SCL signals. Because this synchronization of SCL signals must be bit-by-bit, the IIC includes an SCL synchronization circuit to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the IIC detects a rising edge on the SCLn line and starts counting the high-level period specified in ICBRH, and the level on the SCLn line falls because an SCL signal is being generated by another master device, the IIC performs the following:

1. Stops counting when it detects the falling edge.
2. Drives the level on the SCLn line low.
3. Starts counting the low-level period specified in ICBRL.

When the IIC finishes counting the low-level period, it stops driving the SCLn line low. If the low-level period of the SCL clock signal from the other master device is longer than the low-level period set in the IIC, the low-level period of the SCL signal is extended. If the low-level period for the other master device ends, the SCL signal rises because the SCLn line is released.

When the IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, when SCL signals from more than one master are contending, the high-level period of the SCL signal is synchronized with that of the clock with the narrower period, and the low-level period of the SCL signal is synchronized with that of the clock with the broader period. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

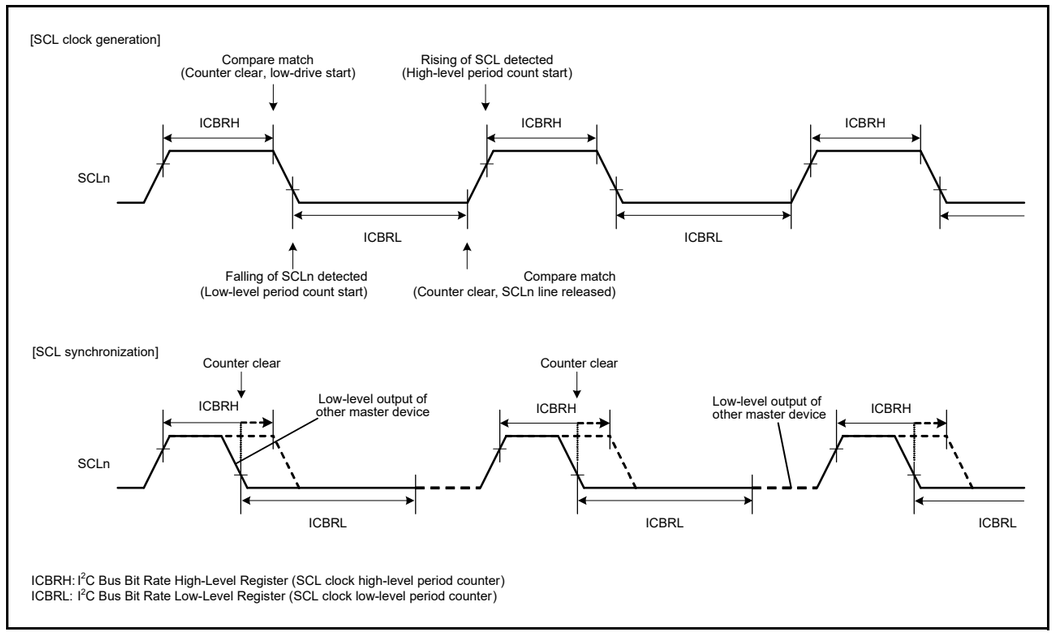


Figure 30.21 Generation and synchronization of SCL signal from IIC

30.4 SCL同步电路

为了生成SCL时钟，IIC在检测到SCLn线上的上升沿时开始对ICBRH中指定的高电平周期的值进行计数，并在完成计数时将SCLn线驱动为低电平。当IIC检测到SCLn线的下降沿时，它开始对ICBRL中指定的低电平周期的值进行计数，然后在完成计数时停止驱动SCLn线（释放线）。IIC重复此过程以生成SCL时钟。

如果多个主设备连接到I2C总线，由于与另一个主设备争用，可能会出现SCL信号冲突。在这种情况下，主设备必须同步它们的SCL信号。因为SCL信号的这种同步必须是逐位的，所以IIC包括一个SCL同步电路，通过在主机模式下监视SCLn线来获得SCL时钟信号的逐位同步。

当IIC检测到SCLn线上的上升沿并开始计算ICBRH中指定的高电平周期，并且由于另一个主设备正在生成SCL信号而导致SCLn线上的电平下降时，IIC执行以下操作：

1. 检测到下降沿时停止计数。
2. 将SCLn线上的电平驱动为低电平。
3. 开始计算ICBRL中指定的低电平周期。

当IIC完成对低电平周期的计数时，它停止将SCLn线驱动为低电平。如果来自其他主设备的SCL时钟信号的低电平周期长于IIC中设置的低电平周期，则延长SCL信号的低电平周期。如果其他主设备的低电平周期结束，则SCL信号上升，因为SCLn线被释放。

当IIC输出完SCL时钟的低电平周期后，SCLn线被释放，SCL时钟上升。即当来自多个主控的SCL信号竞争时，SCL信号的高电平周期与周期较窄的时钟同步，SCL信号的低电平周期与主控的低电平周期同步。具有更广泛周期的时钟。但是，只有当ICFER中的SCLE位设置为1时，才会启用SCL信号的这种同步。

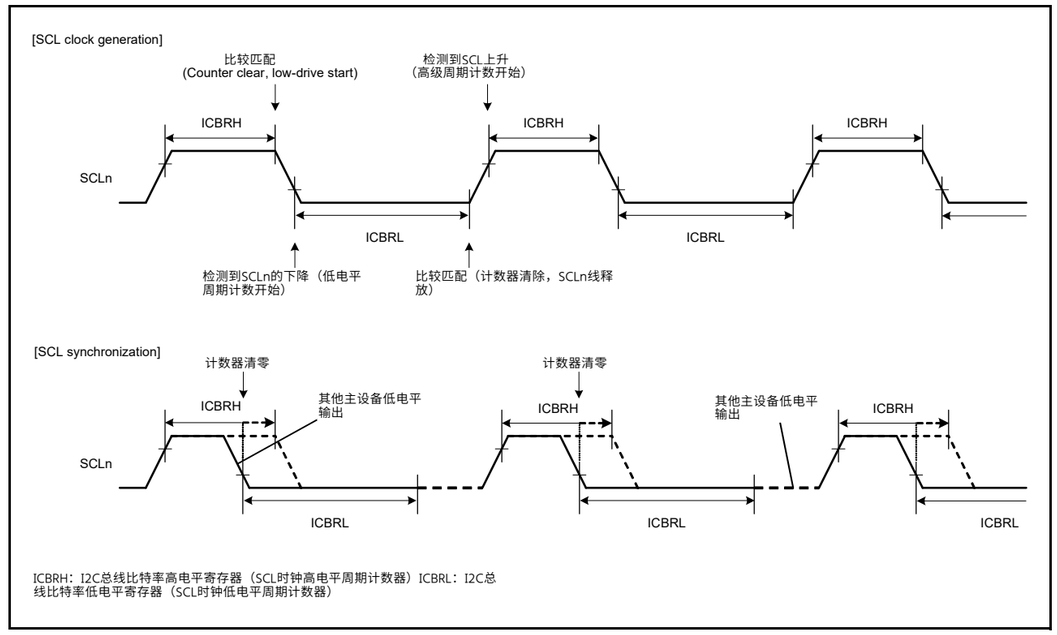


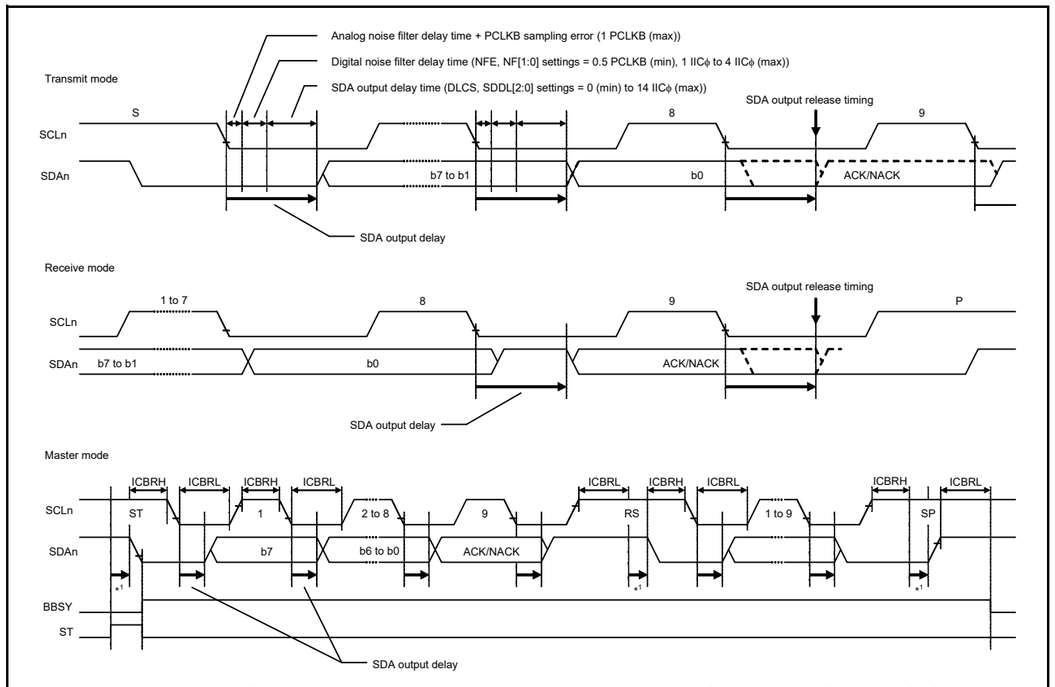
Figure 30.21 从IIC生成和同步SCL信号

30.5 SDA Output Delay Function

The IIC module provides a function for delaying output on the SDA line. The delay can be applied to all output on the SDA line, including issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals.

With this function, SDA output is delayed from the detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval during which the SCL clock is low. This approach helps to prevent erroneous operation of communication devices, with the aim of satisfying the 300-ns minimum data-hold time requirement of the SMBus specification. The output delay function is enabled by setting the SDDL[2:0] bits in ICMR2 to any value other than 000b, and disabled by setting the same bits to 000b.

When the SDA output delay function is enabled, for example, the DLCS bit in ICMR2 selects the clock source for the SDA output delay counter, either as the internal base clock (IICϕ) for the IIC module or as the internal base clock divided by two (IICϕ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. When the delay count is reached, the IIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.



Note 1. The output delay function is set by the DLCS and SDDL[2:0] bits when a start (ST), restart (RS), or stop (SP) condition is issued.

Figure 30.22 SDA output delay function

30.6 Digital Noise Filter Circuits

The internal circuitry sees the states of the SCLn and SDAn pins through analog and digital noise-filter circuits. Figure 30.23 shows a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the IIC consists of four flip-flop circuit stages connected in series, and a match-detection circuit.

The number of valid stages in the digital noise filter is selected in the NF[1:0] bits in ICMR3. The selected number of valid stages determines the noise-filtering capability as a period from 1 to 4 IICϕ cycles.

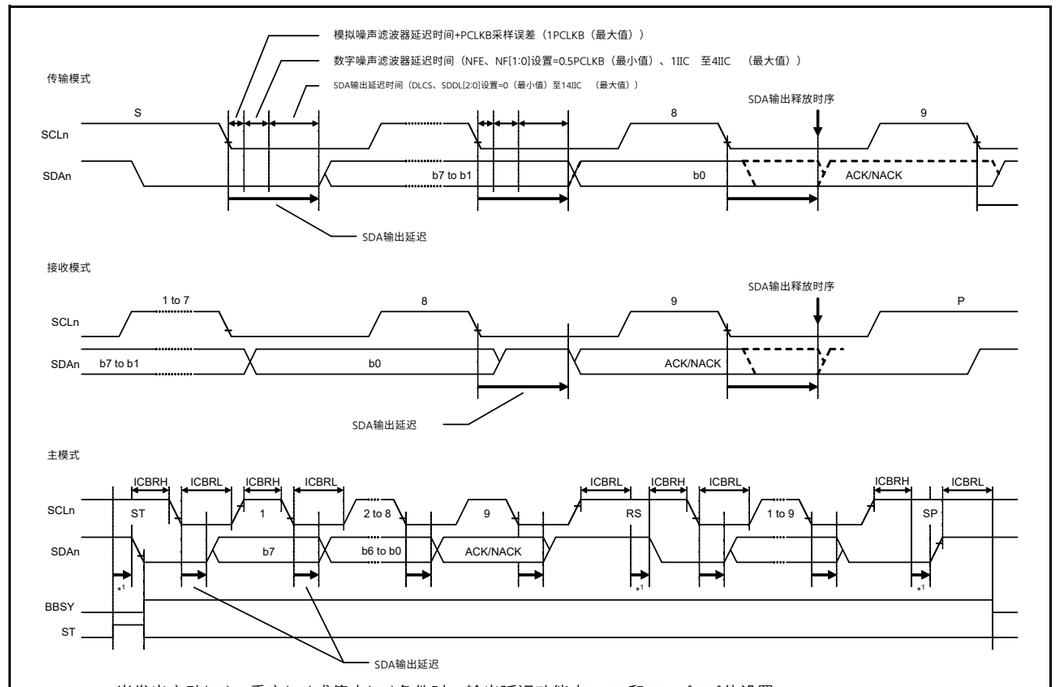
The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICϕ signal. When the input signal

30.5 SDA输出延迟功能

IIC模块提供了延迟SDA线上输出的功能。延迟可以应用于所有输出
SDA线，包括发出启动、重新启动和停止条件、数据以及ACK和NACK信号。

使用此功能，SDA输出从检测到SCL信号的下降沿开始延迟，以确保在SCL时钟为低电平的时间间隔内输出SDA信号。这种方法有助于防止通信设备的错误操作，旨在满足SMBus规范的300ns最小数据保持时间要求。通过将ICMR2中的SDDL[2:0]位设置为000b以外的任何值来启用输出延迟功能，并通过将相同位设置为000b来禁用输出延迟功能。

当SDA输出延迟功能使能时，例如ICMR2中的DLCS位选择时钟源
SDA输出延迟计数器，可以作为IIC模块的内部基本时钟(IIC)或作为内部基本时钟除以2(IIC 2)。计数器计算ICMR2中SDDL[2:0]位中设置的周期数。当达到延迟计数时，IIC模块将所需的输出（启动、重启或停止条件、数据或ACK或NACK信号）放在SDA线上。



Note 1. 当发出启动(ST)、重启(RS)或停止(SP)条件时，输出延迟功能由DLCS和SDDL[2:0]位设置。

Figure 30.22 SDA输出延迟功能

30.6 数字噪声滤波器电路

内部电路通过模拟和数字噪声滤波器电路查看SCLn和SDAn引脚的状态。图30.23显示了数字噪声滤波器电路的框图。

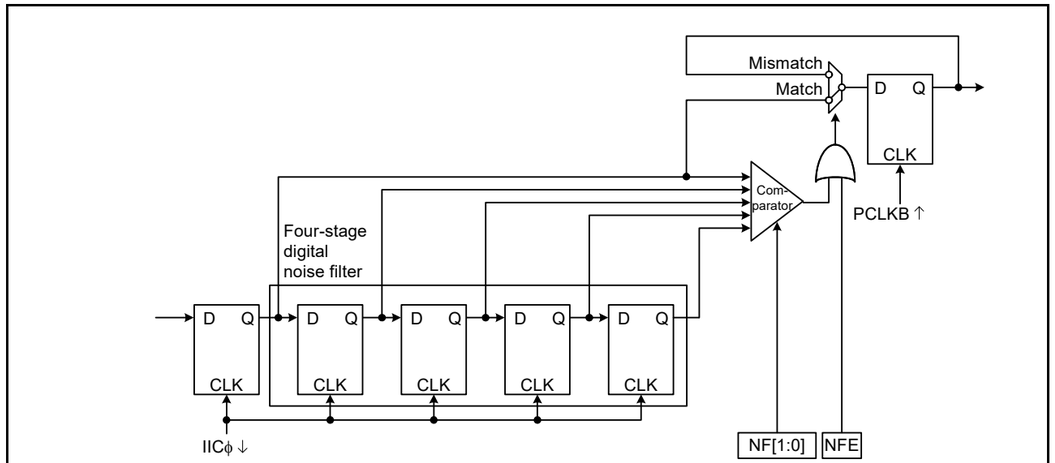
IIC的片上数字噪声滤波器电路由四个串联的触发器电路级和一个匹配检测电路组成。

数字噪声滤波器的有效级数在ICMR3的NF[1:0]位中选择。选定的有效级数决定了噪声过滤能力，周期为1到4个IIC 周期。

SCLn引脚（或SDAn引脚）的输入信号在IIC 信号的下降沿采样。当输入信号

level matches the output level of the number of effective flip-flop circuit stages as selected in the NF[1:0] bits in ICMR3, the signal level is seen in the subsequent stage. If the signal levels do not match, the previous value is saved.

If the ratio between the frequency of the internal operating clock (PCLKB) and the transfer rate is small, for example, for data transfer at 400 kbps with PCLKB at 4 MHz, the digital noise filter might lead to the elimination of the required signals as noise. In such cases, it is possible to disable the digital noise-filter circuit by setting the ICFER.NFE bit to 0, and use only the analog noise filter circuit.



NFE: Digital noise filter circuit enable bit
NF[1:0]: Noise filter stage select bits

Figure 30.23 Digital noise filter circuit block diagram

30.7 Address Match Detection

The IIC can set three unique slave addresses in addition to the general call address and host address. The slave addresses can be 7-bit or 10-bit slave addresses.

30.7.1 Slave-Address Match Detection

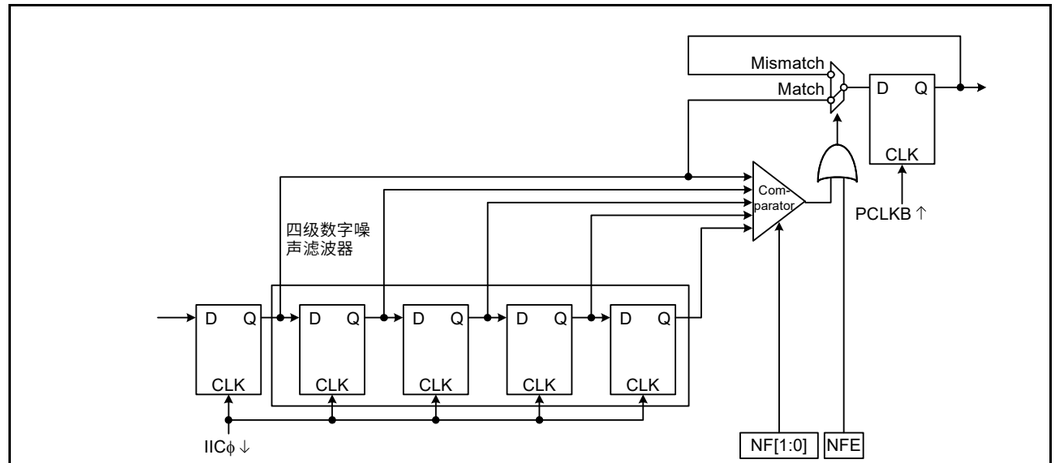
The IIC can set three unique slave addresses and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the IIC detects a match of the set slave address, the associated AASy flag (y = 0 to 2) in ICSR1 is set to 1 on the rising edge of the 9th SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the subsequent R/W# bit. This causes a receive data full interrupt (IICn_RXI) or transmit data empty interrupt (IICn_TXI) to be generated. The AASy flag identifies which slave address is specified.

Figure 30.24 to Figure 30.26 show the AASy flag set timing in three cases.

电平与在ICMR3的NF[1:0]位中选择的有效触发器电路级数的输出电平相匹配，信号电平在后续级中可见。如果信号电平不匹配，则保存先前的值。

如果内部工作时钟(PCLKB)的频率与传输速率之间的比率很小，例如，对于400kbps的数据传输，PCLKB为4MHz，则数字噪声滤波器可能会导致所需信号的消除，因为噪音。在这种情况下，可以通过将ICFER.NFE位设置为0来禁用数字噪声滤波器电路，并仅使用模拟噪声滤波器电路。



NFE：数字噪声滤波器电路使能位
NF[1:0]: 噪声滤波器级选择位

Figure 30.23 数字噪声滤波器电路框图

30.7 地址匹配检测

IIC除了广播地址和主机地址外，还可以设置三个唯一的从机地址。从地址可以是7位或10位从地址。

30.7.1 从地址匹配检测

IIC可以设置三个唯一的从机地址，并对每个唯一的从机地址具有从机地址检测功能。
当ICSER中的SARyE位（y=0到2）设置为1时，可以检测到设置在SARUy和SARLy（y=0到2）中的从机地址。

当IIC检测到设置的从地址匹配时，ICSR1中相关的AASy标志（y=0到2）在第9个SCL时钟周期的上升沿设置为1，并且ICSR2或TDRE中的RDRF标志ICSR2中的标志由随后的RW#位设置为1。这会导致产生接收数据满中断（IICn_RXI）或发送数据空中断（IICn_TXI）。AASy标志标识指定了哪个从地址。

图30.24至图30.26显示了三种情况下的AASy标志设置时序。

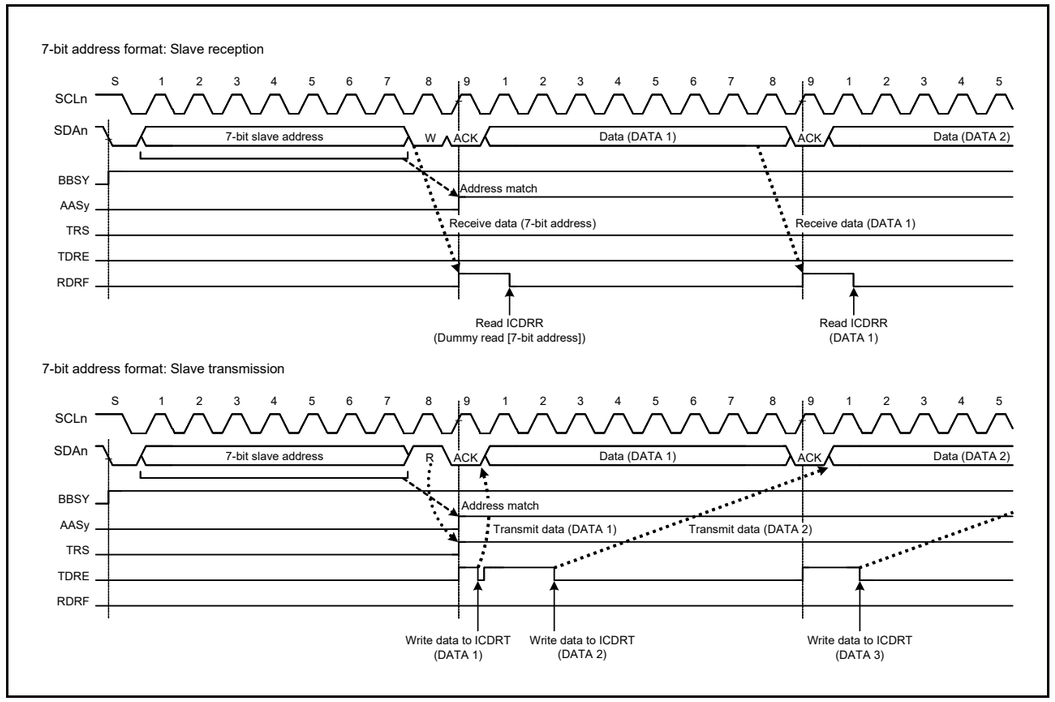


Figure 30.24 AASy flag set timing with 7-bit address format selected

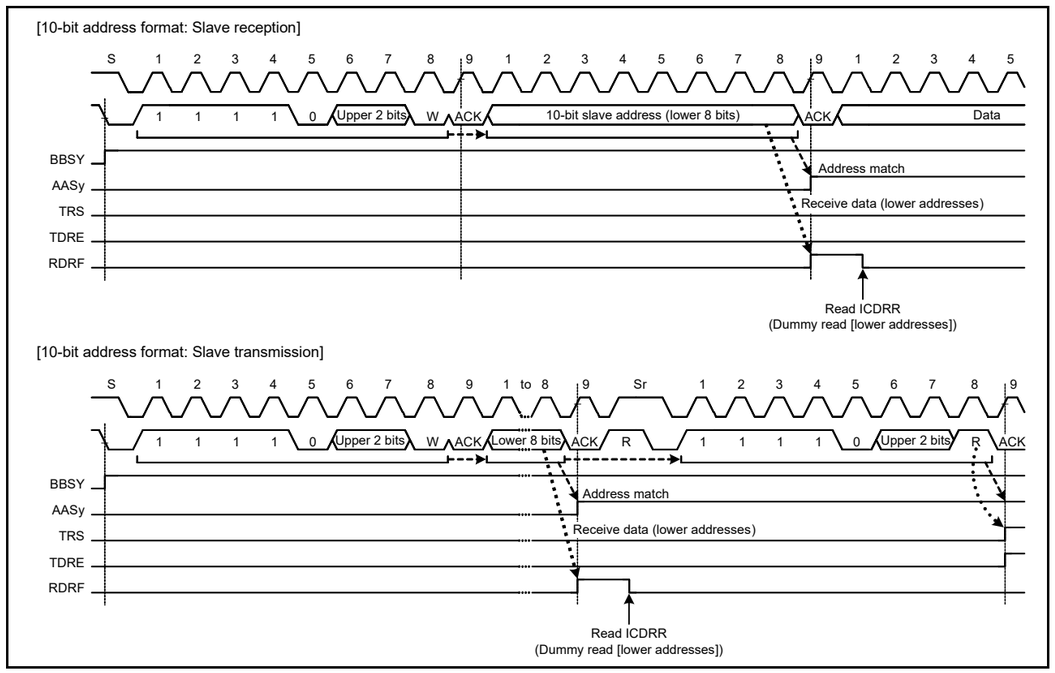


Figure 30.25 AASy flag set timing with 10-bit address format selected

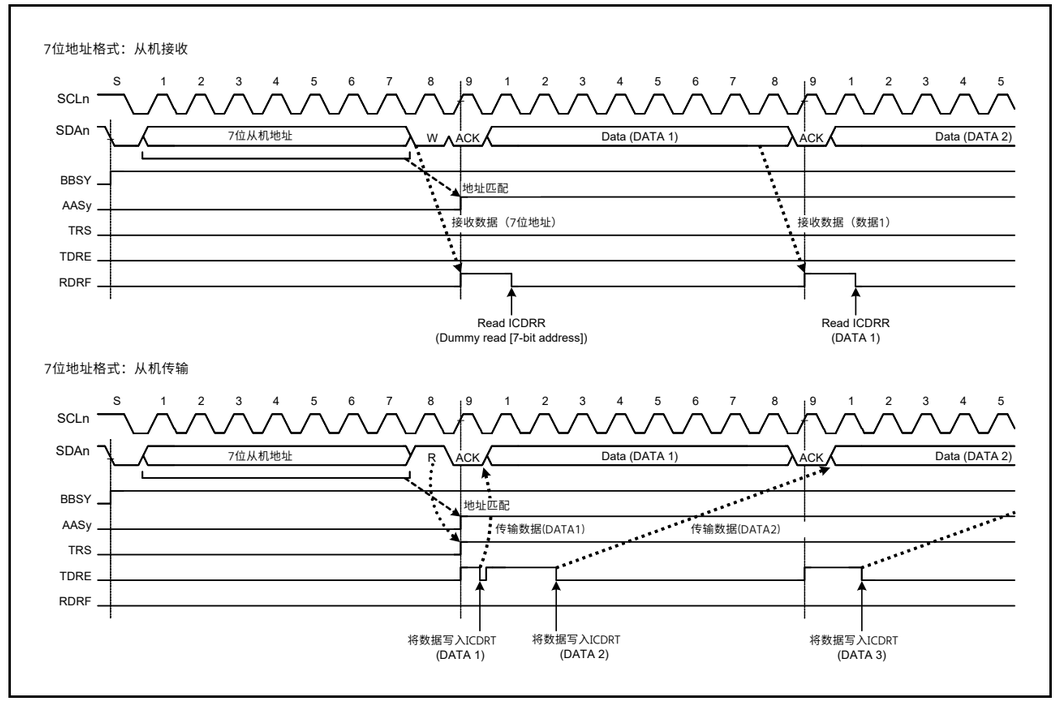


Figure 30.24 选择7位地址格式的AASy标志设置时序

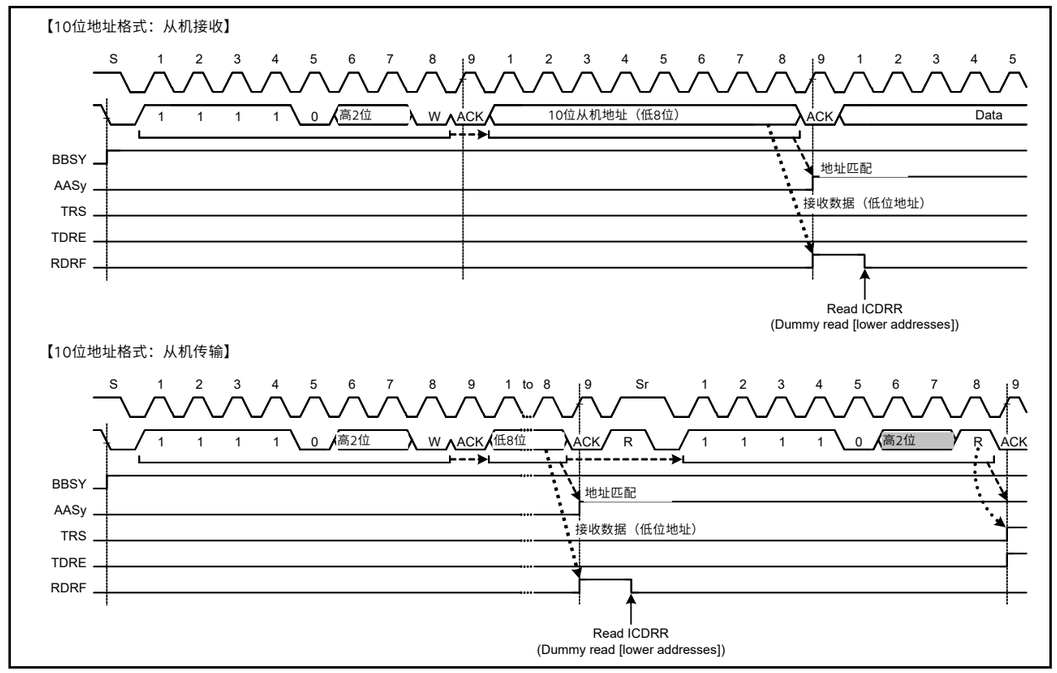


Figure 30.25 选择10位地址格式的AASy标志设置时序

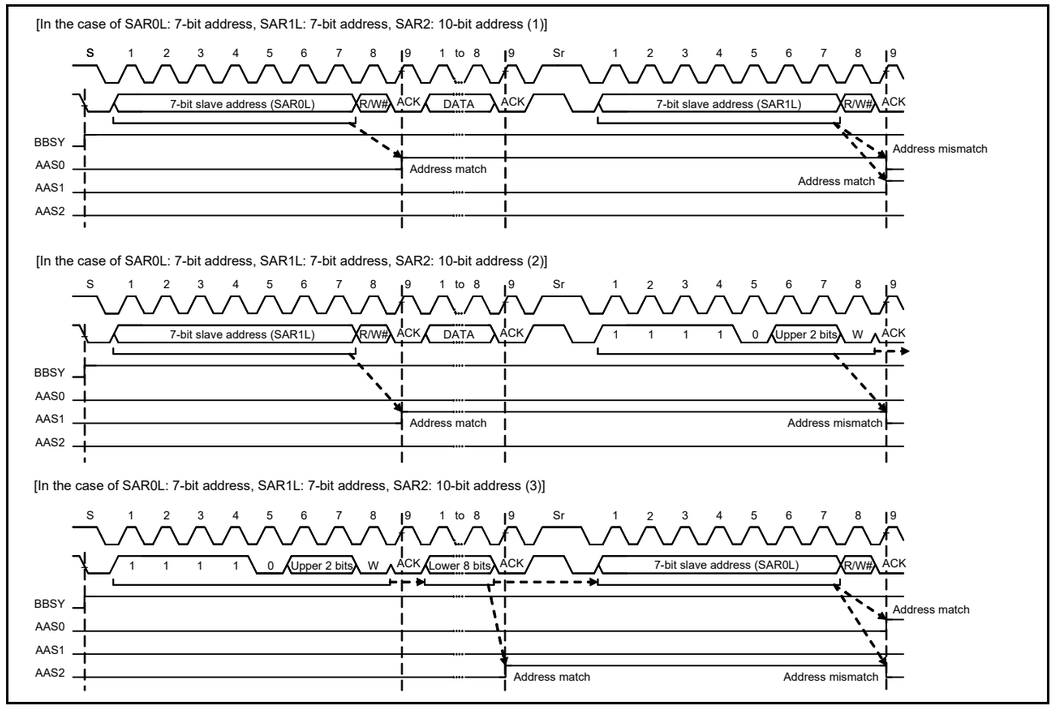


Figure 30.26 AASy flag set and clear timing with 7-bit and 10-bit address formats mixed

30.7.2 Detection of General Call Address

The IIC provides detection of the general call address (0000 000b + 0 [W]). General call address detection is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the IIC recognizes this as the address of a slave device with an all-zero address, but not as the general call address.

When the IIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 are set to 1 on the rising edge of the 9th cycle of SCL clock. This leads to the generation of a receive data full interrupt (IICn_RXI). The value of the GCA flag can be checked to confirm whether the general call address is transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

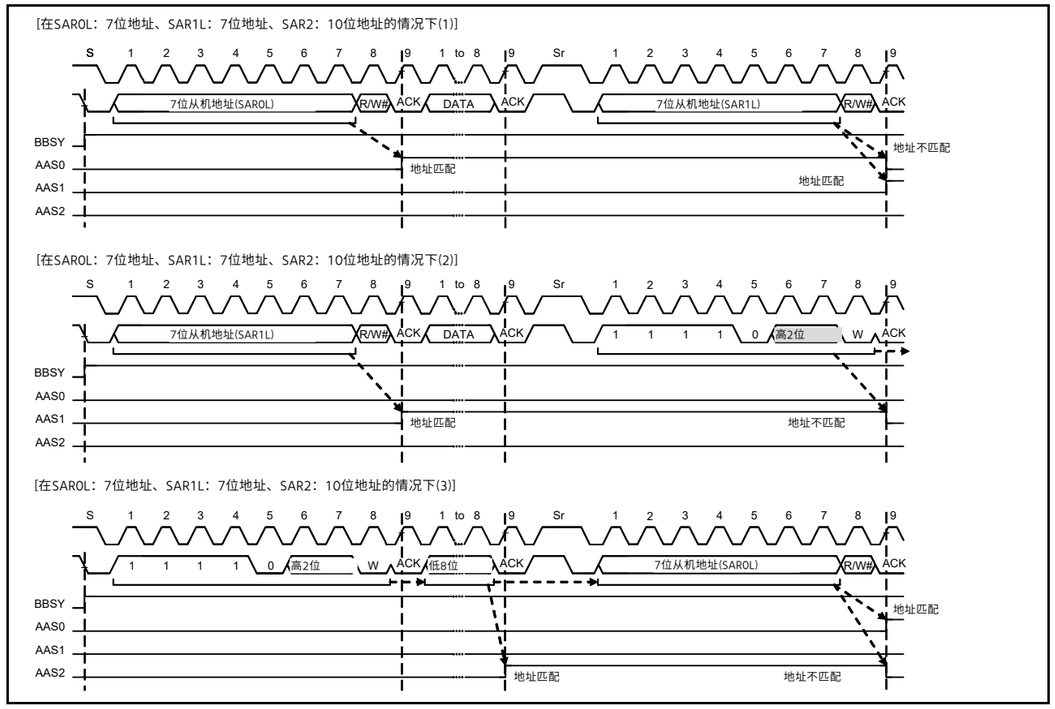


Figure 30.26 混合7位和10位地址格式的AASy标志设置和清除时序

30.7.2 广播呼叫地址检测

IIC提供对广播呼叫地址(0000000b+0[W])的检测。通过将ICSER中的GCAE位设置为1来启用广播呼叫地址检测。

如果在发出启动或重新启动条件后接收到的地址是0000000b+1[R]（起始字节），则IIC将其识别为具有全零地址的从设备的地址，但不是广播地址.

当IIC检测到广播呼叫地址时，ICSR1中的GCA标志和ICSR2中的RDRF标志都在SCL时钟的第9个周期的上升沿设置为1。这会导致接收数据完全中断(IICn_RXI)的产生。可以通过检查GCA标志的值来确认是否发送了广播呼叫地址。

检测到广播呼叫地址后的操作与正常的从机接收操作相同。

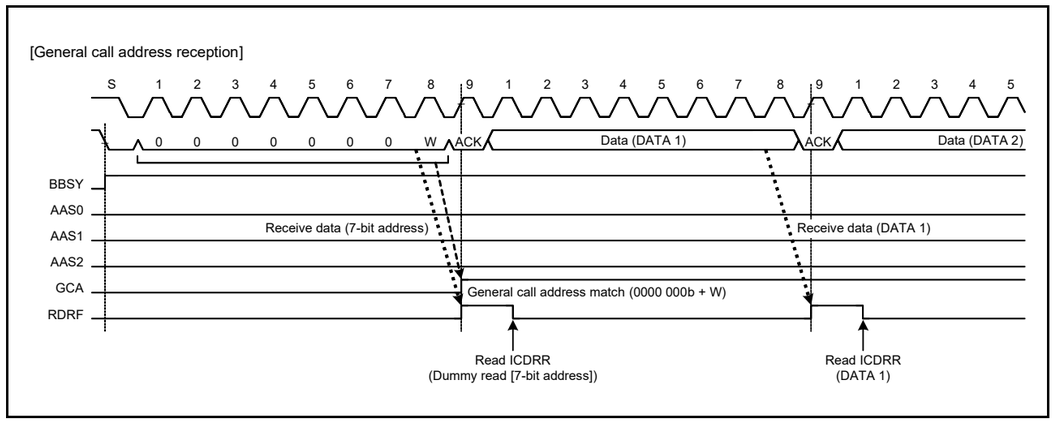


Figure 30.27 Timing of GCA flag setting during reception of general call address

30.7.3 Device ID Address Detection

The IIC module provides detection of device ID address in compliance with the I2C bus specification (Rev. 03). When the IIC receives 1111 100b as the first byte after a start condition or restart condition is issued with the DIDE bit in ICSER set to 1, the IIC recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the 8th SCL clock cycle when the subsequent R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the IIC sets the associated AASy flag (y = 0 to 2) in ICSR1 to 1.

When the first byte received after the issue of a start or restart condition matches the device ID address (1111 100b) again and the subsequent R/W# bit is 1, the IIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device ID address detection function, the IIC sets the DID flag to 0 if a match with the IIC slave address is not obtained or a match with the device ID address is not obtained after a match with the IIC slave address, and the detection of a restart condition. If the first byte after detection of a start or restart condition matches the device ID address (1111 100b) and the R/W# bit is 0, the IIC sets the DID flag to 1 and compares the second and subsequent bytes with the slave address of the IIC. If the R/W# bit is 1, the DID flag holds the previous value and the IIC does not compare the second and subsequent bytes. Therefore, the reception of a device ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Additionally, prepare the device ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device ID field as normal transmit data. For details of the information that must be included in device ID fields, contact NXP Semiconductors.

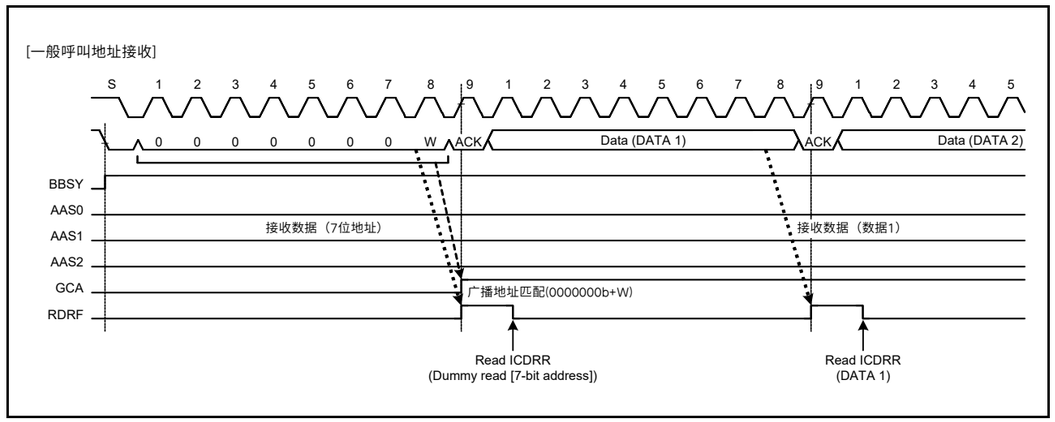


Figure 30.27 在接收广播呼叫地址期间设置GCA标志的时机

30.7.3 设备ID地址检测

IIC模块提供符合I2C总线规范(Rev.03)的设备ID地址检测。当IIC在ICSER中的DIDE位设置为1的情况下在发出启动条件或重启条件后接收到1111100b作为第一个字节时，IIC将地址识别为设备ID，在上升时将ICSR1中的DID标志设置为1当后续的RW#位为0时，第8个SCL时钟周期的边沿，然后将第二个和后续字节与自己的从地址进行比较。如果地址与从地址寄存器中的值匹配，则IIC将ICSR1中相关的AASy标志（y=0到2）设置为1。

当发出启动或重启条件后接收到的第一个字节再次与设备ID地址(1111100b)匹配且后续RW#位为1时，IIC不比较第二个和后续字节并设置ICSR2.TDRE标志为1。

在设备ID地址检测功能中，如果没有匹配到IIC从机地址或者匹配到IIC从机地址后没有匹配到设备ID地址，则IIC设置DID标志为0，检测的重新启动条件。如果检测到启动或重启条件后的第一个字节与设备ID地址(1111100b)匹配且RW#位为0，则IIC将DID标志设置为1，并将第二个和后续字节与从机地址进行比较国际集成电路。如果RW#位为1，则DID标志保持前一个值，并且IIC不比较第二个和后续字节。因此，在确认TDRE=1后，可以通过读取DID标志来检查设备ID地址的接收。

此外，准备设备ID字段（3个字节：12位表示制造商+9位表示部件+3位表示版本），在接收到连续的设备ID字段作为正常发送数据后必须发送到主机。有关必须包含在设备ID字段中的信息的详细信息，请联系NXPSemiconductors。

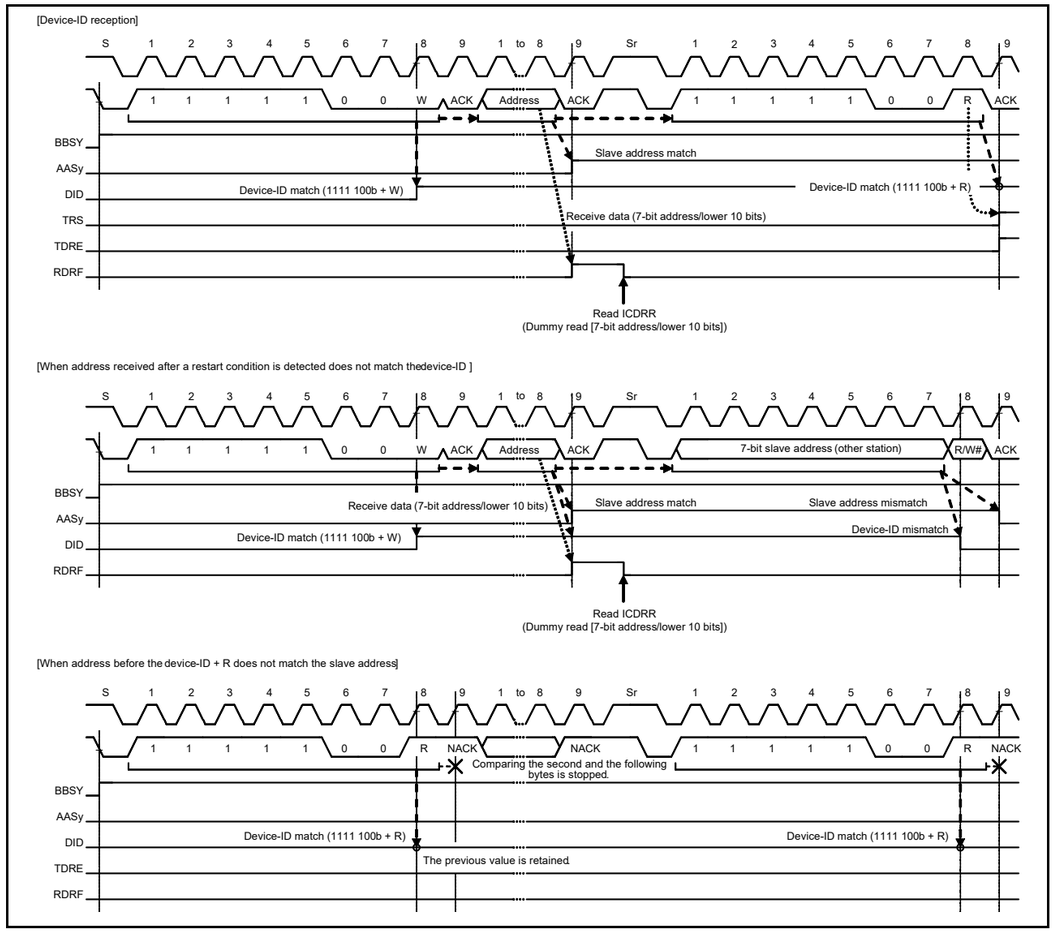


Figure 30.28 AASy/DID flag set/clear timing during reception of device ID

30.7.4 Host Address Detection

The IIC provides host address detection when operating in SMBus mode. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the IIC can detect the host address (0001 000b) in slave receive mode (ICCR2.MST and ICCR2.TRS bits = 00b).

When the IIC detects the host address, the HOA flag in the ICSR1 register is set to 1 on the rising edge of the 9th SCL clock cycle. At the same time, the RDRF flag in the ICSR2 register is set to 1 if the R/W# bit is 0. This causes a receive data full interrupt (IICn_RXI) to be generated. The HOA flag indicates that the host address was detected.

If the bit following the host address (0001 000b) is a read bit (R/W# bit = 1), the IIC can also detect the host address. After the host address is detected, the IIC operates in the same manner as in normal slave operation.

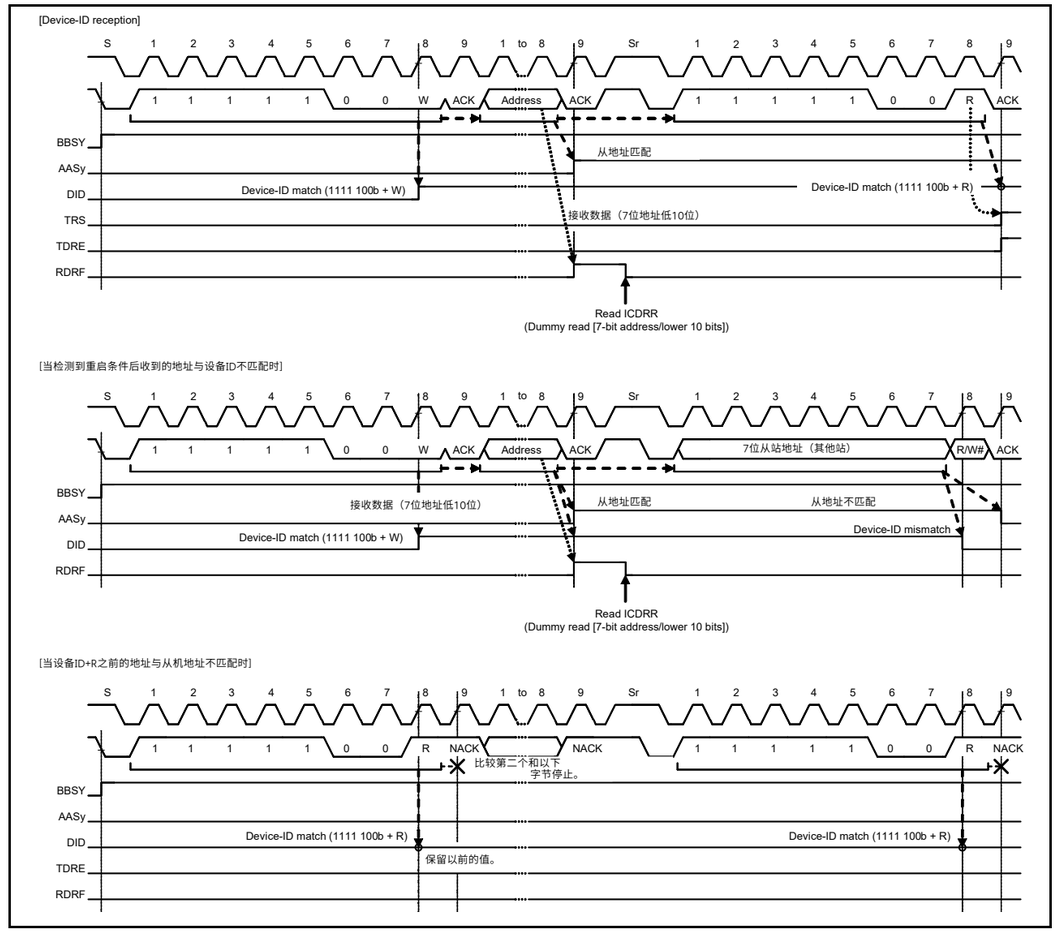


Figure 30.28 AASyDID标志在接收设备ID期间设置清除时序

30.7.4 主机地址检测

IIC在SMBus模式下工作时提供主机地址检测。当ICSER中的HOAE位设置为1而ICMR3中的SMBS位为1时，IIC可以在从机接收模式下检测主机地址（0001000b）（ICCR2.MST和ICCR2.TRS位=00b）。

当IIC检测到主机地址时，ICSR1寄存器中的HOA标志在第9个SCL时钟周期的上升沿被设置为1。同时，如果RW#位为0，则ICSR2寄存器中的RDRF标志设置为1。这会导致产生接收数据满中断（IICn_RXI）。HOA标志表示检测到主机地址。

如果主机地址（0001000b）后面的位是读取位（RW#位=1），则IIC也可以检测主机地址。
检测到主机地址后，IIC以与正常从机操作相同的方式运行。

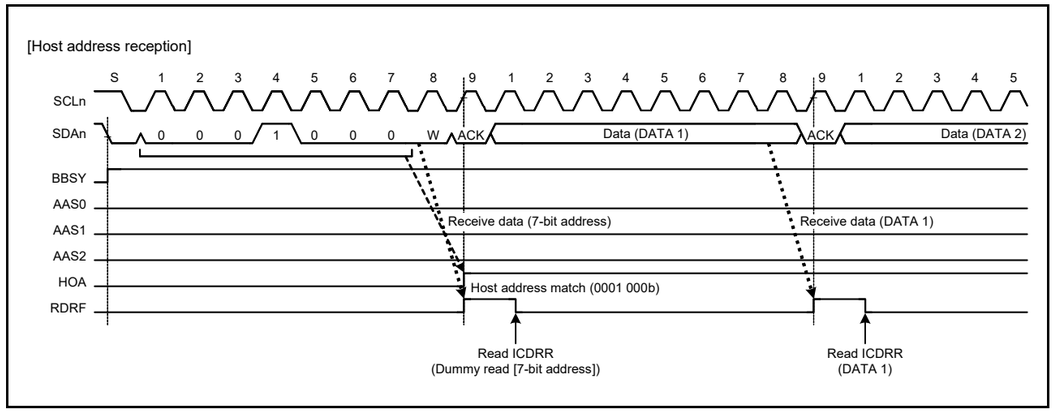


Figure 30.29 HOA flag set timing during reception of host address

30.8 Wakeup Function

The IIC provides a wakeup function that causes the MCU to transition from Software Standby mode to normal operation. The wakeup function enables the reception of data when the system clock is stopped, and it generates a wakeup interrupt signal on the match of the slave address of the received data. This wakeup interrupt signal triggers the return to normal operation.

The wakeup function has four operation modes:

- Normal wakeup mode 1
- Normal wakeup mode 2
- Command recovery mode
- EEP response mode.

Table 30.9 describes the behavior in these modes.

Table 30.9 Wakeup operation modes

Operation mode	ACK response timing	ACK response before wakeup	SCL state during wakeup
Normal wakeup mode 1	Before wakeup	ACK	Fixed low
Normal wakeup mode 2	After wakeup	Before wakeup: no response After wakeup: ACK response	Fixed low
Command recovery mode	Before wakeup	ACK	Open
EEP response mode	Before wakeup	NACK	Open

Precautions on the use of the wakeup function

- Disable the wakeup function (WUE = 0) after a wakeup interrupt triggers the transition from Software Standby mode to normal operation
- Do not change the content of the IIC registers while WUF = 0, even if the wakeup interrupt recovers the system clock. Specify the register settings after confirming that WUF = 1
- Set WUE = WUIE = 1 and MST = TRS = 0 (slave reception mode) before entering Software Standby mode
- Do not transition to Software Standby mode while BBSY = 1
- The wakeup function supports the 7-bit slave address of slave address register SARL0, the general call address, and the host address. 10-bit slave addresses, SARL1 and SARL2, are not supported
- When the wakeup function is enabled, disable the interrupts selectable in the TIE, TEIE, RIE, NAKIE, SPIE, STIE, ALIE, and TMOIE bits in the ICIER register

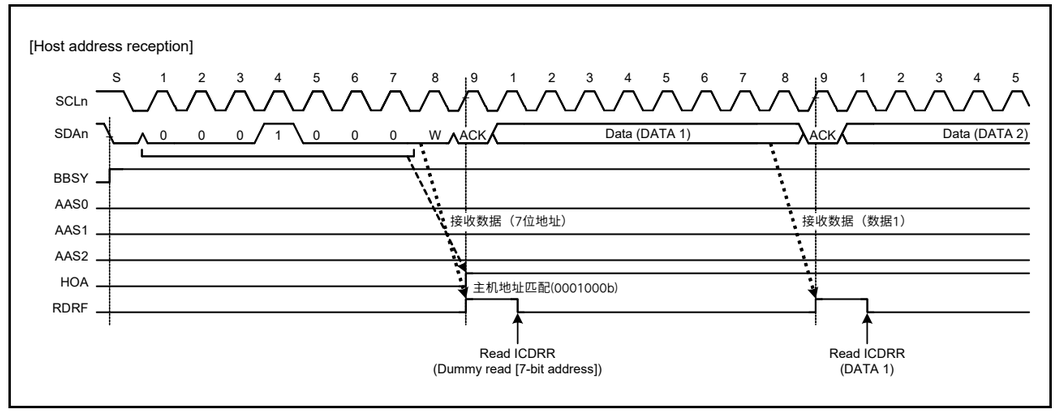


Figure 30.29 接收主机地址期间的HOA标志设置时序

30.8 唤醒功能

IIC提供唤醒功能，使MCU从软件待机模式转换到正常操作。唤醒功能在系统时钟停止时启用数据接收，并在接收到的数据的从地址匹配时产生唤醒中断信号。该唤醒中断信号触发恢复正常操作。

唤醒功能有四种操作模式：

- 正常唤醒模式1
- 正常唤醒模式2
- 命令恢复模式
- EEP响应模式。

表30.9描述了这些模式下的行为。

Table 30.9 唤醒操作模式

操作模式	ACK响应时间	唤醒前的ACK响应	唤醒期间的SCL状态
正常唤醒模式1	醒来前	ACK	固定低
正常唤醒模式2	醒来后	唤醒前：无响应唤醒后：ACK响应	固定低
命令恢复模式	醒来前	ACK	Open
EEP响应模式	醒来前	NACK	Open

唤醒功能使用注意事项

- 在唤醒中断触发从软件待机模式转换到正常操作后禁用唤醒功能(WUE=0)
- 当WUF=0时不要改变IIC寄存器的内容，即使唤醒中断恢复了系统时钟。确认WUF=1后指定寄存器设置
- 在进入软件待机模式之前设置WUE=WUIE=1和MST=TRS=0（从接收模式）
- BBSY=1时不要转换到软件待机模式
- 唤醒功能支持从地址寄存器SARL0的7位从地址、广播地址和主机地址。不支持10位从机地址SARL1和SARL2
- 启用唤醒功能时，禁用TIE、TEIE、RIE、NAKIE、SPIE、STIE、ICIER寄存器中的ALIE和TMOIE位

- When the wakeup function is enabled, do not use the timeout function
- If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, for example IRQn, the WUF flag is not set to 1.

30.8.1 Normal Wakeup Mode 1

This section describes the behavior, timing, and an example operation in normal wakeup mode 1.

In normal wakeup mode 1, a wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

Before wakeup: ACK is sent in response to the data received with its own slave address of the IIC.
During wakeup: ACK response is made on the 9th clock cycle of SCL, after which SCL is held low.*1
After wakeup: Normal operation continues.

If the slave address does not match, the SCL line is not held low after the 9th clock cycle of SCL, and the slave operation continues.

Figure 30.30 shows an operation example and Figure 30.32 shows the detailed timing.

Note 1. Between the 9th clock cycle and 1st clock cycle during wakeup, WAIT = 1 does not work.

If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, for example the IRQn, the WUF flag is not set to 1. Figure 30.31 shows an operation example.

- 开启唤醒功能时，不要使用超时功能
- 如果从软件待机模式的转换是由唤醒中断以外的中断触发的，例如IRQn，WUF标志未设置为1。

30.8.1 正常唤醒模式1

本节介绍正常唤醒模式1下的行为、时序和示例操作。

在正常唤醒模式1中，由匹配从机地址触发的唤醒中断启动到正常操作的转换，如下所示：

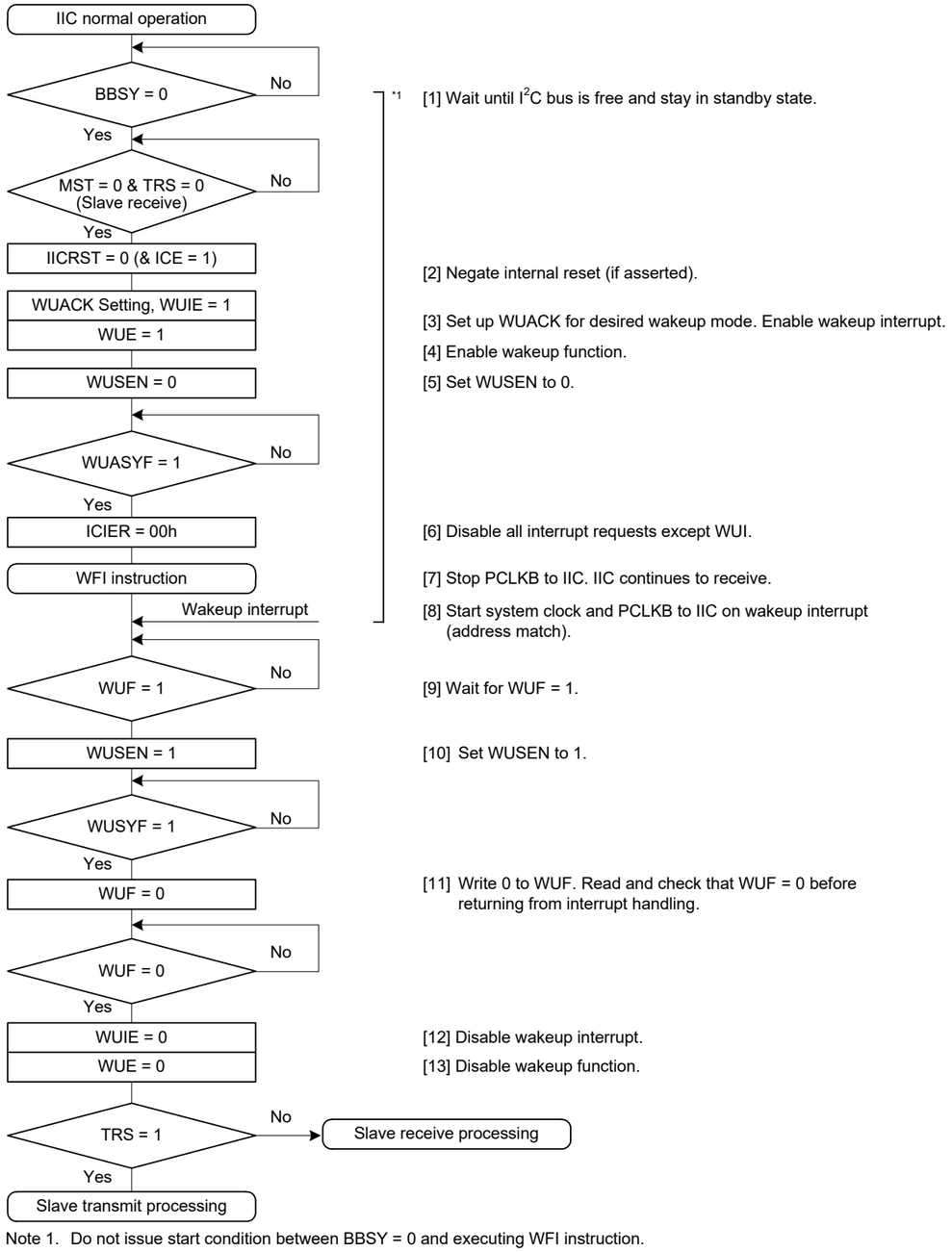
Before wakeup: ACK是响应接收到的带有IIC从机地址的数据而发送的。
During wakeup: 在SCL的第9个时钟周期做出ACK响应，之后SCL保持低电平。*1
After wakeup: 正常操作继续。

如果从机地址不匹配，则SCL线在SCL的第9个时钟周期后不保持低电平，从机操作继续。

图30.30显示了一个操作示例，图30.32显示了详细的时序。

注1.在唤醒期间的第9个时钟周期和第1个时钟周期之间，WAIT=1不起作用。

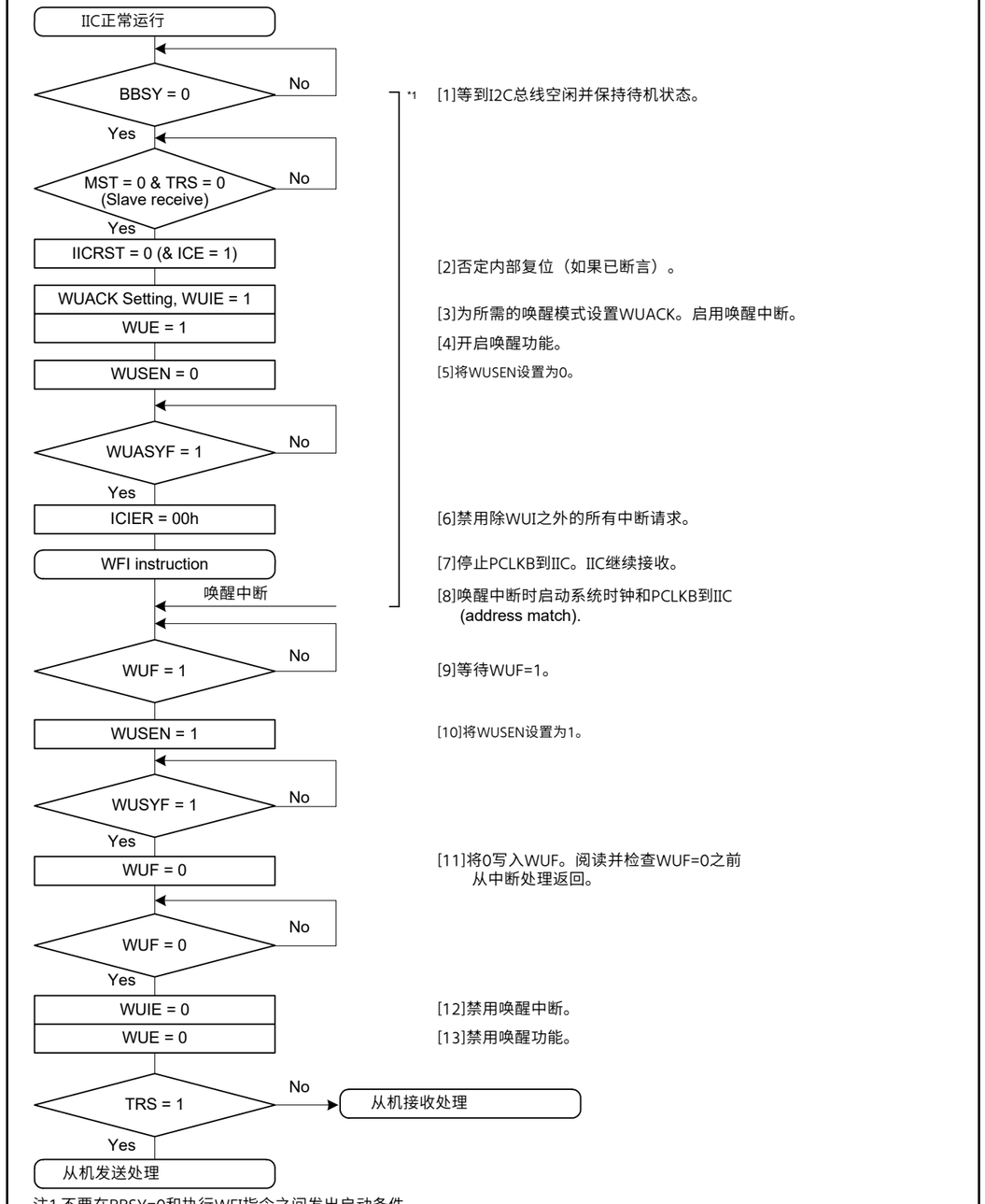
如果从软件待机模式的转换是由唤醒中断以外的中断触发的，例如IRQn，WUF标志未设置为1。图30.31显示了一个操作示例。



Note 1. Do not issue start condition between BBSY = 0 and executing WFI instruction.

Figure 30.30 Example operation of normal wakeup mode 1 when wakeup is triggered by a wakeup interrupt on match of the slave address

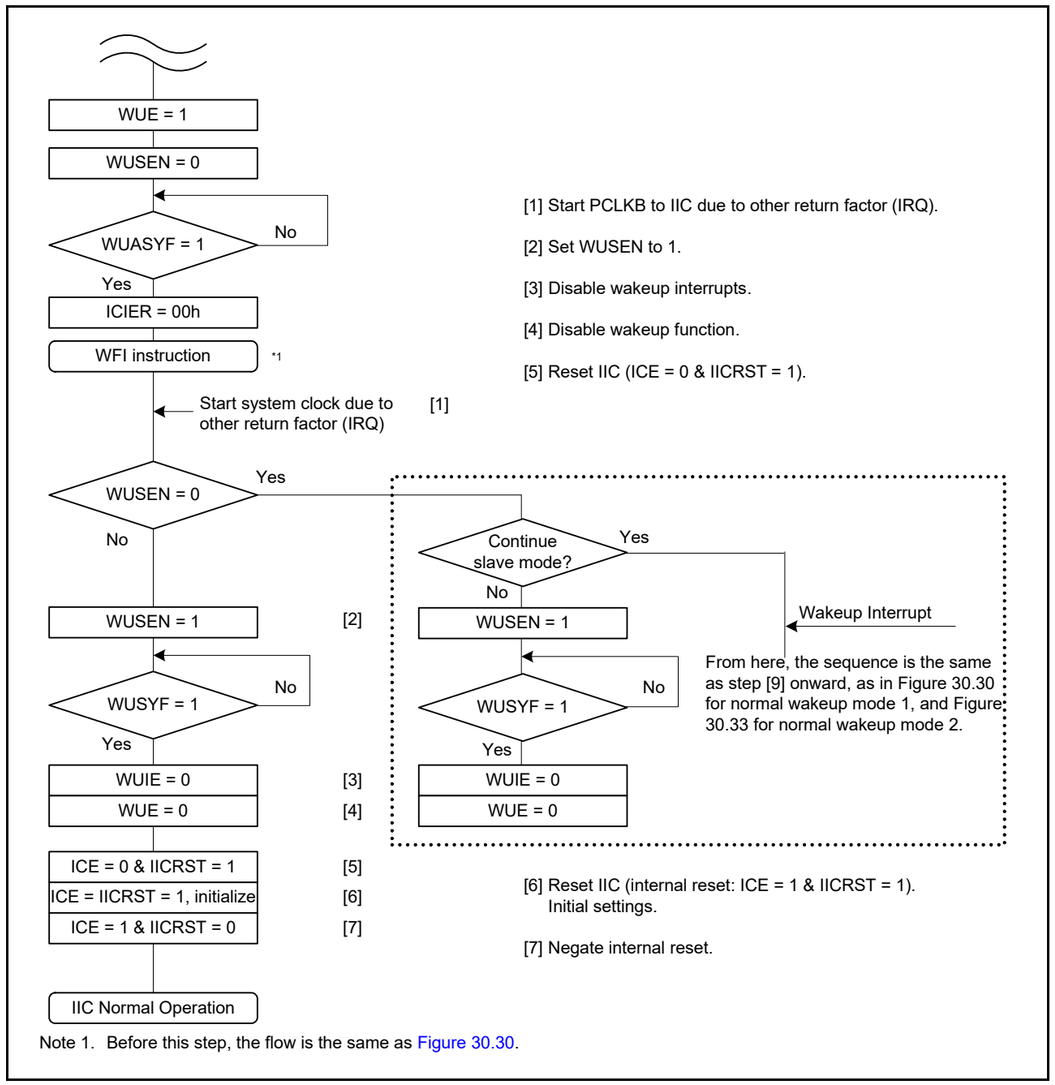
Note: See Precautions on the use of the wakeup function.



注1.不要在BBSY=0和执行WFI指令之间发出启动条件。

Figure 30.30 正常唤醒模式1的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

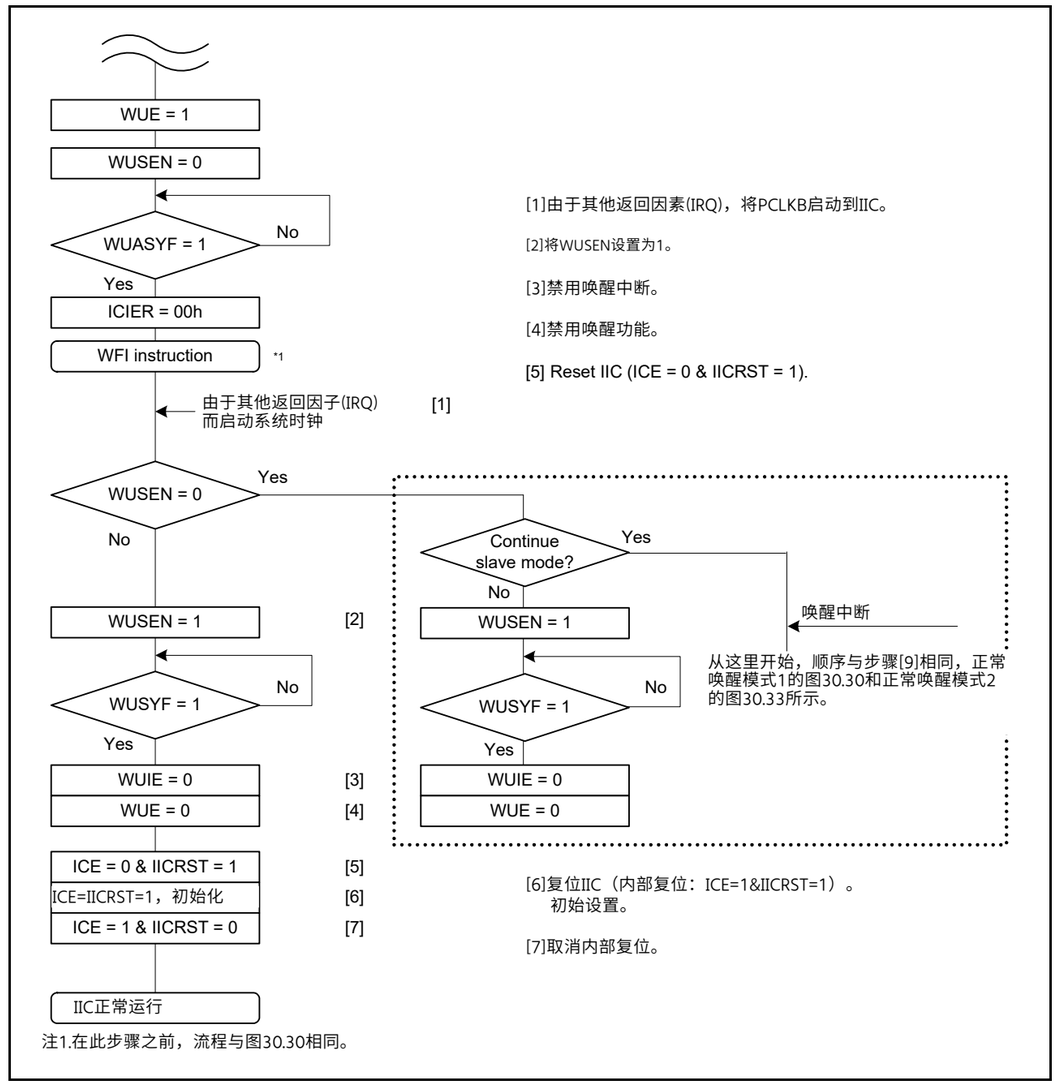
Note: 请参阅唤醒功能使用注意事项。



Note 1. Before this step, the flow is the same as Figure 30.30.

Figure 30.31 Example operation of normal wakeup modes 1 and 2 when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, IRQn

Note: For details of the IIC initial settings, see section 30.3.2, Initial Settings.



注1.在此步骤之前，流程与图30.30相同。

Figure 30.31 当唤醒由IIC唤醒中断以外的中断（例如IRQn）触发时，正常唤醒模式1和2的示例操作

Note: 有关IIC初始设置的详细信息，请参阅第30.3.2节，初始设置。

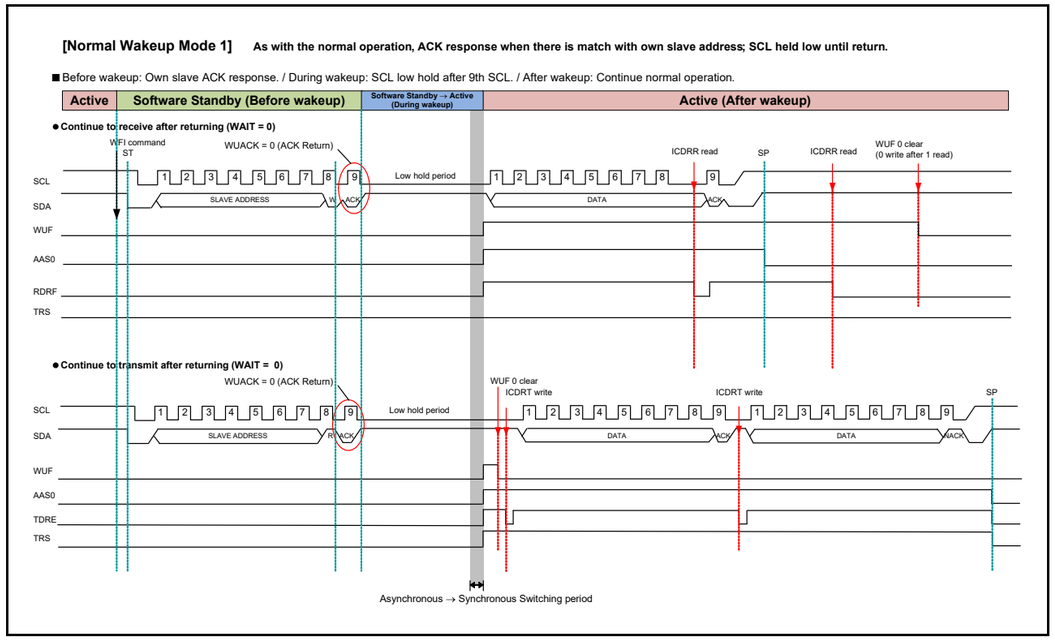


Figure 30.32 Timing of normal wakeup mode 1

30.8.2 Normal Wakeup Mode 2

This section describes the behavior, timing, and an example operation in normal wakeup mode 2.

In normal wakeup mode 2, a wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

Before wakeup: No response to the data received with its own slave address until the end of the 8th SCL cycle
During wakeup: SCL line held low during the 8th and 9th clock cycles.
After wakeup: ACK returns on the 9th clock cycle of SCL and normal operation continues.

If the slave address does not match, the SCL line is not held low after the 8th SCL clock cycle, and the slave operation continues.

For an example operation in normal wakeup mode 2, see Figure 30.33. Figure 30.34 shows the detailed timing.

If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, for example IRQ, the WUF flag is not set to 1. Figure 30.31shows an operation example.

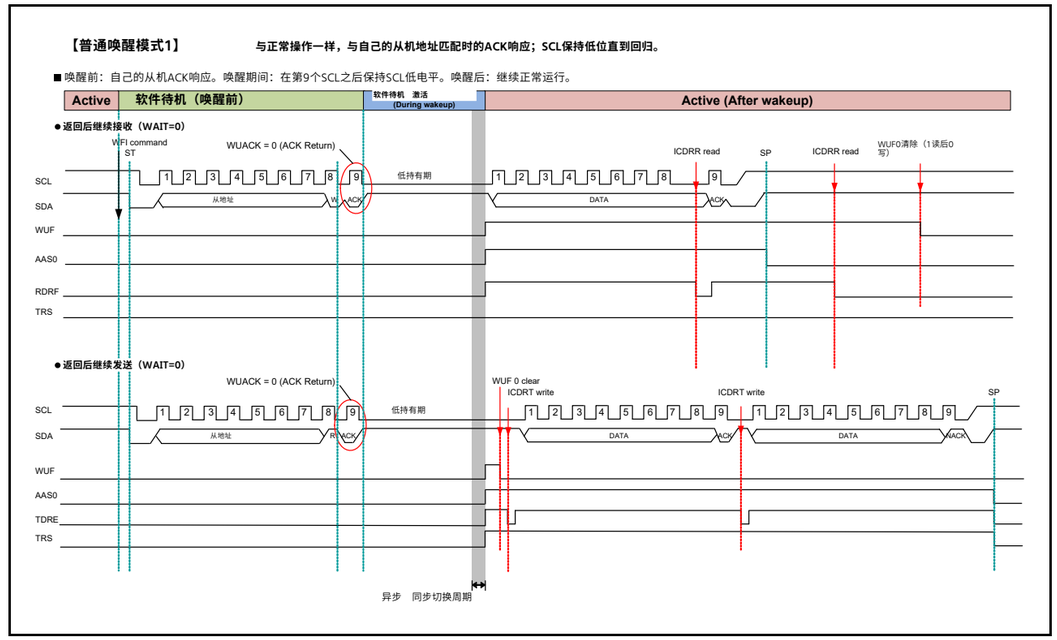


Figure 30.32 正常唤醒模式1的时序

30.8.2 正常唤醒模式2

本节介绍正常唤醒模式2中的行为、时序和示例操作。

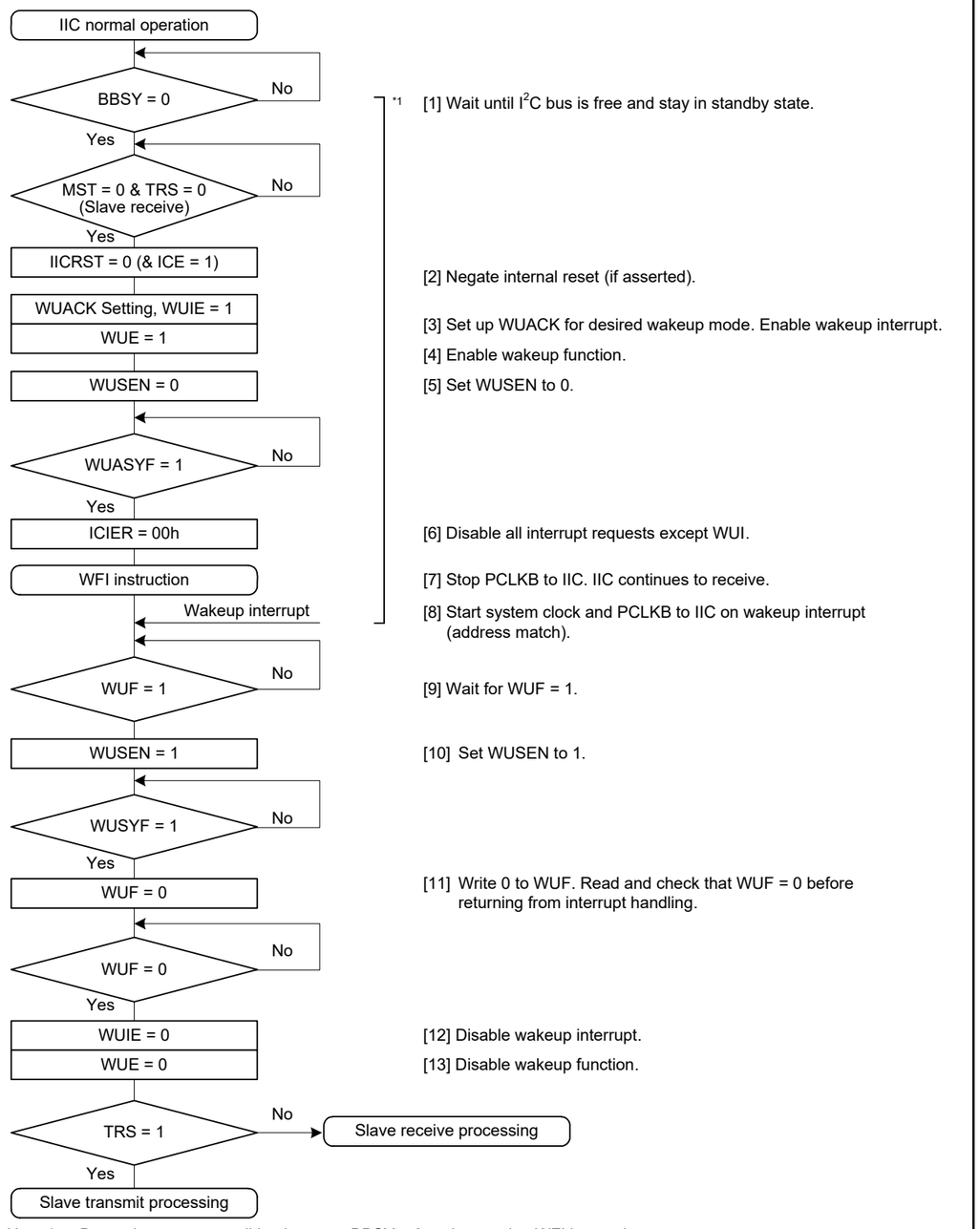
在正常唤醒模式2中，由匹配从机地址触发的唤醒中断启动到正常操作的转换，如下所示：

唤醒前：在第8个SCL周期结束之前，对接收到的带有自己从机地址的数据没有响应
During wakeup: SCL线在第8和第9个时钟周期内保持低电平。
After wakeup: ACK在SCL的第9个时钟周期返回并继续正常操作。

如果从机地址不匹配，则SCL线在第8个SCL时钟周期后不会保持低电平，从机操作继续。

有关正常唤醒模式2下的示例操作，请参见图30.33。图30.34显示了详细的时序。

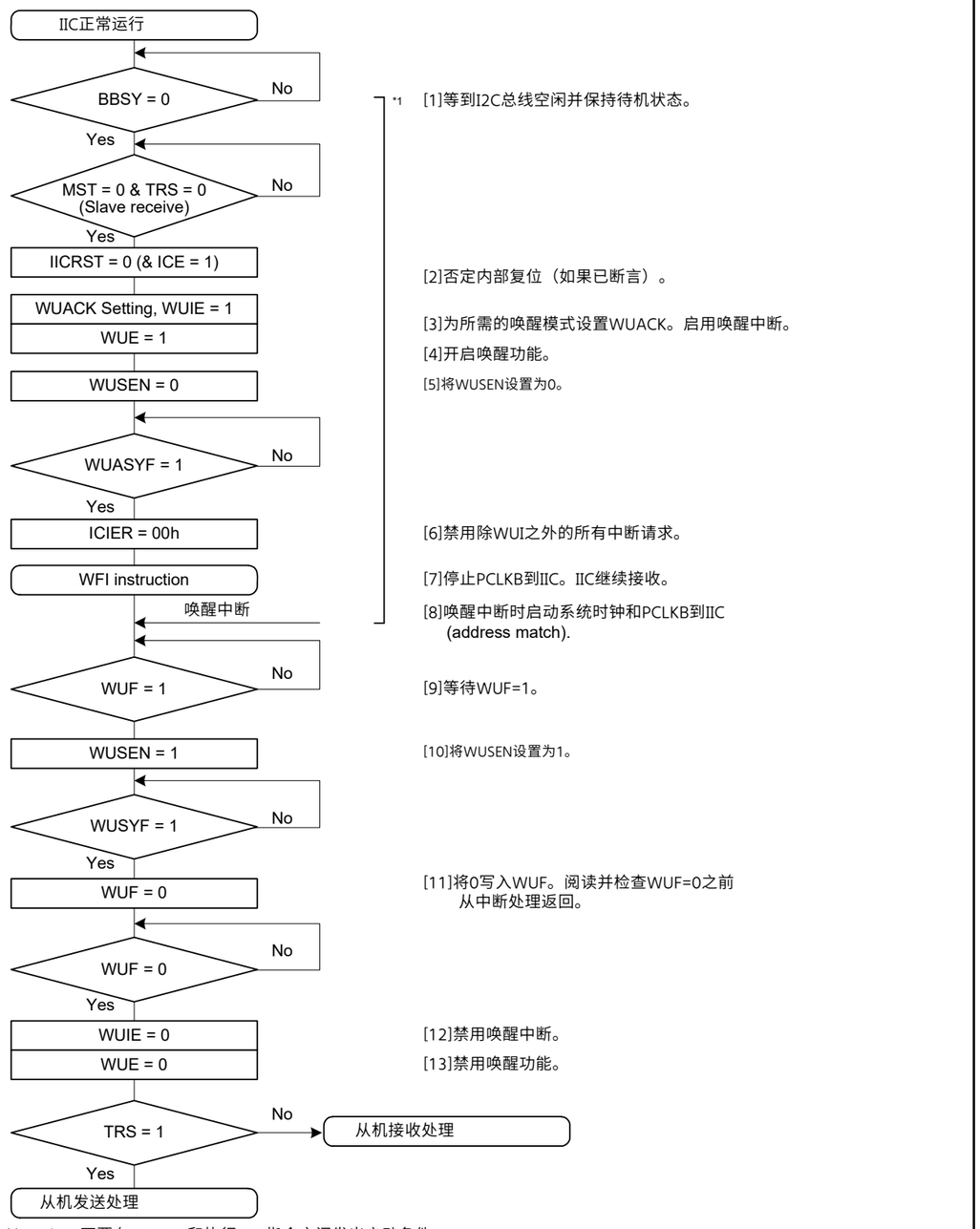
如果从软件待机模式的转换是由唤醒中断以外的中断触发的，例如IRQ，则WUF标志不设置为1。图30.31显示了一个操作示例。



Note 1. Do not issue start condition between BBSY = 0 and executing WFI instruction.

Figure 30.33 Example operation of normal wakeup mode 2 when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



Note 1. 不要在BBSY=0和执行WFI指令之间发出启动条件。

Figure 30.33 正常唤醒模式2的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

Note: 请参阅唤醒功能使用注意事项。

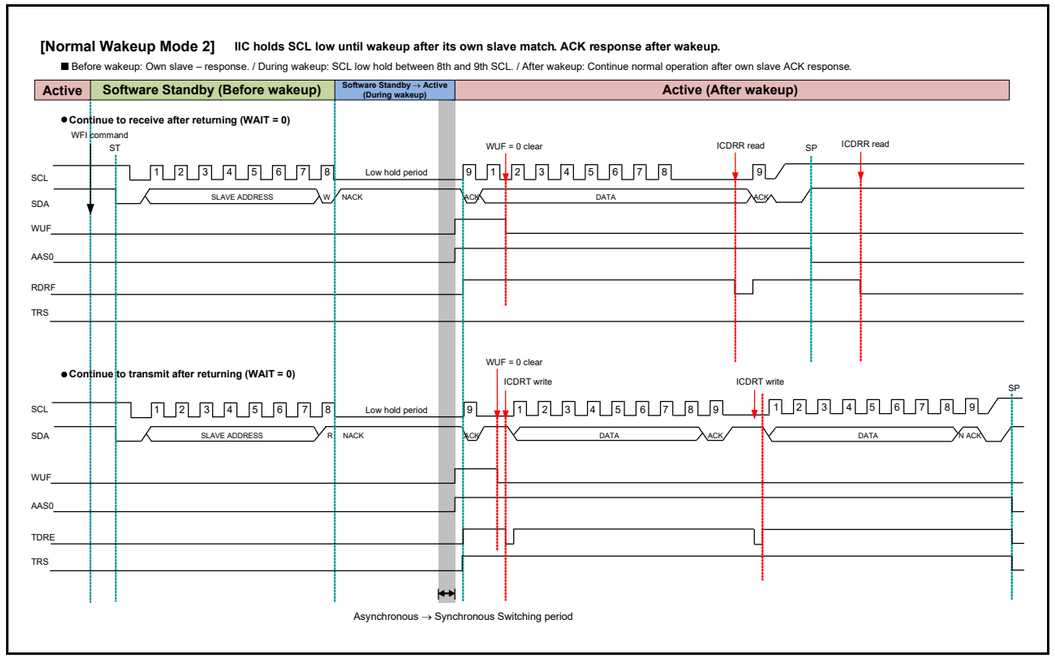


Figure 30.34 Timing of normal wakeup mode 2

30.8.3 Command Recovery Mode/ EEP Response Mode (Special Wakeup Mode)

In the command recovery and EEP response modes, the SCL line is not held low during the wakeup period (after the rise of the 9th clock cycle of SCL). Therefore, the other IIC devices can use the I2C bus during this period.

This section describes the behavior, timing, and an example operation in command recovery and EEP response modes.

A wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

Before wakeup: In response to the data received with its own slave address, the IIC returns ACK (command recovery mode) or NACK (EEP response mode).
During wakeup: The SCL line is not held low.
After wakeup: Normal operation continues after the IIC initialization.

If the slave address does not match, the slave operation continues.

For an example operation in command recovery and EEP response modes, see Figure 30.35. Figure 30.37 shows the detailed timing.

Note: Because the SCL line is not held low during wakeup, transmission or reception of the data that follows the slave address is not possible.
Note: The command recovery and EEP response modes are internal reset states (ICE = IICRST = 1). Therefore, the match of the slave address does not set the flags HOA, GCA, AAS0, AAS1, and AAS2 in the ICSR1 register.

If the transition from Software Standby mode is triggered by an interrupt other than a wakeup interrupt, such as the IRQn for example, the WUF flag is not set to 1. Figure 30.36 shows an operation example.

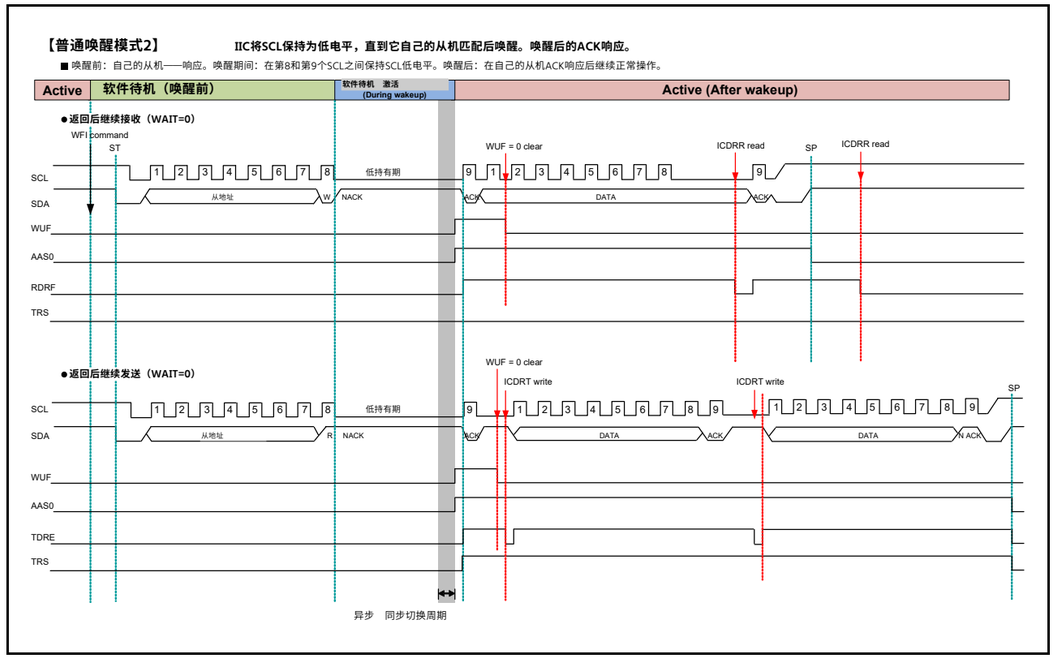


Figure 30.34 正常唤醒模式2的时序

30.8.3 命令恢复模式EEP响应模式（特殊唤醒模式）

在命令恢复和EEP响应模式下，SCL线在唤醒期间（在SCL的第9个时钟周期上升之后）不保持低电平。因此，其他IIC设备在此期间可以使用I2C总线。

本节介绍命令恢复和EEP响应模式下的行为、时序和示例操作。

由从地址匹配触发的唤醒中断启动到正常操作的转换，如下所示：

Before wakeup: IIC以自己的从机地址响应接收到的数据，返回ACK（命令恢复模式）或NACK（EEP响应模式）。
During wakeup: SCL线没有保持低电平。
After wakeup: IIC初始化后继续正常操作。

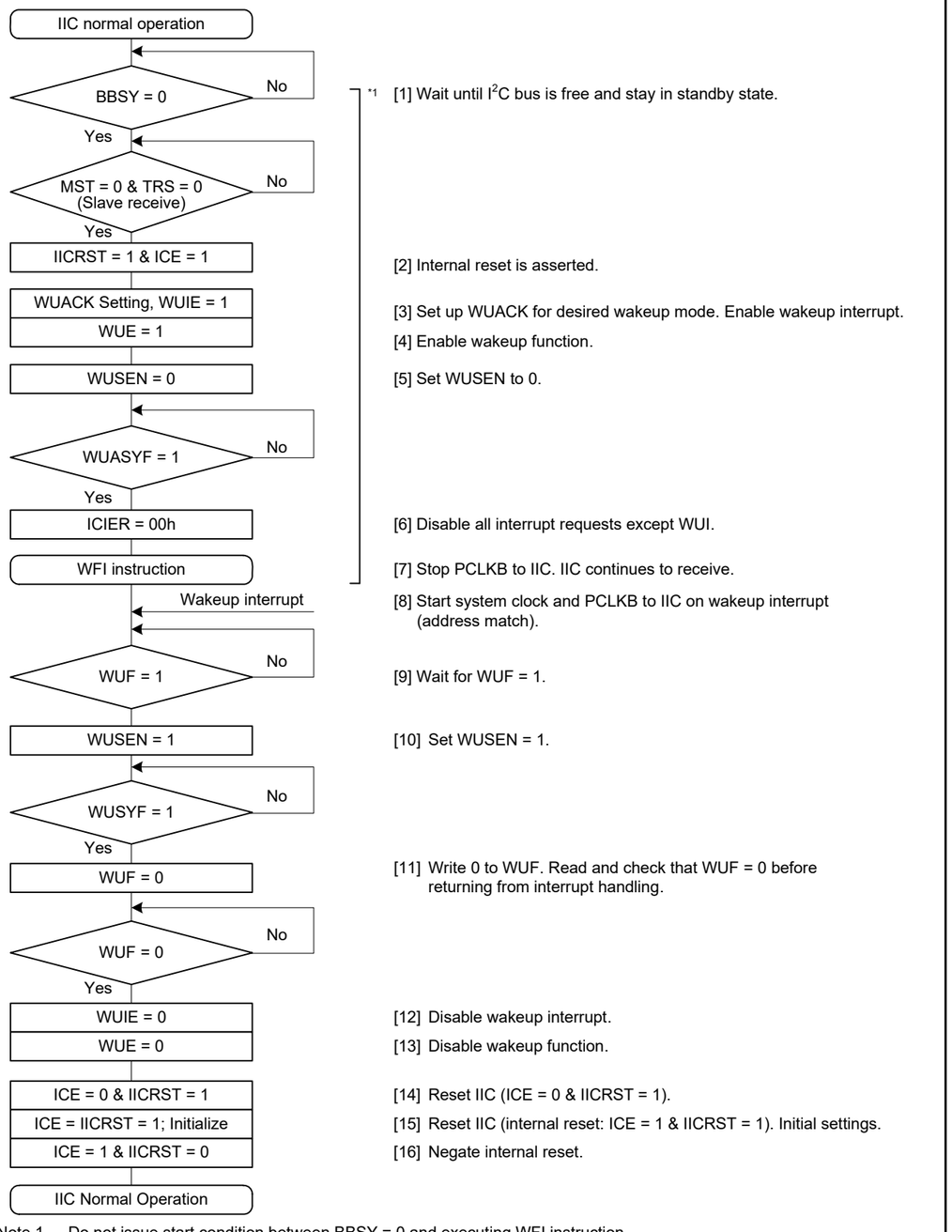
如果从机地址不匹配，从机操作继续。

命令恢复和EEP响应模式下的示例操作，请参见图30.35。图30.37显示了详细的时序。

Note: 因为SCL线在唤醒期间没有保持低电平，所以无法发送或接收跟随从地址的数据。

Note: 命令恢复和EEP响应模式是内部复位状态(ICE=IICRST=1)。因此，从地址的匹配不会设置ICSR1寄存器中的标志HOA、GCA、AAS0、AAS1和AAS2。

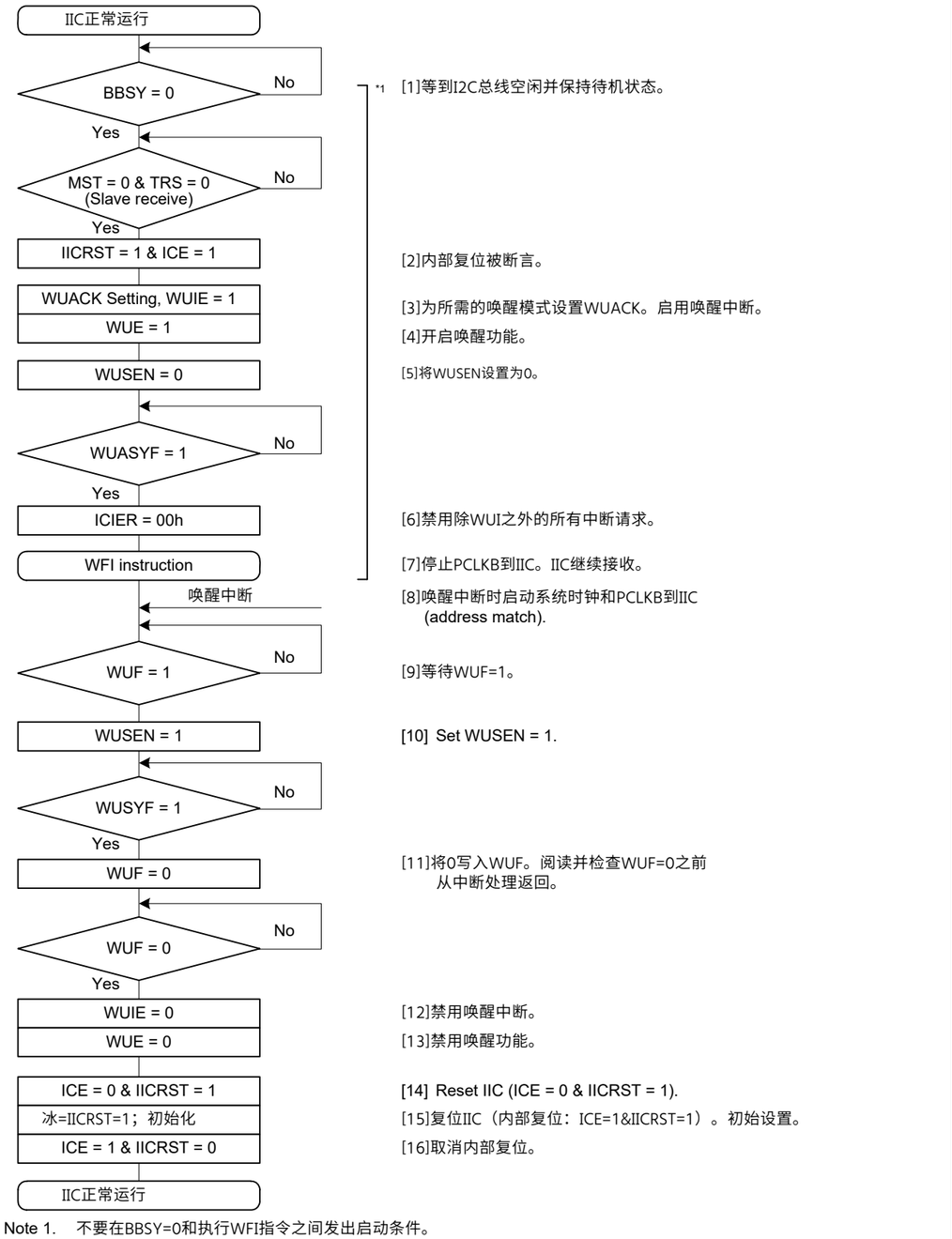
如果从软件待机模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。图30.36显示了一个操作示例。



Note 1. Do not issue start condition between BBSY = 0 and executing WFI instruction.

Figure 30.35 Example operation of command recovery and EEP response modes when wakeup is triggered by a wakeup interrupt on a match of the slave address

Note: See Precautions on the use of the wakeup function.



Note 1. 不要在BBSY=0和执行WFI指令之间发出启动条件。

Figure 30.35 当从地址匹配时由唤醒中断触发唤醒时命令恢复和EEP响应模式的示例操作

Note: 请参阅唤醒功能使用注意事项。

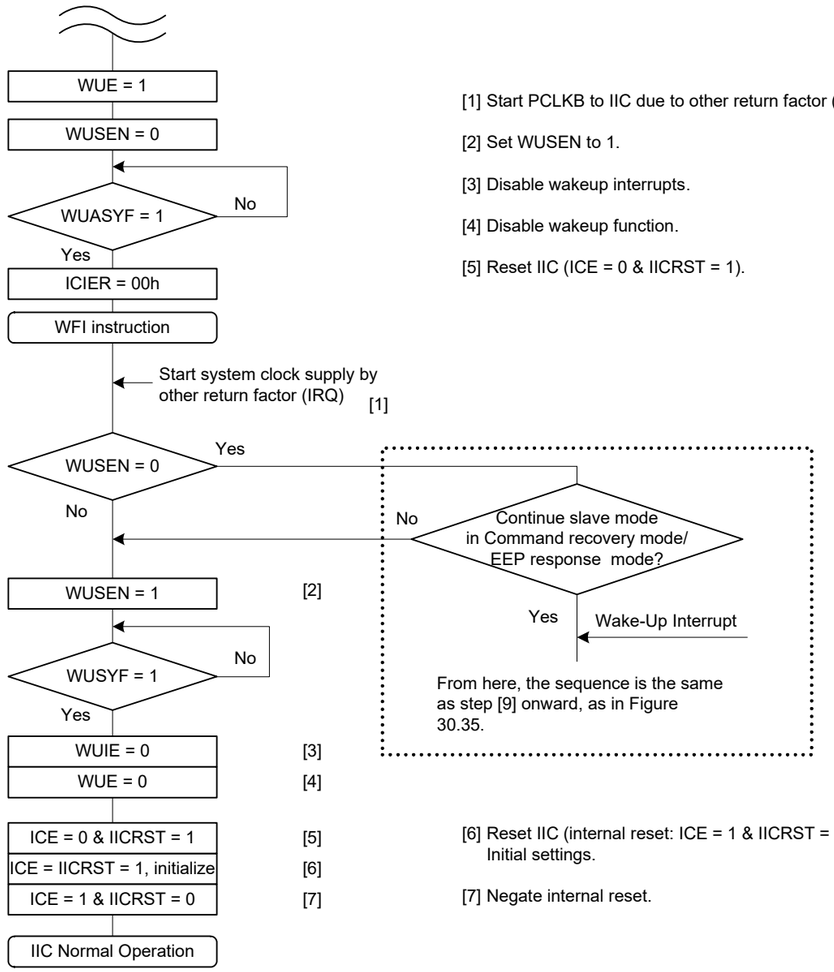


Figure 30.36 Example operation of command recovery and EEP response modes when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, the IRQn

Note: For details of the IIC initial settings, see section 30.3.2, Initial Settings.

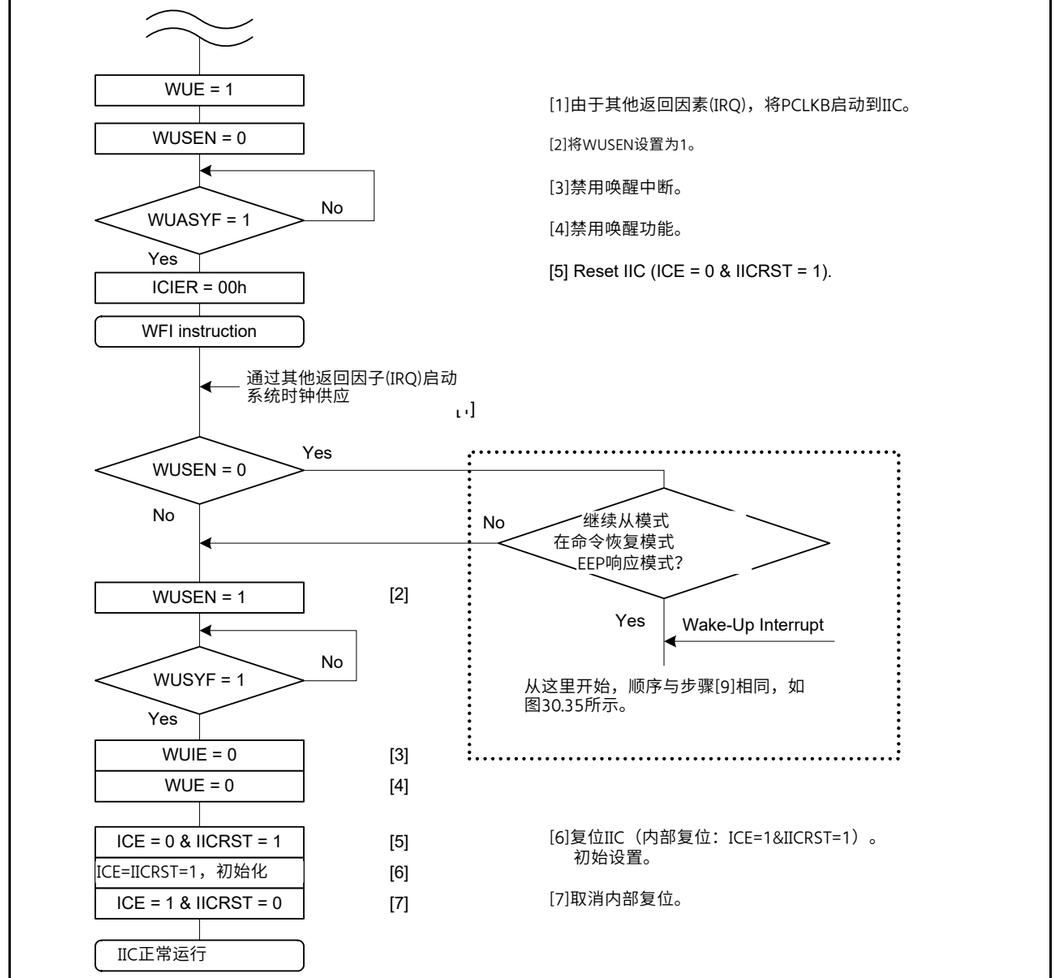


Figure 30.36 由IIC唤醒中断以外的中断（例如IRQn）触发唤醒时的命令恢复和EEP响应模式的示例操作

Note: 有关IIC初始设置的详细信息，请参阅第30.3.2节，初始设置。

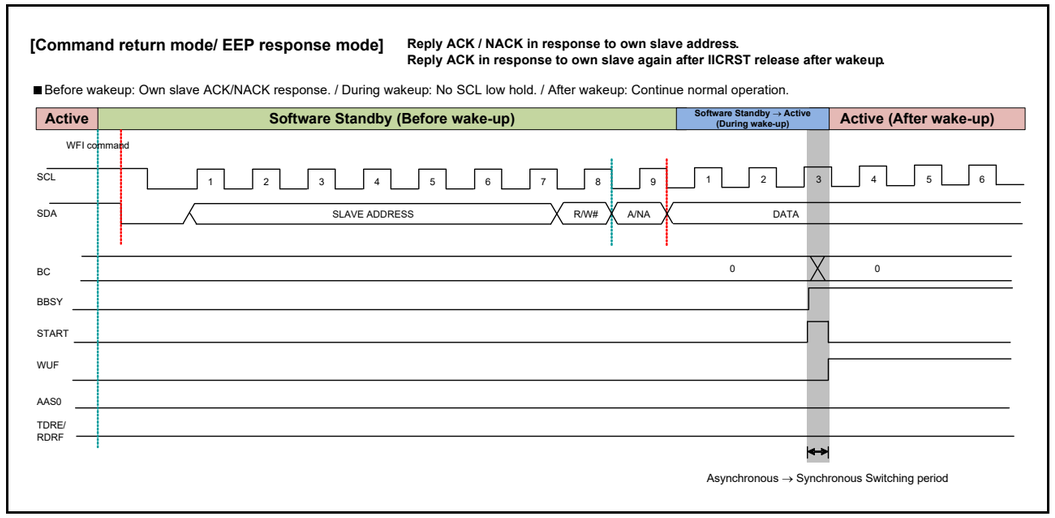


Figure 30.37 Timing of command recovery and EEP response modes

30.8.4 Precautions for WFI Instruction Execution

In the wakeup function examples shown in Figure 30.30, Figure 30.33, and Figure 30.35, make sure that the start condition is not issued during the period from the setting of BBSY = 0 to the execution of the WFI instruction.

When a start condition is issued during this period, NACK is returned after the reception of the first byte of the first data block. Detection of the start or restart condition then enables the wakeup function.

30.9 Automatic Low-Hold Function for SCL

30.9.1 Function to Prevent Wrong Transmission of Transmit Data

If the I2C Bus Shift Register (ICDRS) is empty when data has not been written to the I2C Bus Transmit Data Register (ICDRT) with the IIC in transmission mode (ICCR2.TRS = 1), the SCLn line is automatically held low over the subsequent intervals. This low-hold period is extended until the transmit data is written, which prevents the unintended transmission of erroneous data.

Master transmit mode:

- Low-level interval after a start or restart condition is issued
- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

Slave transmit mode:

- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

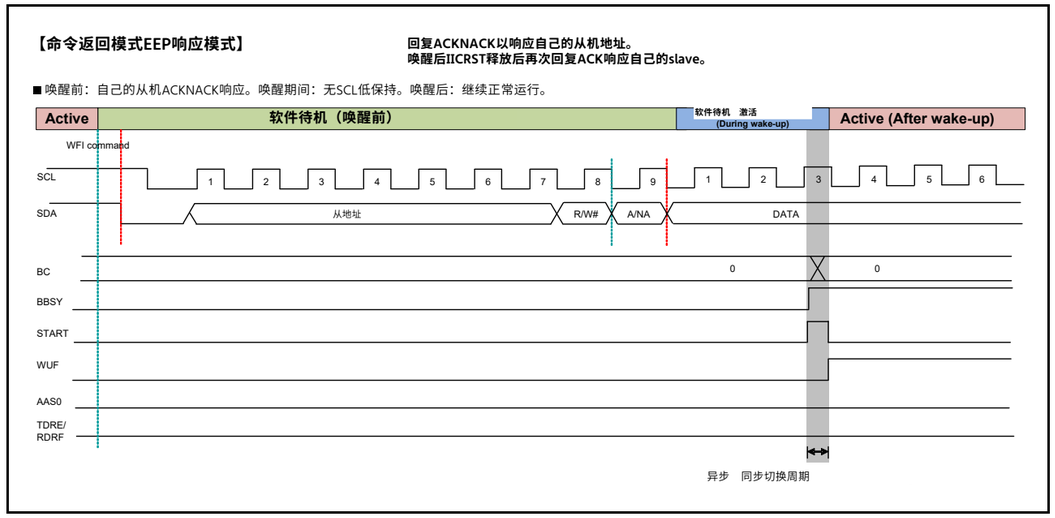


Figure 30.37 命令恢复和EEP响应模式的时序

30.8.4 WFI指令执行注意事项

在图30.30、图30.33和图30.35所示的唤醒功能示例中，请确保从设置BBSY=0到执行WFI指令期间不发出启动条件。

如果在此期间发出启动条件，则在接收到第一个数据块的第一个字节后返回NACK。启动或重启条件的检测然后启用唤醒功能。

30.9 SCL的自动低保持功能

30.9.1 防止传输数据错误传输的功能

如果I2C总线移位寄存器(ICDRS)在IIC处于传输模式(ICCR2.TRS=1)时尚未将数据写入I2C总线传输数据寄存器(ICDRT)时为空，则SCLn线自动在随后的时间间隔内保持低位。这个低保持期一直延长到发送数据被写入，这样可以防止错误数据的意外传输。

主传输模式：

- 发出启动或重启条件后的低电平间隔
- 一次传输的第9个时钟周期和下一次传输的第1个时钟周期之间的低电平间隔。

从机发送模式：

- 一次传输的第9个时钟周期和下一次传输的第1个时钟周期之间的低电平间隔。

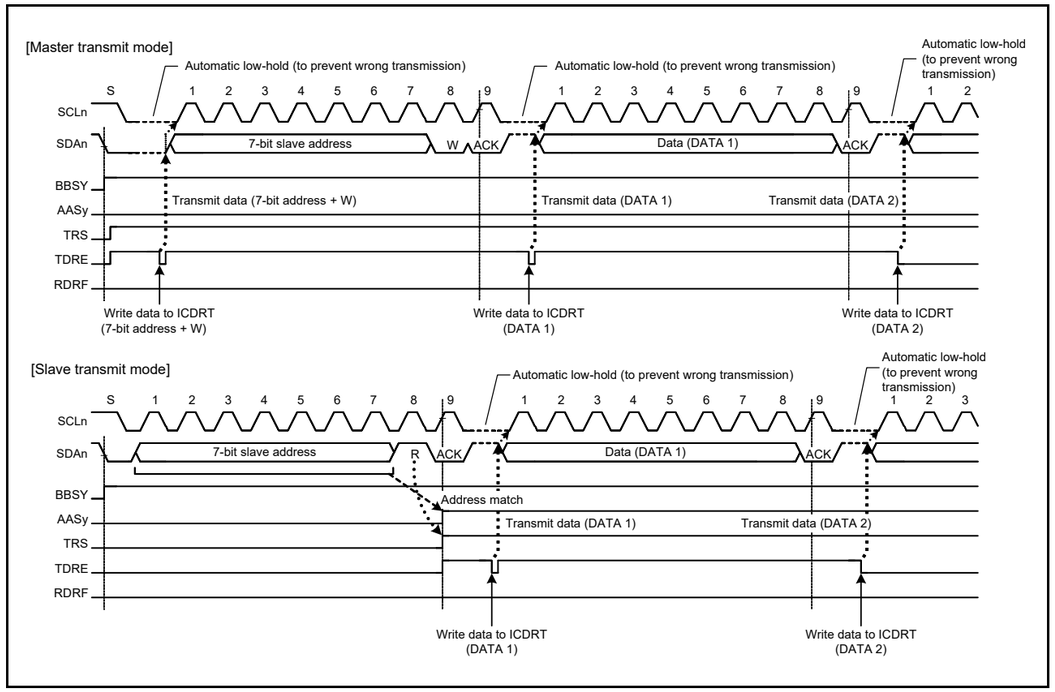


Figure 30.38 Automatic low-hold operation in transmit mode

30.9.2 NACK Reception Transfer Suspension Function

This function suspends transfer operation when NACK is received in transmit mode (the ICCR2.TRS bit is 1). This function is enabled when the NACKE bit in ICFER is set to 1 (transfer suspension enabled). If the next transmit data is written (ICSR2.TDRE flag is 0) when the NACK is received, the next data transmission on the falling edge of the 9th SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (ICSR2.NACKF flag is 1), transmit and receive operations are discontinued. To restore transmit and receive operations, set the NACKF flag to 0. In master transmit mode, after issuing a restart or stop condition, set the NACKF flag to 0, and then issue a start condition again.

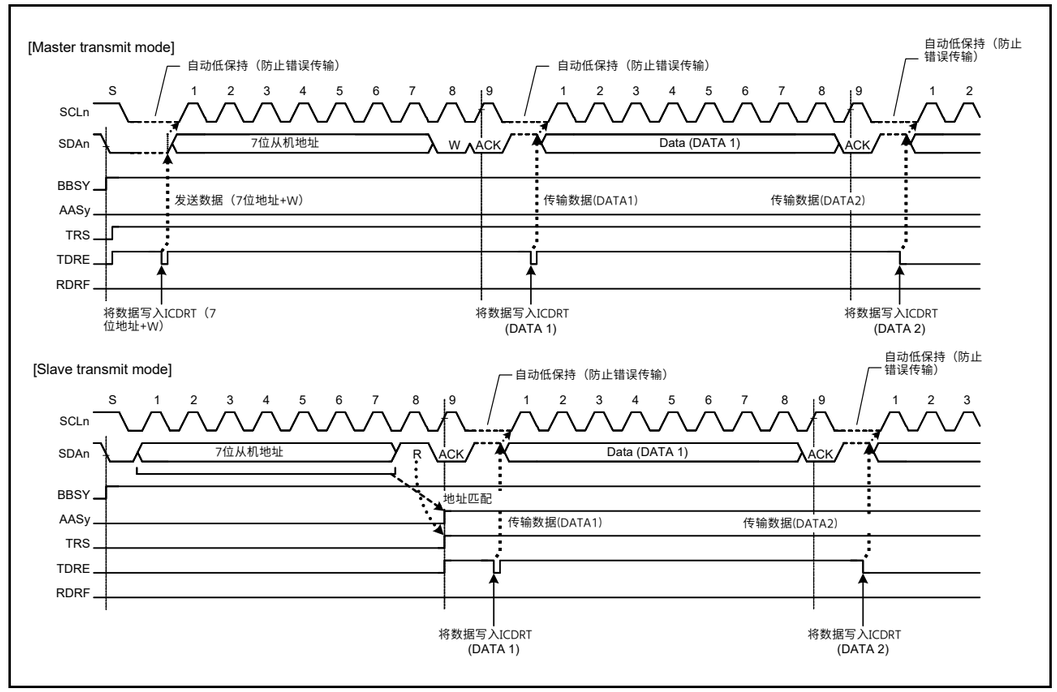


Figure 30.38 发送模式下的自动低保持操作

30.9.2 NACK接收传输暂停功能

当在发送模式下接收到NACK（ICCR2.TRS位为1）时，该函数暂停传输操作。当ICFER中的NACKE位设置为1（传输暂停使能）时，该功能被启用。如果在收到NACK时写入下一个发送数据（ICSR2.TDRE标志为0），则在第9个SCL时钟周期的下降沿自动暂停下一个数据发送。这可以防止SDAn线路输出电平保持在低电平时

下一个发送数据的MSB为0。

如果该函数暂停传输操作（ICSR2.NACKF标志为1），则停止发送和接收操作。要恢复发送和接收操作，请将NACKF标志设置为0。在主机发送模式下，发出重新启动或停止条件后，将NACKF标志设置为0，然后再次发出启动条件。

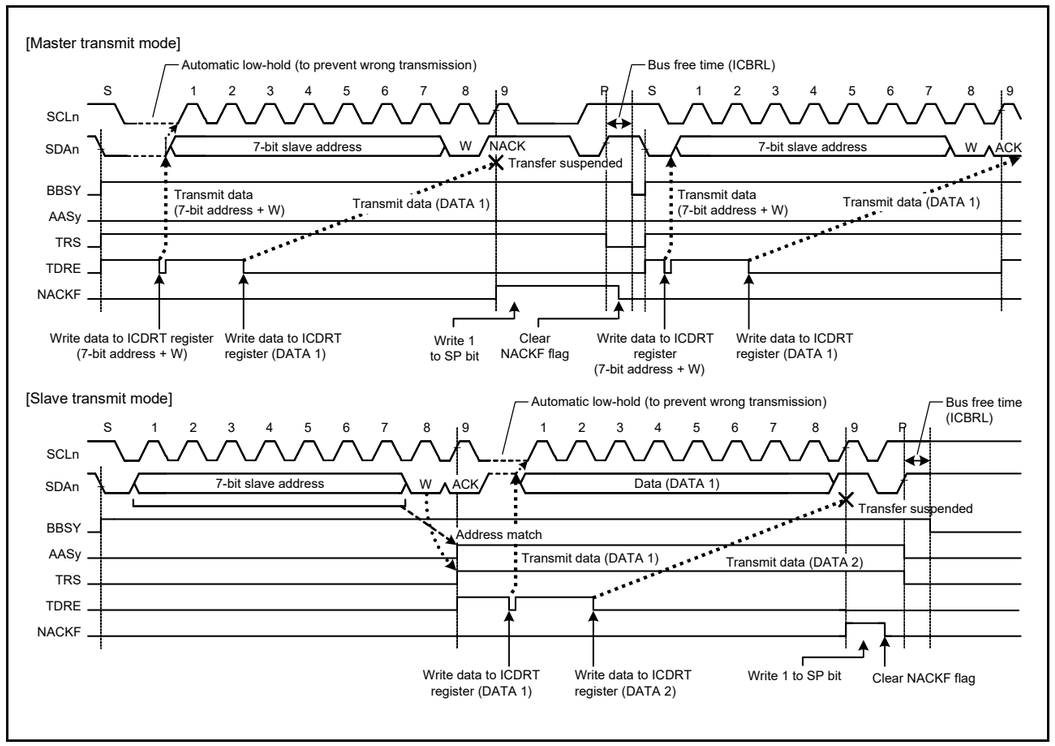


Figure 30.39 Suspension of data transfer when NACK is received (NACKE = 1)

30.9.3 Function to Prevent Failure to Receive Data

If response processing when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (ICSR2.RDRF = 1) in receive mode (ICCR2.TRS = 0), the IIC holds the SCLn line low automatically immediately before the next data is received to prevent failure to receive data.

This function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, the IIC slave address is designated after a stop condition is issued. This function does not interfere other communication because the IIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Periods in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in the ICMR3 register.

(1) 1-byte receive operation and automatic low-hold function using the WAIT bit

When the WAIT bit in the ICMR3 register is set to 1, the IIC performs a 1-byte receive operation using the WAIT bit function. Additionally, when the ICMR3.RDRFS bit is 0, the IIC automatically sends the ICMR3.ACKBT bit value for the acknowledge bit in the period from the falling edge of the 8th SCL clock cycle to the falling edge of the 9th SCL clock cycle, and automatically holds the SCLn line low on the falling edge of the 9th SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from the ICDRR register, which enables byte-wise receive operation.

The WAIT bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master receive mode or slave receive mode.

(2) 1-byte receive operation (ACK/NACK transmission control) and automatic low-hold function using the RDRFS bit

When the RDRFS bit in the ICMR3 register is set to 1, the IIC performs a 1-byte receive operation using the RDRFS bit

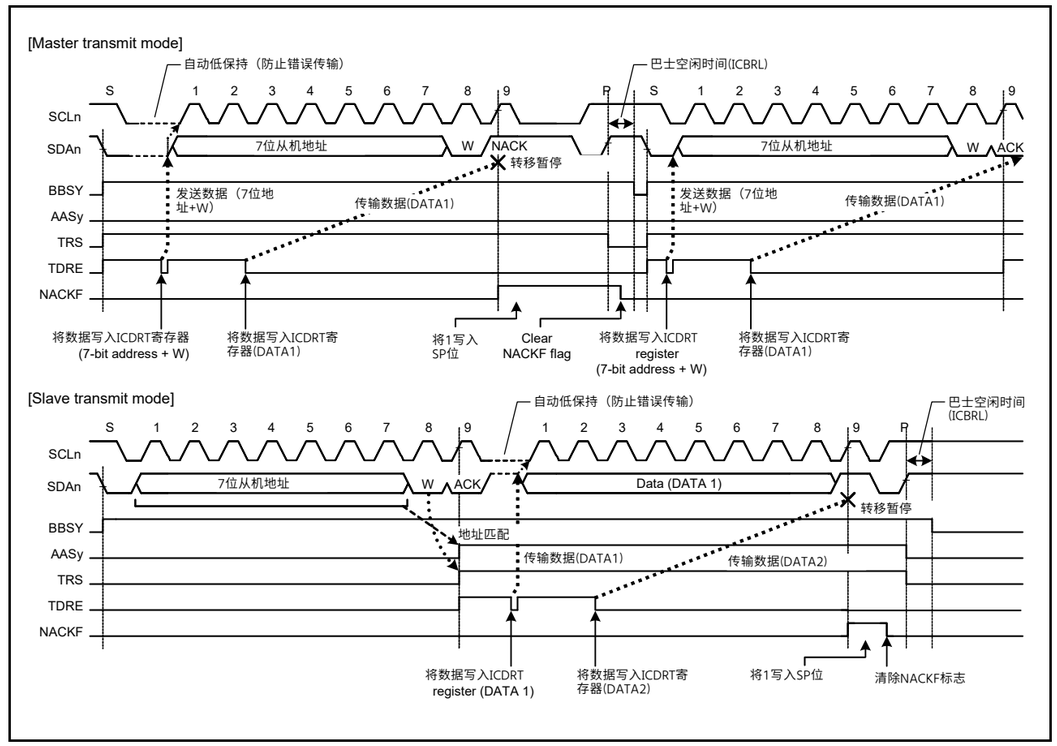


Figure 30.39 接收到NACK时暂停数据传输(NACKE=1)

30.9.3 防止数据接收失败的功能

如果在接收模式(ICCR2.TRS=0)下接收数据(ICDRR)读取延迟一个传输帧或更长时间且接收数据已满(ICSR2.RDRF=1)时的响应处理，则IIC将SCLn线保持为低电平在接收到下一个数据之前自动进行，以防止接收数据失败。

即使最终接收数据的读取处理被延迟，该功能也被启用，同时，在发出停止条件后指定IIC从地址。此功能不会干扰其他通信，因为在发出停止条件后发生与其自己的从地址不匹配时，IIC不会将SCLn线保持为低电平。

SCLn线保持低电平的周期可以通过WAIT和RDRFS位的组合来选择
ICMR3 register.

(1) 使用WAIT位的1字节接收操作和自动低保持功能

当ICMR3寄存器中的WAIT位设置为1时，IIC使用WAIT位功能执行1字节接收操作。此外，当ICMR3.RDRFS位为0时，IIC会在第8个SCL时钟周期的下降沿到第9个SCL时钟周期的下降沿期间自动发送ICMR3.ACKBT位值作为确认位，并使用WAIT位功能在第9个SCL时钟周期的下降沿自动将SCLn线保持为低电平。该低保持通过从ICDRR寄存器读取数据来释放，从而启用逐字节接收操作。

在主机接收模式或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧使能WAIT位功能。

(2) 1字节接收操作（ACKNACK传输控制）和使用RDRFS位的自动低保持功能

当ICMR3寄存器中的RDRFS位设置为1时，IIC使用RDRFS位执行1字节接收操作

function. When the RDRFS bit is set to 1, the RDRF flag (receive data full) in ICSR2 is set to 1 on the rising edge of the 8th SCL clock cycle, and the SCLn line is automatically held low on the falling edge of the 8th SCL clock cycle. This low-hold is released by writing to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation through the ACK or NACK transmission control based on the data received in byte units.

The RDRFS bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master receive mode or slave receive mode.

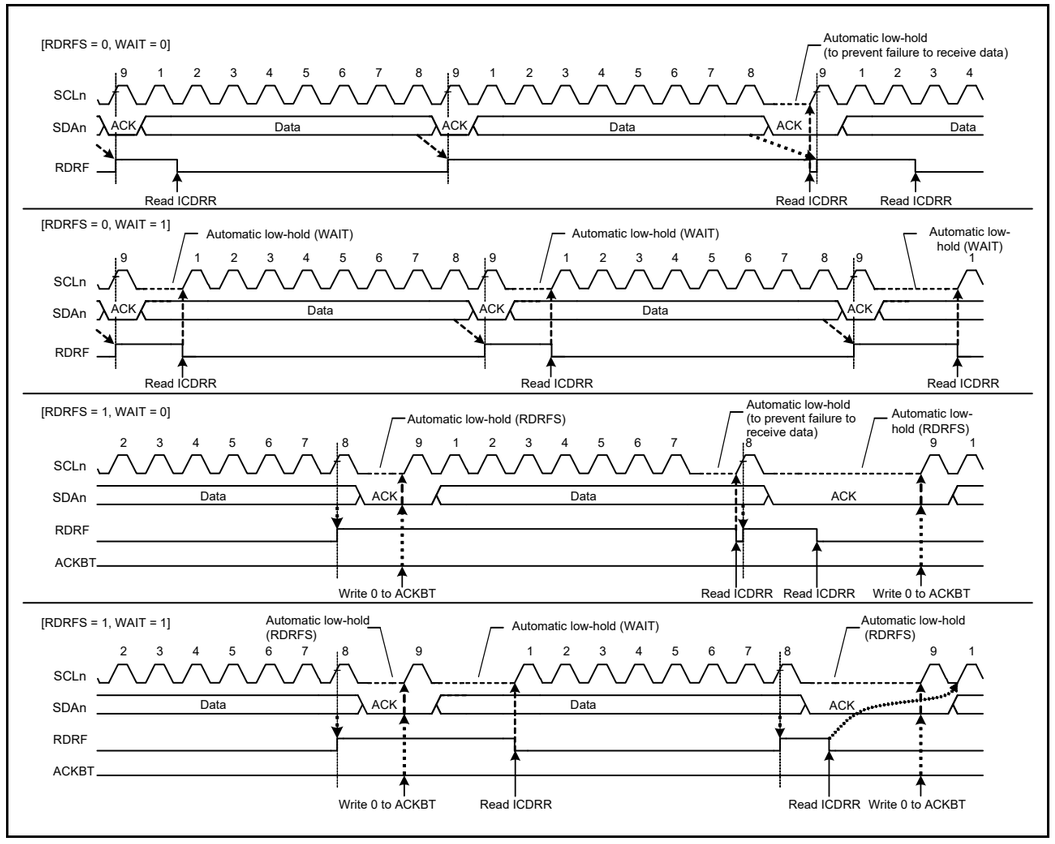


Figure 30.40 Automatic low-hold operation in receive mode using RDRFS and WAIT bits

30.10 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C bus standard, the IIC has functions to prevent double-issue of a start condition, detect arbitration-lost during transmission of NACK, and detect arbitration-lost in slave transmit mode.

30.10.1 Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line was already driven low by another master device issuing a start condition, the IIC regards its own start condition issue as an error and considers this a loss in arbitration. Priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the IIC regards this as a double-issuing-of-start-condition error and considers itself to have lost the arbitration. This prevents a failure of transfer resulting from a start condition issued while transfer is in progress.

When a start condition is issued successfully, if the transmit data including the address bits (internal SDA output level) and the level on the SDAn line do not match, the IIC loses the arbitration.

功能。当RDRFS位设置为1时，ICSR2中的RDRF标志（接收数据已满）在第8个SCL时钟周期的上升沿设置为1，并且SCLn线在第8个下降沿自动保持为低第SCL时钟周期。该低保持可通过写入ICMR3中的ACKBT位来释放，但不能通过从ICDRR读取数据来释放，这样可以根据以字节为单位接收的数据通过ACK或NACK传输控制进行接收操作。

在主接收模式或从接收模式下获得与IIC从地址匹配的接收帧（包括广播地址和主机地址）后，使能RDRFS位功能。

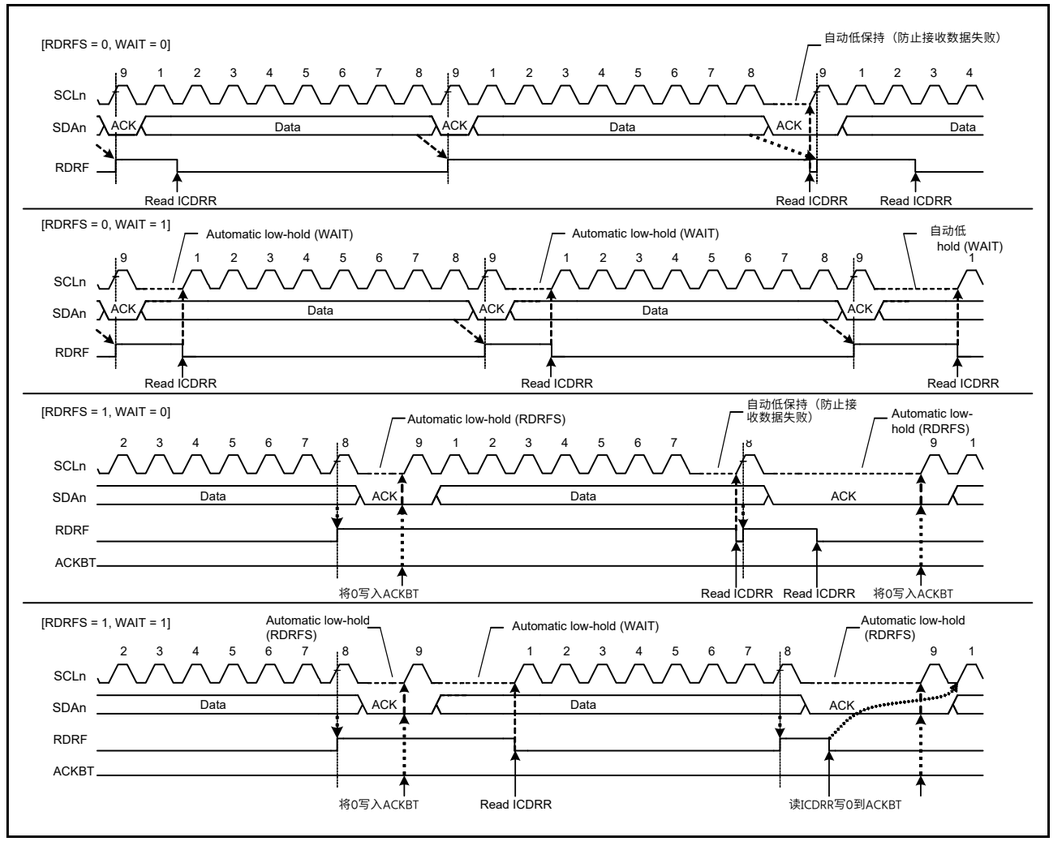


Figure 30.40 使用RDRFS和WAIT位在接收模式下自动保持低电平操作

30.10 仲裁丢失检测功能

除了I2C总线标准定义的正常仲裁丢失检测功能外，IIC还具有防止重复发出启动条件、在NACK传输期间检测仲裁丢失以及在从机发送中检测仲裁丢失的功能模式。

30.10.1 主仲裁丢失检测（MALE位）

IIC将SDAn线驱动为低电平以发出启动条件。但是，如果SDAn线已经被另一个发出启动条件的主设备驱动为低电平，则IIC将自己的启动条件问题视为错误，并认为这是仲裁失败。其他主设备优先传输。类似地，如果在总线繁忙时通过将ICCR2中的ST位设置为1来请求发出启动条件（ICCR2中的BBSY标志=1），则IIC将此视为双重发出启动条件错误并认为自己失去了仲裁。这可以防止传输过程中发出的开始条件导致传输失败。

成功发出启动条件后，如果发送数据包括地址位（内部SDA输出电平）与SDAn线上的电平不匹配，则IIC失去仲裁。

After a loss in arbitration of mastership, the IIC immediately enters slave receive mode. If a slave address, including the general call address, matches its own address at this time, the IIC continues in slave operation.

A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER register is 1 (master arbitration-lost detection enabled).

[Master arbitration-lost conditions]

- Mismatching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ST bit in ICCR2 to 1 while the ICCR2.BBSY flag is set to 0 (erroneous issuing of a start condition)
- Setting of the ICCR2.ST bit to 1 (start condition double-issue error) while the BBSY flag is 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2).

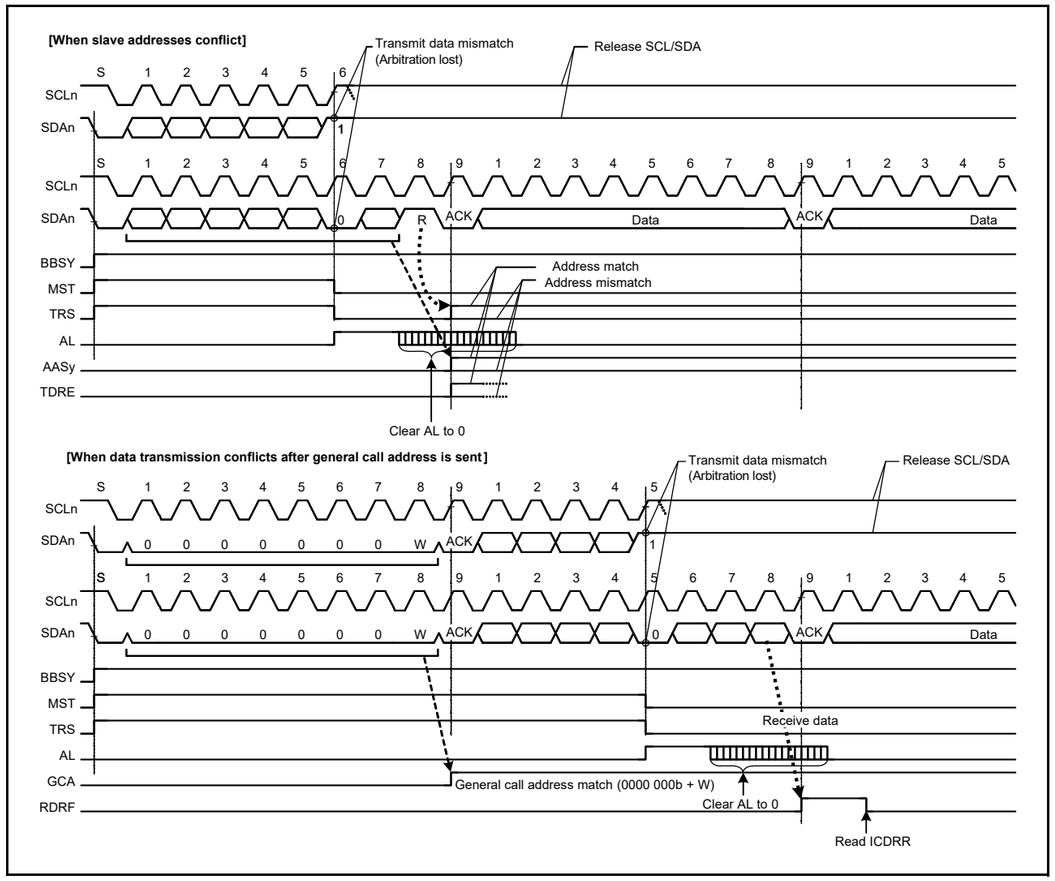


Figure 30.41 Examples of master arbitration-lost detection (MALE = 1)

在主控权仲裁失败后，IIC立即进入从机接收模式。如果此时从机地址（包括广播地址）与自己的地址匹配，则IIC继续从机操作。

当ICFER寄存器中的MALE位为1（启用主控仲裁丢失检测）时满足以下条件时，检测到主控仲裁丢失。

[Master arbitration-lost conditions]

- 通过将ICCR2中的ST位设置为1而ICCR2.BBSY标志设置为0发出启动条件后，SDA输出的内部电平与SDAn线上的电平不匹配（错误发出启动条件）
- 当BBSY标志为1时，将ICCR2.ST位设置为1（启动条件双发错误）
- 当发送数据不包括确认（内部SDA输出电平）与主发送模式下SDAn线上的电平不匹配时（ICCR2中的MST和TRS位=11b）。

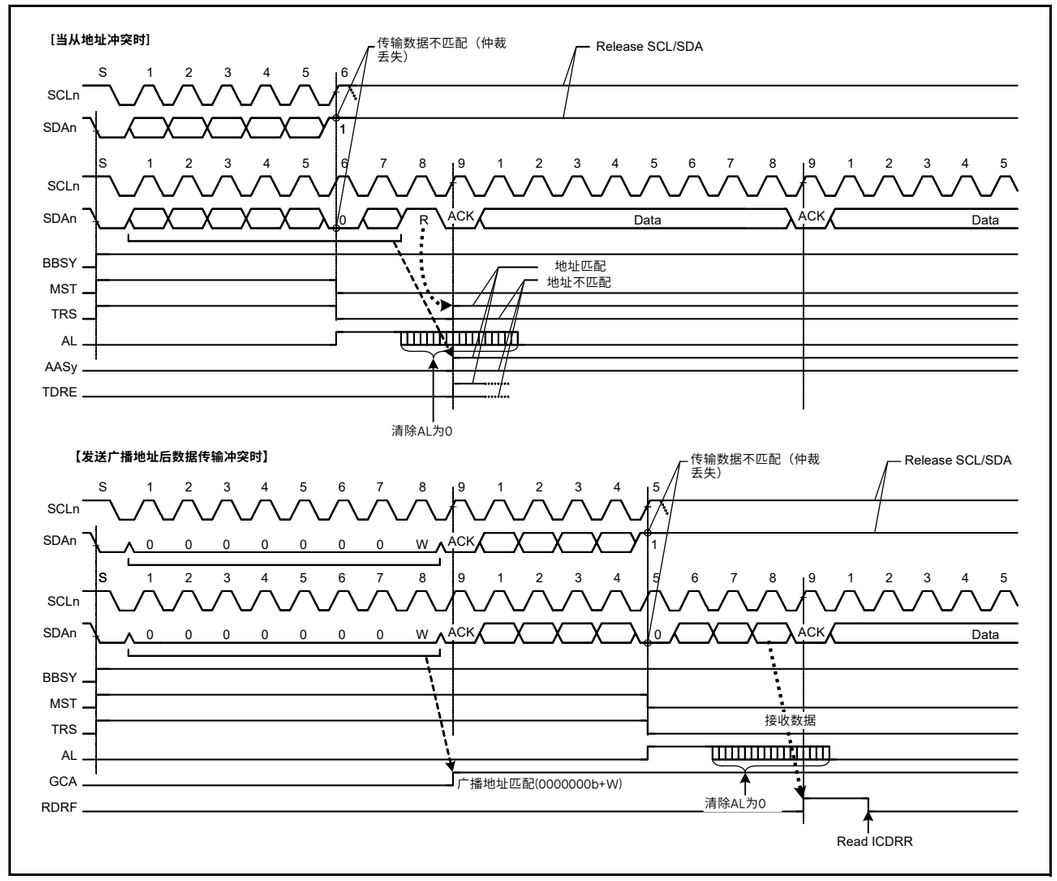


Figure 30.41 主仲裁丢失检测示例(MALE=1)

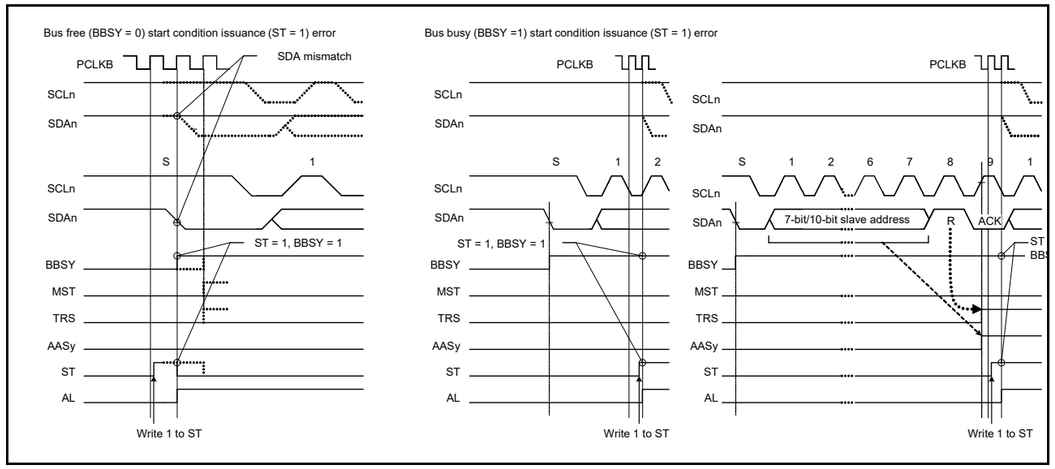


Figure 30.42 Arbitration-lost when start condition is issued (MALE = 1)

30.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

This function causes arbitration to be lost if the internal SDA output level does not match the level on the SDAn line during transmission of NACK in receive mode. Arbitration is lost because of a conflict between NACK and ACK transmissions when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such a conflict occurs when multiple master devices send or receive the same information through a single slave device. Figure 30.43 shows an example of arbitration-lost detection during transmission of NACK.

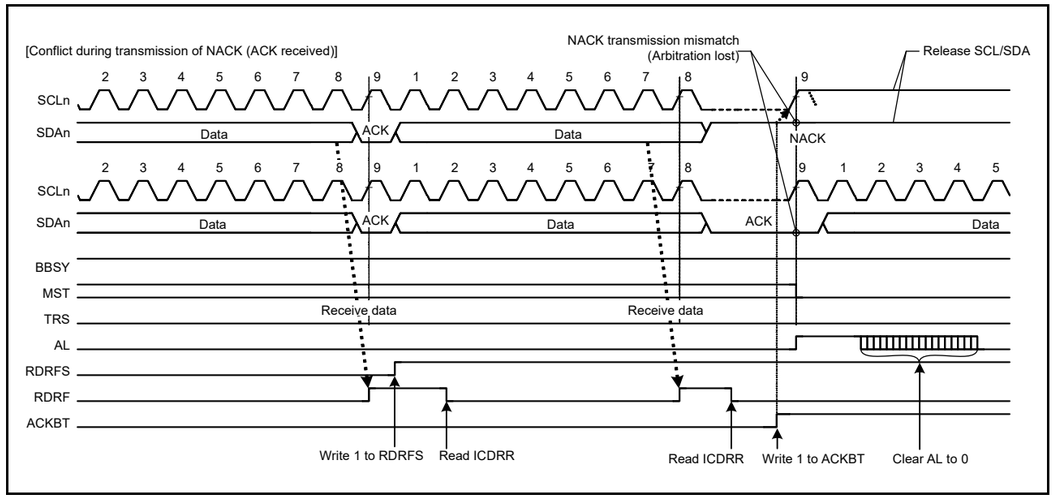


Figure 30.43 Example of arbitration-lost detection during transmission of NACK (NALE = 1)

The following description explains arbitration-lost detection using an example in which two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in either master A and master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the required 4 bytes of data.

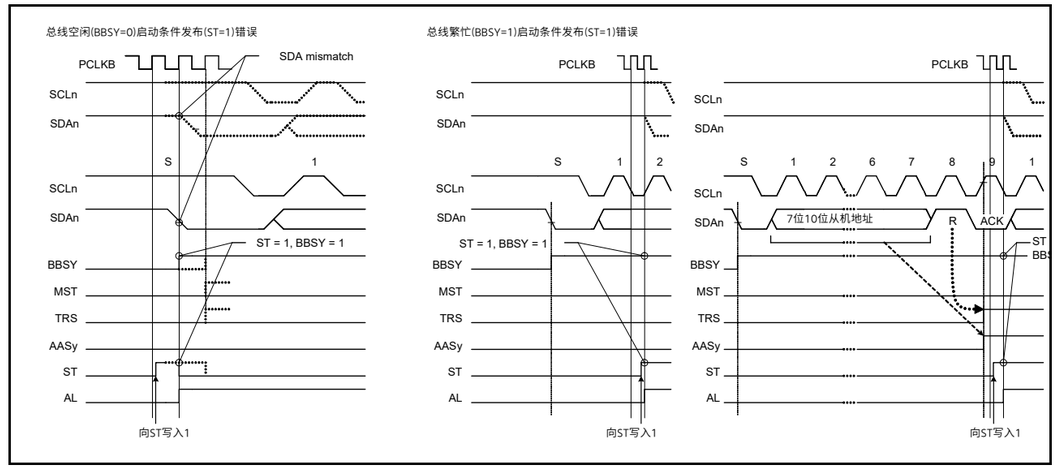


Figure 30.42 发出启动条件时仲裁失败(MALE=1)

30.10.2 在NACK传输期间检测仲裁丢失的功能（NALE位）

如果在接收模式下发送NACK期间内部SDA输出电平与SDAn线上的电平不匹配，此功能会导致仲裁丢失。当多主控系统中两个或多个主控设备同时从同一从属设备接收数据时，由于NACK和ACK传输之间的冲突，仲裁会丢失。当多个主设备通过单个从设备发送或接收相同的信息时，就会发生这种冲突。图30.43显示了在NACK传输期间检测仲裁丢失的示例。

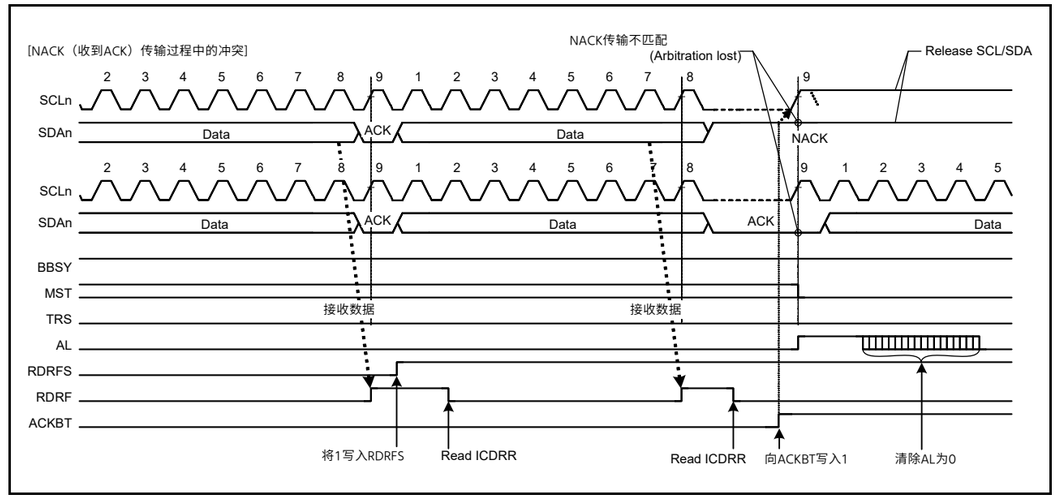


Figure 30.43 NACK(NALE=1)传输期间的仲裁丢失检测示例

以下描述使用通过总线连接两个主设备（主设备A和主设备B）和单个从设备的示例来说明仲裁丢失检测。在本例中，主设备A从从设备接收2个字节的数据，主设备B从从设备接收4个字节的数据。

如果主设备A和主设备B同时访问从设备，由于从设备地址相同，在访问从设备期间，主设备A和主设备B都不会丢失仲裁。因此，主机A和主机B都承认他们已经获得了总线控制权并照此运行。主设备A在从从设备接收到2个最终字节的数据时发送NACK。同时，masterB发送ACK，因为它没有收到所需的4字节数据。

The NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect the ACK transmitted by master B and issues a stop condition. Therefore, the stop condition issue conflicts with the SCL clock output of master B, which disrupts communication.

When the IIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost. If arbitration is lost during transmission of NACK, the IIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing, such as FFh transmission processing, which is required if the UDID (Unique Device Identifier) of the assigned address does not match in the Get UDID general processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ICMR3.ACKBT = 1).

30.10.3 Slave Arbitration-Lost Detection (SALE Bit)

This function causes arbitration to be lost if the transmit data and the level on the SDAn line do not match in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

When the IIC loses slave arbitration, the IIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing, or processing for the transmission of FFh.

The IIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2).

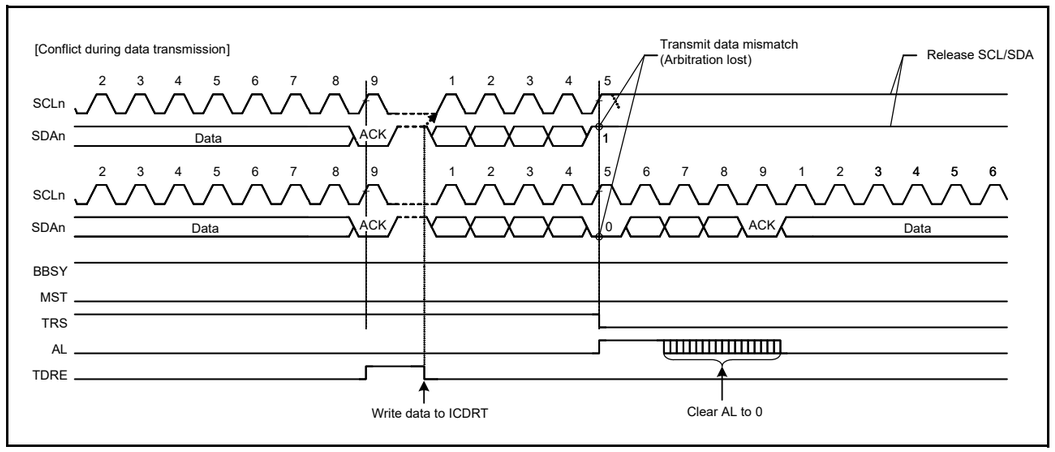


Figure 30.44 Example of slave arbitration-lost detection (SALE = 1)

来自主机A的NACK传输和来自主机B的ACK传输冲突。一般来说，如果发生这样的冲突，masterA无法检测到masterB发送的ACK并发出停止条件。因此，停止条件问题与主B的SCL时钟输出冲突，从而中断通信。

当IIC在NACK传输过程中收到ACK时，它会检测到与其他主设备冲突的失败并导致仲裁丢失。如果在NACK传输过程中仲裁丢失，IIC立即取消从机匹配条件并进入从机接收模式。这可以防止发出停止条件，从而防止总线上的通信故障。

同样，在SMBus的ARP命令处理中，检测传输过程中仲裁丢失的功能
NACK也可用于消除额外的时钟周期处理，例如FFh传输处理，如果分配地址的UDID（唯一设备标识符）在分配地址命令后的获取UDID常规处理中不匹配，则需要此处理。

IIC在NACK传输期间检测到仲裁丢失，当满足以下条件时
ICFER设置为1（启用NACK传输期间的仲裁丢失检测）。

[在NACK传输期间仲裁丢失的条件]

- 在NACK(ICMR3.ACKBT=1)传输期间内部SDA输出电平与SDAn线不匹配时（接收到ACK）。

30.10.3 从设备仲裁丢失检测（SALE位）

如果在从发送模式下发送数据和SDAn线上的电平不匹配，此功能会导致仲裁丢失。这种仲裁丢失检测功能主要用于通过SMBus传输UDID（唯一设备标识符）时。

当IIC失去从机仲裁时，IIC立即从从机匹配状态中释放并进入从机接收模式。此功能可以检测在SMBus上传输UDID期间的数据冲突，并消除后续的冗余处理或FFh传输处理。

当ICFER中的SALE位设置为1（启用从设备仲裁丢失检测）满足以下条件时，IIC检测从设备仲裁丢失。

[从机仲裁失败的条件]

- 当发送数据不包括确认（内部SDA输出电平）与从发送模式下的SDAn线不匹配时（MST和TRS位=ICCR2中的01b）。

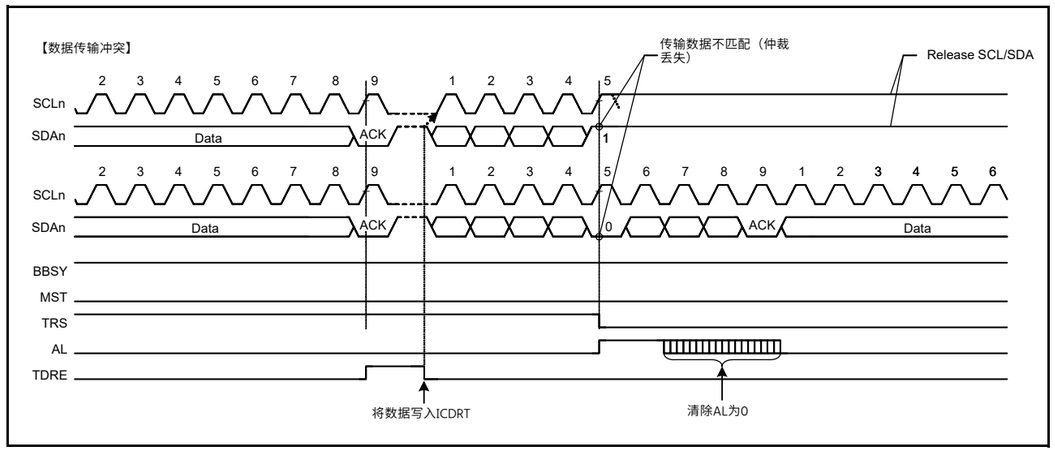


Figure 30.44 从机仲裁丢失检测示例(SALE=1)

30.11 Start, Restart, and Stop Condition Issuing Function

30.11.1 Issuing a Start Condition

The IIC issues a start condition when the ST bit in ICCR2 is set to 1.

When the ST bit is set to 1, a start condition request is made. The IIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the IIC automatically shifts to the master transmit mode.

To issue a start condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the time set in ICBRH and the start condition hold time elapse.
3. Drive the SCLn line low (high level to low level).
4. Detect low level of the SCLn line and ensure that the low-level period of the SCLn line set in ICBRL elapses.

30.11.2 Issuing a Restart Condition

The IIC issues a restart condition when the RS bit in ICCR2 is set to 1.

When the RS bit is set to 1, a restart condition request is made. The IIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a restart condition:

1. Release the SDAn line.
2. Ensure the low-level period of SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level of the SCLn line and ensure that the time set in ICBRL and the restart condition setup time elapse.
5. Drive the SDAn line low (high level to low level).
6. Ensure the time set in ICBRH and the restart condition hold time elapse.
7. Drive the SCLn line low (high level to low level).
8. Detect a low level of the SCLn line and ensure the low-level period of SCLn line set in ICBRL elapses.

Note: When issuing restart condition requests, write the slave address to ICDRT after confirming that ICCR2.RS is 0. Data written while ICCR2.RS = 1 is not forwarded because of the retransmission condition before the occurrence.

30.11 启动、重启和停止条件发布功能

30.11.1 发出开始条件

当ICCR2中的ST位设置为1时，IIC发出启动条件。

当ST位设置为1时，发出启动条件请求。IIC发出一个启动条件，当BBSY标志在ICCR2为0（总线空闲状态）。当启动条件正常发出时，IIC自动切换到主机发送模式。

发出开始条件：

1. 将SDAn线驱动为低电平（高电平到低电平）。
2. 确保ICBRH中设置的时间和启动条件保持时间已过。
3. 将SCLn线驱动为低电平（高电平到低电平）。
4. 检测SCLn线的低电平，确保经过ICBRL中设置的SCLn线的低电平周期。

30.11.2 发出重启条件

当ICCR2中的RS位设置为1时，IIC发出重启条件。

当RS位设置为1时，发出重启条件请求。当BBSY标志在IIC发出重启条件ICCR2为1（总线繁忙状态），ICCR2中的MST位为1（主机模式）。

发出重启条件：

1. 释放SDAn线。
2. 确保ICBRL中设置的SCLn线的低电平周期已过。
3. 释放SCLn线（低电平到高电平）。
4. 检测SCLn线的高电平，并确保经过ICBRL中设置的时间和重启条件设置时间。
5. 将SDAn线驱动为低电平（高电平到低电平）。
6. 确保ICBRH中设置的时间和重启条件保持时间已过。
7. 将SCLn线驱动为低电平（高电平到低电平）。
8. 检测SCLn线的低电平，确保经过ICBRL中设置的SCLn线的低电平周期。

Note: 发出重启条件请求时，确认ICCR2.RS为0后，将从机地址写入ICDRT。在ICCR2.RS=1时写入的数据由于发生前的重传条件而不会转发。

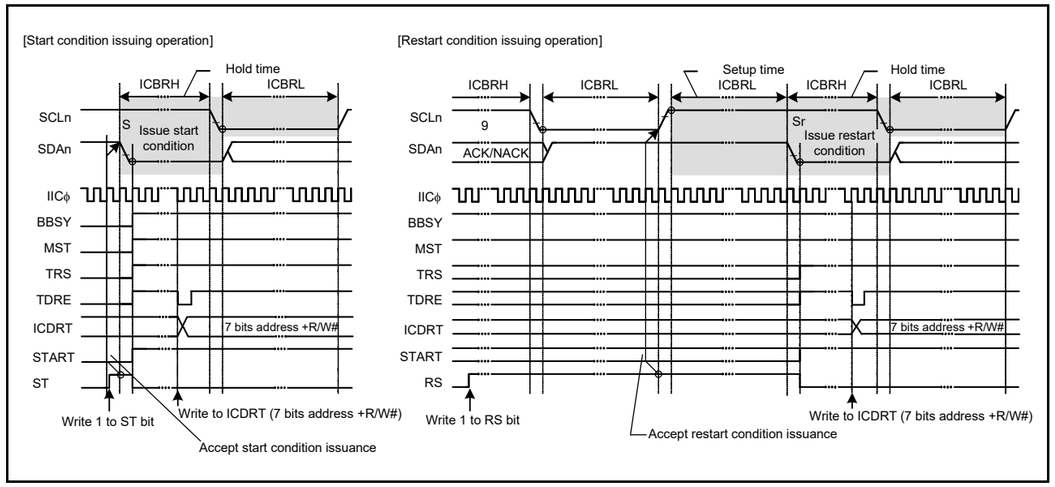


Figure 30.45 Start or restart condition issue timing using the ST and RS bits

Figure 30.46 shows the operation timing when a restart condition is issued after the master transmission.

To issue a restart condition after the master transmission:

1. Initialize the IIC using the details provided in section 30.3.2, Initial Settings.
2. Read the IICR2.BBSY flag to check that the bus is free, and then set the ICCR2.ST bit to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the ICSR2.BBSY flag and ICSR2.START flag are automatically set to 1 and the ST bit is automatically set to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that a start condition is successfully issued as requested by the ST bit. The MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 when the TRS bit is set to 1.
3. Check that the ICSR2.TDRE flag is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. After the transmit data is written to ICDRT, the TDRE flag is automatically set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag is set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 0, the IIC continues in master transmit mode. If the ICSR2.NACKF flag is 1 at this time, indicating that no slave device recognized the address or there was an error in communications, write 1 to ICCR2.SP bit to issue a stop condition.

   To transmit data with an address in the 10-bit format, start by writing 1111 0b, the 2 upper bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower bits of the slave address to the ICDRT register.
4. After confirming that the TDRE flag in ICSR2 is 1, write the data for transmission to the ICDRT register. The IIC automatically holds the SCLn line low until the data for transmission is ready, and a restart or a stop condition is issued.
5. After all bytes of data for transmission are written to the ICDRT register, wait until the value of the ICSR2.TEND flag returns to 1. Then, after checking that the ICSR2.START flag is 1, set the ICSR2.START to 0.
6. Set the ICCR2.RS bit to 1 (restart condition issue request). On receiving the request, the IIC issues a restart condition.
7. After checking that the ICSR2.START flag is 1, write the value for transmission (the slave address and the R/W# bit) to the ICDRT register.

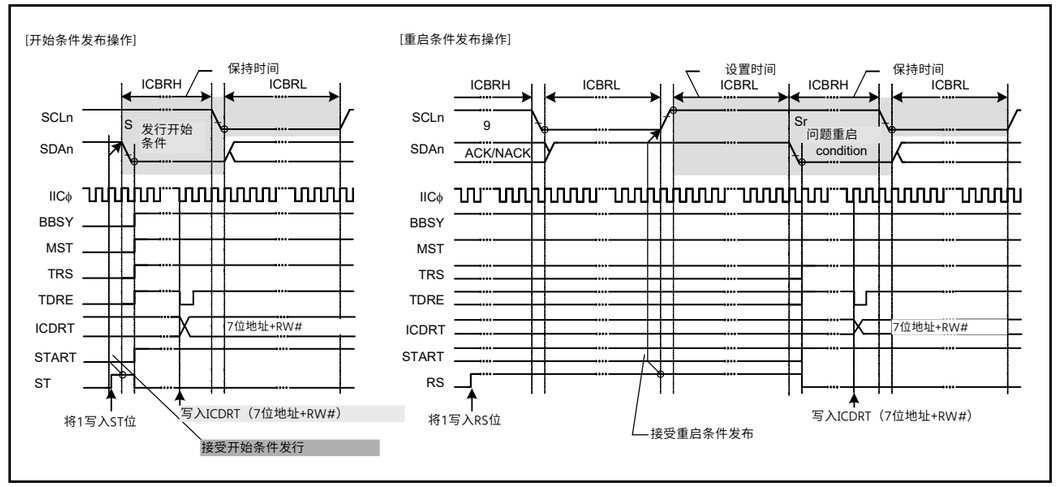


Figure 30.45 使用ST和RS位启动或重启条件发出时序

图30.46显示了在主机发送后发出重新启动条件时的操作时序。

在主传输后发出重启条件：

1. 使用第30.3.2节，初始设置中提供的详细信息初始化IIC。
2. 读取IICR2.BBSY标志以检查总线是否空闲，然后将ICCR2.ST位设置为1（启动条件请求）。收到请求后，IIC发出一个开始条件。同时，ICSR2.BBSY标志和ICSR2.START标志自动设置为1，ST位自动设置为0。如果检测到启动条件并且SDA输出状态的内部电平和SDAn线上的电平在ST位为1时匹配，则IIC识别出启动条件已按照ST位的请求成功发出。ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。当TRS位设置为1时，ICSR2中的TDRE标志也自动设置为1。
3. 检查ICSR2.TDRE标志是否为1，然后将传输值（从机地址和RW#位）写入ICDRT。发送数据写入ICDRT后，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志设置为1。发送包含从机地址和RW#位的字节后，TRS位的值会根据发送的RW#位的值自动更新以选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。如果此时ICSR2.NACKF标志位为1，表示没有从设备识别该地址或通信出现错误，向ICCR2.SP位写入1发出停止条件。

   要使用10位格式的地址传输数据，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。然后，作为第二次地址传输，将从地址的低8位写入ICDRT寄存器。
4. 确认ICSR2中的TDRE标志为1后，将要发送的数据写入ICDRT寄存器。IIC自动将SCLn线保持在低电平，直到传输数据准备好，并发出重新启动或停止条件。
5. 待发送数据的所有字节写入ICDRT寄存器后，等待ICSR2.TEND标志的值返回1。然后，在检查ICSR2.START标志为1后，将ICSR2.START设置为0。
6. 将ICCR2.RS位设置为1（重启条件发出请求）。收到请求后，IIC发出重启条件。
7. 检查ICSR2.START标志为1后，将发送值（从机地址和RW#位）写入ICDRT寄存器。

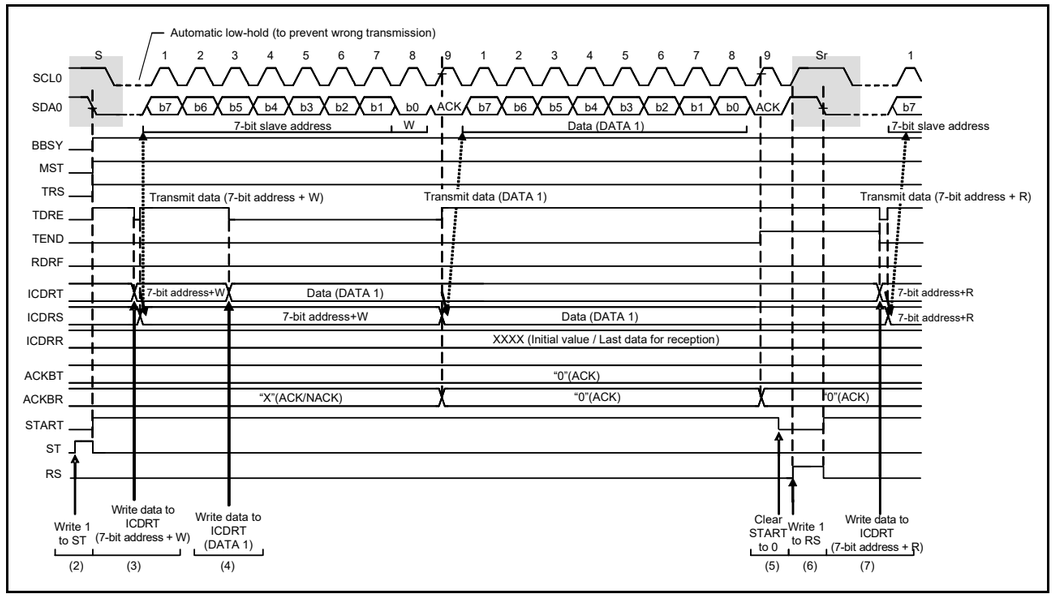


Figure 30.46 Restart condition issue timing after master transmission

30.11.3 Issuing a Stop Condition

The IIC issues a stop condition when the SP bit in ICCR2 is set to 1.

When the SP bit is set to 1, a stop condition request is made. The IIC issues a stop condition when the ICCR2.BBSY flag is 1 (bus busy state) and the ICCR2.MST bit is 1 (master mode).

To issue a stop condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure the low-level period of SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level of the SCLn line and ensure that the time set in ICBRH and the stop condition setup time elapse.
5. Release the SDAn line (low level to high level).
6. Ensure the time set in ICBRL and the bus free time elapse.
7. Clear the BBSY flag to 0 to release the bus mastership.

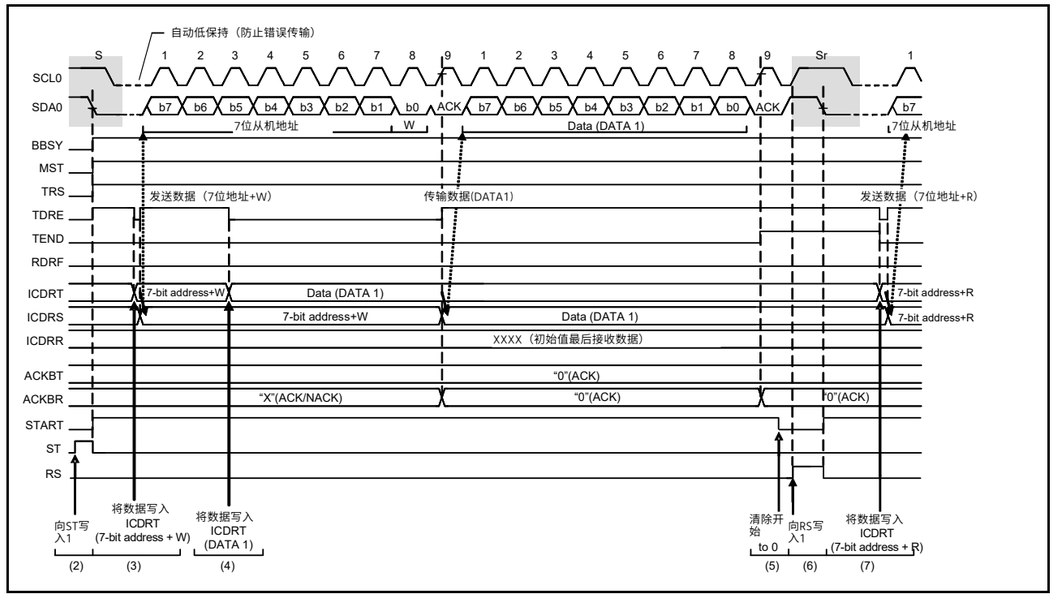


Figure 30.46 主机发送后重启条件发出时序

30.11.3 发出停止条件

当ICCR2中的SP位设置为1时，IIC发出停止条件。

当SP位设置为1时，发出停止条件请求。当ICCR2.BBSY标志为1（总线忙状态）且ICCR2.MST位为1（主机模式）时，IIC发出停止条件。

发出停止条件：

1. 将SDAn线驱动为低电平（高电平到低电平）。
2. 确保ICBRL中设置的SCLn线的低电平周期已过。
3. 释放SCLn线（低电平到高电平）。
4. 检测SCLn线的高电平并确保在ICBRH中设置的时间和停止条件设置时间已过。
5. 释放SDAn线（低电平到高电平）。
6. 确保ICBRL中设置的时间和巴士空闲时间已过。
7. 将BBSY标志清除为0以释放总线主控权。

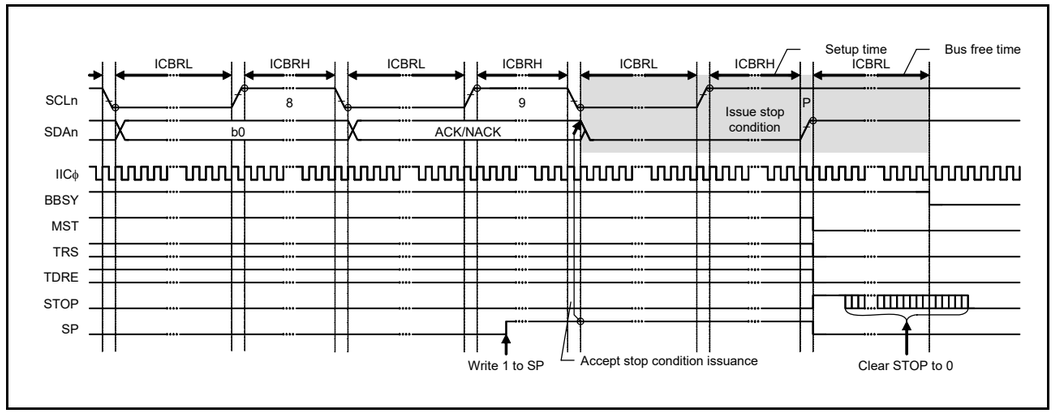


Figure 30.47 Stop condition issue timing using the SP bit

30.12 Bus Hanging

If the clock signals from the master and slave devices are out of synchronization because of noise or other factors, the I2C bus might hang with a fixed level on the SCLn line or SDAn line.

To manage bus hanging, the IIC has:

- A timeout function to detect hanging by monitoring the SCLn line
- A function for the output of an extra SCL clock cycle to release the bus from a hung state because of clock signals being out of synchronization
- The IIC reset function
- An internal reset function.

By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to determine whether the IIC or its communicating partner is placing the low level on the SCLn or SDAn lines.

30.12.1 Timeout Function

The timeout function can detect when the SCLn line is stuck longer than the predetermined time. The IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rising or falling), but continues to count unless the SCLn line changes. If the internal counter overflows because no SCLn line changes, the IIC can detect the timeout and report the bus hung state.

This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state when the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1)
- The IIC slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0)
- The bus is free (ICCR2.BBSY flag is 0) while a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function uses the internal reference clock (IICϕ) set in the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (ICMR2.TMOS = 0) or a 14-bit counter when short mode is selected (ICMR2.TMOS = 1).

The SCLn line level (low, high, or both levels) during which this counter is activated can be selected in the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter is disabled.

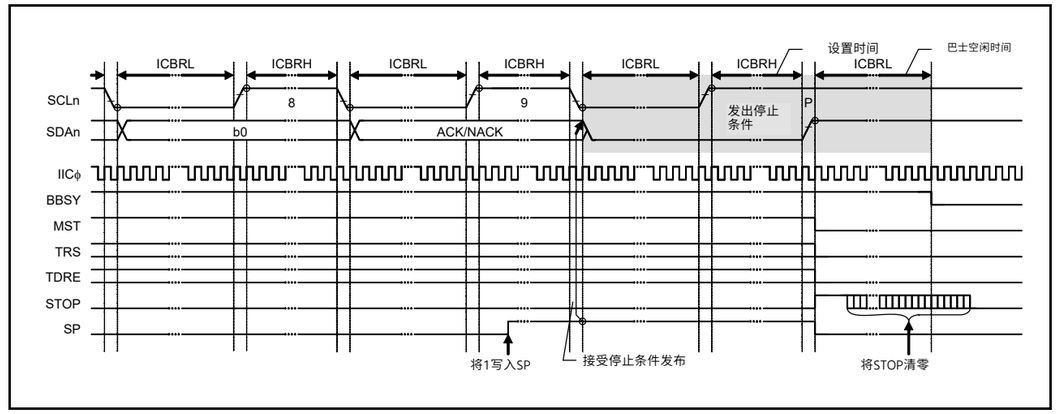


Figure 30.47 使用SP位的停止条件发出时序

30.12 巴士挂

如果来自主从设备的时钟信号由于噪声或其他因素不同步，则I2C总线可能会在SCLn线或SDAn线上以固定电平挂起。

为了管理总线挂起，IIC具有：

- 通过监控SCLn线路来检测挂起的超时功能
- 由于时钟信号不同步而输出额外SCL时钟周期以将总线从挂起状态中释放的功能
- IIC复位功能
- 内部复位功能。

通过检查ICCR1中的SCLO、SDAO、SCLI和SDAI位，可以确定IIC或其通信伙伴是否在SCLn或SDAn线上设置了低电平。

30.12.1 超时功能

超时功能可以检测SCLn线路何时卡住超过预定时间。IIC可以通过监视SCLn线在预定时间内保持低电平或高电平来检测异常总线状态。

超时功能监控SCLn线路状态并使用内部计数器计算低电平周期或高电平周期。每次SCLn线改变（上升或下降）时，超时功能都会复位内部计数器，但除非SCLn线改变，否则会继续计数。如果内部计数器因为SCLn线没有变化而溢出，IIC可以检测到超时并报告总线挂起状态。

此超时功能在ICFER.TMOE位为1时启用。在以下情况下，当SCLn线卡在低电平或高电平时，它会检测到挂起状态：

- 总线繁忙（ICCR2.BBSY标志为1）处于主模式（ICCR2.MST位为1）
- 检测到IIC从机地址（ICSR1寄存器不是00h）并且在从机模式下总线忙（ICCR2.BBSY标志为1）（ICCR2.MST位为0）
- 当请求启动条件时（ICCR2.ST位为1），总线空闲（ICCR2.BBSY标志为0）。

超时功能的内部计数器使用ICMR1的CKS[2:0]位中设置的内部参考时钟(IIC)作为计数源。Itfunctionsasa16-bitcounterwhenlongmodeisselected(ICMR2.TMOS=0)ora14-bitcounterwhenshortmodeisselected(ICMR2.TMOS=1).

可以在TMOH和
ICMR2中的TMOL位。如果TMOL和TMOH位都设置为0，则内部计数器被禁用。

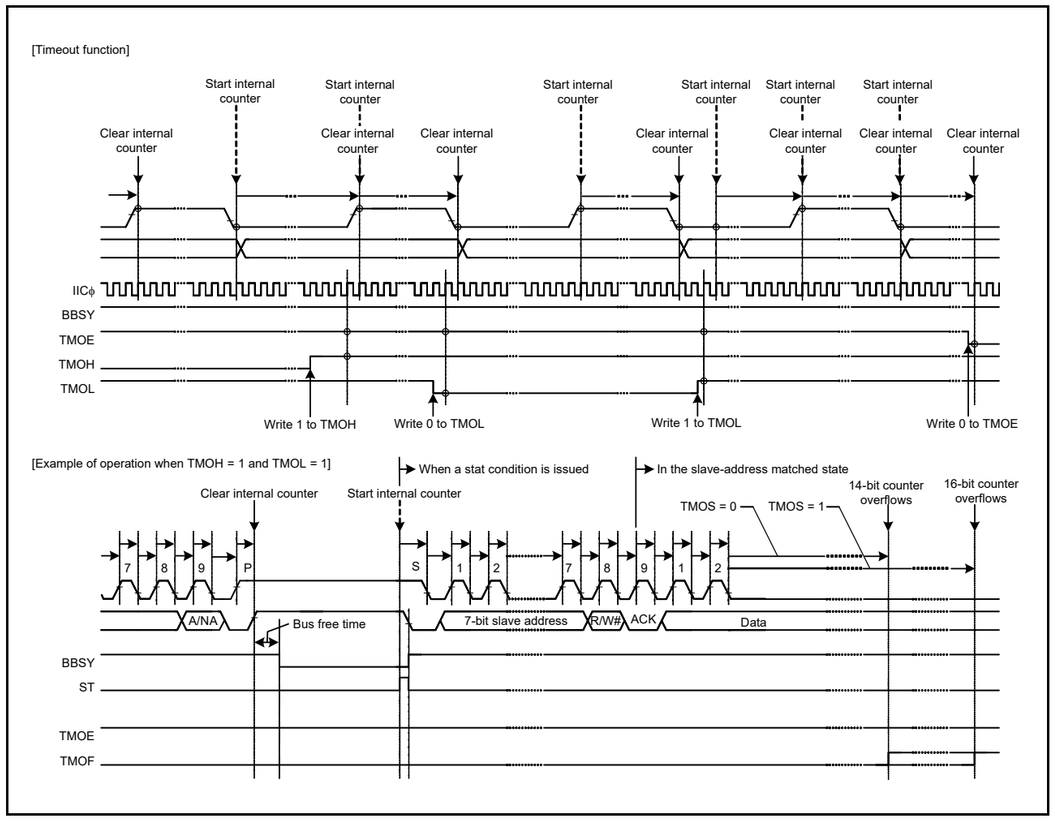


Figure 30.48 Timeout function using the TMOE, TMOS, TMOH, and TMOL bits

30.12.2 Extra SCL Clock Cycle Output Function

In master mode, this function outputs extra SCL clock cycles to release the SDAn line of the slave device from being held low because the master is out of synchronization with the slave device.

This function uses single cycles of the SCL clock for a bus error when the IIC cannot issue a stop condition because the slave device is holding the SDAn line low. Do not use this function in normal situations. Using it when communications are proceeding correctly leads to malfunctions.

When the CLO bit in the ICCR1 register is set to 1 in master mode, a single cycle of the SCL clock at the transfer rate specified in the ICMR1.CKS[2:0] bits, and in the ICBRH and ICBRL registers, is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically set to 0. Therefore, additional extra clock cycles can be output consecutively by writing 1 to the CLO bit after having read CLO = 0.

When the IIC module is in master mode and the slave device is holding the SDAn line low because synchronization with the slave device is lost because of the effects of noise, the output of a stop condition is not possible. This function can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held low, and recover the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming the release of the SDAn line by the slave device, complete communications by reissuing the stop condition.

Use this function with the MALE bit in the ICFER register set to 0 (master arbitration-lost detection disabled). If the MALE bit is set to 1 (enabled), arbitration is lost when the value of the ICCR1.SDAO bit does not match the state of the SDAn line.

[Output conditions for using the CLO bit in ICCR1]:

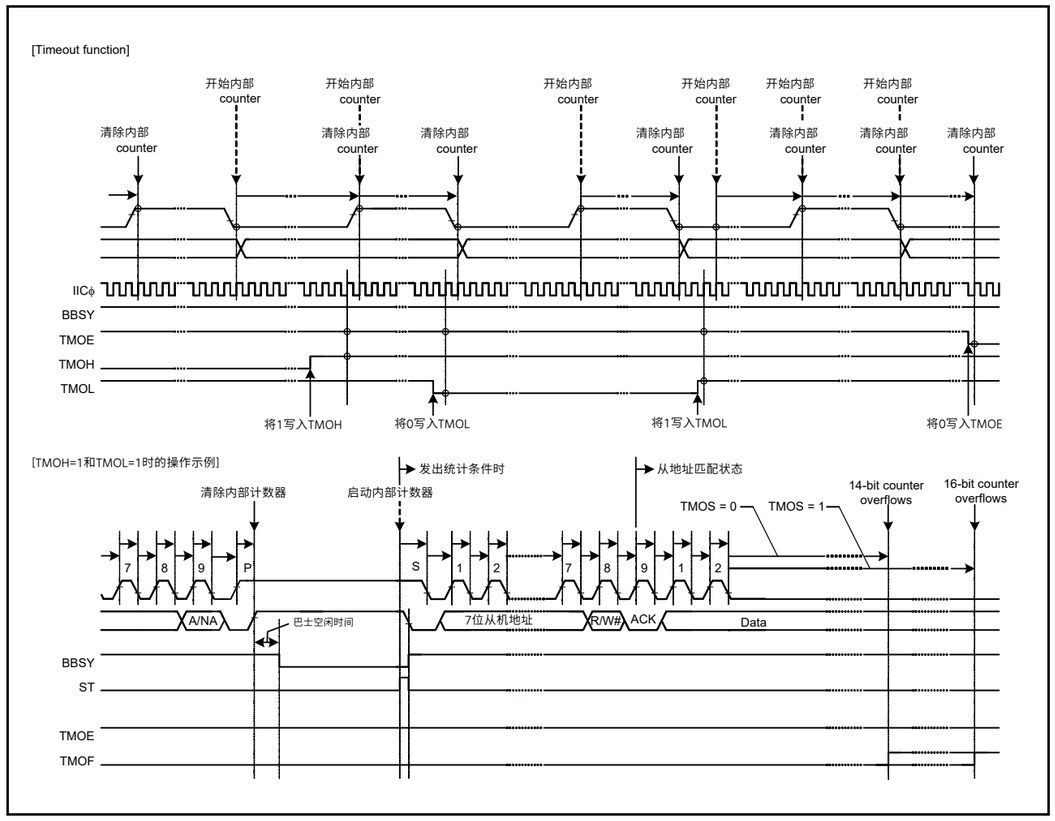


Figure 30.48 使用TMOE、TMOS、TMOH和TMOL位的超时功能

30.12.2 额外的SCL时钟周期输出功能

在主模式下，该函数输出额外的SCL时钟周期，以释放从设备的SDAn线保持低电平，因为主设备与从设备不同步。

当IIC由于从设备将SDAn线保持为低电平而无法发出停止条件时，该函数使用SCL时钟的单个周期来处理总线错误。在正常情况下不要使用此功能。在通信正常进行时使用它会导致故障。

当ICCR1寄存器中的CLO位在主机模式下设置为1时，以ICMR1.CKS[2:0]位以及ICBRH和ICBRL寄存器中指定的传输速率输出一个SCL时钟周期作为一个额外的时钟周期。在SCL时钟的这个单周期输出后，CLO位自动设置为0。因此，在读取CLO=0后，通过向CLO位写入1可以连续输出额外的时钟周期。

当IIC模块处于主模式且从设备保持SDAn线为低电平时，因为与从设备的同步由于噪声的影响而丢失，因此无法输出停止条件。该功能可用于逐个输出额外的SCL周期，使从设备解除SDAn线的低电平状态，使总线从不可用状态恢复。从设备释放SDAn线可以通过读取ICCR1中的SDAI位来监控。从设备确认SDAn线的释放后，通过重新发出停止条件完成通信。

在将ICFER寄存器中的MALE位设置为0（禁用主机仲裁丢失检测）时使用此功能。如果
MALE位设置为1（启用），当ICCR1.SDAO位的值与
SDAn line.

[使用ICCR1中CLO位的输出条件]:

- When the bus is free (ICCR2.BBSY = 0) or in master mode (ICCR2.MST = 1 and ICCR2.BBSY = 1)
- When the communication device does not hold the SCLn line low.

Figure 30.49 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

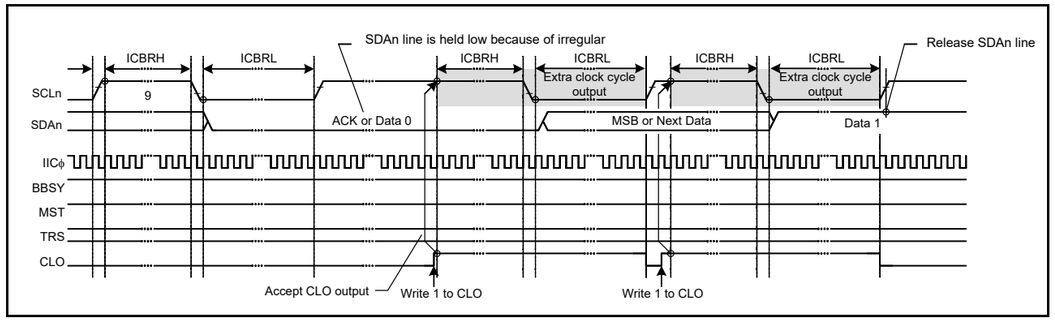


Figure 30.49 Extra SCL clock cycle output function using the CLO bit

30.12.3 IIC Reset and Internal Reset

The IIC has two types of resets:

- IIC reset, which initializes all registers, including the BBSY flag in ICCR2
- Internal reset, which releases the IIC from the slave-address matched state and initializes the internal counter while saving other settings.

After issuing a reset, be sure to set the ICCR1.IICRST bit to 0. Both types of resets are valid for release from bus-hung states, because both restore the output state of the SCLn and SDAn pins to the high-impedance state.

Issuing a reset during slave operation might lead to a loss of synchronization between the master device clock and the slave device clock, so avoid this when possible. In addition, monitoring the bus state, such as for the presence of a start condition, is not possible during an IIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the IIC and internal resets, see section 30.15, State of Registers when Issuing each Condition.

30.13 SMBus Operation

The IIC supports data communication conforming to the SMBus Specification (version 2.0). To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus standard, set the ICMR1.CKS[2:0] bits, the ICBRH, and ICBRL registers. In addition, determine the values of the ICMR2.DLCS bit and the ICMR2.SDDL[2:0] bits to meet the data hold time specification of 300 ns or more. When the IIC is used only as a slave device, the transfer rate setting is not required, but ICBRL must be set to a value longer than the data setup time of 250 ns.

For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the associated FS bit (7-bit or 10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).

When transmitting the UDID (Unique Device Identifier), set the ICFER.SALE bit to 1 to enable the slave arbitration-lost detection function.

30.13.1 SMBus Timeout Measurement

(1) Measuring slave device timeout

The following period (timeout interval: $T_{LOW: SEXT}$) must be measured for slave devices in SMBus communication:

- From start condition to stop condition.

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with

- 当总线空闲(ICCR2.BBSY=0)或处于主机模式时(ICCR2.MST=1和ICCR2.BBSY=1)
- 当通信设备不保持SCLn线为低电平时。

图30.49显示了额外SCL时钟周期输出功能（CLO位）的操作时序。

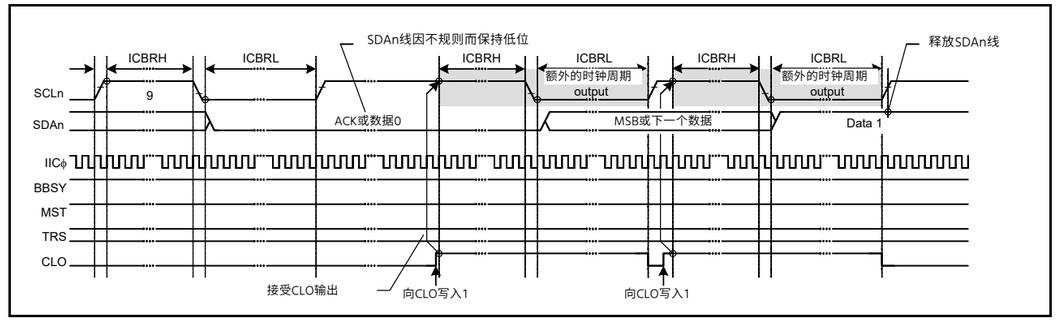


Figure 30.49 使用CLO位的额外SCL时钟周期输出功能

30.12.3 IIC复位和内部复位

IIC有两种类型的复位：

- IIC复位，初始化所有寄存器，包括ICCR2中的BBSY标志
- 内部复位，将IIC从从地址匹配状态释放并初始化内部计数器，同时保存其他设置。

发出复位后，务必将ICCR1.IICRST位设置为0。这两种复位都对从总线挂起状态释放有效，因为两者都将SCLn和SDAn引脚的输出状态恢复为高阻状态。

在从机操作期间发出复位可能会导致主设备时钟和从设备时钟之间失去同步，因此请尽可能避免这种情况。此外，在IIC复位（ICE和IICRST位=ICCR1中的01b）期间无法监控总线状态，例如是否存在启动条件。

有关IIC和内部复位的详细说明，请参阅第30.15节，发出每个寄存器时的寄存器状态
Condition.

30.13 SMBus Operation

IIC支持符合SMBus规范（2.0版）的数据通信。要执行SMBus通信，请将ICMR3中的SMBS位设置为1。要使用SMBus标准的10kbps至100kbps范围内的传输速率，请设置ICMR1.CKS[2:0]位、ICBRH和ICBRL寄存器。此外，确定ICMR2.DLCS位和ICMR2.SDDL[2:0]位的值以满足300ns或更长的数据保持时间规范。当IIC仅用作从设备时，不需要设置传输速率，但必须将ICBRL设置为大于数据设置时间250ns的值。

对于SMBus器件默认地址(1100001b)，使用从地址寄存器L0到L2之一（SARL0、SARL1和SARL2），并将SARUy(y=0to2)中的相关FS位（7位或10位地址格式选择）设置为0（7位地址格式）。

发送UDID（唯一设备标识符）时，将ICFER.SALE位设置为1，以启用从设备仲裁丢失检测功能。

30.13.1 SMBus超时测量

(1) 测量从设备超时

对于SMBus通信中的从设备，必须测量以下周期（超时间隔：TLOW:SEXT）：

- 从开始条件到停止条件。

要测量从设备的超时，请测量从开始条件检测到停止条件检测的时间段

the GPT using the IIC start condition detection interrupt (STIn) and stop condition detection interrupt (SPIn). The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW: SEXT}$: 25 ms (maximum) of the SMBus standard.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the slave device must release the bus by writing 1 to the ICCR1.IICRST to issue an internal reset of the IIC. When an internal reset is issued, the IIC stops driving the bus for the SCLn and SDAn pins and makes the SCLn/SDAn pin output high-impedance, which releases the bus.

(2) Measuring master device timeout

The following periods (timeout interval: $T_{LOW: MEXT}$) must be measured for master devices in SMBus communication:

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition.

To measure timeout for master devices, measure these periods with the GPT using the IIC start condition detection interrupt (STIn), stop condition detection interrupt (SPIn), and transmit end interrupt (IICn_TEI) or receive data full interrupt (IICn_RXI). The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard, and the total of all $T_{LOW: MEXT}$ from start condition to stop condition must be within $T_{LOW: SEXT}$: 25 ms (maximum).

For the ACK receive timing (rising edge of the 9th SCL clock cycle), monitor the ICSR2.TEND flag in master transmit mode (master transmitter) and the ICSR2.RDRF flag in master receive mode (master receiver). Perform byte-wise transmit operations in master transmit mode, and hold the ICMR3.RDRFS bit 0 until the byte immediately before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (stop writing data to the ICDRT register).

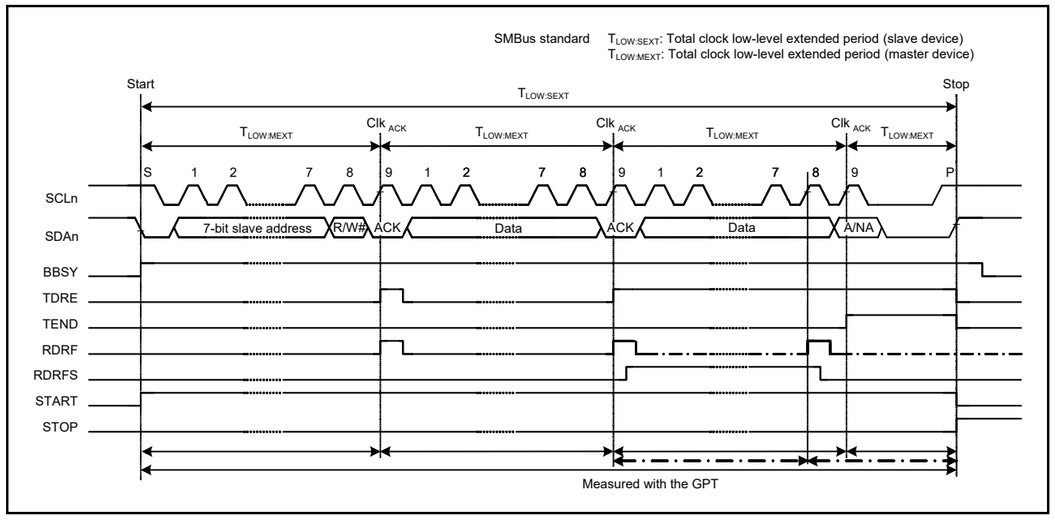


Figure 30.50 SMBus timeout measurement

30.13.2 Packet Error Code (PEC)

The MCU provides a CRC calculator that enables transmission of a Packet Error Code (PEC) or allows checking the received data in SMBus data communication. For the CRC generating polynomials of the CRC calculator, see section 33,

GPT使用IIC启动条件检测中断(STIn)和停止条件检测中断(SPIn)。测得的超时周期必须在总时钟低电平周期[从设备]TLOW:SEXT:SMBus标准的25ms（最大值）内。

如果使用GPT测量的时间超过时钟低电平检测超时TTIMEOUT:SMBus标准的25ms（最小值），从设备必须通过向ICCR1.IICRST写入1来释放总线以发出内部复位
国际集成电路。发出内部复位时，IIC停止驱动SCLn和SDAn引脚的总线并使SCLn
SDAn引脚输出高阻，从而释放总线。

(2) 测量主设备超时

对于SMBus通信中的主设备，必须测量以下周期（超时间隔：TLOW:MEXT）：

- 从开始条件到确认位
- 确认位之间
- 从确认位到停止条件。

要测量主设备的超时，请使用GPT使用IIC开始条件检测中断(STIn)、停止条件检测中断(SPIn)和发送结束中断(IICn_TEI)或接收数据完整中断(IICn_RXI)来测量这些周期。测得的超时时间必须在总时钟低电平扩展周期（主设备）TLOW:MEXT:SMBus标准的10ms（最大值）内，并且所有TLOW:MEXT从启动条件到停止条件的总和必须在TLOW内：SEXT：25毫秒（最大值）。

对于ACK接收时序（第9个SCL时钟周期的上升沿），监控主机发送模式（主机发送器）下的ICSR2.TEND标志和主机接收模式（主机接收器）下的ICSR2.RDRF标志。在主机发送模式下执行逐字节发送操作，并保持ICMR3.RDRFS位0直到在主机接收模式下接收到最后一个字节之前的字节。当RDRFS位为0时，RDRF标志在第9个SCL时钟周期的上升沿设置为1。

如果用GPT测量的周期超过总时钟低电平延长周期（主设备）TLOW:MEXT:SMBus标准的10ms（最大值）或总测量周期超过时钟低电平检测超时TTIMEOUT：SMBus标准的25ms（最小值），主设备必须通过发出停止条件来停止事务。在主机发送模式下，立即停止发送操作（停止向ICDRT寄存器写入数据）。

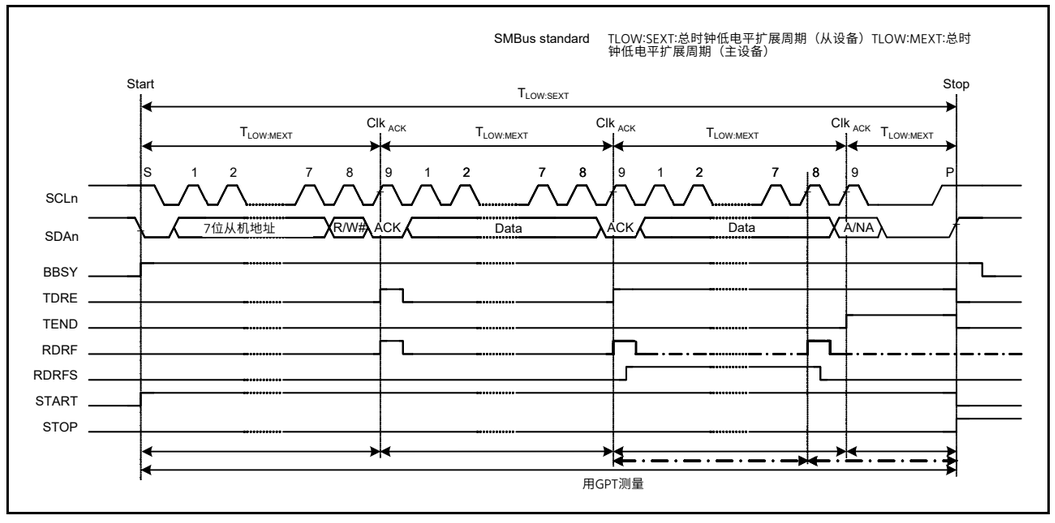


Figure 30.50 SMBus超时测量

30.13.2 数据包错误代码(PEC)

MCU提供了一个CRC计算器，可以传输数据包错误代码(PEC)或检查SMBus数据通信中接收到的数据。有关CRC计算器的CRC生成多项式，请参见第33节，

Cyclic Redundancy Check (CRC) Calculator.

The PEC data in master transmit mode can be generated by writing all transmit data to the CRC Data Input Register (CRCDIR) in the CRC calculator.

The PEC data in master receive mode can be checked by writing all receive data to the CRCDIR register in the CRC calculator and comparing the obtained value in the CRC Data Output Register (CRCDOR) with the received PEC data.

To send ACK or NACK according to the match or mismatch result when the final byte is received as a result of the PEC code check, set the ICMR3.RDRFS to 1 before the rising edge of the 8th SCL clock cycle during reception of the final byte, and hold the SCLn line low on the falling edge of the 8th clock cycle.

30.13.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address, or to request its own slave address from the SMBus host.

For a product using the MCU to operate as an SMBus host (or ARP master), the host address (0001 000b) sent from the slave device must be detected as a slave address, and so the IIC has a function for detecting the host address. To detect the host address as a slave address, set the ICMR3.SMBS bit and the ICSER.HOAE bit to 1. Operation after the host address is detected is the same as normal slave operation.

30.14 Interrupt Sources

The IIC issues five types of interrupt requests:

- Transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection)
- Receive data full
- Transmit data empty
- Transmit end
- Address match during wakeup function.

Table 30.10 lists details of the interrupt requests. The receive data full and transmit data empty conditions can activate data transfer by the DTC or DMAC.

Table 30.10 Interrupt sources

Symbol	Interrupt source	Interrupt flag	DTC activation	DMAC activation	Interrupt condition
IICn_EEI*5	Transfer error/event generation	AL	Not possible	Not possible	AL = 1, ALIE = 1
		NACKF			NACKF = 1, NAKIE = 1
		TMOF			TMOF = 1, TMOIE = 1
		START			START = 1, STIE = 1
		STOP			STOP = 1, SPIE = 1
IICn_RXI*2, *5	Receive data full	RDRF	Possible	Possible	RDRF = 1, RIE = 1
IICn_TXI*1, *5	Transmit data empty	TDRE	Possible	Possible	TDRE = 1, TIE = 1
IICn_TEI*3, *5	Transmit end	TEND	Not possible	Not possible	TEND = 1, TEIE = 1
IIC0_WUI*4	Slave address match during wakeup function	WUF	Not possible	Not possible	Slave address match Slave receive complete RWAK operation ASY0 = 1 WUIE = 1

Note: There is a delay time between the execution of a write instruction for a peripheral module by the CPU and the actual writing to the module. When an interrupt flag is cleared or masked, read the relevant flag again to check whether clearing or masking has completed, and then return from interrupt handling. Not doing so creates the possibility of repeated processing of the same interrupt.

Note 1. Because IICn_TXI is an edge-detected interrupt, it does not require clearing. Additionally, the ICSR2.TDRE flag (a condition for IICn_TXI) is automatically set to 0 when transmit data is written to the ICDRT register or a stop condition is detected

循环冗余校验(CRC)计算器。

主机发送模式下的PEC数据可以通过将所有发送数据写入CRC计算器中的CRC数据输入寄存器(CRCDIR)来生成。

主机接收模式下的PEC数据可以通过将所有接收数据写入CRC计算器中的CRCDIR寄存器并将CRC数据输出寄存器(CRCDOR)中获得的值与接收到的PEC数据进行比较来检查。

当作为PEC代码检查的结果接收到最后一个字节时，要根据匹配或不匹配结果发送ACK或NACK，请在接收最后一个字节期间的第8个SCL时钟周期的上升沿之前将ICMR3.RDRFS设置为1字节，并在第8个时钟周期的下降沿保持SCLn线为低电平。

30.13.3 SMBus主机通知协议（通知ARP主机命令）

在通过SMBus进行通信时，从设备可以临时充当主设备来通知SMBus主机（或ARP主机）自己的从地址，或从SMBus主机请求自己的从地址。

对于使用MCU作为SMBus主机（或ARP主机）的产品，从机发送的主机地址（0001000b）必须被检测为从机地址，因此IIC具有主机地址检测功能.要将主机地址检测为从机地址，请将ICMR3.SMBS位和ICSER.HOAE位设置为1。检测到主机地址后的操作与正常从机操作相同。

30.14 中断源

IIC发出五种类型的中断请求：

- 传输错误或事件生成（仲裁丢失、NACK检测、超时检测、开始条件检测和停止条件检测）
- 接收数据已满
- 传输数据为空
- 发射端
- 唤醒功能期间的地址匹配。

表30.10列出了中断请求的详细信息。接收数据满和发送数据空的情况可以激活DTC或DMAC的数据传输。

Table 30.10 中断源

Symbol	中断源	中断标志	DTC activation	DMAC activation	中断条件
IICn_EEI*5	传输错误事件生成	AL	不可能	不可能	AL = 1, ALIE = 1
		NACKF			NACKF = 1, NAKIE = 1
		TMOF			TMOF = 1, TMOIE = 1
		START			START = 1, STIE = 1
		STOP			STOP = 1, SPIE = 1
IICn_RXI*2, *5	接收数据已满	RDRF	Possible	Possible	RDRF = 1, RIE = 1
IICn_TXI*1, *5	传输数据为空	TDRE	Possible	Possible	TDRE = 1, TIE = 1
IICn_TEI*3, *5	发射端	TEND	不可能	不可能	TEND = 1, TEIE = 1
IIC0_WUI*4	唤醒功能期间的从机地址匹配	WUF	不可能	不可能	从地址匹配 从机接收完成 RWAK operation ASY0 = 1 WUIE = 1

Note: CPU对外围模块执行写指令与实际写入模块之间存在延迟时间。当一个中断标志被清除或屏蔽后，再次读取相关标志，检查清除或屏蔽是否完成，然后从中断处理返回。不这样做会产生重复处理同一中断的可能性。

Note 1. 因为IICn_TXI是边沿检测中断，所以不需要清除。此外，ICSR2.TDRE标志（用于当发送数据写入ICDRT寄存器或检测到停止条件时，IICn_TXI)自动设置为0

(ICSR2.STOP = 1).
Note 2. Because IICn_RXI is an edge-detected interrupt, it does not require clearing. Additionally, the ICSR2.RDRF flag (a condition for IICn_RXI) is automatically set to 0 when data is read from ICDRR.
Note 3. When using the IICn_TEI interrupt, clear the ICSR2.TEND flag in the IICn_TEI interrupt handling.
The ICSR2.TEND is automatically set to 0 when transmit data is written to ICDRT or a stop condition is detected (ICSR2.STOP = 1).
Note 4. Only channel 0 has a wakeup function, therefore IIC0_WUI is for channel 0 only.
Note 5. Channel number (n = 0 to 1).

Clear or mask each flag during interrupt handling.

30.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts

If the conditions for generating an IICn_TXI and IICn_RXI interrupt are satisfied while the associated IR flag is 1, the interrupt request is not output for the ICU but saved internally. One request per source can be saved internally.

An interrupt request that is saved within the ICU is output when the value of the ICU.IELSRn.IR flag becomes 0. Internally saved interrupt requests are automatically cleared under normal usage conditions. Internally saved interrupt requests can also be cleared by writing 0 to the interrupt enable bit within the associated peripheral module.

30.15 State of Registers when Issuing each Condition

The IIC has two dedicated resets, IIC reset and internal reset. Table 30.11 lists the register states when issuing each condition.

Table 30.11 State of registers when issuing each condition (1 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	Reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		Reset	Reset		
	Others			Saved		
ICCR2	BBSY	Reset	Reset	Saved	Set	Saved
	ST			Reset	Saved	Saved
	TRS, MST				Set or saved	Reset
	Others				Reset	Reset or saved
ICMR1	BC[2:0]	Reset	Reset	Reset	Reset	Saved
	Others			Saved	Saved	
ICMR2		Reset	Reset	Saved	Saved	Saved
ICMR3		Reset	Reset	Saved	Saved	Saved
ICFER		Reset	Reset	Saved	Saved	Saved
ICSER		Reset	Reset	Saved	Saved	Saved
ICIER		Reset	Reset	Saved	Saved	Saved
ICSR1		Reset	Reset	Reset	Saved	Reset
ICSR2	TDRE, TEND	Reset	Reset	Reset	Saved	Reset
	START				Set	
	STOP				Saved	Set
	Others					Saved
ICWUR		Reset	Reset	Saved	Saved	Saved
ICWUR2	WUSEN	Reset	Reset	Saved	Saved	Saved
	Others					Saved or Set or Reset
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		Reset	Reset	Saved	Saved	Saved
ICBRH, ICBRL		Reset	Reset	Saved	Saved	Saved
ICDRT		Reset	Reset	Saved	Saved	Saved

(ICSR2.STOP = 1).
Note 2. 因为IICn_RXI是边沿检测中断，所以不需要清除。此外，ICSR2.RDRF标志（用于当从ICDRR读取数据时，IICn_RXI)自动设置为0。
Note 3. 使用IICn_TEI中断时，在IICn_TEI中断处理中清除ICSR2.TEND标志。
当发送数据写入ICDRT或检测到停止条件(ICSR2.STOP=1)时，ICSR2.TEND自动设置为0。
Note 4. 只有通道0具有唤醒功能，因此IIC0_WUI仅适用于通道0。
Note 5. 通道号（n=0到1）。

在中断处理期间清除或屏蔽每个标志。

30.14.1 IICn_TXI和IICn_RXI中断的缓冲区操作

如果在相关的IR标志为1时产生IICn_TXI和IICn_RXI中断的条件得到满足，则中断请求不会输出给ICU，而是在内部保存。每个源的一个请求可以在内部保存。

当ICU.IELSRn.IR标志的值变为0时，将输出保存在ICU内的中断请求。
在正常使用条件下，内部保存的中断请求会自动清除。内部保存的中断请求也可以通过向相关外围模块中的中断使能位写入0来清除。

30.15 发布每个条件时的注册状态

IIC有两个专用复位，IIC复位和内部复位。表30.11列出了发出每个条件时的寄存器状态。

Table 30.11 发出每个条件时的寄存器状态（2个中的1个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICCR1	ICE, IICRST	Reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		Reset	Reset		
	Others			Saved		
ICCR2	BBSY	Reset	Reset	Saved	Set	Saved
	ST			Reset	Saved	Saved
	TRS, MST				设置或保存	Reset
	Others				Reset	重置或保存
ICMR1	BC[2:0]	Reset	Reset	Reset	Reset	Saved
	Others			Saved	Saved	
ICMR2		Reset	Reset	Saved	Saved	Saved
ICMR3		Reset	Reset	Saved	Saved	Saved
ICFER		Reset	Reset	Saved	Saved	Saved
ICSER		Reset	Reset	Saved	Saved	Saved
ICIER		Reset	Reset	Saved	Saved	Saved
ICSR1		Reset	Reset	Reset	Saved	Reset
ICSR2	TDRE, TEND	Reset	Reset	Reset	Saved	Reset
	START				Set	
	STOP				Saved	Set
	Others					Saved
ICWUR		Reset	Reset	Saved	Saved	Saved
ICWUR2	WUSEN	Reset	Reset	Saved	Saved	Saved
	Others					保存或设置或 Reset
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		Reset	Reset	Saved	Saved	Saved
ICBRH, ICBRL		Reset	Reset	Saved	Saved	Saved
ICDRT		Reset	Reset	Saved	Saved	Saved

Table 30.11 State of registers when issuing each condition (2 of 2)

Registers	Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICDRR	Reset	Reset	Saved	Saved	Saved
ICDRS	Reset	Reset	Reset	Saved	Saved
Timeout function	Reset	Reset	Operation	Operation	Operation
Bus free time measurement	Reset	Reset	Operation	Operation	Operation

30.16 Event Link Output

IIC0 to IIC1 handle event output for the Event Link Controller (ELC) for the following sources:

(1) Transfer error event

When a transfer error event occurs, the associated event signal can be output to another module by the ELC.

(2) Receive data full

When a receive data register becomes full, the associated event signal can be output to another module by the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the associated event signal can be output to another module by the ELC.

(4) Transmit end

On completion of transfer, the associated event signal can be output to another module by the ELC.

30.16.1 Interrupt Handling and Event Linking

Each of the IIC interrupt types (see Table 30.10) has an enable bit to control enabling and disabling of the associated interrupt signal. An interrupt request signal is output to the CPU when an interrupt source condition is satisfied while the associated enable bit is set.

The associated event link output signals are sent to other modules as event signals by the ELC when the interrupt source conditions are satisfied, regardless of the interrupt enable bit settings. For details on interrupt sources, see Table 30.10.

30.17 Usage Notes

30.17.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable IIC operation. The module is initially stopped after a reset. The registers become accessible on release from the module-stop state.

For details on Module Stop Control Register B, see section 11, Low Power Modes.

30.17.2 Notes on Starting Transfer

If the IR flag associated with the IIC interrupt is 1 when transfer is started (ICCR1.ICE = 1), use the following procedure to clear interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unexpected behavior of the IR flag.

Before starting transfer operation:

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits, such as ICIER.TIE to 0.
3. Read the relevant interrupt enable bits, such as ICIER.TIE, and confirm that the value is 0.
4. Set the IR flag to 0.

Table 30.11 发出每个条件时的寄存器状态（2个中的2个）

Registers	Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICDRR	Reset	Reset	Saved	Saved	Saved
ICDRS	Reset	Reset	Reset	Saved	Saved
超时功能	Reset	Reset	Operation	Operation	Operation
公交车空闲时间测量	Reset	Reset	Operation	Operation	Operation

30.16 事件链接输出

IIC0到IIC1为以下源处理事件链接控制器(ELC)的事件输出：

(1) 传输错误事件

当发生传输错误事件时，ELC可以将相关事件信号输出到另一个模块。

(2) 接收数据已满

当接收数据寄存器变满时，ELC可以将相关的事件信号输出到另一个模块。

(3) 传输数据为空

当发送数据寄存器变为空时，ELC可以将相关的事件信号输出到另一个模块。

(4) 发射端

传输完成后，ELC可以将相关的事件信号输出到另一个模块。

30.16.1 中断处理和事件链接

每种IIC中断类型（见表30.10）都有一个启用位来控制相关中断信号的启用和禁用。当相关的使能位设置时，中断源条件成立时，将向CPU输出中断请求信号。

当满足中断源条件时，ELC将关联的事件链接输出信号作为事件信号发送到其他模块，而不管中断使能位设置如何。有关中断源的详细信息，请参见表30.10。

30.17 使用说明

30.17.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用IIC操作。模块在复位后最初停止。寄存器在从模块停止状态释放时变得可访问。

有关模块停止控制寄存器B的详细信息，请参见第11节，低功耗模式。

30.17.2 开始转移注意事项

如果在传输开始时与IIC中断相关的IR标志为1(ICCR1.ICE=1)，请使用以下程序在使能操作之前清除中断。在ICCR1.ICE位为1时将IR标志设置为1开始传输会导致在传输开始后内部保存中断请求，这可能导致IR标志的意外行为。

在开始传输操作之前：

1.确认ICCR1.ICE位为0。

2.设置相关的中断使能位，如ICIER.TIE为0。

3、读取相关的中断使能位，如ICIER.TIE，确认值为0。

4.将IR标志设置为0。

31. Controller Area Network (CAN) Module

31.1 Overview

The CAN module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver.

Table 31.1 lists the features of the CAN module and Figure 31.1 shows a block diagram.

Table 31.1 CAN module specifications (1 of 2)

Parameter	Description
Data transfer rate	• ISO11898-1 compliant for standard and extended frames
Bit rate	• Programmable up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes, with two selectable mailbox modes: • Normal mode: 32 mailboxes independently configurable for transmission or reception • FIFO mode: 24 mailboxes independently configurable for transmission or reception, with remaining mailboxes used for receive and transmit 4-stage FIFOs.
Reception	• Support for data frame and remote frame reception • Reception ID format selectable to only standard ID, only extended ID, or mixed IDs • Programmable one-shot reception function • Selectable between overwrite mode (unread message overwritten) and overrun mode (unread message saved) • Reception complete interrupt independently enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • Masks independently enabled or disabled for each mailbox.
Transmission	• Support for data frame and remote frame transmission • Transmission ID format selectable to only standard ID, only extended ID, or mixed IDs • Programmable one-shot transmission function • Broadcast messaging function • Priority mode selectable based on message ID or mailbox number • Support for transmission request abort, with abort completion confirmable in status flag • Transmission complete interrupt independently enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state selectable to: • ISO11898-1 specification compliant • Automatic invoking of CAN halt mode on bus-off entry • Automatic invoking of CAN halt mode on bus-off end • Invoking of CAN halt mode through software • Transition to error-active state through software.
Error status monitoring	• Monitoring of CAN bus errors, including stuff error, form error, ACK error, 15-bit CRC error, bit error, and ACK delimiter error • Detection of transition to error states including error-warning, error-passive, bus-off entry, and bus-off recovery • Support for reading of error counters.
Time stamping	• Time stamp function using a 16-bit counter • Reference clock selectable from 1-bit, 2-bit, 4-bit and 8-bit time periods.
Interrupt function	Support for five interrupt sources: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error interrupts.
CAN sleep mode	• CAN clock stopped to reduce power consumption

31. 控制器局域网(CAN)模块

31.1 Overview

CAN模块使用基于消息的协议在电磁噪声应用中的多个从机和主机之间接收和传输数据。该模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。CAN模块需要额外的外部CAN收发器。

表31.1列出了CAN模块的特性，图31.1显示了框图。

Table 31.1 CAN模块规格(1of2)

Parameter	Description
数据传输率	符合ISO11898-1标准和扩展框架
比特率	可编程高达1Mbps(fCAN 8MHz)fCAN：CAN时钟源
消息框	32个邮箱，有两种可选邮箱模式： 普通模式：32个邮箱可独立配置用于发送或接收 FIFO模式：24个邮箱可独立配置用于发送或接收，其余邮箱用于接收和发送4级FIFO。
Reception	支持数据帧和远程帧接收 接收ID格式可选择仅标准ID、仅扩展ID或混合ID 可编程一次性接收功能可选择覆盖模式（未读消息覆盖）和溢出模式（未读消息已保存）） 为每个邮箱独立启用或禁用接收完成中断。
验收过滤器	八个接受掩码（每四个邮箱一个掩码） 每个邮箱独立启用或禁用掩码。
Transmission	支持数据帧和远程帧传输 传输ID格式可选择仅标准ID、仅扩展ID或混合ID 可编程一次性传输功能 广播消息功能 基于消息ID或邮箱号选择优先模式 支持对于传输请求中止，在状态标志中可确认中止完成 为每个邮箱独立启用或禁用传输完成中断。
总线关闭恢复的模式转换	从总线关闭状态恢复的模式转换可选择： 符合ISO11898-1规范 在总线关闭进入时自动调用CAN暂停模式 在总线关闭结束时自动调用CAN暂停模式 调用CAN暂停模式通过软件 通过软件转换到错误激活状态。
错误状态监控	监控CAN总线错误，包括填充错误、格式错误、ACK错误、15位CRC错误、位错误和ACK分隔符错误 检测到错误状态的转换，包括错误警告、错误被动、总线关闭进入 和总线关闭恢复 支持读取错误计数器。
时间戳	使用16位计数器的时间戳功能 可从1位、2位、4位和8位时间周期中选择参考时钟。
中断功能	支持五个中断源： 接收完成 发送完成 接收FIFO 发送FIFO 错误中断。
CAN睡眠模式	CAN时钟停止以降低功耗

Table 31.1 CAN module specifications (2 of 2)

Parameter	Description
Software support unit	Three software support units: • Acceptance filter support • Mailbox search support, including receive mailbox search, transmit mailbox search, and message lost search • Channel search support.
CAN clock source	PCLKB or CANMCLK
Test mode	Three test modes available for evaluation purposes: • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback).
Module-stop function	Module-stop state can be set to reduce power consumption

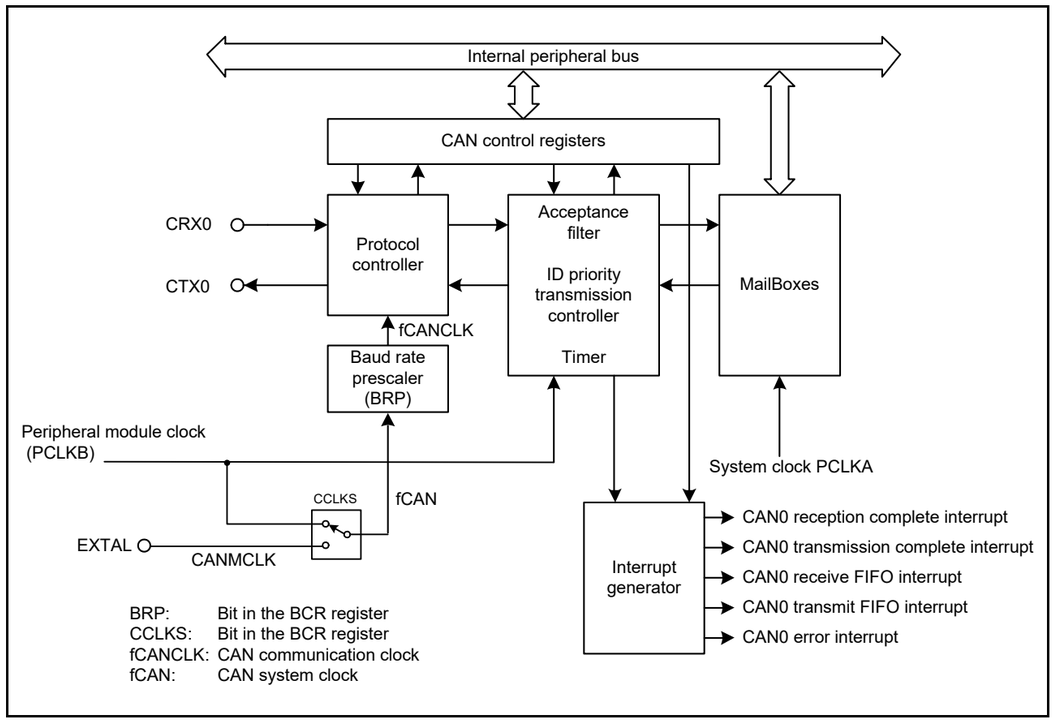


Figure 31.1 CAN module block diagram

The CAN module constitutes the following blocks:

- CAN input and output pins
  CRX0 and CTX0
- Protocol controller
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling
- Mailboxes
  Consists of 32 mailboxes, which can be configured as either transmit or receive. Each mailbox has an individual ID, data length code (DLC), a data field (8 bytes), and a time stamp.
- Acceptance filter
  Filters received messages using MKR0 to MKR7 register settings.
- Timer

Table 31.1 CAN模块规格（2个中的2个）

Parameter	Description
软件支持单位	三个软件支持单元： 接受过滤器支持 邮箱搜索支持，包括接收邮箱搜索、发送邮箱搜索和邮件丢失搜索 渠道搜索支持。
CAN时钟源	PCLKB or CANMCLK
测试模式	三种测试模式可用于评估目的： 只听模式 自测模式0 （外部环回） 自测模式1（内部环回）。
Module-stop function	可设置模块停止状态以降低功耗

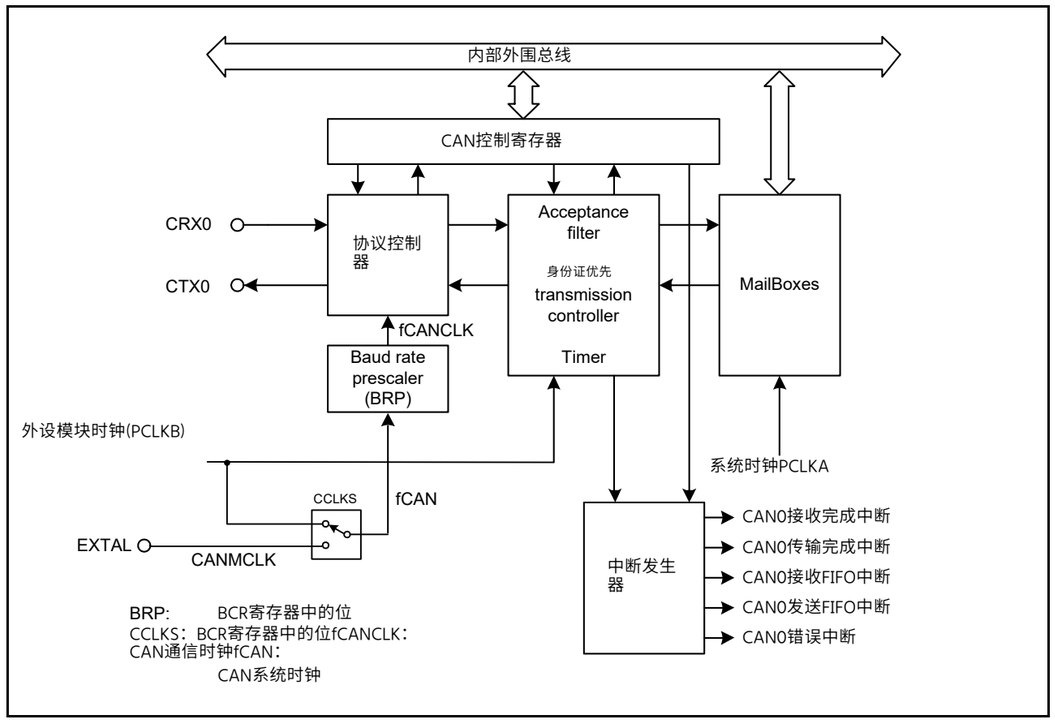


Figure 31.1 CAN模块框图

CAN模块由以下模块组成：

- CAN输入和输出引脚
  CRX0 and CTX0
- 协议控制器
  处理CAN协议处理，例如总线仲裁、发送和接收时的位时序、填充和错误处理
- Mailboxes
  包含32个邮箱，可配置为发送或接收。每个邮箱都有一个单独的ID、数据长度代码(DLC)、一个数据字段（8个字节）和一个时间戳。
- 验收过滤器
  使用MKR0到MKR7寄存器设置过滤接收到的消息。
- Timer

Used for the time stamp function. The timer value when a message is stored in the mailbox is written as the time stamp value.

- Interrupt generator for five types of interrupts:
  - CAN0 reception complete interrupt
  - CAN0 transmission complete interrupt
  - CAN0 receive FIFO interrupt
  - CAN0 transmit FIFO interrupt
  - CAN0 error interrupt.

Table 31.2 lists the CAN module pins. These pins are multiplexed with other signals on the MCU. For details, see section 20, I/O Ports.

Table 31.2 Pin configuration

Pin name	I/O	Function
CRX0	Input	Data receive pin
CTX0	Output	Data transmit pin

31.2 Register Descriptions

31.2.1 Control Register (CTLR)

Address(es): CAN0.CTLR 4005 0840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MBM	CAN Mailbox Mode Select*1	0: Normal mailbox mode 1: FIFO mailbox mode.	R/W
b2, b1	IDFM[1:0]	ID Format Mode Select *1	b2 b1 0 0: Standard ID mode: All mailboxes, including FIFO mailboxes, handle only standard IDs 0 1: Extended ID mode: All mailboxes, including FIFO mailboxes, handle only extended IDs 1 0: Mixed ID mode: All mailboxes, including FIFO mailboxes, handle both standard IDs and extended IDs. In normal mailbox mode, use the associated IDE bit to differentiate standard or extended IDs. In FIFO mailbox mode, the associated IDE bit are used for mailboxes 0 to 23, the IDE bits in FIDCR0 and FIDCR1 are used for the receive FIFO, and the IDE bit in mailbox 24 is used for the transmit FIFO. 1 1: Setting prohibited.	R/W
b3	MLM	Message Lost Mode Select*1	0: Overwrite mode 1: Overrun mode.	R/W
b4	TPM	Transmission Priority Mode Select*1	0: ID priority transmit mode 1: Mailbox number priority transmit mode.	R/W
b5	TSRC	Time Stamp Counter Reset Command*4	0: Do not reset time stamp counter 1: Reset time stamp counter.*3	R/W

用于时间戳功能。将消息存储在邮箱中时的计时器值作为时间戳值写入。

- 用于五种类型中断的中断发生器：
  - CAN0接收完成中断
  - CAN0传输完成中断
  - CAN0接收FIFO中断
  - CAN0发送FIFO中断
  - CAN0错误中断。

表31.2列出了CAN模块引脚。这些引脚与MCU上的其他信号复用。有关详细信息，请参阅第20节，IO端口。

Table 31.2 引脚配置

引脚名称	I/O	Function
CRX0	Input	数据接收引脚
CTX0	Output	数据传输引脚

31.2 注册说明

31.2.1 控制寄存器(CTLR)

Address(es): CAN0.CTLR 4005 0840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
重置后的值:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MBM	CAN邮箱模式 Select*1	0：普通邮箱模式1：FIF O邮箱模式。	R/W
b2, b1	IDFM[1:0]	ID格式模式选择*1	b2b100：标准ID模式： 所有邮箱，包括FIFO邮箱，只处理标准ID01：扩展ID模式： 所有邮箱，包括FIFO邮箱，只处理扩展ID10：混合ID模式： 所有邮箱，包括FIFO邮箱，都处理标准ID和扩展ID。在普通邮箱模式下，使用相关的IDE位来区分标准ID或扩展ID。在FIFO邮箱模式下，相关的IDE位用于邮箱0到23，FIDCR0和FIDCR1中的IDE位用于接收FIFO，邮箱24中的IDE位用于发送FIFO。11：禁止设置。	R/W
b3	MLM	消息丢失模式 Select*1	0：覆盖模式1： 溢出模式。	R/W
b4	TPM	传输优先级 Mode Select*1	0：ID优先发送模式1：邮箱号码优先发送模式。	R/W
b5	TSRC	时间戳计数器 Reset Command*4	0：不重置时间戳计数器1：重置时间戳计数器。*3	R/W

Bit	Symbol	Bit name	Description	R/W
b7, b6	TSPS[1:0]	Time Stamp Prescaler Select*1	b7 b6 0 0: Every 1-bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time.	R/W
b9, b8	CANM[1:0]	CAN Mode of Operation Select*5	b9 b8 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: CAN reset mode (forced transition).	R/W
b10	SLPM	CAN Sleep Mode*5, *6	0: Exit CAN sleep mode 1: Enter CAN sleep mode.	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12 b11 0 0: Normal mode (ISO11898-1 specification compliant) 0 1: Entry to CAN halt mode automatic on entering bus-off state 1 0: Entry to CAN halt mode automatic at the end of bus-off state 1 1: Entry to CAN halt mode during bus-off recovery period through software request.	R/W
b13	RBOC	Forcible Return from Bus-Off*2	0: No return occurred 1: Forced return from bus-off.*3	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Write to the BOM[1:0], TSPS[1:0], TPM, MLM, IDFM[1:0], and MBM bits in CAN reset mode.
Note 2. Set the RBOC bit to 1 in the bus-off state.
Note 3. This bit is automatically set to 0 after being set to 1. It should be read as 0.
Note 4. Set the TSRC bit to 1 in CAN operation mode.
Note 5. When the CANM[1:0] and SLPM bits are changed, check STR to ensure that the mode is switched. Do not change the CANM[1:0] bits or SLPM bit until the mode is switched.
Note 6. Write to the SLPM bit in CAN reset mode or CAN halt mode. When changing the SLPM bit, write 0 or 1 only to the SLPM bit.

MBM bit (CAN Mailbox Mode Select)

When the MBM bit is 0 (normal mailbox mode), mailboxes 0 to 31 are configured as transmit or receive mailboxes.

When the MBM bit is 1 (FIFO mailbox mode):

- Mailboxes 0 to 23 are configured as transmit or receive mailboxes
- Mailboxes 24 to 27 are configured as a transmit FIFO
- Mailboxes 28 to 31 are configured as a receive FIFO
- Transmit data is written into mailbox 24, the window mailbox for the transmit FIFO
- Receive data is read from mailbox 28, the window mailbox for the receive FIFO.

Table 31.3 lists the mailbox configuration.

IDFM[1:0] bits (ID Format Mode Select)

The IDFM[1:0] bits specify the ID format.

MLM bit (Message Lost Mode Select)

The MLM bit specifies the operation when a new message is captured in an unread mailbox. Overwrite mode or overrun mode can be selected. All mailboxes, including the receive FIFO are set to either overwrite mode or overrun mode.

When this bit is 0, all mailboxes are set to overwrite mode. Any new message received overwrites the pre-existing message.

When this bit is 1, all mailboxes are set to overrun mode. Any new message received does not overwrite the pre-existing message, and the new message and is discarded.

TPM bit (Transmission Priority Mode Select)

The TPM bit specifies the priority when transmitting messages.

The ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

Bit	Symbol	位名称	Description	R/W
b7, b6	TSPS[1:0]	时间戳预分频器 Select*1	b7b600：每1位时间0 1：每2位时间10：每 4位时间11：每8位时 间。	R/W
b9, b8	CANM[1:0]	CAN模式 Operation Select*5	b9b800：CAN操作模式01：CAN复位模 式10：CAN暂停模式11：CAN复位模式 （强制转换）。	R/W
b10	SLPM	CAN睡眠模式*5 *6	0：退出CAN睡眠模式1： 进入CAN睡眠模式。	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12b1100：正常模式（符合ISO11898-1规范）01：进入总线关闭状态 时自动进入CAN停止模式10：在总线关闭状态结束时自动进入CAN停止模 式11：进入在总线关闭恢复期间通过软件请求到CAN暂停模式。	R/W
b13	RBOC	强行返回 Bus-Off*2	0：未发生返回1：从总线关闭 强制返回。*3	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在CAN复位模式下写入BOM[1:0]、TSPS[1:0]、TPM、MLM、IDFM[1:0]和MBM位。
Note 2. 在总线关闭状态下将RBOC位设置为1。
Note 3. 该位设置为1后自动设置为0，应读为0。
Note 4. 在CAN操作模式下将TSRC位设置为1。
Note 5. 当CANM[1:0]和SLPM位改变时，检查STR以确保模式切换。不要改变 CANM[1:0]位或SLPM位，直到模式切换。
Note 6. 在CAN复位模式或CAN暂停模式下写入SLPM位。更改SLPM位时，仅向SLPM位写入0或1。

MBM位（CAN邮箱模式选择）

当MBM位为0（正常邮箱模式）时，邮箱0到31被配置为发送或接收邮箱。

当MBM位为1（FIFO邮箱模式）时：

- 邮箱0到23被配置为发送或接收邮箱
- 邮箱24到27被配置为发送FIFO
- 邮箱28到31配置为接收FIFO
- 发送数据写入邮箱24，发送FIFO的窗口邮箱
- 接收数据从邮箱28中读取，该邮箱是接收FIFO的窗口邮箱。

表31.3列出了邮箱配置。

IDFM[1:0]位（ID格式模式选择）

IDFM[1:0]位指定ID格式。

MLM位（消息丢失模式选择）

MLM位指定在未读邮箱中捕获新消息时的操作。可以选择覆盖模式或溢出模式。所有邮箱，包括接收FIFO都设置为覆盖模式或溢出模式。

当该位为0时，所有邮箱都设置为覆盖模式。收到的任何新消息都会覆盖先前存在的消息。

当该位为1时，所有邮箱都设置为溢出模式。收到的任何新消息都不会覆盖先前存在的消息，并且新消息会被丢弃。

TPM位（传输优先模式选择）

TPM位指定传输消息时的优先级。

可选择ID优先传送模式或信箱号码传送模式。所有信箱都设置为ID优先传输或信箱号码优先传输。

When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO11898-1 CAN specification. In ID priority transmit mode, mailboxes 0 to 31 (in normal mailbox mode), mailboxes 0 to 23 (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a FIFO message is currently being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (0 to 23).

TSRC bit (Time Stamp Counter Reset Command)

The TSRC bit resets the time stamp counter. When this bit is set to 1, the TSR register is set to 0000h. This bit is automatically set to 0.

TSPS[1:0] bits (Time Stamp Prescaler Select)

The TSPS[1:0] bits select the prescaler for the time stamp. The reference clock for the time stamp can be selected to either 1-bit, 2-bit, 4-bit, or 8-bit time periods.

CANM[1:0] bits (CAN Mode of Operation Select)

The CANM[1:0] bits select one of the following modes for the CAN module:

- CAN operation mode
- CAN reset mode
- CAN halt mode.

The CAN sleep mode is set by the SLPM bit. For details, see section 31.3, Modes of Operation. When the CAN module enters CAN halt mode based on the BOM[1:0] bits setting, the CANM[1:0] bits are automatically set to 10b.

SLPM bit (CAN Sleep Mode)

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode. When the SLPM bit is set to 0, the CAN module exits CAN sleep mode. For details, see section 31.3, Modes of Operation.

BOM[1:0] bits (Bus-Off Recovery Mode)

The BOM[1:0] bits select bus-off recovery mode for the CAN module.

When the BOM[1:0] bits are 00b, the recovery from bus-off is compliant with the ISO11898-1 CAN specification. The CAN module recovers CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.

When the BOM[1:0] bits are 01b and the CAN module reaches the bus-off state, the CANM[1:0] bits in the CTLR register are set to 10b to enter the CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off, and the TECR and RECR registers are set to 00h.

When the BOM[1:0] bits are 10b, the CANM[1:0] bits are set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters the CAN halt mode after a recovery from the bus-off state, that is, after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off, and the TECR and RECR registers are set to 00h.

When the BOM[1:0] bits are 11b, the CAN module enters the CAN halt mode by setting the CANM[1:0] bits to 10b while the CAN module is still in the bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and TECR and RECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM[1:0] bits are set to 10b, a bus-off recovery interrupt request is generated.

If the CPU requests an entry to the CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM[1:0] bits are 01b, or at bus-off end when the BOM[1:0] bits are 10b), then the

当TPM位为0时，选择ID优先传输模式，传输优先级符合ISO11898-1CAN规范中定义的CAN总线仲裁规则。在ID优先传输模式下，邮箱0到31（在正常邮箱模式下）、邮箱0到23（在FIFO邮箱模式下）和传输FIFO将针对配置为传输的邮箱ID进行比较。如果两个或多个邮箱ID相同，则编号较小的邮箱优先级较高。

只有从发送FIFO发送的下一条消息包含在发送仲裁中。如果当前正在发送FIFO消息，则发送FIFO中的下一个未决消息将包含在发送仲裁中。

当TPM位为1时，选择邮箱号发送模式，邮箱号最小的发送邮箱优先级最高。在FIFO邮箱模式下，发送FIFO的优先级低于普通邮箱（0到23）。

TSRC位（时间戳计数器复位命令）

TSRC位复位时间戳计数器。当该位设置为1时，TSR寄存器设置为0000h。该位自动设置为0。

TSPS[1:0]位（时间戳预分频器选择）

TSPS[1:0]位选择时间戳的预分频器。时间戳的参考时钟可以选择为1位、2位、4位或8位时间段。

CANM[1:0]位（CAN操作模式选择）

CANM[1:0]位为CAN模块选择以下模式之一：

- CAN操作模式
- CAN复位模式
- CAN暂停模式。

CAN睡眠模式由SLPM位设置。有关详细信息，请参阅第31.3节，操作模式。当CAN模块根据BOM[1:0]位设置进入CAN暂停模式时，CANM[1:0]位自动设置为10b。

SLPM位（CAN休眠模式）

当SLPM位设置为1时，CAN模块进入CAN睡眠模式。当SLPM位设置为0时，CAN模块退出CAN睡眠模式。有关详细信息，请参阅第31.3节，操作模式。

BOM[1:0]位（总线关闭恢复模式）

BOM[1:0]位选择CAN模块的总线关闭恢复模式。

当BOM[1:0]位为00b时，总线关闭恢复符合ISO11898-1CAN规范。CAN模块在检测到11个连续隐性位128次后恢复CAN通信（错误激活状态）。
从总线关闭恢复时会产生一个总线关闭恢复中断请求。

当BOM[1:0]位为01b且CAN模块达到总线关闭状态时，CTLR寄存器中的CANM[1:0]位设置为10b以进入CAN暂停模式。总线关闭恢复时不产生总线关闭恢复中断请求，TECR和RECR寄存器设置为00h。

当BOM[1:0]位为10b时，CAN模块一到达总线关闭状态，CANM[1:0]位就会设置为10b。CAN模块从总线关闭状态恢复后，即检测到连续11个隐性位128次后，进入CAN停止模式。从总线关闭恢复时产生一个总线关闭恢复中断请求，并将TECR和RECR寄存器设置为00h。

当BOM[1:0]位为11b时，CAN模块通过将CANM[1:0]位设置为10b进入CAN停止模式，同时CAN模块仍处于总线关闭状态。从总线关闭恢复时不产生总线关闭恢复中断请求，并且TECR和RECR设置为00h。但是，如果CAN模块在CANM[1:0]位设置为10b之前128次检测到11个连续隐性位后从总线关闭中恢复，则会产生总线关闭恢复中断请求。

如果CPU在CAN模块尝试进入CAN暂停模式的同时请求进入CAN复位模式（当BOM[1:0]位为01b时在总线关闭进入，或在总线关闭结束时BOM[1:0]位为10b），则

CPU request has higher priority.

RBOC bit (Forcible Return from Bus-Off)

When the RBOC bit is set to 1 in the bus-off state, the CAN module forcibly exits the bus-off state. This bit is automatically set to 0, and the error state changes from bus-off to error-active. When the RBOC bit is set to 1, the RECR and TECR registers are set to 00h and the BOST bit in the STR register is set to 0, indicating that the CAN module is not in bus-off state. The other registers remain unchanged even when the RBOC bit is set to 1. No bus-off recovery interrupt request is generated by this recovery from the bus-off state. Use the RBOC bit only when the BOM[1:0] bits are 00b (normal mode).

Table 31.3 Mailbox configuration

Mailbox	MBM bit = 0 (normal mailbox mode)	MBM bit = 1*1 to *5 (FIFO mailbox mode)
Mailboxes 0 to 23	Normal mailbox	Normal mailbox
Mailboxes 24 to 27		Transmit FIFO
Mailboxes 28 to 31		Receive FIFO

Note 1. The transmit FIFO is controlled by the TFCR register. The MCTL_TXj registers associated with mailboxes 24 to 27 are disabled. MCTL_TX24 to MCTL_TX27 cannot be used by the transmit FIFO.
Note 2. The receive FIFO is controlled by the RFCR register. The MCTL_RXj registers associated with mailboxes 28 to 31 are disabled. MCTL_RX28 to MCTL_RX31 cannot be used by the receive FIFO.
Note 3. See the MIER_FIFO register for information on FIFO interrupts.
Note 4. The MKIVLR register bits associated with mailboxes 24 to 31 are disabled. Set these bits to 0.
Note 5. The transmit and receive FIFOs can be used for both data and remote frames.

31.2.2 Bit Configuration Register (BCR)

Address(es): CAN0.BCR 4005 0844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—	—	BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CCLKS	CAN Clock Source Selection	0: PCLKB (generated by the PLL clock) 1: CANMCLK (generated by the main clock).	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	TSEG2[2:0]	Time Segment 2 Control	b10 b8 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	SJW[1:0]	Synchronization Jump Width Control	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq.	R/W

CPU请求具有更高的优先级。

RBOC位（从总线关闭强制返回）

当RBOC位在总线关闭状态下设置为1时，CAN模块强制退出总线关闭状态。该位自动设置为0，错误状态从总线关闭变为错误激活。当RBOC位设置为1时，RECR和TECR寄存器设置为00h，STR寄存器中的BOST位设置为0，表示CAN模块不处于总线关闭状态。即使RBOC位设置为1，其他寄存器也保持不变。从总线关闭状态恢复不会产生总线关闭恢复中断请求。仅当BOM[1:0]位为00b（正常模式）时才使用RBOC位。

Table 31.3 邮箱配置

Mailbox	MBM位=0（正常邮箱模式）	MBM位=1*1到*5（FIFO邮箱模式）
邮箱0到23	普通邮箱	普通邮箱
邮箱24至27		Transmit FIFO
邮箱28至31		Receive FIFO

Note 1. 发送FIFO由TFCR寄存器控制。与邮箱24到27关联的MCTL_TXj寄存器被禁用。发送FIFO不能使用MCTL_TX24到MCTL_TX27。
Note 2. 接收FIFO由RFCR寄存器控制。与邮箱28到31关联的MCTL_RXj寄存器被禁用。MCTL_RX28到MCTL_RX31不能被接收FIFO使用。
Note 3. 有关FIFO中断的信息，请参见MIER_FIFO寄存器。
Note 4. 与邮箱24到31相关的MKIVLR寄存器位被禁用。将这些位设置为0。
Note 5. 发送和接收FIFO可用于数据帧和远程帧。

31.2.2 位配置寄存器(BCR)

Address(es): CAN0.BCR 4005 0844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—	—	BRP[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CCLKS	CAN时钟源选择	0：PCLKB（由PLL时钟产生）1：CANMCLK（由主时钟产生）。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10 to b8	TSEG2[2:0]	时间段2控制	b10b8000：禁止设置001：2Tq010：3Tq011：4Tq100：5Tq101：6Tq110：7Tq111：8Tq.	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b13, b12	SJW[1:0]	同步跳转宽度 Control	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq.	R/W

Bit	Symbol	Bit name	Description	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25 to b16	BRP[9:0]	Baud Rate Prescaler select*1	These bits set the frequency of the CAN communication clock (fCANCLK)	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b28	TSEG1[3:0]	Time Segment 1 Control	b31 b28 0 0 0 0: Setting prohibited 0 0 0 1: Setting prohibited 0 0 1 0: Setting prohibited 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq.	R/W

Tq: Time Quantum

Note 1. Do not select a value less than 1 when the SCKSCR.CKSEL[2:0] bits are 011b (selecting the main clock oscillator).

For details about setting the bit timing, see section 31.4, Data Transfer Rate Configuration. Set the BCR register before entering CAN halt mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode. A 32-bit read/write access must be performed carefully so as not to change bits 0 to 7.

CCLKS bit (CAN Clock Source Selection)

When the CCLKS bit is 0, the peripheral module clock (PCLKB) produced by the PLL frequency synthesizer is used as the CAN clock source (fCAN). When the CCLKS bit is 1, CANMCLK produced externally by the EXTAL pins is used as the CAN clock source (fCAN).

TSEG2[2:0] bits (Time Segment 2 Control)

The TSEG2[2:0] bits specify the length of the phase buffer segment 2 (PHASE_SEG2) with a Tq value. A value from 2 to 8 Tq can be set. Set a value smaller than that of the TSEG1[3:0] bits.

SJW[1:0] bits (Synchronization Jump Width Control)

The SJW[1:0] bits specify the synchronization jump width with a Tq value. A value from 1 to 4 Tq can be set. Set a value smaller than or equal to that of the TSEG2[2:0] bits.

BRP[9:0] bits (Baud Rate Prescaler select)

The BRP[9:0] bits set the frequency of the CAN communication clock (fCANCLK). The fCANCLK cycle is 1 Tq. If the setting is P (0 to 1,023), the baud rate prescaler divides fCAN by P + 1.

TSEG1[3:0] bits (Time Segment 1 Control)

The TSEG1[3:0] bits specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with a time quantum (Tq) value. A value from 4 to 16 Tq can be set.

Bit	Symbol	位名称	Description	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25 to b16	BRP[9:0]	Baud Rate Prescaler select*1	这些位设置CAN通信时钟(fCANCLK)的频率	R/W
b27, b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b28	TSEG1[3:0]	时间段1控制	b31b280000：禁止设置000 1：禁止设置0010：禁止设 置0011：4Tq0100：5Tq01 01：6Tq0110：7Tq0111： 8Tq1000：9Tq1001：10Tq 1010：11Tq1011：12Tq11 00：13Tq1101：14Tq1110 ：15Tq1111：16Tq。	R/W

Tq：时间量子

Note 1. 当SCKSCR.CKSEL[2:0]位为011b（选择主时钟振荡器）时，不要选择小于1的值。

有关设置位时序的详细信息，请参见第31.4节，数据传输速率配置。在从CAN复位模式进入CAN停止模式或CAN操作模式之前设置BCR寄存器。设置一次后，可在CAN复位模式或CAN暂停模式下写入该寄存器。必须小心执行32位读写访问，以免更改位0到7。

CCLKS位（CAN时钟源选择）

当CCLKS位为0时，PLL频率合成器产生的外设模块时钟（PCLKB）用作CAN时钟源（fCAN）。当CCLKS位为1时，由EXTAL引脚从外部产生的CANMCLK用作CAN时钟源(fCAN)。

TSEG2[2:0]位（时间段2控制）

TSEG2[2:0]位用Tq值指定相位缓冲段2(PHASE_SEG2)的长度。可以设置2到8Tq的值。设置一个小于TSEG1[3:0]位的值。

SJW[1:0]位（同步跳转宽度控制）

SJW[1:0]位用Tq值指定同步跳转宽度。可以设置1到4Tq的值。设置小于或等于TSEG2[2:0]位的值。

BRP[9:0]位（波特率预分频器选择）

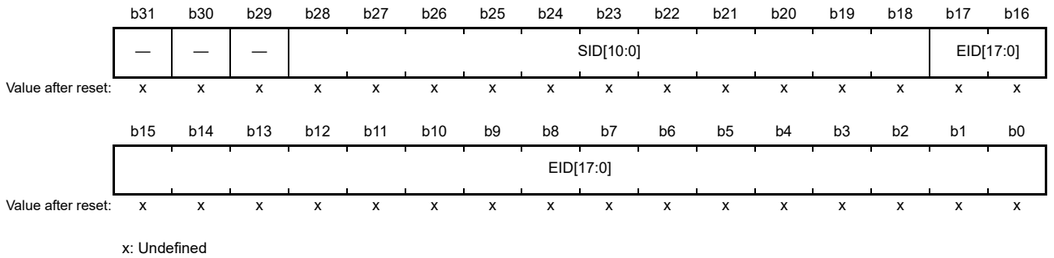
BRP[9:0]位设置CAN通信时钟(fCANCLK)的频率。fCANCLK周期为1Tq。如果设置为P（0到1 023），则波特率预分频器将fCAN除以P+1。

TSEG1[3:0]位（时间段1控制）

TSEG1[3:0]位用时间量(Tq)值指定传播时间段(PROP_SEG)和相位缓冲段1(PHASE_SEG1)的总长度。可以设置4到16Tq的值。

31.2.3 Mask Register k (MKRk) (k = 0 to 7)

Address(es): CAN0.MKR0 4005 0400h to CAN0.MKR7 4005 041Ch



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	0: Do not compare associated EID[17:0] bit 1: Compare associated EID[17:0] bit.	R/W
b28 to b18	SID[10:0]	Standard ID	0: Do not compare associated SID[10:0] bit 1: Compare associated SID[10:0] bit.	R/W
b31 to b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W

For the mask function in FIFO mailbox mode, see section 31.6, Acceptance Filtering and Masking Functions.

Write to MKR0 to MKR7 registers in CAN reset mode or CAN halt mode.

EID[17:0] bits (Extended ID)

The EID[17:0] bits are the filter mask bits associated with the CAN extended ID bits. These bits are used to receive extended ID messages. When an EID[17:0] bit is set to 0, the respective received ID bit is not compared with the associated mailbox ID bit. When an EID[17:0] bit is set to 1, the respective received ID bit is compared with the associated mailbox ID bit.

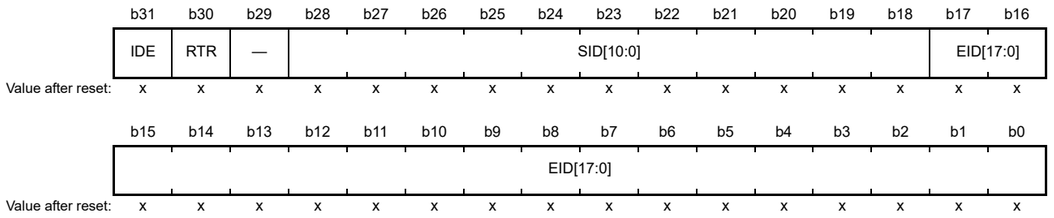
SID[10:0] bits (Standard ID)

The SID[10:0] bits are the filter mask bits associated with the CAN standard ID bits. These bits are used to receive both standard ID and extended ID messages.

When an SID[10:0] bits is set to 0, the respective received ID is not compared with the associated mailbox ID bit. When an SID[10:0] bit is set to 1, the respective received ID is compared with the associated mailbox ID bit.

31.2.4 FIFO Received ID Compare Registers 0 and 1 (FIDCR0 and FIDCR1)

Address(es): CAN0.FIDCR0 4005 0420h, CAN0.FIDCR1 4005 0424h

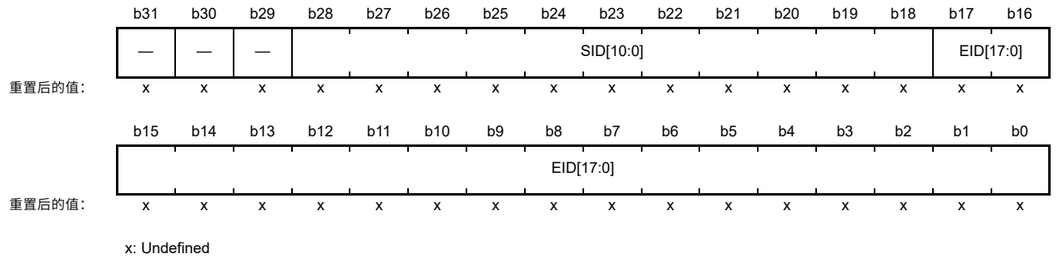


x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	Extended ID of the data and remote frames	R/W

31.2.3 屏蔽寄存器k(MKRk)(k=0到7)

Address(es): CAN0.MKR0 4005 0400h to CAN0.MKR7 4005 041Ch



x: Undefined

Bit	Symbol	位名称	Description	R/W
b17 to b0	EID[17:0]	扩展ID	0：不比较关联的EID[17:0]位1：比较关联的EID[17:0]位。	R/W
b28 to b18	SID[10:0]	标准标识	0：不比较关联的SID[10:0]位1：比较关联的SID[10:0]位。	R/W
b31 to b29	—	Reserved	读取值未定义。写入值应为0。	R/W

对于FIFO邮箱模式下的屏蔽功能，请参见第31.6节，接受过滤和屏蔽功能。

在CAN复位模式或CAN暂停模式下写入MKR0至MKR7寄存器。

EID[17:0]位（扩展ID）

EID[17:0]位是与CAN扩展ID位相关的过滤器掩码位。这些位用于接收扩展ID消息。当EID[17:0]位设置为0时，相应接收的ID位不与相关邮箱ID位进行比较。当EID[17:0]位设置为1时，将接收到的相应ID位与相关邮箱ID位进行比较。

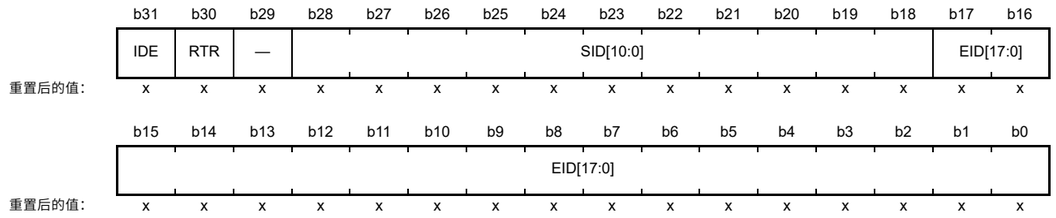
SID[10:0]位（标准ID）

SID[10:0]位是与CAN标准ID位相关的过滤器掩码位。这些位用于接收标准ID和扩展ID消息。

当SID[10:0]位设置为0时，相应接收到的ID不与相关邮箱ID位进行比较。当SID[10:0]位设置为1时，将接收到的相应ID与相关邮箱ID位进行比较。

31.2.4 FIFO接收ID比较寄存器0和1（FIDCR0和FIDCR1）

Address(es): CAN0.FIDCR0 4005 0420h, CAN0.FIDCR1 4005 0424h



x: Undefined

Bit	Symbol	位名称	Description	R/W
b17 to b0	EID[17:0]	扩展ID	数据和远程帧的扩展ID	R/W

Bit	Symbol	Bit name	Description	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of the data and remote frames	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*1	0: Standard ID 1: Extended ID.	R/W

Note 1. When the CTLR.IDFM[1:0] bits are any value other than 10b, the IDE bit should be written with 0 and read as 0.

The FIDCR0 and FIDCR1 registers are enabled when the MBM bit in the CTLR register is set to 1 (FIFO mailbox mode). In FIFO mailbox mode, the EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 are disabled. Write to the FIDCR0 and FIDCR1 registers in CAN reset mode or CAN halt mode. For information on using the FIDCR0 and FIDCR1 registers, see section 31.6, Acceptance Filtering and Masking Functions.

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data and remote frames. These bits are used to receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames. These bits are used to receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the specified frame format of data frames or remote frames:

- When the RTR bits in both FIDCR0 and FIDCR1 registers are set to 0, only data frames can be received
- When the RTR bits in both FIDCR0 and FIDCR1 registers are set to 1, only remote frames can be received
- When the RTR bits in both FIDCR0 and FIDCR1 registers are set to different values, both data frames and remote frames can be received.

IDE bit (ID Extension)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode):

- When the IDE bits in both the FIDCR0 and FIDCR1 registers are set to 0, only standard ID frames can be received
- When the IDE bits in both the FIDCR0 and FIDCR1 registers are set to 1, only extended ID frames can be received
- When the IDE bits in both the FIDCR0 and FIDCR1 registers are set to different values, both standard ID and extended ID frames can be received.

Bit	Symbol	位名称	Description	R/W
b28 to b18	SID[10:0]	标准标识	数据和远程帧的标准ID	R/W
b29	—	Reserved	读取值未定义。写入值应为0。	R/W
b30	RTR	远程传输 Request	0：数据帧1：远程帧。	R/W
b31	IDE	身份扩展 *1	0：标准ID1：扩展ID。	R/W

Note 1. 当CTLR.IDFM[1:0]位为10b以外的任何值时，IDE位应写为0，读为0。

当CTLR寄存器中的MBM位设置为1（FIFO邮箱模式）时，FIDCR0和FIDCR1寄存器被使能。在FIFO邮箱模式下，邮箱28到邮箱31中的EID[17:0]、SID[10:0]、RTR和IDE位被禁用。在CAN复位模式或CAN暂停模式下写入FIDCR0和FIDCR1寄存器。有关使用

FIDCR0和FIDCR1寄存器，请参见第31.6节，验收过滤和屏蔽功能。

EID[17:0]位（扩展ID）

EID[17:0]位设置数据和远程帧的扩展ID。这些位用于接收扩展ID消息。

SID[10:0]位（标准ID）

SID[10:0]位设置数据帧和远程帧的标准ID。这些位用于接收标准ID和扩展ID消息。

RTR位（远程传输请求）

RTR位设置数据帧或远程帧的指定帧格式：

- 当FIDCR0和FIDCR1寄存器中的RTR位都设置为0时，只能接收数据帧
- 当FIDCR0和FIDCR1寄存器中的RTR位都设置为1时，只能接收远程帧
- 当FIDCR0和FIDCR1寄存器中的RTR位设置为不同的值时，可以接收数据帧和远程帧。

IDE位（ID扩展）

IDE位将ID格式设置为标准ID或扩展ID。当CTLR中的IDFM[1:0]位为10b（混合ID模式）时，IDE位被使能：

- 当FIDCR0和FIDCR1寄存器中的IDE位都设置为0时，只能接收标准ID帧
- 当FIDCR0和FIDCR1寄存器中的IDE位都设置为1时，只能接收扩展ID帧
- 当FIDCR0和FIDCR1寄存器中的IDE位设置为不同的值时，可以接收标准ID和扩展ID帧。

31.2.5 Mask Invalid Register (MKIVLR)

Address(es): CAN0.MKIVLR 4005 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Mask Invalid	0: Mask valid 1: Mask invalid.	R/W

Each bit in the MKIVLR register is associated with a mailbox of the same number. Bit [0] in the MKIVLR register corresponds to mailbox 0 (MB0) and bit [31] corresponds to mailbox 31 (MB31).*1

Note 1. Set bits [31:24] to 0 in FIFO mailbox mode.

When an MBn bit is set to 1, the corresponding acceptance mask register becomes invalid for the associated mailbox. When an MBn bit is set to 1, a message is received by the associated mailbox only if the receive message ID exactly matches the mailbox ID. Write to the MKIVLR register in CAN reset mode or CAN halt mode.

31.2.6 Mailbox Register j (MBj_ID, MBj_DL, MBj_Dm, MBj_TS) (j = 0 to 31, m = 0 to 7)

Table 31.4 lists the CAN0 mailbox memory mapping, and Table 31.5 lists the CAN data frame configuration. The value of the CAN0 mailbox is undefined after reset.

Write to the MBj_ID, MBj_DL, MBj_Dm and MBj_TS registers only when the related MCTL_TXj or MCTL_RXj (j = 0 to 31) register is 00h and the associated mailbox does not process an abort request. See Table 31.4 for details on register addresses.

Table 31.4 CAN0 mailbox memory mapping (1 of 2)

Address for CAN0	Mapped message content
4005 0200h + 16 × j + 0	IDE, RTR, SID10 to SID6
4005 0200h + 16 × j + 1	SID5 to SID0, EID17, EID16
4005 0200h + 16 × j + 2	EID15 to EID8
4005 0200h + 16 × j + 3	EID7 to EID0
4005 0200h + 16 × j + 4	—
4005 0200h + 16 × j + 5	Data length code (DLC[3:0])
4005 0200h + 16 × j + 6	Data byte 0
4005 0200h + 16 × j + 7	Data byte 1
4005 0200h + 16 × j + 8	Data byte 2
4005 0200h + 16 × j + 9	Data byte 3
4005 0200h + 16 × j + 10	Data byte 4
4005 0200h + 16 × j + 11	Data byte 5
4005 0200h + 16 × j + 12	Data byte 6

31.2.5 屏蔽无效寄存器(MKIVLR)

Address(es): CAN0.MKIVLR 4005 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MB31 to MB0	掩码无效	0：屏蔽有效1 ：屏蔽无效。	R/W

MKIVLR寄存器中的每一位都与一个相同编号的邮箱相关联。MKIVLR寄存器中的位[0]对应邮箱0(MB0)，位[31]对应邮箱31(MB31)。*1

Note 1. 在FIFO邮箱模式下将位[31:24]设置为0。

当MBn位设置为1时，相应的接受屏蔽寄存器对相关邮箱无效。当MBn位设置为1时，只有当接收消息ID与邮箱ID完全匹配时，相关邮箱才会接收消息。在CAN复位模式或CAN暂停模式下写入MKIVLR寄存器。

31.2.6 邮箱寄存器j(MBj_ID MBj_DL MBj_Dm MBj_TS)(j=0到31 m=0到7)

表31.4列出了CAN0邮箱内存映射，表31.5列出了CAN数据帧配置。复位后CAN0邮箱的值未定义。

仅当相关的MCTL_TXj或MCTL_RXj（j=0到31）寄存器为00h且相关邮箱不处理中止请求时，才写入MBj_ID、MBj_DL、MBj_Dm和MBj_TS寄存器。有关寄存器地址的详细信息，请参见表31.4。

Table 31.4 CAN0邮箱内存映射（1of2）

CAN0的地址	映射的消息内容
4005 0200h + 16 × j + 0	IDE、RTR、SID10到SID6
4005 0200h + 16 × j + 1	SID5 to SID0, EID17, EID16
4005 0200h + 16 × j + 2	EID15 to EID8
4005 0200h + 16 × j + 3	EID7 to EID0
4005 0200h + 16 × j + 4	—
4005 0200h + 16 × j + 5	数据长度码（DLC[3:0]）
4005 0200h + 16 × j + 6	数据字节0
4005 0200h + 16 × j + 7	数据字节1
4005 0200h + 16 × j + 8	数据字节2
4005 0200h + 16 × j + 9	数据字节3
4005 0200h + 16 × j + 10	数据字节4
4005 0200h + 16 × j + 11	数据字节5
4005 0200h + 16 × j + 12	数据字节6

Table 31.4 CAN0 mailbox memory mapping (2 of 2)

Address for CAN0	Mapped message content
4005 0200h + 16 × j + 13	Data byte 7
4005 0200h + 16 × j + 14	Time stamp upper byte
4005 0200h + 16 × j + 15	Time stamp lower byte

Table 31.5 CAN data frame configuration

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC1	DATA0	DATA1	…	DATA7

The previous value of each mailbox is saved unless a new message is received.

Address(es): CAN0.MB0_ID 4005 0200h to CAN0.MB31_ID 4005 03F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID*1	Extended ID of the data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of the data and remote frames	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*2	0: Standard ID 1: Extended ID.	R/W

Note 1. If the mailbox receives a standard ID message, the EID bits in the mailbox are undefined.
Note 2. The IDE bit is enabled when the IDFM[1:0] bits in the CTLR register are 10b (mixed ID mode). When the IDFM[1:0] bits are any value other than 10b, the IDE bit should be written with 0 and read as 0.

Address(es): CAN0.MB0_DL 4005 0204h to CAN0.MB31_DL 4005 03F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Table 31.4 CAN0邮箱内存映射（2个中的2个）

CAN0的地址	映射的消息内容
4005 0200h + 16 × j + 13	数据字节7
4005 0200h + 16 × j + 14	时间戳高字节
4005 0200h + 16 × j + 15	时间戳低字节

Table 31.5 CAN数据帧配置

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC1	DATA0	DATA1	…	DATA7

除非收到新邮件，否则会保存每个邮箱的先前值。

Address(es): CAN0.MB0_ID 4005 0200h to CAN0.MB31_ID 4005 03F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称		Description	R/W
b17 to b0	EID[17:0]	扩展ID	*1	数据和远程帧的扩展ID	R/W
b28 to b18	SID[10:0]	标准标识		数据和远程帧的标准ID	R/W
b29	—	Reserved		读取值未定义。写入值应为0。	R/W
b30	RTR	远程传输请求		0：数据帧1：远程帧。	R/W
b31	IDE	身份扩展	*2	0：标准ID1：扩展ID。	R/W

Note 1. 如果邮箱收到标准ID消息，则邮箱中的EID位未定义。
Note 2. 当CTLR寄存器中的IDFM[1:0]位为10b（混合ID模式）时，IDE位被使能。当IDFM[1:0]位为10b以外的任何值时，IDE位应写为0，读为0。

Address(es): CAN0.MB0_DL 4005 0204h to CAN0.MB31_DL 4005 03F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	DLC[3:0]	Data Length Code*1	b3 b0 0 0 0 0: Data length = 0 byte 0 0 0 1: Data length = 1 byte 0 0 1 0: Data length = 2 bytes 0 0 1 1: Data length = 3 bytes 0 1 0 0: Data length = 4 bytes 0 1 0 1: Data length = 5 bytes 0 1 1 0: Data length = 6 bytes 0 1 1 1: Data length = 7 bytes 1 x x x: Data length = 8 bytes.	R/W
b15 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

x: Don't care

Note 1. If the mailbox receives a message with data length (set in DLC[3:0]) of n bytes, where n is less than 8, the data in the DATAn to DATA7 registers in the mailbox is undefined. DATA0 to DATA7 are data registers for this mailbox. For example, if data length is 6 bytes (DLC[3:0] = 6h), the data in DATA6 and DATA7 registers is undefined.

Address(es): CAN0.MB0_D0 4005 0206h to CAN0.MB31_D0 4005 03F6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA0							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D1 4005 0207h to CAN0.MB31_D1 4005 03F7h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA1							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D2 4005 0208h to CAN0.MB31_D2 4005 03F8h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA2							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D3 4005 0209h to CAN0.MB31_D3 4005 03F9h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA3							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D4 4005 020Ah to CAN0.MB31_D4 4005 03FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA4							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D5 4005 020Bh to CAN0.MB31_D5 4005 03FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA5							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	位名称	Description	R/W
b3 to b0	DLC[3:0]	数据长度代码 *1	b3b00000：数据长度=0字节0 001：数据长度=1字节0010： 数据长度=2字节0011：数据长 度=3字节0100：数据长度=4 字节0101：数据长度=5字节0 110：数据长度=6字节0111： 数据长度=7字节1xxx：数据长 度=8字节。	R/W
b15 to b4	—	Reserved	读取值未定义。写入值应为0。	R/W

x：不关心注

1。 如果邮箱接收到数据长度（在DLC[3:0]中设置）为n字节的消息，其中n小于8，则邮箱中DATAn到DATA7寄存器中的数据未定义。DATA0到DATA7是该邮箱的数据寄存器。例如，如果数据长度为6字节（DLC[3:0]=6h），则DATA6和DATA7寄存器中的数据未定义。

Address(es): CAN0.MB0_D0 4005 0206h to CAN0.MB31_D0 4005 03F6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA0							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D1 4005 0207h to CAN0.MB31_D1 4005 03F7h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA1							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D2 4005 0208h to CAN0.MB31_D2 4005 03F8h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA2							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D3 4005 0209h to CAN0.MB31_D3 4005 03F9h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA3							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D4 4005 020Ah to CAN0.MB31_D4 4005 03FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA4							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D5 4005 020Bh to CAN0.MB31_D5 4005 03FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA5							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D6 4005 020Ch to CAN0.MB31_D6 4005 03FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA6							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D7 4005 020Dh to CAN0.MB31_D7 4005 03FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA7							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DATA0 to DATA7	Data Bytes 0 to 7*1,*2	DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB-first, and transmission or reception starts from bit [7].	R/W

Note 1. If the mailbox receives a message with n bytes, where n is less than 8 bytes, the DATAn to DATA7 values in the mailbox are undefined. For example, if the received data length is 6 bytes, the values of DATA6 and DATA7 are undefined.
Note 2. If the mailbox receives a remote frame, the previous values of DATA0 to DATA7 in the mailbox are saved.

Address(es): CAN0.MB0_TS 4005 020Eh to CAN0.MB31_TS 4005 03FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSH[7:0]								TSL[7:0]							
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSL[7:0]	Time Stamp Lower Byte	Bits TSH[7:0] and TSL[7:0] store the counter value of the time stamp when received messages are stored in the mailbox.	R/W
b15 to b8	TSH[7:0]	Time Stamp Higher Byte		R/W

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data and remote frames. These bits transmit or receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data and remote frames. These bits transmit or receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames:

- The receive mailbox only receives frames with the format specified in the RTR bit
- The transmit mailbox only transmits frames with the format specified in the RTR bit
- The receive FIFO mailbox receives the data frame, remote frame, or both frames specified in the RTR bit in the FIDCR0 and FIDCR1 registers
- The transmit FIFO mailbox transmits the data frame or remote frame specified in the RTR bit in the relevant transmit message.

Address(es): CAN0.MB0_D6 4005 020Ch to CAN0.MB31_D6 4005 03FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA6							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D7 4005 020Dh to CAN0.MB31_D7 4005 03FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA7							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	DATA0 to DATA7	数据字节0到7*1 *2	DATA0到DATA7存储发送或接收的CAN报文数据。发送或接收从DATA0开始。CAN总线上的位顺序是MSB优先，发送或接收从位[7]开始。	R/W

Note 1. 如果邮箱收到n字节的消息，其中n小于8字节，则邮箱中的DATAn到DATA7值未定义。例如，如果接收到的数据长度为6字节，则DATA6和DATA7的值是未定义的。
Note 2. 如果邮箱接收到远程帧，则邮箱中DATA0到DATA7的先前值被保存。

Address(es): CAN0.MB0_TS 4005 020Eh to CAN0.MB31_TS 4005 03FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSH[7:0]								TSL[7:0]							
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	TSL[7:0]	时间戳低字节	位TSH[7:0]和TSL[7:0]存储收到的消息存储在邮箱中时的时间戳的计数器值。	R/W
b15 to b8	TSH[7:0]	时间戳高字节		R/W

EID[17:0]位（扩展ID）

EID[17:0]位设置数据和远程帧的扩展ID。这些位发送或接收扩展ID消息。

SID[10:0]位（标准ID）

SID[10:0]位设置数据和远程帧的标准ID。这些位发送或接收标准ID和扩展ID消息。

RTR位（远程传输请求）

RTR位将帧格式设置为数据帧或远程帧：

- 接收邮箱只接收RTR位指定格式的帧
- 发送邮箱仅发送RTR位中指定格式的帧
- 接收FIFO邮箱接收数据帧，远程帧，或在RTR位中指定的两个帧FIDCR0和FIDCR1寄存器
- 发送FIFO邮箱发送相关发送报文中RTR位中指定的数据帧或远程帧。

IDE bit (ID Extension)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in the CTLR register are 10b (mixed ID mode):

- The receive mailbox receives only the ID format specified in the IDE bit
- The transmit mailbox transmits with the ID format specified in the IDE bit
- The receive FIFO mailbox receives messages with the standard ID and extended ID settings specified in the IDE bit in the FIDCR0 and FIDCR1 registers
- The transmit FIFO mailbox transmits messages with the standard ID or extended ID settings specified in the IDE bit in the transmit message.

DLC[3:0] bits (Data Length Code)

The DLC[3:0] bits specify the data length to be transmitted in data frames. When a remote frame is used to request data, this field specifies the requested data length.

When a data frame is received, the received data length is stored in this field. When a remote frame is received, this field stores the requested data length.

31.2.7 Mailbox Interrupt Enable Register (MIER)

Address(es): CAN0.MIER 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled. Bit [31] is associated with mailbox 31 (MB31) and bit [0] with mailbox 0 (MB0).	R/W

The MIER register allows independent enabling of interrupts for each mailbox. This register is available in normal mailbox mode. Do not access this register in FIFO mailbox mode

Each bit is associated with a mailbox with the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes as follows:

- Bit [0] in MIER is associated with mailbox 0 (MB0)
- Bit [31] in MIER is associated with mailbox 31 (MB31).

Write to MIER only when the related MCTL_TXj or MCTL_RXj (j = 0 to 31) register is 00h and the associated mailbox does not process a transmission or reception abort request.

IDE位（ID扩展）

IDE位将ID格式设置为标准ID或扩展ID。当IDFM[1:0]位在CTLR寄存器为10b（混合ID模式）：

- 接收邮箱只接收IDE位指定的ID格式
- 发送邮箱以IDE位中指定的ID格式发送
- 接收FIFO邮箱接收具有标准ID和扩展ID设置的报文，该设置在FIDCR0和FIDCR1寄存器的IDE位中指定
- 发送FIFO邮箱使用发送消息的IDE位中指定的标准ID或扩展ID设置发送消息。

DLC[3:0]位（数据长度代码）

DLC[3:0]位指定要在数据帧中传输的数据长度。当使用远程帧请求数据时，该字段指定请求的数据长度。

当接收到一个数据帧时，接收到的数据长度存储在该字段中。当接收到远程帧时，该字段存储请求的数据长度。

31.2.7 邮箱中断使能寄存器(MIER)

Address(es): CAN0.MIER 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MB31 to MB0	中断使能	0：中断禁止1：中断允许。位[31]与邮箱31(MB31)相关联，位[0]与邮箱0(MB0)相关联。	R/W

MIER寄存器允许独立启用每个邮箱的中断。该寄存器在正常邮箱模式下可用。不要在FIFO邮箱模式下访问该寄存器

每个位都与具有相同编号的邮箱相关联。这些位启用或禁用相关邮箱的发送和接收完成中断，如下所示：

- MIER中的位[0]与邮箱0(MB0)相关联
- MIER中的位[31]与邮箱31(MB31)相关联。

仅当相关的MCTL_TXj或MCTL_RXj（j=0到31）寄存器为00h且相关邮箱不处理发送或接收中止请求时才写入MIER。

31.2.8 Mailbox Interrupt Enable Register for FIFO Mailbox Mode (MIER_FIFO)

Address(es): CAN0.MIER_FIFO 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	MB29	MB28	—	—	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b23 to b0	MB23 to MB0	Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled. Bit [23] corresponds to mailbox 23 (MB23) and bit [0] corresponds to mailbox 0 (MB0).	R/W
b24	MB24	Transmit FIFO Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b25	MB25	Transmit FIFO Interrupt Generation Timing Control	0: Generated every time transmission completes 1: Generated when the transmit FIFO empties on transmission completion.	R/W
b27, b26	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b28	MB28	Receive FIFO Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled.	R/W
b29	MB29	Receive FIFO Interrupt Generation Timing Control*1	0: Generated every time reception completes 1: Generated when the receive FIFO becomes buffer warning*2 on reception completion.	R/W
b31, b30	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. No interrupt request is generated when the receive FIFO becomes a buffer warning from full.
Note 2. Buffer warning indicates a state in which the third message is stored in the receive FIFO.

The MIER_FIFO register allows independent enabling of interrupts for each mailbox and FIFO. This register is available in FIFO mailbox mode. Do not access this register in normal mailbox mode.

The MB0 to MB23 bits are associated with the mailbox of the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes:

- Bit [0] in MIER_FIFO is associated with mailbox 0 (MB0)
- Bit [23] in MIER_FIFO is associated with mailbox 23 (MB23).

The MB24, MB25, MB28 and MB29 bits specify whether transmit and receive FIFO interrupts are enabled or disabled and the timing when interrupt requests are generated.

Write to the MIER_FIFO register only when the related MCTL_TXj or MCTL_RXj (j = 0 to 31) register is 00h and the associated mailbox does not process a transmission or reception abort request. In addition, change the bits in MIER_FIFO for the related FIFO only when all the following conditions are true:

- The TFE bit in TFCR is 0 and the TFEST bit is 1
- The RFE bit in RFCR is 0 and the RFEST flag in RFCR is 1.

31.2.8 FIFO邮箱模式的邮箱中断使能寄存器(MIER_FIFO)

Address(es): CAN0.MIER_FIFO 4005 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	MB29	MB28	—	—	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b23 to b0	MB23 to MB0	中断使能	0：中断禁止1：中断允许。位[23]对应邮箱23(MB23)，位[0]对应邮箱0(MB0)。	R/W
b24	MB24	发送FIFO中断Enable	0：中断禁止1：中断允许。	R/W
b25	MB25	发送FIFO中断发电时序控制	0：每次发送完成时产生1：发送完成时发送FIFO清空时产生。	R/W
b27, b26	—	Reserved	读取值未定义。写入值应为0。	R/W
b28	MB28	接收FIFO中断Enable	0：中断禁止1：中断允许。	R/W
b29	MB29	接收FIFO中断发电时序控制*1	0：每次接收完成时产生1：当接收FIFO变为缓冲区警告*时产生2接收完成时产生。	R/W
b31, b30	—	Reserved	读取值未定义。写入值应为0。	R/W

Note 1. 当接收FIFO从已满变为缓冲区警告时，不会产生中断请求。
Note 2. 缓冲区警告表示第三个消息存储在接收FIFO中的状态。

MIER_FIFO寄存器允许独立启用每个邮箱和FIFO的中断。该寄存器在FIFO邮箱模式下可用。不要在普通邮箱模式下访问该寄存器。

MB0到MB23位与相同编号的邮箱相关联。这些位启用或禁用相关邮箱的发送和接收完成中断：

- MIER_FIFO中的位[0]与邮箱0(MB0)相关联
- MIER_FIFO中的位[23]与邮箱23(MB23)相关联。

MB24、MB25、MB28和MB29位指定是启用还是禁用发送和接收FIFO中断以及生成中断请求的时间。

仅当相关MCTL_TXj或MCTL_RXj（j=0到31）寄存器为00h且相关邮箱不处理发送或接收中止请求时才写入MIER_FIFO寄存器。此外，仅当满足以下所有条件时，才更改相关FIFO的MIER_FIFO中的位：

- TFCR中的TFE位为0，TFEST位为1
- RFCR中的RFE位为0，RFCR中的RFEST标志为1。

31.2.9 Message Control Registers for Transmit (MCTL_TXj) (j = 0 to 31)

- Transmit mode (when the TRMREQ bit is 1 and the RECREQ bit is 0)

Address(es): CAN0.MCTL_TX0 4005 0820h to CAN0.MCTL_TX31 4005 083Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SENTDATA	Transmission Complete Flag*1,*2	0: Transmission not complete 1: Transmission complete.	R/W
b1	TRMACTIVE	Transmission-in-Progress Status Flag	0: Transmission pending or transmission is not requested 1: Transmission in progress.	R
b2	TRMABT	Transmission Abort Complete Flag*1,*2	0: Transmission started, transmission abort failed because transmission completed, or transmission abort not requested 1: Transmission abort complete.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot transmission 1: Enable one-shot transmission.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits of this register, write 1 to the SENTDATA and TRMABT flags if they are not the write target.
Note 3. To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1.
To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message is transmitted or aborted.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set the SENDDATA, TRMACTIVE, and TRMABT flags to 0 simultaneously.

The MCTL_TXj register sets the mailbox j to transmit mode or receive mode. In transmit mode, MCTL_TXj also controls and indicates the status of transmission. Do not access the MCTL_TXj register if the mailbox j is in receive mode. Only write to the MCTL_TXj register in CAN operation mode or CAN halt mode. Do not use the MCTL_TX24 through MCTL_TX31 registers in FIFO mailbox mode.

SENTDATA flag (Transmission Complete Flag)

The SENTDATA flag is set to 1 when data transmission from the associated mailbox is complete. This flag is set to 0 through a software write.

To set this flag to 0, first set the TRMREQ bit to 0. The SENTDATA flag and the TRMREQ bit cannot be set to 0 simultaneously. To transmit a new message from the associated mailbox, set the SENTDATA flag to 0.

TRMACTIVE flag (Transmission-in-Progress Status Flag)

The TRMACTIVE flag is set to 1 when the associated mailbox of the CAN module begins to transmit a message. The TRMACTIVE flag is set to 0 when the CAN module loses the CAN bus arbitration, a CAN bus error occurs, or data transmission is complete.

TRMABT flag (Transmission Abort Complete Flag)

The TRMABT flag is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort completes before starting transmission
- Following a transmission abort request, when the CAN module detects CAN bus arbitration-lost or CAN bus error

31.2.9 用于发送的消息控制寄存器(MCTL_TXj)(j=0到31)

发送模式（当TRMREQ位为1且RECREQ位为0时）

Address(es): CAN0.MCTL_TX0 4005 0820h to CAN0.MCTL_TX31 4005 083Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SENTDATA	传输完成 Flag*1,*2	0：传输未完成1：传输完成 。	R/W
b1	TRMACTIVE	Transmission-in-Progress 状态标志	0：传输未决或未请求传输1：传输中。	R
b2	TRMABT	传输中止完成 Flag*1,*2	0：传输开始，传输中止失败，因为 传输完成，或未请求传输中止1：传输中止完成。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0：禁止一次性发送1：允许一次 性发送。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	RECREQ	接收邮箱请求 *2,*3,*4,*5	0：不配置接收1：配置接收。	R/W
b7	TRMREQ	发送邮箱请求 *2,*4	0：不配置传输1：配置传输。	R/W

Note 1. 只写0。写1无效。
Note 2. 写入该寄存器的位时，如果SENTDATA和TRMABT标志不是写入目标，则向它们写入1。
Note 3. 要进入一次性发送模式，在将TRMREQ位设置为1的同时将1写入ONESHOT位。
要退出一次性发送模式，请在发送或中止消息后将0写入ONESHOT位。
Note 4. 不要将RECREQ和TRMREQ位都设置为1。
Note 5. 将RECREQ位设置为0时，同时将SENDDATA、TRMACTIVE和TRMABT标志设置为0。

MCTL_TXj寄存器将邮箱j设置为发送模式或接收模式。在传输模式下，MCTL_TXj还控制和指示传输状态。如果邮箱j处于接收模式，则不要访问MCTL_TXj寄存器。仅在CAN操作模式或CAN暂停模式下写入MCTL_TXj寄存器。不要在FIFO邮箱模式下使用MCTL_TX24到MCTL_TX31寄存器。

SENTDATA标志（传输完成标志）

当来自相关邮箱的数据传输完成时，SENTDATA标志设置为1。该标志通过软件写入设置为0。

要将此标志设置为0，首先将TRMREQ位设置为0。SENTDATA标志和TRMREQ位不能同时设置为0。要从关联邮箱发送新消息，请将SENTDATA标志设置为0。

TRMACTIVE标志（传输中状态标志）

当CAN模块的相关邮箱开始发送消息时，TRMACTIVE标志设置为1。这
当CAN模块失去CAN总线仲裁、发生CAN总线错误或数据传输完成时，TRMACTIVE标志设置为0。

TRMABT标志（传输中止完成标志）

在以下情况下，TRMABT标志设置为1：

- 在传输中止请求之后，当传输中止在开始传输之前完成时
- 在发送中止请求之后，当CAN模块检测到CAN总线仲裁丢失或CAN总线错误时

- In one-shot transmission mode (RECREQ = 0, TRMREQ = 1, and ONESHOT = 1), when the CAN module detects CAN bus arbitration-lost or CAN bus error.

The TRMABT flag is not set to 1 when data transmission is complete. The SENTDATA flag is set to 1 and the TRMABT flag is set to 0 through a software write.

ONESHOT bit (One-Shot Enable)

When the ONESHOT bit is set to 1 in transmit mode (RECREQ = 0 and TRMREQ = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration-lost occurs. When transmission is complete, the SENTDATA flag is set to 1. If transmission is not complete due to a CAN bus error or CAN bus arbitration-lost, the TRMABT flag is set to 1. Set the ONESHOT bit to 0 after the SENTDATA or TRMABT flag is set to 1.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 31.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data frame or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data frame or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after the acceptance filter processing
  - If no mailbox is specified to receive the message, after the acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission, then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_TXj.RECREQ is the mirror bit of MCTL_RXj.RECREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 31.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data frame or a remote frame.

When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data frame or a remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, then set the NEWDATA and MSGLOST flags to 0 before changing to transmission.

Note: MCTL_TXj.TRMREQ is the mirror bit of MCTL_RXj.TRMREQ.

- 在一次性传输模式下（RECREQ=0、TRMREQ=1和ONESHOT=1），当CAN模块检测到CAN总线仲裁丢失或CAN总线错误。

当数据传输完成时，TRMABT标志不设置为1。SENTDATA标志设置为1，TRMABT标志通过软件写入设置为0。

ONESHOT位（一次性启用）

在发送模式下（RECREQ=0且TRMREQ=1）将ONESHOT位设置为1时，CAN模块仅发送一次报文。如果发生CAN总线错误或CAN总线仲裁失败，CAN模块不会再次发送消息。传输完成时，SENTDATA标志设置为1。如果由于CAN总线错误或CAN总线仲裁丢失而导致传输未完成，则TRMABT标志设置为1。在SENTDATA或TRMABT之后将ONESHOT位设置为0标志设置为1。

RECREQ位（接收邮箱请求）

RECREQ位选择表31.10中列出的接收模式。

当RECREQ位设置为1时，相关邮箱配置为接收数据帧或远程帧。

当RECREQ位设置为0时，相关邮箱未配置为接收数据帧或远程帧。

由于硬件保护，RECREQ位在以下期间不能通过软件写入设置为0：

- 硬件保护从验收过滤器处理开始（CRC字段的开始）
- 硬件保护发布：
  - 对于指定接收传入报文的邮箱，在接收到的数据存入邮箱后或出现CAN总线错误。这意味着硬件保护的最大周期是从CRC字段的开始到EOF的第7位结束。
  - 对于其他邮箱，接受过滤处理后
  - 如果没有指定邮箱接收邮件，则在接受过滤处理后。

将RECREQ位设置为1时，不要将TRMREQ位设置为1。要将邮箱配置从发送更改为接收，首先中止发送，然后在更改为接收之前将SENTDATA和TRMABT标志设置为0。

Note: MCTL_TXj.RECREQ是MCTL_RXj.RECREQ的镜像位。

TRMREQ位（发送邮箱请求）

TRMREQ位选择表31.10中列出的发送模式。

当TRMREQ位设置为1时，相关邮箱配置为传输数据帧或远程帧。

当TRMREQ位设置为0时，相关邮箱未配置为传输数据帧或远程帧。

如果TRMREQ位从1更改为0以取消相关的发送请求，则TRMABT或SENTDATA标志设置为1。将TRMREQ位设置为1时，不要将RECREQ位设置为1。要更改邮箱从接收到发送，首先中止接收，然后将NEWDATA和MSGLOST标志设置为0，然后再更改为发送。

Note: MCTL_TXj.TRMREQ是MCTL_RXj.TRMREQ的镜像位。

31.2.10 Message Control Register for Receive (MCTL_RXj) (j = 0 to 31)

- Receive mode (when the TRMREQ bit is 0 and the RECREQ bit is 1)

Address(es): CAN0.MCTL_RX0 4005 0820h to CAN0.MCTL_RX31 4005 083Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NEWDATA	Reception Complete Flag*1,*2	0: No data received, or 0 was written to the NEWDATA flag 1: New message is being stored or was stored in the mailbox.	R/W
b1	INVALDATA	Reception-in-Progress Status Flag	0: Message valid 1: Message updated.	R
b2	MSGLOST	Message Lost Flag*1,*2	0: Message not overwritten or overrun 1: Message overwritten or overrun.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot reception 1: Enable one-shot reception.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits in this register, write 1 to the NEWDATA and MSGLOST flags if they are not the write target.
Note 3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1.
To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming that it is set to 0.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set MSGLOST, NEWDATA, and RECREQ to 0 simultaneously.

The MCTL_RXj register sets mailbox j to transmit mode or receive mode. In receive mode, MCTL_RXj also controls and indicates status of reception.

Do not access the MCTL_RXj register if mailbox j is in transmit mode. Only write to the MCTL_RXj register in CAN operation mode or CAN halt mode. Do not use the MCTL_RX24 to MCTL_RX31 registers in FIFO mailbox mode.

NEWDATA flag (Reception Complete Flag)

The NEWDATA flag is set to 1 when a new message is being stored or was stored in the mailbox. Always set this bit to 1 simultaneously with the INVALDATA flag. The NEWDATA flag is set to 0 through a software write. The NEWDATA flag cannot be set to 0 through a software write when the associated INVALDATA flag is 1.

INVALDATA flag (Reception-in-Progress Status Flag)

After the completion of a message reception, the INVALDATA flag is set to 1 while the received message is updated in the associated mailbox. The INVALDATA flag is set to 0 immediately after the message is stored. If the mailbox is read when the INVALDATA flag is 1, the data is undefined.

MSGLOST flag (Message Lost Flag)

The MSGLOST flag is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA flag is 1. The MSGLOST flag is set to 1 at the end of the 6th bit of EOF. The MSGLOST flag is set to 0 through a software write.

In both overwrite and overrun modes, the MSGLOST flag cannot be set to 0 through a software write during the 5 PCLKB cycles following the 6th bit of EOF.

31.2.10 接收消息控制寄存器(MCTL_RXj)(j=0to31)

接收模式（当TRMREQ位为0且RECREQ位为1时）

Address(es): CAN0.MCTL_RX0 4005 0820h to CAN0.MCTL_RX31 4005 083Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	NEWDATA	接收完成标志 *1,*2	0：未接收到数据，或向NEWDATA标志写入01：新消息正在存储或已存储在邮箱中。	R/W
b1	INVALDATA	Reception-in-Progress Status Flag	0：消息有效1：消息已更新。	R
b2	MSGLOST	消息丢失标志 *1,*2	0：信息未被覆盖或溢出1：信息被覆盖或溢出。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0：关闭一键接收1：打开一键接收。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	RECREQ	接收邮箱请求 *2,*3,*4,*5	0：不配置接收1：配置接收。	R/W
b7	TRMREQ	发送邮箱请求 *2,*4	0：不配置传输1：配置传输。	R/W

Note 1. 只写0。写1无效。
Note 2. 写入此寄存器中的位时，如果NEWDATA和MSGLOST标志不是写入目标，则将它们写入1。
Note 3. 要进入一次性接收模式，在将RECREQ位设置为1的同时将1写入ONESHOT位。
要退出一次性接收模式，在向RECREQ位写入0并确认其设置为0后，向ONESHOT位写入0。
Note 4. 不要将RECREQ和TRMREQ位都设置为1。
Note 5. 将RECREQ位设置为0时，同时将MSGLOST、NEWDATA和RECREQ设置为0。

MCTL_RXj寄存器将邮箱j设置为发送模式或接收模式。在接收模式下，MCTL_RXj还控制和指示接收状态。

如果邮箱j处于发送模式，则不要访问MCTL_RXj寄存器。仅在CAN操作模式或CAN暂停模式下写入MCTL_RXj寄存器。不要在FIFO邮箱模式下使用MCTL_RX24到MCTL_RX31寄存器。

NEWDATA标志（接收完成标志）

当新消息正在存储或已存储在邮箱中时，NEWDATA标志设置为1。始终将此位与INVALDATA标志同时设置为1。NEWDATA标志通过软件写入设置为0。当关联的INVALDATA标志为1时，不能通过软件写入将NEWDATA标志设置为0。

INVALDATA标志（接收进行中状态标志）

消息接收完成后，INVALDATA标志设置为1，同时在相关邮箱中更新接收到的消息。INVALDATA标志在消息存储后立即设置为0。如果在INVALDATA标志为1时读取邮箱，则数据未定义。

MSGLOST标志（消息丢失标志）

当邮箱被新收到的消息覆盖或溢出时，MSGLOST标志设置为1，而NEWDATA标志为1。MSGLOST标志在EOF的第6位末尾设置为1。MSGLOST标志通过软件写入设置为0。

在覆盖和溢出模式下，MSGLOST标志不能在5期间通过软件写入设置为0在EOF的第6位之后的PCLKB周期。

ONESHOT bit (One-Shot Enable)

When the ONESHOT bit is set to 1 in receive mode (RECREQ = 1 and TRMREQ = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after it receives the message. The behavior of the NEWDATA and INVALDATA flags is the same as in normal receive mode. In one-shot receive mode, the MSGLOST flag is not set to 1. To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it is 0.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 31.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data frame or a remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from the acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox, or a CAN bus error occurs. The maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after the acceptance filter processing
  - If no mailbox is specified to receive the message, after the acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission, and then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_RXj.RECREQ is the mirror bit of MCTL_TXj.REQREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 31.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data frame or a remote frame.

If the TRMREQ bit changes from 1 to 0 to cancel the associated transmission request, either the TRMABT flag or the SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, and then set the NEWDATA and MSGLOST flags to 0 before changing to transmission.

Note: MCTL_RXj.TRMREQ is the mirror bit of MCTL_TXj.TRMREQ.

31.2.11 Receive FIFO Control Register (RFCR)

Address(es): CAN0.RFCR 4005 0848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RFE	Receive FIFO Enable	0: Disable receive FIFO 1: Enable receive FIFO.	R/W

ONESHOT位（一次性启用）

在接收模式下（RECREQ=1和TRMREQ=0）将ONESHOT位设置为1时，邮箱只接收一次消息。邮箱在收到邮件后不会充当接收邮箱。NEWDATA和INVALDATA标志的行为与正常接收模式相同。在单次接收模式下，MSGLOST标志不设置为1。要将ONESHOT位设置为0，首先将0写入RECREQ位并确保其为0。

RECREQ位（接收邮箱请求）

RECREQ位选择表31.10中列出的接收模式。

当RECREQ位设置为1时，相关邮箱配置为接收数据帧或远程帧。

由于硬件保护，RECREQ位在以下期间不能通过软件写入设置为0：

- 硬件保护从验收过滤器处理开始（CRC字段的开始）
- 硬件保护发布：
  - 对于指定接收传入报文的邮箱，在将接收到的数据存入邮箱后，或出现CAN总线错误。硬件保护的最大周期是从CRC域开始到EOF第7位结束。
  - 对于其他邮箱，接受过滤处理后
  - 如果没有指定邮箱接收邮件，则在接受过滤处理后。

将RECREQ位设置为1时，不要将TRMREQ位设置为1。要将邮箱配置从发送更改为接收，首先中止发送，然后在更改为接收之前将SENTDATA和TRMABT标志设置为0。

Note: MCTL_RXj.RECREQ是MCTL_TXj.REQREQ的镜像位。

TRMREQ位（发送邮箱请求）

TRMREQ位选择表31.10中列出的发送模式。

当TRMREQ位设置为1时，相关邮箱配置为传输数据帧或远程帧。

如果TRMREQ位从1变为0以取消相关的传输请求，则TRMABT标志或SENTDATA标志设置为1。将TRMREQ位设置为1时，不要将RECREQ位设置为1。要将邮箱配置从接收更改为发送，首先中止接收，然后将NEWDATA和MSGLOST标志设置为0在更改为传输之前。

Note: MCTL_RXj.TRMREQ是MCTL_TXj.TRMREQ的镜像位。

31.2.11 接收FIFO控制寄存器(RFCR)

Address(es): CAN0.RFCR 4005 0848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RFE	接收FIFO使能	0：禁用接收FIFO1：启用接收FIFO。	R/W

Bit	Symbol	Bit name	Description	R/W
b3 to b1	RFUST[2:0]	Receive FIFO Unread Message Number Status	b3 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b4	RFMLF	Receive FIFO Message Lost Flag	0: Receive FIFO message not lost 1: Receive FIFO message lost.	R/W
b5	RFFST	Receive FIFO Full Status Flag	0: Receive FIFO not full 1: Receive FIFO full (4 unread messages).	R
b6	RFWST	Receive FIFO Buffer Warning Status Flag	0: Receive FIFO has no buffer warning 1: Receive FIFO has buffer warning (3 unread messages).	R
b7	RFEST	Receive FIFO Empty Status Flag	0: Unread message in receive FIFO 1: No unread message in receive FIFO.	R

Write to the RFCR register in CAN operation mode or CAN halt mode.

RFE bit (Receive FIFO Enable)

When the RFE bit is set to 1, the receive FIFO is enabled. When the RFE bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST = 1). Write 0 to the RFE bit simultaneously with the RFMLF flag setting.

Do not set this bit to 1 in normal mailbox mode (MBM = 0). Due to hardware protection, the RFE bit is not set to 0 through a software write during the following period:

- Hardware protection is started from the acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - If the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. The maximum period of hardware protection is from the beginning of the CRC field to the end of 7th bit of EOF.
  - If the receive FIFO is not specified to receive the message, after the acceptance filter processing.

RFUST[2:0] bits (Receive FIFO Unread Message Number Status)

The RFUST[2:0] bits indicate the number of unread messages in the receive FIFO. The value of the RFUST[2:0] bits is initialized to 000b when the RFE bit is set to 0.

RFMLF flag (Receive FIFO Message Lost Flag)

The RFMLF flag is set to 1 (receive FIFO message lost) when the receive FIFO receives a new message and is full. This flag is set to 1 at the end of the 6th bit of EOF.

The RFMLF flag is set to 0 through a software write (writing 1 has no effect). In both overwrite and overrun modes, if the receive FIFO is full and determined to receive a message, the RFMLF flag cannot be set to 0 (no receive FIFO message lost) through a software write during 5 PCLKB cycles following the 6th bit of EOF, due to hardware protection.

RFFST flag (Receive FIFO Full Status Flag)

The RFFST flag is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. The RFFST flag is 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The RFFST flag is set to 0 when the RFE bit is 0.

RFWST flag (Receive FIFO Buffer Warning Status Flag)

The RFWST flag is set to 1 (receive FIFO buffer warning) when the number of unread messages in the receive FIFO is 3. The RFWST flag is 0 (no receive FIFO buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. The RFWST flag is set to 0 when the RFE bit is 0.

Bit	Symbol	位名称	Description	R/W
b3 to b1	RFUST[2:0]	接收FIFO未读消息号码状态	b3b1000：没有未读消息00 1：1条未读消息010：2条未读消息011：3条未读消息100：4条未读消息101：保留110：保留111：预订的。	R
b4	RFMLF	接收FIFO消息丢失标志	0：接收FIFO报文不丢失1：接收FIFO报文丢失。	R/W
b5	RFFST	接收FIFO满状态标志	0：接收FIFO未满1：接收FIFO已满（4个未读消息）。	R
b6	RFWST	接收FIFO缓冲区警告状态标志	0：接收FIFO没有缓冲区警告1：接收FIFO有缓冲区警告（3个未读消息）。	R
b7	RFEST	接收FIFO空状态标志	0：接收FIFO中未读消息1：接收FIFO中没有未读消息。	R

在CAN操作模式或CAN暂停模式下写入RFCR寄存器。

RFE位（接收FIFO使能）

当RFE位设置为1时，启用接收FIFO。当RFE位设置为0时，接收FIFO禁止接收并变为空(RFEST=1)。在设置RFMLF标志的同时将0写入RFE位。

在正常邮箱模式(MBM=0)下不要将此位设置为1。由于硬件保护，RFE位在以下期间不会通过软件写入设置为0：

- 硬件保护从验收过滤器处理开始（CRC字段的开始）
- 硬件保护发布：
  - 如果指定接收FIFO接收传入报文，则在接收到的数据存储到接收FIFO后或出现CAN总线错误。硬件保护的最大周期是从CRC域开始到EOF第7位结束。
  - 如果接收FIFO没有指定接收报文，接受过滤后处理。

RFUST[2:0]位（接收FIFO未读消息编号状态）

RFUST[2:0]位指示接收FIFO中未读消息的数量。当RFE位设置为0时，RFUST[2:0]位的值初始化为000b。

RFMLF标志（接收FIFO消息丢失标志）

当接收FIFO接收到新消息并已满时，RFMLF标志设置为1（接收FIFO消息丢失）。该标志在EOF的第6位末尾设置为1。

RFMLF标志通过软件写入设置为0（写入1无效）。在覆盖和溢出模式下，如果接收FIFO已满并确定接收消息，则在EOF第6位之后的5个PCLKB周期内，RFMLF标志不能通过软件写入设置为0（没有接收FIFO消息丢失），由于硬件保护。

RFFST标志（接收FIFO满状态标志）

当接收FIFO中的未读消息数为4时，RFFST标志设置为1（接收FIFO已满）。
当接收FIFO中未读消息的数量小于4时，RFFST标志为0（接收FIFO未满）。
当RFE位为0时，RFFST标志设置为0。

RFWST标志（接收FIFO缓冲区警告状态标志）

当接收FIFO中未读消息的数量为3时，RFWST标志设置为1（接收FIFO缓冲区警告）。当接收FIFO中的未读消息数量较少时，RFWST标志为0（无接收FIFO缓冲区警告）大于3或等于4。当RFE位为0时，RFWST标志设置为0。

RFEST flag (Receive FIFO Empty Status Flag)

The RFEST flag is set to 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. The RFEST flag is set to 1 when the RFE bit is set to 0. The RFEST flag is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 31.2 shows the receive FIFO mailbox operation.

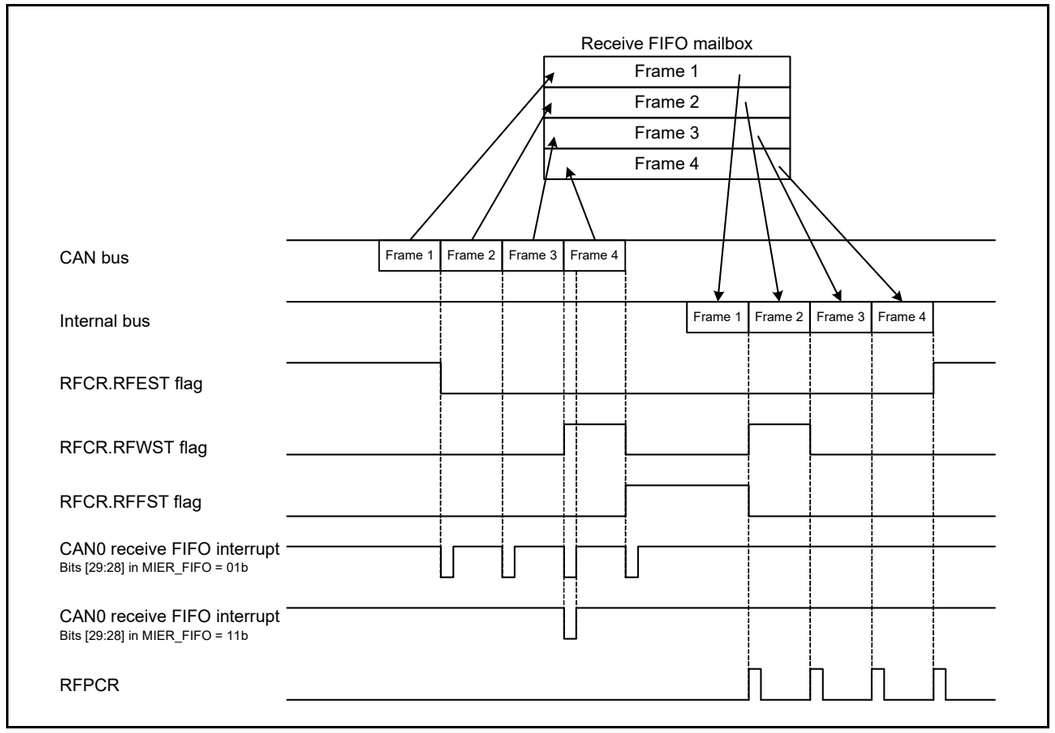


Figure 31.2 Receive FIFO mailbox operation with bits [29:28] in MIER_FIFO = 01b or 11b

31.2.12 Receive FIFO Pointer Control Register (RFPCR)

Address(es): CAN0.RFPCR 4005 0849h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the receive FIFO is incremented by writing FFh to RFPCR	W

When the receive FIFO is not empty, write FFh to the RFPCR register through software to increment the CPU pointer to the next mailbox location. Do not write to the RFPCR register when the RFE bit in RFCR is 0 (receive FIFO disabled).

Both the CAN and CPU pointers are incremented when a new message is received and the RFFST flag is 1 (receive FIFO is full) in overwrite mode. When the RFMLF flag is 1 in this condition, the CPU pointer cannot be incremented on a software write to RFPCR.

RFEST标志（接收FIFO空状态标志）

RFEST标志设置为1（接收FIFO中没有未读消息），当接收中的未读消息数FIFO为0。当RFE位设置为0时，RFEST标志设置为1。RFEST标志设置为0（接收中的未读消息FIFO)当接收FIFO中的未读消息数为1或更多时。

图31.2显示了接收FIFO邮箱操作。

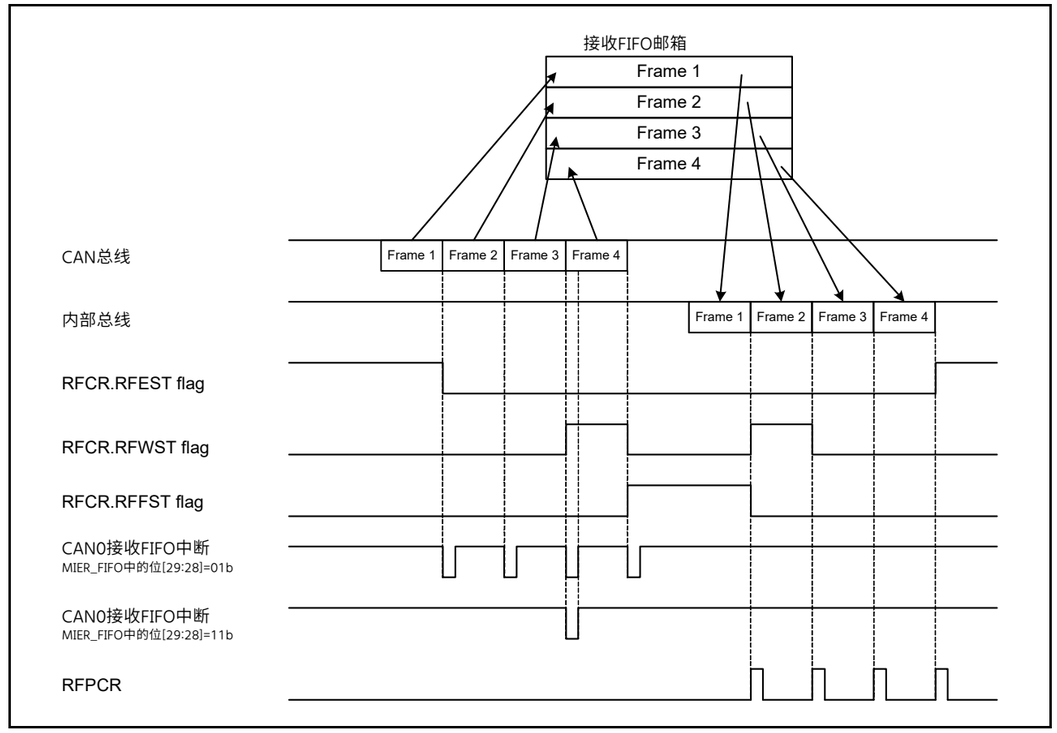


Figure 31.2 使用MIER_FIFO=01b或11b中的位[29:28]接收FIFO邮箱操作

31.2.12 接收FIFO指针控制寄存器(RFPCR)

Address(es): CAN0.RFPCR 4005 0849h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	通过将FFh写入RFPCR，接收FIFO的CPU指针递增	W

当接收FIFO不为空时，通过软件将FFh写入RFPCR寄存器，使CPU指针递增到下一个邮箱位置。当RFCR中的RFE位为0（禁用接收FIFO）时，不要写入RFPCR寄存器。

CAN和CPU指针都在收到新消息并且RFFST标志为1时递增（接收FIFO已满）处于覆盖模式。在这种情况下，当RFMLF标志为1时，CPU指针不能在软件写入RFPCR时递增。

31.2.13 Transmit FIFO Control Register (TFCR)

Address(es): CAN0.TFCR 4005 084Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TFE	Transmit FIFO Enable	0: Disable transmit FIFO 1: Enable transmit FIFO.	R/W
b3 to b1	TFUST[2:0]	Transmit FIFO Unsent Message Number Status	b3 b1 0 0 0: 0 unsent messages 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	TFFST	Transmit FIFO Full Status	0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages).	R
b7	TFEST	Transmit FIFO Empty Status	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO.	R

Write to TFCR in CAN operation mode or CAN halt mode.

TFE bit (Transmit FIFO Enable)

When the TFE bit is set to 1, the transmit FIFO is enabled.

When the TFE bit is set to 0, the transmit FIFO becomes empty (TFEST bit = 1), and unsent messages from the transmit FIFO are lost in the following ways:

- Immediately if a message from the transmit FIFO is not scheduled for the next transmission or already in transmission
- Following the completion of transmission, a CAN bus error, CAN bus arbitration-lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already in transmission.

Before setting the TFE bit to 1 again, ensure that the TFEST bit is set to 1. After setting the TFE bit to 1, write transmit data to mailbox 24.

Do not set the TFE bit to 1 in normal mailbox mode (MBM bit in CTLR = 0).

TFUST[2:0] bits (Transmit FIFO Unsent Message Number Status)

The TFUST[2:0] bits indicate the number of unsent messages in the transmit FIFO. The TFUST[2:0] bits are set to 000b after the TFE bit is set to 0 and transmission is aborted or completed.

TFFST bit (Transmit FIFO Full Status)

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to 0 when transmission from the transmit FIFO is aborted.

TFEST bit (Transmit FIFO Empty Status)

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. The TFEST bit is set to 1 when transmission from the transmit FIFO aborts. The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

31.2.13 发送FIFO控制寄存器(TFCR)

Address(es): CAN0.TFCR 4005 084Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TFE	发送FIFO使能	0：禁用发送FIFO1：启用发送FIFO。	R/W
b3 to b1	TFUST[2:0]	发送FIFO未发送消息号码状态	b3b1000：0条未发送消息001：1条未发送消息010：2条未发送消息011：3条未发送消息100：4条未发送消息101：保留110：保留111：预订的。	R
b5, b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	TFFST	发送FIFO满状态	0：发送FIFO未满1：发送FIFO已满（4条未发送消息）。	R
b7	TFEST	发送FIFO空状态	0：发送FIFO中未发送消息1：发送FIFO中没有未发送消息。	R

在CAN操作模式或CAN暂停模式下写入TFCR。

TFE位（发送FIFO使能）

当TFE位设置为1时，使能发送FIFO。

当TFE位设置为0时，发送FIFO变为空（TFEST位=1），并且未发送的消息从发送FIFO通过以下方式丢失：

- 如果来自发送FIFO的消息未安排用于下一次传输或已在传输中，则立即执行
- 传输完成后，如果来自传输FIFO的消息被安排用于下一次传输或已经在传输中，则CAN总线错误、CAN总线仲裁丢失或进入CAN暂停模式。

再次将TFE位设置为1之前，请确保TFEST位设置为1。将TFE位设置为1后，将发送数据写入邮箱24。

不要在正常邮箱模式下将TFE位设置为1（CTLR中的MBM位=0）。

TFUST[2:0]位（发送FIFO未发送消息编号状态）

TFUST[2:0]位指示发送FIFO中未发送消息的数量。在TFE位设置为0并且传输被中止或完成后，TFUST[2:0]位设置为000b。

TFFST位（发送FIFO满状态）

当发送FIFO中未发送的消息数为4时，TFFST位设置为1（发送FIFO已满）。
当发送FIFO中未发送消息的数量小于4时，TFFST位设置为0（发送FIFO未满）。
当来自发送FIFO的发送被中止时，TFFST位设置为0。

TFEST位（发送FIFO空状态）

当发送FIFO中未发送消息的数量为0时，TFEST位设置为1（发送FIFO中没有消息）。
当来自发送FIFO的发送中止时，TFEST位设置为1。当发送FIFO中未发送消息的数量不为0时，TFEST位设置为0（发送FIFO中的消息）。

Figure 31.3 shows the transmit FIFO mailbox operation.

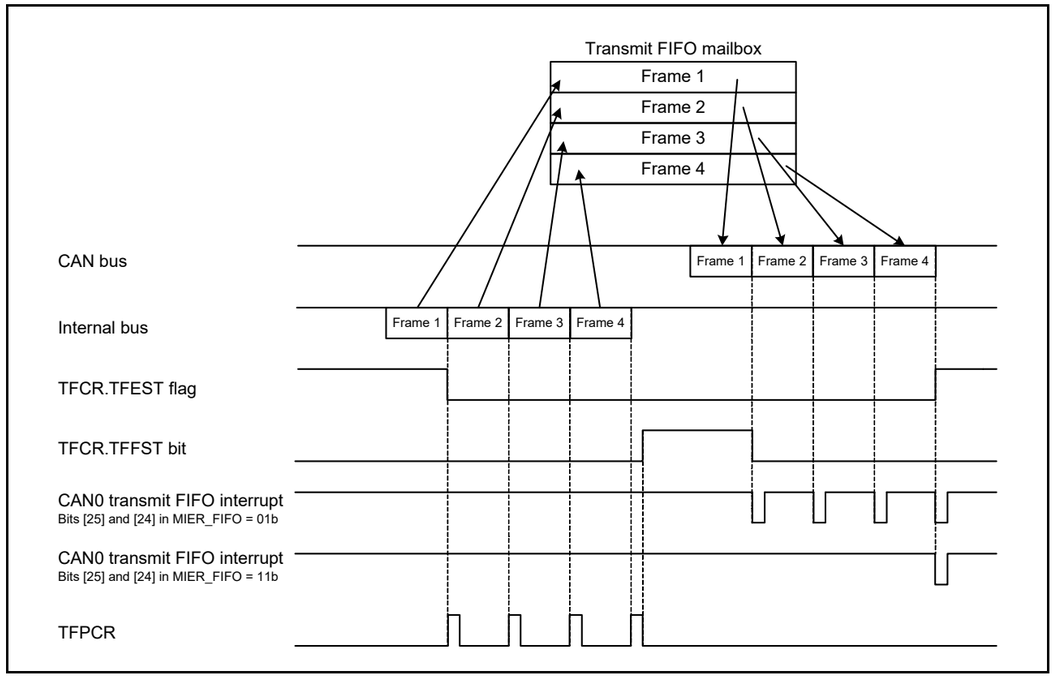


Figure 31.3 Transmit FIFO mailbox operation when MIER_FIFO[25:24] = 01b or 11b

31.2.14 Transmit FIFO Pointer Control Register (TFPCR)

Address(es): CAN0.TFPCR 4005 084Bh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the transmit FIFO is incremented by writing FFh to TFPCR	W

When the transmit FIFO is not full, write FFh to the TFPCR register through software to increment the CPU pointer for the transmit FIFO to the next mailbox location.

Do not write to the TFPCR register when the TFE bit in TFCR is 0 (transmit FIFO disabled).

图31.3显示了发送FIFO邮箱操作。

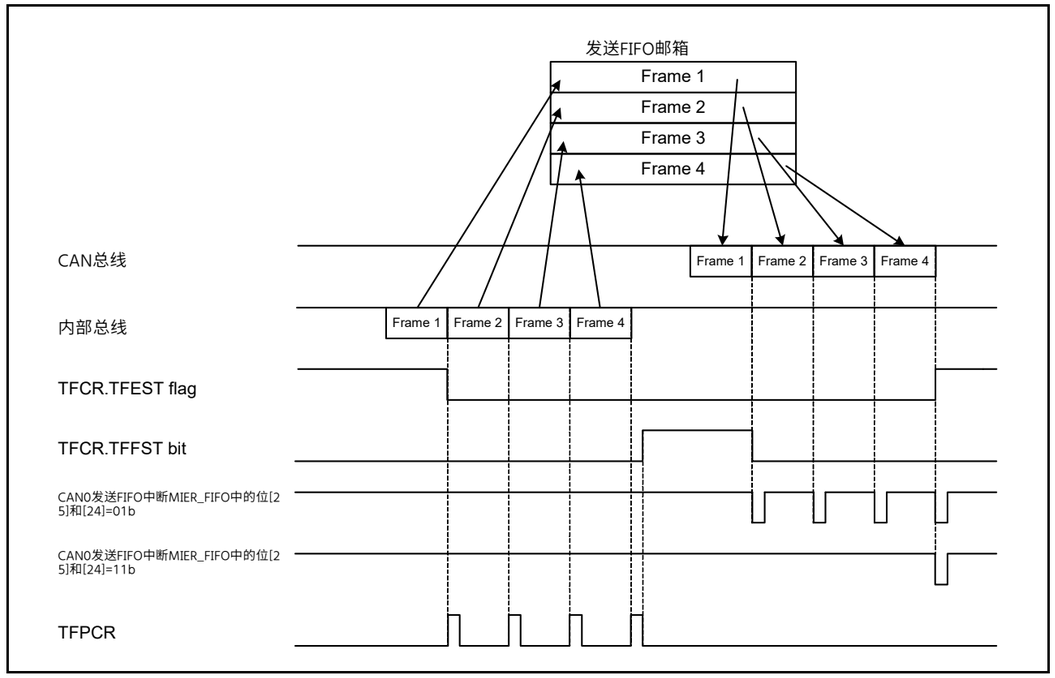


Figure 31.3 当MIER_FIFO[25:24]=01b或11b时发送FIFO邮箱操作

31.2.14 发送FIFO指针控制寄存器(TFPCR)

Address(es): CAN0.TFPCR 4005 084Bh

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	通过将FFh写入TFPCR，发送FIFO的CPU指针递增	W

当发送FIFO未满时，通过软件将FFh写入TFPCR寄存器，以将发送FIFO的CPU指针递增到下一个邮箱位置。

当TFCR中的TFE位为0（禁止发送FIFO）时，不要写入TFPCR寄存器。

31.2.15 Status Register (STR)

Address(es): CAN0.STR 4005 0842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NDST	NEWDATA Status Flag	0: No mailbox with NEWDATA = 1 1: 1 or more mailboxes with NEWDATA = 1.	R
b1	SDST	SENTDATA Status Flag	0: No mailbox with SENTDATA = 1 1: 1 or more mailboxes with SENTDATA = 1.	R
b2	RFST	Receive FIFO Status Flag	0: Receive FIFO empty 1: Message in receive FIFO.	R
b3	TFST	Transmit FIFO Status Flag	0: Transmit FIFO full 1: Transmit FIFO not full.	R
b4	NMLST	Normal Mailbox Message Lost Status Flag	0: No mailbox with MSGLOST = 1 1: One or more mailboxes with MSGLOST = 1.	R
b5	FMLST	FIFO Mailbox Message Lost Status Flag	0: RFMLF = 0 1: RFMLF = 1.	R
b6	TABST	Transmission Abort Status Flag	0: No mailbox with TRMABT = 1 1: 1 or more mailboxes with TRMABT = 1.	R
b7	EST	Error Status Flag	0: No error occurred 1: Error occurred.	R
b8	RSTST	CAN Reset Status Flag	0: Not in CAN reset mode 1: In CAN reset mode.	R
b9	HLTST	CAN Halt Status Flag	0: Not in CAN halt mode 1: In CAN halt mode.	R
b10	SLPST	CAN Sleep Status Flag	0: Not in CAN sleep mode 1: In CAN sleep mode.	R
b11	EPST	Error-Passive Status Flag	0: Not in error-passive state 1: In error-passive state.	R
b12	BOST	Bus-Off Status Flag	0: Not in bus-off state 1: In bus-off state.	R
b13	TRMST	Transmit Status Flag	0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state.	R
b14	RECST	Receive Status Flag	0: Bus idle or transmission in progress 1: Reception in progress.	R
b15	—	Reserved	The read value is 0	R

NDST flag (NEWDATA Status Flag)

The NDST flag is set to 1 when at least one NEWDATA flag in the MCTL_RXj (j = 0 to 31) registers is 1, regardless of the value of the MIER or MIER_FIFO registers. The NDST flag is set to 0 when all the NEWDATA flags are 0.

SDST flag (SENTDATA Status Flag)

The SDST flag is set to 1 when at least one SENTDATA flag in the MCTL_TXj (j = 0 to 31) registers is 1, regardless of the value of the MIER or MIER_FIFO registers. The SDST flag is set to 0 when all the SENTDATA flags are 0.

RFST flag (Receive FIFO Status Flag)

The RFST flag is set to 1 when the receive FIFO is not empty. The RFST flag is set to 0 when the receive FIFO is empty or normal mailbox mode is selected.

31.2.15 状态寄存器(STR)

Address(es): CAN0.STR 4005 0842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
重置后的值：	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	NDST	NEWDATA状态标志	0：没有NEWDATA=1的邮箱1：有1个或多个NEWDATA=1的邮箱。	R
b1	SDST	SENTDATA状态标志	0：没有SENTDATA=1的邮箱1：1个或多个SENTDATA=1的邮箱。	R
b2	RFST	接收FIFO状态标志	0：接收FIFO空1：接收FIFO中的消息。	R
b3	TFST	发送FIFO状态标志	0：发送FIFO已满1：发送FIFO未满。	R
b4	NMLST	普通邮箱消息丢失状态标志	0：没有MSGLOST=1的邮箱1：一个或多个MSGLOST=1的邮箱。	R
b5	FMLST	FIFO邮箱消息丢失状态Flag	0: RFMLF = 0 1: RFMLF = 1.	R
b6	TABST	传输中止状态标志	0：没有TRMABT=1的邮箱1：1个或多个TRMABT=1的邮箱。	R
b7	EST	错误状态标志	0：未发生错误1：发生错误。	R
b8	RSTST	CAN复位状态标志	0：不处于CAN复位模式1：处于CAN复位模式。	R
b9	HLTST	CAN停止状态标志	0：不处于CAN停止模式 1：处于CAN停止模式。	R
b10	SLPST	CAN睡眠状态标志	0：不处于CAN睡眠模式1：处于CAN睡眠模式。	R
b11	EPST	错误被动状态标志	0：不处于被动错误状态1：处于被动错误状态。	R
b12	BOST	总线关闭状态标志	0：不处于总线关闭状态 1：处于总线关闭状态。	R
b13	TRMST	发送状态标志	0：总线空闲或接收中1：传输中或总线关闭状态。	R
b14	RECST	接收状态标志	0：总线空闲或传输中1：接收中。	R
b15	—	Reserved	读取值为0	R

NDST标志（NEWDATA状态标志）

无论MIER或MIER_FIFO寄存器的值如何，当MCTL_RXj(j=0到31)寄存器中的至少一个NEWDATA标志为1时，NDST标志设置为1。当所有NEWDATA标志为0时，NDST标志设置为0。

SDST标志（SENTDATA状态标志）

无论MIER或MIER_FIFO寄存器的值如何，当MCTL_TXj（j=0到31）寄存器中的至少一个SENTDATA标志为1时，SDST标志设置为1。当所有SENTDATA标志为0时，SDST标志设置为0。

RFST标志（接收FIFO状态标志）

当接收FIFO不为空时，RFST标志设置为1。当接收FIFO为空或选择正常邮箱模式时，RFST标志设置为0。

TFST flag (Transmit FIFO Status Flag)

The TFST flag is set to 1 when the transmit FIFO is not full. The TFST flag is set to 0 when the transmit FIFO is full or normal mailbox mode is selected.

NMLST flag (Normal Mailbox Message Lost Status Flag)

The NMLST flag is set to 1 when at least one MSGLOST flag in MCTL_RXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. The NMLST flag is set to 0 when all MSGLOST flags are 0.

FMLST flag (FIFO Mailbox Message Lost Status Flag)

The FMLST flag is set to 1 when the RFMLF flag in RFCR is 1, regardless of the value of MIER_FIFO. The FMLST flag is set to 0 when the RFMLF flag is 0.

TABST flag (Transmission Abort Status Flag)

The TABST flag is set to 1 when at least one TRMABT flag in the MCTL_TXj (j = 0 to 31) registers is 1, regardless of the value of the MIER or MIER_FIFO registers. The TABST flag is set to 0 when all TRMABT flags are 0.

EST flag (Error Status Flag)

The EST flag is set to 1 when at least one error is detected by the EIFR register, regardless of the value of the EIER register. The EST flag is set to 0 when no error is detected by EIFR.

RSTST flag (CAN Reset Status Flag)

The RSTST flag is set to 1 when the CAN module is in CAN reset mode. The RSTST flag is 0 when the CAN module is not in CAN reset mode. Even when the state changes from CAN reset mode to CAN sleep mode, the RSTST flag remains 1.

HLTST flag (CAN Halt Status Flag)

The HLTST flag is set to 1 when the CAN module is in CAN halt mode. The HLTST flag is set to 0 when the CAN module is not in CAN halt mode. Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST flag remains 1.

SLPST flag (CAN Sleep Status Flag)

The SLPST flag is set to 1 when the CAN module is in CAN sleep mode. The SLPST flag is set to 0 when the CAN module is not in CAN sleep mode.

EPST flag (Error-Passive Status Flag)

The EPST flag is set to 1 when the value in the TECR or RECR registers exceeds 127 and the CAN module is in the error-passive state (128 ≤ TEC < 256 or 128 ≤ REC < 256). The EPST flag is set to 0 when the CAN module is not in the error-passive state.

BOST flag (Bus-Off Status Flag)

The BOST flag is set to 1 when the value in the TECR register exceeds 255 and the CAN module is in the bus-off state (TEC ≥ 256). The BOST flag is set to 0 when the CAN module is not in the bus-off state.

TRMST flag (Transmit Status Flag)

The TRMST flag is set to 1 when the CAN module performs as a transmitter node or is in the bus-off state. The TRMST flag is set to 0 when the CAN module performs as a receiver node or is in the bus-idle state.

RECST flag (Receive Status Flag)

The RECST flag is set to 1 when the CAN module performs as a receiver node. The RECST flag is set to 0 when the CAN module performs as a transmitter node or is in the bus-idle state.

TFST标志（发送FIFO状态标志）

当发送FIFO未满时，TFST标志设置为1。当发送FIFO已满或选择正常邮箱模式时，TFST标志设置为0。

NMLST标志（正常邮箱消息丢失状态标志）

当MCTL_RXj(j=0to31)中的至少一个MSGLOST标志为1时，NMLST标志设置为1，无论MIER或MIER_FIFO。当所有MSGLOST标志为0时，NMLST标志设置为0。

FMLST标志（FIFO邮箱消息丢失状态标志）

当RFCR中的RFMLF标志为1时，无论MIER_FIFO的值如何，FMLST标志都设置为1。当RFMLF标志为0时，FMLST标志设置为0。

TABST标志（传输中止状态标志）

无论MIER或MIER_FIFO寄存器的值如何，当MCTL_TXj(j=0到31)寄存器中的至少一个TRMABT标志为1时，TABST标志设置为1。当所有TRMABT标志为0时，TABST标志设置为0。

EST标志（错误状态标志）

无论EIER寄存器的值如何，当EIFR寄存器检测到至少一个错误时，EST标志设置为1。当EIFR未检测到错误时，EST标志设置为0。

RSTST标志（CAN复位状态标志）

当CAN模块处于CAN复位模式时，RSTST标志设置为1。当CAN模块未处于CAN复位模式时，RSTST标志为0。即使状态从CAN复位模式更改为CAN睡眠模式，RSTST标志仍保持为1。

HLTST标志（CAN停止状态标志）

当CAN模块处于CAN暂停模式时，HLTST标志设置为1。当CAN模块未处于CAN暂停模式时，HLTST标志设置为0。即使状态从CAN停止模式更改为CAN睡眠模式，HLTST标志仍保持为1。

SLPST标志（CAN睡眠状态标志）

当CAN模块处于CAN睡眠模式时，SLPST标志设置为1。当CAN模块未处于CAN睡眠模式时，SLPST标志设置为0。

EPST标志（错误被动状态标志）

当TECR或RECR寄存器中的值超过127并且CAN模块处于错误被动状态（128≤TEC<256或128≤REC<256）时，EPST标志设置为1。当CAN模块不处于被动错误状态时，EPST标志设置为0。

BOST标志（总线关闭状态标志）

当TECR寄存器中的值超过255并且CAN模块处于总线关闭状态（TEC≥256）时，BOST标志设置为1。当CAN模块不处于总线关闭状态时，BOST标志设置为0。

TRMST标志（发送状态标志）

当CAN模块作为发送器节点运行或处于总线关闭状态时，TRMST标志设置为1。当CAN模块作为接收器节点运行或处于总线空闲状态时，TRMST标志设置为0。

RECST标志（接收状态标志）

当CAN模块作为接收器节点运行时，RECST标志设置为1。RECST标志设置为0，当CAN模块作为发送器节点运行或处于总线空闲状态。

31.2.16 Mailbox Search Mode Register (MSMR)

Address(es): CAN0.MSMR 4005 0853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	MBSM[1:0]	Mailbox Search Mode Select	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Write to the MSMR register in CAN operation mode or CAN halt mode.

MBSM[1:0] bits (Mailbox Search Mode Select)

The MBSM[1:0] bits select the search mode for the mailbox search function.

When the MBSM[1:0] bits are 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA flag in the MCTL_RXj (j = 0 to 31) registers for the normal mailbox, and the RFEST flag in the RFCR register.

When the MBSM[1:0] bits are 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA flag in the MCTL_TXj register.

When the MBSM[1:0] bits are 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST flag in the MCTL_RXj register for the normal mailbox, and the RFMLF flag in the RFCR register.

When the MBSM[1:0] bits are 11b, channel search mode is selected. In this mode, the search target is the CSSR register. See section 31.2.18, Channel Search Support Register (CSSR).

31.2.17 Mailbox Search Status Register (MSSR)

Address(es): CAN0.MSSR 4005 0852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	MBNST[4:0]	Search Result Mailbox Number Status	These bits output the smallest mailbox number that is found in each search mode selected in the MSMR register	R
b6, b5	—	Reserved	These bits are read as 0	R
b7	SEST	Search Result Status	0: Search result found 1: No search result.	R

MBNST[4:0] bits (Search Result Mailbox Number Status)

In all mailbox search modes, the MBNST[4:0] bits output the smallest mailbox number found. In receive mailbox search mode, transmit mailbox search mode, and message lost search mode, the value of the mailbox (search result to be output) is updated under the following conditions:

- When the respective NEWDATA, SENTDATA, or MSGLOST flag is set to 0 for a mailbox output by

31.2.16 邮箱搜索模式寄存器(MSMR)

Address(es): CAN0.MSMR 4005 0853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	MBSM[1:0]	邮箱搜索模式选择	b1b000：接收邮箱搜索模式01：发送邮箱搜索模式10：消息丢失搜索模式11：频道搜索模式。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

在CAN操作模式或CAN暂停模式下写入MSMR寄存器。

MBSM[1:0]位（邮箱搜索模式选择）

MBSM[1:0]位选择邮箱搜索功能的搜索模式。

当MBSM[1:0]位为00b时，选择接收邮箱搜索模式。在此模式下，搜索目标是普通邮箱的MCTL_RXj(j=0到31)寄存器中的NEWDATA标志，以及RFCR寄存器中的RFEST标志。

当MBSM[1:0]位为01b时，选择发送邮箱搜索模式。在这种模式下，搜索目标是MCTL_TXj寄存器中的SENTDATA标志。

当MBSM[1:0]位为10b时，选择消息丢失搜索模式。在这种模式下，搜索目标是正常邮箱的MCTL_RXj寄存器中的MSGLOST标志，以及RFCR寄存器中的RFMLF标志。

当MBSM[1:0]位为11b时，选择频道搜索模式。在这种模式下，搜索目标是CSSR寄存器。请参阅第31.2.18节，频道搜索支持寄存器(CSSR)。

31.2.17 邮箱搜索状态寄存器(MSSR)

Address(es): CAN0.MSSR 4005 0852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	MBNST[4:0]	搜索结果邮箱号码状态	这些位输出在MSMR寄存器中选择的每个搜索模式中找到的最小邮箱号	R
b6, b5	—	Reserved	这些位被读为0	R
b7	SEST	搜索结果状态	0：找到搜索结果1：没有搜索结果。	R

MBNST[4:0]位（搜索结果邮箱号码状态）

在所有邮箱搜索模式中，MBNST[4:0]位输出找到的最小邮箱号。在接收邮箱搜索模式、发送邮箱搜索模式和消息丢失搜索模式下，邮箱的值（要输出的搜索结果）在以下条件下更新：

- 当邮箱输出的相应NEWDATA、SENTDATA或MSGLOST标志设置为0时

MBNST[4:0]

- When the respective NEWDATA, SENTDATA or MSGLOST flag is set to 1 for a mailbox with a smaller number than that in MBNST[4:0].

If the MBSM[1:0] bits are set to 00b (receive mailbox search mode) or 10b (message lost search mode), the receive FIFO (mailbox 28) is output when it is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (0 to 23). If the MBSM[1:0] bits are set to 01b (transmit mailbox search mode), the transmit FIFO (mailbox 24) is not output. Table 31.6 lists the behavior of the MBNST[4:0] bits in FIFO mailbox mode.

In channel search mode, the MBNST[4:0] bits output the associated channel number. After the MSSR register is read by software, the next target channel number is output.

SEST bit (Search Result Status)

The SEST bit is set to 1 (no search result) when no associated mailbox is found after searching all the mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA flag is 1 for any mailbox. The SEST bit is set to 0 when at least one SENTDATA flag is 1. When the SEST bit is 1, the value of the MBNST[4:0] bits is undefined.

Table 31.6 Behavior of MBNST[4:0] bits in FIFO mailbox mode

MBSM[1:0] bits	Mailbox 24 (transmit FIFO)	Mailbox 28 (receive FIFO)
00b	Mailbox 24 is not output.	Mailbox 28 is output when no MCTL_RXj.NEWDATA flag for the normal mailboxes is set to 1 (no message is being stored or was stored to the mailbox) and the receive FIFO is not empty
01b		Mailbox 28 is not output
10b		Mailbox 28 is output when no MCTL_RXj.MSGLOST flag for the normal mailboxes is set to 1 (no message is overwritten or overrun) and the RFCR.RFMLF flag is set to 1 (receive FIFO message was lost) in the receive FIFO
11b		Mailbox 28 is not output

31.2.18 Channel Search Support Register (CSSR)

Address(es): CAN0.CSSR 4005 0851h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	When the value for the channel search is input, the channel number is output to the MSSR register	R/W

The bits that are set to 1 in the CSSR register are encoded by an 8/3 encoder (the LSB position has the higher priority) and output to the MBNST[4:0] bits in the MSSR register. The MSSR register outputs the updated value whenever it is read by software.

Write to the CSSR register only when the MSMR.MBSM[1:0] bits are 11b (channel search mode). Write to the CSSR register in CAN operation mode or CAN halt mode.

Figure 31.4 shows the write and read operations of the CSSR and MSSR registers.

MBNST[4:0]

- 当邮箱的相应NEWDATA、SENTDATA或MSGLOST标志设置为1时，邮箱的编号小于MBNST[4:0]中的编号。

如果MBSM[1:0]位设置为00b（接收邮箱搜索模式）或10b（邮件丢失搜索模式），则当接收FIFO（邮箱28）不为空且没有未读接收到的消息或在任何普通邮箱（0到23）中都没有丢失消息。如果MBSM[1:0]位设置为01b（发送邮箱搜索模式），则不输出发送FIFO（邮箱24）。表31.6列出了MBNST[4:0]位在FIFO邮箱模式下的行为。

在频道搜索模式下，MBNST[4:0]位输出相关的频道号。软件读取MSSR寄存器后，输出下一个目标通道号。

SEST位（搜索结果状态）

当搜索所有邮箱后未找到相关邮箱时，SEST位设置为1（无搜索结果）。例如，在发送邮箱搜索模式中，当没有任何邮箱的SENTDATA标志为1时，SEST位设置为1。当至少一个SENTDATA标志为1时，SEST位设置为0。当SEST位为1时，MBNST[4:0]位的值未定义。

Table 31.6 FIFO邮箱模式下MBNST[4:0]位的行为

MBSM[1:0] bits	Mailbox 24 (transmit FIFO)	Mailbox 28 (receive FIFO)
00b	邮箱24不输出。	当正常邮箱的MCTL_RXj.NEWDATA标志没有设置为1（没有消息正在存储或存储到邮箱）并且接收FIFO不为空时，输出邮箱28
01b		28号邮箱不输出
10b		当正常邮箱的MCTL_RXj.MSGLOST标志没有设置为1（没有消息被覆盖或溢出）并且RFCR.RFMLF标志在接收中设置为1（接收FIFO消息丢失）时，输出邮箱28 FIFO
11b		28号邮箱不输出

31.2.18 频道搜索支持寄存器(CSSR)

Address(es): CAN0.CSSR 4005 0851h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	输入通道搜索值时，通道号输出到MSSR寄存器	R/W

CSSR寄存器中设置为1的位由83编码器（LSB位置具有较高优先级）编码并输出到MSSR寄存器中的MBNST[4:0]位。每当软件读取时，MSSR寄存器就会输出更新的值。

仅当MSMR.MBSM[1:0]位为11b（通道搜索模式）时才写入CSSR寄存器。在CAN操作模式或CAN暂停模式下写入CSSR寄存器。

图31.4显示了CSSR和MSSR寄存器的写和读操作。

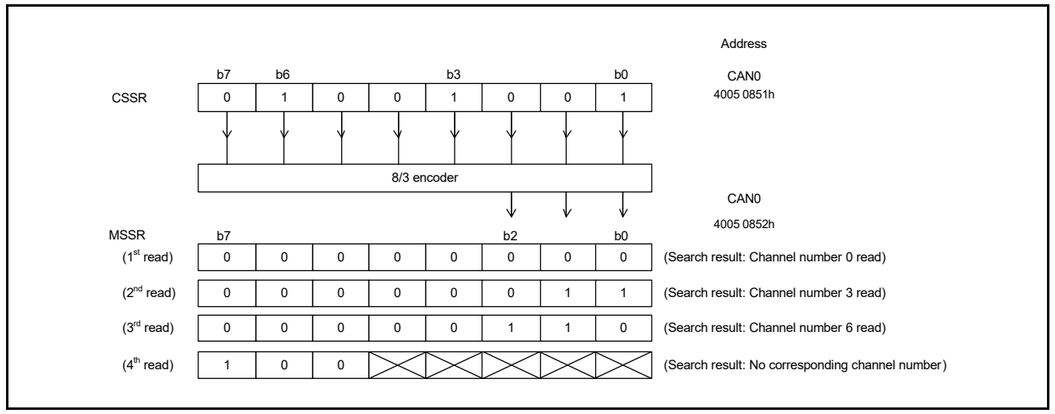


Figure 31.4 Write and read operations of the CSSR and MSSR registers

The value of the CSSR register is also updated whenever the MSSR register is read. On this read, the value prior to conversion by the 8/3 encoder can be read.

31.2.19 Acceptance Filter Support Register (AFSR)

Address(es): CAN0.AFSR 4005 0856h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b15 to b0	After the standard ID of a received message is written, the value converted for data table search can be read	R/W

Note: Write to AFSR in CAN operation mode or CAN halt mode.

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs that you create are set to be valid or invalid in bit units. When the AFSR register is written with data in 16-bit units including the SID[10:0] bit in the MBj_ID (j = 0 to 31) register, in which a received standard ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

The ASU is enabled in the following cases:

- When the IDs to be received cannot be masked by the acceptance filter, for example if the IDs to be received are 078h, 087h, and 111h
- When there are too many IDs to receive and the software filtering time is expected to be shortened.

Note: The AFSR register cannot be set in CAN reset mode.

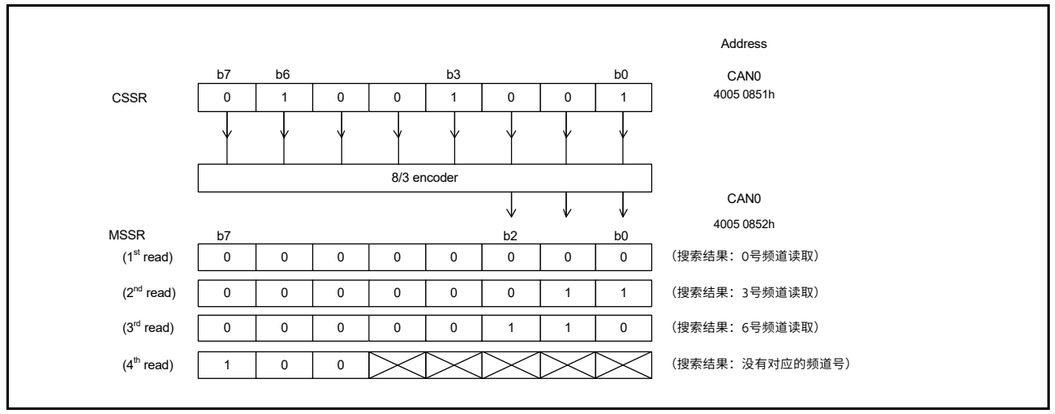


Figure 31.4 CSSR和MSSR寄存器的写和读操作

每当读取MSSR寄存器时，CSSR寄存器的值也会更新。在此读取中，可以读取83编码器转换之前的值。

31.2.19 接受过滤器支持寄存器(AFSR)

Address(es): CAN0.AFSR 4005 0856h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b15 to b0	接收报文的标准ID写入后，即可读取数据查表转换后的值	R/W

Note: 在CAN操作模式或CAN暂停模式下写入AFSR。

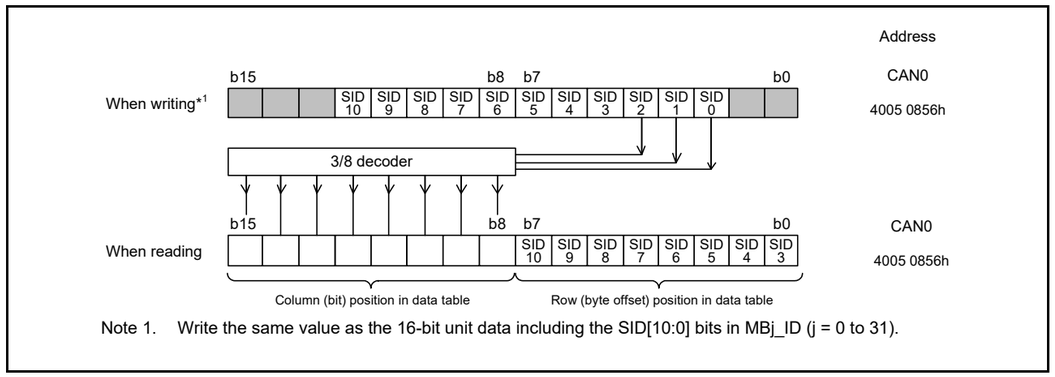
验收滤波器支持单元(ASU)可用于数据表（8位×256）搜索。在数据表中，您创建的所有标准ID均以位为单位设置为有效或无效。当AFSR寄存器以16位为单位写入数据时，包括存储接收到的标准ID的MBj_ID(j=0至31)寄存器中的SID[10:0]位，解码的行（字节偏移）可以读取数据表搜索的位置和列（位）位置。ASU只能用于标准（11位）ID。

ASU在以下情况下启用：

- 当要接收的ID不能被接受过滤器屏蔽时，例如要接收的ID为078h、087h和111h
- 当接收的ID过多，预计软件过滤时间会缩短时。

Note: 在CAN复位模式下不能设置AFSR寄存器。

Figure 31.5 shows the write and read operation in the AFSR register.



Note 1. Write the same value as the 16-bit unit data including the SID[10:0] bits in MBj_ID (j = 0 to 31).

Figure 31.5 Write and read operations in the AFSR register

31.2.20 Error Interrupt Enable Register (EIER)

Address(es): CAN0.EIER 4005 084Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIE	Bus Error Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b1	EWIE	Error-Warning Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b2	EPIE	Error-Passive Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b3	BOEIE	Bus-Off Entry Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b4	BORIE	Bus-Off Recovery Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b5	ORIE	Overrun Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b6	OLIE	Overload Frame Transmit Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b7	BLIE	Bus Lock Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W

The EIER register independently enables or disables the error interrupt for each error interrupt source. Write to the EIER register in CAN reset mode.

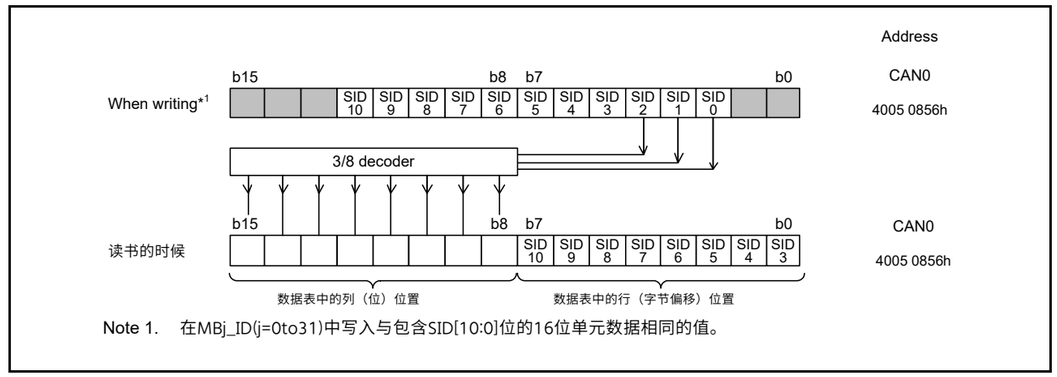
BEIE bit (Bus Error Interrupt Enable)

When the BEIE bit is 0, no error interrupt request is generated even if the BEIF flag in the EIFR register is 1. When the BEIE bit is 1, an error interrupt request is generated if the BEIF flag is set to 1.

EWIE bit (Error-Warning Interrupt Enable)

When the EWIE bit is 0, no error interrupt request is generated even if the EWIF flag in the EIFR register is 1. When the

图31.5显示了AFSR寄存器中的写和读操作。



Note 1. 在MBj_ID(j=0to31)中写入与包含SID[10:0]位的16位单元数据相同的值。

Figure 31.5 AFSR寄存器中的写和读操作

31.2.20 错误中断使能寄存器(EIER)

Address(es): CAN0.EIER 4005 084Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BEIE	总线错误中断使能	0：禁用中断1：启用中断。	R/W
b1	EWIE	错误警告中断使能	0：禁用中断1：启用中断。	R/W
b2	EPIE	错误被动中断使能	0：禁用中断1：启用中断。	R/W
b3	BOEIE	总线关闭进入中断使能	0：禁用中断1：启用中断。	R/W
b4	BORIE	总线关闭恢复中断使能	0：禁用中断1：启用中断。	R/W
b5	ORIE	溢出中断使能	0：禁用中断1：启用中断。	R/W
b6	OLIE	过载帧发送中断 Enable	0：禁用中断1：启用中断。	R/W
b7	BLIE	总线锁定中断使能	0：禁用中断1：启用中断。	R/W

EIER寄存器独立启用或禁用每个错误中断源的错误中断。在CAN复位模式下写入EIER寄存器。

BEIE位（总线错误中断使能）

当BEIE位为0时，即使EIFR寄存器中的BEIF标志为1，也不会产生错误中断请求。当BEIE位为1，如果BEIF标志设置为1，则产生错误中断请求。

EWIE位（错误警告中断使能）

当EWIE位为0时，即使EIFR寄存器中的EWIF标志为1，也不会产生错误中断请求。当

EWIE bit is 1, an error interrupt request is generated if the EWIF flag is set to 1.

EPIE bit (Error-Passive Interrupt Enable)

When the EPIE bit is 0, no error interrupt request is generated even if the EPIF flag in the EIFR register is 1. When the EPIE bit is 1, an error interrupt request is generated if the EPIF flag is set to 1.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE bit is 0, no error interrupt request is generated even if the BOEIF flag in the EIFR register is 1. When the BOEIE bit is 1, an error interrupt request is generated if the BOEIF flag is set to 1.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE bit is 0, no error interrupt request is generated even if the BORIF flag in the EIFR register is 1. When the BORIE bit is set to 1, an error interrupt request is generated if the BORIF flag is set to 1.

ORIE bit (Overrun Interrupt Enable)

When the ORIE bit is 0, no error interrupt request is generated even if the ORIF flag in the EIFR register is 1. When the ORIE bit is 1, an error interrupt request is generated if the ORIF flag is set to 1.

OLIE bit (Overload Frame Transmit Interrupt Enable)

When the OLIE bit is 0, no error interrupt request is generated even if the OLIF flag in the EIFR register is 1. When the OLIE bit is 1, an error interrupt request is generated if the OLIF flag is set to 1.

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE bit is 0, no error interrupt request is generated even if the BLIF flag in the EIFR register is 1. When the BLIE bit is 1, an error interrupt request is generated if the BLIF flag is set to 1.

31.2.21 Error Interrupt Factor Judge Register (EIFR)

Address(es): CAN0.EIFR 4005 084Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIF	Bus Error Detect Flag	0: No bus error detected 1: Bus error detected.	R/W
b1	EWIF	Error-Warning Detect Flag	0: No error-warning detected 1: Error-warning detected.	R/W
b2	EPIF	Error-Passive Detect Flag	0: No error-passive detected 1: Error-passive detected.	R/W
b3	BOEIF	Bus-Off Entry Detect Flag	0: No bus-off entry detected 1: Bus-off entry detected.	R/W
b4	BORIF	Bus-Off Recovery Detect Flag	0: No bus-off recovery detected 1: Bus-off recovery detected.	R/W
b5	ORIF	Receive Overrun Detect Flag	0: No receive overrun detected 1: Receive overrun detected.	R/W
b6	OLIF	Overload Frame Transmission Detect Flag	0: No overload frame transmission detected 1: Overload frame transmission detected.	R/W
b7	BLIF	Bus Lock Detect Flag	0: No bus lock detected 1: Bus lock detected.	R/W

If an event associated with an EIFR flag occurs, the associated bit in EIFR is set to 1, regardless of the setting of EIER.

EWIE位为1，如果EWIF标志设置为1，则产生错误中断请求。

EPIE位（错误被动中断使能）

当EPIE位为0时，即使EIFR寄存器中的EPIF标志为1，也不会产生错误中断请求。当EPIE位为1，如果EPIF标志设置为1，则产生错误中断请求。

BOEIE位（总线关闭进入中断使能）

当BOEIE位为0时，即使EIFR寄存器中的BOEIF标志为1，也不会产生错误中断请求。当BOEIE位为1时，如果将BOEIF标志设置为1，则产生错误中断请求。

BORIE位（总线关闭恢复中断使能）

当BORIE位为0时，即使EIFR寄存器中的BORIF标志为1，也不会产生错误中断请求。当BORIE位被设置为1时，如果BORIF标志被设置为1，则产生错误中断请求。

ORIE位（溢出中断使能）

当ORIE位为0时，即使EIFR寄存器中的ORIF标志为1，也不会产生错误中断请求。ORIE位为1，如果ORIF标志设置为1，则产生错误中断请求。

OLIE位（过载帧发送中断使能）

当OLIE位为0时，即使EIFR寄存器中的OLIF标志为1，也不会产生错误中断请求。当OLIE位为1，如果OLIF标志设置为1，则产生错误中断请求。

BLIE位（总线锁定中断使能）

当BLIE位为0时，即使EIFR寄存器中的BLIF标志为1，也不会产生错误中断请求。当BLIE位为1，如果BLIF标志设置为1，则产生错误中断请求。

31.2.21 错误中断因素判断寄存器（EIFR）

Address(es): CAN0.EIFR 4005 084Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BEIF	总线错误检测标志	0：未检测到总线错误1 ：检测到总线错误。	R/W
b1	EWIF	错误警告检测标志	0：未检测到错误警告1：检 测到错误警告。	R/W
b2	EPIF	错误被动检测标志	0：未检测到被动错误1：检 测到被动错误。	R/W
b3	BOEIF	总线关闭进入检测标志	0：未检测到总线关闭条目1 ：检测到总线关闭条目。	R/W
b4	BORIF	总线关闭恢复检测标志	0：未检测到总线关闭恢复1： 检测到总线关闭恢复。	R/W
b5	ORIF	接收溢出检测标志	0：未检测到接收溢出1：检测 到接收溢出。	R/W
b6	OLIF	过载帧传输 检测标志	0：未检测到过载帧传输1：检测到过载帧传 输。	R/W
b7	BLIF	总线锁定检测标志	0：未检测到总线锁定1 ：检测到总线锁定。	R/W

如果发生与EIFR标志相关的事件，则EIFR中的相关位设置为1，而与EIER的设置无关。

Clear the bits to 0 through a software write. If a bit is set to 1 at the same time that software clears it, the bit becomes 1. When setting a single bit to 0 in software, use the transfer instruction (MOV) to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect on these bit values.

BEIF flag (Bus Error Detect Flag)

The BEIF flag is set to 1 when a bus error is detected.

EWIF flag (Error-Warning Detect Flag)

The EWIF flag is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95. This flag is set to 1 only when the REC or TEC value initially exceeds 95. If software writes 0 to this flag while the REC or TEC value remains greater than 95, the EWIF flag is not set to 1 until the REC or TEC value goes below 95, and then exceeds 95 again.

EPIF flag (Error-Passive Detect Flag)

The EPIF flag is set to 1 when the CAN error state becomes error-passive, when the REC or TEC value exceeds 127. This flag is set to 1 only when the REC or TEC value initially exceeds 127. If software writes 0 to this flag while the REC or TEC value remains greater than 127, the EPIF flag is not set to 1 until the REC or TEC value goes below 127, and then exceeds 127 again.

BOEIF flag (Bus-Off Entry Detect Flag)

The BOEIF flag is set to 1 when the CAN error state becomes bus-off, while the TEC value exceeds 255. The BOEIF flag is also set to 1 when the BOM[1:0] bits in CTLR are 01b (automatic entry to CAN halt mode on bus-off entry) and the CAN module enters the bus-off state.

BORIF flag (Bus-Off Recovery Detect Flag)

The BORIF flag is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive recessive bits 128 times in the following conditions:

- When the BOM[1:0] bits in CTLR are 00b
- When the BOM[1:0] bits in CTLR are 10b
- When the BOM[1:0] bits in CTLR are 11b.

The BORIF flag is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:

- When the CANM[1:0] bits in CTLR are set to 01b or 11b (CAN reset mode)
- When the RBOC bit in CTLR is set to 1 (forced return from bus-off)
- When the BOM[1:0] bits in CTLR are set to 01b
- When the BOM[1:0] bits in CTLR are set to 11b and the CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) before normal recovery occurs.

Table 31.7 shows the behavior of the BOEIF and BORIF flags for each CTLR.BOM[1:0] bit setting.

Table 31.7 Behavior of BOEIF and BORIF flags according to CTLR.BOM[1:0] bit setting

BOM[1:0] bits	BOEIF flag	BORIF flag
00b	Set to 1 on entry to the bus-off state	Set to 1 on exit from the bus-off state
01b		Do not set to 1
10b		Set to 1 on exit from the bus-off state
11b		Set to 1 if normal bus-off recovery occurs before the CANM[1:0] bits are set to 10b (CAN halt mode)

ORIF flag (Receive Overrun Detect Flag)

The ORIF flag is set to 1 when a receive overrun occurs. This flag is not set to 1 in overwrite mode. In this mode, a reception complete interrupt request is generated if an overwrite condition occurs and the ORIF flag is not set to 1.

通过软件写入将这些位清除为0。如果在软件清零的同时将某个位设置为1，则该位变为1。在软件中将单个位设置为0时，使用传输指令(MOV)确保只有指定的位设置为0，并且其他位设置为1。写入1对这些位值没有影响。

BEIF标志（总线错误检测标志）

当检测到总线错误时，BEIF标志设置为1。

EWIF标志（错误警告检测标志）

当接收错误计数器(REC)或发送错误计数器(TEC)的值超过95时，EWIF标志设置为1。仅当REC或TEC值最初超过95时，该标志才设置为1。如果软件将0写入当REC或TEC值保持大于95时，EWIF标志不会设置为1，直到REC或TEC值低于95，然后再次超过95。

EPIF标志（错误被动检测标志）

当CAN错误状态变为被动错误时，当REC或TEC值超过127时，EPIF标志设置为1。仅当REC或TEC值最初超过127时，此标志设置为1。如果软件将0写入此标志而
REC或TEC值保持大于127，EPIF标志不会设置为1，直到REC或TEC值低于127，然后再次超过127。

BOEIF标志（总线关闭进入检测标志）

当CAN错误状态变为总线关闭时，BOEIF标志设置为1，而TEC值超过255。当CTLR中的BOM[1:0]位为01b（自动进入CAN进入总线关闭时的暂停模式）并且CAN模块进入总线关闭状态。

BORIF标志（总线关闭恢复检测标志）

当CAN模块在以下情况下通过检测11个连续的隐性位128次从总线关闭状态正常恢复时，BORIF标志设置为1：

- CTLR的BOM[1:0]位为00b时
- CTLR中BOM[1:0]位为10b时
- 当CTLR的BOM[1:0]位为11b时。

如果CAN模块在以下情况下从总线关闭状态恢复，则BORIF标志不设置为1：

- 当CTLR中的CANM[1:0]位设置为01b或11b时（CAN复位模式）
- 当CTLR的RBOC位设置为1时（从总线关闭强制返回）
- 当CTLR中的BOM[1:0]位设置为01b
- 当CTLR中的BOM[1:0]位设置为11b且CTLR中的CANM[1:0]位设置为10b（CAN停止模式）时，才会发生正常恢复。

表31.7显示了每个CTLR.BOM[1:0]位设置的BOEIF和BORIF标志的行为。

Table 31.7 根据CTLR.BOM[1:0]位设置的BOEIF和BORIF标志的行为

BOM[1:0] bits	BOEIF flag	BORIF flag
00b	进入总线关闭状态时设置为1	退出总线关闭状态时设置为1
01b		不要设置为1
10b		退出总线关闭状态时设置为1
11b		如果在CANM[1:0]位设置为10b（CAN停止模式）之前发生正常的总线关闭恢复，则设置为1

ORIF标志（接收溢出检测标志）

当发生接收溢出时，ORIF标志设置为1。此标志在覆盖模式下不设置为1。在此模式下，如果发生覆盖条件且ORIF标志未设置为1，则生成接收完成中断请求。

In overrun mode with normal mailbox mode, if an overrun occurs in any of the mailboxes 0 through 31, the ORIF flag is set to 1. In overrun mode with FIFO mailbox mode, if an overrun occurs in any of the mailboxes 0 through 23, or the receive FIFO, the ORIF flag is set to 1.

OLIF flag (Overload Frame Transmission Detect Flag)

The OLIF flag is set to 1 if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception.

BLIF flag (Bus Lock Detect Flag)

The BLIF flag is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF flag is set to 1, the 32 consecutive dominant bits are detected again in either of the following conditions:

- Recessive bits are detected after the BLIF flag changes from 0 to 1
- The CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again, after the BLIF flag changes from 0 to 1.

31.2.22 Receive Error Count Register (RECR)

Address(es): CAN0.RECR 4005 084Eh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Receive error count function. RECR increments or decrements the counter value based on the error status of the CAN module during reception.	R

The RECR register indicates the value of the receive error counter. See the CAN specification (ISO11898-1) for the increment or decrement conditions of the receive error counter. The value of the RECR register in the bus-off state is undefined.

31.2.23 Transmit Error Count Register (TECR)

Address(es): CAN0.TECR 4005 084Fh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Transmit error count function. TECR increments or decrements the counter value based on the error status of the CAN module during transmission.	R

The TECR register indicates the value of the transmit error counter. See the CAN specification (ISO11898-1) for the increment and decrement conditions of the transmit error counter. The value of the TECR register in the bus-off state is undefined.

在具有正常邮箱模式的溢出模式中，如果在任何邮箱0到31中发生溢出，则ORIF标志设置为1。在具有FIFO邮箱模式的溢出模式中，如果在任何邮箱0到23中发生溢出，或接收FIFO，ORIF标志设置为1。

OLIF标志（过载帧传输检测标志）

如果在CAN模块执行发送或接收时检测到过载帧的发送条件，则OLIF标志设置为1。

BLIF标志（总线锁定检测标志）

如果在CAN模块处于CAN操作模式时在CAN总线上检测到32个连续显性位，则BLIF标志设置为1。

将BLIF标志设置为1后，在以下任一情况下再次检测到32个连续的显性位：

- BLIF标志从0变为1后检测到隐性位
- CAN模块进入CAN复位模式或CAN暂停模式，然后再次进入CAN操作模式，经过BLIF标志从0变为1。

31.2.22 接收错误计数寄存器(RECR)

Address(es): CAN0.RECR 4005 084Eh

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	接收错误计数功能。RECR根据错误状态递增或递减计数器值接收期间的CAN模块。	R

RECR寄存器指示接收错误计数器的值。有关接收错误计数器的递增或递减条件，请参见CAN规范(ISO11898-1)。总线关闭状态下的RECR寄存器的值是未定义的。

31.2.23 发送错误计数寄存器(TECR)

Address(es): CAN0.TECR 4005 084Fh

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	发送错误计数功能。TECR根据错误状态递增或递减计数器值CAN模块在传输过程中。	R

TECR寄存器指示发送错误计数器的值。有关发送错误计数器的递增和递减条件，请参见CAN规范(ISO11898-1)。总线关闭状态下的TECR寄存器的值未定义。

31.2.24 Error Code Store Register (ECSR)

Address(es): CAN0.ECSR 4005 0850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEF	Stuff Error Flag*1,*2	0: No stuff error detected 1: Stuff error detected.	R/W
b1	FEF	Form Error Flag*1,*2	0: No form error detected 1: Form error detected.	R/W
b2	AEF	ACK Error Flag*1,*2	0: No ACK error detected 1: ACK error detected.	R/W
b3	CEF	CRC Error Flag*1,*2	0: No CRC error detected 1: CRC error detected.	R/W
b4	BE1F	Bit Error (recessive) Flag*1,*2	0: No bit error (recessive) detected 1: Bit error (recessive) detected.	R/W
b5	BE0F	Bit Error (dominant) Flag*1,*2	0: No bit error (dominant) detected 1: Bit error (dominant) detected.	R/W
b6	ADEF	ACK Delimiter Error Flag*1,*2	0: No ACK delimiter error detected 1: ACK delimiter error detected.	R/W
b7	EDPM	Error Display Mode Select*3,*4	0: Output of first detected error code 1: Output of accumulated error code.	R/W

Note 1. Writing 1 has no effect on these bit values.
Note 2. To write 0 to the SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF bits, use the transfer (MOV) instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
Note 3. Write to the EDPM bit in CAN reset mode or CAN halt mode.
Note 4. If more than one error condition is detected simultaneously, all the related bits are set to 1.

The ECSR register can be used to monitor whether an error occurred on the CAN bus. See the CAN specification (ISO11898-1) for the conditions when each error occurs.

Clear all the bits except for the EDPM bit to 0 through a software write. If an ECSR bit is set to 1 by the CAN module at the same time that software writes 0 to it, the bit is set to 1.

SEF flag (Stuff Error Flag)

The SEF flag is set to 1 when a stuff error is detected.

FEF flag (Form Error Flag)

The FEF flag is set to 1 when a form error is detected.

AEF flag (ACK Error Flag)

The AEF flag is set to 1 when an ACK error is detected.

CEF flag (CRC Error Flag)

The CEF flag is set to 1 when a CRC error is detected.

BE1F flag (Bit Error (recessive) Flag)

The BE1F flag is set to 1 when a recessive bit error is detected.

BE0F flag (Bit Error (dominant) Flag)

The BE0F flag is set to 1 when a dominant bit error is detected.

31.2.24 错误代码存储寄存器(ECSR)

Address(es): CAN0.ECSR 4005 0850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SEF	填充错误标志 *1,*2	0：未检测到填充错误1 ：检测到填充错误。	R/W
b1	FEF	表单错误标志 *1,*2	0：未检测到表单错误1 ：检测到表单错误。	R/W
b2	AEF	ACK错误标志 *1,*2	0：未检测到ACK错误1： 检测到ACK错误。	R/W
b3	CEF	CRC错误标志 *1,*2	0：未检测到CRC错误1： 检测到CRC错误。	R/W
b4	BE1F	位错误（隐性）标志 *1,*2	0：未检测到位错误（隐性）1：检 测到位错误（隐性）。	R/W
b5	BE0F	位错误（显性）标志 *1,*2	0：未检测到位错误（显性）1：检 测到位错误（显性）。	R/W
b6	ADEF	ACK定界符错误标志 *1,*2	0：未检测到ACK分隔符错误1：检 测到ACK分隔符错误。	R/W
b7	EDPM	错误显示模式选择 *3,*4	0：输出第一个检测到的错误代码1： 输出累积错误代码。	R/W

Note 1. 写1对这些位值没有影响。
Note 2. 要将0写入SEF、FEF、AEF、CEF、BE1F、BE0F和ADEF位，请使用传输(MOV)指令确保仅将指定位设置为0，而将其他位设置为1。
Note 3. 在CAN复位模式或CAN暂停模式下写入EDPM位。
Note 4. 如果同时检测到多个错误条件，则所有相关位都设置为1。

ECSR寄存器可用于监控CAN总线是否发生错误。有关每个错误发生的条件，请参见CAN规范(ISO11898-1)。

通过软件写入将除EDPM位之外的所有位清零。如果在软件向其写入0的同时CAN模块将ECSR位设置为1，则该位设置为1。

SEF标志（东西错误标志）

当检测到填充错误时，SEF标志设置为1。

FEF标志（表单错误标志）

当检测到表单错误时，FEF标志设置为1。

AEF标志（ACK错误标志）

当检测到ACK错误时，AEF标志设置为1。

CEF标志（CRC错误标志）

当检测到CRC错误时，CEF标志设置为1。

BE1F标志（位错误（隐性）标志）

当检测到隐性位错误时，BE1F标志设置为1。

BE0F标志（位错误（显性）标志）

当检测到显性位错误时，BE0F标志设置为1。

ADEF flag (ACK Delimiter Error Flag)

The ADEF flag is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM bit (Error Display Mode Select)

The EDPM bit selects the output mode of ECSR. When the EDPM bit is set to 0, the ECSR register outputs the first error code. When the EDPM bit is set to 1, the ECSR register outputs the accumulated error code.

31.2.25 Time Stamp Register (TSR)

Address(es): CAN0.TSR 4005 0854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	Free-running counter value for the time stamp function	R

Note: Read the TSR register in 16-bit units.

Reading the TSR register returns the current value of the 16-bit free-running time stamp counter. The time stamp counter reference clock is configured in the TSPS[1:0] bits in CTLR. The counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode. The time stamp counter value is stored in the TSL[7:0] and TSH[7:0] bits in the MBj_TS register when a received message is stored in a receive mailbox.

31.2.26 Test Control Register (TCR)

Address(es): CAN0.TCR 4005 0858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTE	CAN Test Mode Enable	0: Disable CAN test mode 1: Enable CAN test mode.	R/W
b2, b1	TSTM[1:0]	CAN Test Mode Select	b2 b1 0 0: Not CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback) 1 1: Self-test mode 1 (internal loopback).	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TCR register controls the CAN test mode. Write to the TCR register in CAN halt mode only.

(1) Listen-only mode

The CAN specification (ISO11898-1) recommends an optional bus monitoring mode. In listen-only mode, valid data frames and valid remote frames can be received. However, only the recessive bits can be sent on the CAN bus. The ACK bit, overload flag, and active error flag cannot be sent. Listen-only mode can be used for baud rate detection. Do not request transmission from any mailboxes in listen-only mode.

Figure 31.6 shows the connection when listen-only mode is selected.

ADEF标志（ACK分隔符错误标志）

当在传输过程中使用ACK定界符检测到格式错误时，ADEF标志设置为1。

EDP M位（错误显示模式选择）

EDP M位选择ECSR的输出模式。当EDPM位设置为0时，ECSR寄存器输出第一个错误代码。当EDPM位设置为1时，ECSR寄存器输出累积的错误代码。

31.2.25 时间戳寄存器(TSR)

Address(es): CAN0.TSR 4005 0854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	时间戳功能的自由运行计数器值	R

Note: 以16位为单位读取TSR寄存器。

读取TSR寄存器返回16位自由运行时间戳计数器的当前值。时间戳计数器参考时钟在CTLR的TSPS[1:0]位中配置。计数器在CAN睡眠模式和CAN暂停模式下停止，并在CAN复位模式下初始化。当接收到的消息存储在接收邮箱中时，时间戳计数器值存储在MBj_TS寄存器的TSL[7:0]和TSH[7:0]位中。

31.2.26 测试控制寄存器(TCR)

Address(es): CAN0.TCR 4005 0858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSTE	CAN测试模式启用	0：禁用CAN测试模式1： 启用CAN测试模式。	R/W
b2, b1	TSTM[1:0]	CAN测试模式选择	b2b100：非CAN测试模式01：只听模式1 0：自测模式0（外部环回）11：自测模式 1（内部环回）。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TCR寄存器控制CAN测试模式。仅在CAN暂停模式下写入TCR寄存器。

(1) Listen-only mode

CAN规范(ISO11898-1)推荐一种可选的总线监控模式。在只听模式下，可以接收到有效的数据帧和有效的远程帧。但是，只能在CAN总线上发送隐性位。不能发送ACK位、过载标志和活动错误标志。只听模式可用于波特率检测。不要在只听模式下从任何邮箱请求传输。

图31.6显示了选择只听模式时的连接。

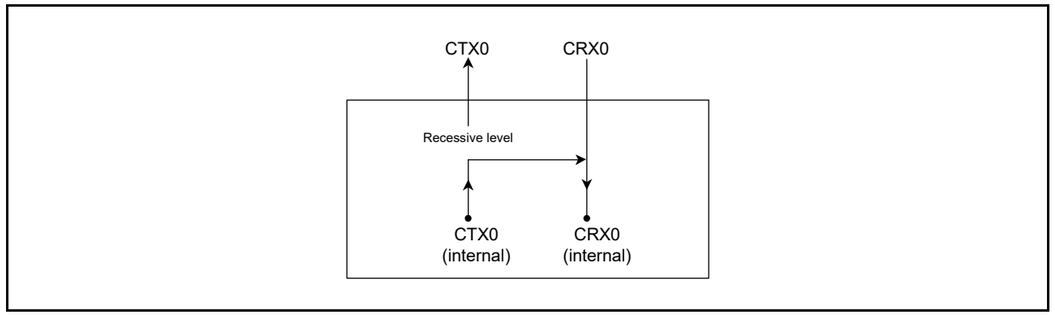


Figure 31.6 Connection when listen-only mode is selected

(2) Self-test mode 0 (external loopback)

Self-test mode 0 is provided for CAN transceiver tests.

In this mode, the protocol module treats its own transmitted messages as those received by the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol module generates the ACK bit. Connect the CTX0 and CRX0 pins to the transceiver.

Figure 31.7 shows the connection when self-test mode 0 is selected.

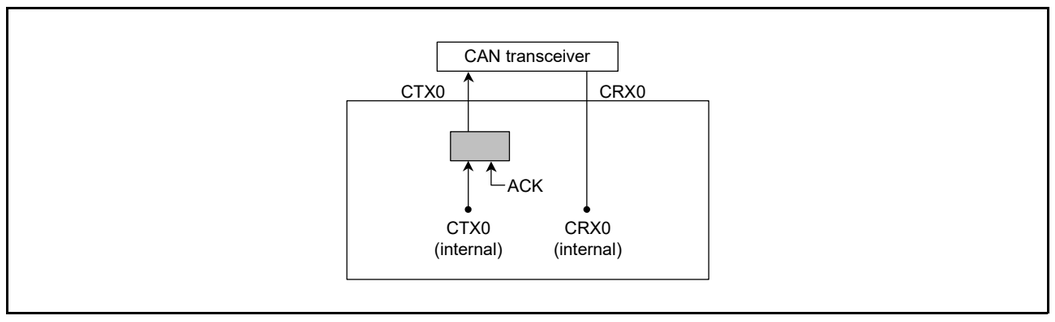


Figure 31.7 Connection when self-test mode 0 is selected

(3) Self-test mode 1 (internal loopback)

Self-test mode 1 is provided for self-test functions. In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CTX0 pin to the internal CRX0 pin. The input value of the external CRX0 pin is ignored. The external CTX0 pin outputs only recessive bits. The CTX0 and CRX0 pins are not required to be connected to the CAN bus or any external device.

Figure 31.8 shows the connection when self-test mode 1 is selected.

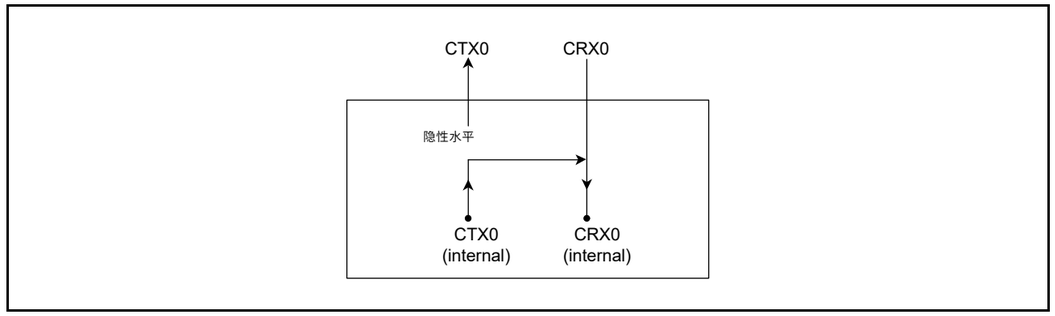


Figure 31.6 选择只听模式时的连接

(2) Self-test mode 0 (external loopback)

自测模式0用于CAN收发器测试。

在该模式下，协议模块将自己发送的报文视为CAN收发器接收到的报文，并将其存储到接收邮箱中。为独立于外部刺激，协议模块生成ACK位。将CTX0和CRX0引脚连接到收发器。

图31.7显示了选择自检模式0时的连接。

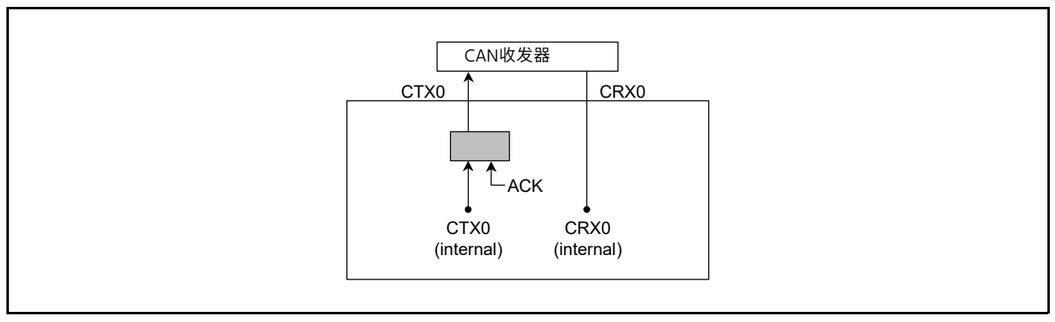


Figure 31.7 选择自检模式0时的连接

(3) Self-test mode 1 (internal loopback)

自检模式1用于自检功能。在这种模式下，协议控制器将其发送的消息视为接收的消息，并将它们存储到接收邮箱中。为了独立于外部刺激，协议控制器生成ACK位。

在自检模式1中，协议控制器执行从内部CTX0引脚到内部的内部反馈
CRX0引脚。外部CRX0引脚的输入值被忽略。外部CTX0引脚仅输出隐性位。这
CTX0和CRX0引脚不需要连接到CAN总线或任何外部设备。

图31.8显示了选择自检模式1时的连接。

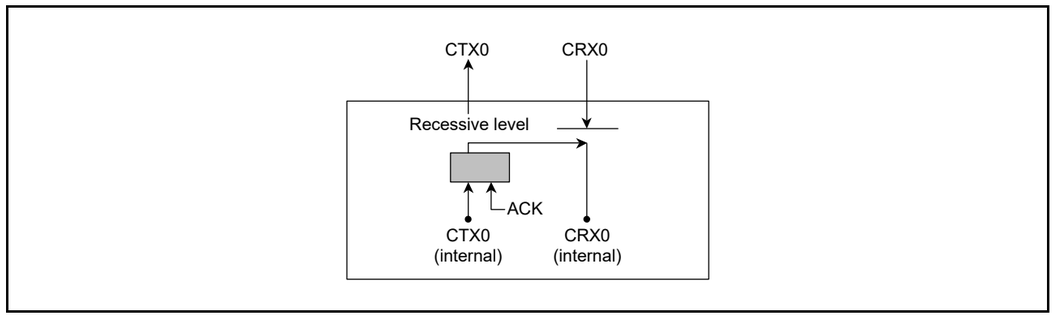


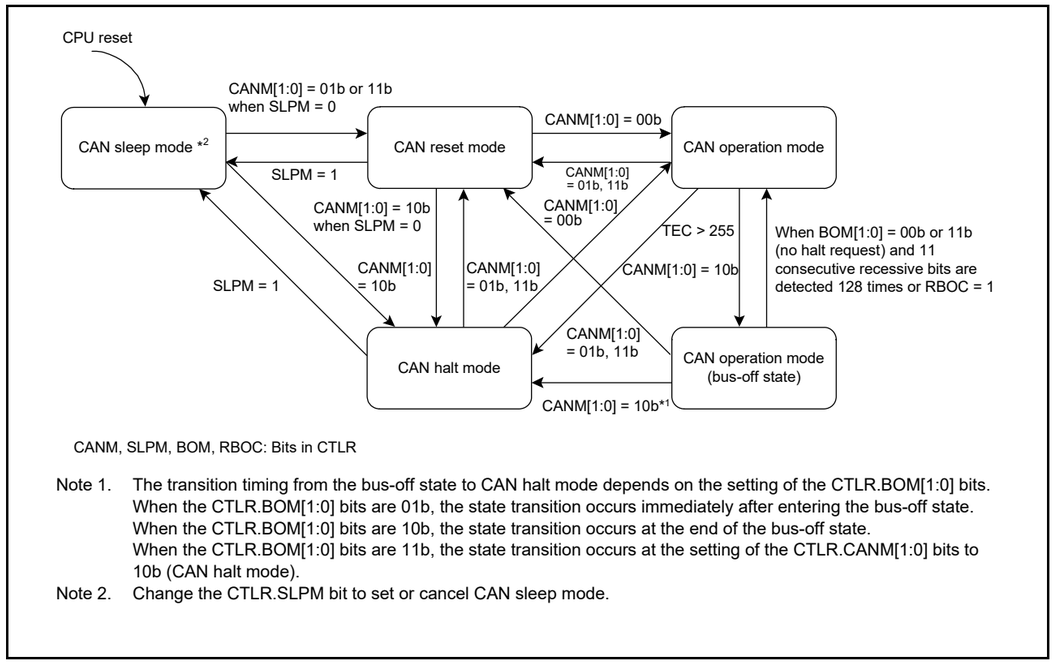
Figure 31.8 Connection when self-test mode 1 is selected

31.3 Modes of Operation

The CAN module operation modes include:

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode.

Figure 31.9 shows the transition between different modes of operation.



Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
When the CTLR.BOM[1:0] bits are 01b, the state transition occurs immediately after entering the bus-off state.
When the CTLR.BOM[1:0] bits are 10b, the state transition occurs at the end of the bus-off state.
When the CTLR.BOM[1:0] bits are 11b, the state transition occurs at the setting of the CTLR.CANM[1:0] bits to 10b (CAN halt mode).

Note 2. Change the CTLR.SLPM bit to set or cancel CAN sleep mode.

Figure 31.9 Transition between different modes of operation

31.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration. When the CTLR.CANM[1:0] bits are set to 01b or 11b, the CAN module enters CAN reset mode. The STR.RSTST flag is then set to 1. Do not change the

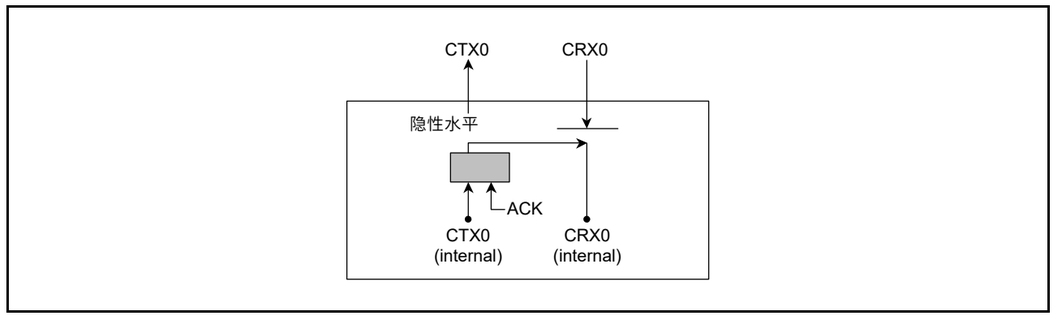


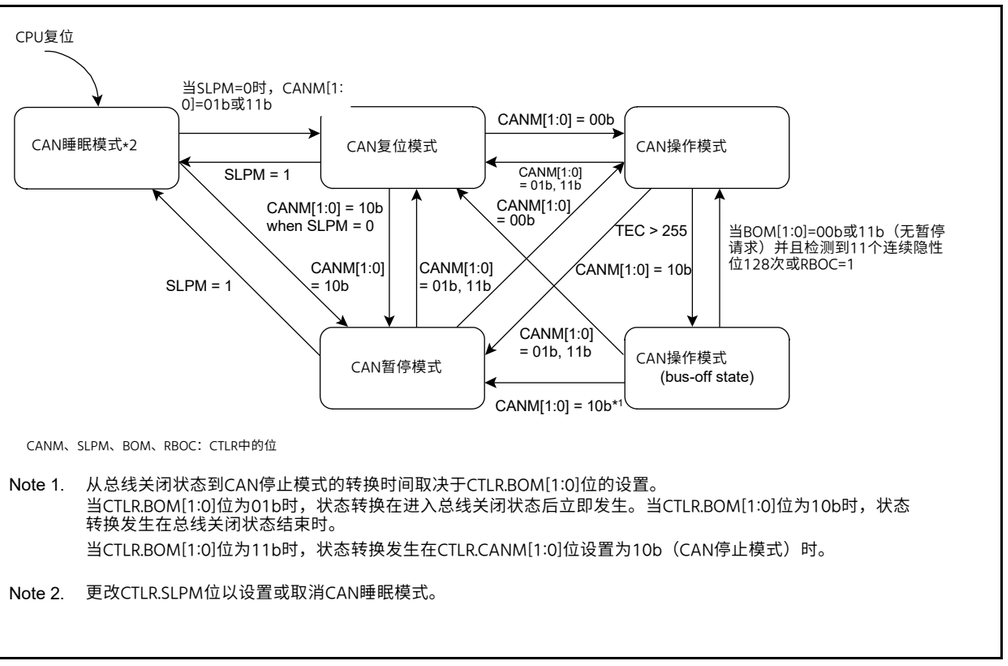
Figure 31.8 选择自检模式1时的连接

31.3 运作模式

CAN模块操作模式包括：

- CAN复位模式
- CAN暂停模式
- CAN操作模式
- CAN睡眠模式。

图31.9显示了不同操作模式之间的转换。



Note 1. 从总线关闭状态到CAN停止模式的转换时间取决于CTLR.BOM[1:0]位的设置。
当CTLR.BOM[1:0]位为01b时，状态转换在进入总线关闭状态后立即发生。当CTLR.BOM[1:0]位为10b时，状态转换发生在总线关闭状态结束时。
当CTLR.BOM[1:0]位为11b时，状态转换发生在CTLR.CANM[1:0]位设置为10b（CAN停止模式）时。

Note 2. 更改CTLR.SLPM位以设置或取消CAN睡眠模式。

Figure 31.9 不同操作模式之间的转换

31.3.1 CAN复位模式

CAN复位模式用于CAN通信配置。当CTLR.CANM[1:0]位设置为01b或11b时，CAN模块进入CAN复位模式。然后将STR.RSTST标志设置为1。不要更改

CTLR.CANM[1:0] bits until the RSTST flag is set to 1. Set the BCR register before exiting CAN reset mode to enter any other modes.

The following registers are initialized to their reset values after entering CAN reset mode, and their initial values are retained during CAN reset mode:

- MCTL_TXj and MCTL_RXj
- STR (except for the SLPST and TFST bits)
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR
- RFCR
- TFCR
- TCR
- ECSR (except for the EDPM bit).

The following registers retain their previous values even after entering CAN reset mode:

- CTLR
- STR (only the SLPST and TFST bits)
- MIER and MIER_FIFO
- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj_ID, MBj_DL, MBj_Dm and MBj_TS
- MKRk
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR.

31.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting. When the CANM[1:0] bits in the CTLR register are set to 10b, CAN halt mode is selected and the HLTST bit in the STR register is set to 1. Do not change the CANM[1:0] bits in the CTLR register until the HLTST bit is 1. See Table 31.8 for the state transition conditions when transmitting or receiving.

All registers except for the RSTST, HLTST, and SLPST bits in the STR register remain unchanged when the CAN enters CAN halt mode.

Do not change the CTLR register (except for the CANM[1:0] and SLPM bits) and the EIER register in CAN halt mode. The BCR register can be changed in CAN halt mode only when listen-only mode is selected for automatic baud rate detection.

CTLR.CANM[1:0]位，直到RSTST标志设置为1。在退出CAN复位模式以进入任何其他模式之前设置BCR寄存器。

以下寄存器在进入CAN复位模式后初始化为其复位值，在CAN复位模式期间保持其初始值：

- MCTL_TXj and MCTL_RXj
- STR（SLPST和TFST位除外）
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR
- RFCR
- TFCR
- TCR
- ECSR（EDPM位除外）。

即使在进入CAN复位模式后，以下寄存器仍保留其先前的值：

- CTLR
- STR（仅SLPST和TFST位）
- MIER and MIER_FIFO
- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj_ID, MBj_DL, MBj_Dm and MBj_TS
- MKRk
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR.

31.3.2 CAN暂停模式

CAN暂停模式用于邮箱配置和测试模式设置。当CTLR寄存器中的CANM[1:0]位设置为10b时，选择CAN停止模式且STR寄存器中的HLTST位设置为1。请勿更改CTLR中的CANM[1:0]位寄存器，直到HLTST位为1。有关发送或接收时的状态转换条件，请参见表31.8。

CAN进入时，除STR寄存器中的RSTST、HLTST和SLPST位之外的所有寄存器保持不变CAN暂停模式。

不要在CAN暂停模式下更改CTLR寄存器（CANM[1:0]和SLPM位除外）和EIER寄存器。只有在为自动波特率检测选择只听模式时，才能在CAN暂停模式下更改BCR寄存器。

Table 31.8 Operation in CAN reset mode and CAN halt mode

Operation mode	Receiver	Transmitter	Bus-off
CAN reset mode (forced transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode without waiting for the end of message transmission	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode after waiting for the end of message transmission*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission*1,*4	• When the BOM[1:0] bits are 00b: A halt request from software is accepted only after bus-off recovery. • When the BOM[1:0] bits are 01b: CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery, regardless of a halt request from software. • When the BOM[1:0] bits are 10b: CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery, regardless of a halt request from software. • When the BOM[1:0] bits are 11b: CAN module enters CAN halt mode without waiting for the end of bus-off recovery, if a halt is requested by software during bus-off.

Note 1. If transmission of multiple messages is requested, a mode transition occurs after completion of the first transmission. If the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF flag in the EIFR register.
Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transitions to CAN halt mode.
Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transitions to the requested CAN mode.

31.3.3 CAN Sleep Mode

CAN sleep mode reduces power consumption by stopping the clock supply to the CAN module. After a reset from an MCU pin or a software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in the CTLR register is set to 1, the CAN module enters CAN sleep mode and the SLPST bit in STR is set to 1. Do not change the value of the SLPM bit until the SLPST bit is 1. The other registers remain unchanged when the CAN module enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any registers (except for the SLPM bit) during CAN sleep mode. Read operation is still allowed.

When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

31.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication. When the CANM[1:0] bits in the CTLR register are set to 00b, the CAN module enters CAN operation mode. The RSTST and HLTST bits in STR are set to 0. Do not change the value of the CANM[1:0] bits until the RSTST and HLTST bits are set to 0.

If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network, which enables transmission and reception of CAN messages
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

Table 31.8 CAN复位模式和CAN暂停模式下的操作

操作模式	Receiver	Transmitter	Bus-off
CAN复位模式（强制转换）CANM[1:0]=11b	CAN模块无需等待报文接收结束即可进入CAN复位模式	CAN模块无需等待报文传输结束即可进入CAN复位模式	CAN模块无需等待总线关闭恢复结束即可进入CAN复位模式
CAN复位模式CANM[1:0]=01b	CAN模块无需等待报文接收结束即可进入CAN复位模式	CAN模块等待报文传输结束后进入CAN复位模式*1、*4	CAN模块无需等待总线关闭恢复结束即可进入CAN复位模式
CAN暂停模式	CAN模块等待报文接收结束后进入CAN停机模式*2 *3	CAN模块等待报文传输结束后进入CAN停机模式*1、*4	当BOM[1:0]位为00b时：仅在总线关闭恢复后才接受来自软件的停止请求。 当BOM[1:0]位为01b时：CAN模块自动进入CAN暂停模式，无需等待总线关闭恢复结束，无论软件是否发出暂停请求。 当BOM[1:0]位为10b时：CAN模块在等待总线关闭恢复结束后自动进入CAN停止模式，无论软件是否发出停止请求。 当BOM[1:0]位为11b时：如果在总线关闭期间软件请求停止，则CAN模块无需等待总线关闭恢复结束即可进入CAN停止模式。

Note 1. 如果请求传输多个消息，则在第一次传输完成后发生模式转换。如果在暂停传输期间请求CAN复位模式，当总线空闲、下一次传输结束或CAN模块成为接收器时发生模式转换。
Note 2. 如果CAN总线被锁定在显性电平，程序可以通过监控EIFR寄存器中的BLIF标志来检测该状态。
Note 3. 如果在请求CAN暂停模式后接收期间发生CAN总线错误，则CAN模块将转换到CAN暂停模式。
Note 4. 如果在请求CAN复位模式或CAN暂停模式后的传输过程中发生CAN总线错误或仲裁丢失，则CAN模块将转换到请求的CAN模式。

31.3.3 CAN睡眠模式

CAN睡眠模式通过停止向CAN模块提供时钟来降低功耗。从一个复位后MCU引脚或软件复位，CAN模块从CAN睡眠模式启动。

当CTLR寄存器中的SLPM位设置为1时，CAN模块进入CAN休眠模式，并且STR中的SLPST位设置为1。在SLPST位为1之前不要更改SLPM位的值。其他寄存器CAN模块进入CAN休眠模式时保持不变。

在CAN复位模式和CAN暂停模式下写入SLPM位。在CAN睡眠模式期间不要更改任何寄存器（SLPM位除外）。仍然允许读取操作。

当SLPM位设置为0时，CAN模块从CAN睡眠模式中释放。当CAN模块退出CAN休眠模式时，其他寄存器保持不变。

31.3.4 CAN操作模式（不包括总线关闭状态）

CAN操作模式用于CAN通信。当CTLR寄存器中的CANM[1:0]位设置为00b时，CAN模块进入CAN操作模式。STR中的RSTST和HLTST位设置为0。在RSTST和HLTST位设置为0之前不要更改CANM[1:0]位的值。

如果进入CAN工作模式后检测到11个连续的隐性位，则CAN模块处于以下状态：

- CAN模块成为网络上的一个活动节点，可以传输和接收CAN报文
- 执行CAN总线的错误监控，例如接收和发送错误计数器。

During CAN operation mode, the CAN module may be in one of the following three sub-modes, depending on the status of the CAN bus:

- Idle mode: No transmission or reception is occurring
- Receive mode: A CAN message sent by another node is being received
- Transmit mode: A CAN message is being transmitted. The CAN module receives a message transmitted by the local node simultaneously when self-test mode 0 (TSTM[1:0] bits in TCR = 10b) or self-test mode 1 (TSTM[1:0] bits = 11b) is selected.

Figure 31.10 shows the sub-modes of CAN operation mode.

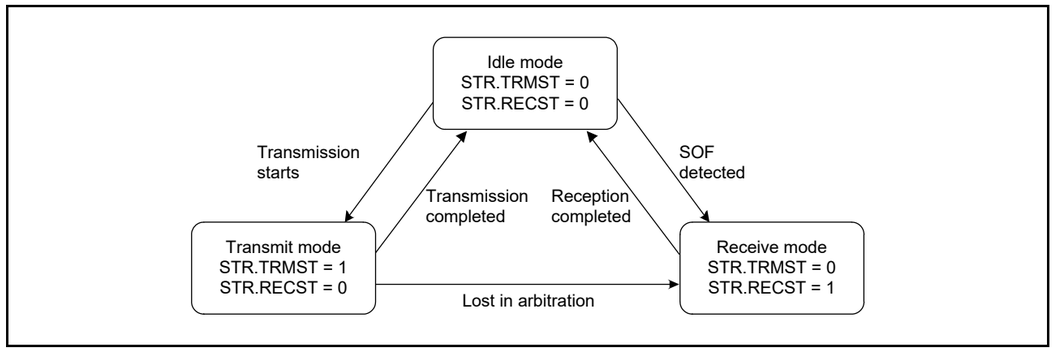


Figure 31.10 Sub-modes of CAN operation mode

31.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state based on the increment or decrement rules for the transmit or receive error counters, as defined in the CAN specification.

The following cases apply when the CAN module is recovering from the bus-off state. When the CAN module is in the bus-off state, the values of the CAN-related registers remain unchanged, except for those in STR, EIFR, RECR, TECR, and TSR.

(1) When BOM[1:0] bits in CTLR are 00b (normal mode)

The CAN module enters the error-active state after it completes recovery from the bus-off state and CAN communication is enabled. The BORIF flag in the EIFR register is set to 1 (bus-off recovery detected).

(2) When RBOC bit in CTLR is set to 1 (forced return from bus-off)

The CAN module enters the error-active state when it is in the bus-off state and the RBOC bit is set to 1. CAN communication is enabled again after 11b consecutive recessive bits are detected. The BORIF flag is not set to 1.

(3) When BOM[1:0] bits are 01b (automatic transition to CAN halt mode on bus-off entry)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF flag is not set to 1.

(4) When BOM[1:0] bits are 10b (automatic transition to CAN halt mode at bus-off end)

The CAN module enters CAN halt mode when it completes the recovery from bus-off. The BORIF flag is set to 1.

(5) When BOM[1:0] bits are 11b (automatic transition to CAN halt mode through software) and CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) during bus-off state

The CAN module enters CAN halt mode when it is in the bus-off state and the CANM[1:0] bits are set to 10b (CAN halt mode). The BORIF flag is not set to 1.

If the CANM[1:0] bits are not set to 10b during bus-off, the same behavior as (1) applies.

在CAN操作模式下，CAN模块可能处于以下三种子模式之一，具体取决于CAN总线的状态：

- 空闲模式：没有发送或接收发生
- 接收模式：正在接收另一个节点发送的CAN报文
- 传输模式：正在传输CAN消息。选择自测模式0（TCR中的TSTM[1:0]位=10b）或自测模式1（TSTM[1:0]位=11b）时，CAN模块同时接收本地节点发送的消息.

图31.10显示了CAN操作模式的子模式。

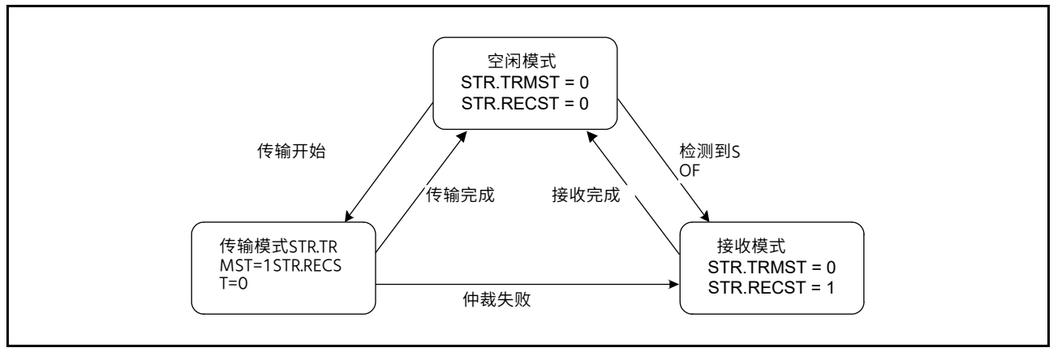


Figure 31.10 CAN操作模式的子模式

31.3.5 CAN操作模式（总线关闭状态）

CAN模块根据CAN规范中定义的发送或接收错误计数器的递增或递减规则进入总线关闭状态。

以下情况适用于CAN模块从总线关闭状态恢复时。当CAN模块处于总线关闭状态时，CAN相关寄存器的值保持不变，除了STR、EIFR、RECR、TECR和TSR中的值。

(1) CTLR中的BOM[1:0]位为00b时（正常模式）

CAN模块在完成从总线关闭状态恢复并启用CAN通信后进入错误激活状态。EIFR寄存器中的BORIF标志设置为1（检测到总线关闭恢复）。

(2) 当CTLR中的RBOC位设置为1时（从总线关闭强制返回）

当CAN模块处于总线关闭状态且RBOC位设置为1时，CAN模块进入错误激活状态。在检测到11b个连续的隐性位后，再次启用CAN通信。BORIF标志未设置为1。

(3) 当BOM[1:0]位为01b时（在总线关闭进入时自动转换到CAN暂停模式）

CAN模块在达到总线关闭状态时进入CAN停止模式。BORIF标志未设置为1。

(4) 当BOM[1:0]位为10b时（总线关闭结束时自动转换到CAN暂停模式）

CAN模块在完成总线关闭恢复后进入CAN停止模式。BORIF标志设置为1。

(5) 当BOM[1:0]位为11b时（通过软件自动转换到CAN暂停模式）并且CTLR中的CANM[1:0]位在总线关闭状态期间设置为10b（CAN停止模式）

CAN模块在总线关闭状态且CANM[1:0]位设置为10b（CAN停止模式）时进入CAN停止模式。BORIF标志未设置为1。

如果在总线关闭期间CANM[1:0]位未设置为10b，则适用与(1)相同的行为。

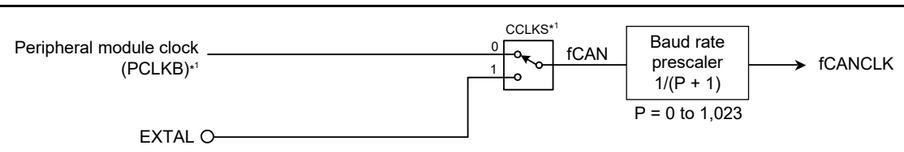
31.4 Data Transfer Rate Configuration

This section describes how to configure the data transfer rate.

31.4.1 Clock Setting

The CAN module has a CAN clock generator. The CAN clock can be set by the CCLKS bit and the BRP[9:0] bits in the BCR register.

Figure 31.11 shows a block diagram of the CAN clock generator.



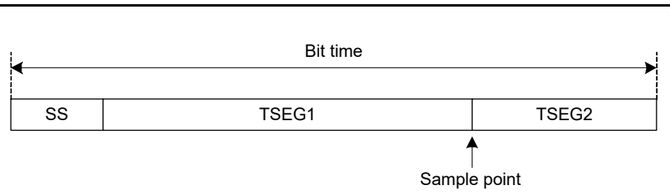
CCLKS: Bit in the BCR register
fCAN: CAN system clock
P: Value selected by BRP[9:0] bits in BCR (P = 0 to 1,023)
fCANCLK: CAN communication clock (fCANCLK = fCAN/(P + 1))

Note 1. See section 9, Clock Generation Circuit. When using the CAN module while the CCLKS bit is set to 0, the PLL must be selected as the source of the peripheral module clock.

Figure 31.11 Block diagram of CAN clock generator

31.4.2 Bit Time Setting

The bit time setting consists of three segments as Figure 31.12 shows.



The range of each segment: Bit time = 8 Tq to 25 Tq
SS = 1 Tq
TSEG1 = 4 Tq to 16 Tq
TSEG2 = 2 Tq to 8 Tq
SJW = 1 Tq to 4 Tq
Setting of TSEG1 and TSEG2: TSEG1 > TSEG2 ≥ SJW

Figure 31.12 Bit timing

31.4.3 Data Transfer Rate

The data transfer rate depends on the division value of fCAN (CAN system clock), the division value of the baud rate prescaler, and the Tq count for 1 bit time.

$$\text{Data transfer rate [bps]} = \frac{\text{fCAN}}{\text{Baud rate prescaler division value}^{*1} \times \text{Tq count for 1 bit time}} = \frac{\text{fCANCLK}}{\text{Tq count for 1 bit time}}$$

Note 1. Division value of baud rate prescaler = P + 1 (P: 0 to 1,023), where P is the BRP[9:0] setting in the BCR register.

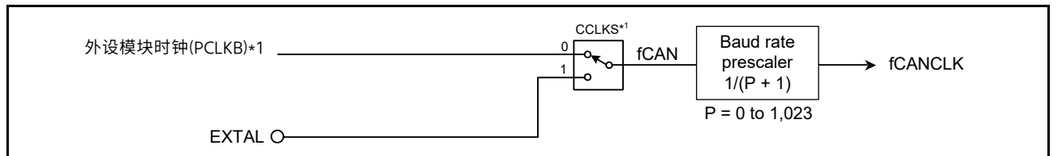
31.4 数据传输率配置

本节介绍如何配置数据传输速率。

31.4.1 时钟设置

CAN模块有一个CAN时钟发生器。CAN时钟可以通过CCLKS位和BRP[9:0]位设置
BCR register.

图31.11显示了CAN时钟发生器的框图。



CCLKS: BCR寄存器中的位
fCAN: CAN系统时钟
P：由BCR中的BRP[9:0]位选择的值（P=0到1 023）fCANCLK：CAN
通信时钟（fCANCLK=fCAN(P+1)）

注1.见第9节，时钟生成电路。在CCLKS位设置为0时使用CAN模块时，必须选择PLL作为外设模块时钟的源。

Figure 31.11 CAN时钟发生器框图

31.4.2 位时间设置

位时间设置由三个部分组成，如图31.12所示。

每个段的范围： 位时间=8Tq到25TqSS=
1Tq
TSEG1 = 4 Tq to 16 Tq
TSEG2 = 2 Tq to 8 Tq
SJW = 1 Tq to 4 Tq
TSEG1和TSEG2的设置：TSEG1>TSEG2 SJW

Figure 31.12 位时序

31.4.3 数据传输率

数据传输速率取决于fCAN（CAN系统时钟）的分频值、波特率预分频器的分频值和1位时间的Tq计数。

$$\text{数据传输率[bps]} = \frac{\text{fCAN}}{\text{波特率预分频器分频值}^{*1}\times\text{Tq计数1位时间}} = \frac{\text{fCANCLK}}{\text{1位时间的Tq计数}}$$

注1.波特率预分频器的分频值=P+1(P:0to1 023)，其中P是BCR寄存器中的BRP[9:0]设置。

Table 31.9 lists data transfer rate examples.

Table 31.9 Data transfer rate examples when fCAN = 32 MHz

Data transfer rate	Tq count	P + 1
1 Mbps	8Tq 16Tq	4 2
500 kbps	8Tq 16Tq	8 4
250 kbps	8Tq 16Tq	16 8
125 kbps	8Tq 16Tq	32 16
83.3 kbps	8Tq 16Tq	48 24
33.3 kbps	8Tq 10Tq 16Tq 20Tq	120 96 60 48

31.5 Mailbox and Mask Register Structure

Figure 31.13 shows the structure of the 32 mailbox registers MBj_ID, MBj_DL, MBj_Dm, and MBj_TS.

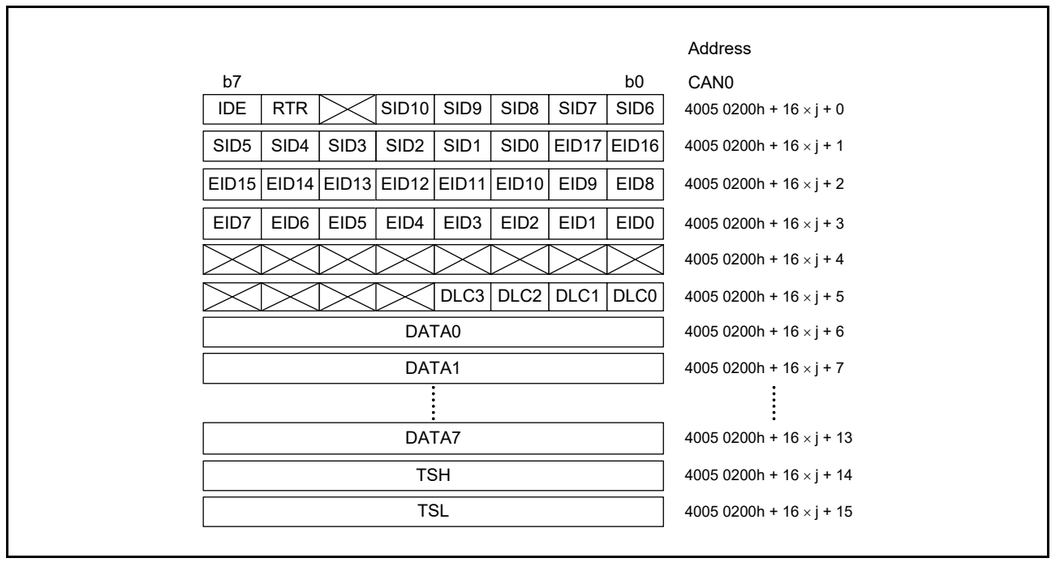


Figure 31.13 Structure of a mailbox register (j = 0 to 31)

Figure 31.14 shows the structure of the eight mask registers MKRk.

表31.9列出了数据传输速率示例。

Table 31.9 fCAN=32MHz时的数据传输速率示例

数据传输率	Tq count	P + 1
1 Mbps	8Tq 16Tq	4 2
500 kbps	8Tq 16Tq	8 4
250 kbps	8Tq 16Tq	16 8
125 kbps	8Tq 16Tq	32 16
83.3 kbps	8Tq 16Tq	48 24
33.3 kbps	8Tq 10Tq 16Tq 20Tq	120 96 60 48

31.5 邮箱和掩码寄存器结构

图31.13显示了32个邮箱寄存器MBj_ID、MBj_DL、MBj_Dm和MBj_TS的结构。

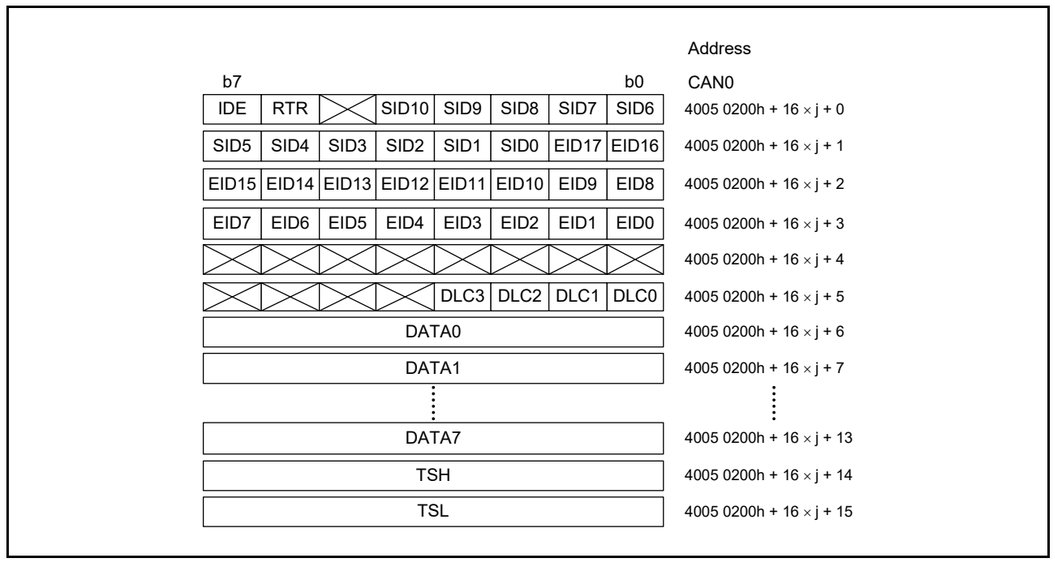


Figure 31.13 邮箱寄存器的结构（j=0到31）

图31.14显示了8个屏蔽寄存器MKRk的结构。

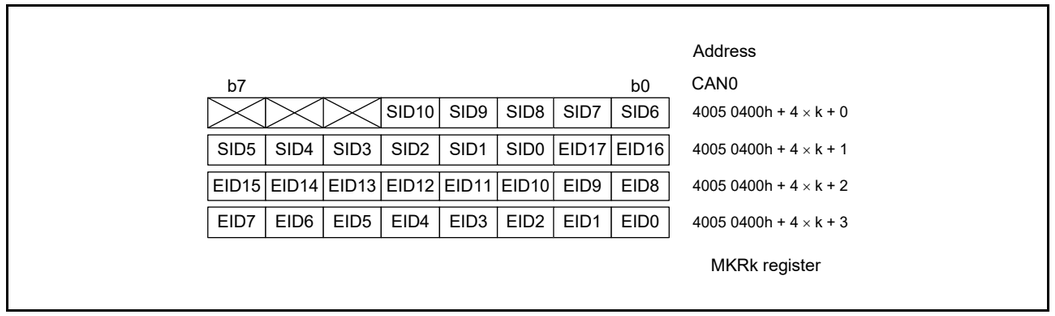


Figure 31.14 Structure of MKRk (k = 0 to 7)

Figure 31.15 shows the structure of the two FIFO received ID compare registers, FIDCR0 and FIDCR1.

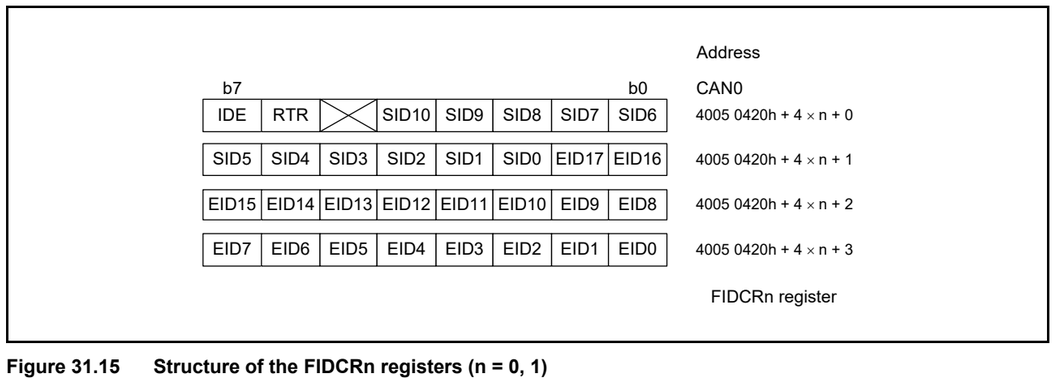


Figure 31.15 Structure of the FIDCRn registers (n = 0, 1)

31.6 Acceptance Filtering and Masking Functions

The acceptance filtering and masking functions allow you to select and receive messages with multiple IDs for mailboxes within a specified range.

The MKRk registers can mask the standard ID and the extended ID of 29 bits:

- MKR0 is the mask register for mailboxes 0 to 3
- MKR1 is the mask register for mailboxes 4 to 7
- MKR2 is the mask register for mailboxes 8 to 11
- MKR3 is the mask register for mailboxes 12 to 15
- MKR4 is the mask register for mailboxes 16 to 19
- MKR5 is the mask register for mailboxes 20 to 23
- MKR6 is the mask register for mailboxes 24 to 27 in normal mailbox mode and receive FIFO mailboxes 28 to 31 in FIFO mailbox mode
- MKR7 is the mask register for mailboxes 28 to 31 in normal mailbox mode and receive FIFO mailboxes 28 to 31 in FIFO mailbox mode.

The MKIVLR register disables acceptance filtering independently for each mailbox.

The IDE bit in the MBj_ID register is valid when the IDFM[1:0] bits in the CTLR register are 10b (mixed ID mode).

The RTR bit in the MBj_ID register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes 0 to 23 use the associated register (MKR0 to MKR5) for acceptance filtering.

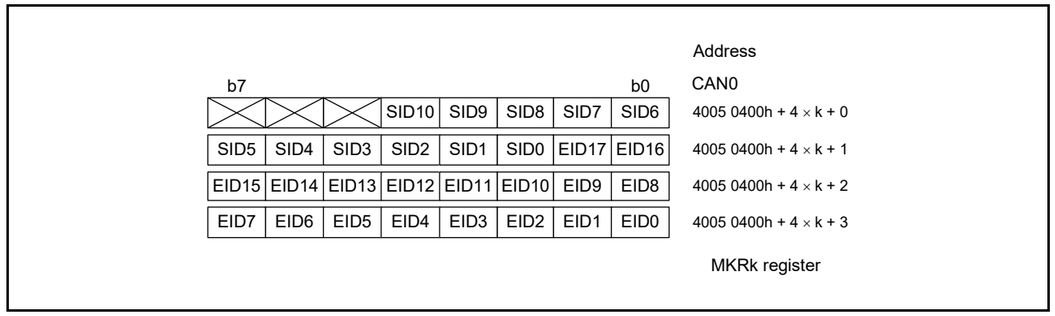


Figure 31.14 MKRk的结构（k=0到7）

图31.15显示了两个FIFO接收ID比较寄存器FIDCR0和FIDCR1的结构。

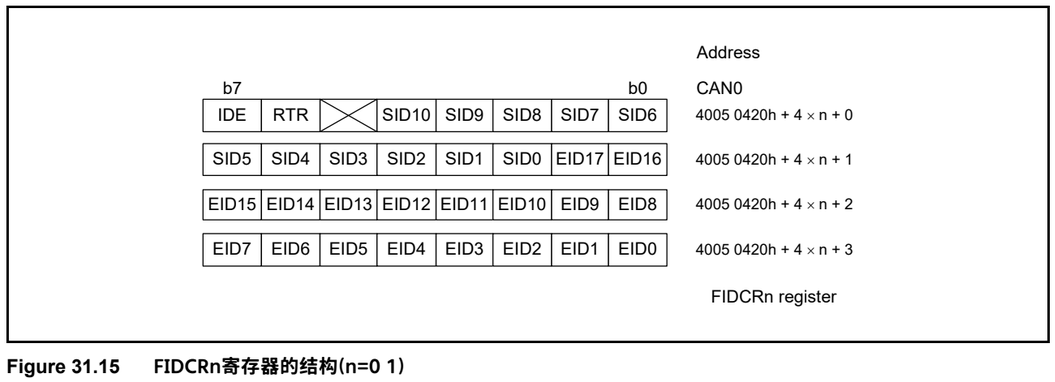


Figure 31.15 FIDCRn寄存器的结构(n=0 1)

31.6 接受过滤和屏蔽功能

接受过滤和屏蔽功能允许您为指定范围内的邮箱选择和接收具有多个ID的消息。

MKRk寄存器可以屏蔽标准ID和29位扩展ID：

- MKR0是邮箱0到3的掩码寄存器
- MKR1是邮箱4到7的掩码寄存器
- MKR2是邮箱8到11的掩码寄存器
- MKR3是邮箱12到15的掩码寄存器
- MKR4是邮箱16到19的掩码寄存器
- MKR5是邮箱20到23的掩码寄存器
- MKR6是普通邮箱模式下邮箱24到27的掩码寄存器，在正常邮箱模式下接收FIFO邮箱28到31 FIFO邮箱模式
- MKR7是普通邮箱模式下邮箱28到31的掩码寄存器，在正常邮箱模式下接收FIFO邮箱28到31 FIFO邮箱模式。

MKIVLR寄存器为每个邮箱单独禁用接受过滤。

当CTLR寄存器中的IDFM[1:0]位为10b（混合ID模式）时，MBj_ID寄存器中的IDE位有效。

MBj_ID寄存器中的RTR位选择数据帧或远程帧。

在FIFO邮箱模式下，普通邮箱0到23使用相关寄存器（MKR0到MKR5）进行接受过滤。

The receive FIFO mailboxes 28 to 31 use two registers, MKR6 and MKR7, for acceptance filtering.

The receive FIFO uses two registers, FIDCR0 and FIDCR1, for ID comparison. The EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two logic OR operations, two ranges of IDs can be received into the receive FIFO. The MKIVLR register is disabled for the receive FIFO.

If different values are set in the IDE bits in the FIDCR0 and FIDCR1 registers, both ID formats are received. If different values are set in the RTR bits in the FIDCR0 and FIDCR1 registers, both data and remote frames are received.

When a combination of two ranges of IDs is not required, set the same mask value and the same ID in both the FIFO ID and mask registers.

Figure 31.16 shows the associations between mask registers and mailboxes. Figure 31.17 shows the acceptance filtering.

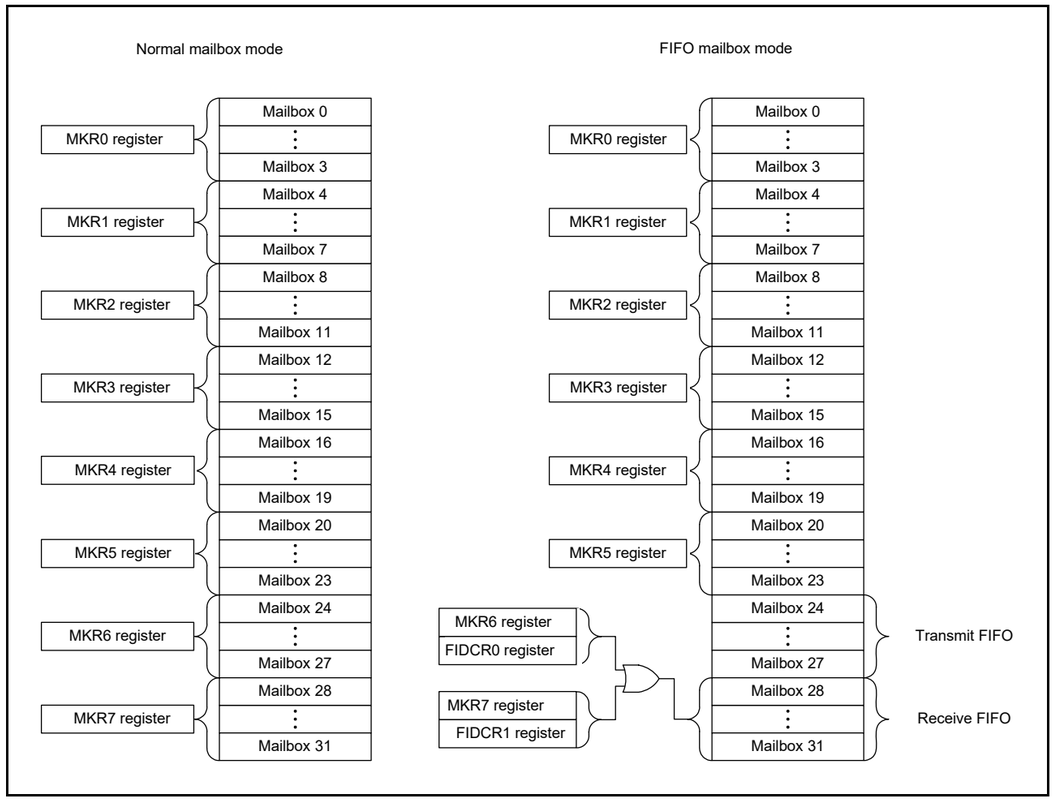


Figure 31.16 Associations between mask registers and mailboxes

接收FIFO邮箱28到31使用两个寄存器，MKR6和MKR7，用于接受过滤。

接收FIFO使用两个寄存器FIDCR0和FIDCR1进行ID比较。EID[17:0]、SID[10:0]、RTR和邮箱28到邮箱31中用于接收FIFO的IDE位被禁用。由于接受过滤取决于两个逻辑或运算的结果，因此可以将两个范围的ID接收到接收FIFO中。MKIVLR寄存器对接收FIFO禁用。

如果在FIDCR0和FIDCR1寄存器的IDE位中设置了不同的值，则会接收两种ID格式。如果在FIDCR0和FIDCR1寄存器的RTR位中设置了不同的值，则数据和远程帧都会被接收。

当不需要两个ID范围的组合时，在FIFOID和掩码寄存器中设置相同的掩码值和相同的ID。

图31.16显示了屏蔽寄存器和邮箱之间的关联。图31.17显示了接受过滤。

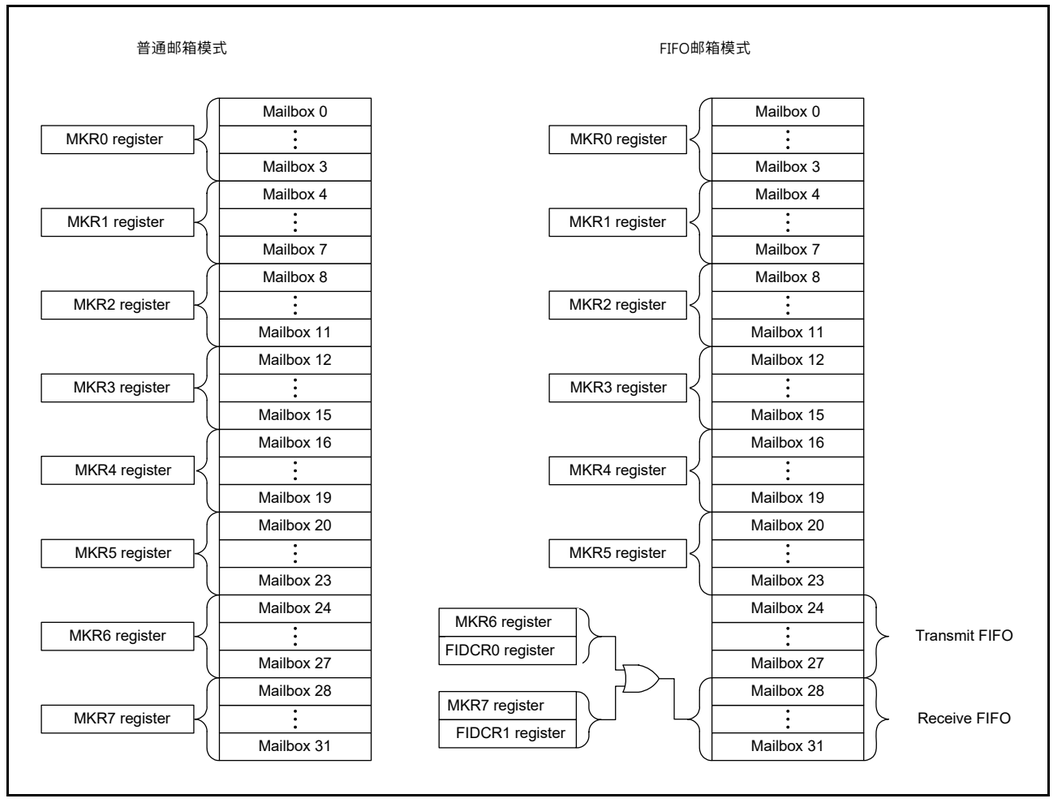


Figure 31.16 掩码寄存器和邮箱之间的关联

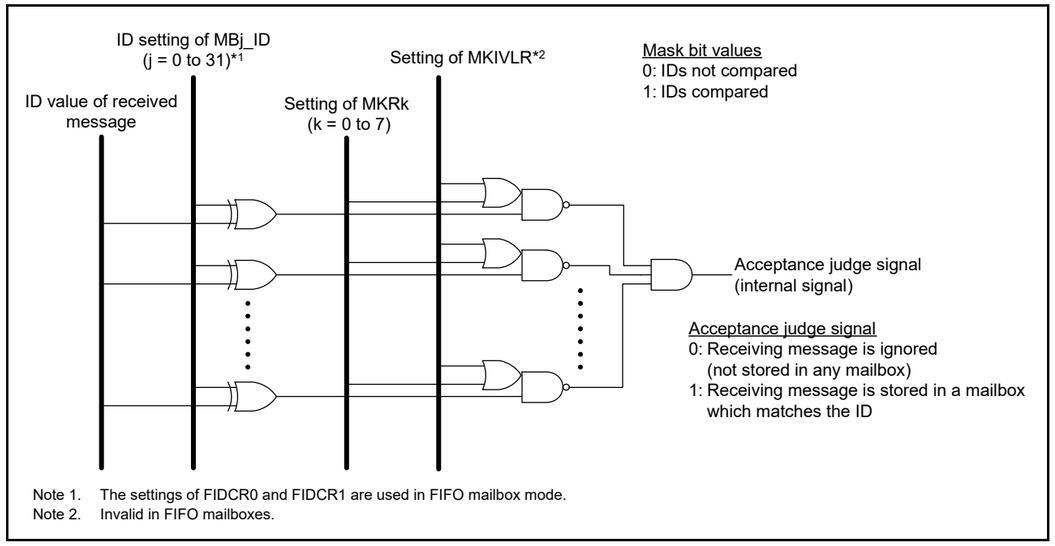


Figure 31.17 Acceptance filtering

31.7 Reception and Transmission

Table 31.10 lists the CAN communication mode settings.

Table 31.10 Settings for CAN receive and transmit modes

MCTL_TXj.TRMREQ and MCTL_RXj.TRMREQ	MCTL_TXj.RECREQ and MCTL_RXj.RECREQ	MCTL_TXj.ONESHOT and MCTL_RX.ONESHOT	Mailbox communication mode
0	0	0	Mailbox disabled or transmission aborted
0	0	1	Can be configured only when transmission or reception from a mailbox programmed in one-shot mode is aborted
0	1	0	Configured as a receive mailbox for a data frame or a remote frame
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame
1	1	0	Do not set
1	1	1	Do not set

j = 0 to 31

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox:

1. Before configuring a mailbox, set the MCTL_RXj register to 00h.
2. A received message is stored into the first mailbox that matches the condition resulting from the receive mode settings and acceptance filtering. The matching mailbox with the smaller number takes priority for storing the received message.
3. In CAN operation mode, the CAN module does not receive its own transmitted data even when the ID is a match. In self-test mode, however, the CAN module receives its own transmitted data and returns ACK.

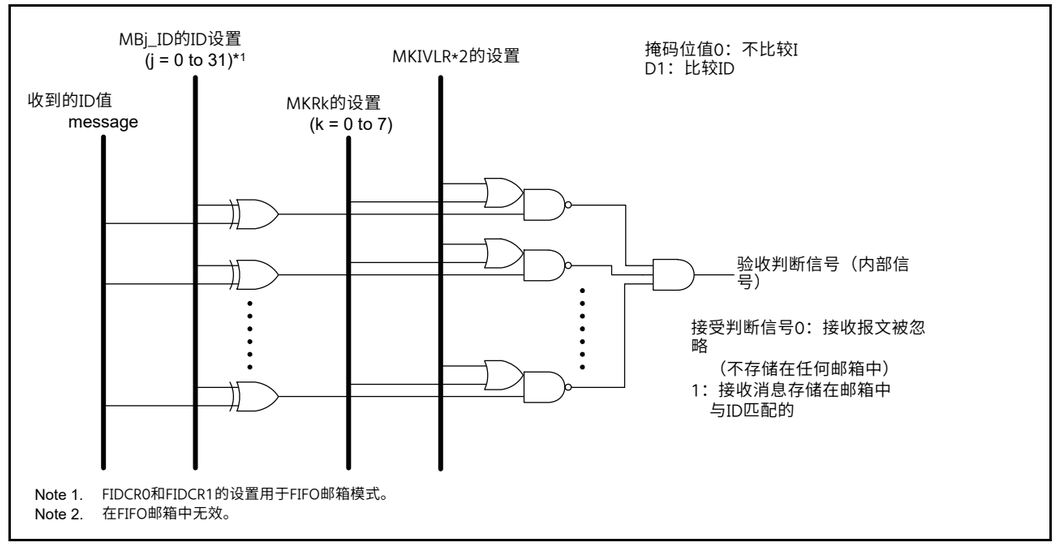


Figure 31.17 验收过滤

31.7 接收和传输

表31.10列出了CAN通信模式设置。

Table 31.10 CAN接收和发送模式的设置

MCTL_TXj.TRMREQ and MCTL_RXj.TRMREQ	MCTL_TXj.RECREQ and MCTL_RXj.RECREQ	MCTL_TXj.ONESHOT and MCTL_RX.ONESHOT	邮箱通讯方式
0	0	0	邮箱禁用或传输中止
0	0	1	只有在一次性模式中编程的邮箱的发送或接收被中止时才可以配置
0	1	0	配置为数据帧或远程帧的接收邮箱
0	1	1	配置为数据帧或远程帧的一次性接收邮箱
1	0	0	配置为数据帧或远程帧的发送邮箱
1	0	1	配置为数据帧或远程帧的一次性发送邮箱
1	1	0	不要设置
1	1	1	不要设置

j = 0 to 31

当邮箱配置为接收邮箱或一次性接收邮箱时：

1. 在配置邮箱之前，将MCTL_RXj寄存器设置为00h。
2. 接收到的消息将存储到与接收模式设置和接受过滤产生的条件匹配的第一个邮箱中。编号较小的匹配邮箱优先存储收到的消息。
3. 在CAN操作模式下，即使ID匹配，CAN模块也不会接收到自己发送的数据。然而，在自检模式下，CAN模块接收自己发送的数据并返回ACK。

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox:

- Before configuring the mailbox, ensure that the MCTL_TXj register is 00h and that there is no pending abort process.

31.7.1 Reception

Figure 31.18 shows an operation example of data frame reception in overwrite mode.

The example shows the overwriting of the first message when the CAN module receives two consecutive CAN messages that match the receiving conditions in the MCTL_RXj (j = 0 to 31) register.

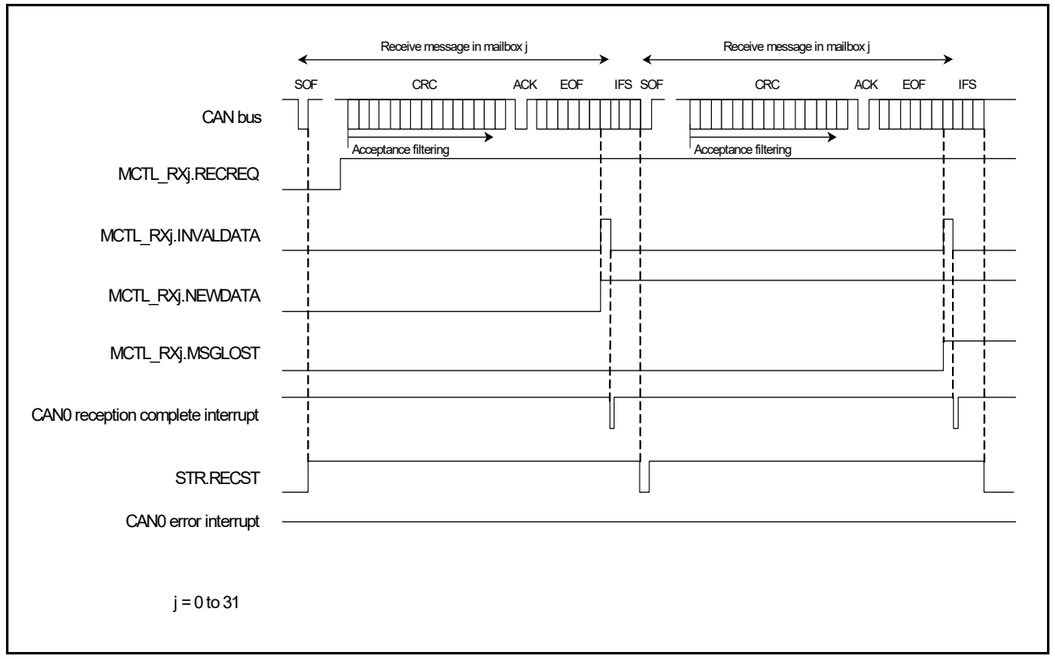


Figure 31.18 Operation example of data frame reception in overwrite mode

1. When an SOF is detected on the CAN bus, the RECST bit in the STR register is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
2. Acceptance filtering starts at the beginning of the CRC field to select the receive mailbox.
3. After a message is received, MCTL_RXj.NEWDATA for the receive mailbox is set to 1 (new message is being stored or was stored to the mailbox). The INVALDATA flag in the MCTL_RXj register is set to 1 (message is being updated) at the same time. The INVALDATA flag is set to 0 (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in the MIER register for the receive mailbox is 1 (interrupt enabled), the INVALDATA flag is set to 0, which triggers a CAN0 reception complete interrupt request.
5. After reading the message from the mailbox, the NEWDATA flag must be set to 0 by software.
6. In overwrite mode, if the next CAN message is received while the NEWDATA bit in MCTL_RXj is set to 1, the MSGLOST flag in MCTL_RXj is set to 1 (message was overwritten). The new received message is transferred to the mailbox. The CAN0 reception complete interrupt request is generated in the same way as in step 4.

将邮箱配置为发送邮箱或一次性发送邮箱时：

- 在配置邮箱之前，请确保MCTL_TXj寄存器为00h，并且没有挂起的中止进程。

31.7.1 Reception

图31.18显示了覆盖模式下数据帧接收的操作示例。

该示例显示当CAN模块接收到与MCTL_RXj(j=0到31)寄存器中的接收条件匹配的两个连续CAN报文时覆盖第一条报文。

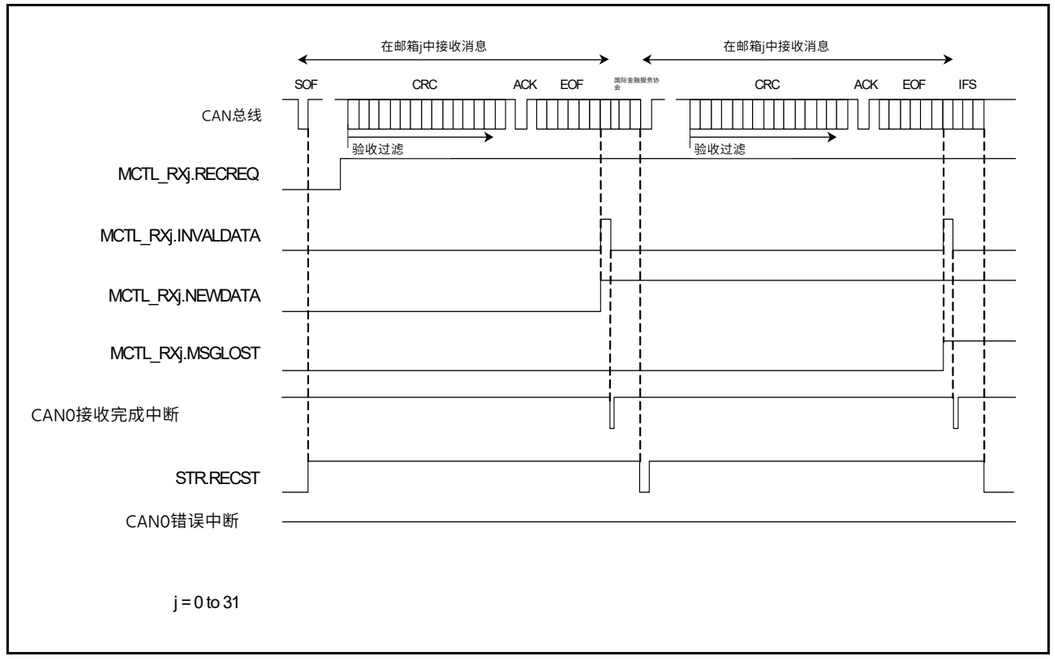


Figure 31.18 覆盖模式下数据帧接收的操作示例

1. 当在CAN总线上检测到SOF时，STR寄存器中的RECST位设置为1（正在接收）
   CAN模块没有准备好开始传输的消息。
2. 接受过滤从CRC字段的开头开始，以选择接收邮箱。
3. 收到消息后，接收邮箱的MCTL_RXj.NEWDATA设置为1（新消息正在存储或已存储到邮箱）。MCTL_RXj寄存器中的INVALDATA标志同时设置为1（正在更新消息）。在完整的消息传送到邮箱后，INVALDATA标志再次设置为0（消息有效）。
4. 当接收邮箱的MIER寄存器中的中断允许位为1（允许中断）时，
   INVALDATA标志设置为0，触发CAN0接收完成中断请求。
5. 从邮箱读取消息后，NEWDATA标志必须由软件设置为0。
6. 在覆盖模式下，如果在MCTL_RXj中的NEWDATA位设置为1时接收到下一个CAN消息，则MCTL_RXj中的MSGLOST标志设置为1（消息被覆盖）。新收到的消息被传送到邮箱。CAN0接收完成中断请求的产生方式与步骤4相同。

Figure 31.19 shows an operation example of data frame reception in overrun mode. The example shows the overrunning of the second message when the CAN module receives two consecutive CAN messages that match the receiving conditions of MCTL_RXj (j = 0 to 31).

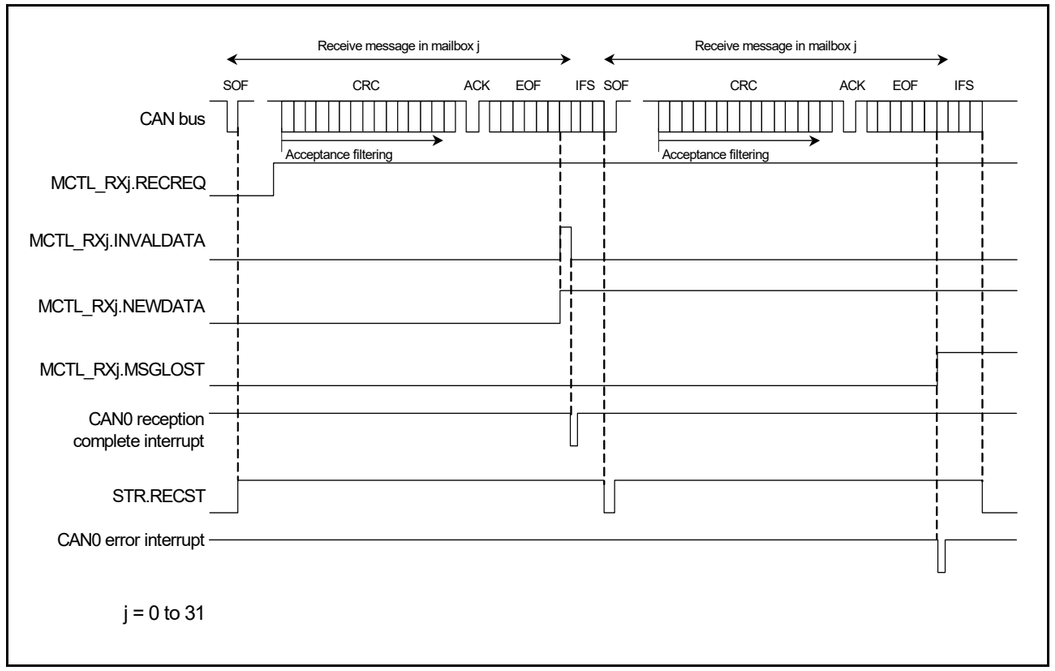


Figure 31.19 Operation example of data frame reception in overrun mode

Steps 1. to 5. are the same as in overwrite mode.

6. In overrun mode, if the next CAN message is received before the NEWDATA flag in MCTL_RXj is set to 0, the MSGLOST flag in MCTL_RXj is set to 1 (message overrun). The new received message is discarded and a CAN0 error interrupt request is generated when the associated interrupt enable bit in the EIER register is set to 1 (interrupt enabled).

31.7.2 Transmission

Figure 31.20 shows an example operation of data frame transmission.

图31.19显示了溢出模式下数据帧接收的操作示例。该示例显示当CAN模块接收到与MCTL_RXj（j=0到31）的接收条件匹配的两个连续CAN报文时，第二条报文的溢出。

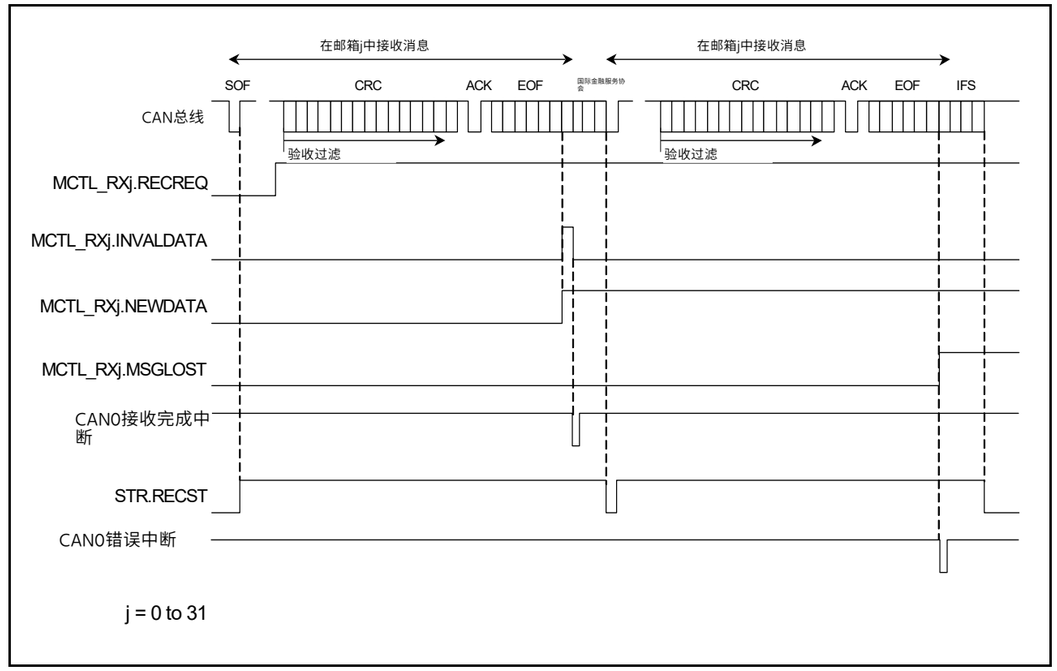


Figure 31.19 溢出模式下数据帧接收的操作示例

步骤1.至5.与覆盖模式相同。

6. 在溢出模式下，如果在MCTL_RXj中的NEWDATA标志设置为0之前接收到下一个CAN报文，则MCTL_RXj中的MSGLOST标志设置为1（消息溢出）。当EIER寄存器中相关的中断使能位设置为1（中断使能）时，新接收到的报文将被丢弃并产生CAN0错误中断请求。

31.7.2 Transmission

图31.20显示了数据帧传输的示例操作。

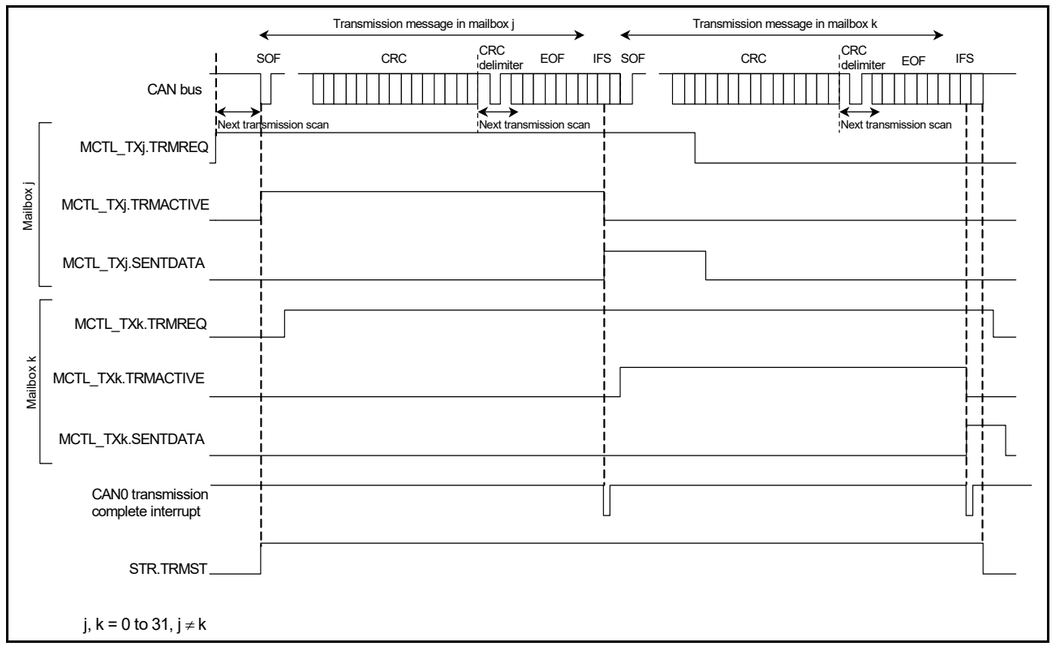


Figure 31.20 Operation example of data frame transmission

1. When a TRMREQ bit in MCTL_TXj (j = 0 to 31) is set to 1 (transmit mailbox) in the bus-idle state, the mailbox scanning determines the highest-priority mailbox for transmission. When the transmit mailbox is determined, the TRMACTIVE flag in MCTL_TXj is set to 1 (from acceptance of transmission request to completion of transmission, or error/arbitration-lost), the TRMST bit in STR is set to 1 (transmission in progress), and the CAN module starts transmission.*1
2. If other TRMREQ bits are set, the transmission scanning starts with the CRC delimiter for the next transmission.
3. If transmission is completed without losing arbitration, the SENTDATA flag in MCTL_TXj is set to 1 (transmission complete) and the TRMACTIVE flag is set to 0 (transmission is pending or transmission is not requested). If the interrupt enable bit in the MIER register is 1 (interrupt enabled), the CAN0 transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set bits SENTDATA and TRMREQ to 0, and then set the TRMREQ bit to 1 after checking that the SENTDATA and TRMREQ bits are set to 0.

Note 1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE flag is set to 0. Transmission scanning is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following arbitration-lost, transmission scanning is performed again to search for the highest-priority transmit mailbox from the start of the CRC delimiter.

31.8 Interrupt

The CAN module provides the following interrupts for each channel:

- CAN0 reception complete interrupt for mailboxes 0 to 31 (CAN0_RXM)
- CAN0 transmission complete interrupt for mailboxes 0 to 31 (CAN0_TXM)
- CAN0 receive FIFO interrupt (CAN0_RXF)
- CAN0 transmit FIFO interrupt (CAN0_TXF)
- CAN0 error interrupt (CAN0_ERS).

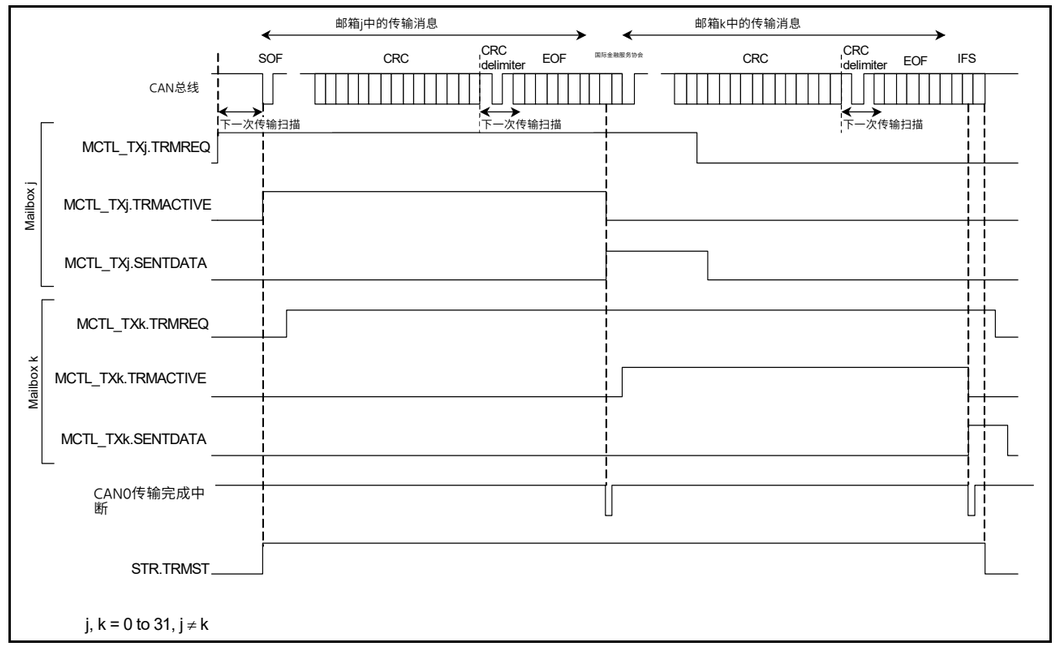


Figure 31.20 数据帧传输的操作示例

1. 当MCTL_TXj（j=0到31）中的TRMREQ位在总线空闲状态下设置为1（发送邮箱）时，邮箱扫描确定发送的最高优先级邮箱。当确定发送邮箱时，MCTL_TXj中的TRMACTIVE标志设置为1（从接受发送请求到发送完成，或错误仲裁失败），STR中的TRMST位设置为1（正在发送），并且CAN模块开始传输。*1
2. 如果设置了其他TRMREQ位，则传输扫描以CRC定界符开始，以进行下一次传输。
3. 如果传输完成且没有丢失仲裁，则MCTL_TXj中的SENTDATA标志设置为1（传输完成），TRMACTIVE标志设置为0（传输未决或未请求传输）。如果MIER寄存器中的中断使能位为1（中断使能），则产生CAN0传输完成中断请求。
4. 当从同一邮箱请求下一次发送时，将SENTDATA和TRMREQ位设置为0，然后在检查SENTDATA和TRMREQ位设置为0后将TRMREQ位设置为1。

注1.如果CAN模块开始发送后仲裁丢失，则TRMACTIVE标志设置为0。再次执行发送扫描以从CRC分隔符的开头搜索优先级最高的发送邮箱。如果在传输过程中或仲裁丢失后发生错误，则再次执行传输扫描以从CRC分隔符的开头搜索最高优先级的传输邮箱。

31.8 Interrupt

CAN模块为每个通道提供以下中断：

- 邮箱0到31(CAN0_RXM)的CAN0接收完成中断
- 邮箱0到31(CAN0_TXM)的CAN0传输完成中断
- CAN0接收FIFO中断(CAN0_RXF)
- CAN0发送FIFO中断(CAN0_TXF)
- CAN0错误中断(CAN0_ERS)。

Eight interrupt sources are available for the CAN0 error interrupts. Check the EIFR register to determine the interrupt sources:

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock.

Table 31.11 lists the CAN interrupts.

Table 31.11 CAN interrupts

Module	Interrupt symbol	Interrupt source	Source flag
CAN0	CAN0_ERS	Bus lock detected	EIFR.BLIF
		Overload frame transmission detected	EIFR.OLIF
		Overrun detected	EIFR.ORIF
		Bus-off recovery detected	EIFR.BORIF
		Bus-off entry detected	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		Bus error detected	EIFR.BEIF
	CAN0_RXF	Receive FIFO message received (MIER_FIFO.MB29 = 0)	RFCR.RFUST[2:0]
		Receive FIFO warning (MIER_FIFO.MB29 = 1)	
	CAN0_TXF	Transmit FIFO message transmission completed (MIER_FIFO.MB25 = 0)	TFCR.TFUST[2:0]
		FIFO last message transmission completed (MIER_FIFO.MB25 = 1)	
	CAN0_RXM	Mailbox 0 to 31 message received	MCTL_RX0.NEWDATA to MCTL_RX31.NEWDATA
	CAN0_TXM	Mailbox 0 to 31 message transmission completed	MCTL_TX0.SENTDATA to MCTL_TX31.SENTDATA

31.9 Usage Notes

31.9.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable CAN operation. The CAN module is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

31.9.2 Settings for the Operating Clock

The settings for the operating clock can be made as follows:

- The following clock constraint must be satisfied for the CAN module when the CCLKS bit is 1:

  $f_{PCLKB} \geq f_{CANMCLK}$

- The source of the peripheral module clocks must be PLL for the CAN module when the CCLKS bit is 0
- The clock frequency ratio of PCLKA and PCLKB must be 2:1 when using the CAN module. Operation is not guaranteed for other settings.

八个中断源可用于CAN0错误中断。检查EIFR寄存器以确定中断源：

- 总线错误
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- 接收溢出
- 过载帧传输
- 巴士锁。

表31.11列出了CAN中断。

Table 31.11 CAN中断

Module	中断符号	中断源	源标志
CAN0	CAN0_ERS	检测到总线锁	EIFR.BLIF
		检测到过载帧传输	EIFR.OLIF
		检测到溢出	EIFR.ORIF
		检测到总线关闭恢复	EIFR.BORIF
		检测到总线关闭条目	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		检测到总线错误	EIFR.BEIF
	CAN0_RXF	接收接收到的FIFO消息(MIER_FIFO.MB29=0)	RFCR.RFUST[2:0]
		接收FIFO警告(MIER_FIFO.MB29=1)	
	CAN0_TXF	传输FIFO消息传输完成(MIER_FIFO.MB25=0)	TFCR.TFUST[2:0]
		FIFO最后一条消息传输完成(MIER_FIFO.MB25=1)	
	CAN0_RXM	邮箱0到31收到消息	MCTL_RX0.NEWDATA to MCTL_RX31.NEWDATA
	CAN0_TXM	邮箱0到31消息传输完成	MCTL_TX0.SENTDATA to MCTL_TX31.SENTDATA

31.9 使用说明

31.9.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用CAN操作。CAN模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

31.9.2 工作时钟设置

工作时钟的设置可按如下方式进行：

- 当CCLKS位为1时，CAN模块必须满足以下时钟约束：

  $f_{PCLKB} \geq f_{CANMCLK}$

- 当CCLKS位为0时，外设模块时钟源必须是CAN模块的PLL
- 使用CAN模块时，PCLKA和PCLKB的时钟频率比必须为2:1。不保证其他设置的操作。

32. Serial Peripheral Interface (SPI)

32.1 Overview

The MCU provides two independent channels of the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices.

Table 32.1 lists the SPI specifications, and Figure 32.1 shows a block diagram.

In this section, PCLK is used to refer to PCLKA. Additionally, *n* indicates A or B, and *i* indicates 0 or 1. A lower-case letter *i* in pin and signal names indicates a value from 0 to 3, and a lower-case letter *m* in SPI Command Register m (SPCMDm) indicates a value from 0 to 7.

Table 32.1 SPI specifications (1 of 2)

Parameter	Description
Number of channels	Two channels
SPI transfer functions	• MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals enable serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation is available • Communication mode: Full-duplex or transmit-only can be selected • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • SPI0: 128 bit transmit and receive buffers, with capability to transfer up to four frames in one round of transmission or reception (each frame consisting of up to 32 bits) • SPI1: 32 bits transmit and receive buffers, with capability to transfer one frame in one round of transmission or reception.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum RSPCK frequency is that of PCLK divided by 6). Width at high level: 3 PCLK cycles Width at low level: 3 PCLK cycles.
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • SPI0: 128 bits for the transmit and receive buffers • SPI1: 32 bits for the transmit and receive buffers.
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection.
SSL control function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins for output • In multi-master mode: SSLn0 pin for input and SSLn1 to SSLn3 pins for either output or unused. • In slave mode: SSLn0 pin for input and SSLn1 to SSLn3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity.

32. 串行外设接口(SPI)

32.1 Overview

MCU提供两个独立的串行外设接口(SPI)通道。SPI通道能够与多个处理器和外围设备进行高速、全双工同步串行通信。

表32.1列出了SPI规范，图32.1显示了框图。

在本节中，PCLK用于指代PCLKA。此外，n表示A或B，i表示0或1。引脚和信号名称中的小写字母i表示从0到3的值，SPI命令寄存器m(SPCMDm)中的小写字母m表示一个从0到7的值。

Table 32.1 SPI规格（2个中的1个）

Parameter	Description
通道数	两个通道
SPI传输函数	MOSI（主机输出从机输入）、MISO（主机输入从机输出）、SSL（从机选择）和RSPCK（SPI时钟）信号可通过SPI操作（4线方法）或时钟同步操作（3线）进行串行通信方法） 仅发送操作可用 通信模式：可选择全双工或仅发送 RSPCK极性切换 RSPCK相位切换。
数据格式	可选择MSB优先或LSB优先 传输位长度可选择为8、9、10、11、12、13、14、15、16、20、24或32位 SPI0：128位发送和接收缓冲区，能够在一轮发送或接收中传输多达四帧（每帧最多包含32位） SPI1：32位发送和接收缓冲区，能够在一轮发送或接收中传输一帧。
比特率	在主机模式下，片内波特率发生器通过对PCLK进行分频产生RSPCK（分频比范围从2分频到4096分频） 在从机模式下，可以输入最小PCLK时钟6分频作为RSPCK（最大RSPCK频率是PCLK除以6的频率）。高电平宽度：3个PCLK周期低电平宽度：3个PCLK周期。
缓冲区配置	发送和接收缓冲区的双缓冲区配置 SPI0：发送和接收缓冲区为128位 SPI1：发送和接收缓冲区为32位。
错误检测	模式故障错误检测 欠载错误检测 溢出错误检测*1 奇偶校验错误检测。
SSL控制功能	每个通道有四个SSL引脚（SSLn0到SSLn3） 在单主模式下，SSLn0到SSLn3引脚用于输出 在多主模式下： SSLn0引脚用于输入，SSLn1至SSLn3引脚用于输出或未使用。 在从属模式下： SSLn0引脚用于输入，SSLn1到SSLn3引脚用于未使用。 从SSL输出断言到RSPCK操作的可控延迟（RSPCK延迟）范围：1到8个RSPCK周期（以RSPCK周期为单位设置） 从RSPCK停止到SSL输出否定的可控延迟（SSL否定延迟）范围：1到8个RSPCK周期（以RSPCK周期为单位设置） 可控制等待下一次访问SSL输出断言（下一次访问延迟）范围：1到8个RSPCK周期（以RSPCK周期为单位设置） 用于更改SSL极性的功能。

Table 32.1 SPI specifications (2 of 2)

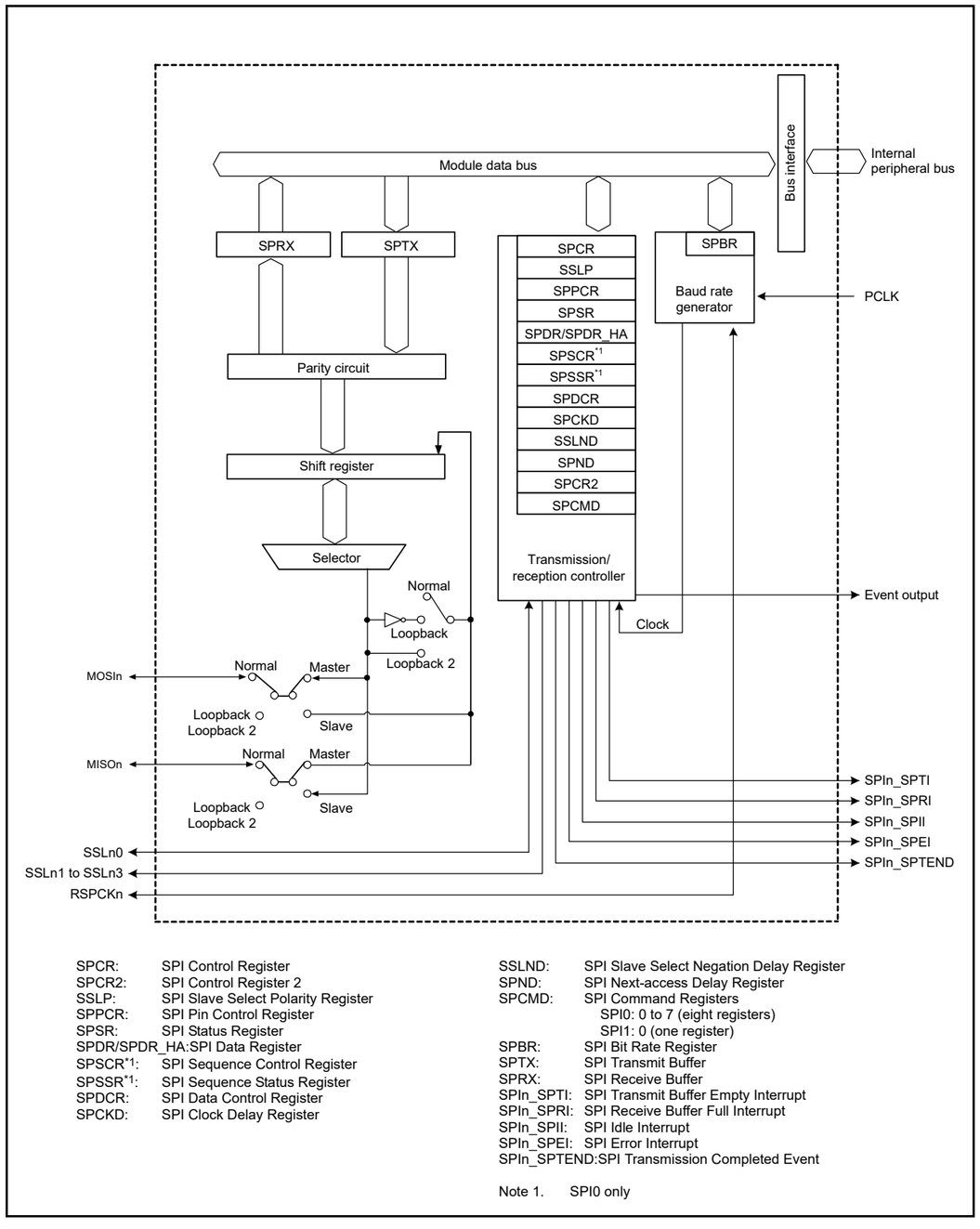
Parameter	Description
Control in master transfer	• A transfer of up to eight commands (for SPI0) can be executed sequentially in looped execution • Support for the following commands: - SPI0: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay - SPI1: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB- or LSB-first, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function.
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode fault, overrun, parity error) • SPI idle interrupt (SPI idle) • Transmission-completed interrupt.
Event link function (output)	The following events can be output to the event link controller: • Receive buffer full • Transmit buffer empty • Mode fault, underrun, overrun, or parity error • SPI idle • Transmission-completed.
Others	• Function for initializing the SPI • Loopback mode.
Module-stop function	Module-stop state can be set to reduce power consumption

Note 1. In master reception, when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.

Table 32.1 SPI规范（2个中的2个）

Parameter	Description
主传输中的控制	最多可以在循环执行中顺序执行8个命令（用于SPI0）的传输 支持以下命令： SPI0：SSL信号值、比特率、RSPCK极性相位、传输数据长度、MSBorLSB优先、突发、RSPCK延迟、SSL否定延迟和下一次访问延迟SPI1：SSL信号值、比特率、RSPCK极性相位、传输数据长度、MSB或LSB优先、RSPCK延迟、SSL否定延迟和下一次访问延迟 可以通过写入发送缓冲区来启动传输 在SSL否定中指定的MOSI信号值 RSPCK自动停止功能。
中断源	接收缓冲区满中断 发送缓冲区空中断 SPI错误中断（模式错误、溢出、奇偶校验错误） SPI空闲中断（SPI空闲） 传输完成中断。
事件链接功能（输出）	以下事件可以输出到事件链接控制器： 接收缓冲区已满 发送缓冲区为空 模式错误、欠载、溢出或奇偶校验错误 SPI空闲 传输完成。
Others	初始化SPI的函数 环回模式。
Module-stop function	可设置模块停止状态以降低功耗

Note 1. 在主机接收中，当启用RSPCK自动停止功能时，不会发生溢出错误，因为在检测到溢出错误时会停止传输时钟。



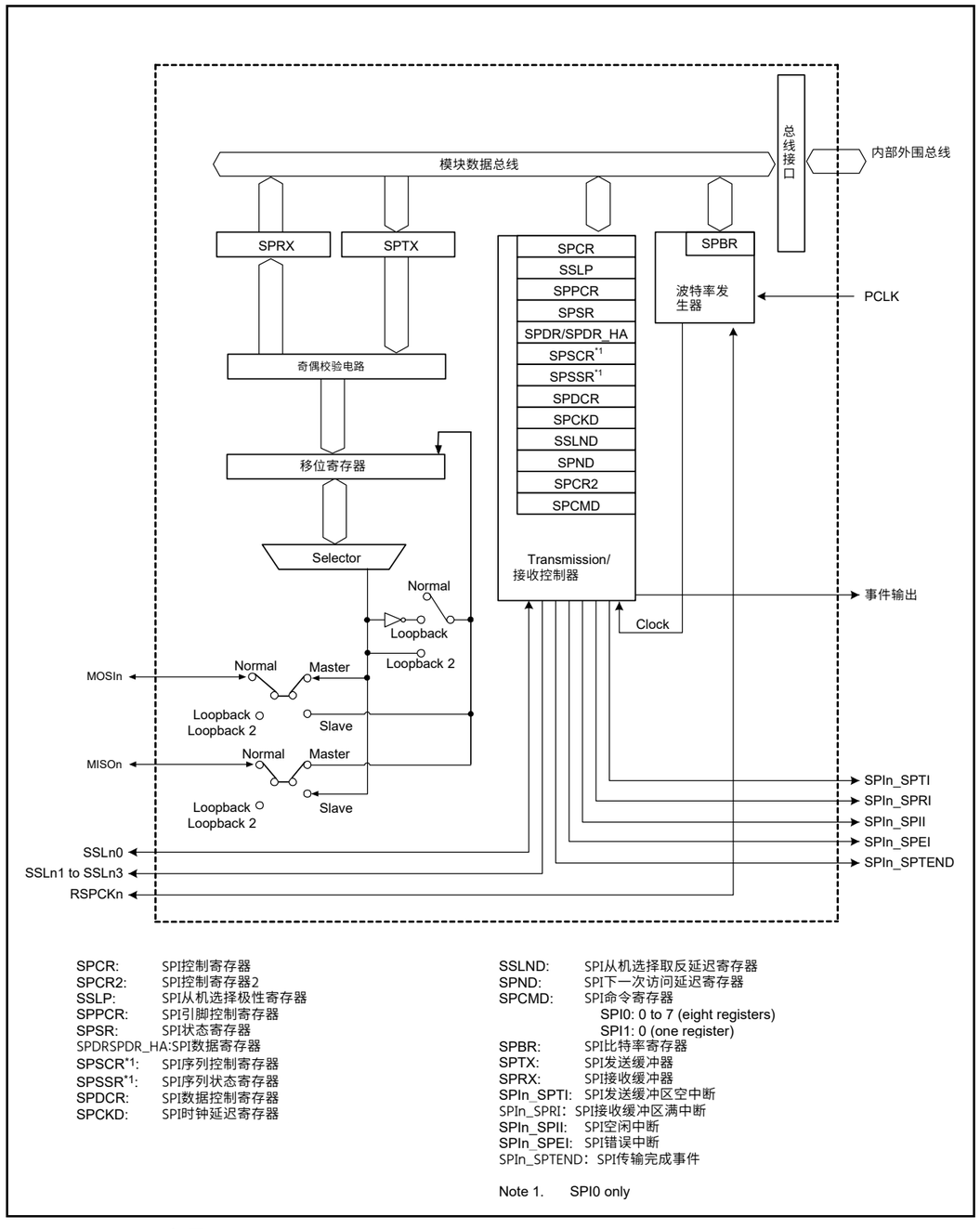
SPCR: SPI Control Register
SPCR2: SPI Control Register 2
SSLP: SPI Slave Select Polarity Register
SPPCR: SPI Pin Control Register
SPSR: SPI Status Register
SPDR/SPDR_HA:SPI Data Register
SPSCR*1: SPI Sequence Control Register
SPSSR*1: SPI Sequence Status Register
SPDCR: SPI Data Control Register
SPCKD: SPI Clock Delay Register

SSLND: SPI Slave Select Negation Delay Register
SPND: SPI Next-access Delay Register
SPCMD: SPI Command Registers
SPI0: 0 to 7 (eight registers)
SPI1: 0 (one register)
SPBR: SPI Bit Rate Register
SPTX: SPI Transmit Buffer
SPRX: SPI Receive Buffer
SPIn_SPTI: SPI Transmit Buffer Empty Interrupt
SPIn_SPRI: SPI Receive Buffer Full Interrupt
SPIn_SPII: SPI Idle Interrupt
SPIn_SPEI: SPI Error Interrupt
SPIn_SPTEND:SPI Transmission Completed Event

Note 1. SPI0 only

Figure 32.1 SPI block diagram

Table 32.2 lists the I/O pins used in the SPI. The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is set as an output when the SPI is a single master and an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 32.3.2, Controlling the SPI Pins.



SPCR: SPI控制寄存器
SPCR2: SPI控制寄存器2
SSLP: SPI从机选择极性寄存器
SPPCR: SPI引脚控制寄存器
SPSR: SPI状态寄存器
SPDRSPDR_HA:SPI数据寄存器
SPSCR*1: SPI序列控制寄存器
SPSSR*1: SPI序列状态寄存器
SPDCR: SPI数据控制寄存器
SPCKD: SPI时钟延迟寄存器

SSLND: SPI从机选择取反延迟寄存器
SPND: SPI下一次访问延迟寄存器
SPCMD: SPI命令寄存器
SPI0: 0 to 7 (eight registers)
SPI1: 0 (one register)
SPBR: SPI比特率寄存器
SPTX: SPI发送缓冲器
SPRX: SPI接收缓冲器
SPIn_SPTI: SPI发送缓冲区空中断
SPIn_SPRI：SPI接收缓冲区满中断
SPIn_SPII: SPI空闲中断
SPIn_SPEI: SPI错误中断
SPIn_SPTEND：SPI传输完成事件

Note 1. SPI0 only

Figure 32.1 SPI框图

表32.2列出了SPI中使用的IO引脚。SPI自动切换SSLn0引脚的IO方向。当SPI为单主机时SSLn0设置为输出，当SPI为多主机或从机时设置为输入。RSPCKn、MOSIn和MISOn引脚会根据主机或从机设置以及SSLn0引脚上的电平输入自动设置为输入或输出。有关详细信息，请参阅第32.3.2节，控制SPI引脚。

Table 32.2 SPI pin configuration

Channel	Pin name	I/O	Function
SPI0	RSPCKA	I/O	Clock I/O
	MOSIA	I/O	Master transmit data I/O
	MISOA	I/O	Slave transmit data I/O
	SSLA0	I/O	Slave selection I/O
	SSLA1	Output	Slave selection output
	SSLA2	Output	Slave selection output
	SSLA3	Output	Slave selection output
SPI1	RSPCKB	I/O	Clock I/O
	MOSIB	I/O	Master transmit data I/O
	MISOB	I/O	Slave transmit data I/O
	SSLB0	I/O	Slave selection I/O
	SSLB1	Output	Slave selection output
	SSLB3	Output	Slave selection output

32.2 Register Descriptions

32.2.1 SPI Control Register (SPCR)

Address(es): SPI0.SPCR 4007 2000h, SPI1.SPCR 4007 2100h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPMS	SPI Mode Select	0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method).	R/W
b1	TXMD	Communications Operating Mode Select	0: Select full-duplex synchronous serial communications 1: Select serial communications consisting of only transmit operations.	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disable detection of mode fault errors 1: Enable detection of mode fault errors.	R/W
b3	MSTR	SPI Master/Slave Mode Select	0: Select slave mode 1: Select master mode.	R/W
b4	SPEIE	SPI Error Interrupt Enable	0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests.	R/W
b5	SPTIE	Transmit Buffer Empty Interrupt Enable	0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests.	R/W
b6	SPE	SPI Function Enable	0: Disable SPI function 1: Enable SPI function.	R/W
b7	SPRIE	SPI Receive Buffer Full Interrupt Enable	0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests.	R/W

If the SPCR.MSTR, SPCR.MODFEN, or SPCR.TXMD bit is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

Table 32.2 SPI引脚配置

Channel	引脚名称	I/O	Function
SPI0	RSPCKA	I/O	Clock I/O
	MOSIA	I/O	主机发送数据IO
	MISOA	I/O	从机发送数据IO
	SSLA0	I/O	从机选择IO
	SSLA1	Output	从机选择输出
	SSLA2	Output	从机选择输出
	SSLA3	Output	从机选择输出
SPI1	RSPCKB	I/O	Clock I/O
	MOSIB	I/O	主机发送数据IO
	MISOB	I/O	从机发送数据IO
	SSLB0	I/O	从机选择IO
	SSLB1	Output	从机选择输出
	SSLB3	Output	从机选择输出

32.2 注册说明

32.2.1 SPI控制寄存器(SPCR)

Address(es): SPI0.SPCR 4007 2000h, SPI1.SPCR 4007 2100h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SPMS	SPI模式选择	0：选择SPI操作（4线方式）1：选择时钟同步操作（3线方式）。	R/W
b1	TXMD	通讯操作模式 Select	0：选择全双工同步串行通信1：选择仅包含发送操作的串行通信。	R/W
b2	MODFEN	模式故障错误检测启用	0：禁用模式故障错误检测1：启用模式故障错误检测。	R/W
b3	MSTR	SPI主从模式选择	0：选择从模式1：选择主模式。	R/W
b4	SPEIE	SPI错误中断使能	0：禁用SPI错误中断请求1：启用SPI错误中断请求。	R/W
b5	SPTIE	发送缓冲区空中断 Enable	0：禁止发送缓冲区空中断请求1：使能发送缓冲区空中断请求。	R/W
b6	SPE	SPI功能使能	0：禁用SPI功能1：启用SPI功能。	R/W
b7	SPRIE	SPI接收缓冲器满中断 Enable	0：禁止SPI接收缓冲区满中断请求1：使能SPI接收缓冲区满中断请求。	R/W

如果在SPCR.SPE位为1时更改了SPCR.MSTR、SPCR.MODFEN或SPCR.TXMD位，则不要执行后续操作。

SPMS位（SPI模式选择）

SPMS位选择SPI操作（4线方法）或时钟同步操作（3线方法）。

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. If clock synchronous operation is in master mode (SPCR.MSTR = 1), the CPHA bit in the SPCMDm register can be set to either 0 or 1. Set the CPHA bit to 1 if clock synchronous operation is in slave mode (SPCR.MSTR = 0). Do not perform operations if the CPHA bit is set to 0 when clock synchronous operation is in slave mode (SPCR.MSTR = 0).

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations.

When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 32.3.6, Data Transfer Modes), and receive buffer full interrupt requests cannot be used.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables detection of mode fault errors (see section 32.3.8, Error Detection). In addition, the SPI determines the I/O direction of the SSLn0 to SSLn3 pins based on combinations of the MODFEN and MSTR bit settings (see section 32.3.2, Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLn0 to SSLn3 pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1.

See section 32.3.8, Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty.

A transmit buffer empty interrupt request on transmission start is generated by setting the SPE and SPTIE bits to 1 at the same time or by setting the SPE bit to 1 after setting the SPTIE bit to 1. The interrupt is generated when the SPTIE bit is 1 even if the SPI function is disabled (the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function. The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 32.3.8, Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 32.3.9, Initializing the SPI. Additionally, a state change on the SPE bit, from 0 to 1 or 1 to 0, triggers a transmit buffer empty interrupt request.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an interrupt request when the SPI detects a receive buffer full write after completing a serial transfer.

SSLn0到SSLn3引脚不用于时钟同步操作。RSPCKn、MOSIn和MIOn引脚处理通信。如果时钟同步操作处于主机模式(SPCR.MSTR=1)，则SPCMDm寄存器中的CPHA位可设置为0或1。如果时钟同步操作处于从机模式(SPCR.MSTR)，则将CPHA位设置为1=0)。当时钟同步操作处于从模式(SPCR.MSTR=0)时，如果CPHA位设置为0，则不要执行操作。

TXMD位（通信操作模式选择）

TXMD位选择全双工同步串行通信或仅发送操作。

当该位设置为1时，SPI仅执行发送操作而不执行接收操作（参见第32.3.6节，数据TransferModes），不能使用接收缓冲区满中断请求。

MODFEN位（模式故障错误检测使能）

MODFEN位启用或禁用模式故障错误检测（参见第32.3.8节，错误检测）。除此之外SPI根据MODFEN和MSTR位设置的组合确定SSLn0到SSLn3引脚的IO方向（参见第32.3.2节，控制SPI引脚）。

MSTR位（SPI主从模式选择）

MSTR位选择SPI的主模式或从模式。根据MSTR位设置，SPI确定RSPCKn、MOSIn、MISOn和SSLn0到SSLn3引脚的方向。

SPEIE位（SPI错误中断使能）

在以下情况下，SPEIE位启用或禁用SPI错误中断请求的生成：

- SPI检测到模式故障错误或欠载错误并将SPSR.MODF标志设置为1
- SPI检测到溢出错误并将SPSR.OVRF标志设置为1
- SPI检测到奇偶校验错误并将SPSR.PERF标志设置为1。

请参阅第32.3.8节，错误检测。

SPTIE位（发送缓冲区空中断使能）

当SPI检测到发送缓冲区为空时，SPTIE位使能或禁止生成发送缓冲区空中断请求。

通过将SPE和SPTIE位同时设置为1或在将SPTIE位设置为1后将SPE位设置为1，在发送开始时产生发送缓冲区空中断请求。当SPTIE位为1时产生中断即使SPI功能被禁用（SPE位变为0）。

SPE位（SPI功能使能）

SPE位启用或禁用SPI功能。当SPSR.MODF标志为1时，SPE位不能设置为1。有关详细信息，请参阅第32.3.8节，错误检测。

将SPE位设置为0将禁用SPI功能并初始化部分模块功能。有关详细信息，请参阅第32.3.9节，初始化SPI。此外，SPE位的状态变化（从0到1或1到0）会触发发送缓冲区空中断请求。

SPRIE位（SPI接收缓冲区满中断使能）

当SPI在完成串行传输后检测到接收缓冲区满写时，SPRIE位启用或禁用中断请求的生成。

32.2.2 SPI Slave Select Polarity Register (SSLP)

Address(es): SPI0.SSLP 4007 2001h, SPI1.SSLP 4007 2101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: SSL0 signal is active-low 1: SSL0 signal is active-high.	R/W
b1	SSL1P	SSL1 Signal Polarity Setting	0: SSL1 signal is active-low 1: SSL1 signal is active-high.	R/W
b2	SSL2P*1	SSL2 Signal Polarity Setting	0: SSL2 signal is active-low 1: SSL2 signal is active-high.	R/W
b3	SSL3P	SSL3 Signal Polarity Setting	0: SSL3 signal is active-low 1: SSL3 signal is active-high.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in SPI1.

If the contents of SSLP are changed when the SPCR.SPE bit is 1, do not perform subsequent operations.

32.2.3 SPI Pin Control Register (SPPCR)

Address(es): SPI0.SPPCR 4007 2002h, SPI1.SPPCR 4007 2102h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPLP	SPI Loopback	0: Normal mode 1: Loopback mode, with data inverted for transmission.	R/W
b1	SPLP2	SPI Loopback 2	0: Normal mode 1: Loopback mode, with data not inverted for transmission.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIn pin during MOSI idling is low 1: The level output on the MOSIn pin during MOSI idling is high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of the SPPCR register are changed when the SPCR.SPE bit is 1, do not perform subsequent operations.

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When the SPLP bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the input path and output path for the shift register, establishing loopback mode.

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When the SPLP2 bit is set to 1, the SPI shuts off the path between the

32.2.2 SPI从机选择极性寄存器(SSLP)

Address(es): SPI0.SSLP 4007 2001h, SPI1.SSLP 4007 2101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SSL0P	SSL0信号极性设置	0：SSL0信号低电平有效1： SSL0信号高电平有效。	R/W
b1	SSL1P	SSL1信号极性设置	0：SSL1信号低电平有效1： SSL1信号高电平有效。	R/W
b2	SSL2P*1	SSL2信号极性设置	0：SSL2信号低电平有效1： SSL2信号高电平有效。	R/W
b3	SSL3P	SSL3信号极性设置	0：SSL3信号低电平有效1： SSL3信号高电平有效。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

注1.该位在SPI1中不可用。

如果SPCR.SPE位为1时SSLP的内容发生变化，则不要进行后续操作。

32.2.3 SPI引脚控制寄存器(SPPCR)

Address(es): SPI0.SPPCR 4007 2002h, SPI1.SPPCR 4007 2102h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SPLP	SPI Loopback	0：正常模式1：环回模式，数据反转传输。	R/W
b1	SPLP2	SPI Loopback 2	0：正常模式1：环回模式，数据不反相传输。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	MOIFV	MOSI空闲固定值	0：MOSI空闲时MOSIn引脚输出低电平1：MOSI空闲时MOSIn引脚输出高电平。	R/W
b5	MOIFE	MOSI空闲值修复Enable	0：MOSI输出值等于上次传输的最终数据1：MOSI输出值等于MOIFV位中设置的值。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

如果SPCR.SPE位为1时SPPCR寄存器的内容发生变化，则不要执行后续操作。

SPLP位（SPI环回）

SPLP位选择SPI引脚的模式。当SPLP位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，如果
SPCR.MSTR位为0。然后SPI连接移位寄存器的输入路径和输出路径，建立环回模式。

SPLP2位（SPI环回2）

SPLP2位选择SPI引脚的模式。当SPLP2位设置为1时，SPI关闭

MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the input path and output path for the shift register, establishing loopback mode.

MOIFV bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period for both SPI0 and SPI1, including the SSL retention period during a burst transfer for the SPI0.

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI in master mode is in an SSL negation period for both SPI0 and SPI1, including the SSL retention period during a burst transfer for the SPI0. When the MOIFE bit is 0, the SPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

32.2.4 SPI Status Register (SPSR)

Address(es): SPI0.SPSR 4007 2003h, SPI1.SPSR 4007 2103h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurs 1: An overrun error occurs.	R/(W)*1
b1	IDLNF	SPI Idle Flag	0: SPI is in idle state 1: SPI is in transfer state.	R
b2	MODF	Mode Fault Error Flag	0: No mode fault error or underrun error occurs 1: A mode fault error or an underrun error occurs.	R/(W)*1
b3	PERF	Parity Error Flag	0: No parity error occurs 1: A parity error occurs.	R/(W)*1
b4	UDRF	Underrun Error Flag	0: A mode fault error occurs (MODF = 1) 1: An underrun error occurs (MODF = 1). This bit is invalid when MODF flag is 0.	R/W*1,*2
b5	SPTEF	SPI Transmit Buffer Empty Flag	0: Data found in the transmit buffer 1: No data in the transmit buffer.	R/(W)*3
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SPRF	SPI Receive Buffer Full Flag	0: No valid data in SPDR/SPDR_HA 1: Valid data found in SPDR/SPDR_HA.	R/(W)*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the UDRF flag at the same time as the MODF flag.
Note 3. The write value should be 1.

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR = 1) and when the RSPCK clock auto-stop function is enabled (SPCR2.SCKASE = 1), an overrun error does not occur and this flag does not become 1. For details, see section 32.3.8.1, Overrun errors.

[Setting condition]

- When the next serial transfer ends when the SPCR.TXMD bit is 0 and the receive buffer is full.

[Clearing condition]

- When SPSR is read while the OVRF flag is 1.

如果SPCR.MSTR位为1，则MISOn引脚和移位寄存器之间，如果MOSIn引脚和移位寄存器之间SPCR.MSTR位为0。然后SPI连接移位寄存器的输入路径和输出路径，建立环回模式。

MOIFV位（MOSI空闲固定值）

如果MOIFE位在主机模式下为1，则MOIFV位决定SPI0和SPI1在SSL否定期间的MOSIn引脚输出值，包括SPI0突发传输期间的SSL保持期。

MOIFE位（MOSI空闲值固定使能）

MOIFE位在主模式的SPI处于SPI0和SPI1的SSL否定周期时固定MOSIn输出值，包括SPI0突发传输期间的SSL保持周期。当MOIFE位为0时，SPI将SSL否定期间上次串行传输的最后一个数据输出到MOSIn引脚。当MOIFE位为1时，SPI将MOIFV位中设置的固定值输出到MOSIn引脚。

32.2.4 SPI状态寄存器(SPSR)

Address(es): SPI0.SPSR 4007 2003h, SPI1.SPSR 4007 2103h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
重置后的值：	0	0	1	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OVRF	溢出错误标志	0：不发生溢出错误1：发生溢出错误。	R/(W)*1
b1	IDLNF	SPI空闲标志	0：SPI处于空闲状态1：SPI处于传输状态。	R
b2	MODF	模式故障错误标志	0：未发生模式故障错误或欠载错误1：发生模式故障错误或欠载错误。	R/(W)*1
b3	PERF	奇偶校验错误标志	0：不发生奇偶校验错误 1：发生奇偶校验错误。	R/(W)*1
b4	UDRF	欠载错误标志	0：发生模式故障错误（MODF=1）1：发生欠载错误（MODF=1）。当MODF标志为0时，该位无效。	R/W*1,*2
b5	SPTEF	SPI发送缓冲区空标志	0：在发送缓冲区中找到数据1：在发送缓冲区中没有数据。	R/(W)*3
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	SPRF	SPI接收缓冲区满标志	0：SPDRSPDR_HA中没有有效数据1：SPDRSPDR_HA中找到有效数据。	R/(W)*3

Note 1. 读1后只能写0清除标志。
Note 2. 在清除MODF标志的同时清除UDRF标志。
Note 3. 写入值应为1。

OVRF标志（溢出错误标志）

OVRF标志指示发生溢出错误。在主机模式(SPCR.MSTR=1)和启用RSPCK时钟自动停止功能(SPCR2.SCKASE=1)时，不会发生溢出错误并且该标志不会变为1。有关详细信息，请参阅第32.3节。8.1，溢出错误。

[Setting condition]

- 当SPCR.TXMD位为0且接收缓冲区已满时，下一次串行传输结束。

[Clearing condition]

- 当OVRF标志为1时读取SPSR。

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

[Setting condition]

Master mode

- When conditions 1. and 2. in the master mode [Clearing condition] are not satisfied.

Slave mode

- When the SPCR.SPE bit is 1, enabling the SPI function.

[Clearing condition]

Master mode

- When either condition 1. is satisfied or conditions 2., 3., and 4. are satisfied for SPI0, and when either condition 1. is satisfied or conditions 2. and 4. are satisfied for SPI1.

1. The SPCR.SPE bit is 0 for SPI initialization.
2. The transmit buffer (SPTX) is empty, meaning data for the next transfer is not set.
3. The SPSSR.SPCP[2:0] bits are 000b, indicating the beginning of sequence control.
4. The SPI internal sequencer is in the idle state, indicating that operations up to the next-access delay are complete.

Slave mode

- When the SPCR.SPE bit is 0 for SPI initialization.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. The UDRF flag indicates which error occurred.

[Setting conditions]

Master mode

- When the input level of the SSLni pin changes to an active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Slave mode

- When either condition 1. or 2. is satisfied.

  1. The SSLni pin is negated before the RSPCK cycle required for data transfer ends, when the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.
  2. The serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), SPCR.SPE bit set to 1, and the transmission data not prepared, triggering an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting).

[Clearing condition]

- When SPSR is read while this flag is 1.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends when the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, triggering a parity error.

[Clearing condition]

- When SPSR is read when the PERF flag is 1.

IDLNF标志（SPI空闲标志）

IDLNF标志指示SPI的传输状态。

[Setting condition]

主模式

- 不满足主模式[清除条件]中的条件1.和2.时。

从机模式

- 当SPCR.SPE位为1时，使能SPI功能。

[Clearing condition]

主模式

- SPI0满足条件1.或条件2.、3.和4.时，以及SPI1.满足条件1.或条件2.和4.时。

1. SPCR.SPE位为0用于SPI初始化。
2. 发送缓冲区(SPTX)为空，意味着未设置下一次传输的数据。
3. SPSSR.SPCP[2:0]位为000b，表示序列控制的开始。
4. SPI内部定序器处于空闲状态，表示直到下一次访问延迟的操作已完成。

从机模式

- 当SPCR.SPE位为0时进行SPI初始化。

MODF标志（模式故障错误标志）

MODF标志指示发生模式故障错误或欠载错误。UDRF标志指示发生了哪个错误。

[Setting conditions]

主模式

- 当SPCR.MSTR位为1（主模式）且SPCR.MODFEN位为1（启用模式故障错误检测）时，当SSLni引脚的输入电平变为有效电平时，触发模式故障错误。

从机模式

- 当满足条件1.或2.时。

  1.在数据传输所需的RSPCK周期结束之前，SSLni引脚被取反，当SPCR.MSTR位为0（从模式）且SPCR.MODFEN位为1（启用模式故障错误检测）时，触发模式故障错误。

  2.串行传输开始时SPCR.MSTR位设置为0（从模式），SPCR.SPE位设置为1，传输数据未准备好，触发欠载错误。

SSLni信号的有效电平由SSLP.SSLiP位（SSLi信号极性设置）确定。

[Clearing condition]

- 当该标志为1时读取SPSR。

PERF标志（奇偶校验错误标志）

PERF标志指示奇偶校验错误的发生。

[Setting condition]

- 当SPCR.TXMD位为0且SPCR2.SPPE位为1时串行传输结束，触发奇偶校验错误。

[Clearing condition]

- 当PERF标志为1时读取SPSR。

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting condition]

- When the serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), SPCR.SPE bit set to 1, and the transmission data not prepared, triggering an underrun error.

[Clearing condition]

- When SPSR is read when the UDRF flag is 1.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- When either condition 1. or 2. is satisfied.
  1. The SPCR.SPE bit is 0 for SPI initialization.
  2. Transmit data is transferred from the transmit buffer to the shift register.

[Clearing condition]

- SPI0: Data written to the SPDR/SPDR_HA register equals the number of frames set by the number of frames specification bits, SPFC[1:0], in the SPI Data Control Register (SPDCR).
- SPI1: Data written to SPDR/SPDR_HA.

Data can only be written to SPDR/SPDR_HA when the SPTEF bit is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF bit is 0, data in the transmit buffer is not updated.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- SPI0: When receive data with the number of frames specified in the SPDCR.SPFC[1:0] bits is transferred from the shift register to SPDR/SPDR_HA, while the SPCR.TXMD bit is 0, and the SPRF flag is 0. When the OVRF flag is 1, however, this flag does not change from 0 to 1.
- SPI1: When receive data is transferred from the shift register to SPDR/SPDR_HA, while the SPCR.TXMD bit is 0, and the SPRF flag is 0. When the OVRF flag is 1, however, this flag does not change from 0 to 1.

[Clearing condition]

- When received data is read from SPDR/SPDR_HA.

UDRF标志（欠载错误标志）

UDRF标志指示发生了欠载错误。

[Setting condition]

- 当串行传输开始时，SPCR.MSTR位设置为0（从模式），SPCR.SPE位设置为1，传输数据未准备好，触发欠载错误。

[Clearing condition]

- 当UDRF标志为1时读取SPSR。

SPTEF标志（SPI发送缓冲区空标志）

SPTEF标志指示SPI数据寄存器(SPDRSPDR_HA)的发送缓冲区的状态。

[Setting conditions]

- 当满足条件1.或2.时。

  1.SPCR.SPE位为0用于SPI初始化。

  2.发送数据从发送缓冲器传送到移位寄存器。

[Clearing condition]

- SPI0：写入SPDRSPDR_HA寄存器的数据等于由SPI数据控制寄存器(SPDCR)中的帧数规范位SPFC[1:0]设置的帧数。
- SPI1：数据写入SPDRSPDR_HA。

数据只能在SPTEF位为1时写入SPDRSPDR_HA。如果数据写入SPDR的发送缓冲区SPDR_HA当SPTEF位为0时，发送缓冲区中的数据不更新。

SPRF标志（SPI接收缓冲区满标志）

SPRF标志指示SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区的状态。

[Setting conditions]

- SPI0：当接收到SPDCR.SPFC[1:0]位指定帧数的数据从移位寄存器传送到SPDRSPDR_HA时，SPCR.TXMD位为0，SPRF标志位为0。OVRF标志为1，但是，该标志不会从0变为1。
- SPI1：当接收数据从移位寄存器传送到SPDRSPDR_HA时，SPCR.TXMD位为0，SPRF标志为0。然而，当OVRF标志为1时，该标志不会从0变为1。

[Clearing condition]

- 当从SPDRSPDR_HA读取接收到的数据时。

32.2.5 SPI Data Register (SPDR/SPDR_HA)

Address(es): SPI0.SPDR 4007 2004h, SPI1.SPDR 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): SPI0.SPDR_HA 4007 2004h, SPI1.SPDR_HA 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SPDR/SPDR_HA register is the interface with the buffers that hold data for transmission and reception by the SPI.

When accessing this register in words (SPLW = 1), access the SPDR register. When accessing it in halfwords (SPLW = 0), access the SPDR_HA register.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA. Figure 32.2 and Figure 32.3 show the configuration of the SPDR/SPDR_HA register for SPI0 and SPI1 channels, respectively.

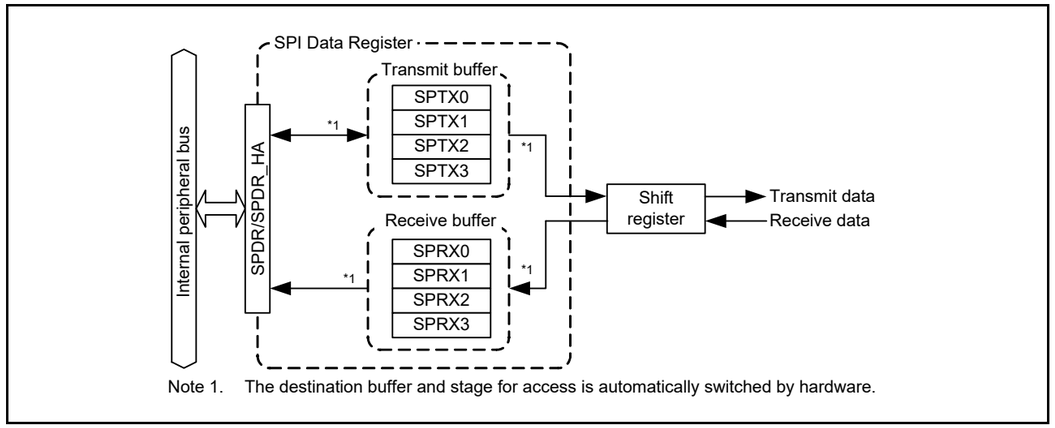


Figure 32.2 Configuration of SPDR/SPDR_HA (SPI0)

32.2.5 SPI数据寄存器(SPDRSPDR_HA)

Address(es): SPI0.SPDR 4007 2004h, SPI1.SPDR 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): SPI0.SPDR_HA 4007 2004h, SPI1.SPDR_HA 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDRSPDR_HA寄存器是与保存数据以供SPI发送和接收的缓冲区的接口。

当以字（SPLW=1）访问该寄存器时，访问SPDR寄存器。以半字(SPLW=0)访问时，访问SPDR_HA寄存器。

发送缓冲区(SPTX)和接收缓冲区(SPRX)是独立的，但都映射到SPDRSPDR_HA。图32.2和图32.3分别显示了SPI0和SPI1通道的SPDRSPDR_HA寄存器的配置。

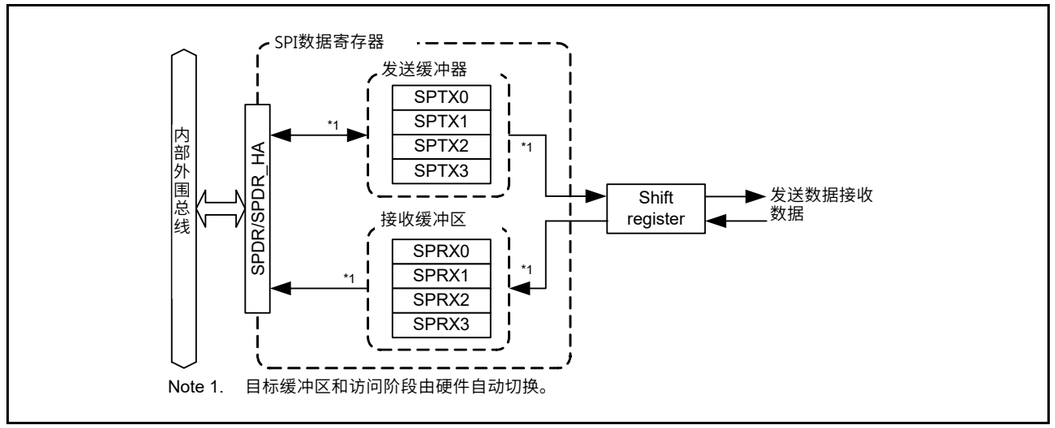


Figure 32.2 SPDRSPDR_HA(SPI0)的配置

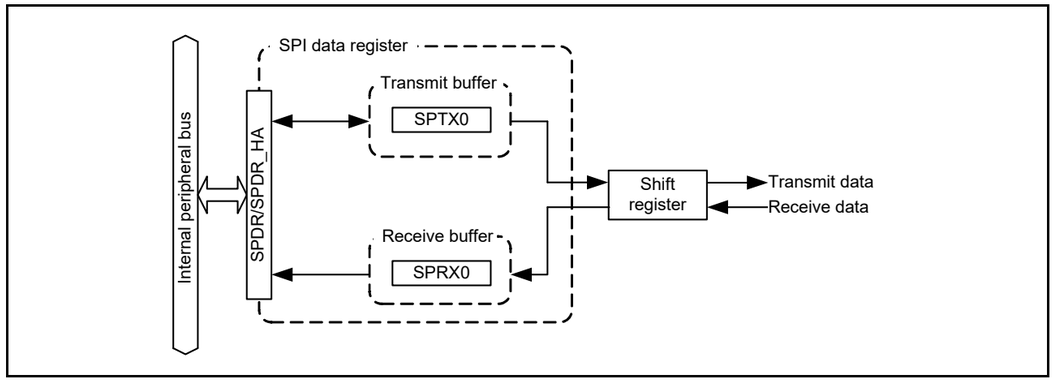


Figure 32.3 Configuration of SPDR/SPDR_HA (SPI1)

The transmit and receive buffers each have four stages for SPI0 and one stage for SPI1. The number of stages used for SPI0 is selectable by the number of frames specification bits, SPDCR, in the SPDCR register. These stages of the buffer are all mapped to the single address of the SPDR/SPDR_HA register.

Data written to the SPDR/SPDR_HA register is written to a transmit-buffer stage (SPTXn) (n = 0 to 3 for SPI0, n = 0 for SPI1), and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.

If the data length is not 32 bits, the bits not referred to in SPTXn (n = 0 to 3 for SPI0, n = 0 for SPI1) are stored in the associated bits in SPRXn (n = 0 to 3 for SPI0, n = 0 for SPI1). For example, if the data length is 9 bits, received data is stored in the SPRXn[8:0] bits and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus interface

SPDR/SPDR_HA is an interface with 32-bit wide transmit and receive buffers, each of which has four stages for SPI0 and one stage for SPI1, for a total of 32 bytes. The 32 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA. The unit of access for SPDR/SPDR_HA is selected in the SPI word access/halfword access specification bit, SPLW, in the SPDCR register.

Flush the transmission data at the LSB end of the register and store the received data at the LSB end.

The following sections describe the operations involved in writing to and reading from the SPDR/SPDR_HA register.

(a) Writing

Data written to SPDR/SPDR_HA is written to a transmit buffer SPTXn (n = 0 to 3 for SPI0, n = 0 for SPI1). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA.

The transmit buffer includes a write pointer that is automatically updated to reference the next stage each time data is written to SPDR/SPDR_HA.

Figure 32.4 and Figure 32.5 show the configuration of the bus interface with the transmit buffer, for writes to SPDR/SPDR_HA, for SPI0 and SPI1 respectively.

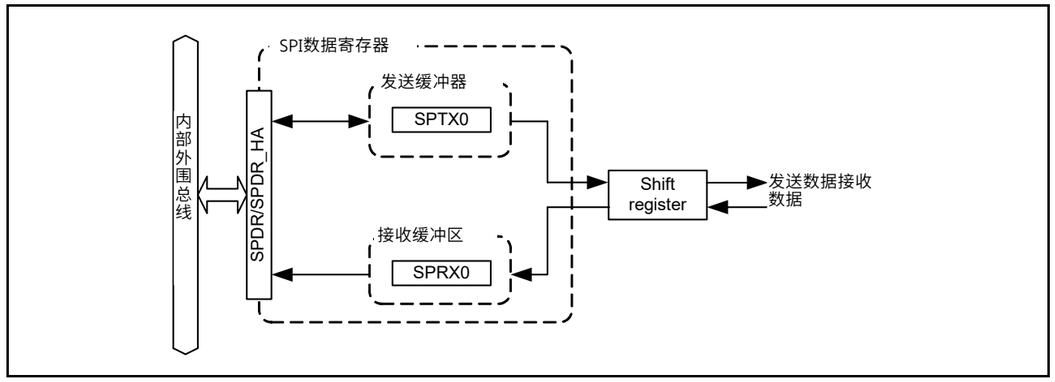


Figure 32.3 SPDRSPDR_HA(SPI1)的配置

发送和接收缓冲器各有四个用于SPI0的级和一个用于SPI1的级。用于的阶段数
SPI0可通过SPDCR寄存器中的帧数规范位SPDCR进行选择。缓冲区的这些阶段都映射到SPDRSPDR_HA寄存器的单个地址。

写入SPDRSPDR_HA寄存器的数据被写入发送缓冲级(SPTXn)（对于SPI0，n=0到3，对于SPI0，n=0
SPI1)，然后从缓冲区传输。接收缓冲器在接收完成时保存接收到的数据。如果产生溢出，接收缓冲区不会更新。

如果数据长度不是32位，则SPTXn中未提及的位（对于SPI0，n=0到3，对于SPI1，n=0）存储在SPRXn的相关位中（对于SPI0，n=0到3，n=0为SPI1)。例如，如果数据长度为9位，则接收到的数据存储在SPRXn[8:0]位中，而SPTXn[31:9]位存储在SPRXn[31:9]位中。

(1) 总线接口

SPDRSPDR_HA是一个具有32位宽的发送和接收缓冲区的接口，每个缓冲区有SPI0的4级和SPI1的1级，共32字节。32个字节映射到SPDRSPDR_HA的4字节地址空间。SPDRSPDR_HA的访问单元在SPI字访问半字访问规范位中选择，

SPLW，在SPDCR寄存器中。

在寄存器的LSB端刷新发送数据，在LSB端存储接收到的数据。

以下部分描述了写入和读取SPDRSPDR_HA寄存器所涉及的操作。

(a) Writing

写入SPDRSPDR_HA的数据被写入发送缓冲器SPTXn（对于SPI0，n=0到3，对于SPI1，n=0）。这不受SPDCR.SPRDTD位值的影响，这与从SPDRSPDR_HA读取时不同。

发送缓冲区包括一个写指针，每次将数据写入SPDRSPDR_HA时，该写指针会自动更新以引用下一阶段。

图32.4和图32.5显示了带有发送缓冲器的总线接口配置，用于写入SPDR
SPDR_HA，分别用于SPI0和SPI1。

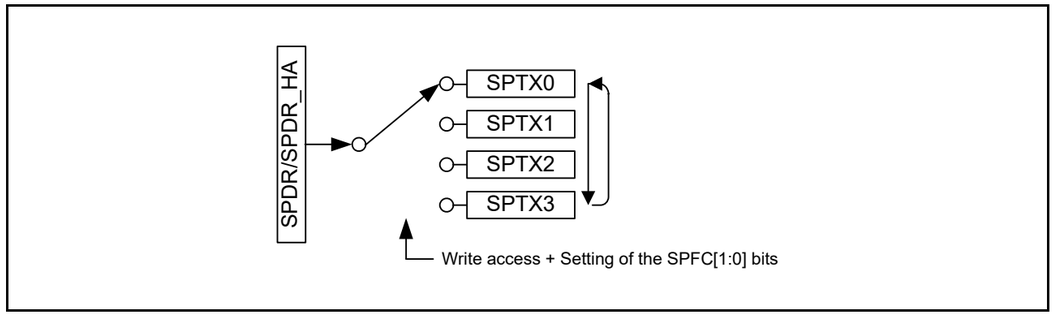


Figure 32.4 Configuration of SPDR/SPDR_HA for write access (SPI0)

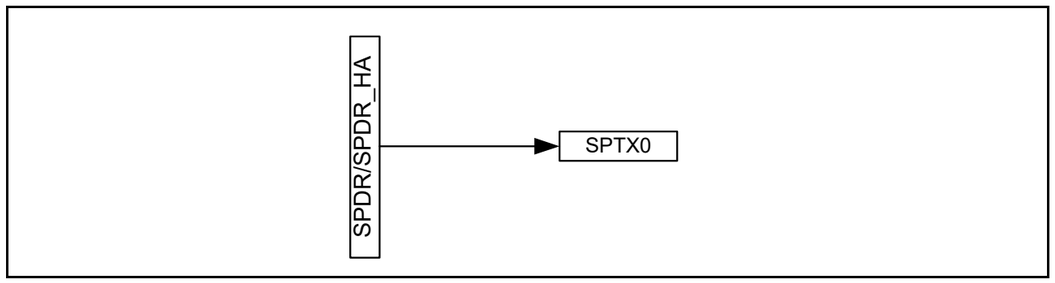


Figure 32.5 Configuration of SPDR/SPDR_HA for write access (SPI1)

For SPI0, the sequence for switching the transmit buffer write pointer changes with the setting of the number of frames specification bits, SPFC[1:0], in the SPDCR register.

- Settings of the SPFC[1:0] bits and sequence of switching the pointer from SPTX0 to SPTX3:
  When the SPFC[1:0] bits are 00b: SPTX0 → SPTX0 → SPTX0 → …
  When the SPFC[1:0] bits are 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the SPI function enable bit, SPE, in the SPI Control Register (SPCR) while the bit is 0, SPTX0 is the destination for the next write.

When writing to the transmit buffer SPTXn (n = 0 to 3 for SPI0, n = 0 for SPI1) after generating the transmit buffer empty interrupt (when SPSR.SPTEF is 1), write the number of frames set in the number of frames specification bits, SPFC[1:0], in the SPDCR register. The value of the buffer is not updated after completion of the writing and before the next transmit buffer empty interrupt is generated (SPSR.SPTEF = 0), even when the number of frames is written to the transmit buffer (SPTXn).

(b) Reading

SPDR/SPDR_HA can be accessed to read the value of a receive buffer SPRXn (n = 0 to 3 for SPI0, n = 0 for SPI1) or a transmit buffer SPTXn (n = 0 to 3 for SPI0, n = 0 for SPI1). The setting of the SPI receive or transmit data select bit, SPRDTD, in the SPDCR register selects whether reading is from the receive or transmit buffer.

The sequence of reading the SPDR/SPDR_HA register is controlled by the independent pointers, receive buffer read pointer and transmit buffer read pointer.

Figure 32.6 and Figure 32.7 show the configuration of a bus interface with the receive and transmit buffers for reading from SPDR/SPDR_HA for SPI0 and SPI1, respectively.

- SPI0

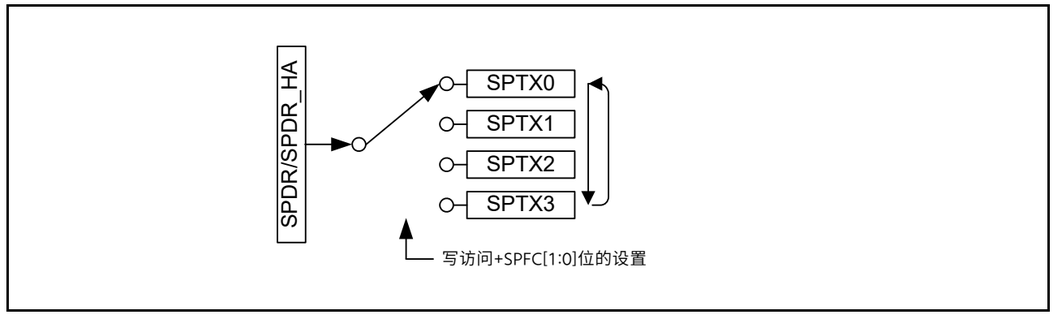


Figure 32.4 用于写访问(SPI0)的SPDRSPDR_HA配置

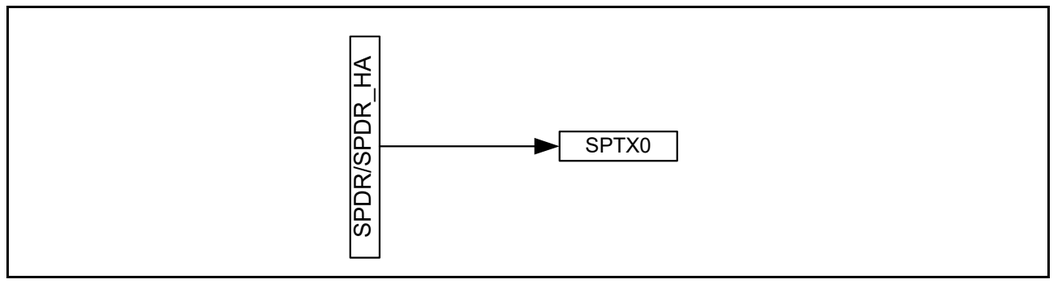


Figure 32.5 用于写访问(SPI1)的SPDRSPDR_HA配置

对于SPI0，切换发送缓冲区写指针的顺序随SPDCR寄存器中帧数规范位SPFC[1:0]的设置而变化。

- SPFC[1:0]位的设置和指针从SPTX0切换到SPTX3的顺序：
  当SPFC[1:0]位为00b时：SPTX0→SPTX0→SPTX0→…
  SPFC[1:0]位为01b时：SPTX0→SPTX1→SPTX0→SPTX1→…
  SPFC[1:0]位为10b时：SPTX0→SPTX1→SPTX2→SPTX0→SPTX1→…
  SPFC[1:0]位为11b时：SPTX0→SPTX1→SPTX2→SPTX3→SPTX0→SPTX1→…

当1写入SPI控制寄存器(SPCR)中的SPI功能使能位SPE而该位为0时，SPTX0是下一次写入的目标。

在产生发送缓冲区空中断（当SPSR.SPTEF为1时）后写入发送缓冲区SPTXn（SPI0为n=0至3，SPI1为n=0）时，写入帧数规范中设置的帧数SPDCR寄存器中的位SPFC[1:0]。在写入完成后和下一个发送缓冲区空中断产生之前（SPSR.SPTEF=0），缓冲区的值不会更新，即使帧数已写入发送缓冲区（SPTXn）。

(b) Reading

可以访问SPDRSPDR_HA以读取接收缓冲区SPRXn（对于SPI0，n=0到3，对于SPI1，n=0）或发送缓冲区SPTXn（对于SPI0，n=0到3，对于SPI1，n=0）的值。SPDCR寄存器中的SPI接收或发送数据选择位SPRDTD的设置选择是从接收缓冲区还是从发送缓冲区读取。

读取SPDRSPDR_HA寄存器的顺序由独立指针、接收缓冲区读取指针和发送缓冲区读取指针控制。

图32.6和图32.7显示了总线接口的配置，其中接收和发送缓冲区分别用于从SPI0和SPI1的SPDRSPDR_HA读取。

- SPI0

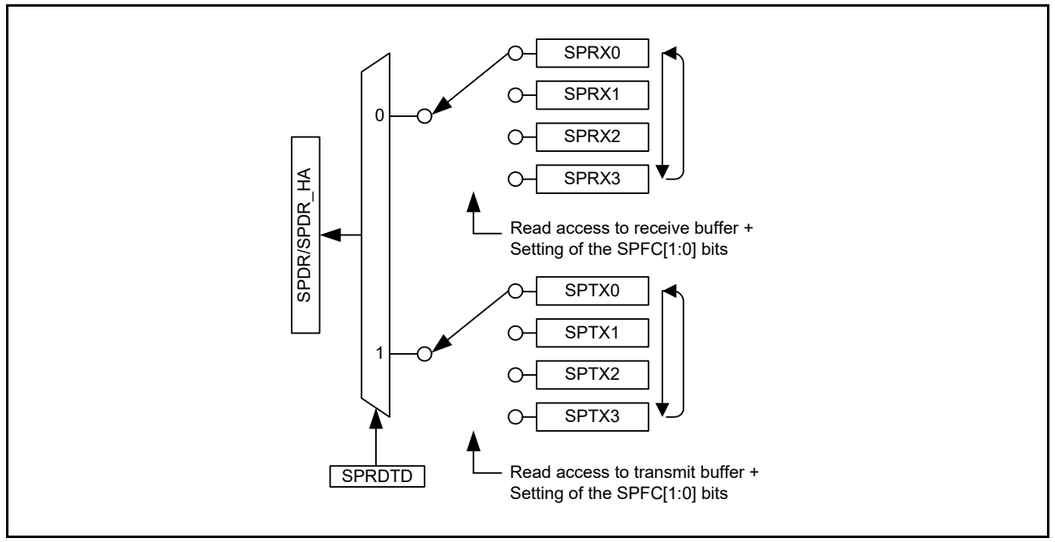


Figure 32.6 Configuration of SPDR/SPDR_HA for read access (SPI0)

Reading the receive buffer switches the receive buffer read pointer to the next buffer automatically. The sequence of switching the receive buffer read pointer is the same as that for the transmit buffer write pointer.

However, when 1 is written to the SPI function enable bit, SPE, in the SPI Control Register (SPCR) when the bit is 1, SPRX0 is referenced by the buffer read pointer for the next read.

The transmit buffer read pointer is updated when writing to SPDR/SPDR_HA, but is not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR/SPDR_HA is read. However, after a transmit buffer empty interrupt is generated, and when the transmit buffer becomes full again (the number of frames of data specified in the number of frames specification bits, SPDCR.SPFC[1:0], are written to the transmit buffer), reading from the transmit buffer returns all 0s until the next transmit buffer empty interrupt is generated.

- SPI1

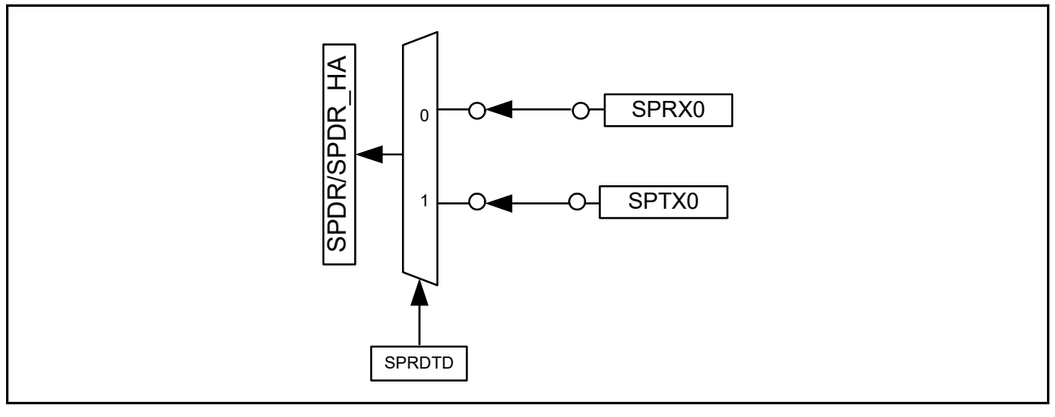


Figure 32.7 Configuration of SPDR/SPDR_HA for read access (SPI1)

The transmit buffer read pointer is updated when writing to SPDR/SPDR_HA, and not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR/SPDR_HA is read. However, after a transmit buffer empty interrupt is generated, and when the transmit buffer becomes full again, reading from the transmit buffer returns all 0s until the next transmit buffer empty interrupt is generated (when SPTEF is 0).

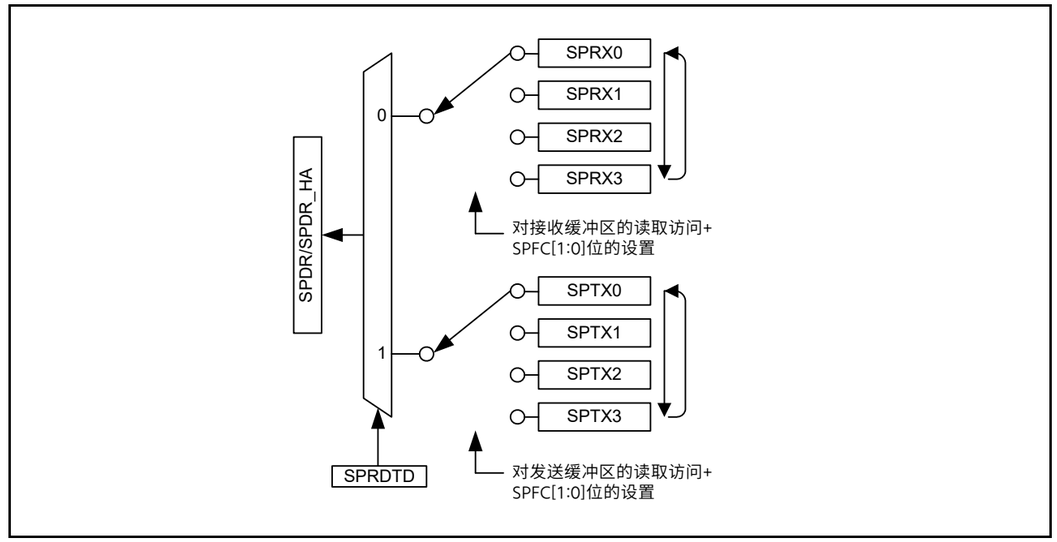


Figure 32.6 用于读取访问(SPI0)的SPDRSPDR_HA配置

读取接收缓冲区会自动将接收缓冲区读取指针切换到下一个缓冲区。接收缓冲区读指针的切换顺序与发送缓冲区写指针的切换顺序相同。

但是，当SPI控制寄存器(SPCR)中的SPI功能使能位SPE为1时写入1，SPRX0由缓冲区读取指针引用以进行下一次读取。

发送缓冲区读指针在写入SPDRSPDR_HA时更新，但在从发送缓冲区读取时不更新。从发送缓冲区读取时，会读取最近写入SPDRSPDR_HA的值。但是，在产生发送缓冲区空中断后，并且当发送缓冲区再次变满时（帧数指定位SPDCR.SPFC[1:0]中指定的数据帧数被写入发送缓冲区），从发送缓冲区读取返回全0，直到产生下一个发送缓冲区空中断。

- SPI1

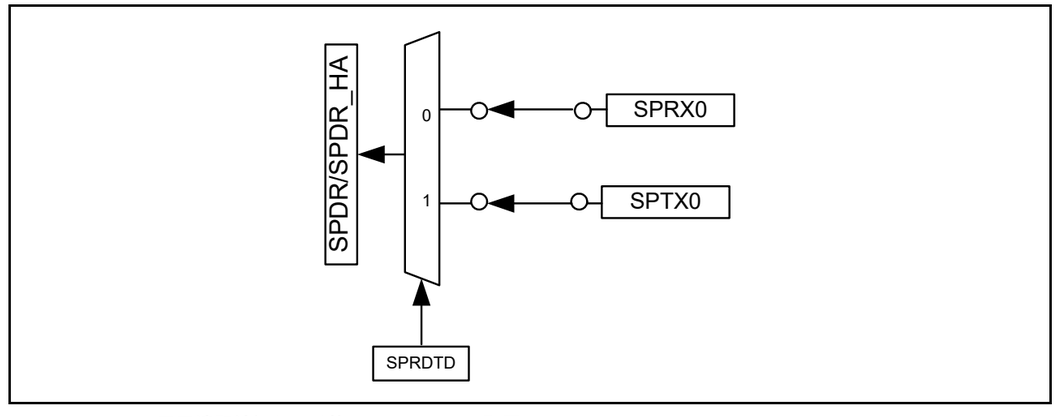


Figure 32.7 用于读取访问(SPI1)的SPDRSPDR_HA配置

发送缓冲区读指针在写入SPDRSPDR_HA时更新，而在从发送缓冲区读取时不更新。从发送缓冲区读取时，会读取最近写入SPDRSPDR_HA的值。但是，在产生发送缓冲区空中断后，并且当发送缓冲区再次变满时，从发送缓冲区读取将返回全0，直到产生下一个发送缓冲区空中断（当SPTEF为0时）。

32.2.6 SPI Sequence Control Register (SPSCR)

Address(es): SPI0.SPSCR 4007 2008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPSLN[2:0]	SPI Sequence Length Specification	b2 b0 Sequence Length — Referenced SPCMD0 to SPCMD7 (Number) 0 0 0: 1 — 0→0→… 0 0 1: 2 — 0→1→0→… 0 1 0: 3 — 0→1→2→0→… 0 1 1: 4 — 0→1→2→3→0→… 1 0 0: 5 — 0→1→2→3→4→0→… 1 0 1: 6 — 0→1→2→3→4→5→0→… 1 1 0: 7 — 0→1→2→3→4→5→6→0→… 1 1 1: 8 — 0→1→2→3→4→5→6→7→0→… The order in which the SPCMD0 to SPCMD07 registers are referenced is changed based on the sequence length that is set in these bits. The relationship between the setting of these bits, sequence length, and the SPCMD0 to SPCMD7 registers referenced by the SPI is shown. However, the SPI in slave mode references SPCMD0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPSCR register sets the sequence length when the SPI operates in master mode. When changing the SPSCR.SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, always check that the SPSR.IDLNF flag is 0.

SPSLN[2:0] bits (SPI Sequence Length Specification)

The SPSLN[2:0] bits specify a sequence length when the SPI in master mode performs sequential operations. The SPI in master mode changes the SPCMD0 to SPCMD7 registers to be referenced, and the order in which they are referenced is based on the sequence length that is set in the SPSLN[2:0] bits. In slave mode, SPCMD0 is referenced.

32.2.7 SPI Sequence Status Register (SPSSR)

Address(es): SPI0.SPSSR 4007 2009h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPCP[2:0]	SPI Command Pointer	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b3	—	Reserved	This bit is read as 0.	R

32.2.6 SPI序列控制寄存器(SPSCR)

Address(es): SPI0.SPSCR 4007 2008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SPSLN[2:0]	SPI序列长度 Specification	b2b0参考SPCMD0到SPCMD7的序列长度（编号）000：10→0→…001：20→1→0→…010：30→1→2→0→…011:40→1→2→3→0→…100:50→1→2→3→4→0→…101:60→1→2→3→4→5→0→…110:70→1→2→3→4→5→6→0→…111:80→1→2→3→4→5→6→7→0→…中的顺序SPCMD0到SPCMD07寄存器被引用的位置会根据这些位中设置的序列长度进行更改。显示了这些位的设置、序列长度和SPI引用的SPCMD0到SPCMD7寄存器之间的关系。但是，从机模式下的SPI参考SPCMD0。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SPSCR寄存器设置SPI在主模式下工作时的序列长度。当改变SPSCR.SPSLN[2:0]位当SPCR.MSTR和SPCR.SPE位均为1时，始终检查SPSR.IDLNF标志是否为0。

SPSLN[2:0]位（SPI序列长度规范）

SPSLN[2:0]位指定当SPI在主模式下执行顺序操作时的序列长度。主模式下的SPI将SPCMD0到SPCMD7寄存器更改为被引用，它们被引用的顺序基于SPSLN[2:0]位中设置的序列长度。在从模式下，以SPMD0为参考。

32.2.7 SPI序列状态寄存器(SPSSR)

Address(es): SPI0.SPSSR 4007 2009h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SPCP[2:0]	SPI命令指针	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b3	—	Reserved	该位读为0。	R

Bit	Symbol	Bit name	Description	R/W
b6 to b4	SPECM[2:0]	SPI Error Command	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b7	—	Reserved	This bit is read as 0.	R

The SPSSR register indicates the sequence control status when the SPI operates in master mode. Any writing to SPSSR is ignored.

SPCP[2:0] bits (SPI Command Pointer)

The SPCP[2:0] bits indicate the SPCMDm register that is referenced to by the pointer during sequence control by the SPI. For the SPI sequence control, see section 32.3.10.1, Master mode operation.

SPECM[2:0] bits (SPI Error Command)

The SPECM[2:0] bits indicate the SPCMDm register that is specified by the SPCP[2:0] bits when an error is detected during sequence control by the SPI. The SPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF flags are 0 and there is no error, the SPECM[2:0] bit values have no meaning.

For the SPI error detection function, see section 32.3.8, Error Detection. For the SPI sequence control, see section 32.3.10.1, Master mode operation.

32.2.8 SPI Bit Rate Register (SPBR)

Address(es): SPI0.SPBR 4007 200Ah, SPI1.SPBR 4007 210Ah

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

The SPBR register sets the bit rate in master mode. If the contents of the SPBR register are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

When the SPI is in slave mode, the bit rate depends on the bit rate of the input clock, regardless of the settings in the SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting bits). Use bit rates that satisfy the electrical characteristics of the device.

The bit rate is determined by combination of the SPBR and BRDV[1:0] settings in the SPI Command Register, SPCMDm (SPCMD0 to SPCMD7 for SPI0, SPCMD0 for SPI1). The equation for calculating the bit rate is given as follows:

$$\text{Bit rate} = \frac{f(\text{PCLK})}{2 \times (n + 1) \times 2^N}$$

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] bit setting (0, 1, 2, 3).

Table 32.3 lists examples of the relationship between the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 32.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates (1 of 2)

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate	
			PCLK = 32 MHz	PCLK = 48 MHz
0	0	2	16.0 Mbps	-

Bit	Symbol	位名称	Description	R/W
b6 to b4	SPECM[2:0]	SPI错误命令	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b7	—	Reserved	该位读为0。	R

SPSSR寄存器指示SPI在主模式下工作时的序列控制状态。对SPSSR的任何写入都将被忽略。

SPCP[2:0]位（SPI命令指针）

SPCP[2:0]位指示在序列控制期间由指针引用的SPCMDm寄存器
SPI。对于SPI序列控制，请参见第32.3.10.1节，主模式操作。

SPECM[2:0]位（SPI错误命令）

SPECM[2:0]位指示在SPI序列控制期间检测到错误时由SPCP[2:0]位指定的SPCMDm寄存器。SPI仅在检测到错误时更新SPECM[2:0]位。如果SPSR.OVRF和SPSR.MODF标志均为0且没有错误，则SPECM[2:0]位值没有意义。

关于SPI错误检测功能，请参见第32.3.8节，错误检测。对于SPI序列控制，请参见第32.3.10.1节，主模式操作。

32.2.8 SPI比特率寄存器（SPBR）

Address(es): SPI0.SPBR 4007 200Ah, SPI1.SPBR 4007 210Ah

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

SPBR寄存器设置主机模式下的比特率。如果SPBR寄存器的内容发生变化，而两者SPCR.MSTR和SPCR.SPE位为1，不执行后续操作。

当SPI处于从机模式时，比特率取决于输入时钟的比特率，与SPBR和SPMDm.BRDV[1:0]位（比特率划分设置位）。使用满足设备电气特性的比特率。

比特率由SPI命令寄存器中的SPBR和BRDV[1:0]设置组合确定，SPCMDm（SPI0为SPCMD0至SPCMD7，SPI1为SPCMD0）。计算比特率的公式如下：

$$\text{比特率} = \frac{f(\text{PCLK})}{2 \times (n + 1) \times 2^N}$$

在等式中，n表示SPBR设置(0 1 2 … 255)，N表示BRDV[1:0]位设置(0 1 2 3)。

表32.3列出了SPBR设置、BRDV[1:0]设置和比特率之间的关系示例。

Table 32.3 SPBR设置、BRDV[1:0]设置和比特率之间的关系（1of2）

SPBR (n)	BRDV[1:0] bits (N)	分工比	比特率	
			PCLK = 32 MHz	PCLK = 48 MHz
0	0	2	16.0 Mbps	-

Table 32.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates (2 of 2)

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate	
			PCLK = 32 MHz	PCLK = 48 MHz
1	0	4	8.00 Mbps	12.0 Mbps
2	0	6	5.33 Mbps	8.00 Mbps
3	0	8	4.00 Mbps	6.00 Mbps
4	0	10	3.20 Mbps	4.80 Mbps
5	0	12	2.67 Mbps	4.00 Mbps
5	1	24	1.33 Mbps	2.00 Mbps
5	2	48	667 kbps	1.00 Mbps
5	3	96	333 kbps	500 kbps
255	3	4096	7.81 kbps	11.7 kbps

32.2.9 SPI Data Control Register (SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh

	b7	b6	b5	b4	b3	b2	b1	b0
(SPI0)	—	—	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Address(es): SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
(SPI1)	—	—	SPLW	SPRDTD	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SPFC[1:0]	Number of Frames Specification	• SPI0: b1 b0 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames.	R/W
	—	Reserved	• SPI1: These bits are read as 0. The write value should be 0.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	SPI Receive/Transmit Data Select	0: Read SPDR/SPDR_HA values from the receive buffer 1: Read SPDR/SPDR_HA values from the transmit buffer (but only if the transmit buffer is empty).	R/W
b5	SPLW	SPI Word Access/Halfword Access Specification	0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Up to four frames for SPI0 and one frame for SPI1 can be transmitted or received in one round of transmission or reception. The amount of data in each transfer for SPI0 is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits. The amount of data in each transfer for SPI1 is controlled by the combination of the SPCMD0.SPB[3:0] bits.

When changing the SPDCR.SPFC[1:0] bits while the SPCR.SPE bit is 1, always check that the SPSR.IDLNF flag is 0.

SPFC[1:0] bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR/SPDR_HA (per transfer activation). Up to four frames can be transmitted or received in one round of transmission or reception.

Table 32.3 SPBR设置、BRDV[1:0]设置和比特率之间的关系(2of2)

SPBR (n)	BRDV[1:0] bits (N)	分工比	比特率	
			PCLK = 32 MHz	PCLK = 48 MHz
1	0	4	8.00 Mbps	12.0 Mbps
2	0	6	5.33 Mbps	8.00 Mbps
3	0	8	4.00 Mbps	6.00 Mbps
4	0	10	3.20 Mbps	4.80 Mbps
5	0	12	2.67 Mbps	4.00 Mbps
5	1	24	1.33 Mbps	2.00 Mbps
5	2	48	667 kbps	1.00 Mbps
5	3	96	333 kbps	500 kbps
255	3	4096	7.81 kbps	11.7 kbps

32.2.9 SPI数据控制寄存器(SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh

	b7	b6	b5	b4	b3	b2	b1	b0
(SPI0)	—	—	SPLW	SPRDTD	—	—	SPFC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Address(es): SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
(SPI1)	—	—	SPLW	SPRDTD	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	SPFC[1:0]	帧数 Specification	SPI0: b1b000 : 1帧01: 2帧 10: 3帧11: 4 帧。	R/W
	—	Reserved	SPI1: 这些位被读取为0。写入值应为0。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SPRDTD	SPI接收发送数据 Select	0: 从接收缓冲区读取SPDRSPDR_HA值1: 从发送缓冲区读取SPDRSPDR_HA值（但仅当发送缓冲区为空时）。	R/W
b5	SPLW	SPI字访问半字 访问规范	0: 将SPDR_HA设置为对半字访问有效1: 将SPDR设置为对字访问有效。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

在一轮发送或接收中最多可以发送或接收SPI0四个帧和SPI1一个帧。SPI0每次传输的数据量由SPCMDm.SPB[3:0]位、SPSCR.SPSLN[2:0]位和SPDCR.SPFC[1:0]位的组合控制。SPI1每次传输的数据量由SPCMD0.SPB[3:0]位的组合控制。

在SPCR.SPE位为1时更改SPDCR.SPFC[1:0]位时，请始终检查SPSR.IDLNF标志是否为0。

SPFC[1:0]位（帧数规范）

SPFC[1:0]位指定可以存储在SPDRSPDR_HA中的帧数（每次传输激活）。在一轮发送或接收中最多可以发送或接收四帧。

When the transmission data with the number of frames specified by the SPFC[1:0] bits are written to the SPDR/SPDR_HA register, the SPI clears the SPSR.SPTEF flag to 0 and begins transmitting. After that, when the transmission data with the number of frames specified by the SPFC[1:0] bits are transmitted to the shift register, the SPI generates a transmission buffer empty interrupt (SPSR.SPTEF = 1).

When the data with the number of frames specified by the SPFC[1:0] bits is received, the SPI generates a receive buffer full interrupt (SPSR.SPRF = 1).

The SPFC[1:0] bits are reserved for SPI1.

Table 32.4 Settable combinations of SPSLN[2:0] bits and SPFC[1:0] bits

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or reception buffer is filled
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA register reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to the SPDR/SPDR_HA register is read. Reading the transmit buffer for SPI0 must take place before the writing of the number of frames set in the SPFC[1:0] bits is finished and after generation of the transmit buffer empty interrupt (SPSR.SPTEF = 1). Reading the transmit buffer for SPI1 must be done after generation of the transmit buffer empty interrupt (SPSR.SPTEF = 1).

For details, see section 32.2.5, SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for the SPDR register. Access to the SPDR_HA register in halfwords is valid when the SPLW bit is 0 and access to the SPDR register in words is valid when the SPLW bit is 1. In addition, when the SPLW bit is 0, set the SPI data length setting bits, SPCMDm.SPB[3:0], from 8 to 16 bits. When a data length of 20, 24, or 32 bits is specified, do not perform any operations.

当SPFC[1:0]位指定的帧数的传输数据写入SPDR时
SPDR_HA寄存器，SPI将SPSR.SPTEF标志清0并开始发送。之后，当SPFC[1:0]位指定的帧数的传输数据被传输到移位寄存器时，SPI产生传输缓冲区空中断（SPSR.SPTEF=1）。

当接收到SPFC[1:0]位指定的帧数的数据时，SPI会产生接收缓冲区满中断(SPSR.SPRF=1)。

SPFC[1:0]位为SPI1保留。

Table 32.4 SPSLN[2:0]位和SPFC[1:0]位的可设置组合

Setting	SPSLN[2:0]	SPFC[1:0]	单个序列中的帧数	填充发送或接收缓冲区的帧数
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD位（SPI接收发送数据选择）

SPRDTD位选择SPDRSPDR_HA寄存器是从接收缓冲区还是从发送缓冲区读取值。如果从发送缓冲区读取，则读取写入SPDRSPDR_HA寄存器的最后一个值。SPI0发送缓冲区的读取必须在SPFC[1:0]位中设置的帧数写入完成之前和发送缓冲区空中断(SPSR.SPTEF=1)生成之后进行。必须在产生发送缓冲区空中断(SPSR.SPTEF=1)后读取SPI1的发送缓冲区。

有关详细信息，请参见第32.2.5节，SPI数据寄存器(SPDRSPDR_HA)。

SPLW位（SPI字访问半字访问规范）

SPLW位指定SPDR寄存器的访问宽度。当SPLW位为0时，以半字访问SPDR_HA寄存器有效，当SPLW位为1时，以字访问SPDR寄存器有效。另外，当SPLW位为0时，设置SPI数据长度设置位，SPMDm.SPB[3:0]，8到16位。当指定数据长度为20、24或32位时，不要执行任何操作。

32.2.10 SPI Clock Delay Register (SPCKD)

Address(es): SPI0.SPCKD 4007 200Ch, SPI1.SPCKD 4007 210Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b0 0 0: 1 RSPCK 0 1: 2 RSPCK 1 0: 3 RSPCK 1 1: 4 RSPCK 0 0: 5 RSPCK 0 1: 6 RSPCK 1 0: 7 RSPCK 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPCKD register sets a period from the beginning of SSLni signal assertion to RSPCK oscillation (RSPCK delay) when the SPCMDm.SCKDEN bit is 1. If the contents of the SPCKD register are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits set an RSPCK delay value when the SPCMDm.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

32.2.11 SPI Slave Select Negation Delay Register (SSLND)

Address(es): SPI0.SSLND 4007 200Dh, SPI1.SSLND 4007 210Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0: 1 RSPCK 0 0: 2 RSPCK 0 1: 3 RSPCK 0 1: 4 RSPCK 1 0: 5 RSPCK 1 0: 6 RSPCK 1 1: 7 RSPCK 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SSLND register sets a period (SSL negation delay) from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of the SSLND register are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits set an SSL negation delay value when the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

32.2.10 SPI时钟延迟寄存器(SPCKD)

Address(es): SPI0.SPCKD 4007 200Ch, SPI1.SPCKD 4007 210Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK延迟设置	b2 b0 0 0: 1 RSPCK 0 0: 2 RSPCK 0 1: 3 RSPCK 0 1: 4 RSPCK 1 0: 5 RSPCK 1 0: 6 RSPCK 1 1: 7 RSPCK 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SPCMDm.SCKDEN位为1时，SPCKD寄存器设置从SSLni信号断言开始到RSPCK振荡（RSPCK延迟）的周期。如果在SPCR.MSTR和SPCR.SPE位都为1时改变了SPCKD寄存器的内容1、不要进行后续操作。

SCKDL[2:0]位（RSPCK延迟设置）

当SPCMDm.SCKDEN位为1时，SCKDL[2:0]位设置RSPCK延迟值。在从机模式下使用SPI时，将SCKDL[2:0]位设置为000b。

32.2.11 SPI从机选择否定延迟寄存器(SSLND)

Address(es): SPI0.SSLND 4007 200Dh, SPI1.SSLND 4007 210Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SLNDL[2:0]	SSL否定延迟设置	b2 b0 0 0: 1 RSPCK 0 0: 2 RSPCK 0 1: 3 RSPCK 0 1: 4 RSPCK 1 0: 5 RSPCK 1 0: 6 RSPCK 1 1: 7 RSPCK 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SSLND寄存器设置一个周期（SSL否定延迟），从发送最终RSPCK边沿到否定SSLni信号期间由SPI在主模式下进行串行传输。如果在SPCR.MSTR和SPCR.SPE位均为1时SSLND寄存器的内容发生了变化，则不要执行后续操作。

SLNDL[2:0]位（SSL否定延迟设置）

SLNDL[2:0]位在SPI处于主模式时设置SSL否定延迟值。在从机模式下使用SPI时，将SLNDL[2:0]位设置为000b。

32.2.12 SPI Next-Access Delay Register (SPND)

Address(es): SPI0.SPND 4007 200Eh, SPI1.SPND 4007 210Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPNDL[2:0]	SPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 PCLK 0 0 1: 2 RSPCK + 2 PCLK 0 1 0: 3 RSPCK + 2 PCLK 0 1 1: 4 RSPCK + 2 PCLK 1 0 0: 5 RSPCK + 2 PCLK 1 0 1: 6 RSPCK + 2 PCLK 1 1 0: 7 RSPCK + 2 PCLK 1 1 1: 8 RSPCK + 2 PCLK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPND register sets the non-active period (next-access delay) of the SSLni signal after termination of a serial transfer when the SPCMDm.SPNDEN bit is 1. If the contents of the SPND register are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits set the next-access delay when the SPCMDm.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

32.2.13 SPI Control Register 2 (SPCR2)

Address(es): SPI0.SPCR2 4007 200Fh, SPI1.SPCR2 4007 210Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPPE	Parity Enable	0: No parity bit added to transmit data and parity bit of receive data not checked 1: Parity bit added to transmit data and parity bit of receive data checked (when SPCR.TXMD = 0). Parity bit added to transmit data but parity bit of receive data not checked (when SPCR.TXMD = 1).	R/W
b1	SPOE	Parity Mode	0: Even parity selected for transmission and reception 1: Odd parity selected for transmission and reception.	R/W
b2	SPIIE	SPI Idle Interrupt Enable	0: Idle interrupt requests disabled 1: Idle interrupt requests enabled.	R/W
b3	PTE	Parity Self-Testing	0: Self-diagnosis function of the parity circuit disabled 1: Self-diagnosis function of the parity circuit enabled.	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0: RSPCK auto-stop function disabled 1: RSPCK auto-stop function enabled.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the SPPE, SPOE, or SCKASE bit in SPCR2 is changed while the SPE bit in the SPCR register is 1, do not perform subsequent operations.

32.2.12 SPI下一次访问延迟寄存器(SPND)

Address(es): SPI0.SPND 4007 200Eh, SPI1.SPND 4007 210Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SPNDL[2:0]	SPI下一次访问延迟设置	b2 b0 0 0 0: 1 RSPCK + 2 PCLK 0 0 1: 2 RSPCK + 2 PCLK 0 1 0: 3 RSPCK + 2 PCLK 0 1 1: 4 RSPCK + 2 PCLK 1 0 0: 5 RSPCK + 2 PCLK 1 0 1: 6 RSPCK + 2 PCLK 1 1 0: 7 RSPCK + 2 PCLK 1 1 1: 8 RSPCK + 2 PCLK.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SPMDm.SPNDEN位为1时，SPND寄存器设置串行传输终止后SSLni信号的非活动周期（下一次访问延迟）。如果在SPCR.MSTR和SPCR.MSTR和SPCR.SPE位为1，不执行后续操作。

SPNDL[2:0]位（SPI下一次访问延迟设置）

当SPMDm.SPNDEN位为1时，SPNDL[2:0]位设置下一次访问延迟。在从机模式下使用SPI时，将SPNDL[2:0]位设置为000b。

32.2.13 SPI控制寄存器2(SPCR2)

Address(es): SPI0.SPCR2 4007 200Fh, SPI1.SPCR2 4007 210Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SPPE	奇偶校验使能	0：不检查发送数据的奇偶校验位和接收数据的奇偶校验位1：检查发送数据的奇偶校验位和接收数据的奇偶校验位（当SPCR.TXMD=0时）。奇偶校验位添加到发送数据但未检查接收数据的奇偶校验位（当SPCR.TXMD=1时）。	R/W
b1	SPOE	奇偶校验模式	0：发送和接收选择偶校验1：发送和接收选择奇校验。	R/W
b2	SPIIE	SPI空闲中断使能	0：禁止空闲中断请求1：允许空闲中断请求。	R/W
b3	PTE	Parity Self-Testing	0：奇偶电路自诊断功能无效1：奇偶电路自诊断功能有效。	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0：RSPCK自动停机功能无效1：RSPCK自动停机功能有效。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

如果SPCR2中的SPPE、SPOE或SCKASE位发生变化，而SPCR寄存器中的SPE位为1，则不要执行后续操作。

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data. When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data, but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is odd.

The SPOE bit is valid only when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an SPI idle state is detected and the SPSR.IDLNF flag is set to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables the self-diagnosis function of the parity circuit to check whether the parity function is operating correctly.

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs when data is received in master mode. For details, see section 32.3.8.1, Overrun errors.

32.2.14 SPI Command Registers (SPCMDm) (m =0 to 7 for SPI0; m = 0 for SPI1)

Address(es): SPI0.SPCMD0 4007 2010h, SPI0.SPCMD1 4007 2012h, SPI0.SPCMD2 4007 2014h, SPI0.SPCMD3 4007 2016h, SPI0.SPCMD4 4007 2018h, SPI0.SPCMD5 4007 201Ah, SPI0.SPCMD6 4007 201Ch, SPI0.SPCMD7 4007 201Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(SPI0)	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Address(es): SPI1.SPCMD0 4007 2110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(SPI1)	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				—	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge.	R/W
b1	CPOL	RSPCK Polarity Setting	0: Set RSPCK low when idle 1: Set RSPCK high when idle.	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8.	R/W

SPPE位（奇偶校验使能）

SPPE位启用或禁用奇偶校验功能。

当SPCR.TXMD位为0且该位为1时，发送数据添加奇偶校验位，接收数据执行奇偶校验。当SPCR.TXMD位为1且该位为1时，发送数据时添加奇偶校验位，但接收数据不进行奇偶校验。

SPOE位（奇偶校验模式）

SPOE位指定奇校验或偶校验。

当设置了偶校验时，执行奇偶校验位相加，以使发送或接收字符中值为1的总位数加上奇偶校验位为偶数。类似地，当设置奇校验时，执行校验位相加，使得发送或接收字符中值为1的位加上奇偶校验位的总数为奇数。

SPOE位仅在SPPE位为1时有效。

SPIIE位（SPI空闲中断使能）

当检测到SPI空闲状态并且
SPSR.IDLNF标志设置为0。

PTE位（奇偶自检）

PTE位启用奇偶校验电路的自诊断功能，以检查奇偶校验功能是否正常运行。

SCKASE位（RSPCK自动停止功能使能）

SCKASE位启用或禁用RSPCK自动停止功能。当此功能使能时，在主机模式下接收数据时，在发生溢出错误之前停止RSPCK时钟。有关详细信息，请参阅第32.3.8.1节，溢出错误。

32.2.14 SPI命令寄存器(SPCMDm)（对于SPI0，m=0到7；对于SPI1，m=0）

Address(es): SPI0.SPCMD0 4007 2010h, SPI0.SPCMD1 4007 2012h, SPI0.SPCMD2 4007 2014h, SPI0.SPCMD3 4007 2016h, SPI0.SPCMD4 4007 2018h, SPI0.SPCMD5 4007 201Ah, SPI0.SPCMD6 4007 201Ch, SPI0.SPCMD7 4007 201Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(SPI0)	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
重置后的值：	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Address(es): SPI1.SPCMD0 4007 2110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(SPI1)	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				—	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
重置后的值：	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	位名称	Description	R/W
b0	CPHA	RSPCK相位设置	0：选择前沿数据采样，后沿数据变化1：选择前沿数据变化，后沿数据采样。	R/W
b1	CPOL	RSPCK极性设置	0：空闲时将RSPCK设置为低1：空闲时将RSPCK设置为高。	R/W
b3, b2	BRDV[1:0]	比特率划分设置	b3b200：基本比特率01：基本比特率除以210：基本比特率除以411：基本比特率除以8。	R/W

Bit	Symbol	Bit name	Description	R/W
b6 to b4	SSLA[2:0] *1	SSL Signal Assertion Setting	b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: Setting prohibited x: Don't care.	R/W
b7	SSLKP	SSL Signal Level Keeping	• SPI0 0: Negates all SSL signals on completion of transfer 1: Keeps the SSL signal level from the end of transfer until the beginning of the next access.	R/W
	—	Reserved	• SPI1 This bit is read as 0. The write value should be 0.	R/W
b11 to b8	SPB[3:0]	SPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits.	R/W
b12	LSBF	SPI LSB-first	0: MSB-first 1: LSB-first.	R/W
b13	SPNDEN	SPI Next-Access Delay Enable	0: A next-access delay of 1 RSPCK + 2 PCLK 1: A next-access delay equal to the setting of the SPI Next-Access Delay register (SPND).	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: An SSL negation delay of 1 RSPCK 1: An SSL negation delay equal to the setting of the SPI Slave Select Negation Delay register (SSLND).	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay equal to the setting of the SPI Clock Delay register (SPCKD).	R/W

Note 1. This bit is not available in SPI1.

- SPI0

The SPCMDm register sets the transfer format for the SPI in master mode. SPI0 has eight SPI command registers, SPCMD0 to SPCMD7. Some of the bits in the SPCMD0 register are used to set a transfer mode for the SPI in slave mode. The SPI in master mode sequentially references the SPCMDm register based on the settings in the SPSCR.SPSLN[2:0] bits and executes the serial transfer that is set in the referenced SPCMDm register.
Set the SPCMDm register while the transmit buffer is empty (SPSR.SPTEF is 1 and data for the next transfer is not set), and before the setting of data to be transmitted when that SPCMDm register is referenced.
The SPCMDm register that the SPI in master mode references can be checked with the SPSSR.SPCP[2:0] bits. If the contents of SPCMDm are changed while the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1, do not perform subsequent operations.

- SPI1

SPI1 has one SPI Command Register (SPCMD). The SPI Command Register (SPCMD) sets the transfer format in master mode. Some of the bits in the SPCMD0 register are used to set the transfer mode for the SPI in slave mode. If the contents of the SPCMD register are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

CPHA bit (RSPCK Phase Setting)

The CPHA bit sets the RSPCK phase of the SPI in master mode or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

Bit	Symbol	位名称	Description	R/W
b6 to b4	SSLA[2:0] *1	SSL信号断言设置	b6b4000：SSL0001：S SL1010：SSL2011：SSL 31xx：设置禁止x：无关 。	R/W
b7	SSLKP	SSL信号电平保持	SPI00：在传输完成时否定所有SSL信号1：从传输结束到下一次访问开始时保持SSL信号电平。	R/W
	—	Reserved	SPI1该位读取为0。写入值应为0。	R/W
b11 to b8	SPB[3:0]	SPI数据长度设置	b11b80100到0111 ：8位1000：9位10 01：10位1010：11 位1011：12位1100 ：13位1101：14位 1110：15位1111： 16位0000：20位00 01：24位0010、00 11：32位。	R/W
b12	LSBF	SPI LSB-first	0: MSB-first 1: LSB-first.	R/W
b13	SPNDEN	SPI下一次访问延迟 Enable	0：1RSPCK+2PCLK的下一次访问延迟1：下一次访问延迟等于SPI下一次访问延迟寄存器(SPND)的设置。	R/W
b14	SLNDEN	SSL否定延迟设置 Enable	0：SSL否定延迟为1RSPCK1：SSL否定延迟等于SPI从器件选择否定延迟寄存器(SSLND)的设置。	R/W
b15	SCKDEN	RSPCK延迟设置启用	0：1RSPCK的RSPCK延迟1：RSPCK延迟等于SPI时钟延迟寄存器(SPCKD)的设置。	R/W

注1.该位在SPI1中不可用。

- SPI0

SPCMDm寄存器设置主模式下SPI的传输格式。SPI0有8个SPI命令寄存器，
SPCMD0到SPCMD7。SPCMD0寄存器中的一些位用于设置SPI在从机模式下的传输模式。主模式下的SPI根据SPSCR.SPSLN[2:0]位中的设置顺序引用SPCMDm寄存器，并执行在引用的SPCMDm寄存器中设置的串行传输。
在发送缓冲区为空时（SPSR.SPTEF为1且未设置下一次传输的数据）设置SPCMDm寄存器，并在参考该SPCMDm寄存器时设置要发送的数据之前。可以使用SPSSR.SPCP[2:0]位检查主模式下SPI引用的SPMDm寄存器。如果在SPCR.MSTR位为0且SPCR.SPE位为1时改变了SPCMDm的内容，则不要执行后续操作。

- SPI1

SPI1有一个SPI命令寄存器(SPCMD)。SPI命令寄存器(SPCMD)将传输格式设置为主机模式。SPCMD0寄存器中的一些位用于设置SPI在从机模式下的传输模式。如果SPCR.SPE位为1时SPCMD寄存器的内容发生变化，则不要执行后续操作。

CPHA位（RSPCK相位设置）

CPHA位将SPI的RSPCK相位设置为主机模式或从机模式。SPI模块之间的数据通信需要模块之间相同的RSPCK相位设置。

CPOL bit (RSPCK Polarity Setting)

The CPOL bit sets the RSPCK polarity of the SPI in master mode or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate. A bit rate is determined by combination of the settings in the BRDV[1:0] bits and the SPBR register. See section 32.2.8, SPI Bit Rate Register (SPBR). The SPBR settings determine the base bit rate. The BRDV[1:0] settings select a bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. In the SPCMDm register for SPI0, different BRDV[1:0] bit settings can be specified, enabling the execution of serial transfers at a different bit rate for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode.

When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state, as the SSLn0 pin acts as input.

When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP bit (SSL Signal Level Keeping)

When the SPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLni signal level for the current command is to be kept or negated between the SSL negation timing associated with the current command and the SSL assertion timing associated with the next command.

Setting the SSLKP bit to 1 enables a burst transfer. For details, see section 32.3.10.1, Master mode operation (4) Burst transfer. When using the SPI in slave mode, set the SSLKP bit to 0.

The SSLKP bit is reserved for SPI1.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits set a transfer data length for the SPI in master mode or slave mode.

When the SPLW bit is 0, set the SPI data length setting bits, SPCMDm.SPB[3:0], from 8 to 16 bits.

LSBF bit (SPI LSB-first)

The LSBF bit sets the data format of the SPI in master mode or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit sets the period from the time the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access (next-access delay). If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLK. If the SPNDEN bit is 1, the SPI inserts a next-access delay according to the SPND setting.

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit sets the period from the time the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal inactive (SSL negation delay). If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal at an SSL negation delay according to the SSLND setting.

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit sets the period from the point when the SPI in master mode activates the SSLni signal until the RSPCK starts oscillation (SPI clock delay). If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at an RSPCK delay according to the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

CPOL位（RSPCK极性设置）

CPOL位设置SPI在主模式或从模式下的RSPCK极性。SPI模块之间的数据通信要求模块之间的RSPCK极性设置相同。

BRDV[1:0]位（比特率划分设置）

BRDV[1:0]位决定比特率。比特率由BRDV[1:0]位和SPBR寄存器中的设置组合确定。请参见第32.2.8节，SPI比特率寄存器(SPBR)。SPBR设置决定了基本比特率。BRDV[1:0]设置选择通过将基本比特率除以1、2、4或8获得的比特率。在SPI0的SPCMDm寄存器中，可以指定不同的BRDV[1:0]位设置，启用每个命令以不同的比特率执行串行传输。

SSLA[2:0]位（SSL信号断言设置）

当SPI在主模式下执行串行传输时，SSLA[2:0]位控制SSLni信号断言。

当SSLni信号被置位时，其极性由相关SSLP中设置的值确定。当SSLA[2:0]位在多主机模式下设置为000b时，所有SSL信号都在否定状态下执行串行传输，因为SSLn0引脚用作输入。

在从机模式下使用SPI时，将SSLA[2:0]位设置为000b。

SSLKP位（SSL信号电平保持）

当主模式的SPI执行串行传输时，SSLKP位指定当前命令的SSLni信号电平是在与当前命令相关的SSL否定时序和与下一个命令相关的SSL断言时序之间保持还是否定.

将SSLKP位设置为1可启用突发传输。有关详细信息，请参阅第32.3.10.1节，主模式操作(4)突发传输。在从机模式下使用SPI时，将SSLKP位设置为0。

SSLKP位为SPI1保留。

SPB[3:0]位（SPI数据长度设置）

SPB[3:0]位设置SPI在主模式或从模式下的传输数据长度。

当SPLW位为0时，将SPI数据长度设置位SPCMDm.SPB[3:0]设置为8至16位。

LSBF位（SPILSB优先）

LSBF位将SPI在主模式或从模式下的数据格式设置为MSB优先或LSB优先。

SPNDEN位（SPI下一次访问延迟使能）

SPNDEN位设置从处于主模式的SPI终止串行传输并将SSLni信号设置为无效到SPI启用SSLni信号断言以进行下一次访问（下一次访问延迟）的时间段。如果SPNDEN位为0，则SPI将下一次访问延迟设置为1RSPCK+2PCLK。如果SPNDEN位为1，则SPI根据SPND设置插入下一次访问延迟。

在从机模式下使用SPI时，将SPNDEN位设置为0。

SLNDEN位（SSL否定延迟设置启用）

SLNDEN位设置从主模式SPI停止RSPCK振荡到SPI设置
SSLni信号无效（SSL否定延迟）。如果SLNDEN位为0，则SPI将SSL否定延迟设置为1RSPCK。如果SLNDEN位为1，则SPI根据SSLND设置以SSL否定延迟否定SSL信号。

在从机模式下使用SPI时，将SLNDEN位设置为0。

SCKDEN位（RSPCK延迟设置使能）

SCKDEN位设置从主模式下的SPI激活SSLni信号到RSPCK开始振荡（SPI时钟延迟）的周期。如果SCKDEN位为0，则SPI将RSPCK延迟设置为1RSPCK。如果SCKDEN位为1，则SPI根据SPCKD设置以RSPCK延迟启动RSPCK的振荡。

在从机模式下使用SPI时，将SCKDEN位设置为0。

32.3 Operation

In this section, the serial transfer period means a period from the beginning of driving valid data to the fetching of the final valid data.

32.3.1 Overview of SPI Operations

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single-master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation).

The SPI mode can be selected with the MSTR, MODFEN, and SPMS bits in SPCR. Table 32.5 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 32.5 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLK/6	Up to PCLK/2	Up to PCLK/2	Up to PCLK/6	Up to PCLK/2
Clock source	RSPCKn input	On-chip baud rate generator	On-chip baud rate generator	RSPCKn input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Supported in SPI0	Supported in SPI0	Supported in SPI0	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmit buffer is written to on generation of a transmit buffer empty interrupt request (SPTEF is 1)	Transmit buffer is written to on generation of a transmit buffer empty interrupt request (SPTEF is 1)	RSPCK oscillation	Transmit buffer is written to on generation of a transmit buffer empty interrupt request (SPTEF is 1)
Sequence control	Not supported	Supported in SPI0	Supported in SPI0	Not supported	Supported in SPI0
Transmit buffer empty detection	Supported				

32.3 Operation

在本节中，串行传输周期是指从驱动有效数据开始到获取最终有效数据的周期。

32.3.1 SPI操作概述

SPI能够在以下模式下进行同步串行传输：

- 从机模式（SPI操作）
- Single-master mode (SPI operation)
- Multi-master mode (SPI operation)
- 从机模式（时钟同步操作）
- 主模式（时钟同步操作）。

SPI模式可以通过SPCR中的MSTR、MODFEN和SPMS位进行选择。表32.5列出了SPI模式和SPCR设置之间的关系，以及每种模式的说明。

Table 32.5 SPCR设置和SPI模式之间的关系(1of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
MSTR位设置	0	1	1	0	1
MODFEN位设置	0 or 1	0	1	0	0
SPMS位设置	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1到SSLn3信号	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL极性改变功能	Supported	Supported	Supported	—	—
传输率	高达PCLK6	高达PCLK2	高达PCLK2	高达PCLK6	高达PCLK2
时钟源	RSPCKn input	片上波特率发生器	片上波特率发生器	RSPCKn input	片上波特率发生器
时钟极性	Two				
时钟相位	Two	Two	Two	One (CPHA = 1)	Two
第一个传输位	MSB/LSB				
传输数据长度	8至16、20、24、32位				
突发传输	支持在SPI0	在SPI0中支持	在SPI0中支持	—	—
RSPCK延迟控制	不支持	Supported	Supported	不支持	Supported
SSL否定延迟控制	不支持	Supported	Supported	不支持	Supported
下一次访问延迟控制	不支持	Supported	Supported	不支持	Supported
转账激活方式	SSL输入有效或RSPCK振荡	在产生发送缓冲区空中断请求时写入发送缓冲区（SPTEF为1）	在产生发送缓冲区空中断请求时写入发送缓冲区（SPTEF为1）	RSPCK oscillation	在产生发送缓冲区空中断请求时写入发送缓冲区（SPTEF为1）
顺序控制	不支持	在SPI0中支持	在SPI0中支持	不支持	在SPI0中支持
发送缓冲区空检测	Supported				

Table 32.5 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
Parity error detection	Supported*2,*3				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported
Underrun error detection	Supported	Not supported	Not supported	Supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, detection of receiver buffer full, overrun error, and parity error are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.

32.3.2 Controlling the SPI Pins

The SPI can switch pin states based on the MSTR, MODFEN, and SPMS bit settings in the SPCR register and the PmnPFS.NCODR bit for I/O ports. Table 32.6 lists the relationship between pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects CMOS output, setting it to 1 selects open-drain output. The I/O port settings must follow this relationship.

Table 32.6 Relationship between pin states and bit settings

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (Clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (Clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in the multiplex pins for which the SPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z.

Table 32.5 SPCR设置和SPI模式之间的关系(2of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
接收缓冲区满检测	Supported*2				
溢出错误检测	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
奇偶校验错误检测	Supported*2,*3				
模式故障错误检测	Supported (MODFEN = 1)	不支持	Supported	不支持	不支持
欠载错误检测	Supported	不支持	不支持	Supported	不支持

Note 1. 此模式不支持此功能。
Note 2. 当SPCR.TXMD位为1时，不执行接收缓冲区满、溢出错误和奇偶校验错误的检测。
Note 3. 当SPCR2.SPPE位为0时，不执行奇偶校验错误检测。
Note 4. 当SPCR2.SCKASE位为1时，不进行溢出错误检测。

32.3.2 控制SPI引脚

SPI可以根据SPCR寄存器中的MSTR、MODFEN和SPMS位设置以及IO端口的PmnPFS.NCODR位来切换引脚状态。表32.6列出了引脚状态和位设置之间的关系。设置
IO端口的PmnPFS.NCODR位为0选择CMOS输出，设置为1选择开漏输出。IO端口设置必须遵循这种关系。

Table 32.6 引脚状态和位设置之间的关系

Mode	Pin	Pin state*2	
		IO端口的PmnPFS.NCODR位=0	IO端口的PmnPFS.NCODR位=1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
从机模式（SPI操作）（MSTR=0，SPMS=0）	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
主模式（时钟同步操作）（MSTR=1，MODFEN=0，SPMS=1）	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
从机模式（时钟同步操作）（MSTR=0，SPMS=1）	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. 此模式不支持此功能。
Note 2. SPI设置不会反映在未选择SPI功能的多路复用管脚中。
Note 3. 当SSLn0处于有效电平时，引脚状态为Hi-Z。

Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master or multi-master mode (SPI operation) determines MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer for SPI0) based on the MOIFE and MOIFV bit settings in SPPCR, as listed in Table 32.7.

Table 32.7 MOSI signal value determination during SSL negation period

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation period
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

32.3.3 SPI System Configuration Examples

32.3.3.1 Single master and single slave with the MCU configured as a master

Figure 32.8 shows a single-master and single-slave SPI system configuration example where the MCU is the master. In the single-master and single-slave configuration, the SSLn0 to SSLn3 outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave stays selected.*1

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signals.

Note 1. In the transfer format used when the SPCMDm.CPHA is 0, the SSL signal for some slave devices cannot be fixed to an active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

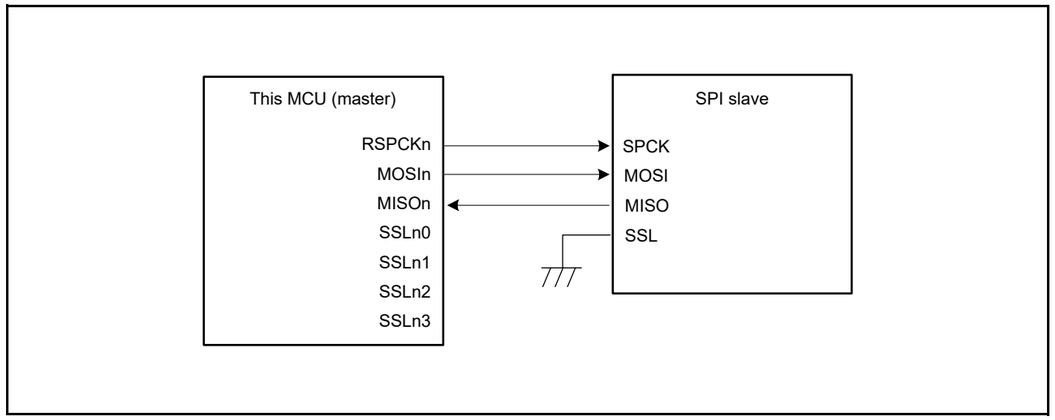


Figure 32.8 Single-master and single-slave configuration example with the MCU as the master

32.3.3.2 Single master and single slave with the MCU configured as a slave

Figure 32.9 shows a single-master and single-slave SPI system configuration example where the MCU is a slave. When the MCU operates as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the SPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

In the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level, and the MCU (slave) stays selected. This enables serial transfer (Figure 32.10).

Note 1. When SSLn0 is at a non-active level, the pin state is Hi-Z.

Note 4. 当SSLn0处于非活动电平或SPCR.SPE位为0时，引脚状态为Hi-Z。
Note 5. 这些引脚可用作IO端口引脚。

单主机或多主机模式（SPI操作）下的SPI根据SPPCR中的MOIFE和MOIFV位设置确定SSL否定期间（包括SPI0突发传输期间的SSL保留期间）的MOSI信号值，如下所示在表32.7中。

Table 32.7 SSL否定期间的MOSI信号值确定

MOIFE bit	MOIFV bit	SSL否定期间的MOSIn信号值
0	0, 1	上次传输的最终数据
1	0	Low
1	1	High

32.3.3 SPI系统配置示例

32.3.3.1 单主单从，MCU配置为主

图32.8显示了单主单从SPI系统配置示例，其中MCU为主。在单主单从配置中，不使用MCU（主）的SSLn0到SSLn3输出。SPI从机的SSL输入固定为低电平，SPI从机保持选中状态。*1

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

注1.在SPCMDm.CPHA为0时使用的传输格式中，某些从设备的SSL信号不能固定为有效电平。在这种情况下，请始终将MCU的SSLni输出连接到从设备的SSL输入。

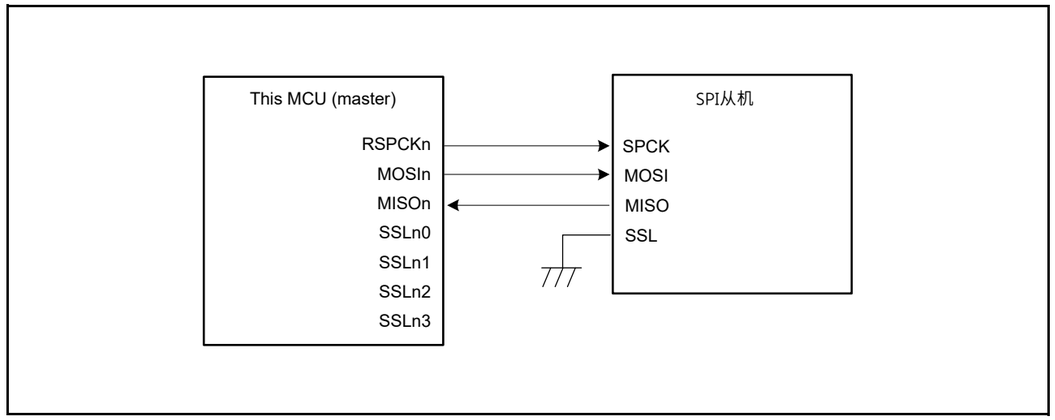


Figure 32.8 MCU为主的单主单从配置示例

32.3.3.2 单主单从机，MCU配置为从机

图32.9显示了单主单从SPI系统配置示例，其中MCU是从设备。当MCU作为从机运行时，SSLn0引脚用作SSL输入。SPI主机驱动SPCK和MOSI信号。MCU（从机）驱动MIOn信号。*1

在SPCMDm.CPHA位设置为1的单从配置中，MCU（从）的SSLn0输入固定为低电平，MCU（从）保持选择状态。这将启用串行传输（图32.10）。

注1.当SSLn0处于非活动电平时，引脚状态为Hi-Z。

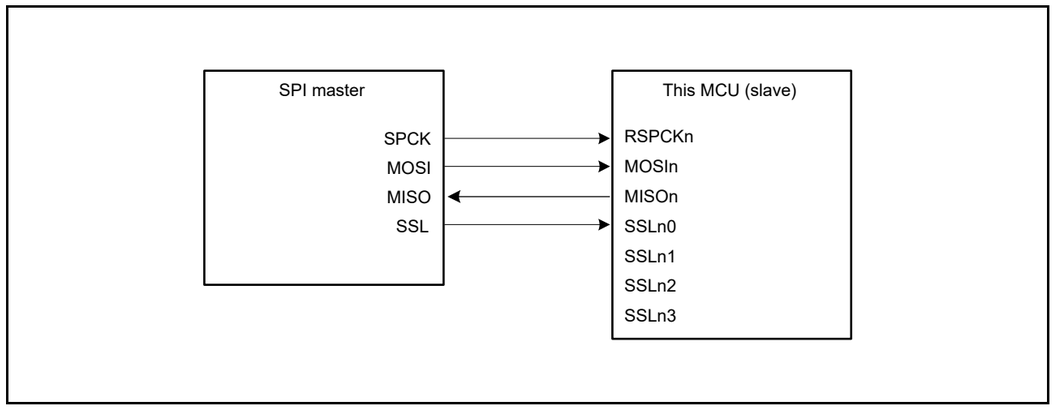


Figure 32.9 Single-master and single-slave configuration example with the MCU as a slave and CPHA = 0

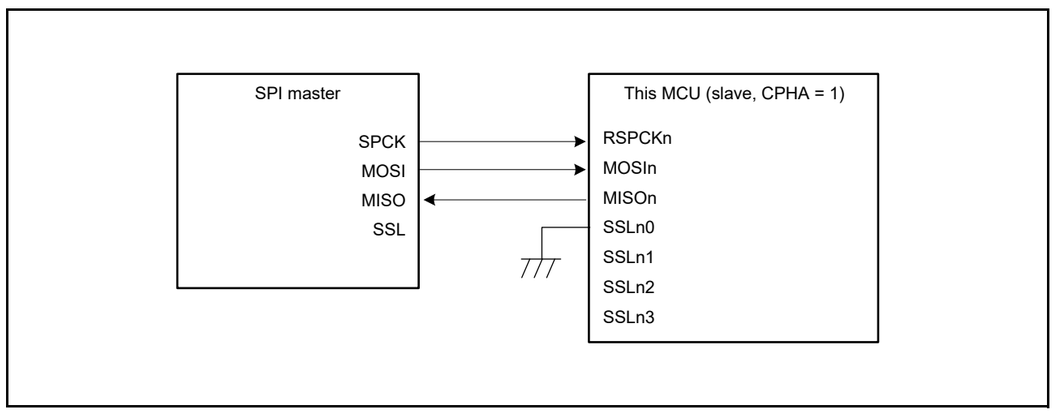


Figure 32.10 Single-master and single-slave configuration example with the MCU as a slave and CPHA = 1

32.3.3.3 Single-master and multi-slave with the MCU configured as a master

Figure 32.11 shows a single-master and multi-slave SPI system configuration example where the MCU is a master. In the example shown in Figure 32.11, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the SPCK and MOSI inputs of SPI slave 0 to SPI slave 3. The MISO outputs of SPI slave 0 to SPI slave 3 are all connected to the MISOn input of the MCU (master). SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slave 0 to SPI slave 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn signals, and SSLn0 to SSLn3 pins. Of the SPI slave 0 to SPI slave 3, the slave that receives low-level input into the SSL input drives the MISO signal.

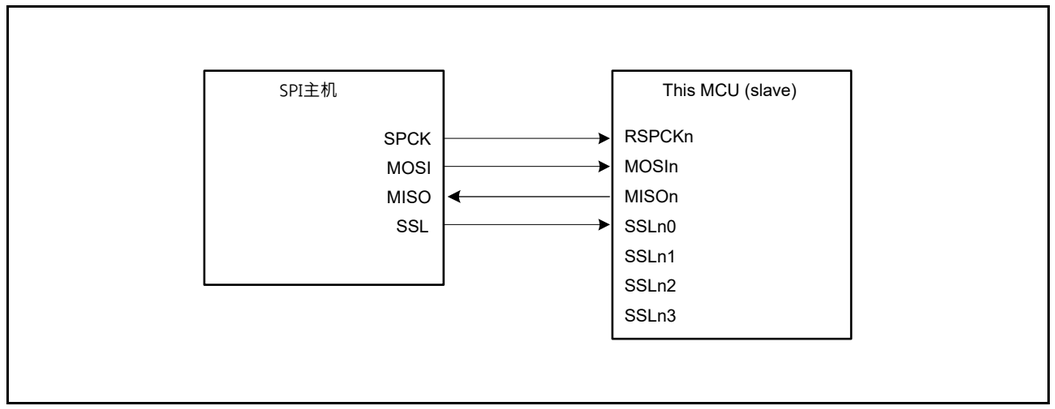


Figure 32.9 MCU作为从机且CPHA=0的单主单从配置示例

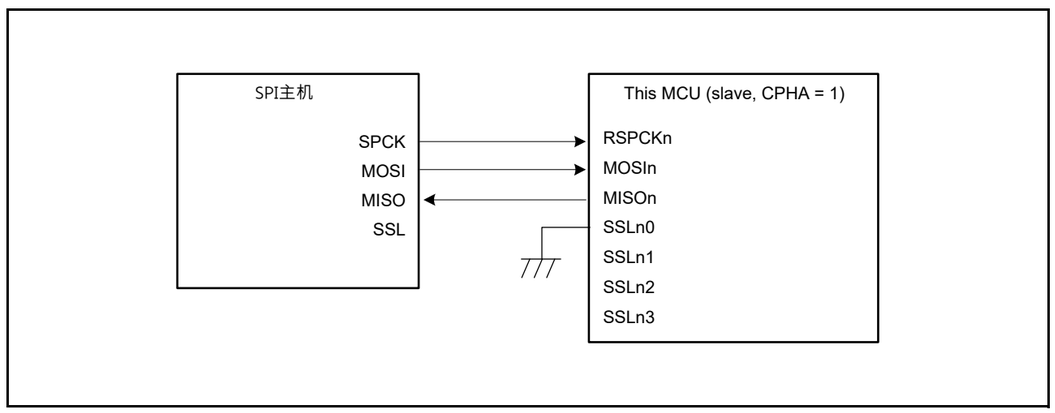


Figure 32.10 MCU作为从机且CPHA=1的单主单从配置示例

32.3.3.3 单主多从，MCU配置为主

图32.11显示了单主和多从SPI系统配置示例，其中MCU为主。在图32.11所示的示例中，SPI系统包括MCU（主机）和四个从机（SPI从机0到SPI从机3）。

MCU（主机）的RSPCKn和MOSIn输出连接到SPI从机0的SPCK和MOSI输入以SPI从机3。SPI从机0到SPI从机3的MISO输出都连接到MCU（主机）的MIOn输入。MCU（主机）的SSLn0到SSLn3输出分别连接到SPI从机0到SPI从机3的SSL输入。

MCU（主控）驱动RSPCKn、MOSIn信号和SSLn0至SSLn3引脚。在SPI从机0到SPI从机3中，接收到SSL输入的低电平输入的从机驱动MISO信号。

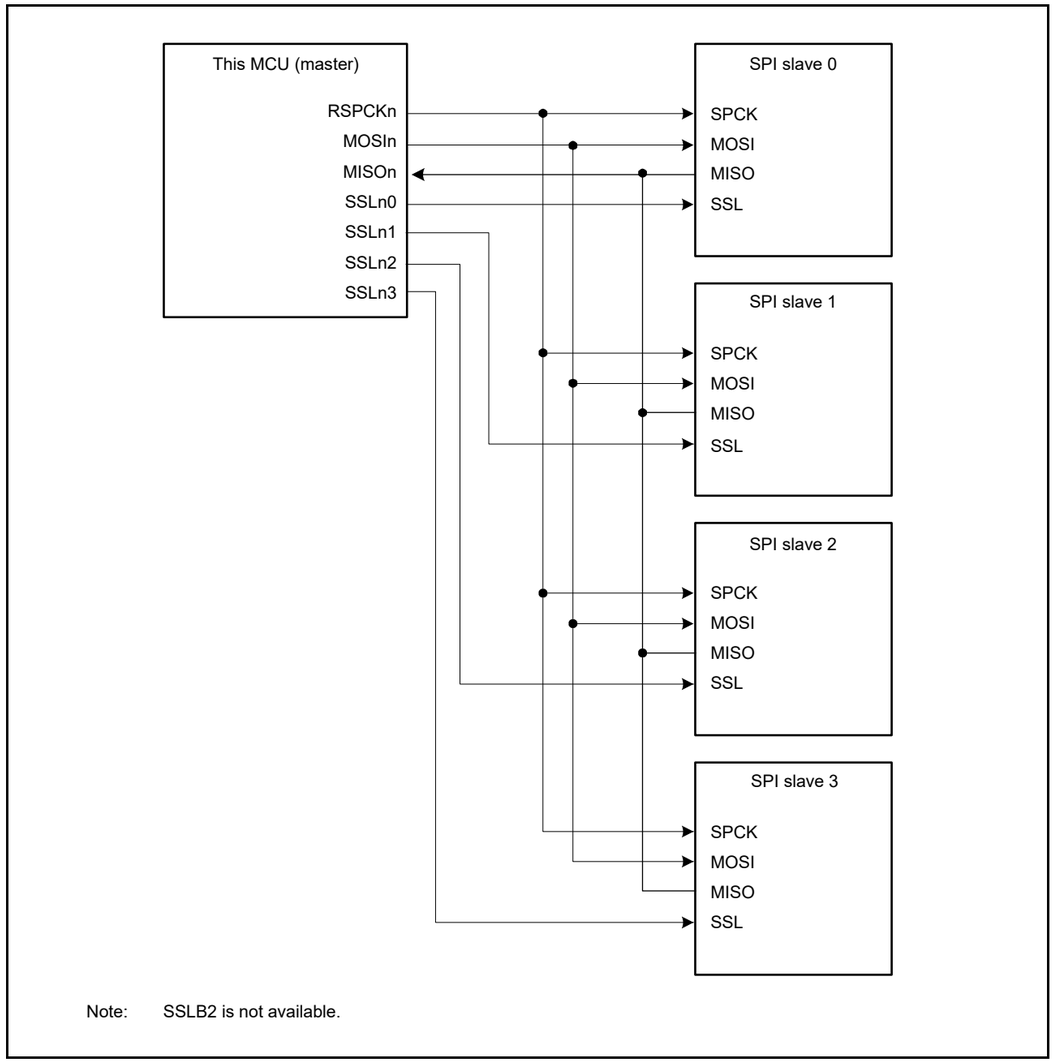


Figure 32.11 Single-master and multi-slave configuration example with the MCU as a master

32.3.3.4 Single master and multi-slave with the MCU configured as a slave

Figure 32.12 shows a single-master and multi-slave SPI system configuration example where the MCU is a slave. In the example shown in Figure 32.12, the SPI system includes an SPI master and two MCUs (slave X and slave Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slave X and slave Y). The MISOn outputs of the MCUs (slave X and slave Y) are all connected to the MISO input of the SPI master. SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slave X and slave Y), respectively.

The SPI master drives SPCK, MOSI, SSLX, and SSLY. The MCU slave (X or Y) that receives low-level input into the SSLn0 input drives the MISOn signal.

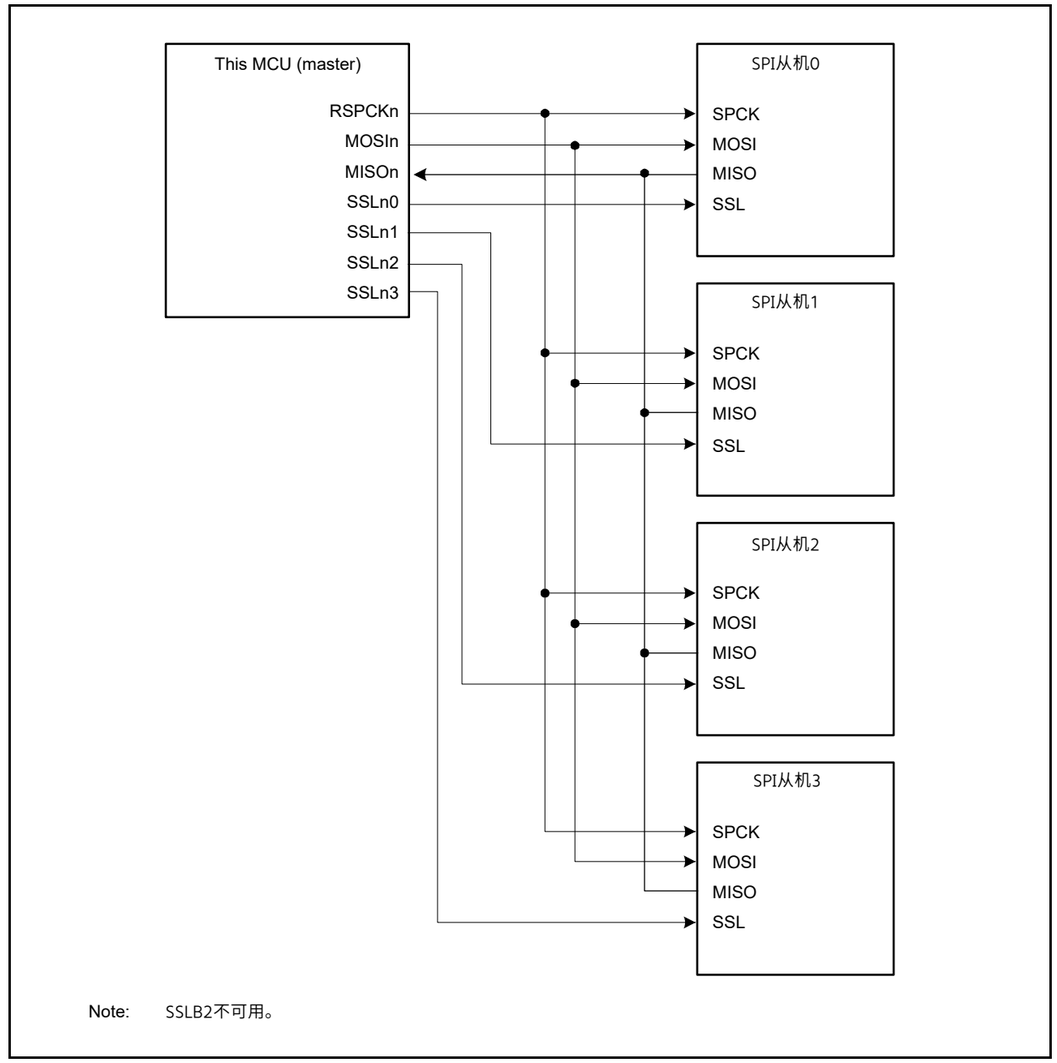


Figure 32.11 MCU为主的单主多从配置示例

32.3.3.4 单主多从，MCU配置为从机

图32.12显示了单主多从SPI系统配置示例，其中MCU是从设备。在图32.12所示的示例中，SPI系统包括一个SPI主机和两个MCU（从机X和从机Y）。

SPI主机的SPCK和MOSI输出连接到MCU（从机X和从机Y）的RSPCKn和MOSIn输入。MCU（从X和从Y）的MISOn输出都连接到SPI主控的MISO输入。SPI主机的SSLX和SSLY输出分别连接到MCU（从机X和从机Y）的SSLn0输入。

SPI主机驱动SPCK、MOSI、SSLX和SSLY。MCU从机（X或Y）接收低电平输入到SSLn0输入驱动MIOn信号。

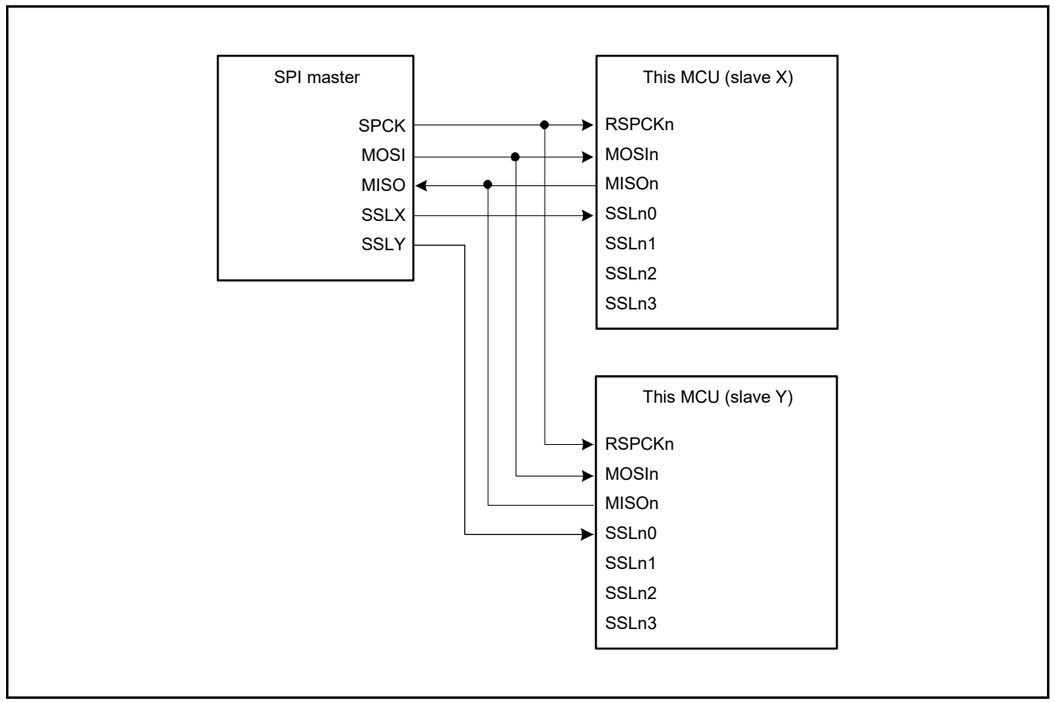


Figure 32.12 Single-master and multi-slave configuration example with the MCU as a slave

32.3.3.5 Multi-master and multi-slave with the MCU configured as a master

Figure 32.13 shows a multi-master and multi-slave SPI system configuration example where the MCU is a master. In the example shown in Figure 32.13, the SPI system includes two MCUs (master X and master Y) and two SPI slaves (SPI slave 1 and SPI slave 2).

The RSPCKn and MOSIn outputs of the MCUs (master X and master Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (master X and master Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (master X and master Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives RSPCKn, MOSIn, SSLn1, and SSLn2 when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

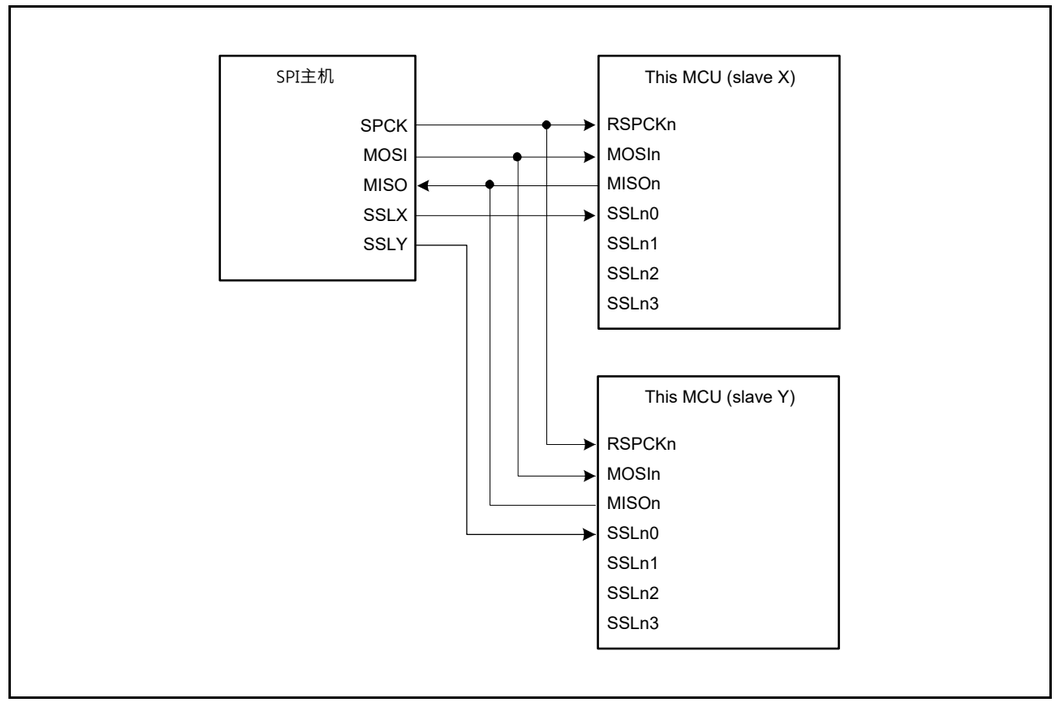


Figure 32.12 MCU作为从机的单主多从配置示例

32.3.3.5 MCU配置为主的多主多从

图32.13显示了一个多主多从SPI系统配置示例，其中MCU为主。在图32.13所示的示例中，SPI系统包括两个MCU（主X和主Y）和两个SPI从机（SPI从机1和SPI从机2）。

MCU（主X和主Y）的RSPCKn和MOSIn输出连接到SPI从设备1和2的RSPCK和MOSI输入。SPI从设备1和2的MISO输出连接到MCU（主设备）的MISOn输入X和主Y）。来自MCU（主X）的任何通用端口Y输出都连接到MCU（主Y）的SSLn0输入。MCU（主设备Y）的任何通用端口X输出都连接到MCU（主设备X）的SSLn0输入。MCU（主机X和主机Y）的SSLn1和SSLn2输出连接到SPI从机1和2的SSL输入。在此配置示例中，因为系统可以仅由SSLn0输入和SSLn1和SSLn2输出组成对于从连接，不需要MCU的SSLn3输出。

当SSLn0输入电平为高时，MCU驱动RSPCKn、MOSIn、SSLn1和SSLn2。当SSLn0输入电平为低时，MCU检测到模式故障错误，将RSPCKn、MOSIn、SSLn1和SSLn2设置为Hi-Z，并将SPI总线直接释放到另一个主控。在SPI从机1和2中，接收到SSL输入的低电平输入的从机驱动MISO信号。

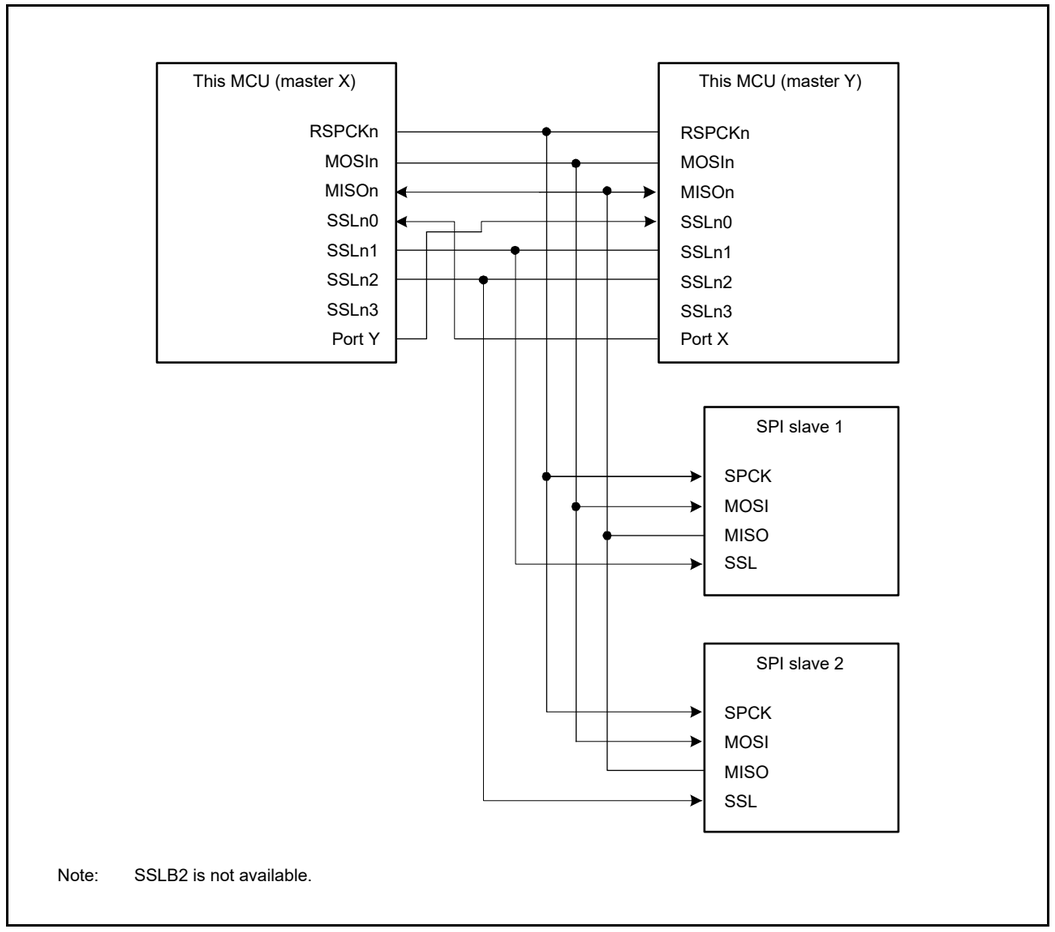


Figure 32.13 Multi-master and multi-slave configuration example with the MCU as a master

32.3.3.6 Master and slave in clock synchronous mode with the MCU configured as a master

Figure 32.14 shows a master and slave clock synchronous mode configuration where the MCU is a master. In the master and slave clock synchronous mode configuration, SSLn0 to SSLn3 of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

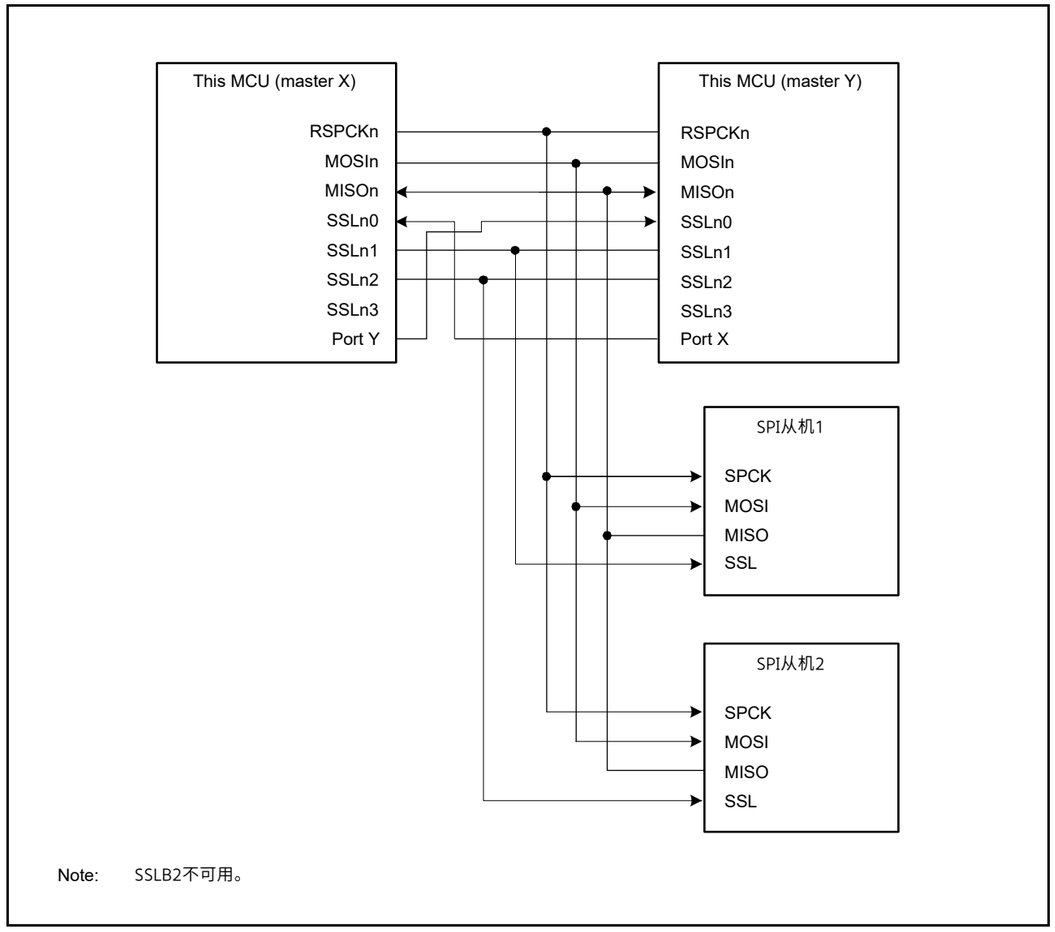


Figure 32.13 MCU为主的多主多从配置示例

32.3.3.6 主从时钟同步模式，MCU配置为主

图32.14显示了MCU为主的主从时钟同步模式配置。在主从时钟同步模式配置中，MCU（主）的SSLn0到SSLn3不使用。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

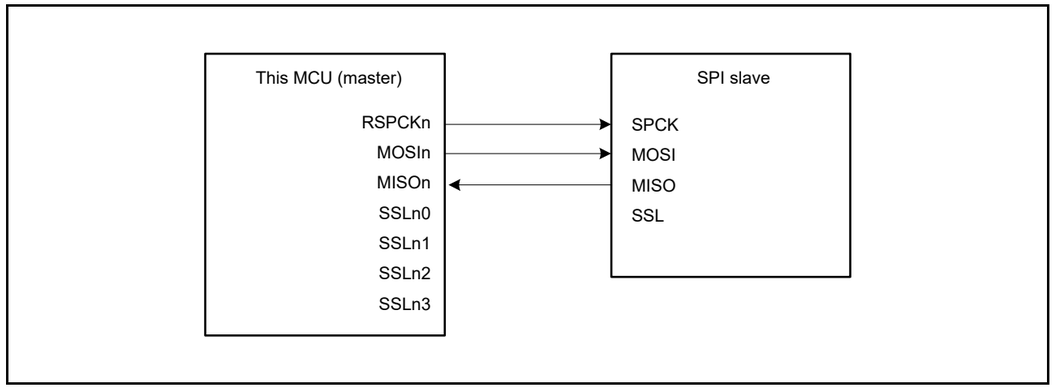


Figure 32.14 Configuration example of master and slave in clock synchronous mode with the MCU as a master

32.3.3.7 Master and slave in clock synchronous mode with the MCU configured as a slave

Figure 32.15 shows a master and slave in clock synchronous mode configuration example where the MCU is a slave. When the MCU is to operate as a slave in clock synchronous operation, the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. The SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfer in the single-slave configuration when the SPCMDm.CPHA is set to 1.

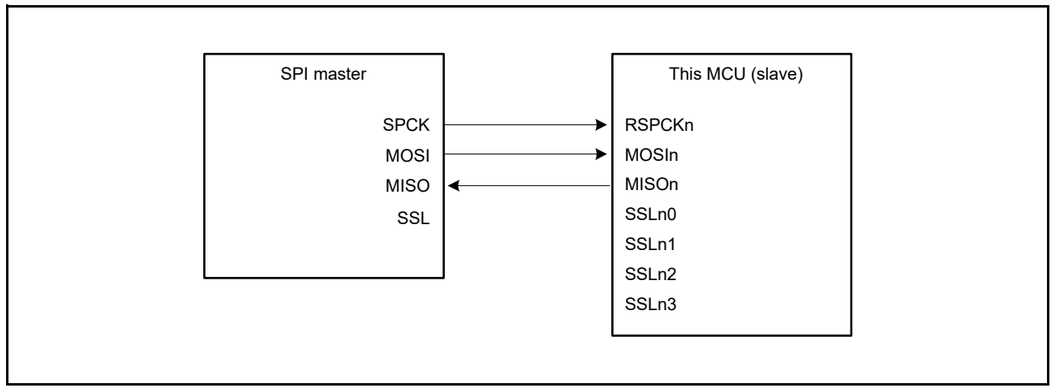


Figure 32.15 Configuration example of master and slave in clock synchronous mode with the MCU as a slave and CPHA = 1

32.3.4 Data Format

The data format of the SPI depends on the settings in the SPI Command Register m (SPCMDm) (m = 0 to 7) and the parity enable bit, SPPE, in the SPI Control Register 2 (SPCR2). Regardless of whether the ordering is MSB- or LSB-first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit associated with the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

(a) Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the bit-length selected in the SPI data length setting bits in the SPI Command Register m (SPCMDm.SPB[3:0] for SPI0, SPCMD0.SPB[3:0] for SPI1).

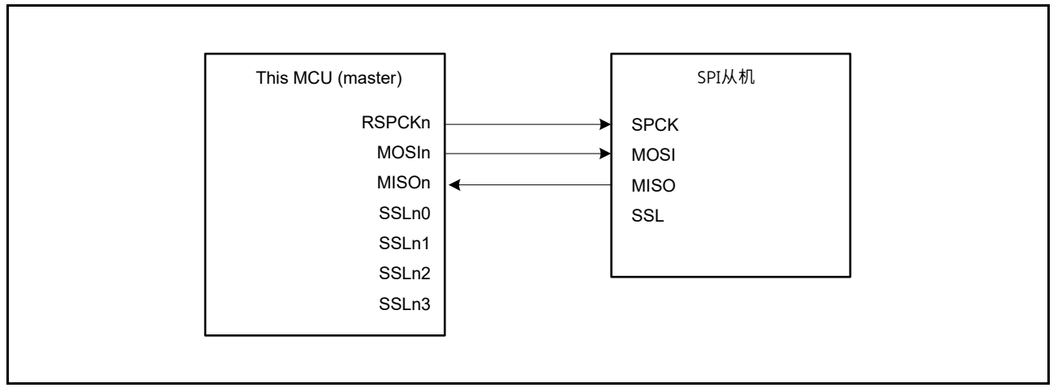


Figure 32.14 MCU作为主控时钟同步模式主从配置示例

32.3.3.7 主从时钟同步模式，MCU配置为从机

图32.15显示了时钟同步模式下的主从配置示例，其中MCU是从设备。
当MCU在时钟同步操作中作为从机运行时，MCU（从机）驱动MISOn信号，SPI主机驱动SPCK和MOSI信号。不使用MCU（从机）的SSLn0到SSLn3。

当SPCMDm.CPHA设置为1时，MCU（从机）只能在单从机配置中执行串行传输。

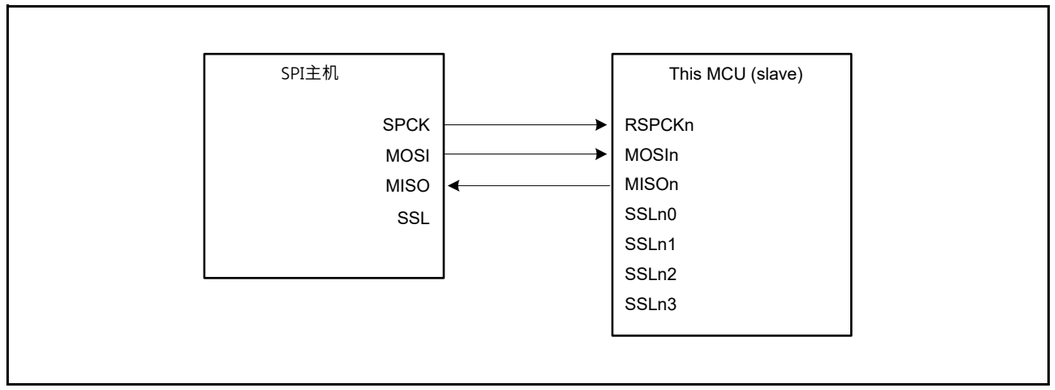


Figure 32.15 单片机作为从机，CPHA=1，时钟同步模式的主从配置示例

32.3.4 数据格式

SPI的数据格式取决于SPI命令寄存器m(SPCMDm)(m=0到7)中的设置以及SPI控制寄存器2(SPCR2)中的奇偶校验使能位SPPE。无论排序是MSB优先还是LSB优先，SPI都会将SPI数据寄存器(SPDRSPDR_HA)中的LSB位到与所选数据长度相关的位的范围视为传输数据。

本节显示传输前后一帧数据的格式。

(a) 禁用奇偶校验的数据格式

当奇偶校验被禁用时，数据的发送或接收将按照SPI命令寄存器m中的SPI数据长度设置位中选择的位长度进行（SPI0的SPCMDm.SPB[3:0]，SPCMD0.SPB[3:0]）对于SPI1)。

(b) Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the bit-length selected in the SPI data length setting bits in SPI Command Register m (SPCMDm.SPB[3:0] for SPI0, SPCMD0.SPB[3:0] for SPI1). In this case, however, the last bit is a parity bit.

- SPI0

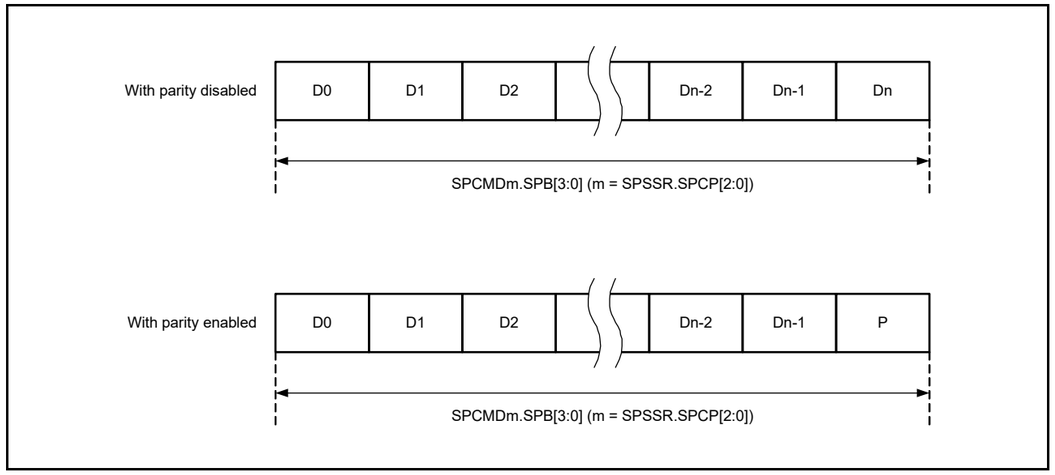


Figure 32.16 Data format with parity disabled and enabled (SPI0)

- SPI1

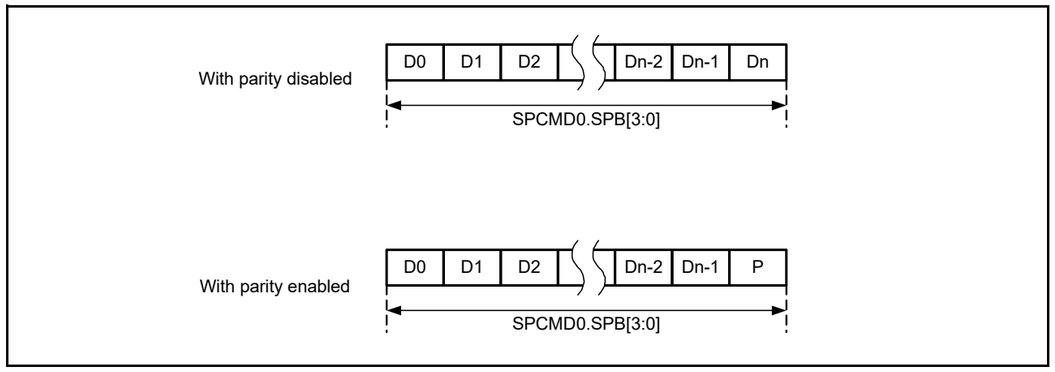


Figure 32.17 Data format with parity disabled and enabled (SPI1)

32.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no prior processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 32.18 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00.

(b) 启用奇偶校验的数据格式

当奇偶校验使能时，数据的发送或接收将按照SPI命令寄存器m的SPI数据长度设置位中选择的位长度进行（SPI0为SPCMDm.SPB[3:0]，SPI0为SPCMD0.SPB[3:0]SPI1)。然而，在这种情况下，最后一位是奇偶校验位。

- SPI0

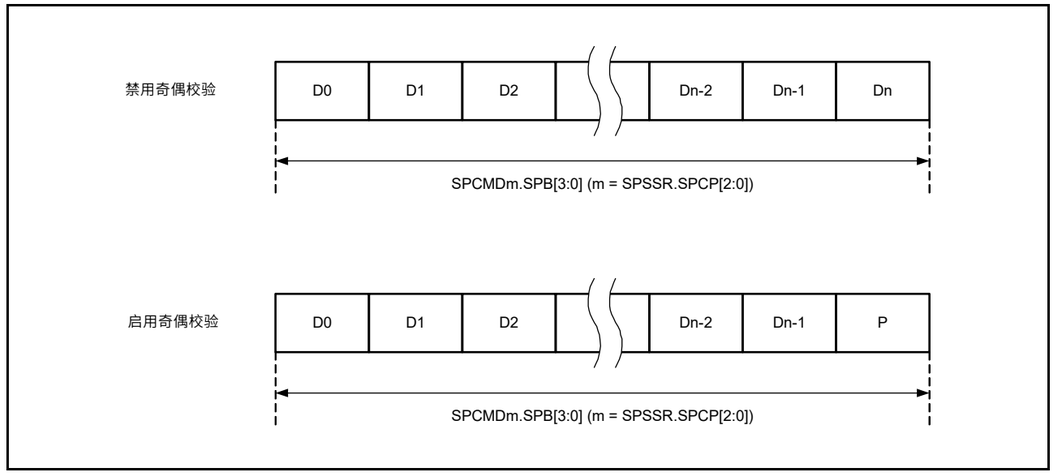


Figure 32.16 禁用和启用奇偶校验的数据格式(SPI0)

- SPI1

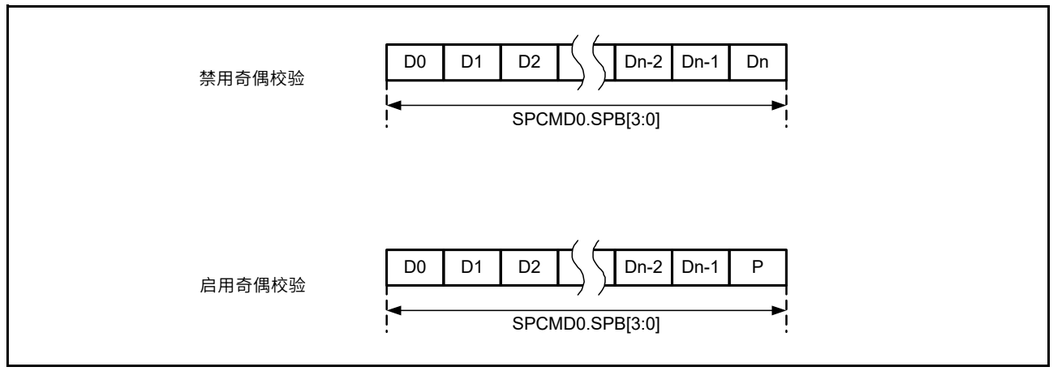


Figure 32.17 禁用和启用奇偶校验的数据格式(SPI1)

32.3.4.1 禁用奇偶校验时的操作(SPCR2.SPPE=0)

当奇偶校验被禁用时，用于传输的数据被复制到移位寄存器而无需事先处理。本节从MSB或LSB-firstorder和数据长度的组合来描述SPI数据寄存器(SPDRSPDR_HA)和移位寄存器之间的连接。

(1) 32位数据的MSB优先传输

图32.18显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用、SPI数据长度为32位且选择MSB优先的传输中的操作。

在发送过程中，发送缓冲器当前级的T31到T00位被复制到移位寄存器。发送数据从移位寄存器从T31移出到T30，并继续到T00。

In reception, received data is shifted in bit by bit through bit 0 of the shift register. When the R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

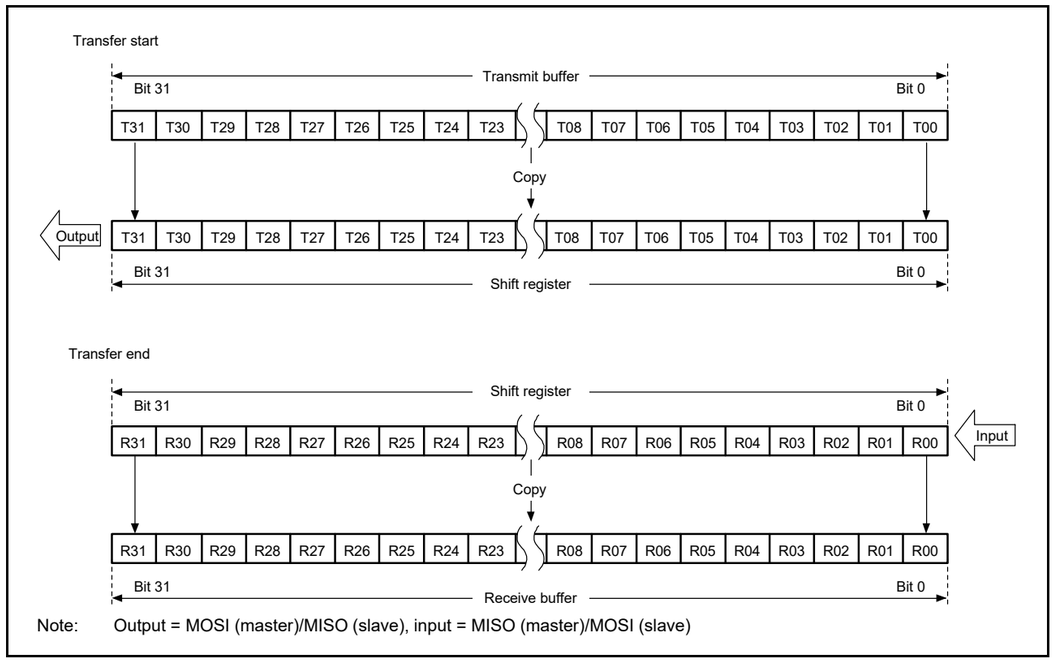


Figure 32.18 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 32.19 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00.

In reception, received data is shifted in bit by bit through bit [0] of the shift register. When bits R23 to R00 are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the transmission results in 0 being inserted in the upper 8 bits of the receive buffer.

接收时，接收到的数据通过移位寄存器的第0位逐位移位。在输入所需的RSPCK周期数后收集R31至R00位时，将移位寄存器中的值复制到接收缓冲区。

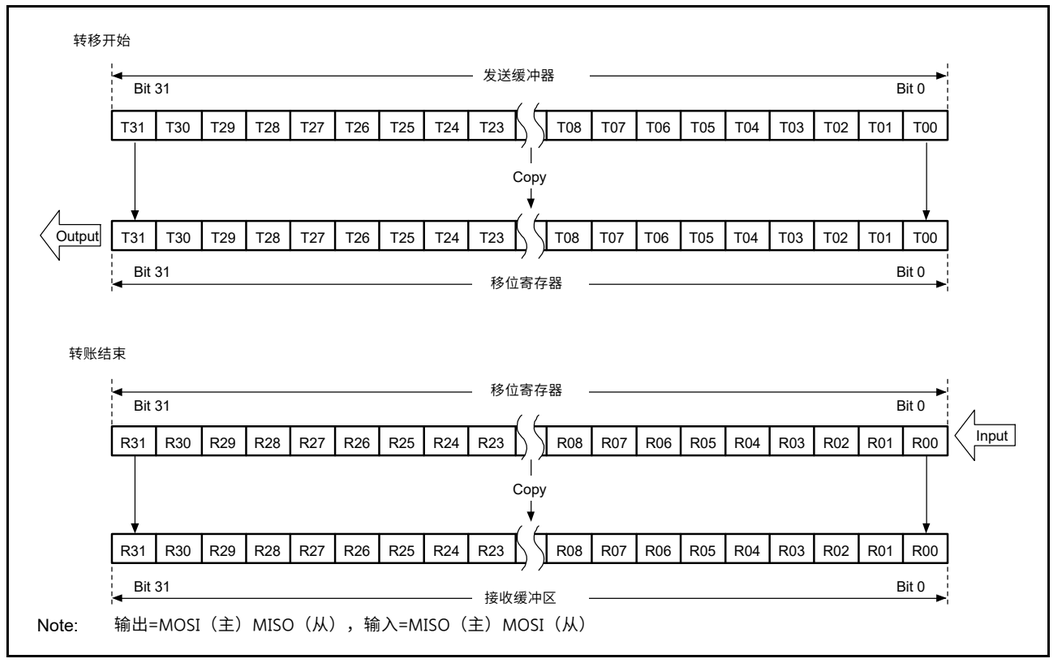


Figure 32.18 禁用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图32.19显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用、SPI数据长度为24位（以非32位为例）和MSB优先选择的传输中的操作。

在发送过程中，来自发送缓冲器当前阶段的低24位（T23到T00）被复制到移位寄存器。发送的数据从移位寄存器从T23移出到T22，并继续到T00。

在接收中，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需的RSPCK周期数后收集位R23到R00时，移位寄存器中的值被复制到接收缓冲区。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送时将0写入位T31至T24会导致将0插入接收缓冲区的高8位。

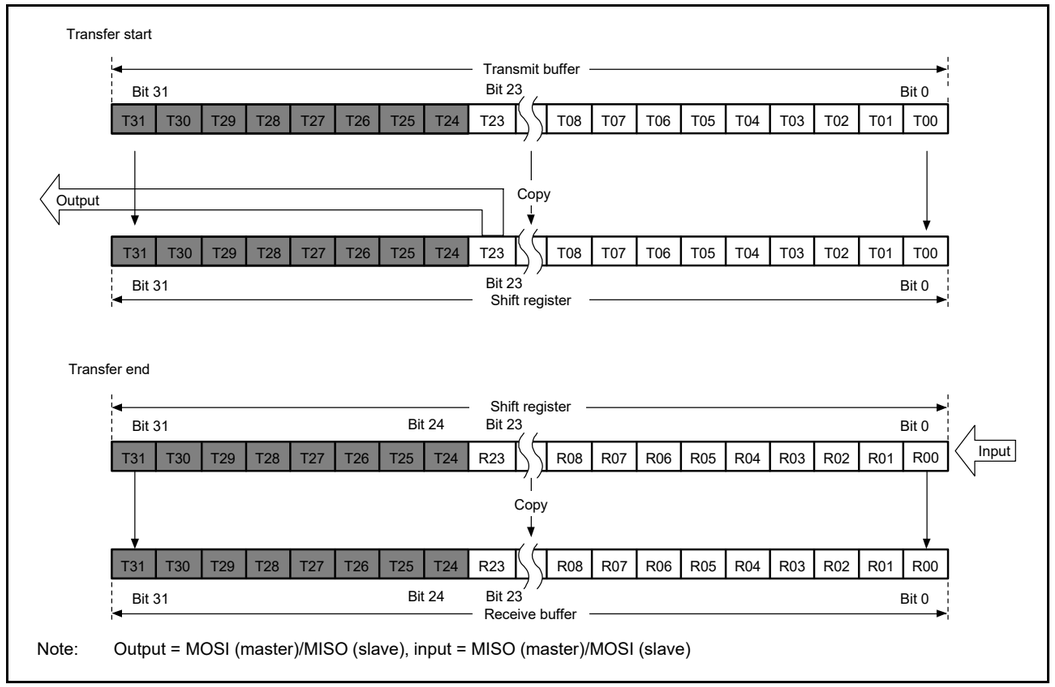


Figure 32.19 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 32.20 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T31.

In reception, received data is shifted in bit by bit through bit [0] of the shift register. When bits R00 to R31 are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

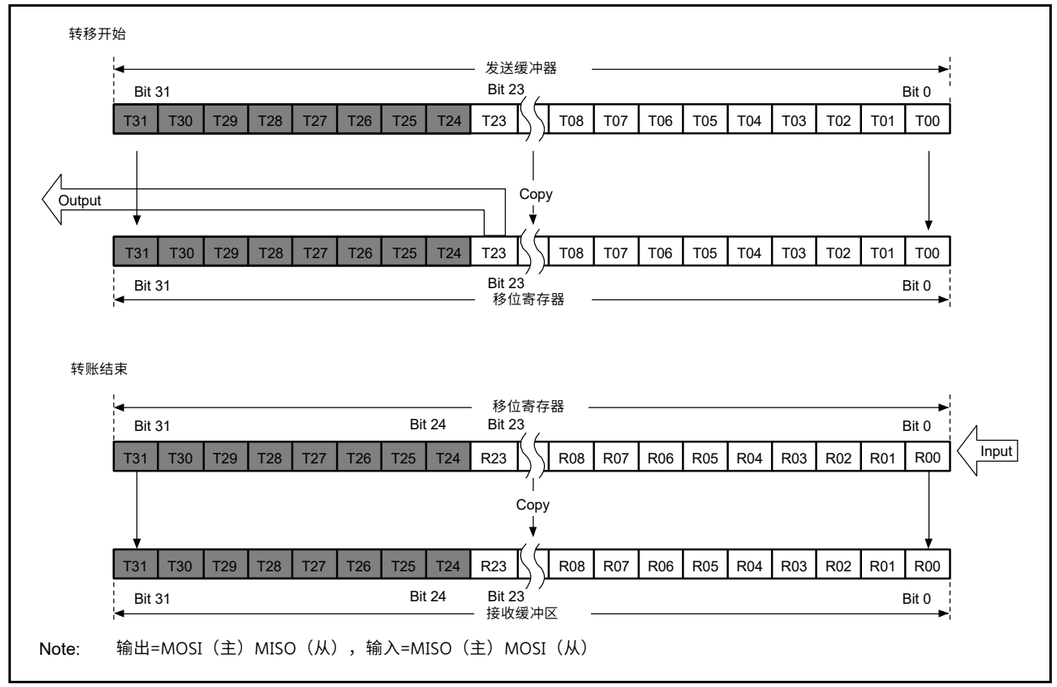


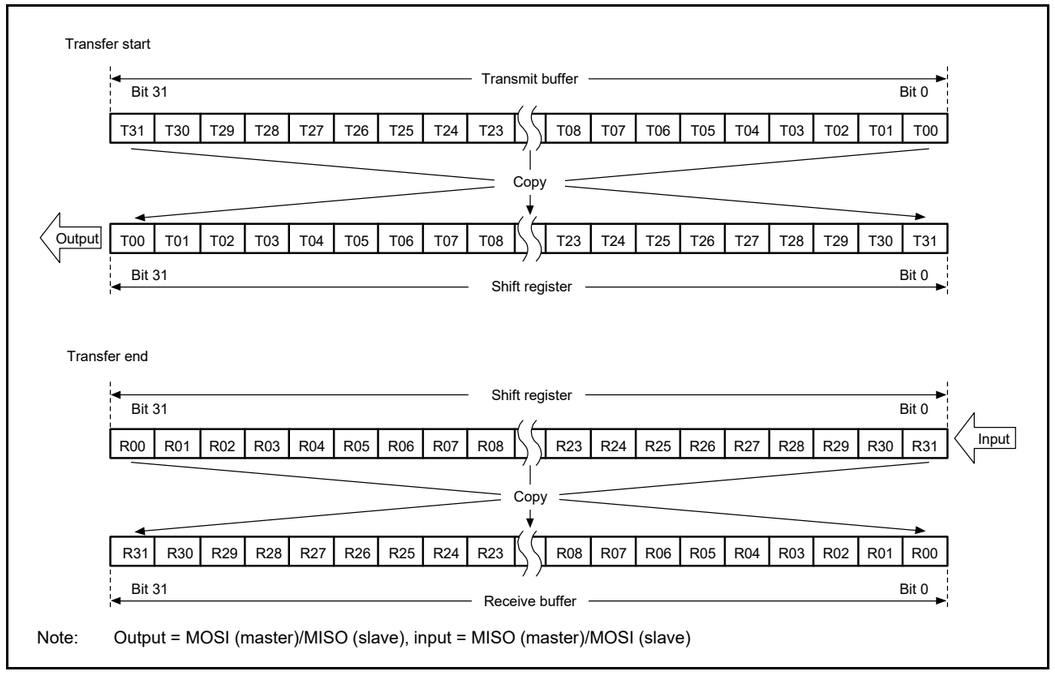
Figure 32.19 禁用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图32.20显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用、SPI数据长度为32位且选择LSB优先的传输中的操作。

在发送时，将发送缓冲器的当前级的位T31到T00逐位重新排序，以获得用于复制到移位寄存器的顺序T00到T31。发送数据从移位寄存器从T00移出到T01，并继续到T31。

在接收中，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需的RSPCK周期数后收集位R00至R31时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 32.20 LSB-first transfer with 32-bit data and parity disabled

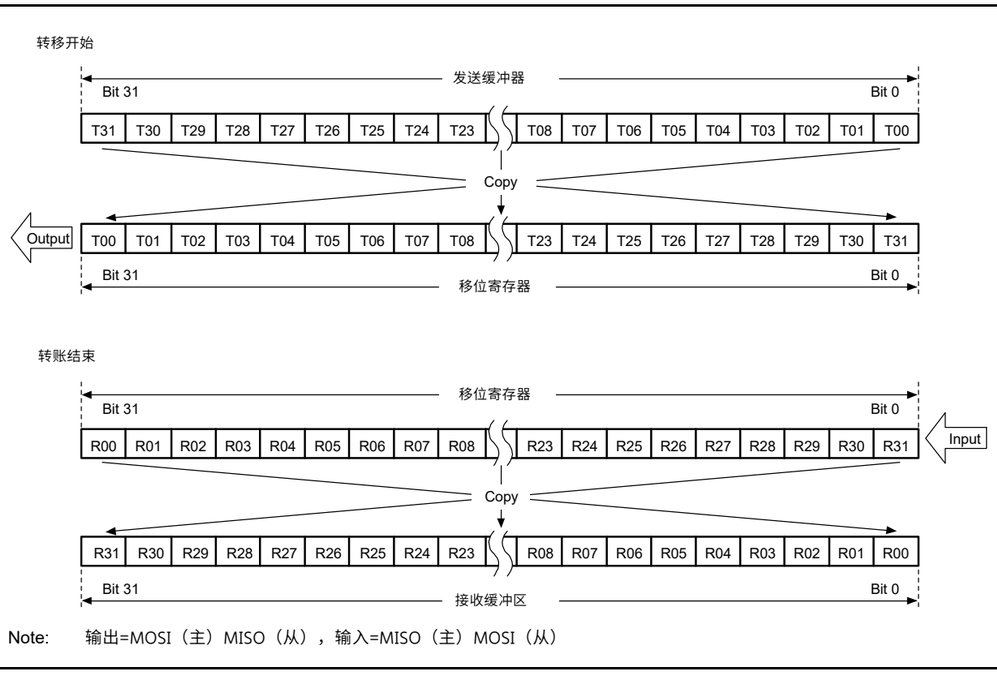
(4) LSB-first transfer with 24-bit data

Figure 32.21 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23.

In reception, received data is shifted in bit by bit through bit [8] of the shift register. When bits R00 to R23 are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission results in 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 32.20 LSB优先传输，32位数据和奇偶校验禁用

(4) 24位数据的LSB优先传输

图32.21显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用、SPI数据长度为24位（以非32位为例）的传输中的操作，并且选择LSB在先。

发送时，将发送缓冲器当前级的低24位（T23到T00）逐位重新排序，得到T00到T23的顺序，用于复制到移位寄存器。发送的数据从移位寄存器从T00移出到T01，并继续到T23。

在接收时，接收到的数据通过移位寄存器的位[8]逐位移位。在输入所需的RSPCK周期数后收集位R00至R23时，将移位寄存器中的值复制到接收缓冲区。

发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送期间将0写入位T31至T24会导致将0插入接收缓冲区的高8位。

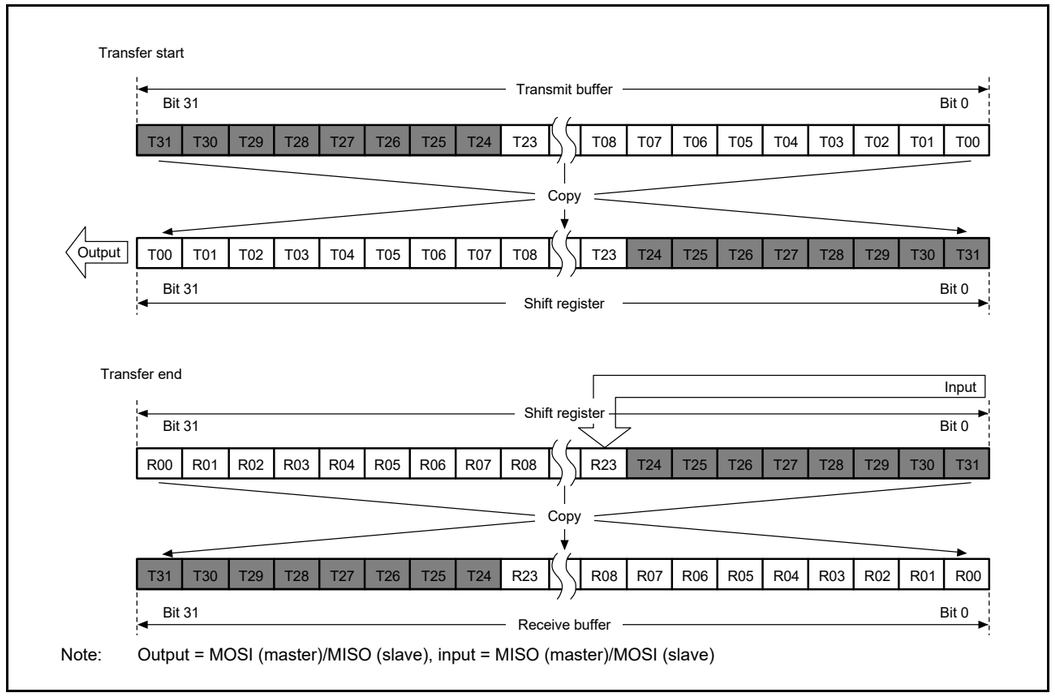


Figure 32.21 LSB-first transfer with 24-bit data and parity disabled

32.3.4.2 When parity is enabled (SPCR2.SPPE = 1)

When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 32.22 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted from T31, T30, …, T01, and P.

In reception, received data is shifted in bit by bit through bit [0] of the shift register. When bits R31 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. After copying data to the shift register, the data from R31 to P is checked for parity.

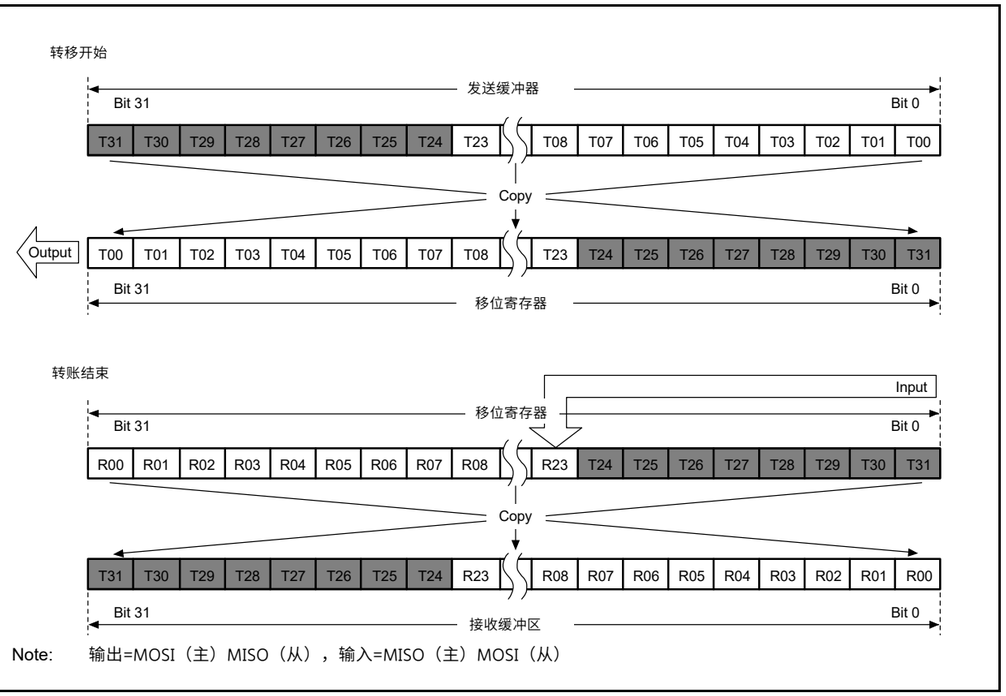


Figure 32.21 LSB优先传输，24位数据和奇偶校验禁用

32.3.4.2 启用奇偶校验时(SPCR2.SPPE=1)

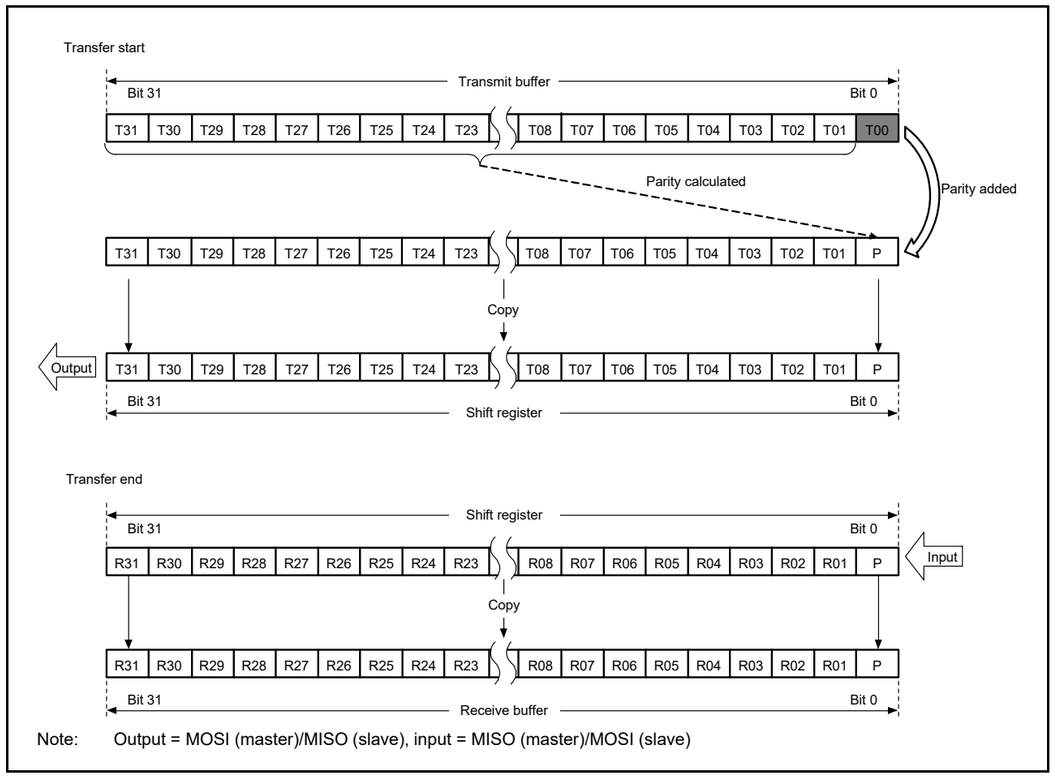
启用奇偶校验时，传输数据的最低位变为奇偶校验位。硬件计算奇偶校验位的值。

(1) 32位数据的MSB优先传输

图32.22显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验、SPI数据长度为32位且选择MSB优先的传输中的操作。

在传输中，奇偶校验位(P)的值是从位T31到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据从T31、T30、……、T01和P传输。

在接收中，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集位R31至P时，将移位寄存器中的值复制到接收缓冲区。将数据复制到移位寄存器后，对R31到P的数据进行奇偶校验。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

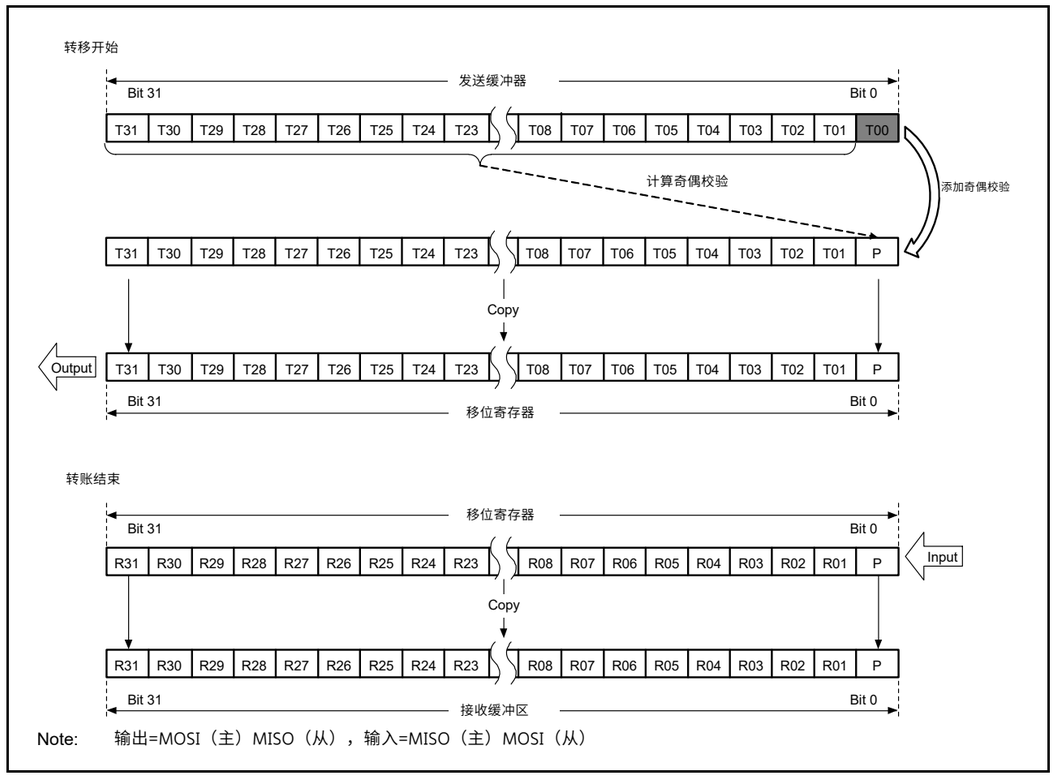
Figure 32.22 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 32.23 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted from T23, T22, …, T01, and P.

In reception, received data is shifted in bit by bit through bit [0] of the shift register. When bits R23 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. After data is copied to the shift register, the data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission results in 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

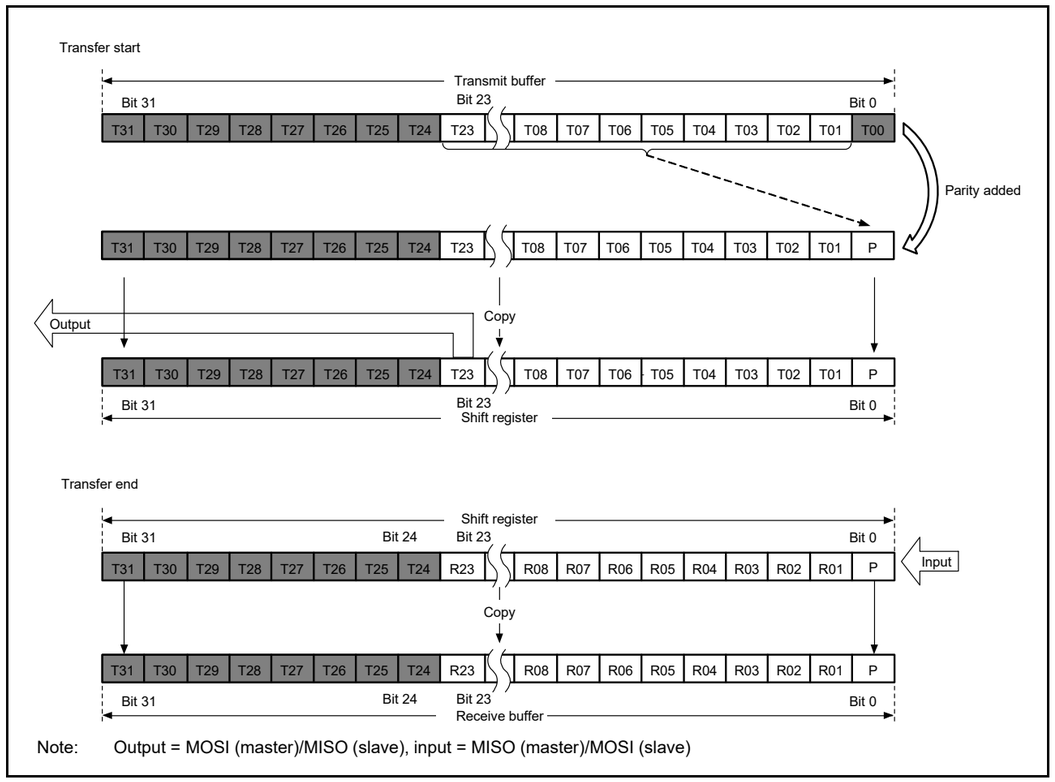
Figure 32.22 启用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图32.23显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，例如24位的SPI数据长度不是32位，并且选择MSB优先。

在传输中，奇偶校验位(P)的值是从位T23到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据从T23、T22、……、T01和P传输。

在接收中，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集位R23至P时，移位寄存器中的值被复制到接收缓冲区。数据复制到移位寄存器后，R23到P的数据进行奇偶校验。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送期间将0写入位T31至T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

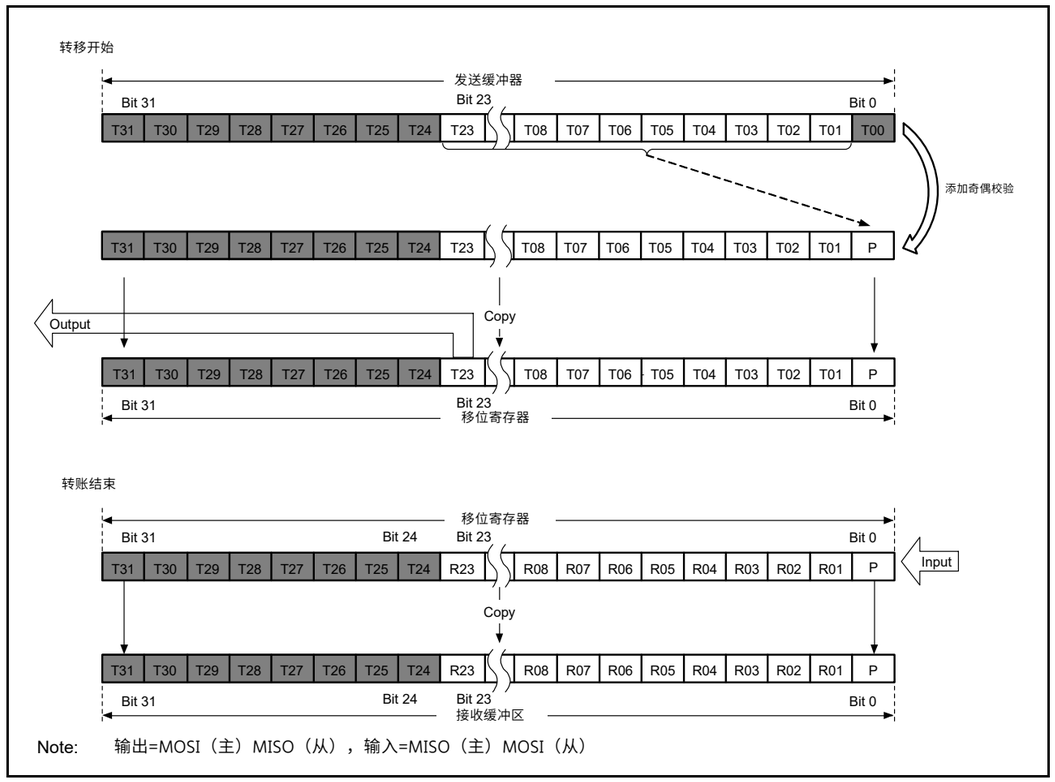
Figure 32.23 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 32.24 shows the operation the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole value is copied to the shift register. Data are transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit by bit through bit [0] of the shift register. When bits R00 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. After data is copied to the shift register, the data from R00 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

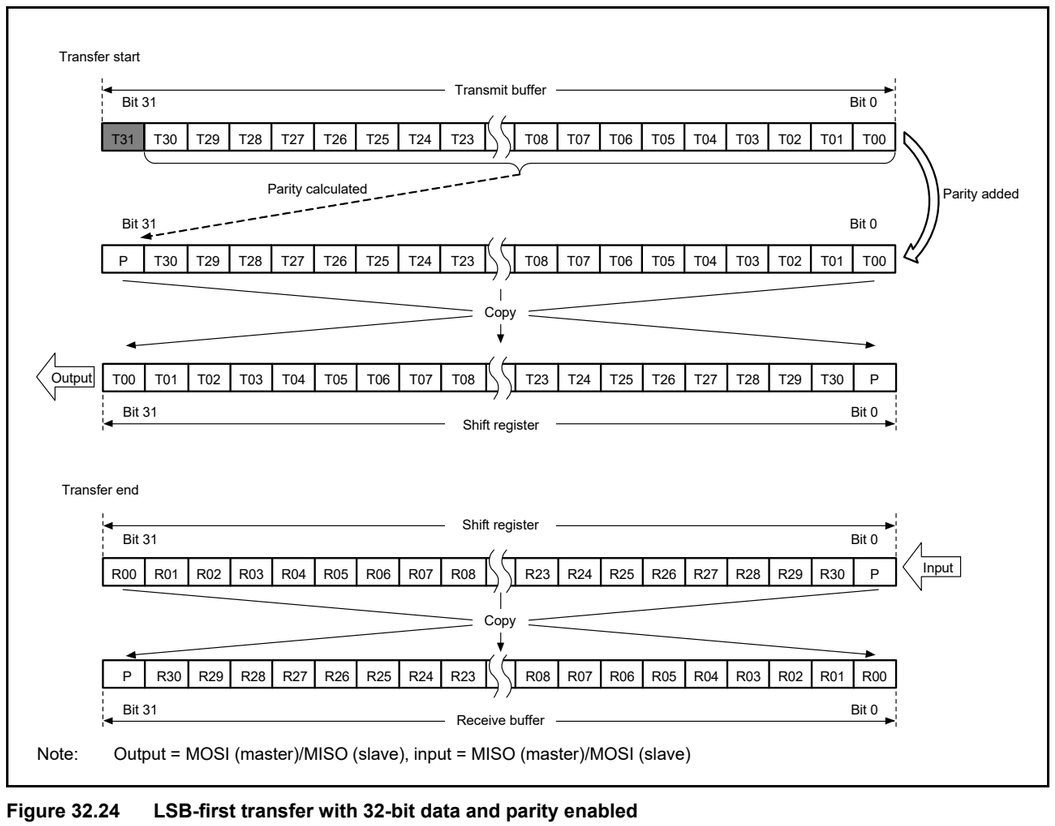
Figure 32.23 启用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图32.24显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，
SPI数据长度为32位，并选择LSB-first。

在传输中，奇偶校验位(P)的值是从位T30到T00计算的。这将替换最后一位T31，并将整个值复制到移位寄存器。数据按T00、T01、……、T30和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集位R00到P时，移位寄存器中的值被复制到接收缓冲区。数据复制到移位寄存器后，对R00到P的数据进行奇偶校验。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

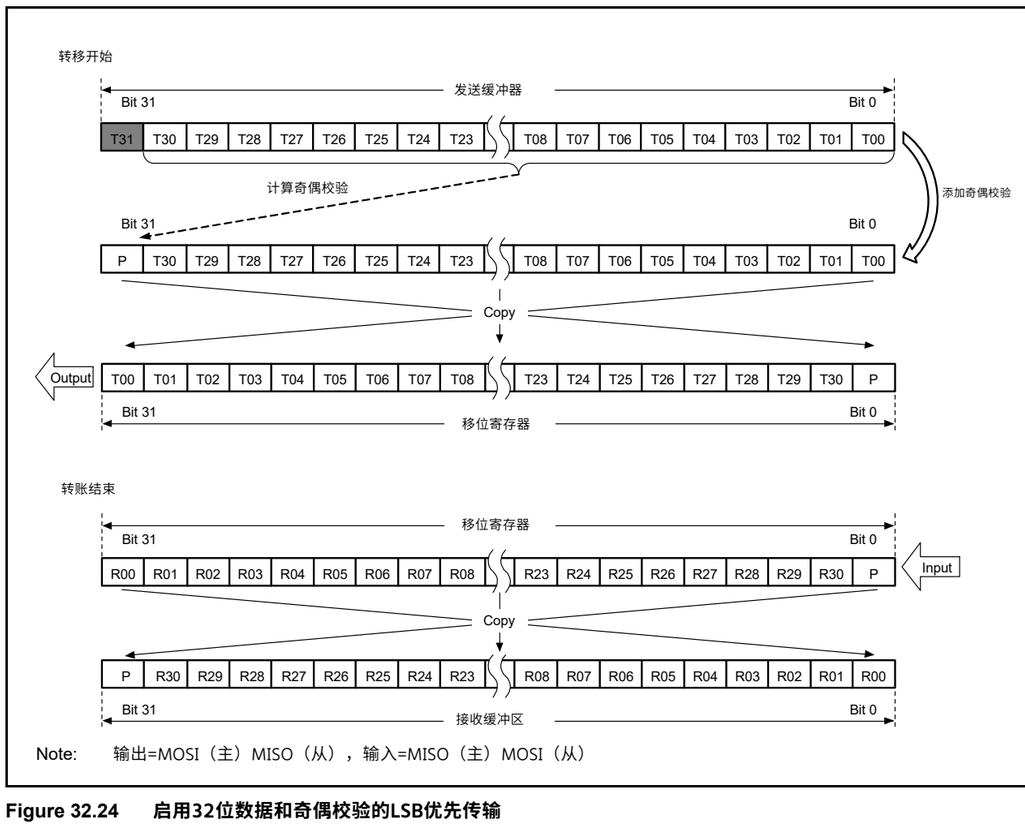
Figure 32.24 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 32.25 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits for an example that is not 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole value is copied to the shift register. Data is transmitted from T00, T01, …, T22, and P.

In reception, received data is shifted in bit by bit through bit [8] of the shift register. When bits R00 to P are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. After data is copied to the shift register, the data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission results in 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

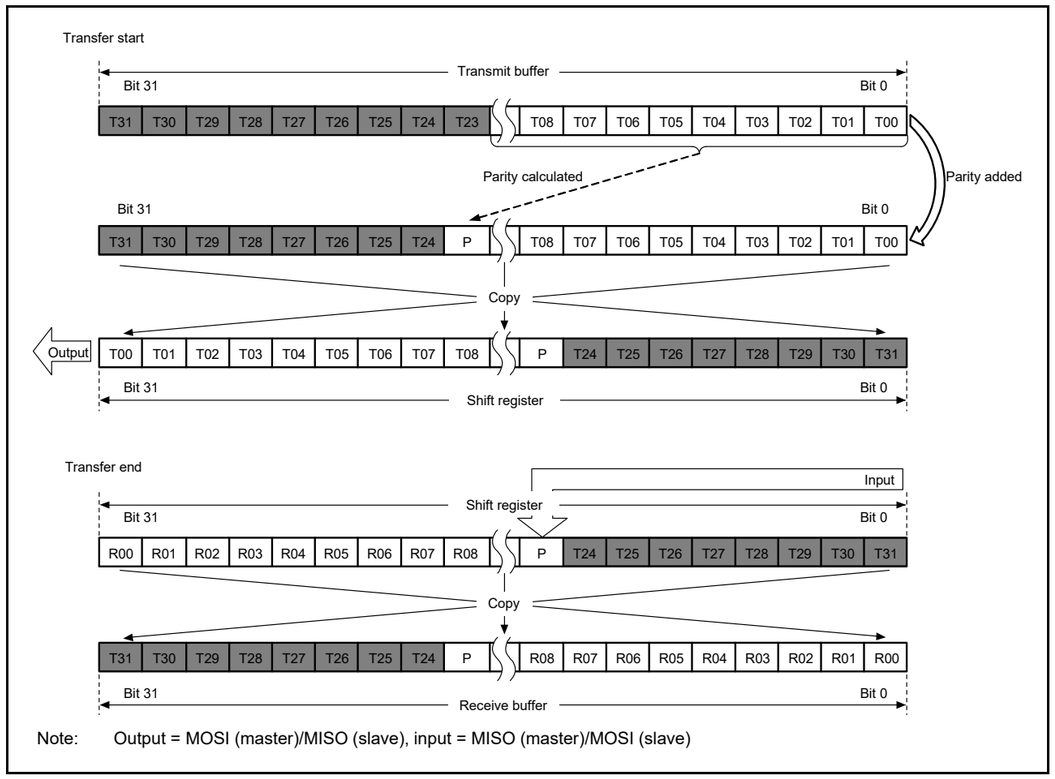
Figure 32.24 启用32位数据和奇偶校验的LSB优先传输

(4) 24位数据的LSB优先传输

图32.25显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，例如24位的SPI数据长度不是32位，并且选择LSB在先。

在传输中，奇偶校验位(P)的值是从位T22到T00计算的。这将替换最后一位T23，并将整个值复制到移位寄存器。数据从T00、T01、……、T22和P传输。

在接收时，接收到的数据通过移位寄存器的位[8]逐位移位。在输入所需数量的RSPCK周期后收集位R00到P时，移位寄存器中的值被复制到接收缓冲区。数据复制到移位寄存器后，对R00到P的数据进行奇偶校验。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送期间将0写入位T31至T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 32.25 LSB-first transfer with 24-bit data and parity enabled

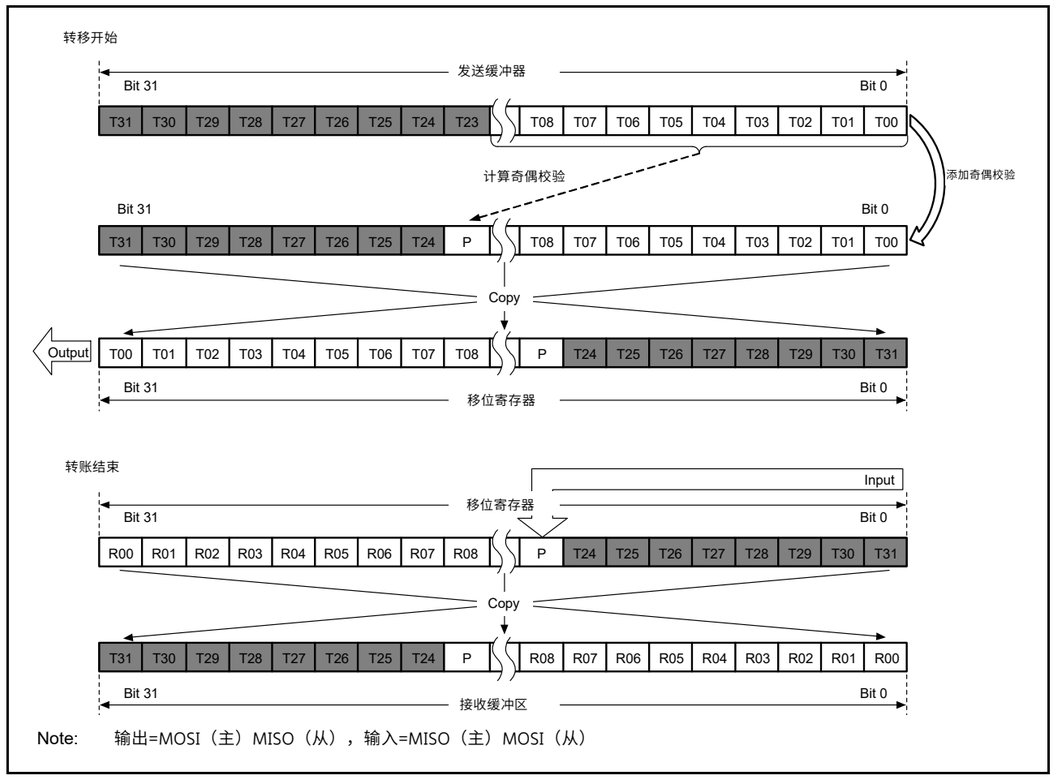
32.3.5 Transfer Format

32.3.5.1 CPHA = 0

Figure 32.26 shows an example transfer format for the serial transfer of 8-bit data when SPCMDm.CPHA is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 32.26, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when SPCMDm.CPOL is 0 and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 32.3.2, Controlling the SPI Pins.

When SPCMDm.CPHA is 0, the driving of valid data to the MOSIn and MISOn signals begins at an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCK cycle. The change timing for the MOSIn and MISOn signals is 1/2 RSPCK cycle after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing. It only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay, the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 32.3.10.1, Master mode operation.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 32.25 启用24位数据和奇偶校验的LSB优先传输

32.3.5 传输格式

32.3.5.1 CPHA = 0

图32.26显示了当SPCMDm.CPHA为0时串行传输8位数据的示例传输格式。当SPI工作在从模式(SPCR.MSTR=0)时，不执行时钟同步操作(SPCR.SPMS=1)CPHA位为0。在图32.26中，RSPCKn(CPOL=0)表示SPCMDm.CPOL为0时的RSPCKn信号波形，RSPCKn(CPOL=1)表示CPOL位为1时的RSPCKn信号波形。采样时序表示SPI将串行传输数据提取到移位寄存器的时序。信号的IO方向取决于SPI设置。有关详细信息，请参阅第32.3.2节，控制SPI引脚。

当SPMDm.CPHA为0时，将有效数据驱动到MOSIn和MISon信号开始于SSLni信号断言。在SSLni信号断言之后发生的第一个RSPCKn信号变化成为第一次传输数据获取。此后，每1个RSPCK周期对数据进行采样。MOSIn和MIOn信号的变化时间是传输数据获取时间之后的12RSPCK周期。CPOL位设置不影响RSPCK信号操作时序。它只影响信号极性。

t1表示RSPCK延迟，即从SSLni信号断言到RSPCKn振荡的周期。t2表示SSL否定延迟，即从RSPCKn振荡终止到SSLni信号否定的周期。t3表示下一次访问延迟，即在串行传输结束后为下一次传输抑制SSLni信号断言的时间段。t1、t2和t3由在SPI系统上运行的主设备控制。有关MCU的SPI处于主机模式时的t1、t2和t3的说明，请参见第32.3.10.1节，主机模式操作。

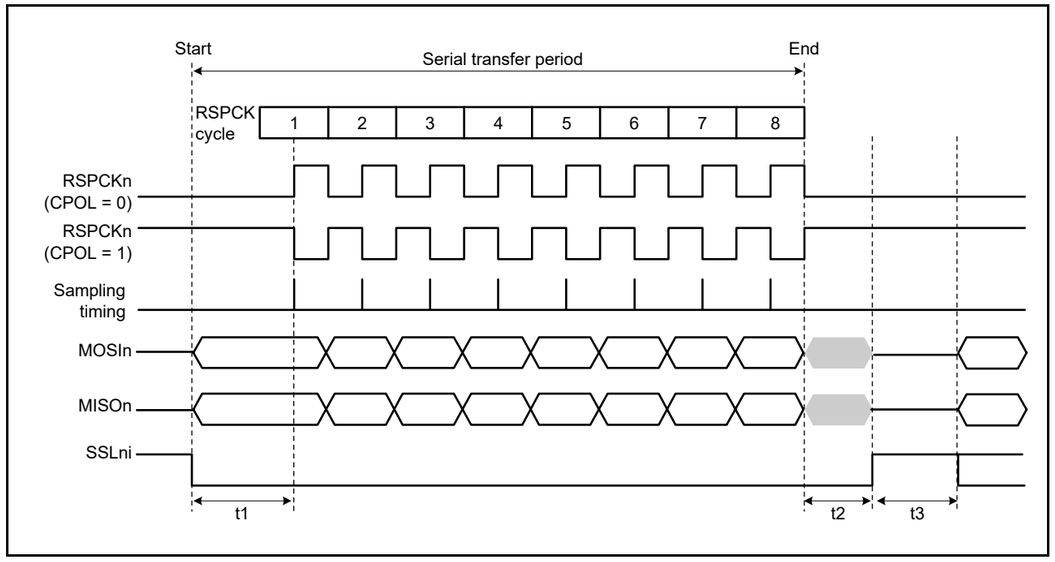


Figure 32.26 SPI transfer format with CPHA = 0

32.3.5.2 CPHA = 1

Figure 32.27 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three RSPCKn, MOSIn, and MISOn signals handle communications. In Figure 32.27, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0 and RSPCK indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave). For details, see section 32.3.2, Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal begins at an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals begins at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycle after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 32.3.10.1, Master mode operation.

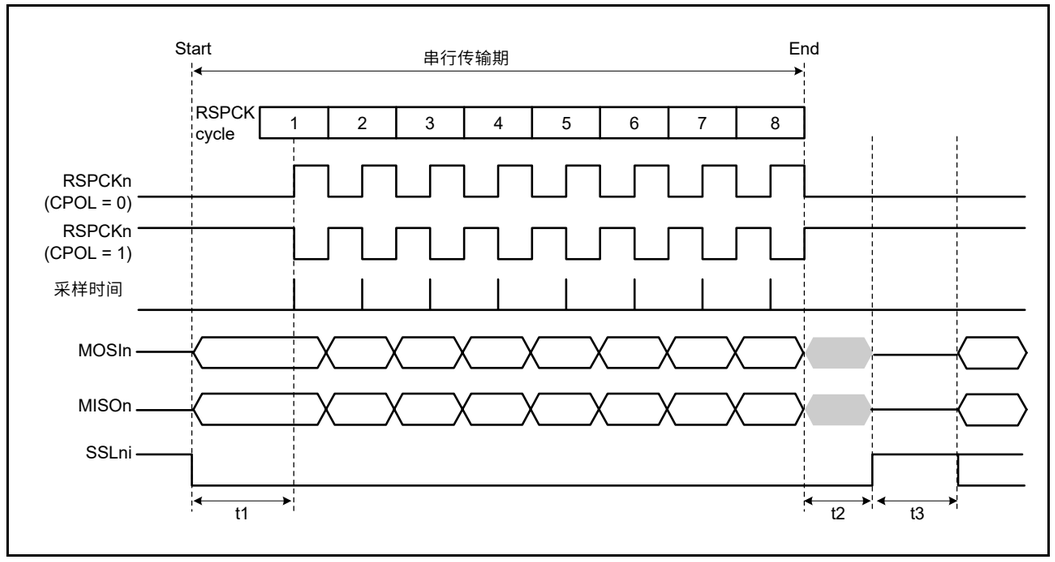


Figure 32.26 CPHA=0的SPI传输格式

32.3.5.2 CPHA = 1

图32.27显示了SPCMDm.CPHA位为1时串行传输8位数据的示例传输格式。但是，当SPCR.SPMS位为1时，不使用SSLni信号，只有三个RSPCKn、MOSIn，和MISON信号处理通信。在图32.27中，RSPCK(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形，RSPCK表示CPOL位为1时的RSPCKn信号波形。采样时序表示SPI获取串行传输的时序数据进入移位寄存器。信号的IO方向取决于SPI模式（主机或从机）。有关详细信息，请参阅第32.3.2节，控制SPI引脚。

当SPCMDm.CPHA位为1时，将无效数据驱动到MIOn信号开始于SSLni信号断言。在SSLni信号置位后发生的第一个RSPCKn信号变化时，开始向MOSIn和MISOn信号输出有效数据。此后，每1个RSPCK周期更新一次数据。传输数据获取时间是数据更新时间之后的12RSPCK周期。SPCMDm.CPOL位设置不影响RSPCKn信号操作时序。它只影响信号极性。

t1、t2、t3与CPHA=0时相同。关于MCU的SPI处于主机模式时的t1、t2和t3说明，请参见第32.3.10.1节，主机模式操作。

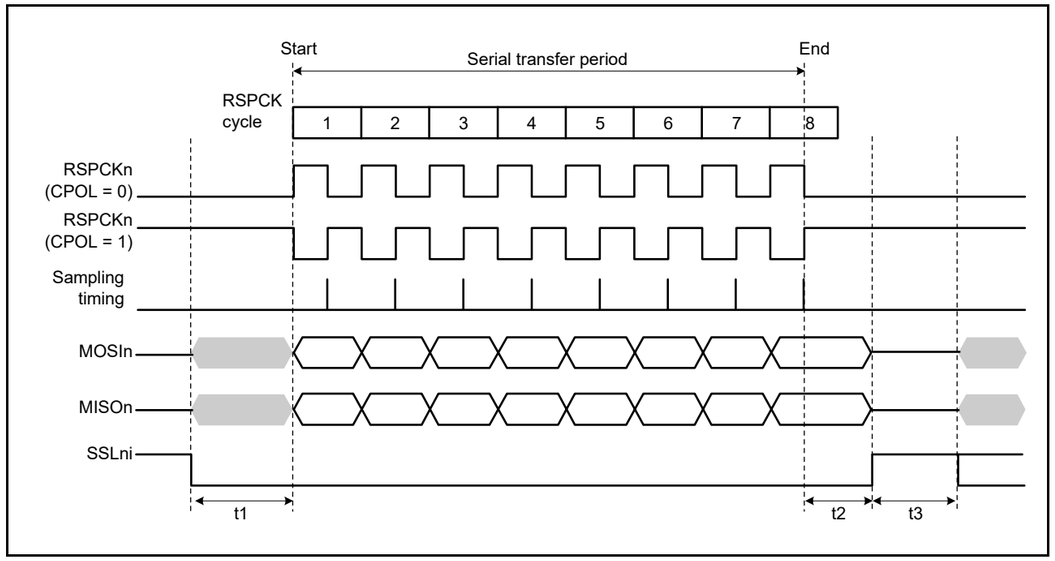


Figure 32.27 SPI transfer format with CPHA = 1

32.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected by the communications operating mode select bit (SPCR.TXMD). The register accesses shown in Figure 32.28 and Figure 32.29 indicate the condition of access to the SPDR/SPDR_HA register, where W denotes a write cycle.

32.3.6.1 Full-duplex synchronous serial communications (SPCR.TXMD = 0)

Figure 32.28 shows an example of operation where the communications operating mode select bit (SPCR.TXMD) is set to 0. In the example, the SPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0 for SPI0, and in which the SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0 for SPI1. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

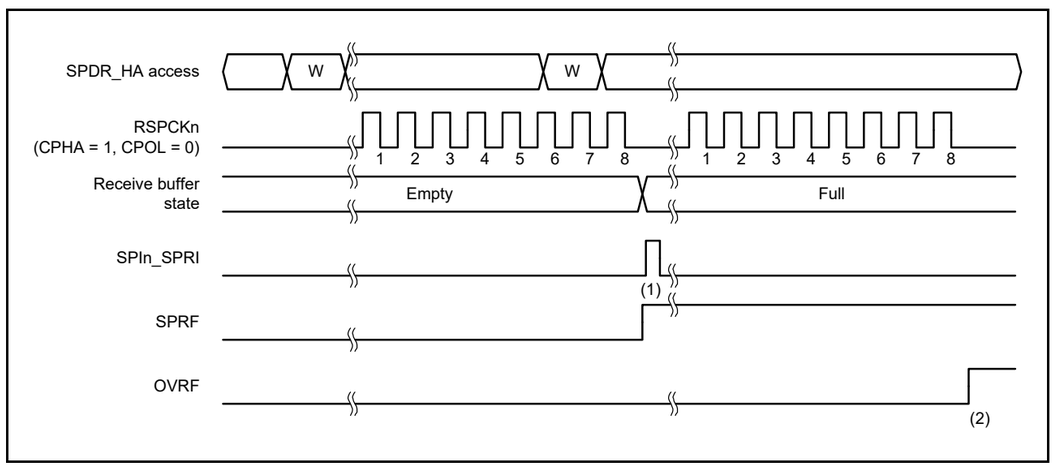


Figure 32.28 Operation example when SPCR.TXMD = 0

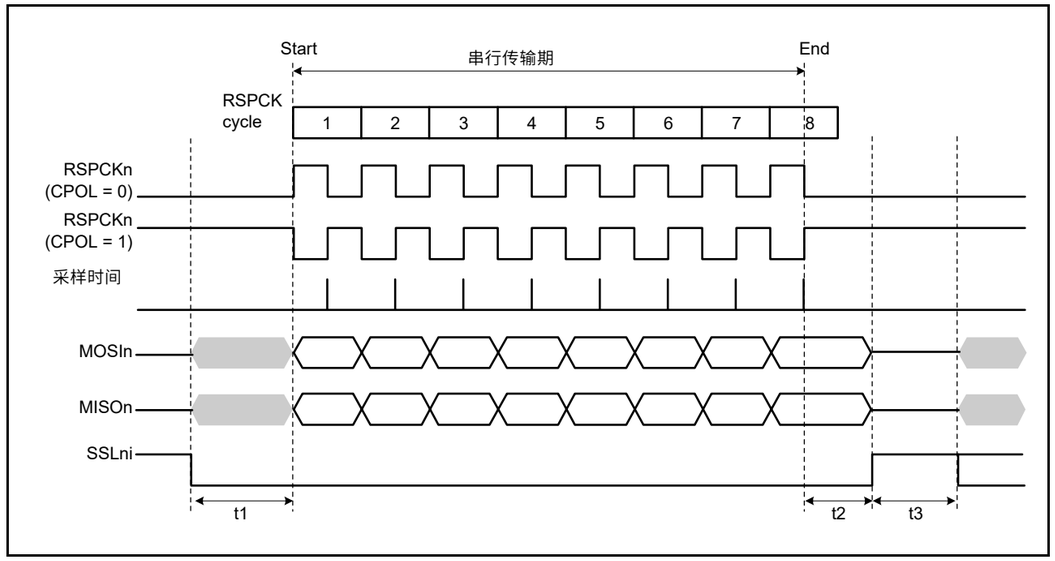


Figure 32.27 CPHA=1的SPI传输格式

32.3.6 数据传输模式

全双工同步串行通信或发送操作只能通过通信操作模式选择位(SPCR.TXMD)进行选择。图32.28和图32.29所示的寄存器访问表示访问SPDRSPDR_HA寄存器的条件，其中W表示写周期。

32.3.6.1 全双工同步串行通信(SPCR.TXMD=0)

图32.28显示了通信操作模式选择位(SPCR.TXMD)设置为0的操作示例。在该示例中，SPI执行8位串行传输，其中SPDCR.SPFC[1:0]位为00b，SPCMDm.CPHA位为1，SPI0时SPCMDm.CPOL位为0，其中SPCMD0.CPHA位为1，

SPI1的SPMD0.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，即传输的位数。

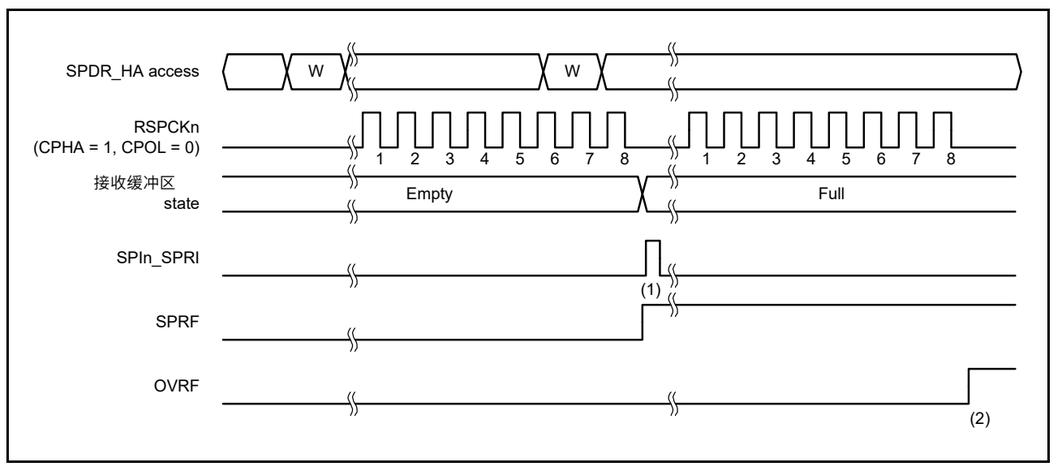


Figure 32.28 SPCR.TXMD=0时的操作示例

The operation of the flags at timings shown in (1) and (2) in Figure 32.28 is as follows:

(1) When a serial transfer ends with the SPDR_HA receive buffer empty, the SPI generates a receive buffer full interrupt request (SPIn_SPRI), the SPI sets the SPSR.SPRF flag to 1, and the received data is copied from the shift register to the receive buffer.

(2) When a serial transfer ends with the SPDR_HA receive buffer holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1 and discards the received data in the shift register.

32.3.6.2 Transmit-only operations (SPCR.TXMD = 1)

Figure 32.29 shows an operation example where the communications operating mode select bit (SPCR.TXMD) is set to 1. In the example in Figure 32.29, the SPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0 for SPI0, and in which the SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0 for SPI1. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

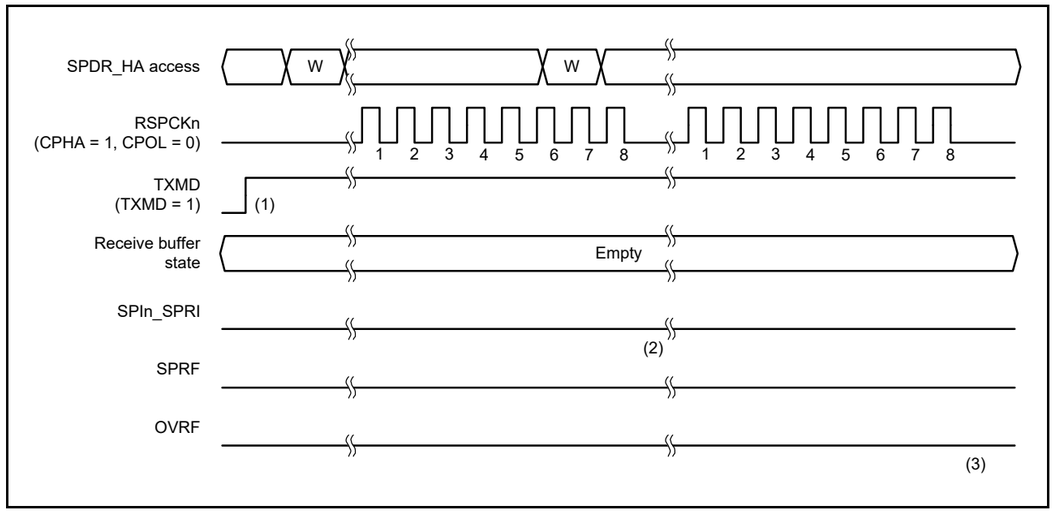


Figure 32.29 Operation example when SPCR.TXMD = 1

The operation of the flags at timings shown in (1) to (3) in Figure 32.29 is as follows:

(1) Make sure there is no data left in the receive buffer (SPSR.SPRF flag = 0) and the SPSR.OVRF flag is 0 before entering the transmit-only operation mode (SPCR.TXMD = 1).

(2) When a serial transfer ends with the receive buffer of SPDR_HA empty, if the transmit-only mode is selected (SPCR.TXMD = 1), the SPSR.SPRF flag remains 0, and the SPI does not copy the data in the shift register to the receive buffer.

(3) Because the receive buffer of SPDR_HA does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag remains 0, and the data in the shift register is not copied to the receive buffer.

When performing transmit-only operations (SPCR.TXMD = 1), the SPI transmits but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

32.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 32.30 and Figure 32.31 show operation examples of the transmit buffer empty interrupt (SPIn_SPTI) and the receive buffer full interrupt (SPIn_SPRI). The register accesses shown in these figures indicate the conditions of access to the SPDR_HA register, where W denotes a write cycle, and R a read cycle. In Figure 32.26, the SPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 0, and the SPCMDm.CPOL bit is 0 for SPI0, and in which the SPCR.TXMD bit is 0, the SPCMD0.CPHA bit is 0, and the

图32.28中(1)和(2)所示时序的标志操作如下：

(1)当串行传输结束且SPDR_HA接收缓冲区为空时，SPI产生接收缓冲区满中断请求（SPIn_SPRI），SPI将SPSR.SPRF标志设置为1，并将接收到的数据从移位寄存器复制到接收缓冲区。

(2)当串行传输结束时，SPDR_HA接收缓冲区保存了前一次串行传输中接收到的数据，SPI将SPSR.OVRF标志设置为1，并丢弃移位寄存器中的接收数据。

32.3.6.2 Transmit-only operations (SPCR.TXMD = 1)

图32.29显示了通信操作模式选择位(SPCR.TXMD)设置为1的操作示例。在图32.29的示例中，SPI执行8位串行传输，其中SPDCR.SPFC[1:0]位为00b，SPCMDm.CPHA位为1，SPI0时SPCMDm.CPOL位为0，其中SPCMD0.CPHA位为1，SPI1时SPCMD0.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，即传输的位数。

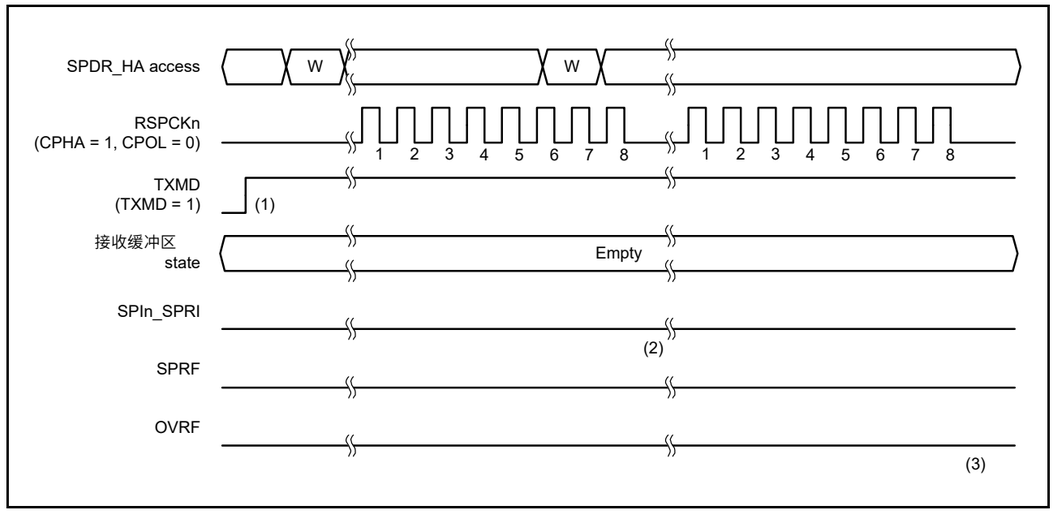


Figure 32.29 SPCR.TXMD=1时的操作示例

图32.29中(1)至(3)所示时序的标志操作如下：

(1)在进入仅发送操作模式(SPCR.TXMD=1)之前，确保接收缓冲区中没有剩余数据(SPSR.SPRF标志=0)并且SPSR.OVRF标志为0。

(2)当串行传输结束且SPDR_HA的接收缓冲区为空时，如果选择了仅发送模式
（SPCR.TXMD=1），SPSR.SPRF标志保持为0，SPI不将移位寄存器中的数据复制到接收缓冲区。

(3)因为SPDR_HA的接收缓冲区中没有保存上一次串行传输接收到的数据，所以即使一次串行传输结束，SPSR.OVRF标志保持为0，移位寄存器中的数据也不会复制到接收缓冲。

执行仅发送操作（SPCR.TXMD=1）时，SPI发送但不接收数据。因此，SPSR.SPRF和SPSR.OVRF标志在时间(1)到(3)保持0。

32.3.7 发送缓冲区空和接收缓冲区满中断

图32.30和图32.31显示了发送缓冲区空中断(SPIn_SPTI)和接收缓冲区满中断(SPIn_SPRI)的操作示例。这些图中显示的寄存器访问表示访问SPDR_HA寄存器的条件，其中W表示写周期，R表示读周期。在图32.26中，SPI执行8位串行传输，其中SPCR.TXMD位为0，SPDCR.SPFC[1:0]位为00b，SPCMDm.CPHA位为0，SPCMDm.CPOL位SPI0为0，其中SPCR.TXMD位为0，SPCMD0.CPHA位为0，

SPCMD0.CPOL bit is 0 for SPI1.

In Figure 32.27, the SPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0 for SPI0, and in which the SPCR.TXMD bit is 0, the SPCMD0.CPHA bit is 1, and the SPCMD0.CPOL bit is 0 for SPI1. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

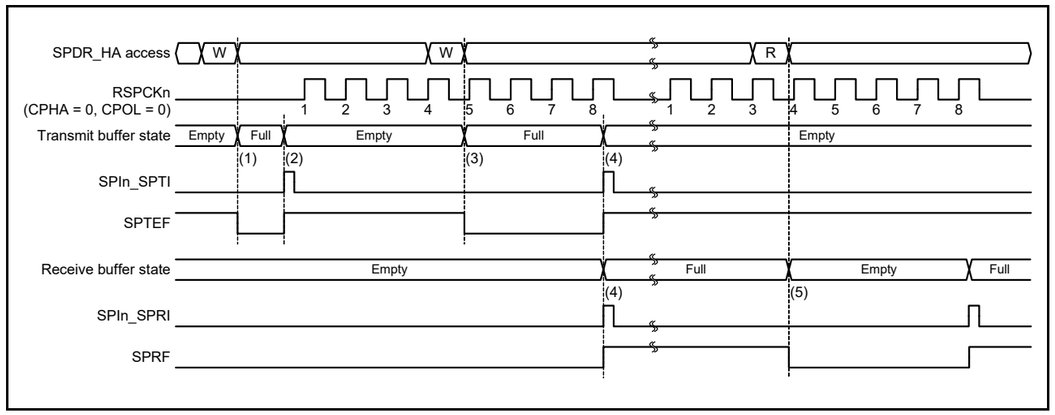


Figure 32.30 Operation example of SPIn_SPTI and SPIn_SPRI interrupts when CPHA = 0 and CPOL = 0

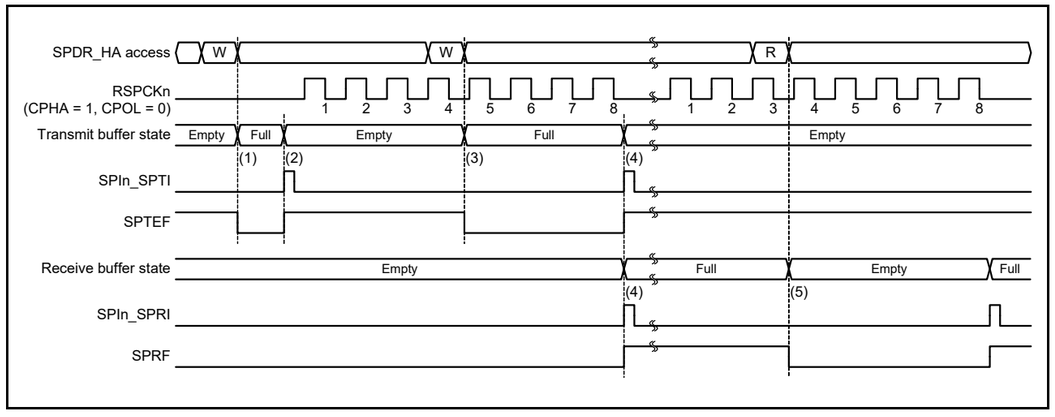


Figure 32.31 Operation example of SPIn_SPTI and SPIn_SPRI interrupts when CPHA = 1 and CPOL = 0

The operation of the SPI at timings shown in (1) to (5) in Figure 32.31 is as follows:

(1) When transmit data is written to the SPDR_HA register with the transmit buffer of SPDR_HA empty and data for the next transfer not set, the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.

(2) If the shift register is empty, the SPI copies data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIn_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the mode of the SPI. For details, see section 32.3.10, SPI Operation, and section 32.3.11, Clock Synchronous Operation.

(3) When transmit data is written to the SPDR_HA register either by the transmit buffer empty interrupt routine, or by the processing of transmit buffer empty using SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the serially transferred data is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.

(4) When the serial transfer ends with the receive buffer of SPDR_HA empty, the SPI copies the receive data in the shift register to the receive buffer and generates a receive buffer full interrupt request (SPIn_SPRI), and sets the

SPI1的SPMD0.CPOL位为0。

在图32.27中，SPI执行8位串行传输，其中SPCR.TXMD位为0，SPDCR.SPFC[1:0]位为00b，SPCMDm.CPHA位为1，SPCMDm.CPOL位SPI0为0，其中SPCR.TXMD位为0，SPCMD0.CPHA位为1，SPCMD0.CPOL位为0为SPI1。波形中为RSPCKn给出的数字表示RSPCK周期数，即传输的位数。

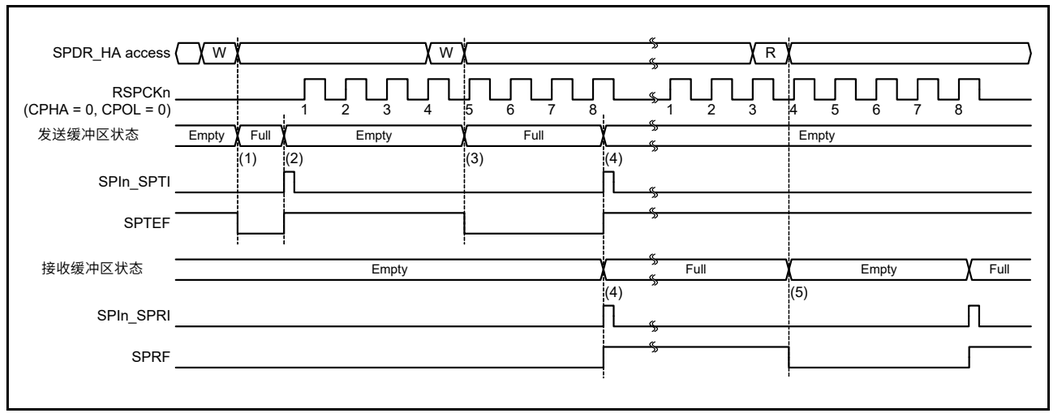


Figure 32.30 CPHA=0和CPOL=0时SPIn_SPTI和SPIn_SPRI中断的操作示例

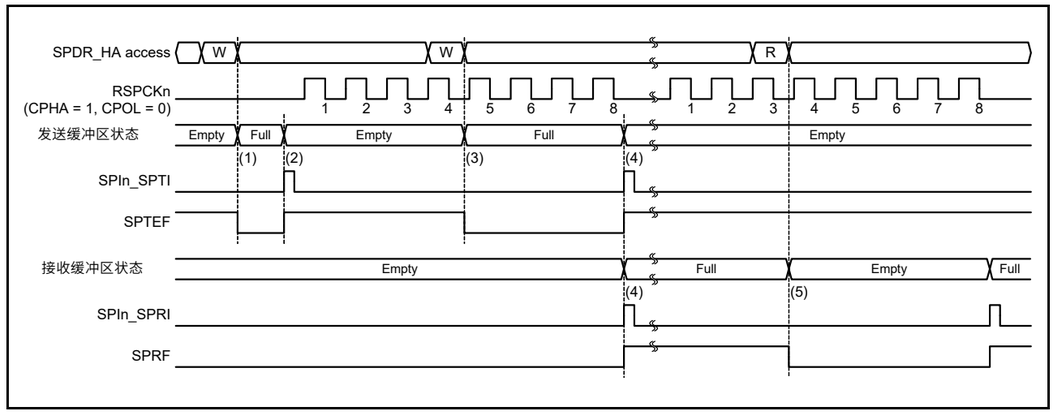


Figure 32.31 CPHA=1和CPOL=0时SPIn_SPTI和SPIn_SPRI中断的操作示例

SPI在图32.31中(1)到(5)所示时序的操作如下：

(1)当发送数据写入SPDR_HA寄存器且SPDR_HA的发送缓冲区为空且未设置下一次传输的数据时，SPI将数据写入发送缓冲区并将SPSR.SPTEF标志清除为0。

(2)如果移位寄存器为空，SPI将发送缓冲区中的数据复制到移位寄存器，产生发送缓冲区空中断请求（SPIn_SPTI），并将SPSR.SPTEF标志设置为1。如何启动串行传输取决于SPI的模式。有关详细信息，请参见第32.3.10节，SPI操作和第32.3.11节，时钟同步操作。

(3)当发送数据被发送缓冲区空中断程序写入SPDR_HA寄存器时，或者通过使用SPTEF标志处理发送缓冲区空，SPI将数据写入发送缓冲区并将SPTEF标志清除为0。因为串行传输的数据存储在移位寄存器中，SPI不会将发送缓冲区中的数据复制到移位寄存器中。

(4)当串行传输结束且SPDR_HA的接收缓冲区为空时，SPI将移位寄存器中的接收数据复制到接收缓冲区并产生接收缓冲区满中断请求(SPIn_SPRI)，并设置

SPRF flag to 1. Because the shift register is empty on completion of the serial transfer, if the transmit buffer was full before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies the data in the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, and data transfer from the transmit buffer to the shift register is enabled.

(5) When SPDR_HA is read either by the receive buffer full interrupt routine or by the processing of the receive buffer full interrupt using the SPRF flag, the receive data can be read.

If SPDR_HA is written to when the transmit buffer holds untransmitted data (SPTEF = 0), the SPI does not update the data in the transmit buffer. When writing to SPDR_HA, make sure to use a transmit buffer empty interrupt request or to process a transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (SPCR.SPE = 0), set the SPTIE bit to 0.

When serial transfer ends with the receive buffer full (SPRF = 1), the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 32.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRj.IR flags in the ICU, where j is the interrupt vector number, can be used to confirm the states of the transmission and reception buffers. Similarly, the SPTEF and the SPRF flags can be used to confirm the states of the transmission and reception buffers. See section 14, Interrupt Controller Unit (ICU), for the interrupt vector numbers.

32.3.8 Error Detection

In normal SPI serial transfer, data written to the transmit buffer of SPDR/SPDR_HA is transmitted, and received data can be read from the SPDR/SPDR_HA receive buffer. If access is made to SPDR/SPDR_HA, an abnormal transfer might occur depending on the status of the transmit or receive buffer, or the status of the SPI at the beginning or end of a serial transfer.

If an abnormal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 32.8 shows the relationship between non-normal transfer operations and the SPI error detection function.

Table 32.8 Relationship between non-normal transfer operations and SPI error detection function (1 of 2)

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full	• The contents of the transmit buffer are kept • Write data is missing.	None
2	SPDR/SPDR_HA is read when the receive buffer is empty	The contents of the receive buffer and previously received data are output	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOA output signal is stopped • SPI function is disabled.	Underrun error
4	Serial transfer terminates when the receive buffer is full	• The contents of the receive buffer are kept • Receive data is missing.	Overrun error
5	An incorrect parity bit is received during full-duplex synchronous serial communications with the parity function enabled	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode	• Driving of the RSPCKn, MOSIn, and SSLn1 to SSLn3 output signals is stopped • SPI function is disabled.	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the RSPCKn, MOSIn, and SSLn1 to SSLn3 output signals is stopped • SPI function is disabled.	Mode fault error

SPRF标志为1。由于串行传输完成时移位寄存器为空，如果在串行传输结束前传输缓冲区已满，SPI将SPTEF标志设置为1，并将传输缓冲区中的数据复制到移位寄存器.即使在溢出错误状态下没有将接收到的数据从移位寄存器复制到接收缓冲区，在串行传输完成时，SPI会确定移位寄存器为空，并且从发送缓冲区到移位寄存器的数据传输是启用。

(5)当接收缓冲区满中断程序或使用SPRF标志的接收缓冲区满中断处理读取SPDR_HA时，可以读取接收数据。

如果在发送缓冲区保存未发送数据（SPTEF=0）时写入SPDR_HA，则SPI不会更新发送缓冲区中的数据。写入SPDR_HA时，请确保使用发送缓冲区空中断请求或使用SPTEF标志处理发送缓冲区空中断。要使用发送缓冲区空中断，请将SPCR中的SPTIE位设置为1。如果禁用SPI功能（SPCR.SPE=0），请将SPTIE位设置为0。

当串行传输以接收缓冲区满（SPRF=1）结束时，SPI不会将数据从移位寄存器复制到接收缓冲区，它会检测到溢出错误（参见第32.3.8节，错误检测）。为防止接收数据溢出错误，请在下一次串行传输结束前使用接收缓冲区满中断请求读取接收数据。要使用SPI接收缓冲区满中断，请将SPCR.SPRIE位设置为1。

ICU中的发送和接收中断或相关的IELSRj.IR标志，其中j是中断向量号，可用于确认发送和接收缓冲区的状态。类似地，SPTEF和SPRF标志可用于确认发送和接收缓冲器的状态。有关中断向量编号，请参见第14节，中断控制器单元(ICU)。

32.3.8 错误检测

在正常的SPI串行传输中，写入SPDRSPDR_HA的发送缓冲区的数据被发送，接收到的数据可以从SPDRSPDR_HA接收缓冲区中读取。如果访问SPDRSPDR_HA，根据发送或接收缓冲区的状态，或串行传输开始或结束时SPI的状态，可能会发生异常传输。

如果发生异常传输，SPI会将事件检测为欠载错误、溢出错误、奇偶校验错误或模式故障错误。表32.8显示了非正常传输操作和SPI错误检测功能之间的关系。

Table 32.8 非正常传输操作与SPI错误检测功能的关系(1of2)

Operation	发生条件	SPI操作	错误检测
1	SPDRSPDR_HA在发送缓冲区已满时写入	发送缓冲区的内容被保留 写数据丢失。	None
2	SPDR接收缓冲区为空时读取SPDR_HA	输出接收缓冲区的内容和先前接收的数据	None
3	当SPI无法传输数据时，串行传输在从模式下启动	串行传输暂停 发送或接收数据丢失 MISOA输出信号的驱动已停止 SPI功能已禁用。	Underrun error
4	当接收缓冲区已满时串行传输终止	接收缓冲区的内容被保留 接收数据丢失。	溢出错误
5	在启用奇偶校验功能的全双工同步串行通信期间接收到错误的奇偶校验位	奇偶错误标志被置位	奇偶校验错误
6	当串行传输在多主模式下空闲时，SSLn0输入信号被置位	停止驱动RSPCKn、MOSIn和SSLn1至SSLn3输出信号 禁用SPI功能。	模式故障错误
7	SSLn0输入信号在多主机模式下的串行传输期间被置位	串行传输暂停 发送或接收数据丢失 RSPCKr模式故障错误 MOSIn和SSLn1至SSLn3输出信号的驱动已停止 SPI功能已禁用。	

Table 32.8 Relationship between non-normal transfer operations and SPI error detection function (2 of 2)

Operation	Occurrence condition	SPI operation	Error detection
8	The SSLn0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended • Missing transmit/receive data • Driving of the MISOn output signal is stopped • SPI function is disabled.	Mode fault error

In operation 1 described in Table 32.8, the SPI does not detect an error. To prevent data omission during writes to SPDR/SPDR_HA, the writes to SPDR/SPDR_HA must be executed using a transmit buffer empty interrupt request (when SPSR.SPTEF flag is 1).

Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR/SPDR_HA reads must be executed using an SPI receive buffer full interrupt request (when SPSR.SPRF flag is 1).

For information on:

- Underrun errors, indicated in operation 3, see section 32.3.8.4, Underrun errors.
- Overrun errors, indicated in operation 4, see section 32.3.8.1, Overrun errors.
- Parity errors, indicated in operation 5, see section 32.3.8.2, Parity errors.
- Mode fault errors, indicated in operations 6 to 8, see section 32.3.8.3, Mode fault errors.
- Transmit and receive interrupts, see section 32.3.7, Transmit Buffer Empty and Receive Buffer Full Interrupts.

32.3.8.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data before the error occurrence is saved in the receive buffer. To set the OVRF flag to 0, write 0 to it after the CPU reads SPSR with the OVRF flag set to 1.

Figure 32.32 shows an example operation of OVRF and SPRF flags. The SPSR and SPDR_HA accesses shown in Figure 32.32 indicate the condition of accesses to the SPSR and SPDR_HA, respectively, where W denotes a write cycle, and R a read cycle. In the example, the SPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

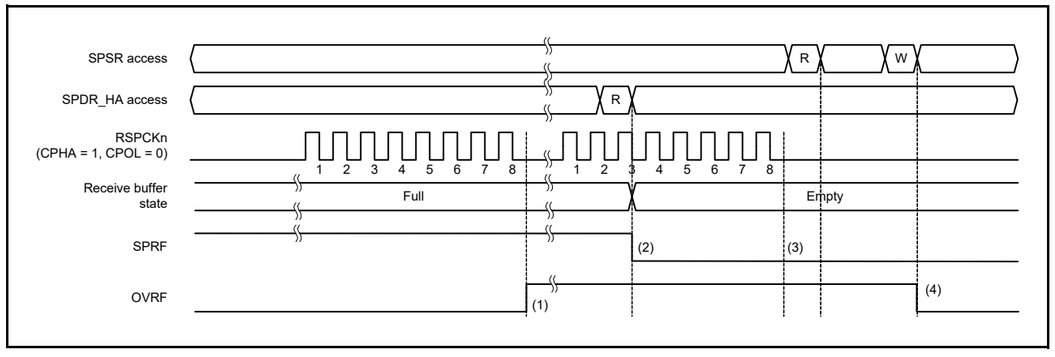


Figure 32.32 Operation example of OVRF and SPRF flags

The operation of the flags at the timing shown in (1) to (4) in Figure 32.32 is as follows:

(1) If a serial transfer terminates with the SPRF flag set to 1 (the receive buffer full), the SPI detects an overrun error and sets the OVRF flag to 1. The SPI does not copy data in the shift register to the receive buffer. Even if the SPPE bit is 1, parity errors are not detected. In master mode for SPI0, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits.

(2) When SPDR/SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The emptying of the receive buffer does not set the OVRF flag to 0.

Table 32.8 非正常传输操作与SPI错误检测功能的关系(2of2)

Operation	发生条件	SPI操作	错误检测
8	SSLn0输入信号在从模式下的串行传输期间被否定。	串行传输暂停 缺少发送接收数据 停止MI On输出信号的驱动 禁用SPI功能。	模式故障错误

在表32.8中描述的操作1中，SPI未检测到错误。防止写入SPDR期间的数据遗漏SPDR_HA，对SPDRSPDR_HA的写入必须使用发送缓冲区空中断请求（当SPSR.SPTEF标志为1)。

同样，SPI不会检测到操作2中的错误。为防止读取无关数据，必须使用SPI接收缓冲区满中断请求（当SPSR.SPRF标志为1时）执行SPDRSPDR_HA读取。

有关以下信息：

- 运行3中指示的欠载错误，请参阅第32.3.8.4节，欠载错误。
- 操作4中指示的溢出错误，请参阅第32.3.8.1节，溢出错误。
- 操作5中指示的奇偶校验错误，请参阅第32.3.8.2节，奇偶校验错误。
- 模式故障错误，在操作6到8中指示，请参阅第32.3.8.3节，模式故障错误。
- 发送和接收中断，请参见第32.3.7节，发送缓冲区空和接收缓冲区满中断。

32.3.8.1 溢出错误

如果串行传输在SPDRSPDR_HA的接收缓冲区已满时结束，则SPI检测到溢出错误并将SPSR.OVRF标志设置为1。当OVRF标志为1时，SPI不会将数据从移位寄存器复制到接收缓冲区，因此错误发生前的数据保存在接收缓冲区中。要将OVRF标志设置为0，请在CPU读取OVRF标志设置为1的SPSR后向其写入0。

图32.32显示了OVRF和SPRF标志的示例操作。图32.32所示的SPSR和SPDR_HA访问分别表示访问SPSR和SPDR_HA的条件，其中W表示写周期，R表示读周期。在示例中，SPI执行8位串行传输，其中SPCMDm.CPHA位为1，SPCMDm.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，表示传输位。

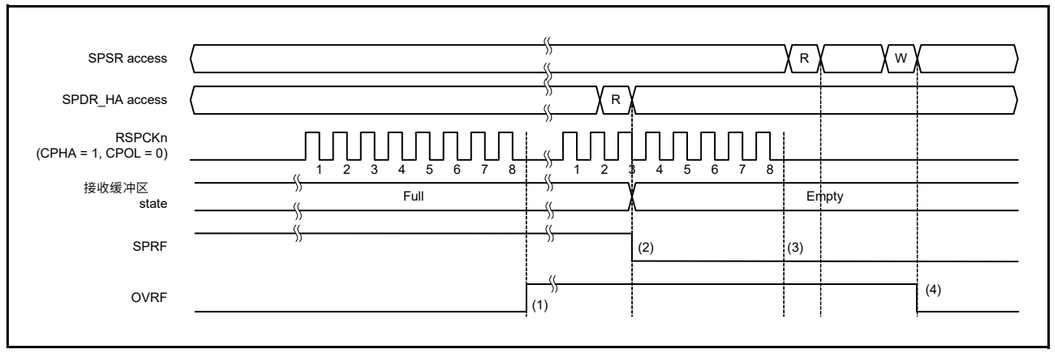


Figure 32.32 OVRF和SPRF标志的操作示例

图32.32中(1)到(4)所示时序的标志操作如下：

(1)如果串行传输终止且SPRF标志设置为1（接收缓冲区已满），则SPI检测到溢出错误并将OVRF标志设置为1。SPI不会将移位寄存器中的数据复制到接收缓冲区.即使SPPE位为1，也不会检测到奇偶校验错误。在SPI0的主模式下，SPI将SPCMDm指针的值复制到SPSSR.SPECM[2:0]位。

(2)当读取SPDRSPDR_HA时，SPI输出接收缓冲区中的数据。然后SPRF标志设置为0。接收缓冲区的清空不会将OVRF标志设置为0。

(3) If the serial transfer ends with the OVRF flag set to 1 (an overrun error occurs), the SPI does not copy the data in the shift register to the receive buffer (the SPRF flag is not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. When in master mode for SPI0, the SPI does not update the SPSSR.SPECM[2:0] bits. When an overrun error occurs and the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.

(4) If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag is set to 0.

The occurrence of an overrun error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, make sure that overrun errors are detected early, for instance by reading SPSR immediately after SPDR/SPDR_HA is read. When the SPI is in master mode for SPI0, the value of the SPCMDm pointer at the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits. If an overrun error occurs and the OVRF flag is set to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

When the RSPCK auto-stop function is enabled in master mode, an overrun error does not occur. Figure 32.33 and Figure 32.34 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

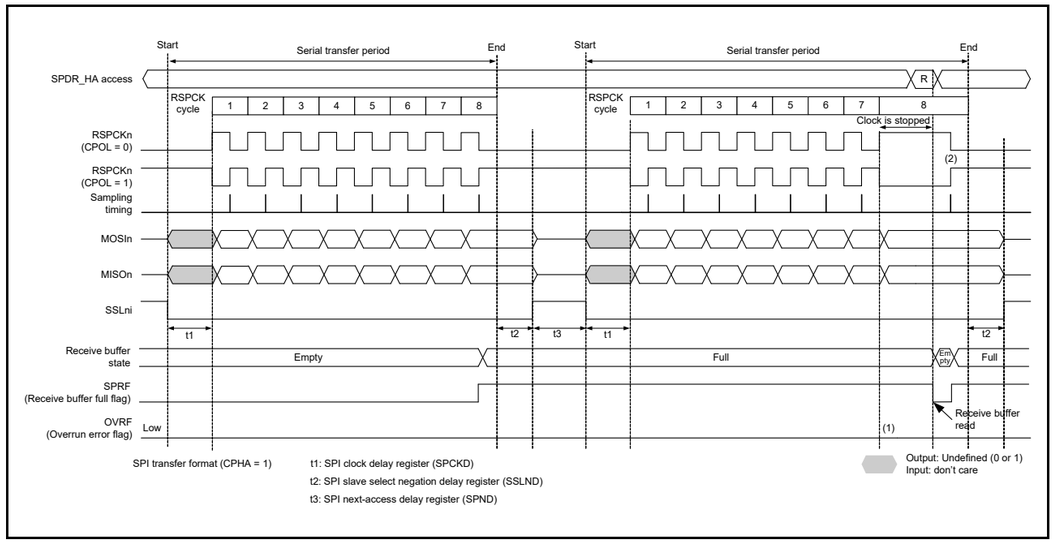


Figure 32.33 Clock stop waveform when serial transfer continues while receive buffer is full in master mode with CPHA = 1

(3)如果串行传输以OVRF标志设置为1（发生溢出错误）结束，则SPI不会将移位寄存器中的数据复制到接收缓冲区（SPRF标志不设置为1）。不产生接收缓冲区满中断。即使SPPE位为1，也不会检测到奇偶校验错误。当SPI0处于主模式时，SPI不会更新SPSSR.SPECM[2:0]位。当发生溢出错误并且SPI没有将接收到的数据从移位寄存器复制到接收缓冲区时，在串行传输终止时，SPI确定移位寄存器为空。这使数据能够从发送缓冲器传输到移位寄存器。

(4)如果在OVRF标志为1时读取SPSR后向OVRF标志写入0，则OVRF标志设置为0。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查溢出错误的发生。执行串行传输时，请确保及早检测到溢出错误，例如在读取SPDRSPDR_HA后立即读取SPSR。当SPI处于SPI0的主模式时，可以通过读取SPSSR.SPECM[2:0]位检查发生错误时SPCMDm指针的值。如果发生溢出错误且OVRF标志设置为1，则在OVRF标志设置为0之前无法执行正常接收操作。

在主机模式下启用RSPCK自动停止功能时，不会发生溢出错误。图32.33和
图32.34显示了在主机模式下接收缓冲区已满时串行传输继续时的时钟停止波形。

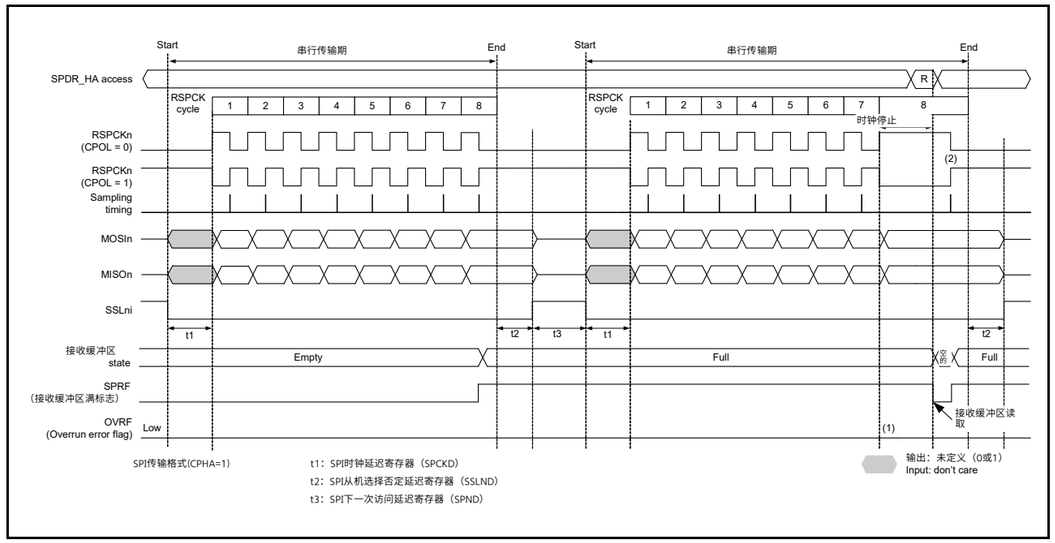


Figure 32.33 在CPHA=1的主模式下，当接收缓冲区已满时串行传输继续时的时钟停止波形

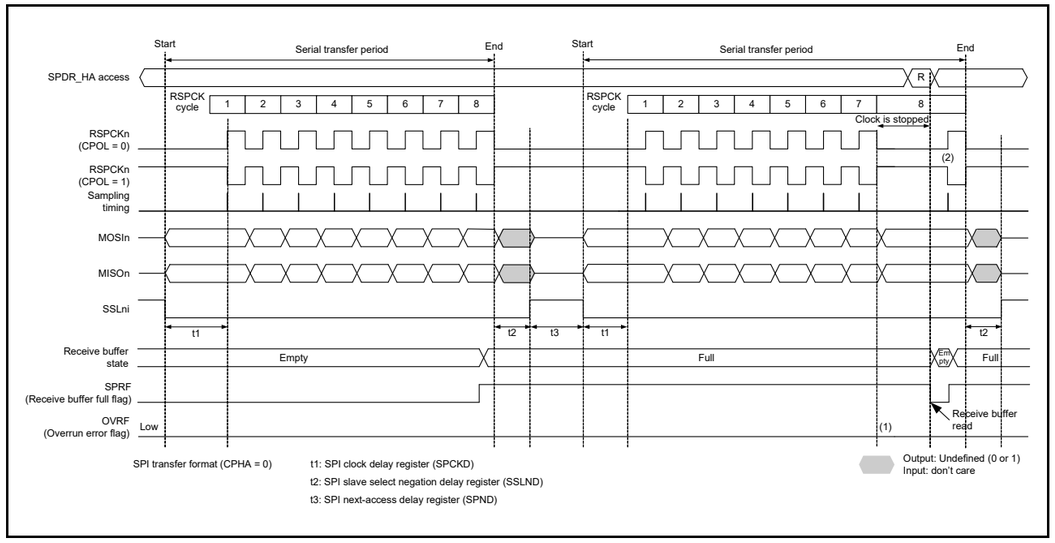


Figure 32.34 Clock stop waveform when serial transfer continues while receive buffer is full in master mode with CPHA = 0

The operation of the flags at the timings shown in (1) and (2) in Figure 32.33 and Figure 32.34 is as follows:

(1) When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.

(2) If SPDR/SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after SPSR.SPRF flag is set to 0).

32.3.8.2 Parity errors

When full-duplex synchronous serial communication is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, the SPI checks for parity errors when serial transfer ends. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 32.35 shows an example operation of OVRF and PERF flags. The SPSR access shown in Figure 32.35 indicates the condition of access to the SPSR register, where W denotes a write cycle, and R a read cycle. In the example in Figure 32.35, full-duplex synchronous serial communication is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

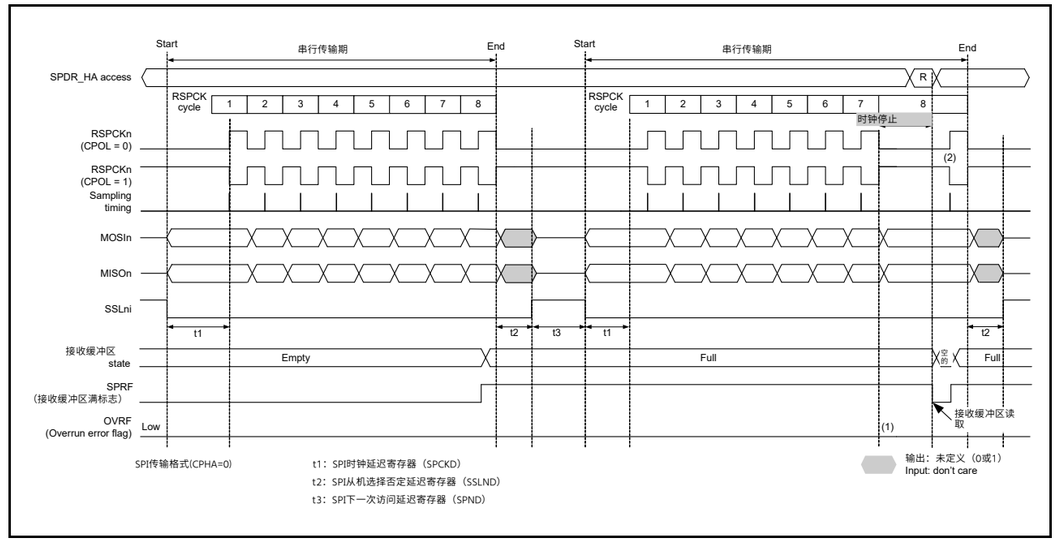


Figure 32.34 在CPHA=0的主模式下，当接收缓冲区已满时串行传输继续时的时钟停止波形

标志在图32.33和图32.34中（1）和（2）所示时序的操作如下：

(1)当接收缓冲器满时，由于RSPCK时钟停止，不会发生溢出错误。

(2)如果在时钟停止时读取SPDRSPDR_HA，则可以读取接收缓冲区中的数据。RSPCK时钟在读取接收缓冲区后重新启动（在SPSR.SPRF标志设置为0之后）。

32.3.8.2 奇偶校验错误

当SPCR.TXMD位设置为0且
SPCR2.SPPE位设置为1，SPI在串行传输结束时检查奇偶校验错误。在检测到接收数据中的奇偶校验错误时，SPI将SPSR.PERF标志设置为1。因为当SPSR.OVRF标志设置为1时，SPI不会将移位寄存器中的数据复制到接收缓冲区，所以奇偶校验错误检测不针对接收到的数据执行。要将PERF标志设置为0，请在读取SPSR寄存器并将PERF标志设置为1后将0写入PERF标志。

图32.35显示了OVRF和PERF标志的示例操作。图32.35所示的SPSR访问表示访问SPSR寄存器的条件，其中W表示写周期，R表示读周期。在图32.35的示例中，当SPCR.TXMD位为0，SPCR2.SPPE位为1时执行全双工同步串行通信。SPI执行8位串行传输，其中SPCMDm.CPHA位为1SPCMDm.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，即传输的位数。

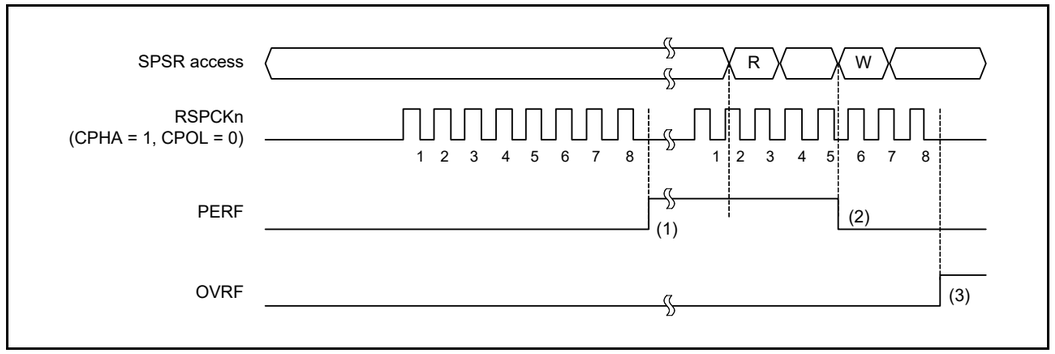


Figure 32.35 Operation example of the OVRF and PERF flags

The operation of the flags at the timing shown in (1) to (3) in Figure 32.35 is as follows:

(1) If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies data in the shift register to the receive buffer. The SPI checks the received data at this timing and sets the PERF flag to 1 if a parity error is detected. In master mode for SPI0, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits.

(2) If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.

(3) When the SPI detects an overrun error and serial transfer is terminated, data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

The occurrence of a parity error can be checked either by reading the SPSR register or by using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, make sure that parity errors are detected early, for instance by reading SPSR errors. When the SPI is in master mode for SPI0, the value of the SPCMDm pointer at the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits.

32.3.8.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If an active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and it sets the SPSR.MODF flag to 1. On detecting the mode fault error for SPI0, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

On detecting a mode fault error, the SPI stops driving of the output signals and clears the SPCR.SPE bit to 0 (see section 32.3.9, Initializing the SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting mode-fault errors without using the SPI error interrupt requires polling of SPSR. When using the SPI in master mode for SPI0, the value of the SPCMDm pointer at the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

32.3.8.4 Underrun errors

When the serial transfer begins with the SPCR.MSTR bit set to 0 (slave mode), the SPCR.SPE bit set to 1, and the transmission data not prepared, the SPI detects an underrun error. The SPI then sets the SPSR.MODF and SPSR.UDRF flags to 1.

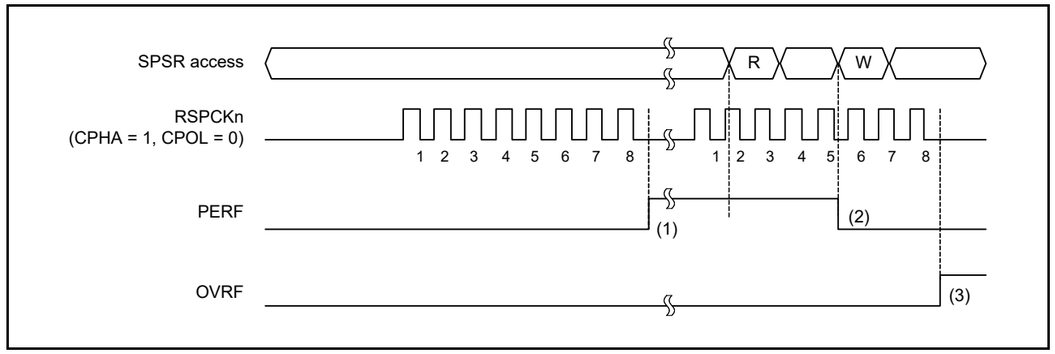


Figure 32.35 OVRF和PERF标志的操作示例

在图32.35中(1)到(3)所示的时序中，标志的操作如下：

(1)如果串行传输因SPI未检测到溢出错误而终止，则SPI将移位寄存器中的数据复制到接收缓冲区。SPI在此时检查接收到的数据，如果检测到奇偶校验错误，则将PERF标志设置为1。在SPI0的主模式下，SPI将SPCMDm指针的值复制到SPSSR.SPECM[2:0]位。

(2)如果在PERF标志为1时读取SPSR寄存器后将0写入PERF标志，则将PERF标志设置为0。

(3)当SPI检测到溢出错误并终止串行传输时，移位寄存器中的数据不会复制到接收缓冲区。此时SPI不执行奇偶校验错误检测。

可以通过读取SPSR寄存器或使用SPI错误中断并读取SPSR寄存器来检查奇偶校验错误的发生。执行串行传输时，请确保尽早检测到奇偶校验错误，例如通过读取SPSR错误。当SPI处于SPI0的主模式时，可以通过读取SPSSR.SPECM[2:0]位检查发生错误时SPCMDm指针的值。

32.3.8.3 模式故障错误

当SPCR.MSTR位为1、SPCR.SPMS位为0且SPCR.MODFEN位为1。如果在多主模式下为SPI的SSLn0输入信号输入有效电平，则无论串行传输的状态如何，SPI都会检测到模式故障错误，并设置SPSR.MODF标志为1。在检测到SPI0的模式故障错误时，SPI将SPCMDm指针的值复制到SPSSR.SPECM[2:0]位。SSLn0信号的有效电平由SSLP.SSL0P位决定。

当MSTR位为0时，SPI工作在从机模式。如果从机模式下SPI的MODFEN位为1，SPMS位为0，并且在串行传输期间（从驱动有效数据开始开始到获取最终有效数据的时间）。

在检测到模式故障错误时，SPI停止驱动输出信号并将SPCR.SPE位清除为0（请参见第32.3.9节，初始化SPI）。对于多主机配置，检测到模式故障错误用于停止驱动输出信号和SPI功能，从而释放主机。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查模式故障错误的发生。在不使用SPI错误中断的情况下检测模式错误需要轮询SPSR。当在主模式下使用SPI用于SPI0时，可以通过读取SPSSR.SPECM[2:0]位来检查发生错误时SPCMDm指针的值。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到模式故障错误后启用SPI功能，MODF标志必须设置为0。

32.3.8.4 Underrun errors

当串行传输开始时SPCR.MSTR位设置为0（从模式），SPCR.SPE位设置为1，并且未准备好传输数据，SPI检测到欠载错误。然后SPI将SPSR.MODF和SPSR.UDRF标志设置为1。

On detecting an underrun error, the SPI stops driving the output signals and clears the SPCR.SPE bit to 0 (see section 32.3.9, Initializing the SPI).

The occurrence of an underrun error can be checked either by reading the SPSR register or by using an SPI error interrupt and reading the SPSR register. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, set the MODF flag to 0.

32.3.9 Initializing the SPI

If 0 is written to the SPCR.SPE bit or if the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset is generated, the SPI initializes all of the module functions. The following section describes initialization by clearing of the SPCR.SPE bit and by a system reset.

32.3.9.1 Initialization by clearing the SPE bit

When the SPCR.SPE bit is set to 0, the SPI initializes by:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the SPI
- Initializing the transmit buffer of the SPI (SPSR.SPTEF flag is set to 1).

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use before initialization when the SPE bit is set to 1 again.

The SPRF, OVRF, MODF, PERF, and UDRF flags in the SPSR register are not initialized. The SPI Sequence Status Register (SPSSR) is not initialized for SPI0. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (SPSR.SPTEF flag is set to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit simultaneously while writing 0 to the SPE bit.

32.3.9.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all bits that control the SPI, the status bits, and the data registers, in addition to the requirements described in section 32.3.9.1, Initialization by clearing the SPE bit.

32.3.10 SPI Operation

32.3.10.1 Master mode operation

The only difference between single-master mode and multi-master mode operation is the use of mode fault error detection (see section 32.3.8, Error Detection). In single-master mode, the SPI does not detect mode fault errors whereas in multi-master mode, it does. This section explains operations that are common to both modes.

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) with the SPI transmit buffer empty, and data for the next transfer is not set (SPSR.SPTEF flag is 1). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA for SPI0, and the shift register is empty for SPI1, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SSLP register settings. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

检测到欠载错误时，SPI停止驱动输出信号并将SPCR.SPE位清除为0（请参见第32.3.9节，初始化SPI）。

可以通过读取SPSR寄存器或使用SPI错误中断并读取SPSR寄存器来检查欠载错误的发生。在不使用SPI错误中断的情况下检测欠载错误需要轮询SPSR。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到欠载错误后启用SPI功能，请将MODF标志设置为0。

32.3.9 初始化SPI

如果将0写入SPCR.SPE位，或者如果SPI由于检测到模式故障错误或欠载错误而将SPE位设置为0，则SPI将禁用SPI功能并初始化一些模块功能。当产生系统复位时，SPI初始化所有模块功能。以下部分描述了通过清除SPCR.SPE位和系统复位进行的初始化。

32.3.9.1 通过清除SPE位进行初始化

当SPCR.SPE位设置为0时，SPI通过以下方式初始化：

- 暂停正在执行的任何串行传输
- 在从模式下停止驱动输出信号(Hi-Z)
- 初始化SPI的内部状态
- 初始化SPI的发送缓冲区（SPSR.SPTEF标志设置为1）。

通过清除SPE位进行的初始化不会初始化SPI的控制位。因此，当SPE位再次设置为1时，SPI可以在初始化之前使用的相同传输模式启动。

SPSR寄存器中的SPRF、OVRF、MODF、PERF和UDRF标志未初始化。SPI序列状态
寄存器(SPSSR)未为SPI0初始化。因此，即使在SPI初始化之后，也可以从接收缓冲区读取数据以检查SPI传输期间的错误状态。

发送缓冲区初始化为空状态（SPSR.SPTEF标志设置为1）。因此，如果SPCR.SPTIE位在SPI初始化后设置为1，则会产生发送缓冲区空中断。要在SPI初始化时禁用任何发送缓冲区空中断，请同时将0写入SPTIE位，同时将0写入SPE位。

32.3.9.2 通过系统复位初始化

除了第32.3.9.1节中描述的要求之外，系统复位还通过初始化所有控制SPI的位、状态位和数据寄存器来完全初始化SPI，通过清除SPE位进行初始化。

32.3.10 SPI操作

32.3.10.1 主模式操作

单主机模式和多主机模式操作之间的唯一区别是使用模式故障错误检测（请参阅第32.3.8节，错误检测）。在单主机模式下，SPI不检测模式故障错误，而在多主机模式下，它可以。本节介绍两种模式共有的操作。

(1) 开始串行传输

当SPI发送缓冲区为空且未设置下一次传输的数据（SPSR.SPTEF标志为1）时，将数据写入SPI数据寄存器(SPDR SPDR_HA)时，SPI更新发送缓冲区(SPTX)中的数据。当SPI0的SPDCR.SPFC[1:0]位设置的帧数写入SPDRSPDR_HA后移位寄存器为空，SPI1的移位寄存器为空，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为满，而在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(2) Terminating serial transfer

Regardless of the SPCMDm.CPHA bit setting, the SPI terminates a serial transfer after transmitting an RSPCKn edge associated with the final sampling timing. If free space is available in the receive buffer (SPRX) (SPSR.SPRF = 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

Note: The final sampling timing varies depending on the bit length of the transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit setting. The polarity of the SSLni output pin depends on the SSLP register settings. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(3) Sequence control

(a) SPI0

The transfer format in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

The SPSCR register determines the sequence configuration for serial transfers that the SPI executes in master mode. The following items are set in the SPCMDm register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity/phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

The SPBR register holds some of the bit rate settings such as the SPI clock delay value (SPCKD), the SSL negation delay value (SSLND), and the next-access delay value (SPND).

According to the sequence length that is assigned to the SPSCR register, the SPI makes up a sequence comprised of a part or all of the SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in the SPCMD0 register, and incorporates the SPCMD0 settings into the transfer format at the beginning of a serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command in the sequence, the SPI sets the pointer to SPCMD0 to execute the sequence repeatedly.

(2) 终止串行传输

无论SPMDm.CPHA位设置如何，SPI在发送与最终采样时序相关的RSPCKn边沿后终止串行传输。如果接收缓冲区(SPRX)(SPSR.SPRF=0)中有可用空间，则在串行传输终止时，SPI将数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。

Note: 最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPMDm.SPB[3:0]位设置。SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(3) 顺序控制

(a) SPI0

主机模式下的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器决定。

SPSCR寄存器确定SPI在主模式下执行的串行传输的序列配置。在SPCMDm寄存器中设置以下项目：

- SSLni管脚输出信号值
- MSB- or LSB-first
- 数据长度
- 一些比特率设置
- RSPCK polarity/phase
- 是否要引用SPCKD
- 是否要引用SSLND
- 是否要引用SPND。

SPBR寄存器保存一些比特率设置，例如SPI时钟延迟值(SPCKD)、SSL否定延迟值(SSLND)和下一次访问延迟值(SPND)。

根据分配给SPSCR寄存器的序列长度，SPI组成一个由部分或全部SPMDm寄存器组成的序列。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPSSR.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI将指针加载到SPCMD0寄存器中的命令，并包含

SPMD0设置成串行传输开始时的传输格式。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于序列中最终命令的串行传输后，SPI将指针设置为SPMD0以重复执行序列。

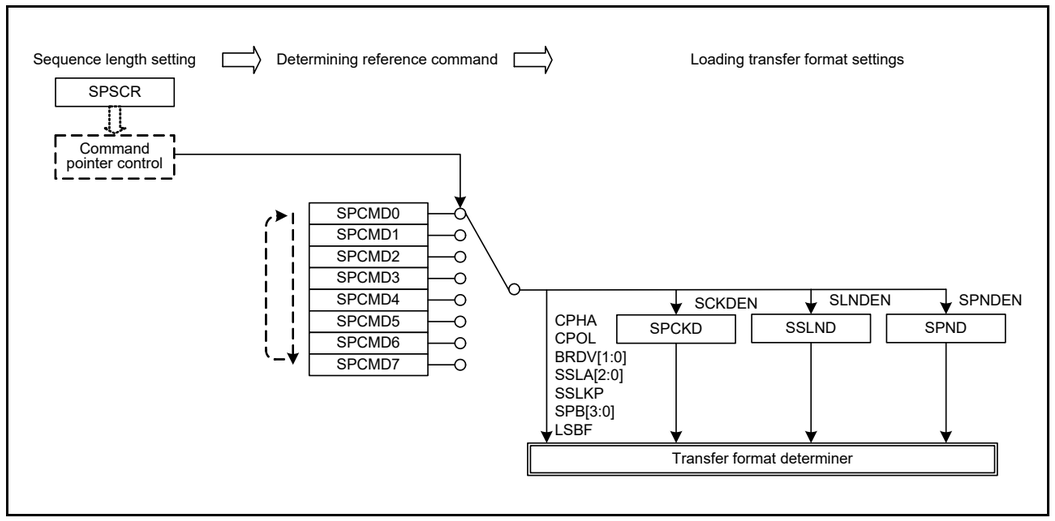


Figure 32.36 Procedure for determining serial transfer format in master mode (SPI0)

In this section, a frame is the combination of the SPDR/SPDR_HA data and the SPCMDm settings.

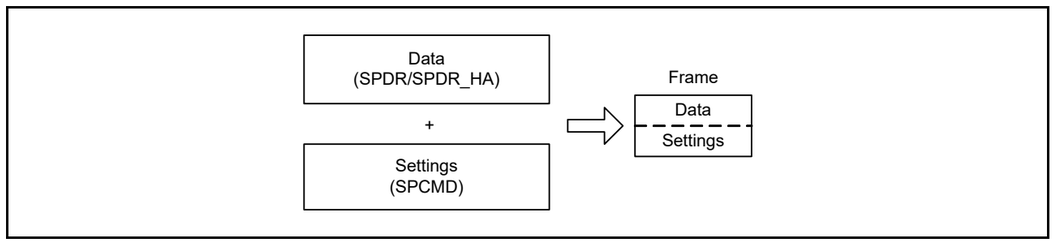


Figure 32.37 Conceptual diagram of frames (SPI0)

Figure 32.38 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 32.4.

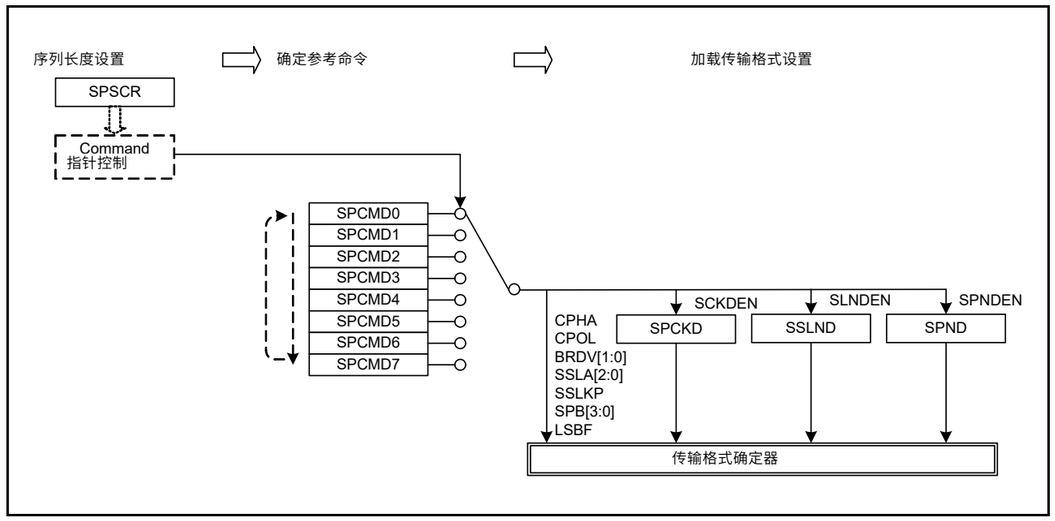


Figure 32.36 确定主机模式下串行传输格式的程序(SPI0)

在本节中，帧是SPDRSPDR_HA数据和SPMDm设置的组合。

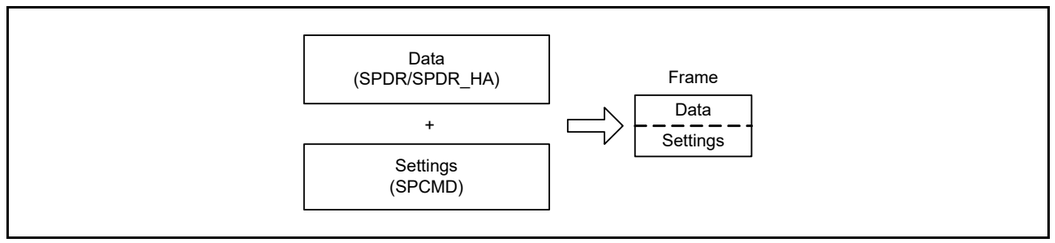


Figure 32.37 帧的概念图（SPI0）

图32.38显示了在表32.4中的设置指定的操作序列中命令与发送和接收缓冲区之间的关系。

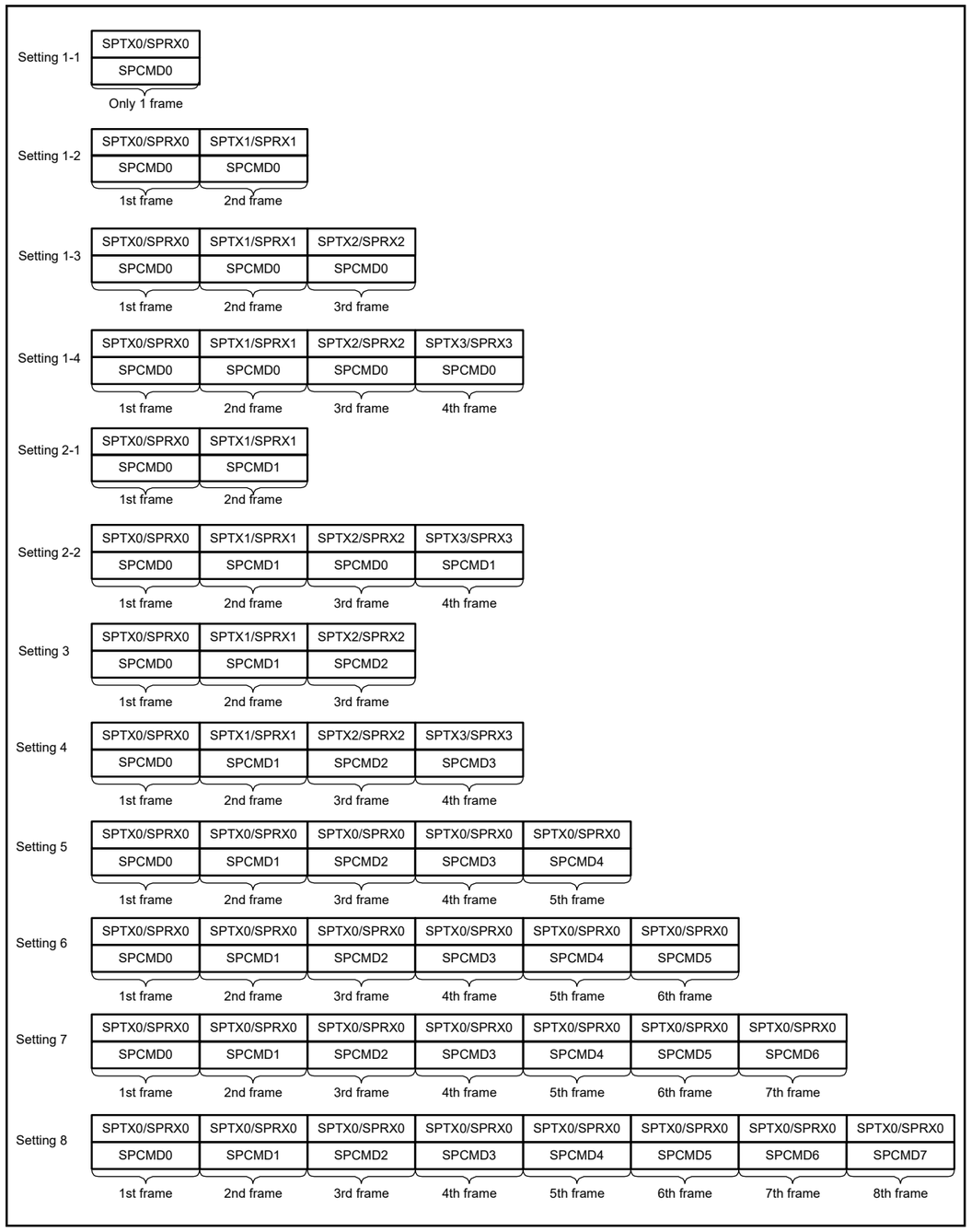


Figure 32.38 Relationship between SPI Command Register (SPCMDm) and transmit and receive buffers in sequence operations (SPI0)

(b) SPI1

The transfer format in master mode is determined by the SPSCR, SPCMD0, SPBR, SPCKD, SSLND, and SPND

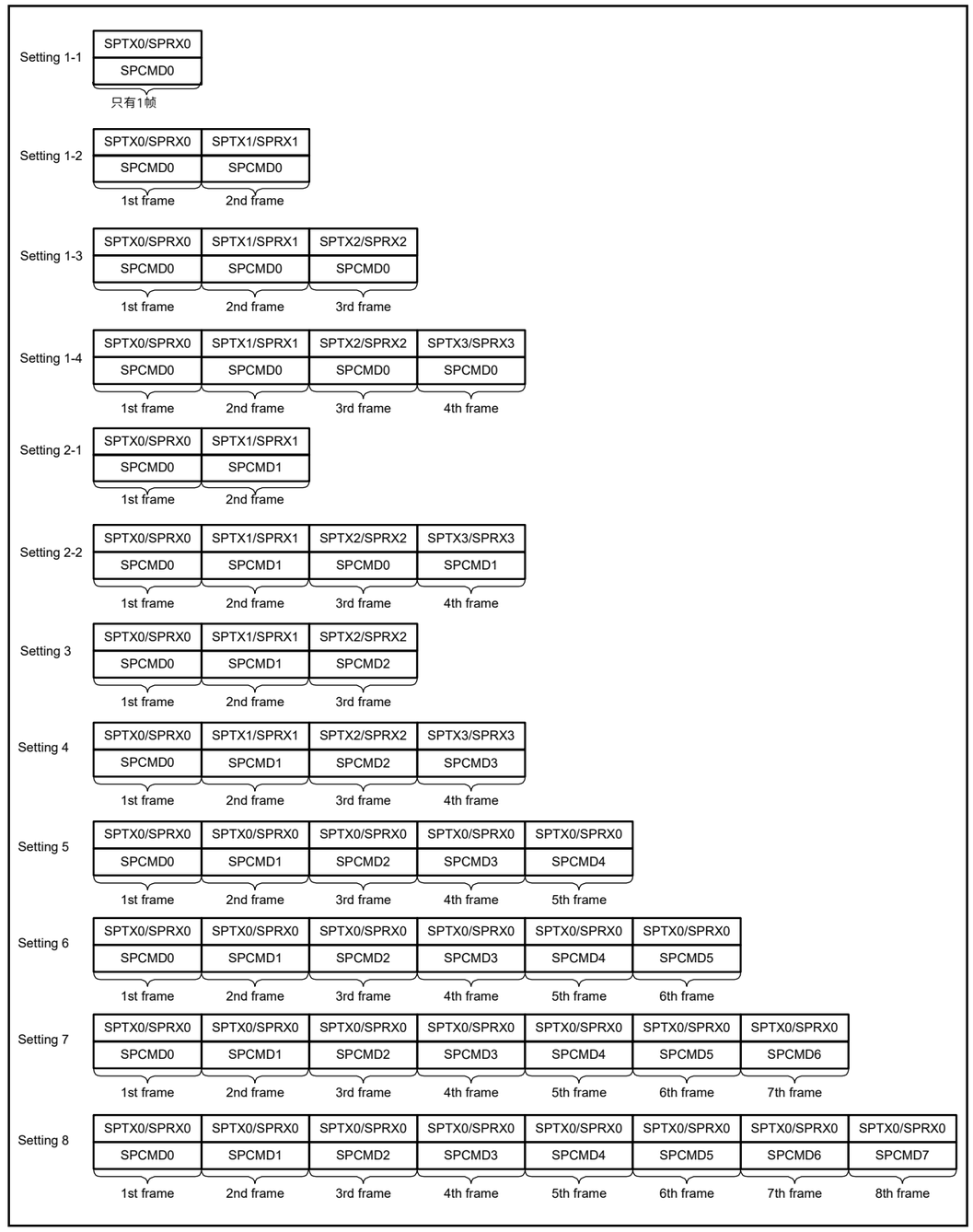


Figure 32.38 SPI命令寄存器(SPCMDm)与顺序操作中的发送和接收缓冲区(SPI0)之间的关系

(b) SPI1

主机模式下的传输格式由SPSCR、SPCMD0、SPBR、SPCKD、SSLND和SPND确定

registers.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following are set in the SPCMD0 register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity/phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

The SPBR register holds some of the bit rate settings such as the SPI clock delay value (SPCKD), the SSL negation delay (SSLND), and the next-access delay value (SPND).

When the SPI function is enabled (SPCR.SPE = 1), the SPI loads the pointer to the commands in SPCMD0 and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer.

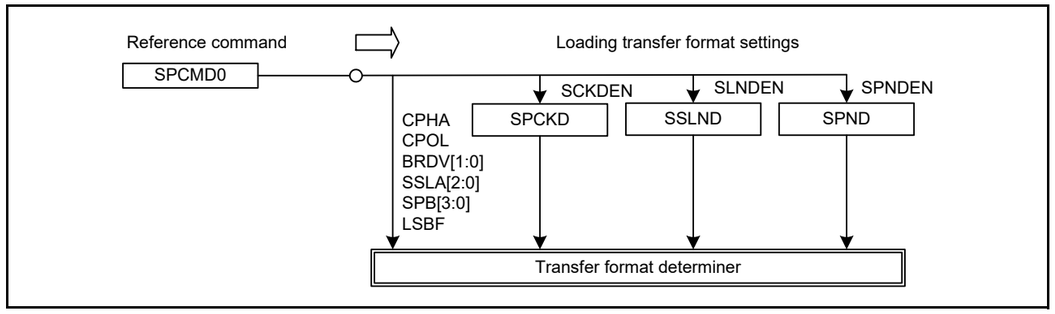


Figure 32.39 Procedure for determining form of serial transfer in master mode (SPI1)

In this section, a frame is the combination of the SPDR/SPDR_HA data and the SPCMD0 settings.

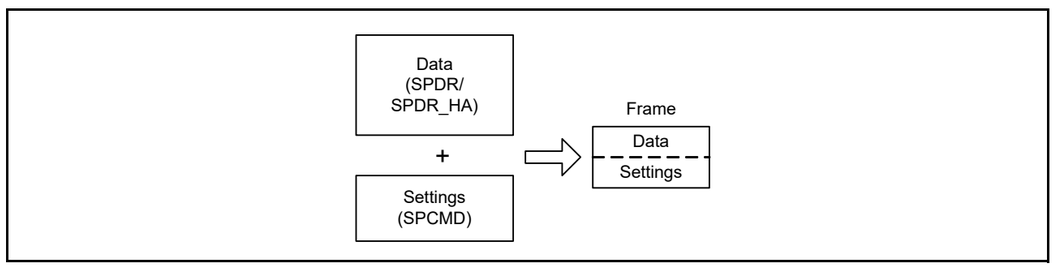


Figure 32.40 Conceptual diagram of frames (SPI1)

Figure 32.41 shows the relationship between the command and the transmit and receive buffers in the sequence of operations.

registers.

SPSCR寄存器确定由SPI在主模式下执行的串行传输的序列配置。在SPMD0寄存器中设置以下内容：

- SSLni管脚输出信号值
- MSB- or LSB-first
- 数据长度
- 一些比特率设置
- RSPCK polarity/phase
- 是否要引用SPCKD
- 是否要引用SSLND
- 是否要引用SPND。

SPBR寄存器保存一些比特率设置，例如SPI时钟延迟值(SPCKD)、SSL否定延迟(SSLND)和下一次访问延迟值(SPND)。

启用SPI功能时（SPCR.SPE=1），SPI加载指向SPCMD0中命令的指针，并在串行传输开始时将SPCMD0设置合并到传输格式中。

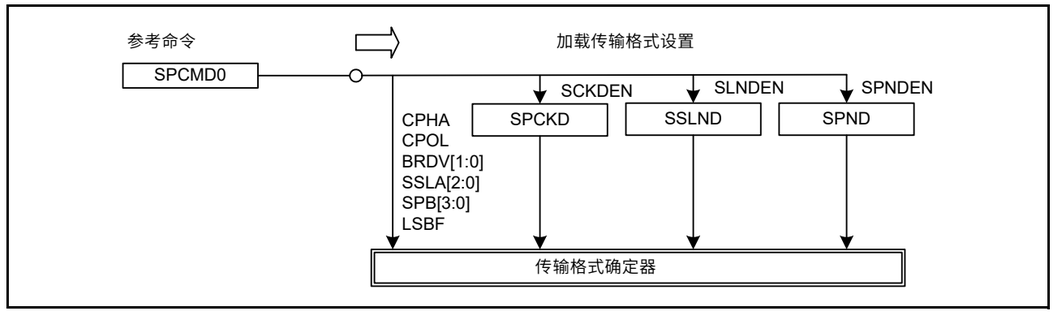


Figure 32.39 确定主模式下串行传输形式的程序(SPI1)

在本节中，帧是SPDRSPDR_HA数据和SPMD0设置的组合。

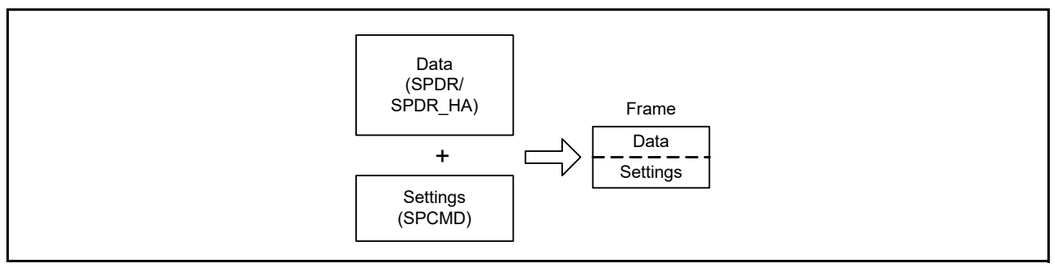


Figure 32.40 帧的概念图（SPI1）

图32.41显示了命令与操作序列中的发送和接收缓冲区之间的关系。

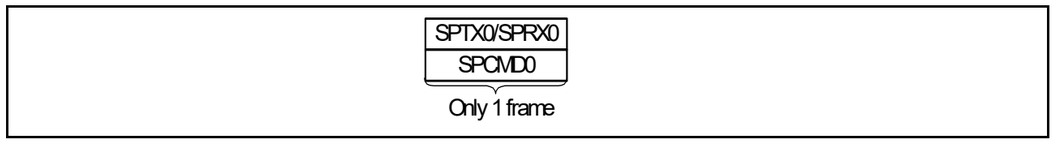


Figure 32.41 Relationship between the SPI Command Register and the transmit and receive buffers in sequence operations (SPI1)

(4) Burst transfer

- SPI0

If the SPCMDm.SSLKP bit that the SPI references during the current serial transfer is 1, the SPI maintains the SSLni signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the SPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

Figure 32.42 shows an example of an SSLni signal operation for a burst transfer that is implemented using the SPCMD0 and SPCMD1 register settings. The following section explains the SPI operations (1) to (7) as shown in Figure 32.42.

Note: The polarity of the SSLni output signal depends on the SSLP register settings.

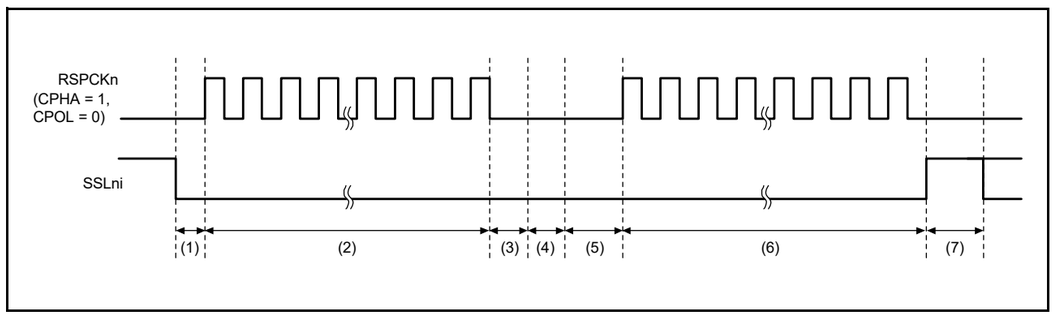


Figure 32.42 Example of burst transfer operation using the SSLKP bit (SPI0)

1. Based on SPCMD0, the SPI asserts the SSLni signal and inserts RSPCK delays.
2. The SPI executes serial transfers according to SPCMD0.
3. The SPI inserts SSL negation delays.
4. Because the SPCMD0.SSLKP bit is 1, the SPI keeps the SSLni signal value on SPCMD0. This period is sustained at a minimum for a period equal to the next-access delay of SPCMD0. If the shift register is empty after the minimum period has passed, this period is sustained until the transmit data is stored in the shift register for the next transfer.
5. Based on SPCMD1, the SPI asserts the SSLni signal and inserts RSPCK delays.
6. The SPI executes serial transfers according to SPCMD1.
7. Because the SPCMD1.SSLKP bit is 0, the SPI negates the SSLni signal. In addition, a next-access delay is inserted according to SPCMD1.

If the SSLni signal output settings in the SPCMDm register, where 1 is assigned to the SSLKP bit, are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the SPI switches the SSLni signal status to SSLni signal assertion as shown in (5) in Figure 32.42. This corresponds to the command for the next transfer.

Note: If such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and collision of signal levels might occur.

In master mode, the SPI references the SSLni signal operation within the module when the SSLKP bit is not used. Even when the SPCMDm.CPHA bit is 0, the SPI can accurately start serial transfers using the SSLni signal assertion for the

Figure 32.41 顺序操作中SPI命令寄存器与发送和接收缓冲区的关系（SPI1）

(4) 突发传输

- SPI0

如果SPI在当前串行传输期间引用的SPCMDm.SSLKP位为1，则SPI在串行传输期间保持SSLni信号电平，直到下一次串行传输的SSLni信号断言开始。如果下一次串行传输的SSLni信号电平与当前串行传输的SSLni信号电平相同，则SPI可以在保持SSLni信号断言状态（突发传输）的同时执行连续串行传输。

图32.42显示了使用SPCMD0和SPCMD1寄存器设置实现的突发传输的SSLni信号操作示例。以下部分解释了SPI操作(1)到(7)，如图32.42所示。

Note: SSLni输出信号的极性取决于SSLP寄存器设置。

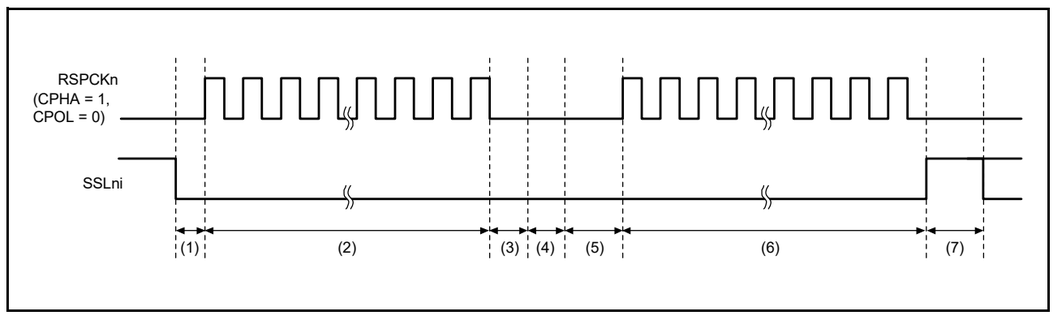


Figure 32.42 使用SSLKP位(SPI0)的突发传输操作示例

1. 基于SPCMD0，SPI断言SSLni信号并插入RSPCK延迟。
2. SPI根据SPMD0执行串行传输。
3. SPI插入SSL否定延迟。
4. 由于SPCMD0.SSLKP位为1，SPI将SSLni信号值保持在SPCMD0上。该周期至少持续等于SPMD0的下一次访问延迟的周期。如果在最小周期过去后移位寄存器为空，则该周期将持续到发送数据存储在移位寄存器中以进行下一次传输。
5. 基于SPCMD1，SPI断言SSLni信号并插入RSPCK延迟。
6. SPI根据SPMD1执行串行传输。
7. 因为SPCMD1.SSLKP位为0，SPI否定SSLni信号。此外，根据SPMD1插入下一个访问延迟。

如果SPCMDm寄存器中的SSLni信号输出设置（其中1分配给SSLKP位）与SPCMDm寄存器中用于下一次传输的SSLni信号输出设置不同，则SPI将SSLni信号状态切换为SSLni信号断言如图32.42中的(5)所示。这对应于下一次传输的命令。

Note: 如果发生这种SSLni信号切换，驱动MISon信号的从机竞争，可能会发生信号电平冲突。

在主机模式下，当SSLKP位未使用时，SPI参考模块内的SSLni信号操作。即使SPCMDm.CPHA位为0，SPI也可以使用SSLni信号断言准确启动串行传输

next transfer that is detected internally.

- SPI1

SPI does not support continuous serial transfer (burst transfer), keeping the SSL signal asserted. However, burst transfer can be implemented by controlling the SSL signal output in general-purpose ports.

(5) RSPCK delay (t1)

The RSPCK delay in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD register setting. For SPI0, the SPI determines the SPCMDm register to be referenced by pointer control during a serial transfer, and determines an RSPCK delay using the SPCMDm.SCKDEN bit and SPCKD, as listed in Table 32.9. For SPI1, the SPI determines an RSPCK delay using the SPCMD0.SCKDEN bit and SPCKD, as listed in Table 32.9. For a definition of RSPCK delay, see section 32.3.5, Transfer Format.

Table 32.9 Relationship between the SCKDEN bit, SPCKD, and RSPCK delay

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL negation delay (t2)

The SSL negation delay in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND register setting. For SPI0, the SPI determines the SPCMDm register to be referenced by pointer control during serial transfer, and determines an SSL negation delay using the SPCMDm.SLNDEN bit and SSLND, as listed in Table 32.10. For SPI1, the SPI determines an SSL negation delay using the SPCMD0.SLNDEN bit and SSLND, as listed in Table 32.10. For a definition of SSL negation delay, see section 32.3.5, Transfer Format.

Table 32.10 Relationship between the SLNDEN bit, SSLND, and SSL negation delay

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

The next-access delay in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND setting. For SPI0, the SPI determines the SPCMDm register to be referenced by pointer control during serial transfer, and determines a next-access delay during serial transfer using the SPCMDm.SPNDEN bit and SPND, as listed in Table 32.11. For SPI1, the SPI determines a next-access delay during serial transfer using the SPCMD0.SPNDEN bit and SPND, as listed in Table 32.11. For a definition of next-access delay, see section 32.3.5, Transfer Format.

内部检测到的下一次传输。

- SPI1

SPI不支持连续串行传输（突发传输），保持SSL信号有效。但是，可以通过控制通用端口中的SSL信号输出来实现突发传输。

(5) RSPCK delay (t1)

主机模式下的RSPCK延迟取决于SPMDm.SCKDEN位设置和SPCKD寄存器设置。对于SPI0，SPI确定串行传输期间指针控制要引用的SPCMDm寄存器，并使用SPCMDm.SCKDEN位和SPCKD确定RSPCK延迟，如表32.9中所列。对于SPI1，SPI使用SPCMD0.SCKDEN位和SPCKD确定RSPCK延迟，如表32.9中所列。有关RSPCK延迟的定义，请参阅第32.3.5节，传输格式。

Table 32.9 SCKDEN位、SPCKD和RSPCK延迟之间的关系

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL否定延迟(t2)

主机模式下的SSL否定延迟取决于SPMDm.SLNDEN位设置和SSLND寄存器设置。对于SPI0，SPI确定串行传输期间指针控制要引用的SPCMDm寄存器，并使用SPCMDm.SLNDEN位和SSLND确定SSL否定延迟，如表32.10中所列。对于SPI1，SPI使用SPCMD0.SLNDEN位和SSLND确定SSL否定延迟，如表32.10中所列。有关SSL否定延迟的定义，请参阅第32.3.5节，传输格式。

Table 32.10 SLNDEN位、SSLND和SSL否定延迟之间的关系

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL否定延迟
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

主机模式下的下一次访问延迟取决于SPMDm.SPNDEN位设置和SPND设置。对于SPI0，SPI确定串行传输期间指针控制要引用的SPCMDm寄存器，并使用SPCMDm.SPNDEN位和SPND确定串行传输期间的下一次访问延迟，如表32.11中所列。对于SPI1，SPI使用SPCMD0.SPNDEN位和SPND确定串行传输期间的下一次访问延迟，如表32.11中所列。有关下一次访问延迟的定义，请参阅第32.3.5节，传输格式。

Table 32.11 Relationship between SPNDEN bit, SPND, and next-access delay

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLK
1	000b	1 RSPCK + 2 PCLK
	001b	2 RSPCK + 2 PCLK
	010b	3 RSPCK + 2 PCLK
	011b	4 RSPCK + 2 PCLK
	100b	5 RSPCK + 2 PCLK
	101b	6 RSPCK + 2 PCLK
	110b	7 RSPCK + 2 PCLK
	111b	8 RSPCK + 2 PCLK

(8) Initialization flow

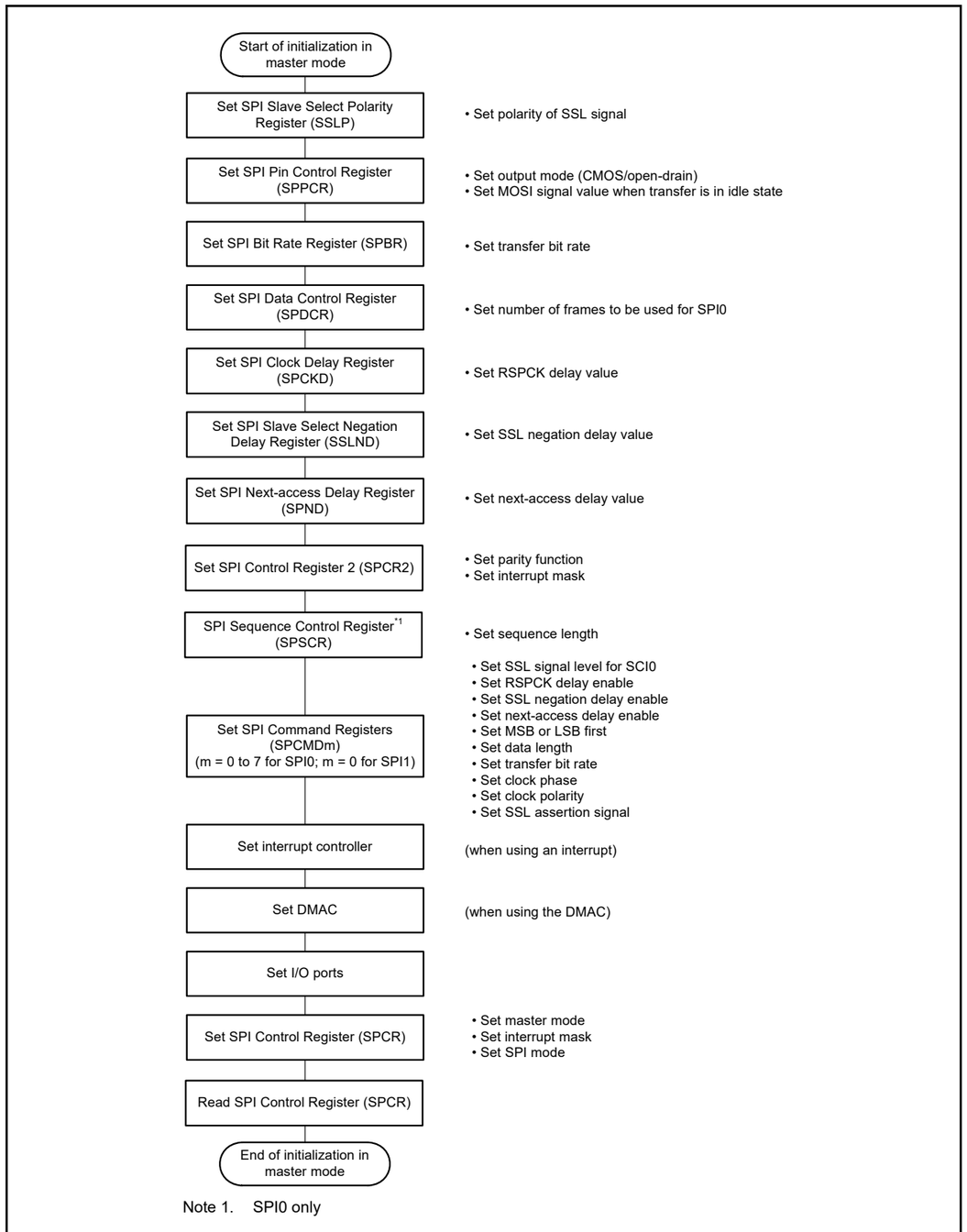
Figure 32.43 shows an example of SPI initialization flow when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit, DMAC, and I/O ports, see the individual block descriptions.

Table 32.11 SPNDEN位、SPND和下一次访问延迟之间的关系

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLK
1	000b	1 RSPCK + 2 PCLK
	001b	2 RSPCK + 2 PCLK
	010b	3 RSPCK + 2 PCLK
	011b	4 RSPCK + 2 PCLK
	100b	5 RSPCK + 2 PCLK
	101b	6 RSPCK + 2 PCLK
	110b	7 RSPCK + 2 PCLK
	111b	8 RSPCK + 2 PCLK

(8) 初始化流程

图32.43显示了SPI处于主机模式时的SPI初始化流程示例。有关如何设置中断控制器单元、DMAC和IO端口的信息，请参见各个模块说明。

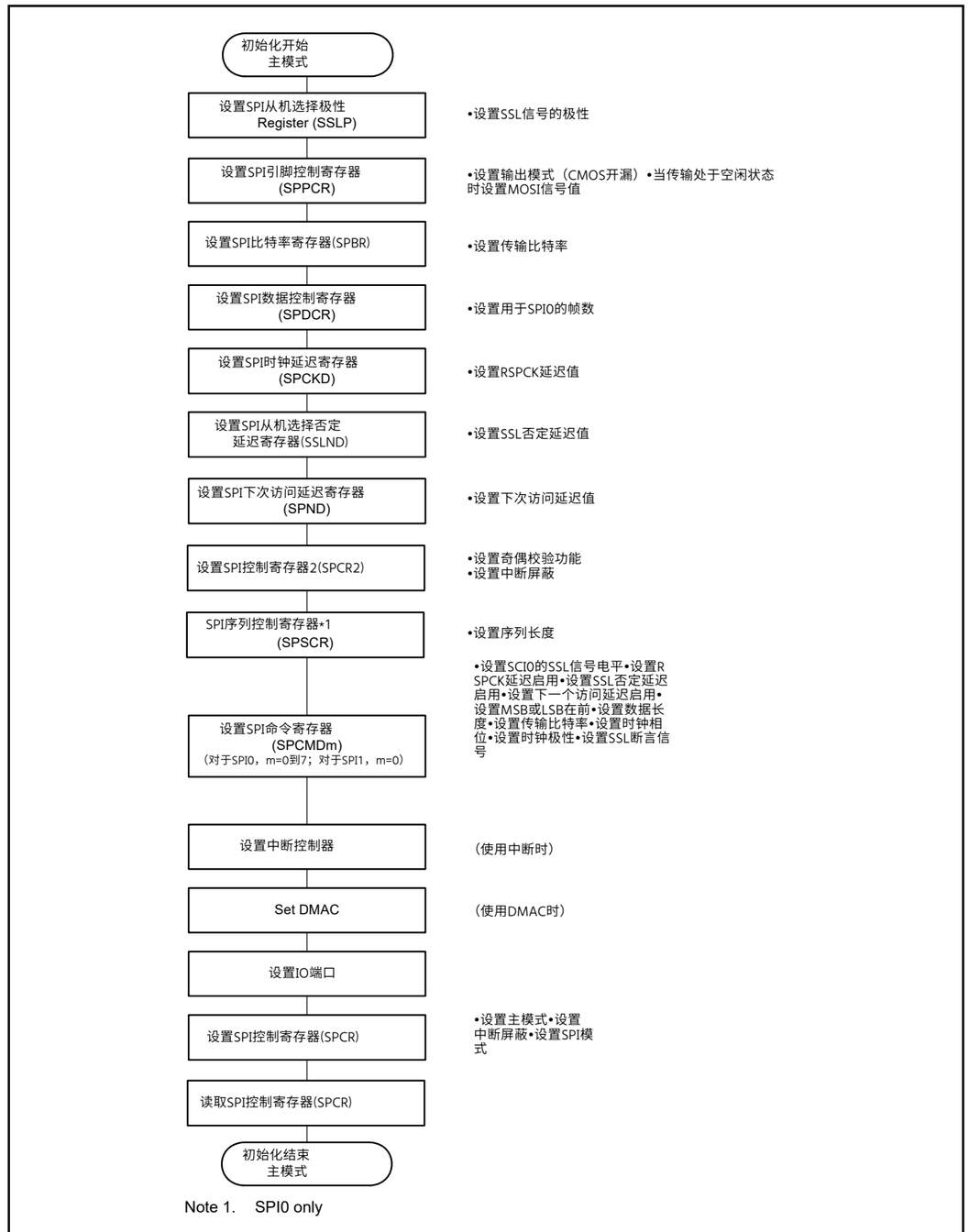


Note 1. SPI0 only

Figure 32.43 Example of initialization flow in master mode for SPI operation

(9) Software processing flow

Figure 32.44 to Figure 32.46 show example flows of software processing.



Note 1. SPI0 only

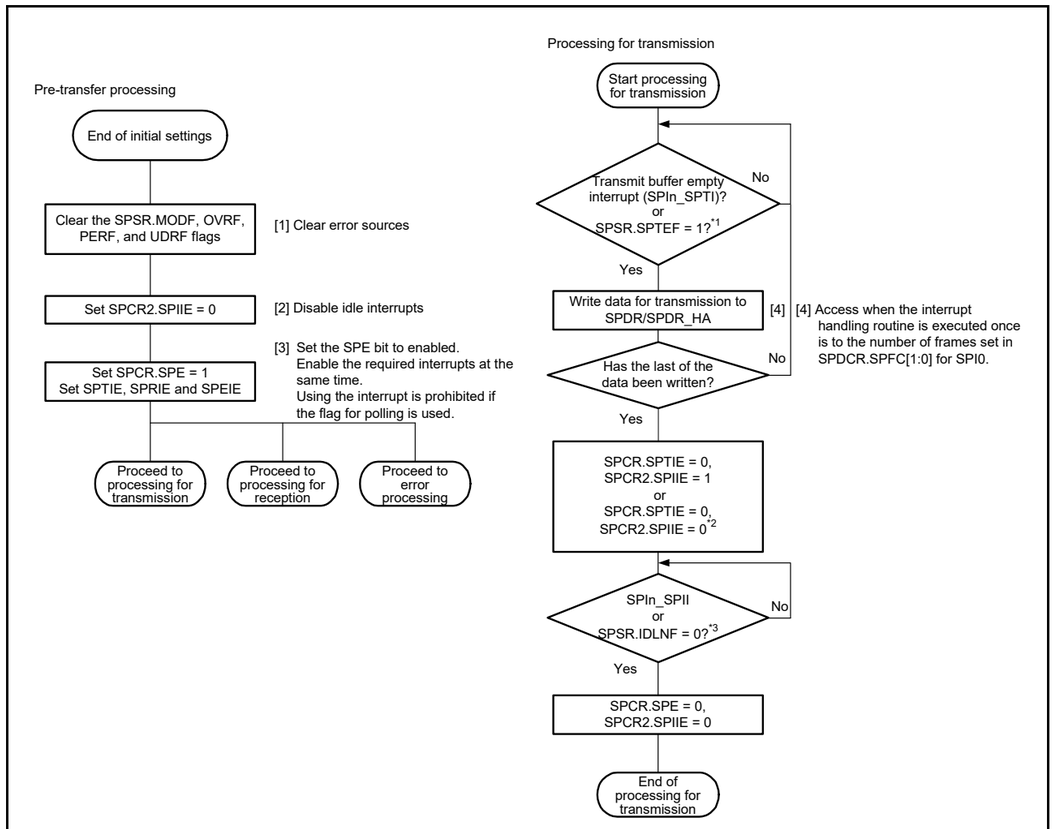
Figure 32.43 SPI操作的主模式初始化流程示例

(9) 软件处理流程

图32.44至图32.46显示了软件处理的示例流程。

(a) Transmit processing flow

When transmitting data and when the SPIn_SPII interrupt is enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.



Note 1. Proceed to writing data for transmission to SPDR/SPDR_HA after checking the transmit buffer empty by reading the SPSR.SPTEF flag if the flag for polling is used.
Note 2. Setting the idle interrupt is prohibited (SPCR2.SPIIE = 0) if the flag for polling is used.
Note 3. Wait more than 1 PCLK after writing data for transmission to SPDE and before starting to poll PSR.IDLNF, if the flag for polling is used.

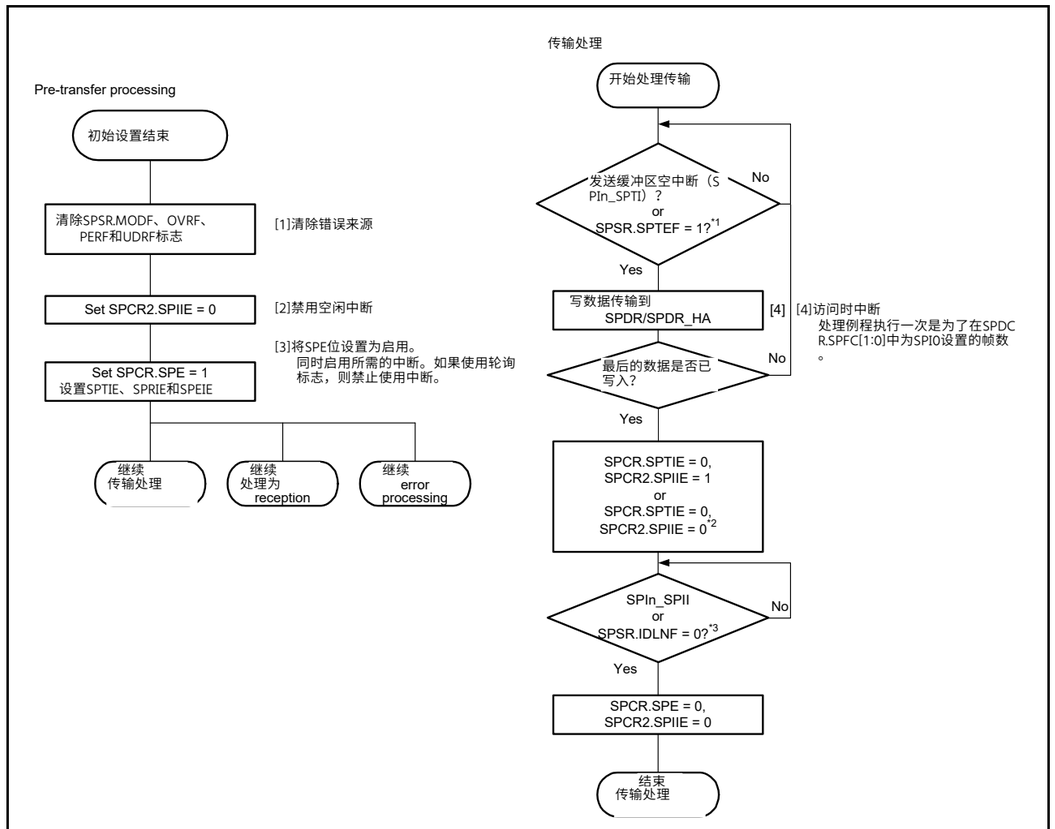
Figure 32.44 Transmission flow in master mode

(b) Receive processing flow

The SPI does not handle receive-only operations, therefore processing for transmission is required.

(a) 传输处理流程

发送数据时，当SPIn_SPII中断使能时，在最后一次数据写入发送后通知CPU数据发送完成。



Note 1. 如果使用轮询标志，则在通过读取SPSR.SPTEF标志检查发送缓冲区为空后，继续将用于发送的数据写入SPDRSPDR_HA。
Note 2. 如果使用轮询标志，则禁止设置空闲中断（SPCR2.SPIIE=0）。
Note 3. 如果使用了轮询标志，则在将数据写入传输到SPDE之后和开始轮询PSR.IDLNF之前等待超过1个PCLK。

Figure 32.44 主模式下的传输流

(b) 接收处理流程

SPI不处理仅接收操作，因此需要处理传输。

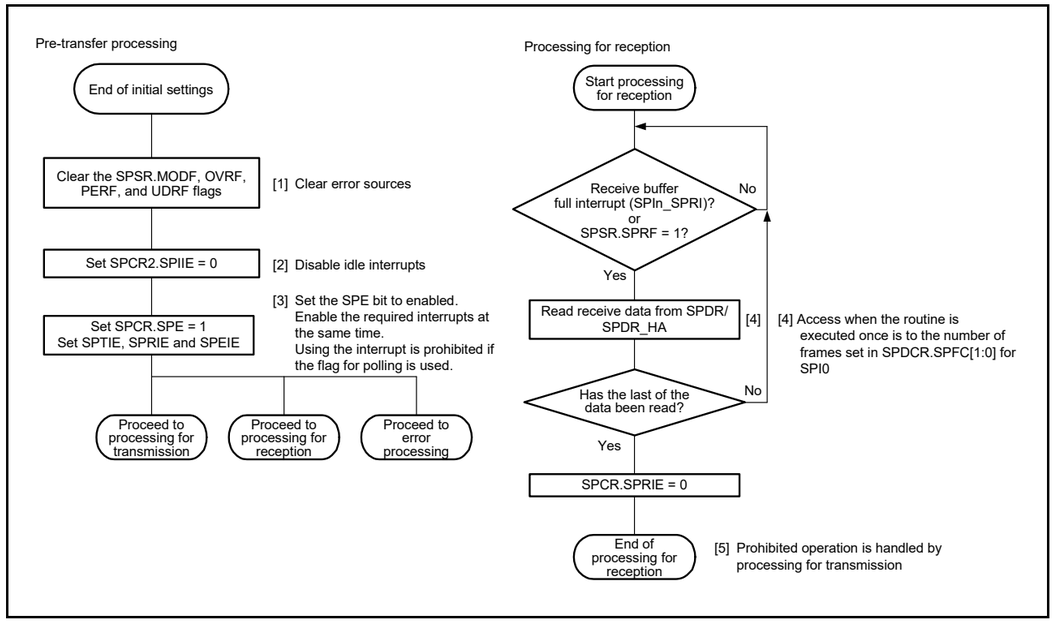


Figure 32.45 Reception flow in master mode

(c) Error processing flow

The SPI detects the following errors:

- Mode fault
- Underrun
- Overrun
- Parity.

When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode-fault errors. Not doing so leads to updating of the SPSSR.SPECM[2:0] bits for SPI0.

When an error is detected using an interrupt, clear the ICU.IELSRj.IR flag in the error processing routine. If this is not done, the ICU.IELSRj.IR flag might continue to indicate a transmit buffer empty or a receive buffer full interrupt request. If an SPIn_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

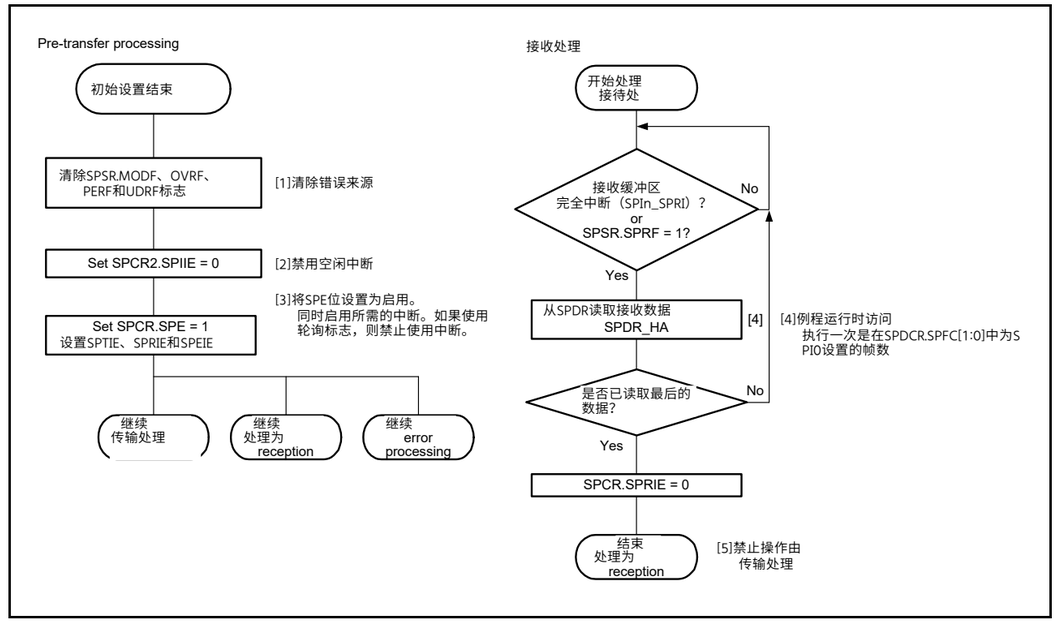


Figure 32.45 主模式下的接收流程

(c) 错误处理流程

SPI检测到以下错误：

- 模式故障
- Underrun
- Overrun
- Parity.

当产生模式故障错误时，SPCR.SPE位自动清零，停止发送和接收操作。对于其他来源的错误，SPCR.SPE位不会被清除，发送和接收操作会继续。Renesas建议清除SPCR.SPE位以停止除模式故障错误以外的错误操作。不这样做会导致更新SPI0的SPSSR.SPECM[2:0]位。

当使用中断检测到错误时，在错误处理例程中清除ICU.IELSRj.IR标志。如果不这样做，ICU.IELSRj.IR标志可能会继续指示发送缓冲区为空或接收缓冲区已满中断请求。如果指示了SPIn_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

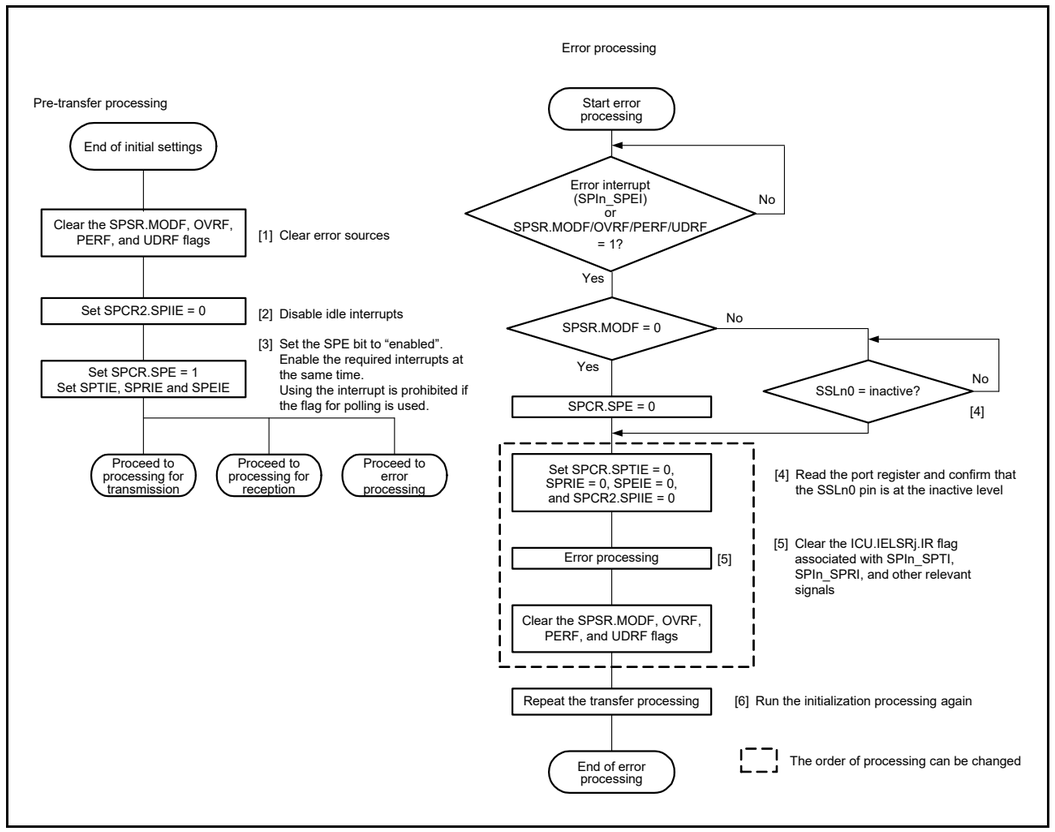


Figure 32.46 Error processing flow in master mode

32.3.10.2 Slave mode operation

(1) Starting serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

The polarity of the SSLn0 input signal depends on the setting of the SSLP.SSL0P bit. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(2) Terminating serial transfer

Regardless of the SPCMD0.CPHA bit, the SPI terminates the serial transfer after detecting an RSPCKn edge associated with the final sampling timing. When free space is available in the receive buffer (SPSR.SPRF = 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of the serial transfer to the end of the serial transfer (see section 32.3.8, Error Detection).

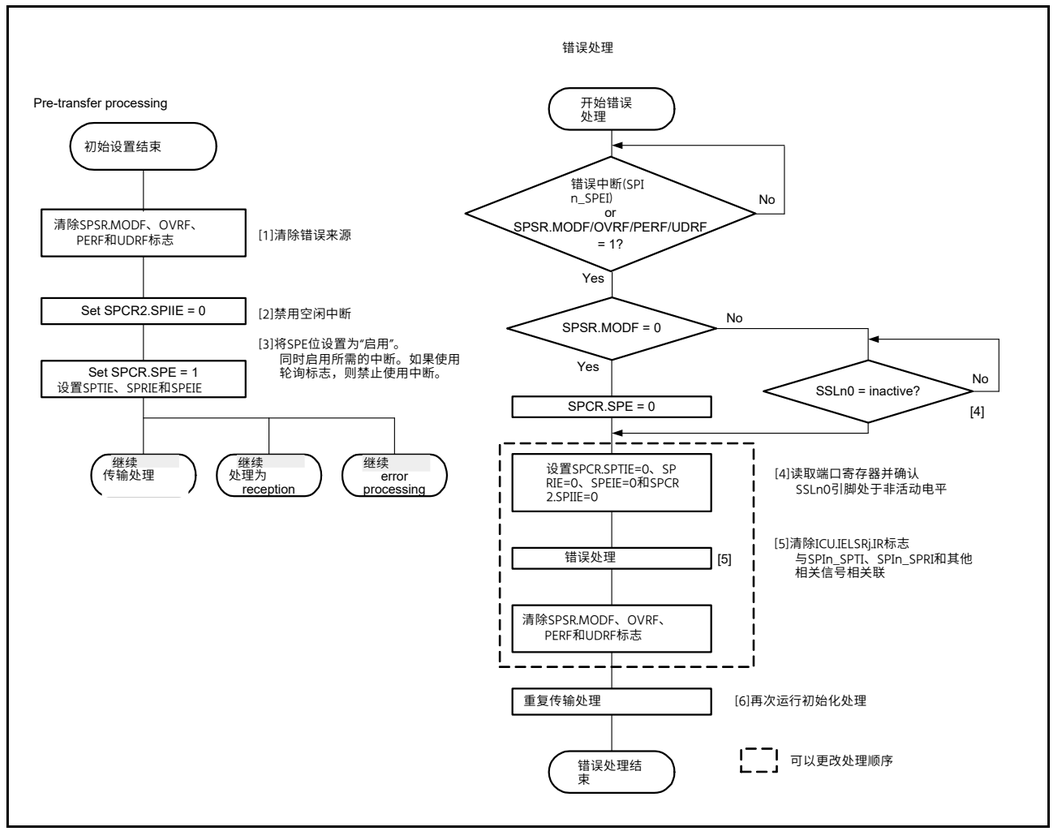


Figure 32.46 主模式下的错误处理流程

32.3.10.2 从模式操作

(1) 开始串行传输

当SPCMD0.CPHA位为0时，如果SPI检测到SSLn0输入信号断言，它必须将有效数据驱动到MISon输出信号。因此，当CPHA位为0时，SSLn0输入信号的断言触发串行传输的开始。

当CPHA位为1时，如果SPI在SSLn0信号置位条件下检测到第一个RSPCKn边沿，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为1时，SSLn0信号断言条件中的第一个RSPCKn边沿触发串行传输的开始。

无论CPHA位设置如何，SPI都会在SSLn0信号置位时驱动MIOn输出信号。SPI输出的数据是有效还是无效，取决于CPHA位设置。

SSLn0输入信号的极性取决于SSLP.SSL0P位的设置。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(2) 终止串行传输

无论SPCMD0.CPHA位如何，SPI在检测到与最终采样时序相关的RSPCKn边沿后都会终止串行传输。当接收缓冲区中有可用空间时（SPSR.SPRF=0），在串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区状态无关。如果SPI从串行传输开始到串行传输结束检测到SSLn0输入信号取反，则会发生模式故障错误（请参阅第32.3.8节，错误检测）。

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(3) Notes on single-slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the configuration example shown in Figure 32.10, if the SPI is in single-slave mode, the SSLn0 signal is fixed at an active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. For the SPI to correctly execute transmit and receive operations in slave mode when the SSLn0 input signal is fixed at an active state, the CPHA bit must be set to 1. If the application requires setting the CPHA bit to 0, the SSLn0 input signal must not be fixed.

(4) Burst transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. If the CPHA bit is 1, the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state corresponds to a serial transfer period. Even when the SSLn0 input signal remains at an active level, the SPI can accommodate burst transfers because it can detect the start of an access.

If the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

Burst transfer cannot be executed for SPI1.

(5) Initialization flow

Figure 32.47 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For information on how to set up the Interrupt Controller Unit, DMAC, and I/O ports, see the individual block descriptions.

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。SSLn0输入信号的极性取决于SSLP.SSL0P位设置。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(3) 单从操作注意事项

如果SPCMD0.CPHA位为0，则SPI在检测到SSLn0输入信号的断言边沿时开始串行传输。
在图32.10所示的配置示例中，如果SPI处于单从模式，则SSLn0信号固定在激活状态。因此，当CPHA位设置为0时，SPI无法正确启动串行传输。为使SPI在SSLn0输入信号固定为有效状态时在从机模式下正确执行发送和接收操作，必须将CPHA位设置为1。如果应用程序需要将CPHA位设置为0，则SSLn0输入信号必须不能固定。

(4) 突发传输

如果SPCMD0.CPHA位为1，则可以执行连续串行传输（突发传输），同时保持SSLn0输入信号的断言状态。如果CPHA位为1，则从第一个RSPCKn边沿到SSLn0信号有效状态下接收最终位的采样定时的周期对应于串行传输周期。即使SSLn0输入信号保持有效电平，SPI也可以适应突发传输，因为它可以检测访问的开始。

如果CPHA位为0，突发传输期间的第二次和后续串行传输将无法正确执行。

SPI1不能执行突发传输。

(5) 初始化流程

图32.47显示了SPI处于从机模式时SPI操作的初始化流程示例。有关如何设置中断控制器单元、DMAC和IO端口的信息，请参见各个模块说明。

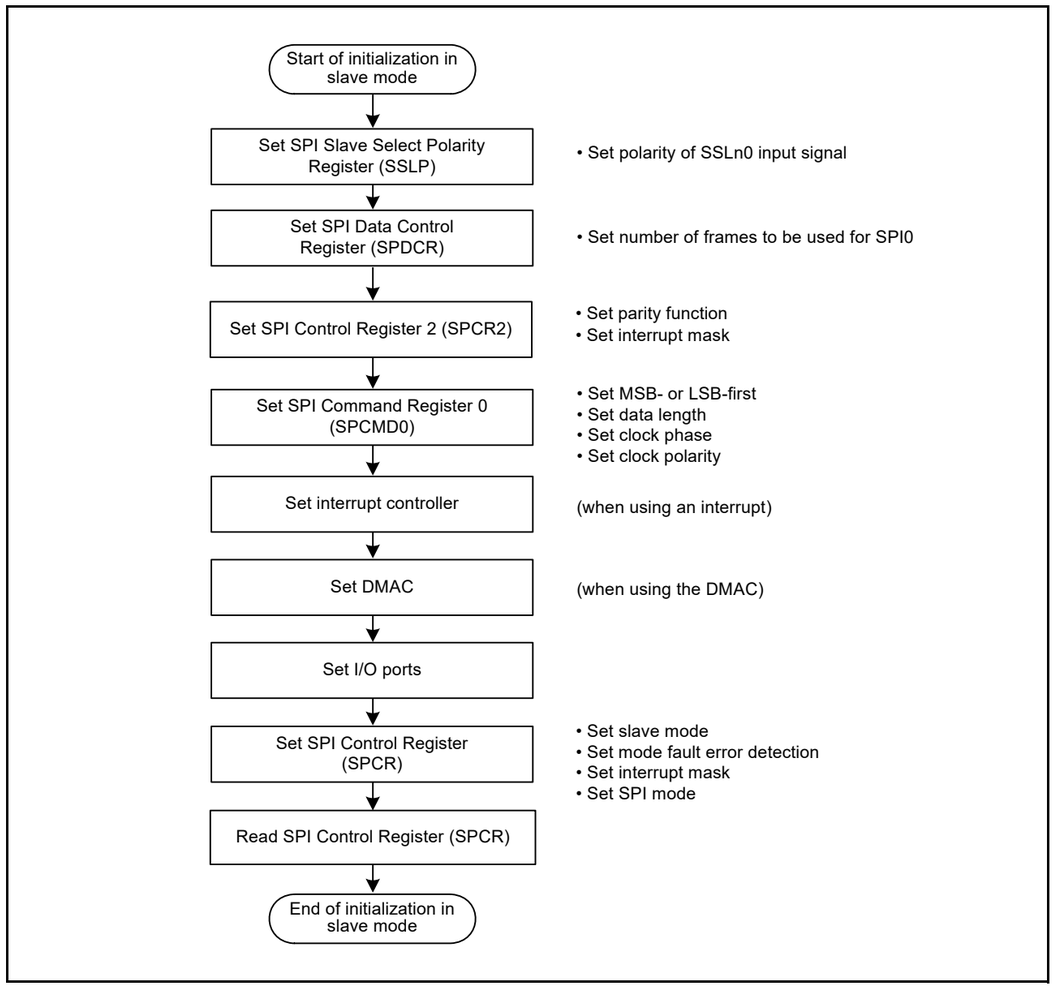


Figure 32.47 Example initialization flow in slave mode for SPI operation

(6) Software processing flow

Figure 32.48 to Figure 32.50 show example flows of software processing.

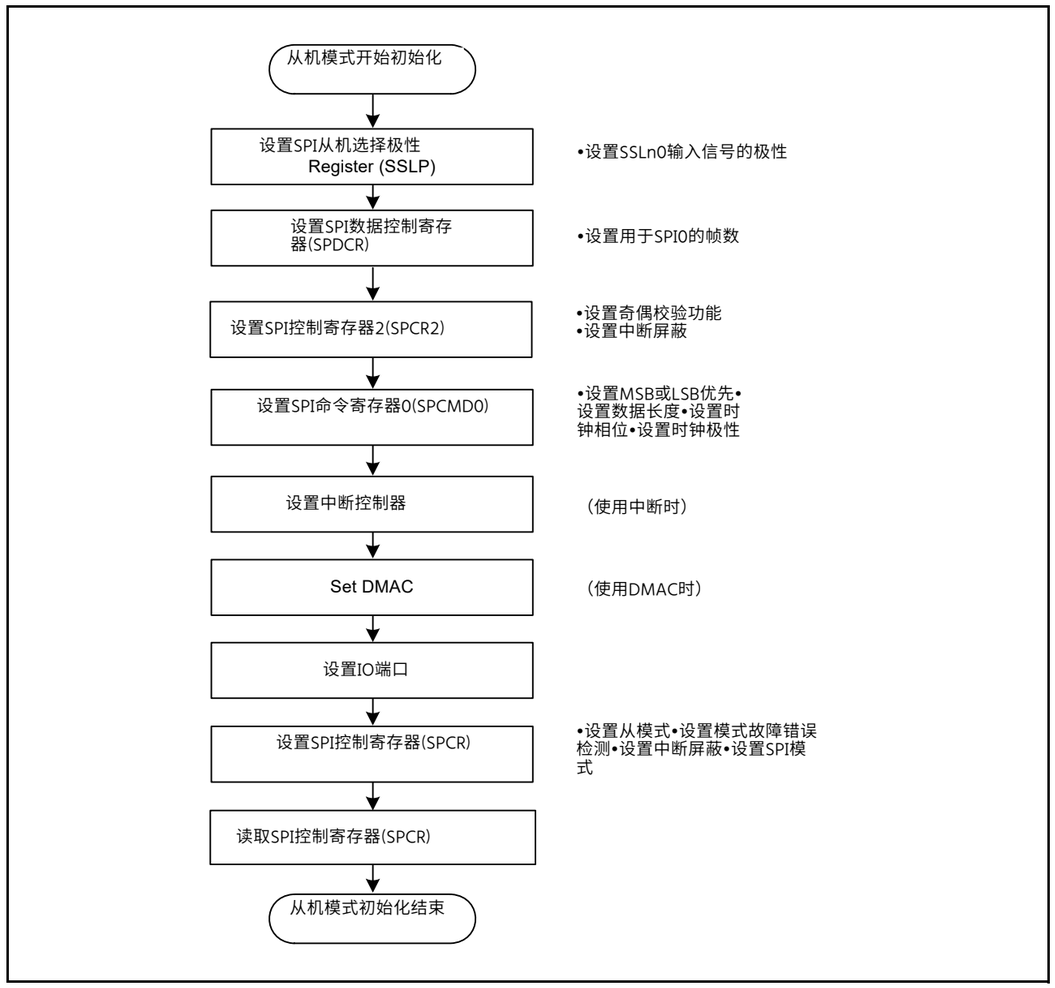
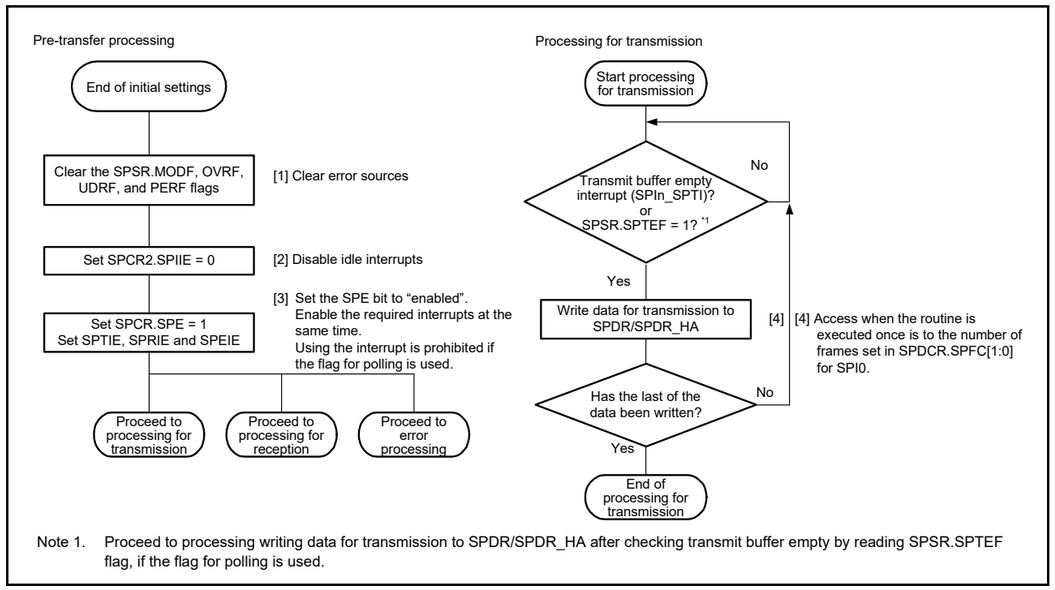


Figure 32.47 SPI操作的从模式初始化流程示例

(6) 软件处理流程

图32.48至图32.50显示了软件处理的示例流程。

(a) Transmit processing flow



Note 1. Proceed to processing writing data for transmission to SPDR/SPDR_HA after checking transmit buffer empty by reading SPSR.SPTEF flag, if the flag for polling is used.

Figure 32.48 Transmission flow in slave mode

(b) Receive processing flow

The SPI does not handle receive-only operation, therefore processing for transmission is required.

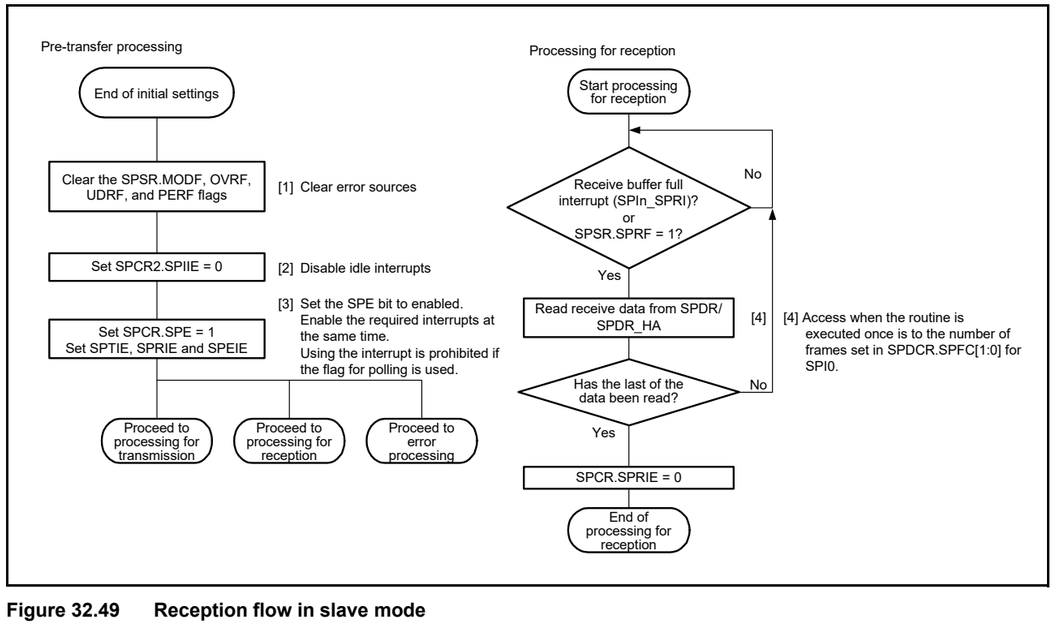
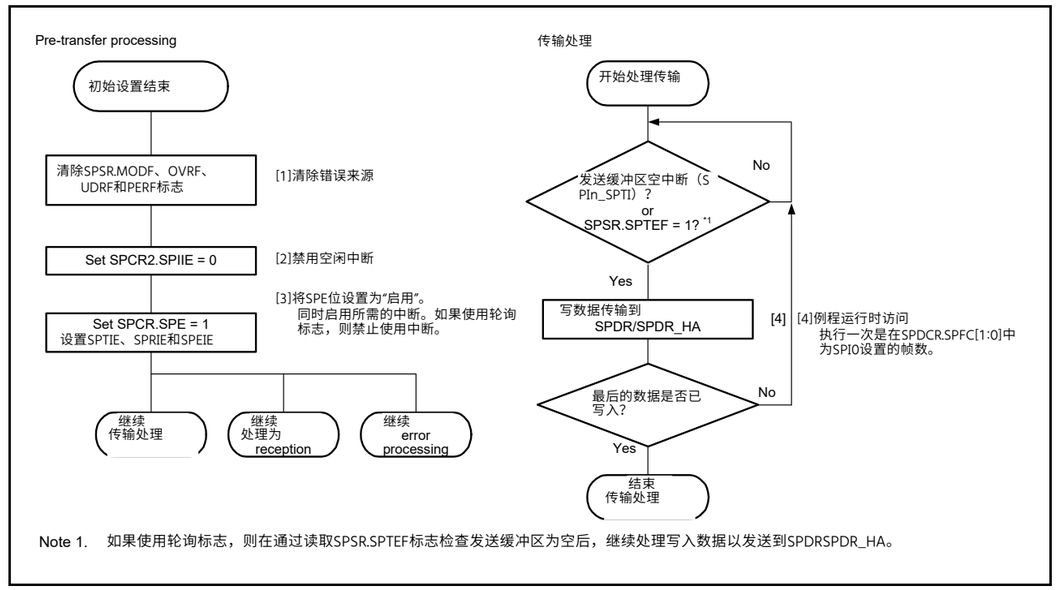


Figure 32.49 Reception flow in slave mode

(a) 传输处理流程



Note 1. 如果使用轮询标志，则在通过读取SPSR.SPTEF标志检查发送缓冲区为空后，继续处理写入数据以发送到SPDRSPDR_HA。

Figure 32.48 从模式下的传输流

(b) 接收处理流程

SPI不处理只接收操作，因此需要处理传输。

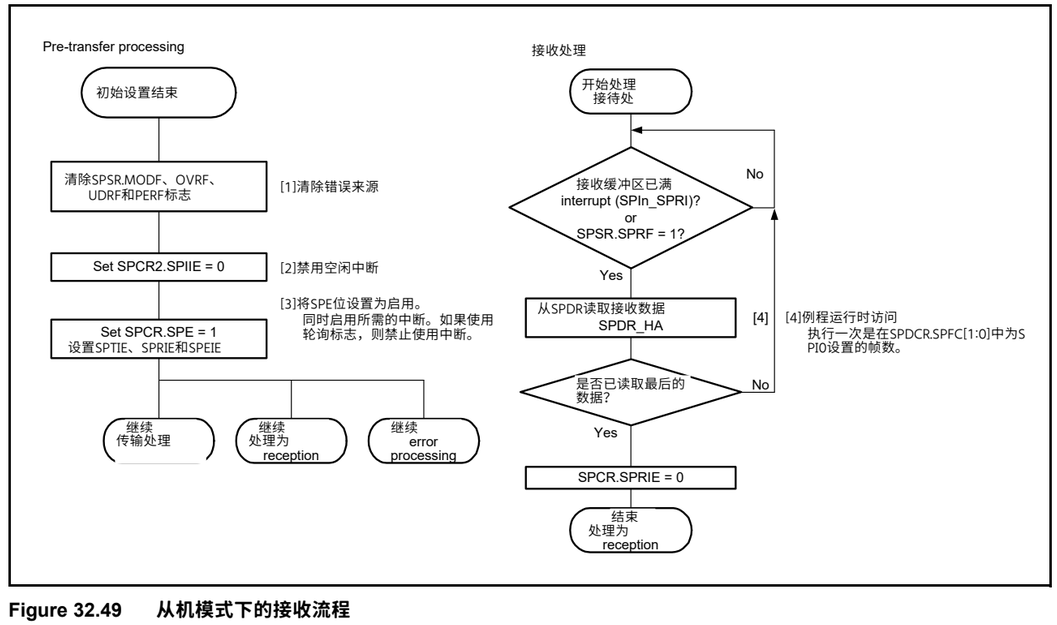


Figure 32.49 从机模式下的接收流程

(c) Error processing flow

In slave operation, even when a mode-fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected using an interrupt, clear the ICU.IELSRj.IR flag in the error processing routine. If this is not done, the ICU.IELSRj.IR flag might continue to indicate a transmit buffer empty or receive buffer full interrupt request. If a receive buffer full request is indicated, read the receive buffer and initialize the sequencer in the SPI.

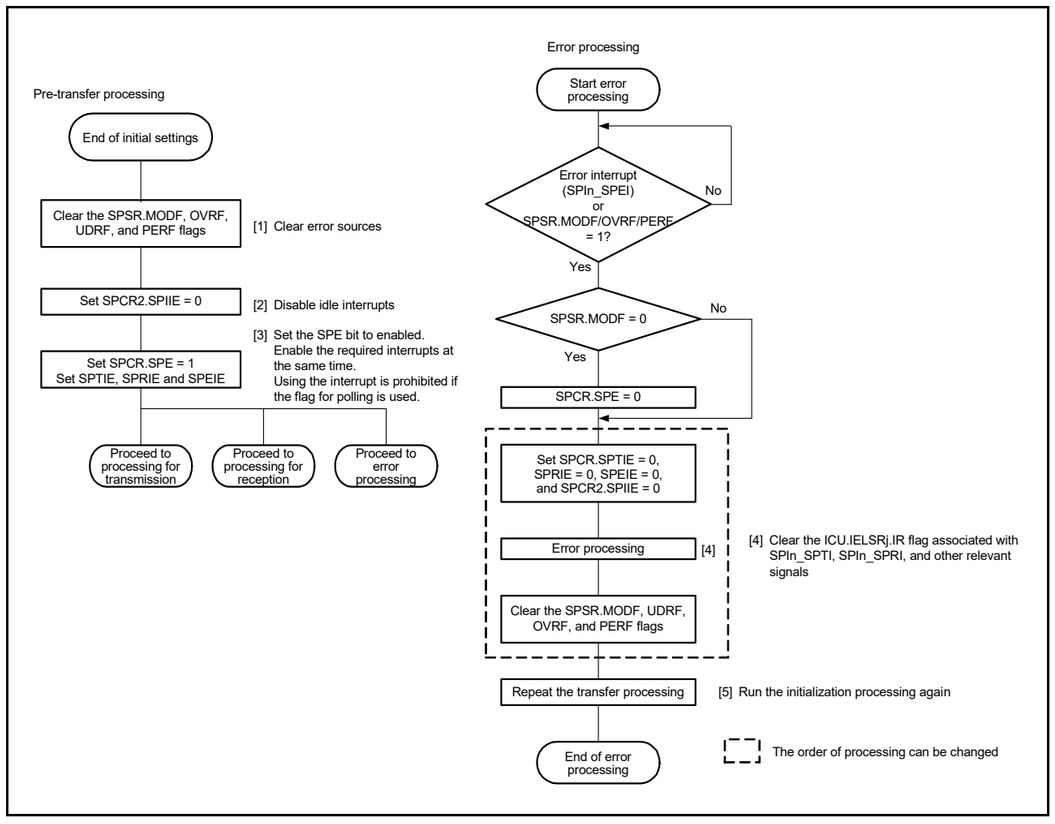


Figure 32.50 Error processing flow for slave mode

32.3.11 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. Each SSLni pin is available as an I/O port pin.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. That is, in both master and slave operations, communications can be performed with the same flow, except that mode fault errors are not detected because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation proceeds when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

32.3.11.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/

(c) 错误处理流程

在从机操作中，即使产生模式故障错误，SPSR.MODF标志也可以被清除，而与SSLn0引脚的状态无关。

当使用中断检测到错误时，在错误处理例程中清除ICU.IELSRj.IR标志。如果不这样做，ICU.IELSRj.IR标志可能会继续指示发送缓冲区为空或接收缓冲区已满中断请求。如果指示接收缓冲区已满请求，则读取接收缓冲区并在SPI中初始化定序器。

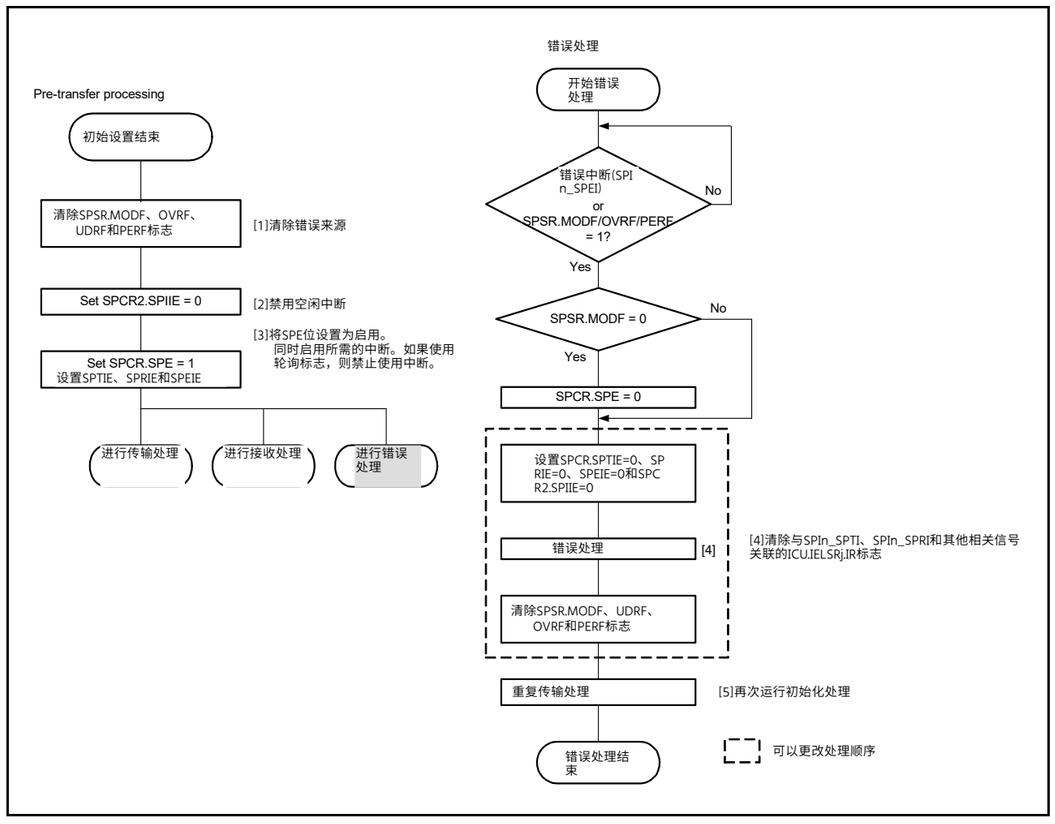


Figure 32.50 从机模式的错误处理流程

32.3.11 时钟同步操作

将SPCR.SPMS位设置为1可选择SPI的时钟同步操作。在时钟同步操作中，
不使用SSLni引脚，而RSPCKn、MOSIn和MISOn引脚处理通信。每个SSLni引脚都可用作IO端口引脚。

虽然时钟同步操作不需要使用SSLni引脚，但模块的操作与SPI操作相同。也就是说，在主机和从机操作中，可以使用相同的流程执行通信，只是由于未使用SSLni引脚而未检测到模式故障错误。

此外，如果在从模式(SPCR.MSTR=0)下SPCMDm.CPHA位设置为0时，时钟同步操作继续进行，则不要执行操作。

32.3.11.1 主模式操作

(1) 开始串行传输

当数据写入SPDR时，SPI会更新SPDRSPDR_HA的发送缓冲区(SPTX)中的数据

SPDR_HA register with the transmit buffer empty, that is, data for the next transfer is not set, and the SPSR.SPTEF flag is 1. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits for SPI0 are written to the SPDR/SPDR_HA, the SPI copies data from the transmission buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge associated with the sampling timing. When free space is available in the receive buffer (SPSR.SPRF = 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI data register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(3) Sequence control

(a) SPI0

The transfer format in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following are set in SPCMDm register:

- SSLni output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCKn polarity/phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

The SPBR register holds some of the bit rate settings such as the SPI clock delay value (SPCKD), the SSL negation delay (SSLND), and the next-access delay value (SPND).

According to the sequence length that is assigned to SPSCR, the SPI makes up a sequence comprised of a part or all of SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command containing the sequence, the SPI sets the pointer to the SPCMD0 register to execute the sequence repeatedly.

SPDR_HA寄存器与发送缓冲区为空，即未设置下一次传输的数据，并且SPSR.SPTEF标志为1。当在SPDCR.SPFC[1:0中设置的帧数后移位寄存器为空时]位SPI0写入SPDRSPDR_HA，SPI将数据从传输缓冲区复制到移位寄存器并开始串行传输。将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为满，而在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(2) 终止串行传输

SPI在发送与采样时序相关的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间(SPSR.SPRF=0)时，串行传输终止时，SPI将数据从移位寄存器复制到SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPMDm.SPB[3:0]位设置。在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(3) 顺序控制

(a) SPI0

主机模式下的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器决定。虽然在时钟同步操作中不输出SSLni信号，但这些设置是有效的。

SPSCR寄存器确定由SPI在主模式下执行的串行传输的序列配置。在SPCMDm寄存器中设置以下内容：

- SSLni输出信号值
- MSB- or LSB-first
- 数据长度
- 一些比特率设置
- RSPCKn polarity/phase
- 是否要引用SPCKD
- 是否要引用SSLND
- 是否要引用SPND。

SPBR寄存器保存一些比特率设置，例如SPI时钟延迟值(SPCKD)、SSL否定延迟(SSLND)和下一次访问延迟值(SPND)。

根据分配给SPSCR的序列长度，SPI组成一个由部分或全部SPMDm寄存器组成的序列。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPSSR.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI将指针加载到SPCMD0寄存器中的命令，并在串行传输开始时将SPCMD0寄存器设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在对应于包含序列的最终命令的串行传输完成后，SPI将指针设置为SPMD0寄存器以重复执行序列。

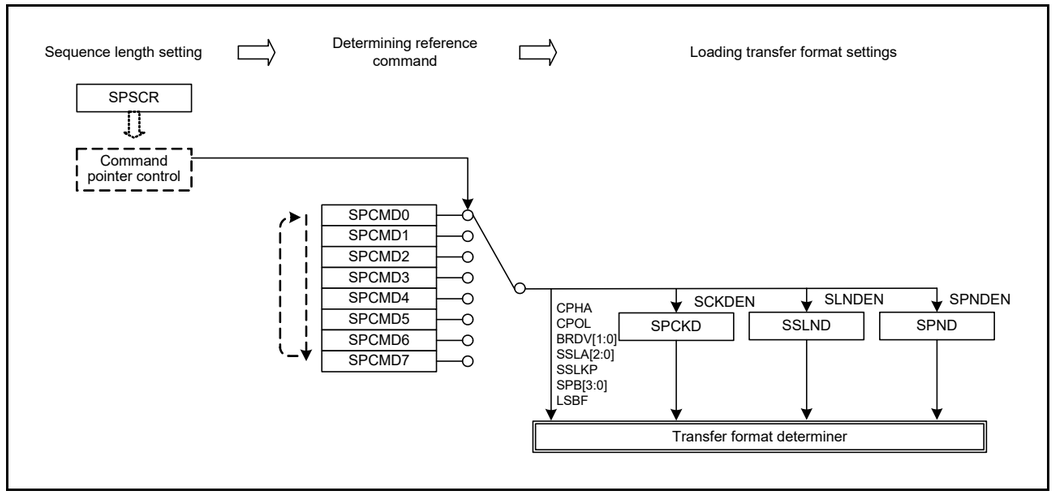


Figure 32.51 Procedure to determine the format of serial transmission in master mode (SPI0)

In this section, a frame is the combination of the SPDR/SPDR_HA data and SPCMDm settings.

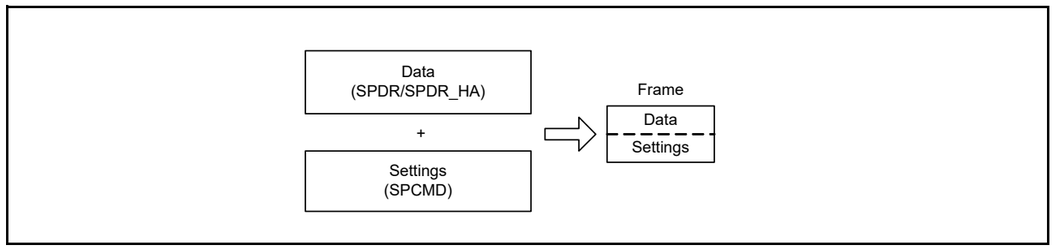


Figure 32.52 Conceptual diagram of frames (SPI0)

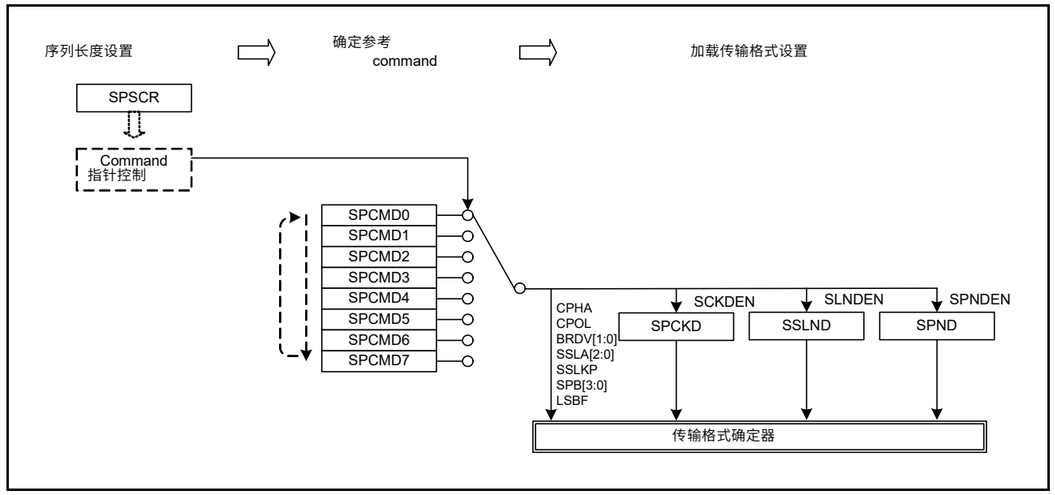


Figure 32.51 确定主机模式下串行传输格式的程序（SPI0）

在本节中，帧是SPDRSPDR_HA数据和SPMDm设置的组合。

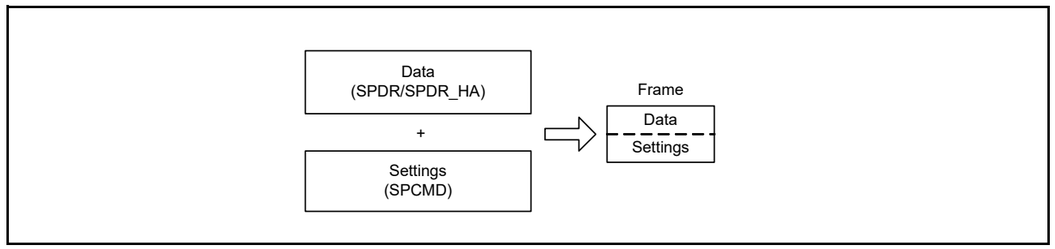


Figure 32.52 帧的概念图（SPI0）

Figure 32.53 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 32.4.

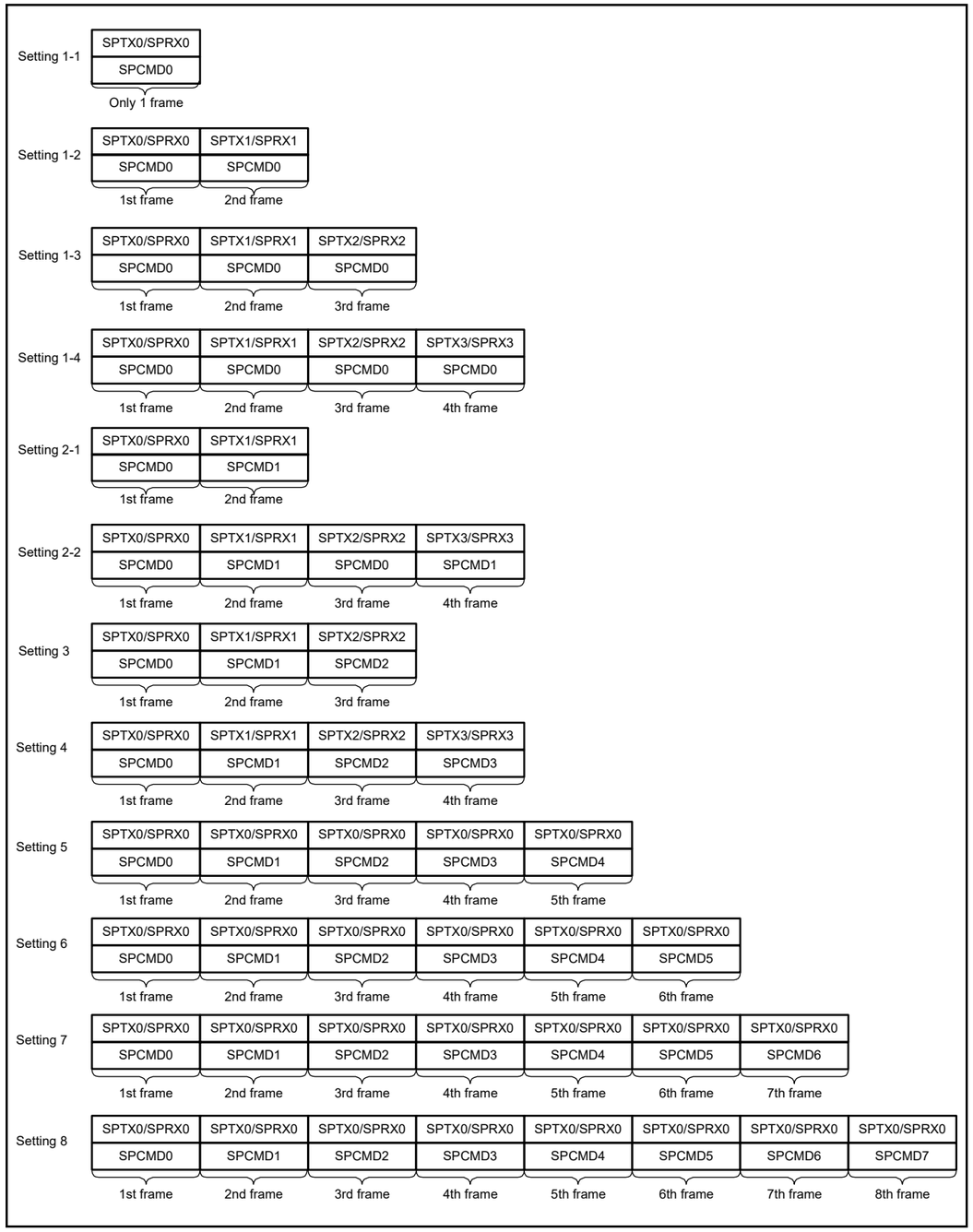


Figure 32.53 Relationship between the SPI Command Register and the transmit and receive buffers in sequence operations (SPI0)

图32.53显示了在表32.4中的设置指定的操作序列中命令与发送和接收缓冲区之间的关系。

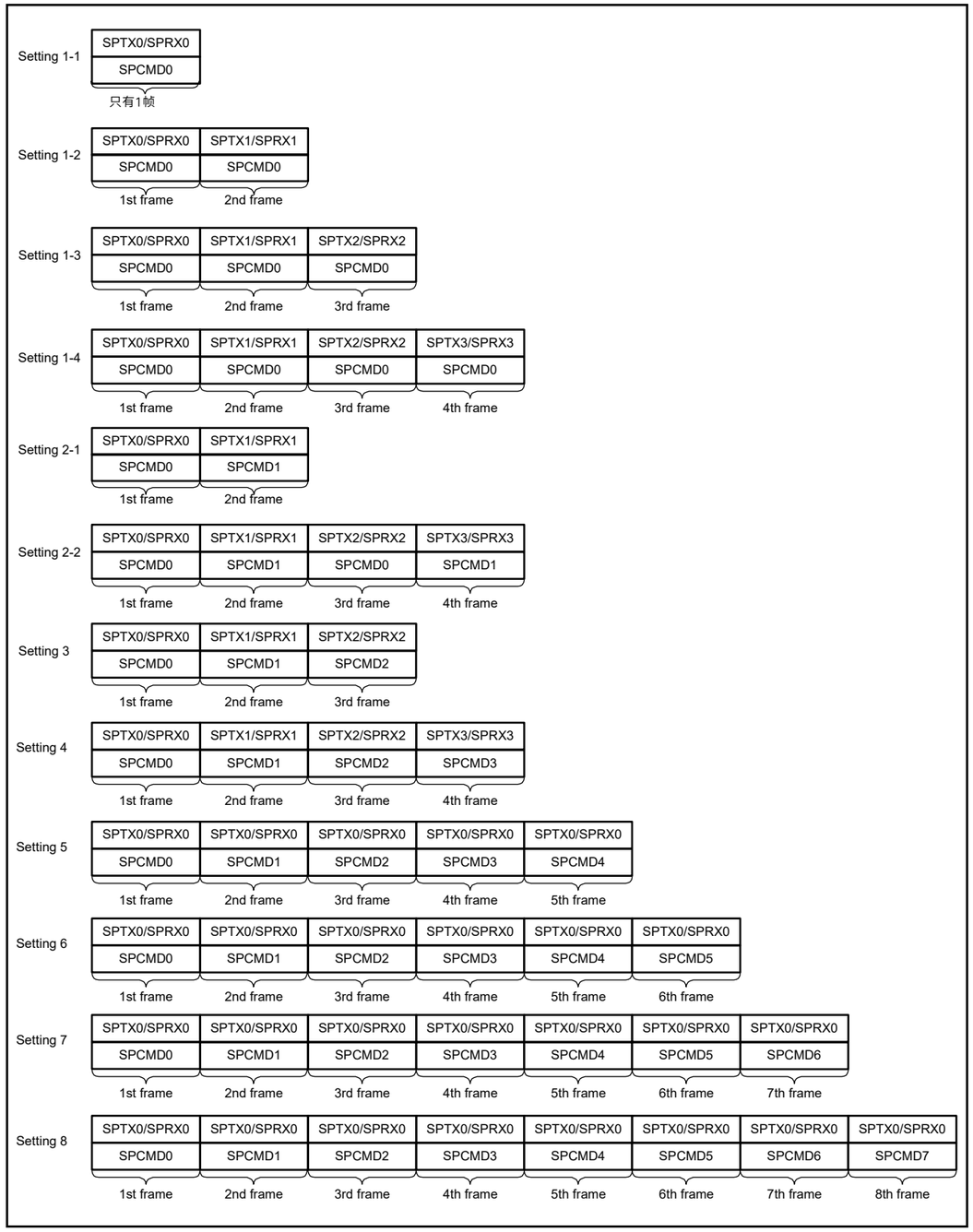


Figure 32.53 顺序操作中SPI命令寄存器与发送和接收缓冲区的关系（SPI0）

(b) SPI1

The transfer format in master mode is determined by the SPCMD0, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The following are set in the SPCMD0 register:

- SSLni output signal value
- MSB-first or LSB-first
- Data length
- Some of the bit rate settings
- RSPCKn polarity/phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

The SPBR register holds some of the bit rate settings such as the SPI clock delay value (SPCKD), the SSL negation delay (SSLND), and the next-access delay value (SPND).

When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer.

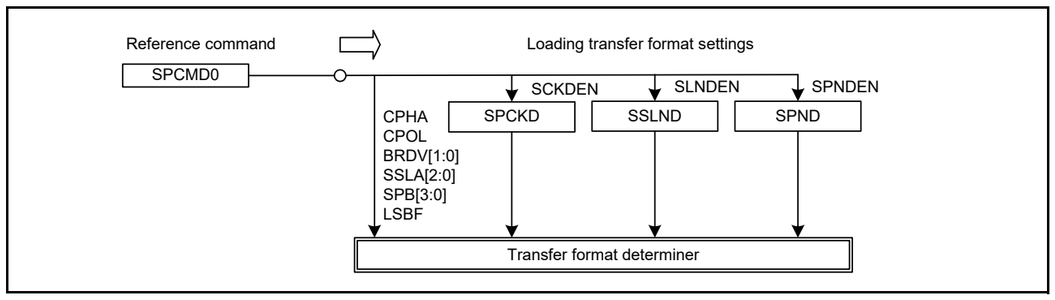


Figure 32.54 Procedure to determine the format of serial transmission in master mode (SPI1)

In this section, a frame is the combination of the SPDR/SPDR_HA data and the SPCMD0 settings.

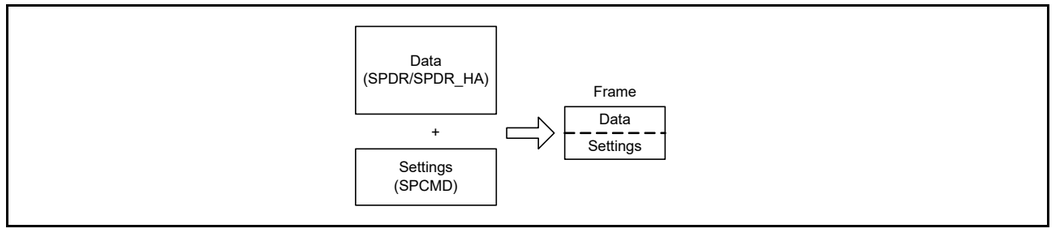


Figure 32.55 Procedure to determine the format of serial transmission in master mode (SPI1)

Figure 32.56 shows the relationship between the command and the transmit and receive buffers in the sequence of operations.

(b) SPI1

主机模式下的传输格式由SPCMD0、SPBR、SPCKD、SSLND和SPND寄存器决定。
虽然在时钟同步操作中不输出SSLni信号，但这些设置是有效的。

在SPMD0寄存器中设置以下内容：

- SSLni输出信号值
- MSB-first or LSB-first
- 数据长度
- 一些比特率设置
- RSPCKn polarity/phase
- 是否要引用SPCKD
- 是否要引用SSLND
- 是否要引用SPND。

SPBR寄存器保存一些比特率设置，例如SPI时钟延迟值(SPCKD)、SSL否定延迟(SSLND)和下一次访问延迟值(SPND)。

当SPCR.SPE位设置为1并启用SPI功能时，SPI加载指向命令的指针
SPCMD0寄存器，并在串行传输开始时将SPCMD0寄存器设置合并到传输格式中。

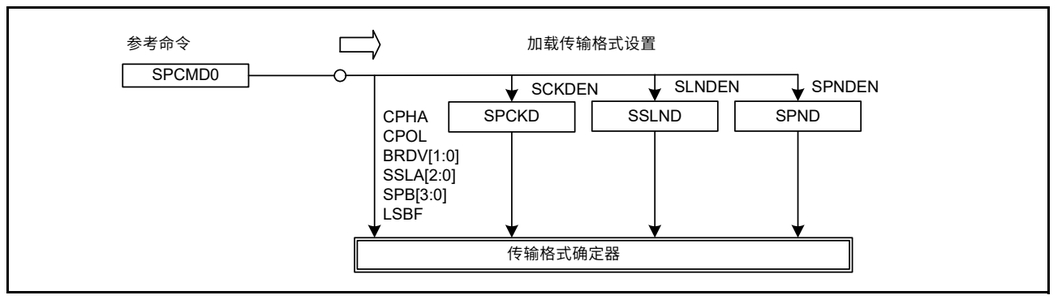


Figure 32.54 确定主机模式下串行传输格式的程序（SPI1）

在本节中，帧是SPDRSPDR_HA数据和SPMD0设置的组合。

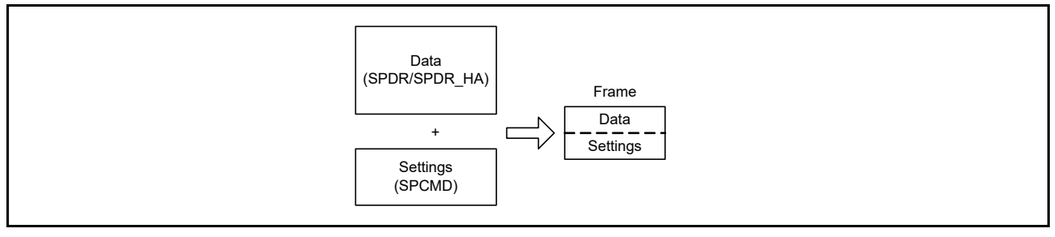


Figure 32.55 确定主机模式下串行传输格式的程序（SPI1）

图32.56显示了命令与操作序列中的发送和接收缓冲区之间的关系。

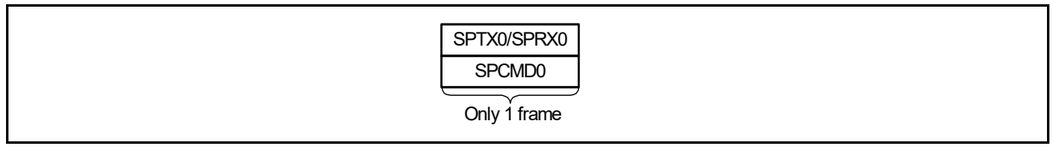


Figure 32.56 Relationship between SPI Command Register and transmit and receive buffers in sequence operations (SPI1)

(4) Initialization flow

Figure 32.57 shows an example of initialization flow for clock synchronous operation when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit, DMAC, and I/O ports, see the individual block descriptions.

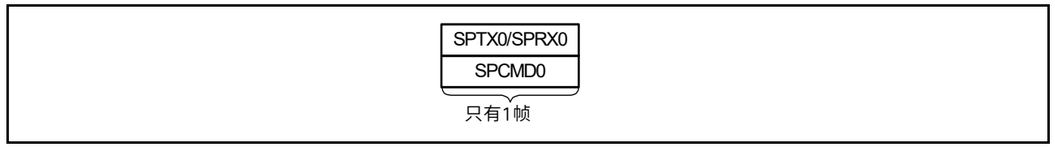


Figure 32.56 顺序操作中SPI命令寄存器与发送和接收缓冲区的关系（SPI1）

(4) 初始化流程

图32.57显示了SPI处于主模式时时钟同步操作的初始化流程示例。
有关如何设置中断控制器单元、DMAC和IO端口的信息，请参见各个模块说明。

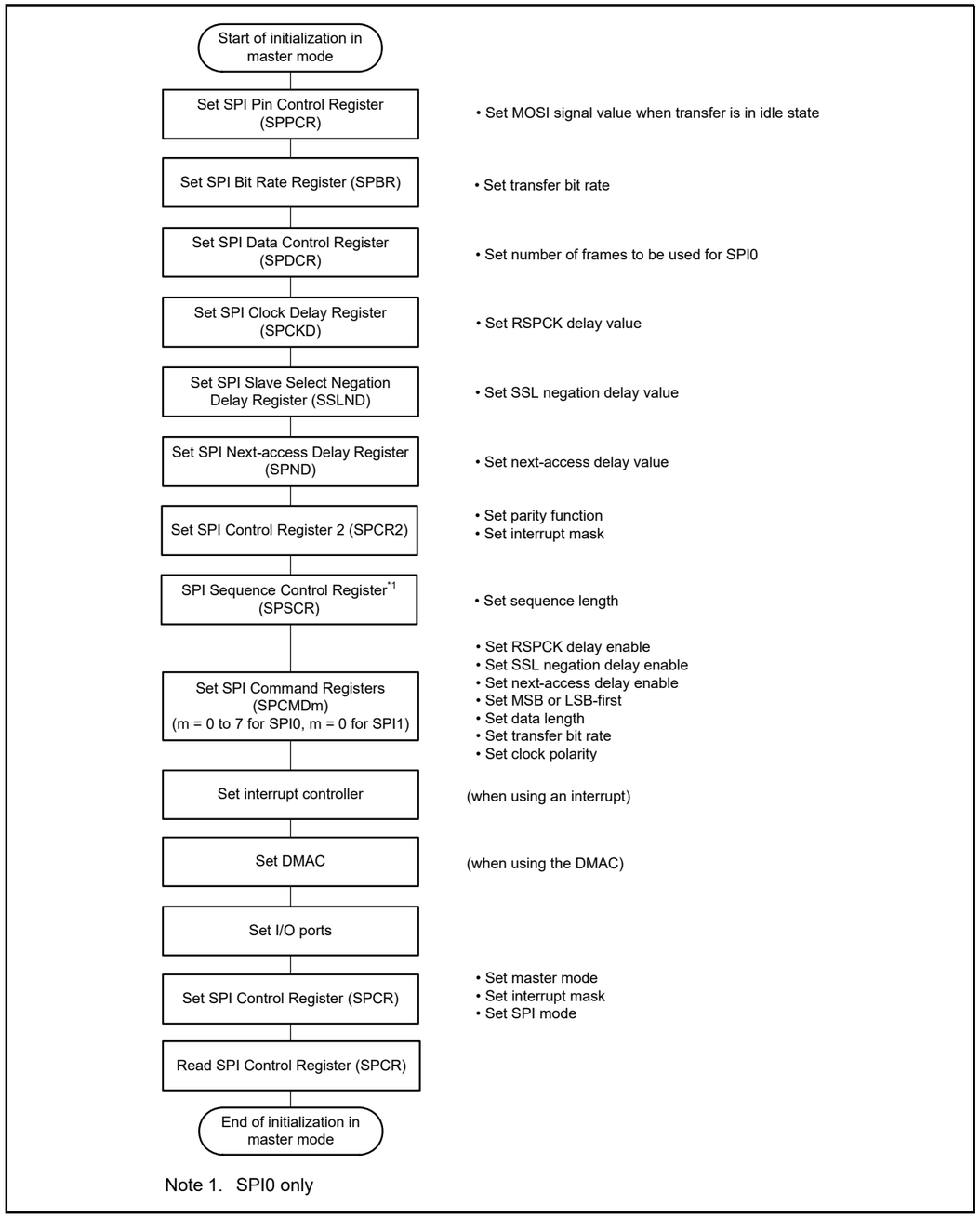


Figure 32.57 Example of initialization flow in master mode for clock synchronous operation

(5) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see section 32.3.10.1, (9) Software processing flow.

Note: Mode fault errors are not generated in clock synchronous operation.

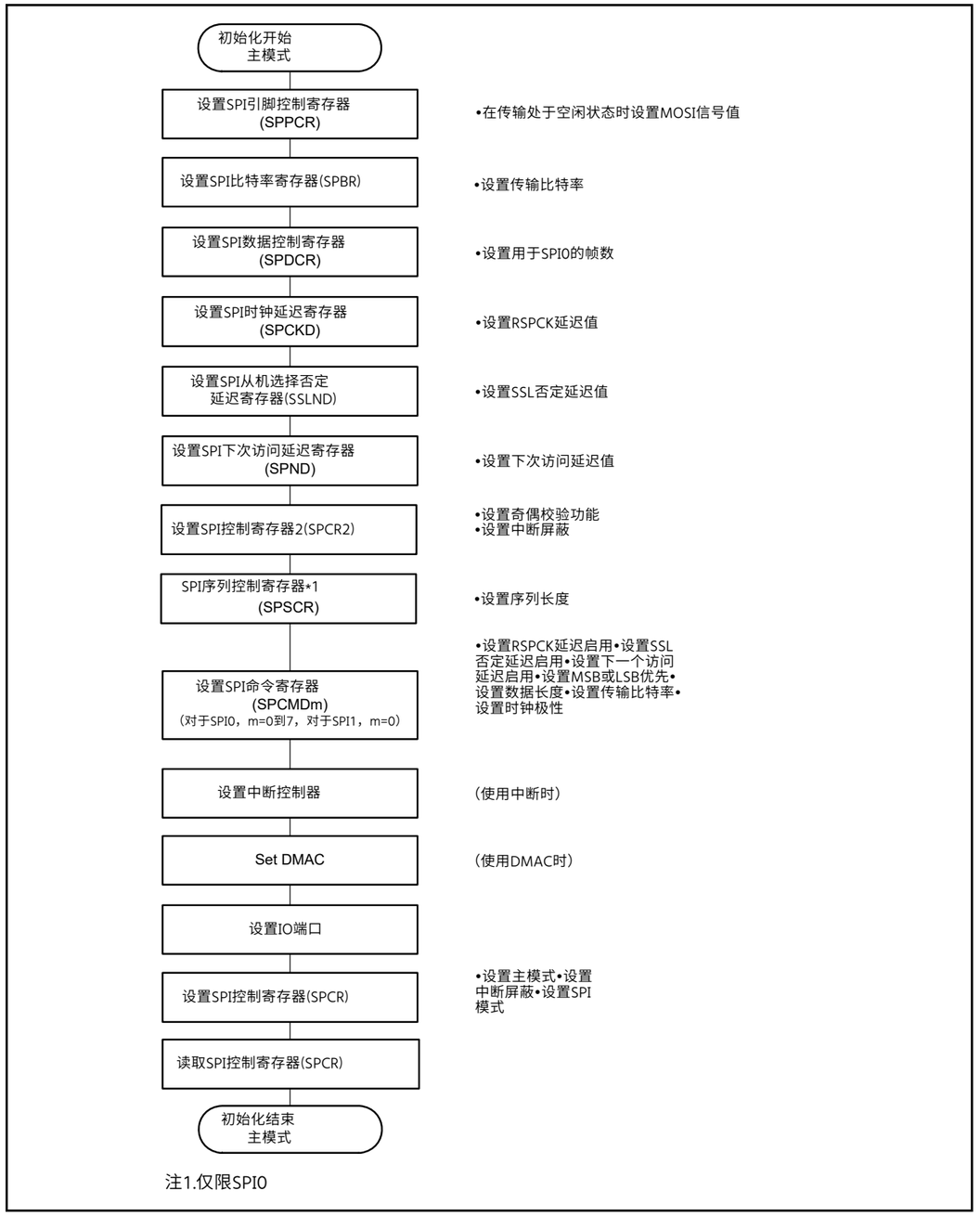


Figure 32.57 时钟同步操作的主模式初始化流程示例

(5) 软件处理流程

时钟同步主机操作期间的软件处理与SPI主机操作相同。详见32.3.10.1节，（9）软件处理流程。

Note: 时钟同步操作中不会产生模式故障错误。

32.3.11.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal.

The SSLn0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(2) Terminating serial transfer

SPI terminates the serial transfer after detecting an RSPCKn edge associated with the final sampling timing. When free space is available in the receive buffer (SPSR.SPRF = 0), on termination of a serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer. The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit setting.

For details on the SPI transfer format, see section 32.3.5, Transfer Format.

(3) Initialization flow

Figure 32.58 shows an example of initialization flow for clock synchronous operation when the SPI is in slave mode. For information on how to set up the Interrupt Controller Unit, DMAC, and I/O ports, see the individual block descriptions.

32.3.11.2 从模式操作

(1) 开始串行传输

当SPCR.SPMS位为1时，第一个RSPCKn边沿触发SPI中串行传输的开始，SPI驱动MISOn输出信号。

SSLn0输入信号不用于时钟同步操作。有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(2) 终止串行传输

SPI在检测到与最终采样时序相关的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间(SPSR.SPRF=0)时，在串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区无关。最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。

有关SPI传输格式的详细信息，请参阅第32.3.5节，传输格式。

(3) 初始化流程

图32.58显示了SPI处于从机模式时时钟同步操作的初始化流程示例。有关如何设置中断控制器单元、DMAC和I/O端口的信息，请参见各个模块说明。

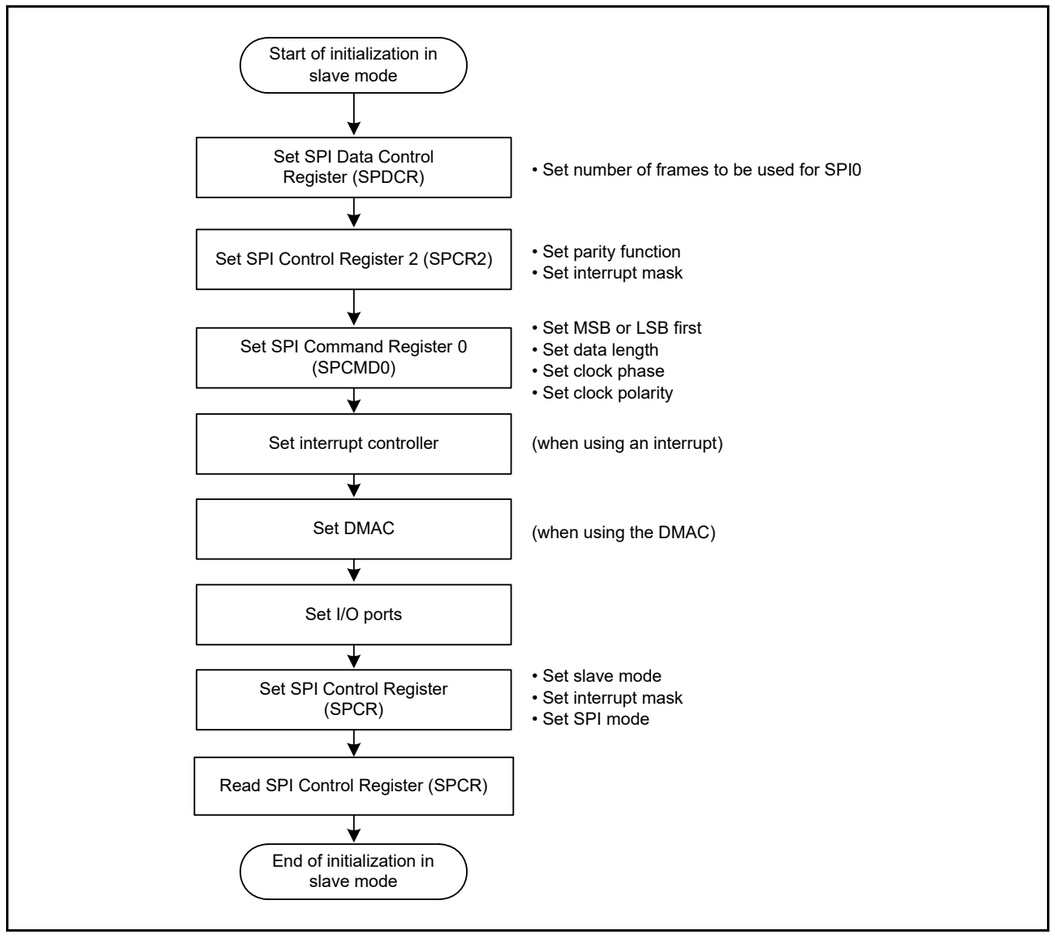


Figure 32.58 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see section 32.3.10.2, (6) Software processing flow.

Note 1. Mode fault errors are not generated in clock synchronous operation.

32.3.12 Loopback mode

When 1 is written to the SPLP2 or SPLP bit in the SPPCR register, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path of the shift register, establishing a loopback mode. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, and between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

Table 32.12 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 32.59 shows the configuration of the shift register I/O paths where the SPI in master mode is set in loopback mode (SPPCR.SPLP2 = 1, SPPCR.SPLP = 0 or 1).

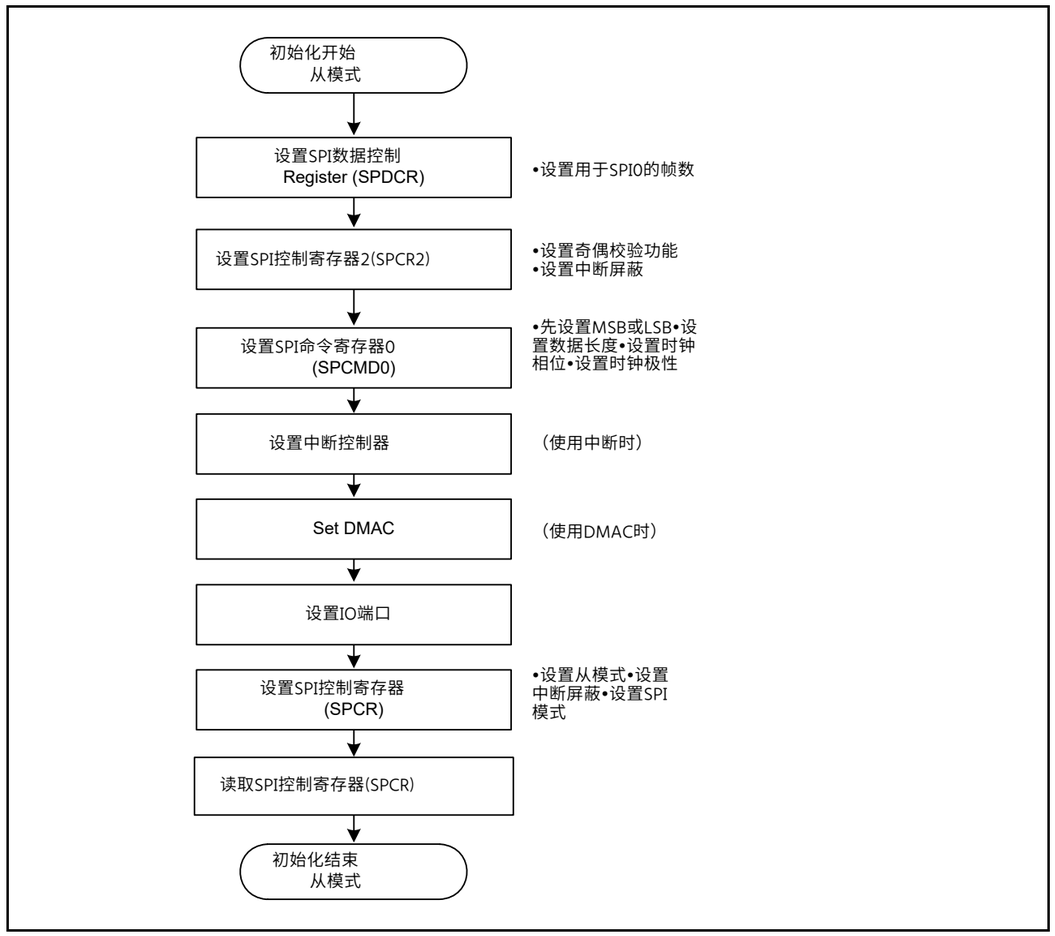


Figure 32.58 时钟同步操作的从模式初始化流程示例

(4) 软件处理流程

时钟同步从机操作期间的软件处理与SPI从机操作相同。详见32.3.10.2节，（6）软件处理流程。

Note 1. 时钟同步操作中不会产生模式故障错误。

32.3.12 Loopback mode

当SPPCR寄存器中的SPLP2或SPLP位写入1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，如果SPCR位为1，则关闭MOSIn引脚和移位寄存器之间的路径.MSTR位为0，连接移位寄存器的输入路径和输出路径，建立环回模式。如果SPCR.MSTR位为1，SPI不关闭MOSIn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则SPI不关闭MISOn引脚和移位寄存器之间的路径。环回模式下，SPI的发送数据或反向发送数据成为SPI的接收数据。

表32.12列出了SPLP2和SPLP位与接收数据之间的关系。图32.59显示了移位寄存器IO路径的配置，其中主模式的SPI设置为环回模式（SPPCR.SPLP2=1，SPPCR.SPLP=0或1）。

Table 32.12 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

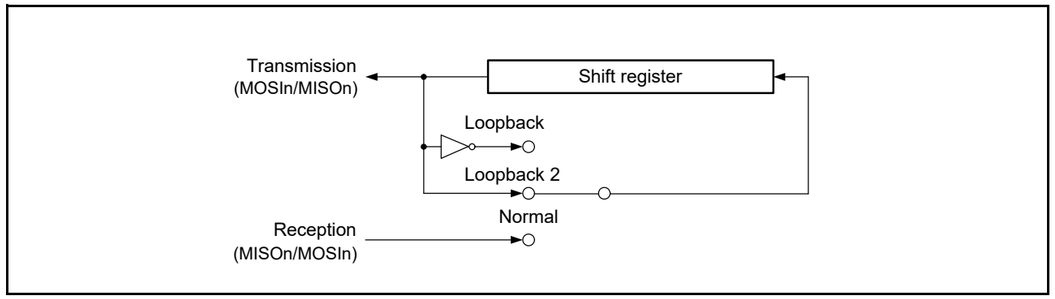


Figure 32.59 Configuration of shift register I/O paths in loopback mode for master mode

32.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for the transmit data and an error detecting unit used for the received data. To detect defects in these units, the parity circuit performs self-diagnosis as shown in Figure 32.60.

Table 32.12 SPLP2和SPLP位设置和接收数据

SPPCR.SPLP2 bit	SPPCR.SPLP bit	接收数据
0	0	从MOSIn引脚或MIOn引脚输入数据
0	1	反相传输数据
1	0	传输数据
1	1	传输数据

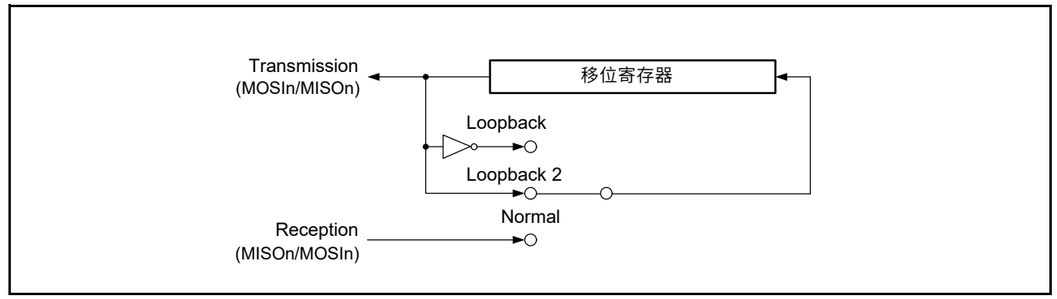


Figure 32.59 在主模式的环回模式下配置移位寄存器IO路径

32.3.13 奇偶校验位功能自诊断

奇偶校验电路由用于发送数据的奇偶校验位添加单元和用于接收数据的错误检测单元组成。为了检测这些单元中的缺陷，奇偶校验电路执行自诊断，如图32.60所示。

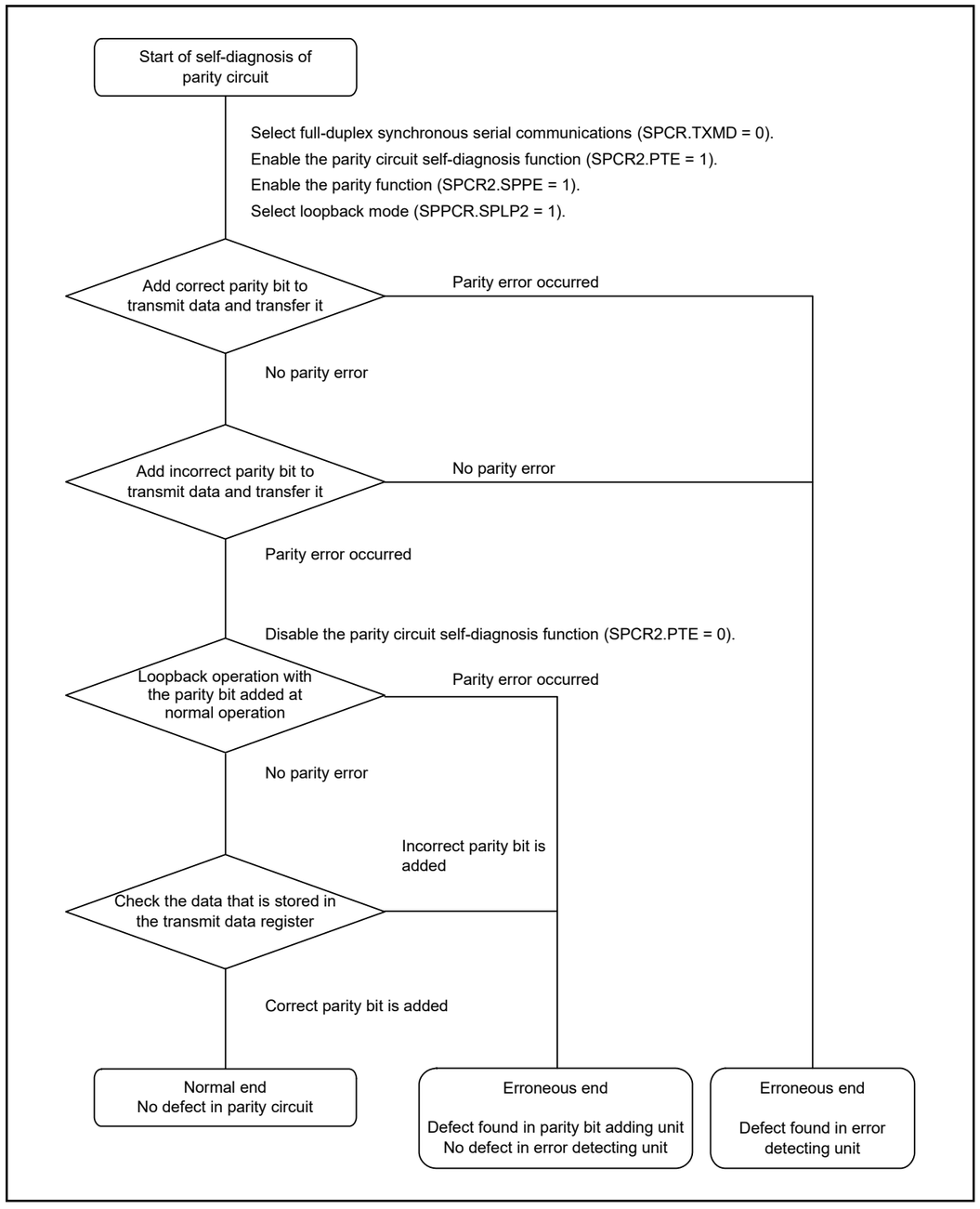


Figure 32.60 Self-diagnosis flow for parity circuit

32.3.14 Interrupt Sources

The SPI has eight interrupt sources:

- Receive buffer full

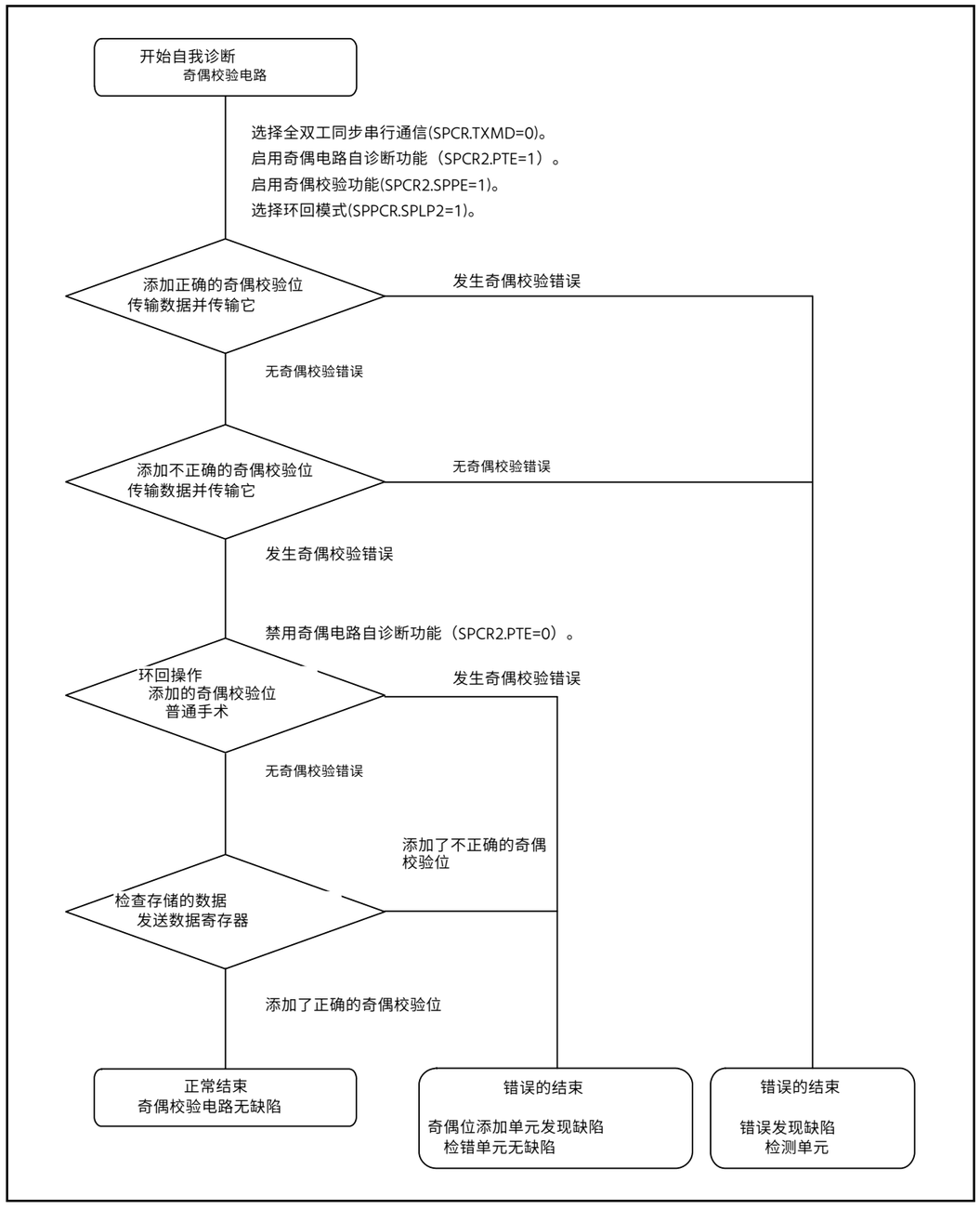


Figure 32.60 奇偶校验电路的自诊断流程

32.3.14 中断源

SPI有8个中断源：

- 接收缓冲区已满

- Transmit buffer empty
- Transmission-completed
- Mode fault
- Underrun
- Overrun
- Parity error
- SPI idle.

In addition, the DTC or DMAC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for SPIn_SPEI is allocated to interrupt requests triggered by mode fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Table 32.13 lists the flags associated with the interrupt sources for the SPI. An interrupt is generated on satisfaction of an interrupt condition in Table 32.13. Clear the receive buffer full and transmit buffer empty sources through data transfer.

When using the DTC or DMAC to perform data transmission or reception, you must first set up the DTC or DMAC to be in a transfer-enabled status before setting the SPI. For information on how to set the DTC or DMAC, see section 17, DMA Controller (DMAC), or section 18, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRj.IR flag is 1, the interrupt is not output as a request for the ICU but is saved internally (the capacity for retention is one request per source). A saved interrupt request is output when the ICU.IELSRj.IR flag becomes 0. A saved interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally saved interrupt request can also be set to 0.

Table 32.13 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DMAC/DTC activation
Receive buffer full	SPIn_SPRI	The receive buffer becomes full (SPSR.SPRF = 1) while the SPCR.SPRIE bit is 1	Possible
Transmit buffer empty	SPIn_SPTI	The transmit buffer becomes empty (SPSR.SPTEF = 1) while the SPCR.SPTIE bit is 1	Possible
SPI errors (mode fault, underrun, overrun, and parity error)	SPIn_SPEI	The SPSR.MODF, OVRF, PERF, or UDRF flag is set to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIn_SPII	The SPSR.IDLNF flag is set to 0 while the SPCR2.SPIIE bit is 1	Impossible
Transmission-completed	SPIn_SPTEND	In master mode, an interrupt is generated when the IDLNF flag (SPI idle flag) changes from 1 to 0. In slave mode, an interrupt occurs on conditions shown in Table 32.15.	Impossible

32.4 Event Link Operation

The Event Link Controller (ELC) can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output.

The event link output signal is output regardless of the interrupt enable bit setting.

- 发送缓冲区为空
- Transmission-completed
- 模式故障
- Underrun
- Overrun
- 奇偶校验错误
- SPI空闲。

此外，可以通过接收缓冲区满或发送缓冲区空中断激活DTC或DMAC以执行数据传输。

由于SPIn_SPEI的向量地址分配给由模式错误、欠载、溢出和奇偶校验错误触发的中断请求，因此必须根据标志确定实际中断源。表32.13列出了与SPI中断源相关的标志。满足表32.13中的中断条件时会生成中断。通过数据传输清除接收缓冲区满和发送缓冲区空源。

使用DTC或DMAC进行数据传输或接收时，必须先将DTC或DMAC设置为传输使能状态，然后再设置SPI。有关如何设置DTC或DMAC的信息，请参阅第17节，DMA控制器(DMAC)或第18节，数据传输控制器(DTC)。

如果在ICU.IELSRj.IR标志为1时发生发送缓冲区空或接收缓冲区满中断的条件，则该中断不会作为对ICU的请求输出，而是在内部保存（保留容量为每个请求一个请求）资源）。当ICU.IELSRj.IR标志变为0时输出保存的中断请求。保存的中断请求在作为实际中断请求输出时自动丢弃。内部保存的中断请求的中断使能位（SPCR.SPTIE或SPCR.SPRIE位）也可以设置为0。

Table 32.13 SPI中断源

中断源	Symbol	中断条件	DMAC/DTC activation
接收缓冲区已满	SPIn_SPRI	当SPCR.SPRIE位为1时，接收缓冲区变满(SPSR.SPRF=1)	Possible
发送缓冲区为空	SPIn_SPTI	当SPCR.SPTIE位为1时，发送缓冲区变为空(SPSR.SPTEF=1)	Possible
SPI错误（模式故障、欠载、溢出和奇偶校验错误）	SPIn_SPEI	SPSR.MODF、OVRF、PERF或UDRF标志设置为1，而SPCR.SPEIE位为1	Impossible
SPI空闲	SPIn_SPII	SPSR.IDLNF标志设置为0，而SPCR2.SPIIE位为1	Impossible
Transmission-completed	SPIn_SPTEND	在主机模式下，当IDLNF标志（SPI空闲标志）从1变为0。 在从机模式下，在表32.15中所示的条件下会发生中断。	Impossible

32.4 事件链接操作

事件链接控制器(ELC)可以产生以下事件输出信号：

- 接收缓冲区满事件输出
- 发送缓冲区空事件输出
- 模式故障、欠载、溢出或奇偶校验错误事件输出
- SPI空闲事件输出
- 传输完成事件输出。

无论中断允许位设置如何，都会输出事件链接输出信号。

32.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of a serial transfer.

32.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmission buffer to the shift register and when the value of the SPE bit changes from 0 to 1.

32.4.3 Mode Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode fault, underrun, overrun or parity error is detected. See section 32.5.4, Constraint on Mode Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode fault

Table 32.14 lists the conditions for occurrence of a mode fault event.

Table 32.14 Conditions for occurrence of mode fault

Condition	SPCR.MODFEN bit	SSLn0 pin	Remark
SPI operation (SPMS = 0) Slave (SPCR.MSTR bit = 0)	1	Not active	Event is output only when the pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the reception buffer contains unread data, and the value of the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

32.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

32.4.5 Transmission-Completed Event Output

During both SPI and clock synchronous operations in master mode, an event is output when the IDLNF flag (SPI idle flag) changes from 1 to 0.

Table 32.15 Conditions for generation of transmission-completed event in slave mode

	Transmit buffer state	Shift register state	Others
SPI operation (SPMS = 0)	Empty	Empty	Negation of SSLn0 input
Clock synchronous operation (SPMS = 1)	Empty	Empty	Edge detection of the last RSPCKn

Whether the operation is in master mode or slave mode, an event is not output if 0 is written to the SPCR.SPE bit in

32.4.1 接收缓冲区满事件输出

串行传输完成后，当接收到的数据从移位寄存器传输到SPDRSPDR_HA时，输出此事件信号。

32.4.2 发送缓冲区空事件输出

当要发送的数据从发送缓冲器传送到移位寄存器时，以及SPE位的值从0变为1时，输出该事件信号。

32.4.3 模式故障、欠载、溢出或奇偶校验错误事件输出

当检测到模式故障、欠载、溢出或奇偶校验错误时，输出该事件信号。如果使用此事件信号，请参见第32.5.4节，模式故障、欠载、溢出或奇偶校验错误事件输出的约束。

(1) 模式故障

表32.14列出了模式故障事件发生的条件。

Table 32.14 发生模式故障的条件

Condition	SPCR.MODFEN bit	SSLn0 pin	Remark
SPI操作(SPMS=0) 从机（SPCR.MSTR位=0）	1	不活跃	仅当在传输过程中禁用该引脚时才输出事件

(2) Underrun

当串行传输开始而传输数据尚未准备好，并且SPCR.MSTR位的值为0且SPCR.SPE位为1时，输出此事件信号以响应欠载。在这些条件下，MODF和UDRF标志设置为1。

(3) Overrun

当串行传输完成而接收缓冲区包含未读数据且SPCR.TXMD位的值为0时，输出此事件信号以响应溢出。在这些情况下，OVRF标志设置为1。

(4) 奇偶校验错误

该事件信号是响应在串行传输完成时检测到的奇偶校验错误而输出的，而SPCR中的TXMD位为0，SPCR2中的SPPE位的值为1。

32.4.4 SPI空闲事件输出

(1) 在主模式

在主机模式下，当将IDLNF标志（SPI空闲标志）设置为0的条件成立时输出事件。

(2) 在从模式

在从机模式下，当SPCR.SPE位设置为0（SPI初始化）时，会输出一个事件。

32.4.5 传输完成事件输出

在主机模式下的SPI和时钟同步操作期间，当IDLNF标志（SPI空闲标志）从1变为0时输出事件。

Table 32.15 从机模式下发生传输完成事件的条件

	发送缓冲区状态	移位寄存器状态	Others
SPI操作(SPMS=0)	Empty	Empty	SSLn0输入的否定
时钟同步操作(SPMS=1)	Empty	Empty	最后一个RSPCKn的边缘检测

无论操作是主模式还是从模式，如果向SPCR.SPE位写入0，则不输出事件

transmission or the SPCR.SPE bit is cleared by the mode fault or underrun error.

32.5 Usage Notes

32.5.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable SPI operation. The SPI is initially stopped after a reset. The registers become accessible on release from the module-stop state. For details on the Module Stop Control Register B, see section 11, Low Power Modes.

32.5.2 Constraint on Low Power Function

When using the module-stop function and entering a low power mode other than sleep mode, set the SPCR.SPE bit to 0 before completing communication.

32.5.3 Constraint on Starting Transfer

If the ICU.IELSRj.IR flag is 1 at the start of transfer, an interrupt request is internally saved after transfer starts, and this can lead to unanticipated behavior of the ICU.IELSRj.IR flag. To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1).

1. Confirm that transfer stopped (SPCR.SPE = 0).
2. Set the relevant interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) to 0.
3. Read the relevant interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) and confirm that its value is 0.
4. Set the ICU.IELSRj.IR flag to 0.

32.5.4 Constraint on Mode Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode fault, underrun, overrun, or parity error event is prohibited if the SPI is in multi-master mode (the SPCR.SPMS bit is 0, SPCR.MSTR bit is 1, and SPCR.MODFEN bit is 1).

32.5.5 Constraint on the SPRF and SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, using an interrupt is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupt or the flag can be used, but not both.

传输或SPCR.SPE位由模式故障或欠载错误清除。

32.5 使用说明

32.5.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SPI操作。SPI在复位后最初停止。寄存器在从模块停止状态释放时变得可访问。有关模块停止控制寄存器B的详细信息，请参见第11节，低功耗模式。

32.5.2 对低功耗函数的约束

当使用模块停止功能并进入除睡眠模式以外的低功耗模式时，在完成通信之前将SPCR.SPE位设置为0。

32.5.3 开始传输的限制

如果ICU.IELSRj.IR标志在传输开始时为1，则在传输开始后内部保存一个中断请求，这可能导致ICU.IELSRj.IR标志的意外行为。为防止这种情况发生，请使用以下程序在使能操作之前清除中断请求（通过将SPCR.SPE位设置为1）。

1.确认传输已停止(SPCR.SPE=0)。
2.将相关中断使能位（SPCR.SPTIE或SPCR.SPRIE）设置为0。
3.读取相关中断使能位（SPCR.SPTIE或SPCR.SPRIE），确认其值为0。
4.将ICU.IELSRj.IR标志设置为0。

32.5.4 模式故障、欠载、溢出或奇偶校验错误事件输出的约束

如果SPI处于多主模式（
SPCR.SPMS位为0，SPCR.MSTR位为1，SPCR.MODFEN位为1)。

32.5.5 SPRF和SPTEF标志的约束

如果使用轮询标志SPRF和SPTEF，则禁止使用中断，您必须设置SPCR.SPRIE和SPCR.SPTIE位为0。可以使用中断或标志，但不能同时使用。

33. Cyclic Redundancy Check (CRC) Calculator

33.1 Overview

The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring of reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

Table 33.1 lists the specifications of the CRC calculator and Figure 33.1 shows a block diagram.

Table 33.1 CRC calculator specifications

Parameter	Description	
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC code generated for data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC]: • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	One of two generating polynomials that is selectable: [32-bit CRC]: • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
CRC snoop	Monitor reads from and writes to a certain register address	-

Note 1. The circuit cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

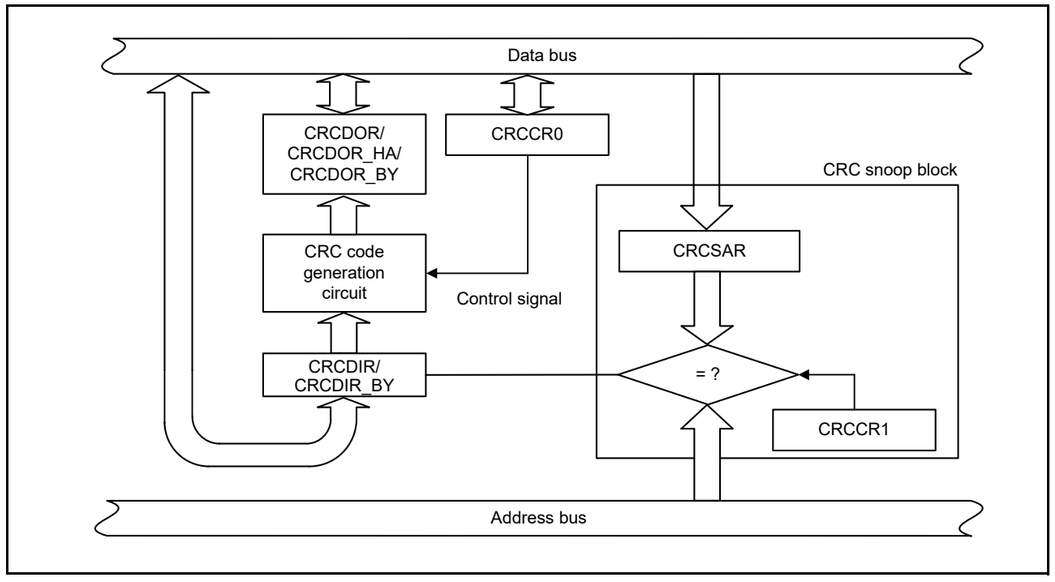


Figure 33.1 CRC calculator block diagram

33. 循环冗余校验(CRC)计算器

33.1 Overview

循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。

表33.1列出了CRC计算器的规格，图33.1显示了框图。

Table 33.1 CRC计算器规格

Parameter	Description	
数据大小	8-bit	32-bit
CRC计算数据*1	以8n位为单位为任何所需数据生成CRC码（其中n是整数）	为32n位单元中的数据生成的CRC码（其中n是整数）
CRC处理器单元	在8位上并行执行的操作	在32位上并行执行的操作
CRC生成多项式	三个可选择的生成多项式之一：[8位CRC]：X8+X2+X+1(CRC-8)[16位CRC] X16+X15+X2+1(CRC-16) X16+X12+X5+1(CRC-CCITT)。	可选择的两个生成多项式之一：[32位CRC]： X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X+1(CRC-32) X32+X28+X27+X26+X25+X23+X22+X20+X19+X18+X14+X13+X11+X10+X9+X8+X6+1(CRC-32C)。
CRC计算切换	CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信	
Module-stop function	可设置模块停止状态以降低功耗	
CRC snoop	监视器读取和写入某个寄存器地址	-

Note 1. 该电路不能划分用于CRC计算的数据。以8位或32位为单位写入数据。

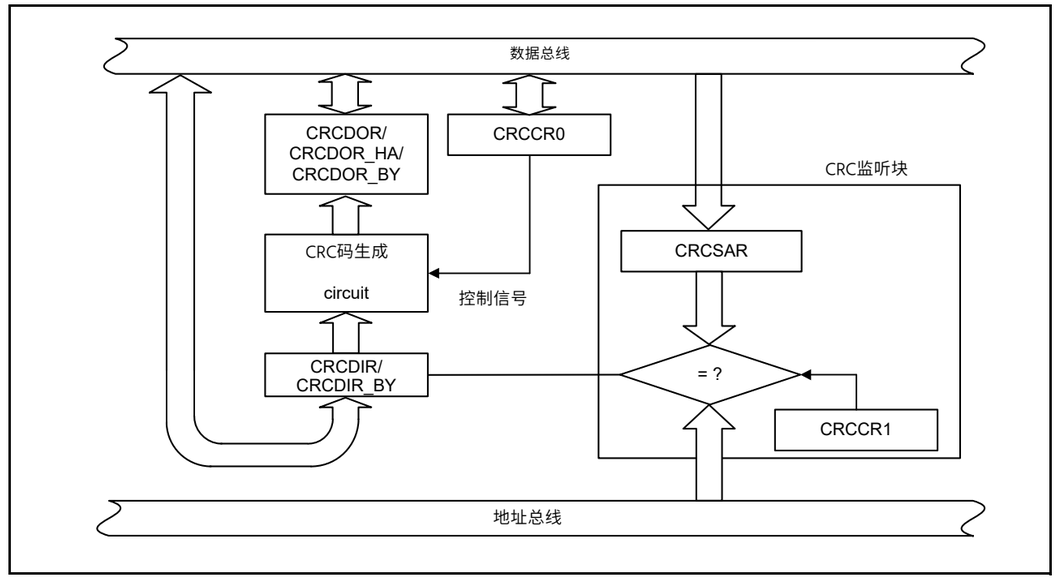


Figure 33.1 CRC计算器框图

33.2 Register Descriptions

33.2.1 CRC Control Register 0 (CRCCR0)

Address(es): CRC.CRCCR0 4007 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	GPS[2:0]	CRC Generating Polynomial Switching	b2 b0 0 0 0: No calculation is executed 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Other: No calculation is executed.	R/W
b5 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LMS	CRC Calculation Switching	0: Generates CRC for LSB-first communication 1: Generates CRC for MSB-first communication.	R/W
b7	DORCLR	CRCDOR/CRCDOR_HA/ CRCDOR_BY Register Clear	1: Clears the CRCDOR/CRCDOR_HA/CRCDOR_BY register. This bit is read as 0.	W*1

Note 1. Always set this bit to 1 when writing to this register.

GPS[2:0] bits (CRC Generating Polynomial Switching)

Set the GPS[2:0] bits to select the CRC Generating Polynomial.

LMS bit (CRC Calculation Switching)

Set this bit to select the bit order of the generated CRC code. Transmit the lower byte of the CRC code first for LSB-first communication and the upper byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 33.3, Operation.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Write 1 to this bit to set the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0000 0000h. This bit is read as 0. Only 1 can be written to it.

33.2.2 CRC Control Register 1 (CRCCR1)

Address(es): CRC.CRCCR1 4007 4001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CRCSEN	CRCSWR	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CRCSWR	Snoop-On-Write/Read Switch	0: Snoop-on-read 1: Snoop-on-write.	R/W

33.2 注册说明

33.2.1 CRC控制寄存器0(CRCCR0)

Address(es): CRC.CRCCR0 4007 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	LMS	—	—	—	GPS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	GPS[2:0]	CRC生成多项式 Switching	b2 b0 0 0 0：不执行计算 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 其他：不执行计算。	R/W
b5 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	LMS	CRC计算切换	0：为LSB优先通信生成CRC1：为MSB优先通信生成CRC。	R/W
b7	DORCLR	CRCDOR/CRCDOR_HA/ CRCDOR_BY Register Clear	1：清除CRCDORCRCDOR_HACRCDOR_BY寄存器。该位读为0。	W*1

Note 1. 写入该寄存器时始终将此位设置为1。

GPS[2:0]位（CRC生成多项式切换）

设置GPS[2:0]位以选择CRC生成多项式。

LMS位（CRC计算切换）

设置该位以选择生成的CRC码的位顺序。对于LSB在先的通信，首先发送CRC码的低字节，对于MSB在先的通信，首先发送高字节。有关发送和接收CRC码的详细信息，请参阅第33.3节，操作。

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY)

向该位写入1可将CRCDORCRCDOR_HACRCDOR_BY寄存器设置为00000000h。该位读为0。只能写入1。

33.2.2 CRC控制寄存器1(CRCCR1)

Address(es): CRC.CRCCR1 4007 4001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CRCSEN	CRCSWR	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	CRCSWR	Snoop-On-Write/Read Switch	0: Snoop-on-read 1: Snoop-on-write.	R/W

Bit	Symbol	Bit name	Description	R/W
b7	CRCSEN	Snoop Enable	0: Disabled 1: Enabled.	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

The CRCSWR bit selects the direction of access in the address monitoring function.

When this bit is set to 0 (initial value), the CRC snoop operation to read a specific register address is valid. Similarly, when this bit is set to 1, the CRC snoop operation to write a specific register address is valid.

CRCSEN bit (Snoop Enable)

When the CRCSEN bit is set to 1, the CRC snoop operation is valid. When this bit is set to 0, the CRC snoop operation is invalid.

33.2.3 CRC Data Input Register (CRCDIR/CRCDIR_BY)

Address(es): CRC.CRCDIR/CRCDIR_BY 4007 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CRCDIR register is a read/write 32-bit register to write data for CRC-32 or CRC-32C calculation. The CRCDIR_BY register is a read/write 8-bit register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.

33.2.4 CRC Data Output Register (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Address(es): CRC.CRCDOR/CRCDOR_HA/CRCDOR_BY 4007 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CRCDOR register is a read/write 32-bit register for CRC-32 or CRC-32C calculation.

The CRCDOR_HA register is a read/write 16-bit register for CRC-16 or CRC-CCITT calculation.

The CRCDOR_BY register is a read/write 8-bit register for CRC-8 calculation.

Because its initial value is 0000 0000h, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to performthe calculations using a value other than the initial value.

Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/ CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following transferred data and the result is 0000 0000h, there is no CRC error.

When an 8-bit CRC ($X^8 + X^2 + X + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_BY.

When a 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$ or $X^{16} + X^{12} + X^5 + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_HA.

Bit	Symbol	位名称	Description	R/W
b7	CRCSEN	侦听启用	0：禁用1 ：启用。	R/W

CRCSWR位（Snoop-On-Write读开关）

CRCSWR位选择地址监控功能中的访问方向。

当该位设置为0（初始值）时，读取特定寄存器地址的CRCsnoop操作有效。同样，当该位设置为1时，写入特定寄存器地址的CRCsnoop操作有效。

CRCSEN位（侦听启用）

当CRCSEN位设置为1时，CRC监听操作有效。当该位设置为0时，CRC监听操作无效。

33.2.3 CRC数据输入寄存器(CRCDIRCRCDIR_BY)

Address(es): CRC.CRCDIR/CRCDIR_BY 4007 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDIR寄存器是一个读写32位寄存器，用于写入数据以进行CRC-32或CRC-32C计算。这CRCDIR_BY寄存器是一个读写8位寄存器，用于为CRC-8、CRC-16或CRC-CCITT计算写入数据。

33.2.4 CRC数据输出寄存器(CRCDORCRCDOR_HACRCDOR_BY)

Address(es): CRC.CRCDOR/CRCDOR_HA/CRCDOR_BY 4007 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDOR寄存器是用于CRC-32或CRC-32C计算的读写32位寄存器。

CRCDOR_HA寄存器是一个用于CRC-16或CRC-CCITT计算的读写16位寄存器。

CRCDOR_BY寄存器是一个用于CRC-8计算的读写8位寄存器。

由于其初始值为00000000h，重写CRCDORCRCDOR_HACRCDOR_BY寄存器以使用初始值以外的值执行计算。

写入CRCDIRCRCDIR_BY寄存器的数据经过CRC计算，结果存储在CRCDOR CRCDOR_HACRCDOR_BY寄存器。如果在传输数据后计算CRC码，结果为00000000h，则没有CRC错误。

当使用8位CRC（X8+X2+X+1多项式）时，在CRCDOR_BY中获得有效的CRC码。

当使用16位CRC（X16+X15+X2+1或X16+X12+X5+1多项式）时，有效的CRC码在CRCDOR_HA.

33.2.5 Snoop Address Register (CRCSAR)

Address(es): CRC.CRCSAR 4007 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CRCSA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CRCSA[13:0]	Register Snoop Address	Set the TDR or RDR address in the SCI module to snoop	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CRCSA[13:0] bits (Register Snoop Address)

Set the CRCSA[13:0] bits to the lower 14-bits of register address monitored by the CRC snoop operation.

Only the following addresses can be used for the CRCSA[13:0] bits:

- 4007 0003h: SCI0.TDR, 4007 0005h: SCI0.RDR
- 4007 0023h: SCI1.TDR, 4007 0025h: SCI1.RDR
- 4007 0123h: SCI9.TDR, 4007 0125h: SCI9.RDR
- 4007 000Fh: SCI0.FTDRL,4007 0011h: SCI0.FRDRL
- 4007 002Fh: SCI1.FTDRL,4007 0031h: SCI1.FRDRL.

33.3 Operation

33.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.

The following examples show CRC code generation for input data (F0h) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When a 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

Figure 33.2 and Figure 33.3 show the LSB-first and MSB-first data transmission examples respectively. Figure 33.4 and Figure 33.5 show the LSB-first and MSB-first data reception examples.

33.2.5 监听地址寄存器(CRCSAR)

Address(es): CRC.CRCSAR 4007 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CRCSA[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	CRCSA[13:0]	注册监听地址	设置SCI模块中的TDR或RDR地址为snoop	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CRCSA[13:0]位（寄存器监听地址）

将CRCSA[13:0]位设置为CRC侦听操作监视的寄存器地址的低14位。

CRCSA[13:0]位只能使用以下地址：

- 4007 0003h: SCI0.TDR, 4007 0005h: SCI0.RDR
- 4007 0023h: SCI1.TDR, 4007 0025h: SCI1.RDR
- 4007 0123h: SCI9.TDR, 4007 0125h: SCI9.RDR
- 4007 000Fh: SCI0.FTDRL,4007 0011h: SCI0.FRDRL
- 4007 002Fh: SCI1.FTDRL,4007 0031h: SCI1.FRDRL.

33.3 Operation

33.3.1 基本操作

CRC计算器生成用于LSB优先或MSB优先传输的CRC代码。

以下示例显示了使用16位CRC-CCITT生成多项式(X16+X12+X5+1)为输入数据(F0h)生成CRC码。在这些示例中，CRC数据输出寄存器(CRCDOR_HA)的值在CRC计算之前被清除。

当使用8位CRC（多项式X8+X2+X+1）时，CRC码的有效位在CRCDOR_BY。使用32位CRC时，在CRCDOR中获取CRC码的有效位。

图33.2和图33.3分别显示了LSB-first和MSB-first数据传输示例。图33.4和图33.5显示了LSB优先和MSB优先的数据接收示例。

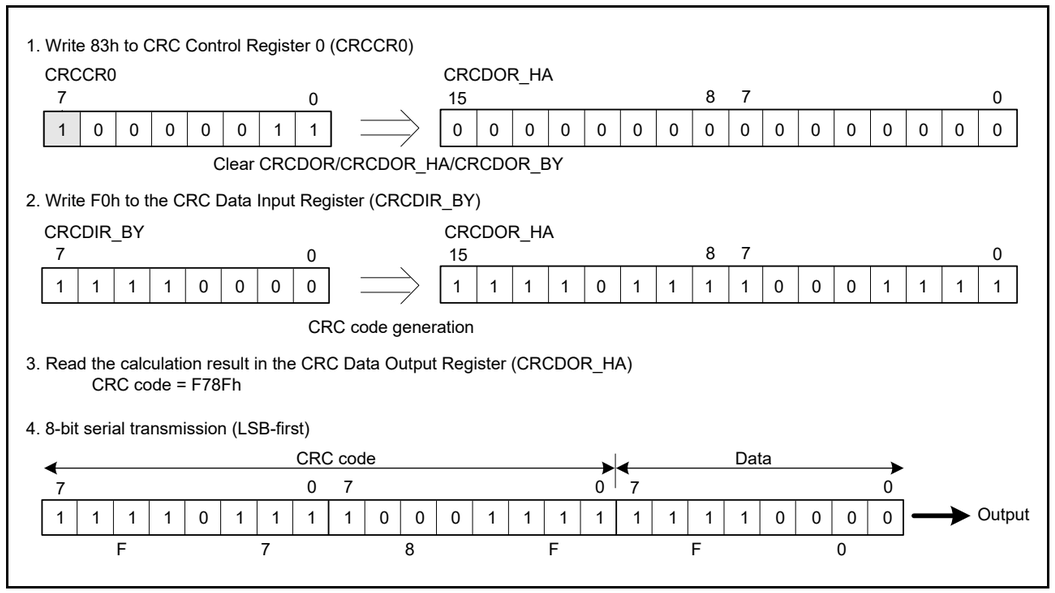


Figure 33.2 LSB-first data transmission

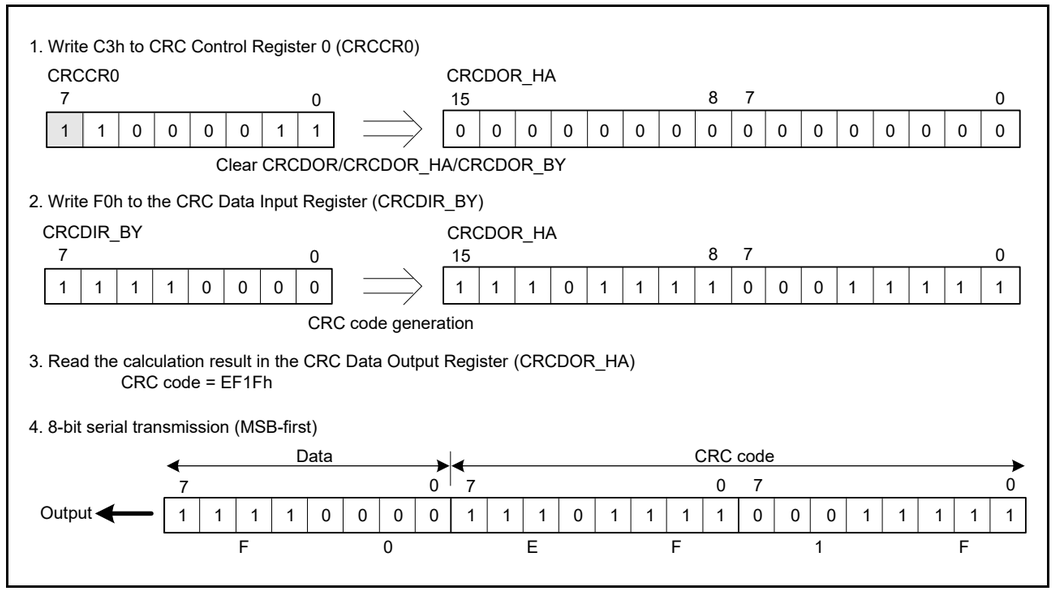


Figure 33.3 MSB-first data transmission

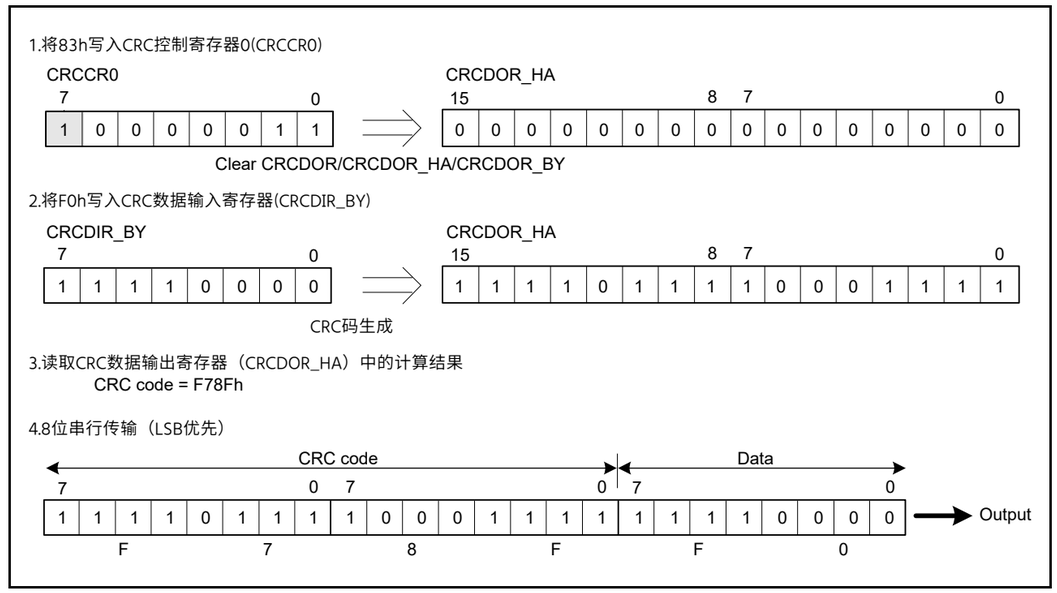


Figure 33.2 LSB−first数据传输

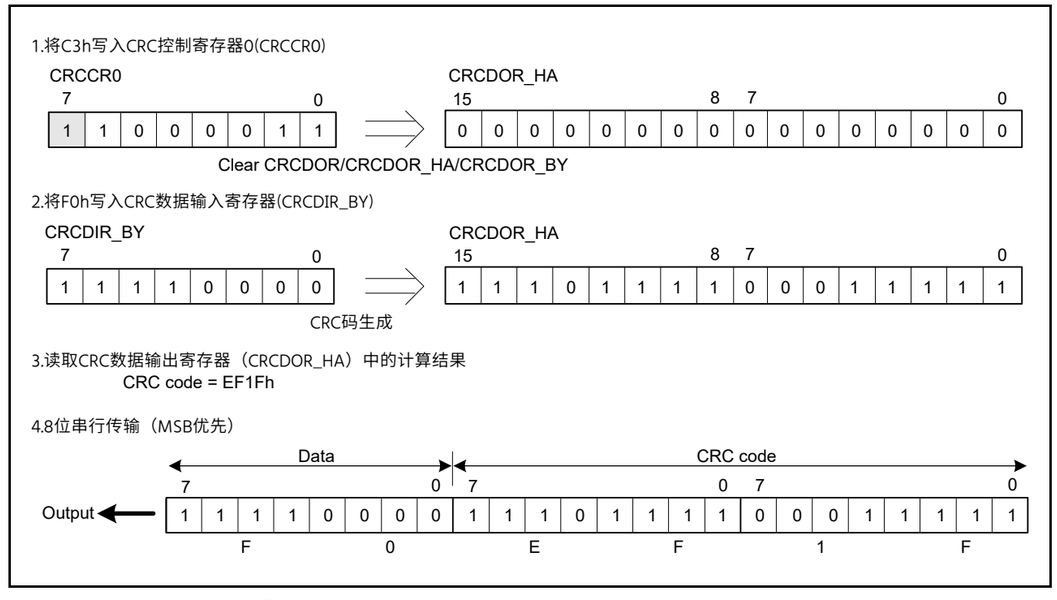


Figure 33.3 MSB优先数据传输

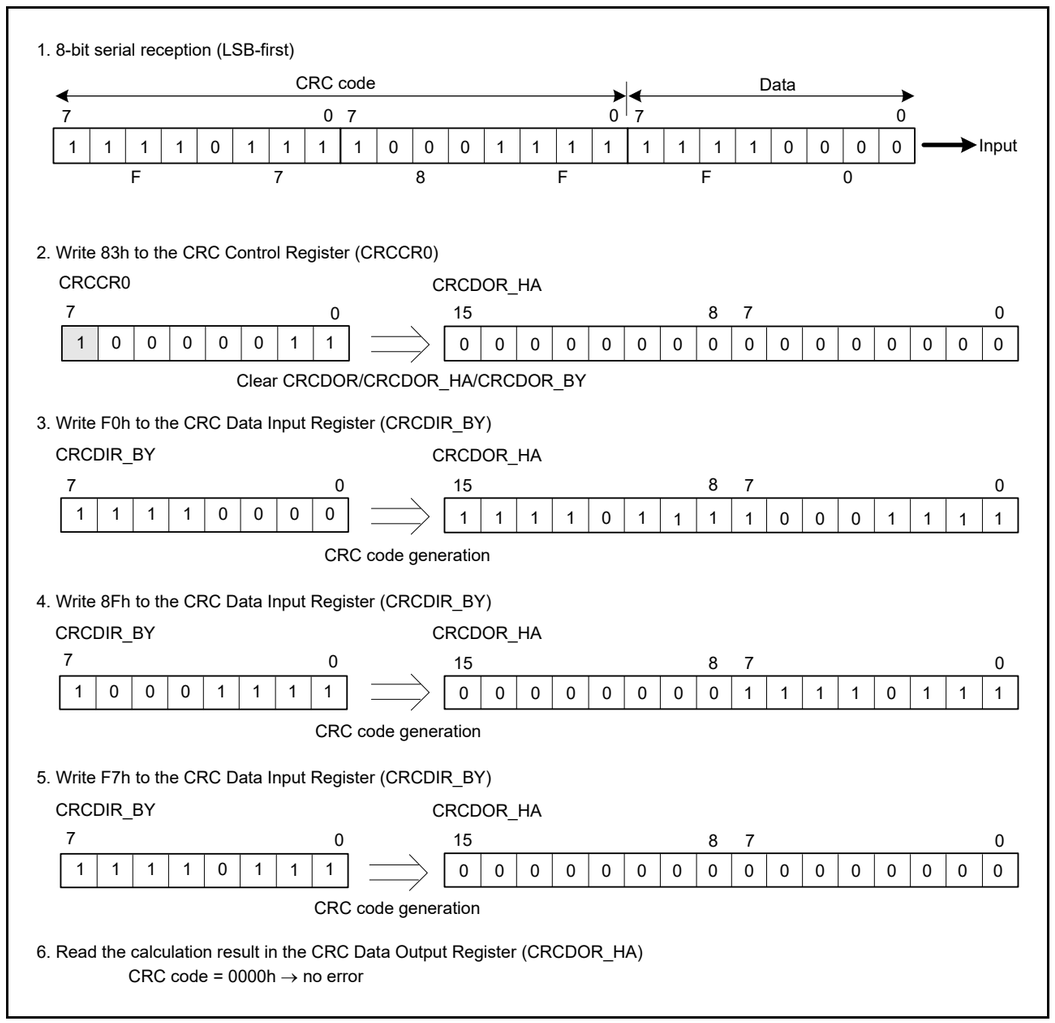


Figure 33.4 LSB-first data reception

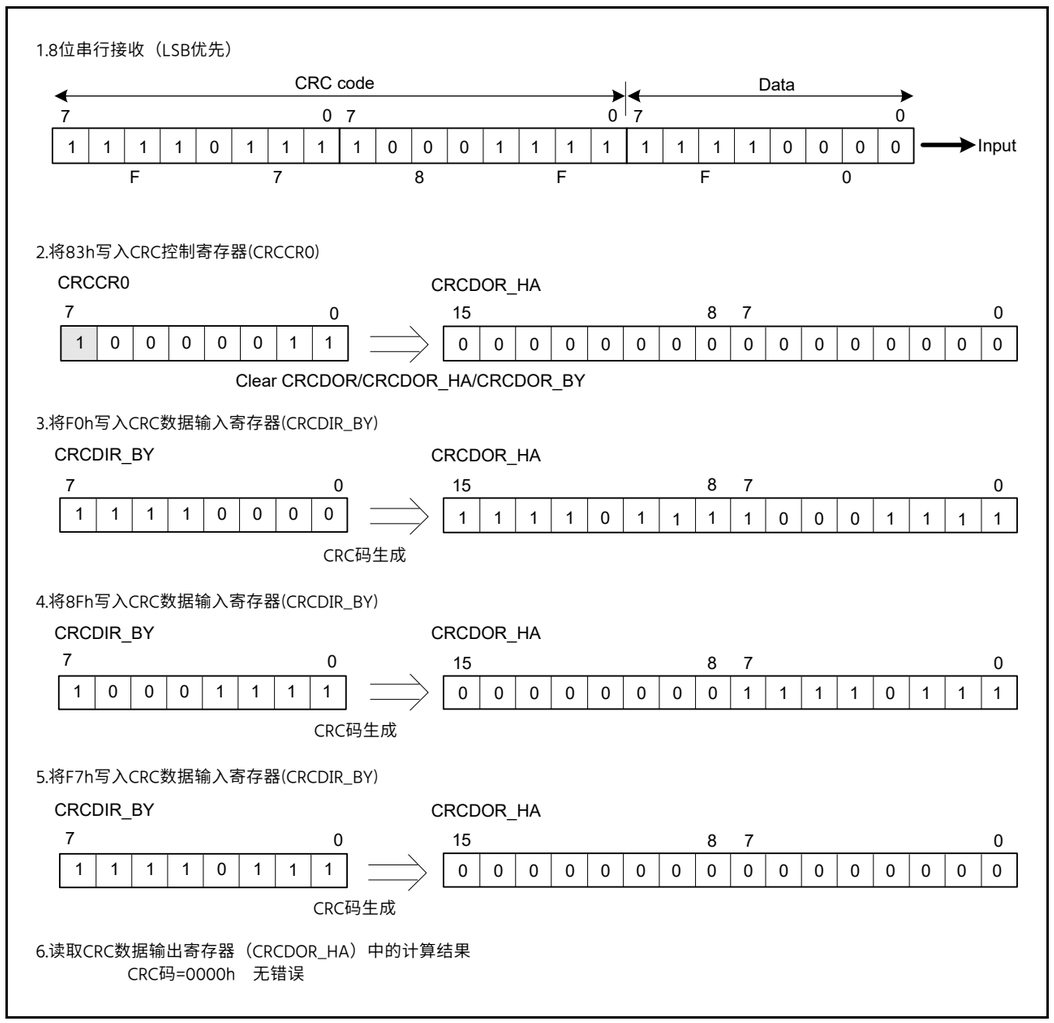


Figure 33.4 LSB−first数据接收

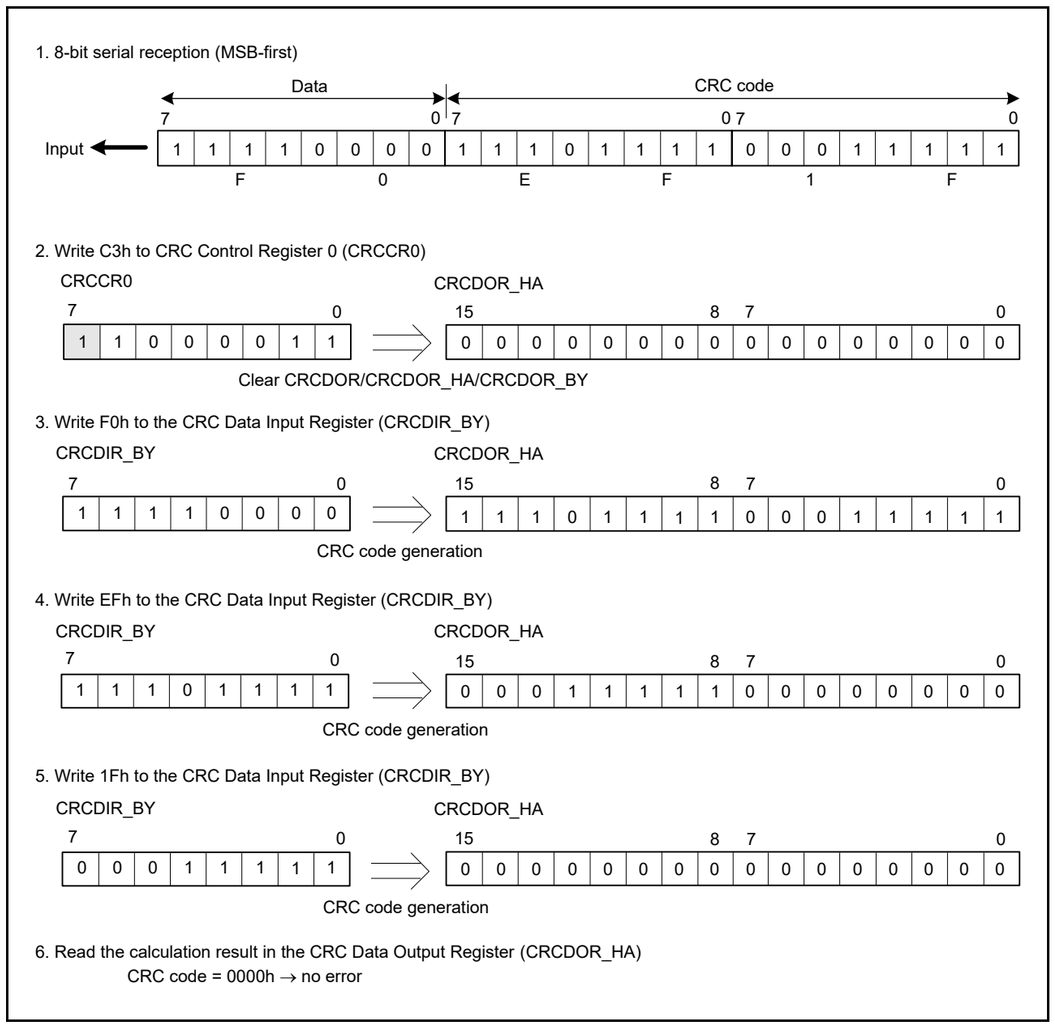


Figure 33.5 MSB-first data reception

33.3.2 CRC Snoop

The CRC snoop function monitors reads from and writes to a specific register address and performs CRC calculation on the data read from and written to that register address automatically. Because the CRC snoop recognizes writes to and reads from a specific register address as a trigger to automatically perform CRC calculations, there is no need to write data to the CRCDIR_BY register. All I/O register addresses specified in the Snoop Address Register (CRCSAR) are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the serial transmit buffer, and reads from the serial receive buffer.

To use this function, write a target I/O register address to bits CRCSA13 to CRCSA0 in the CRCSAR register, and set the CRCSEN bit in the CRCCR1 register to 1. Then, set the CRCSWR bit in the CRCCR1 register to 1 to enable snooping on writes to the target address, or set the CRCSWR bit in the CRCCR1 register to 0 to enable snooping on reads from the target address.

When setting the CRCSEN bit to 1, CRCSWR bit to 1, and writing data to a target I/O register address in a bus master module such as the CPU, DMA, and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculations. Similarly, when setting the CRCSEN bit to 1, CRCSWR bit to 0, and reading data in a target I/O

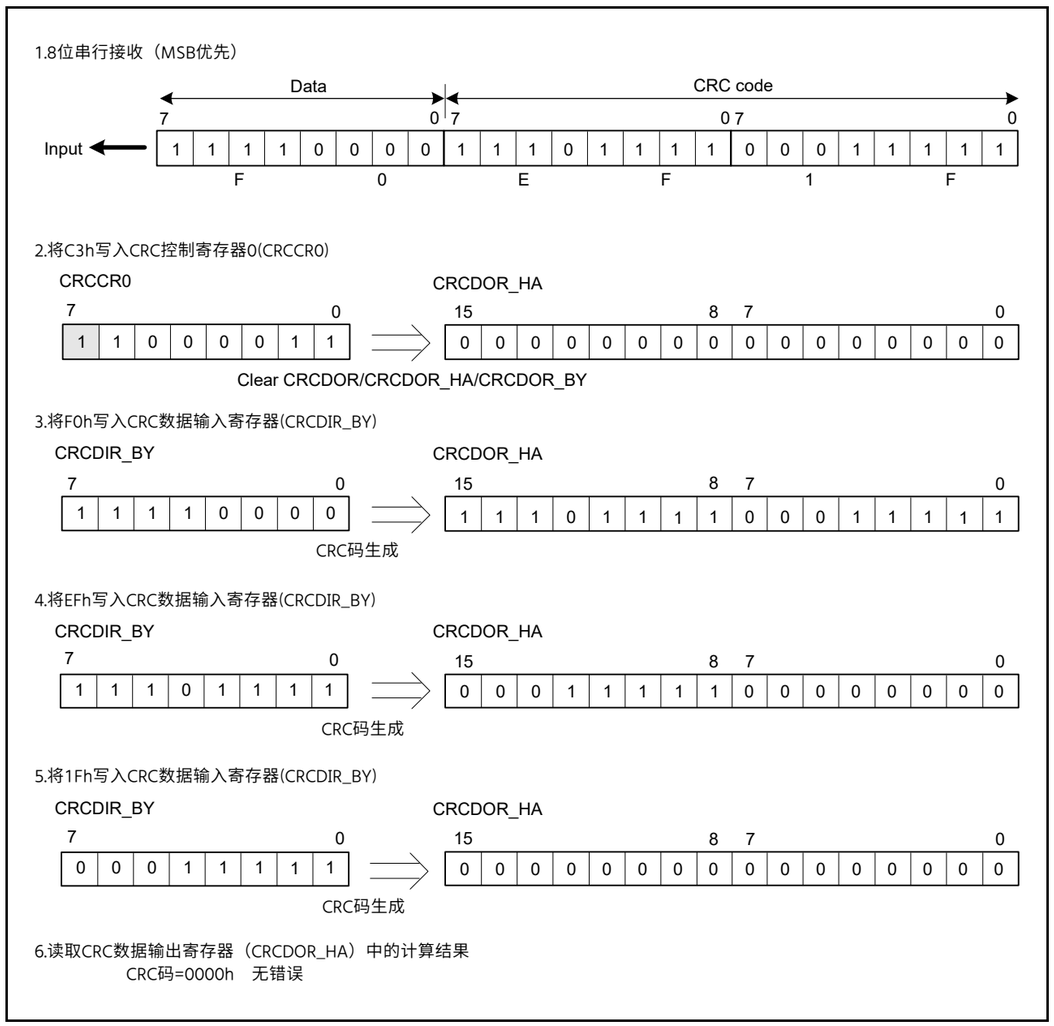


Figure 33.5 MSB优先数据接收

33.3.2 CRC Snoop

CRCsnoop功能监视对特定寄存器地址的读取和写入，并对从该寄存器地址读取和写入的数据自动执行CRC计算。由于CRCsnoop将特定寄存器地址的写入和读取识别为触发以自动执行CRC计算，因此无需将数据写入CRCDIR_BY寄存器。SnoopAddressRegister(CRCSAR)中指定的所有IO寄存器地址都受CRCsnoop影响。CRCsnoop在监视对串行发送缓冲区的写入和从串行接收缓冲区读取时很有用。

要使用此功能，请将目标IO寄存器地址写入CRCSAR寄存器中的CRCSA13至CRCSA0位，并将CRCCR1寄存器中的CRCSEN位设置为1。然后，将CRCCR1寄存器中的CRCSWR位设置为1，以启用写监听到目标地址，或将CRCCR1寄存器中的CRCSWR位设置为0，以启用对目标地址读取的侦听。

CRCSEN位为1，CRCSWR位为1，并将数据写入CPU、DMA和DTC等总线主模块中的目标IO寄存器地址时，CRC计算器将数据存储在CRCDIR_BY寄存器中并执行CRC计算。同理，当设置CRCSEN位为1，CRCSWR位为0，读取目标IO中的数据

register address in a bus master module such as the CPU, DMA, and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculations.

CRC calculation is performed 1 byte at a time. When the target I/O register address is accessed in words (16 bits) or long words (32 bits), the CRC code is generated on the lower byte (1 byte) of data.

33.4 Usage Notes

33.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable CRC calculator operation. The CRC is stopped after a reset. The registers become accessible on releasing the module-stop state. For details, see section 11, Low Power Modes.

33.4.2 Notes on Transmission

The sequence of transmission for the CRC code differs based on whether the transmission is LSB-first or MSB-first. Figure 33.6 shows an LSB-first and MSB-first data transmission.

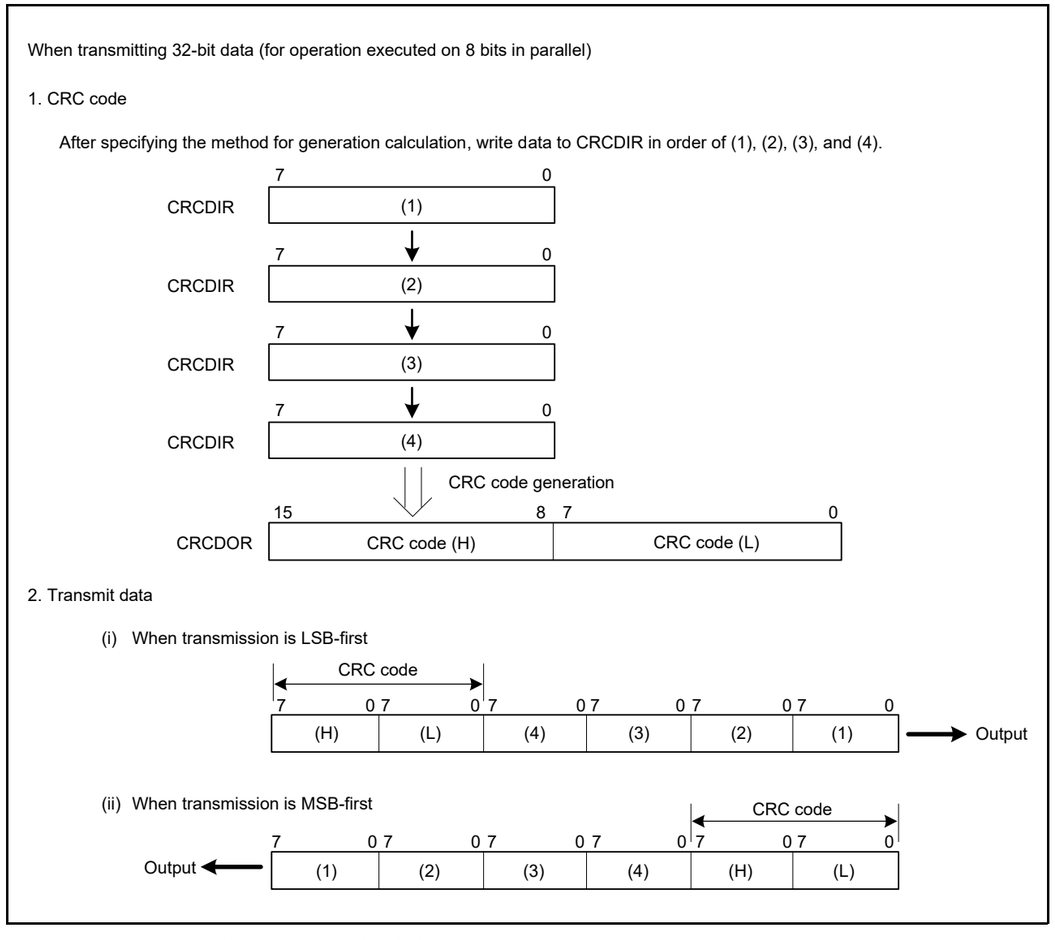


Figure 33.6 LSB-first and MSB-first data transmission

在CPU、DMA和DTC等总线主模块中的寄存器地址，CRC计算器将数据存储在CRCDIR_BY寄存器中并执行CRC计算。

每次执行1个字节的CRC计算。当以字（16位）或长字（32位）访问目标IO寄存器地址时，将在数据的低字节（1字节）上生成CRC码。

33.4 使用说明

33.4.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CRC计算器操作。CRC在复位后停止。释放模块停止状态后，寄存器变得可访问。有关详细信息，请参阅第11节，低功耗模式。

33.4.2 传输注意事项

CRC码的传输顺序根据传输是LSB在先还是MSB在先而有所不同。
图33.6显示了LSB优先和MSB优先的数据传输。

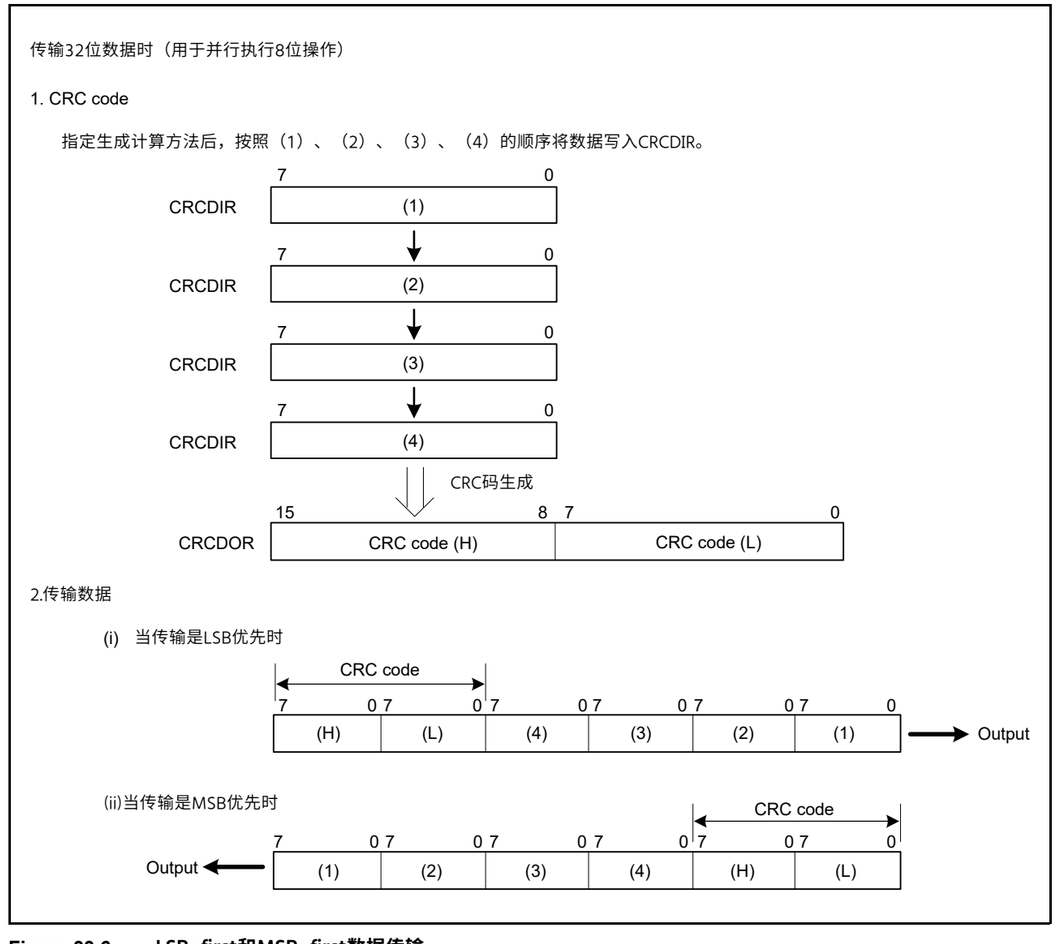


Figure 33.6 LSB−first和MSB−first数据传输

34. 14-Bit A/D Converter (ADC14)

34.1 Overview

The MCU provides a 14-bit successive approximation A/D converter (ADC14) unit. Up to 8 analog input channels are selectable. Temperature sensor output and internal reference voltage can be selected for conversion. The A/D conversion accuracy is 14-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

The ADC14 supports the following operating modes:

- Single scan mode to convert the analog inputs of arbitrarily selected channels in ascending order of channel number
- Continuous scan mode to sequentially convert the analog inputs of arbitrarily selected channels continuously in ascending order of channel number
- Group scan mode to arbitrarily divide the analog inputs of channels into two groups (group A and group B) and convert the analog input of the selected channel for each group in ascending order of channel number.

In group scan mode, you can start group A and group B A/D conversion at different times by individually selecting their scan start conditions. In addition, when a priority control operation for group A is set, the ADC14 accepts group A scan start during group B A/D conversion, suspending group B conversion. This allows you to assign higher priority to A/D conversion start for group A.

In double trigger mode, the analog input of an arbitrarily selected channel is converted in single scan mode or group scan mode (group A), and the data converted by the first and second A/D conversion start triggers are stored in different registers, providing duplexing of A/D-converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three voltage values generated in the ADC14 is A/D-converted.

The temperature sensor output and internal reference voltage cannot be selected for A/D conversion simultaneously. The temperature sensor output and the internal reference voltage are converted independently. If the internal reference voltage is selected as the reference voltage on the high-potential side, A/D conversion of the temperature sensor or the internal reference voltage is also prohibited.

The reference power supply pin (VREFH0), the analog block power supply pin (AVCC0), or the internal reference voltage is selectable as the reference voltage on the high-potential side. The reference power supply ground pin (VREFL0) or the analog block power supply ground pin (AVSS0) is selectable as the reference voltage on the low-potential side.

The ADC14 provides a compare function (window A and window B). This compare function specifies the upper reference value and lower reference value for window A and window B respectively, and outputs an interrupt when the A/D-converted value of the selected channel meets the comparison conditions.

Table 34.1 lists the ADC14 specifications, Table 34.2 lists the functions, and Figure 34.1 shows a block diagram. Table 34.2 lists the I/O pins.

Table 34.1 ADC14 specifications (1 of 3)

Parameter	Specifications
Number of units	One unit
Input channels	Up to 8 channels (AN004 to AN006, AN009, AN010, AN017, AN019, and AN020)
Extended analog function	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method
Resolution	14 bits, selectable to 14-bit or 12-bit conversion
Conversion time	0.79 µs/channel, when A/D conversion clock PCLKC (ADCLK) is operating at 64 MHz
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock PCLKC (ADCLK)*1 can be set with the following division ratios: PCLKB to PCLKC (ADCLK) frequency ratio = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4

34. 14-Bit A/D Converter (ADC14)

34.1 Overview

MCU提供一个14位逐次逼近模数转换器(ADC14)单元。最多可选择8个模拟输入通道。可选择温度传感器输出和内部参考电压进行转换。AD转换精度为14位转换，可以在生成数字值时优化速度和分辨率之间的权衡。

ADC14支持以下工作模式：

- 单次扫描模式，以通道号升序转换任意选择通道的模拟输入
- 连续扫描模式，以通道号升序连续转换任意选择通道的模拟输入
- 组扫描模式，将通道的模拟输入任意分成两组（A组和B组），并按通道编号升序对每组所选通道的模拟输入进行转换。

在组扫描模式下，您可以通过单独选择它们的扫描开始条件，在不同的时间开始A组和B组AD转换。此外，当设置了A组的优先控制操作时，ADC14在B组AD转换期间接受A组扫描开始，暂停B组转换。这允许您为A组的AD转换启动分配更高的优先级。

在双触发模式下，任意选择通道的模拟输入转换为单扫描模式或组扫描模式（A组），第一次和第二次A/D转换开始触发转换的数据存储在不同的寄存器中，提供双工一个D转换数据。

自诊断在每次扫描开始时执行一次，并在生成的三个电压值之一
ADC14 is A/D-converted.

AD转换不能同时选择温度传感器输出和内部参考电压。温度传感器输出和内部参考电压是独立转换的。如果选择内部参考电压作为高电位侧的参考电压，温度传感器或内部参考电压的AD转换也被禁止。

基准电源引脚(VREFH0)、模拟模块电源引脚(AVCC0)或内部基准电压可选择作为高电位侧的基准电压。参考电源接地引脚(VREFL0)或模拟模块电源接地引脚(AVSS0)可选择作为低电位侧的参考电压。

ADC14提供比较功能（窗口A和窗口B）。该比较函数分别指定窗口A和窗口B的上参考值和下参考值，并在所选通道的AD转换值满足比较条件时输出中断。

表34.1列出了ADC14的规格，表34.2列出了功能，图34.1显示了框图。表34.2列出了IO引脚。

Table 34.1 ADC14规格（1个，共3个）

Parameter	Specifications
单位数量	一个单位
输入通道	多达8个通道（AN004至AN006、AN009、AN010、AN017、AN019和AN020）
扩展模拟功能	温度传感器输出，内部参考电压
AD转换方式	逐次逼近法
Resolution	14位，可选择14位或12位转换
转换时间	0.79µs通道，当AD转换时钟PCLKC(ADCLK)以64MHz运行时
AD转换时钟	外围模块时钟PCLKB*1和AD转换时钟PCLKC(ADCLK)*1可以设置为以下分频比：PCLKB与PCLKC(ADCLK)频率比=1:1、2:1、4:1、8:1、1:2 1:4

Table 34.1 ADC14 specifications (2 of 3)

Parameter	Specifications
Data registers	• 8 registers for analog input: - One register for A/D-converted data duplication in double trigger mode - Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • A/D conversion results are stored in A/D data registers • 12-bit and 14-bit accuracy output for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D conversion results are stored in the A/D data registers as the conversion accuracy bit count + 2 bits*4 • Double trigger mode, selectable in single scan and group scan modes: - The first unit of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): - A/D-converted analog input data on one selected channel is stored in the duplication register provided for the associated trigger.
Operating modes	• Single scan mode: - A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, on the temperature sensor output, and on the internal reference voltage • Continuous scan mode: - A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, on the temperature sensor output, and on the internal reference voltage • Group scan mode: - A/D conversion is performed only once on the analog inputs of arbitrarily selected channels divided into group A and group B - The scan start conditions can be independently selected for group A and group B, allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): - If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B stops and A/D conversion is performed on group A - Restart (rescan) of group B conversion after completion of group A conversion can be set.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger from the Event Link Controller (ELC) • Asynchronous trigger from the external trigger pin, ADTRG0.
Function	• Variable sampling state count • Self-diagnosis of ADC14 • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double trigger mode (duplication of A/D conversion data) • Switching function for 12-bit and 14-bit conversion*2 • Automatic clear function for A/D data registers • Digital comparison of values in the comparison and data registers, and between values in the data registers.
Interrupt source	• In single scan mode (double-trigger deselected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of a single scan. - A compare interrupt request (ADC140_CMPAI/ADC140_CMPBI) can be generated in response to matches with a condition for digital comparison. - A window compare ELC event signal (ADC140_WCMPM) can be generated in response to matches with a condition for digital comparison. - A window compare ELC event signal (ADC140_WCMPUM) can be generated in response to mismatches with a condition for digital comparison. • In single scan mode (double-trigger selected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of two scans • In continuous scan mode, an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of all the selected channel scans • In group scan mode (double-trigger deselected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request for group B (ADC140_GBADI) can be generated on completion of group B scan • In group scan mode (double-trigger selected), an A/D scan end interrupt request and ELC event signal (ADC140_ADI) can be generated on completion of two group A scans, whereas an A/D scan end interrupt request for group B (ADC140_GBADI) can be generated on completion of group B scan • The ADC140_ADI, ADC140_GBADI, ADC140_WCMPM, and ADC140_WCMPUM can activate the DMA controller (DMAC) and the Data Transfer Controller (DTC).
ELC interface	Scan can be started by a trigger from the ELC

Table 34.1 ADC14规格（2个，共3个）

Parameter	Specifications
数据寄存器	8个用于模拟输入的寄存器： 一个寄存器用于双触发模式下的AD转换数据复制两个寄存器用于双触发模式下扩展操作期间的AD转换数据复制 1个用于温度传感器输出的寄存器 1个用于内部参考电压的寄存器 1个用于自诊断的寄存器 AD转换结果存储在AD数据寄存器中 AD转换结果的12位和14位精度输出 D转换值加法模式，其中所有AD转换结果的总和存储在AD数据寄存器中转换精度位数+2位*4 双触发模式，可选择单扫描和组扫描模式： 一个选定通道上的AD转换模拟输入数据的第一个单元存储在该通道的数据寄存器中，第二个单元存储在复制寄存器中。 双触发模式下的扩展操作（适用于特定触发）： 一个选定通道上的D转换模拟输入数据存储在为相关触发提供的复制寄存器中。
操作模式	单次扫描模式： D转换仅在任意选择通道的模拟输入、温度传感器输出和内部参考电压上执行一次 连续扫描模式： 对任意选择通道的模拟输入、温度传感器输出和内部参考电压重复执行D转换 组扫描模式： 任意选择通道的模拟输入只进行一次AD转换，分为A组和B组可以独立选择A组和B组的扫描开始条件，允许A组和B组的AD转换独立启动。 组扫描模式（当A组优先时）： 如果在B组的AD转换期间输入A组触发，则B组的AD转换停止，A组进行AD转换可以设置A组转换完成后B组转换的重新启动（重新扫描）。
AD转换开始的条件	软件触发 来自事件链接控制器(ELC)的同步触发 来自外部触发引脚ADTRG0的异步触发。
Function	可变采样状态计数 ADC14的自诊断 可选择AD转换值加法模式或平均模式 模拟输入断开检测功能（放电和预充电功能） 双触发模式（复制AD转换数据） 切换功能12位和14位转换*2 AD数据寄存器的自动清除功能 比较和数据寄存器中的值以及数据寄存器中的值之间的数字比较。
中断源	在单次扫描模式下（取消选择双触发），完成单次扫描后可以生成AD扫描结束中断请求和ELC事件信号(ADC140_ADI)。可以生成比较中断请求(ADC140_CMPAIADC140_CMPBI)以响应与数字比较条件的匹配。响应与数字比较条件的匹配，可以生成窗口比较ELC事件信号(ADC140_WCMPM)。响应与数字比较条件的不匹配，可以生成窗口比较ELC事件信号(ADC140_WCMPUM)。 在单次扫描模式下（选择双触发），在完成两次扫描后可以产生一个AD扫描结束中断请求和ELC事件信号（ADC140_ADI） 在连续扫描模式下，一个AD扫描结束中断请求和ELC事件信号（ADC140_ADI)可在所有选定通道扫描完成时生成 在组扫描模式下（取消选择双触发），在A组扫描完成时可生成AD扫描结束中断请求和ELC事件信号(ADC140_ADI)，而B组扫描完成时可产生B组的AD扫描结束中断请求(ADC140_GBADI) 在组扫描模式下（选择双触发），完成时可产生AD扫描结束中断请求和ELC事件信号(ADC140_ADI)两个A组扫描，而B组(ADC140_GBADI)的AD扫描结束中断请求可以在B组扫描完成时生成ADC140_ADI、ADC140_GBADI、ADC140_WCMPM和ADC140_WCMPUM可以激活DMA连续滚筒(DMAC)和数据传输控制器(DTC)。
ELC interface	扫描可以通过来自ELC的触发器启动

Table 34.1 ADC14 specifications (3 of 3)

Parameter	Specifications
Reference voltage	• VREFH0, AVCC0, or internal reference voltage is selectable as the high-potential reference voltage • VREFL0 or AVSS0 is selectable as the low-potential reference voltage.
Module-stop function	Module-stop state can be specified*3

Note: When selecting the temperature sensor output or the internal reference voltage, do not use continuous scan mode or group scan mode.
Note 1. Peripheral module clock PCLKB frequency is specified in the SCKDIVCR.PCKB[2:0] bits and A/D conversion clock ADCLK is specified in the SCKDIVCR.PCKC[2:0] bits. Maximum frequency of PCLKB is 32 MHz and maximum frequency of PCLKC (ADCLK) is 64 MHz.
Note 2. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 34.3.6, Analog Input Sampling and Scan Conversion Time.
Note 3. For details, see section 11, Low Power Modes.
Note 4. The number of extended bits for addition varies with the A/D conversion accuracy and the number of addition times. A 2-bit extension is up to 4 times conversion (3 times addition) when the A/D conversion accuracy is 12 or 14 bits.

Table 34.2 ADC14 functions

Parameter			ADC140
Analog input channel			AN004 to AN006, AN009, AN010, AN017, AN019, and AN020 Internal reference voltage Temperature sensor output
Conditions for A/D conversion start	External trigger	Trigger input pin	ADTRG0
	Software	Software trigger	Enabled
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00 ELC_AD01
Interrupt			ADC140_ADI ADC140_GBADI ADC140_CMPAI ADC140_CMPBI
Output to ELC			ADC140_ADI ADC140_WCMPM ADC140_WCMPUM
Setting of module-stop function*1, *2			MSTPCRD.MSTPD16 bit

Note 1. For details, see section 11, Low Power Modes.
Note 2. Wait for 1 µs or longer to start A/D conversion after release from the module-stop state.

Table 34.1 ADC14规格（3之3）

Parameter	Specifications
参考电压	VREFH0、AVCC0或内部参考电压可选择作为高电位参考电压 VREFL0或AVSS0可选择作为低电位参考电压。
Module-stop function	可指定模块停止状态*3

Note: 选择温度传感器输出或内部参考电压时，请勿使用连续扫描模式或组扫描模式。
Note 1. 外围模块时钟PCLKB频率在SCKDIVCR.PCKB[2:0]位中指定，AD转换时钟ADCLK在SCKDIVCR.PCKC[2:0]位中指定。PCLKB的最大频率为32MHz，PCLKC(ADCLK)的最大频率为64MHz。
Note 2. 改变AD转换精度也会改变AD转换时间。有关详细信息，请参阅第34.3.6节，模拟输入采样和扫描转换时间。
Note 3. 有关详细信息，请参阅第11节，低功耗模式。
Note 4. 加法的扩展位数随AD转换精度和加法次数而变化。当AD转换精度为12或14位时，2位扩展最多可进行4次转换（3次加法）。

Table 34.2 ADC14 functions

Parameter			ADC140
模拟输入通道			AN004至AN006、AN009、AN010、AN017、AN019和AN020内部参考电压 温度传感器输出
AD转换开始的条件	外部触发	触发输入引脚	ADTRG0
	Software	软件触发	Enabled
	同步触发（来自ELC的触发）	ELC trigger	ELC_AD00 ELC_AD01
Interrupt			ADC140_ADI ADC140_GBADI ADC140_CMPAI ADC140_CMPBI
输出到ELC			ADC140_ADI ADC140_WCMPM ADC140_WCMPUM
模块停止功能设置*1 *2			MSTPCRD.MSTPD16 bit

Note 1. 有关详细信息，请参阅第11节，低功耗模式。
Note 2. 从模块停止状态释放后，等待1µs或更长时间开始AD转换。

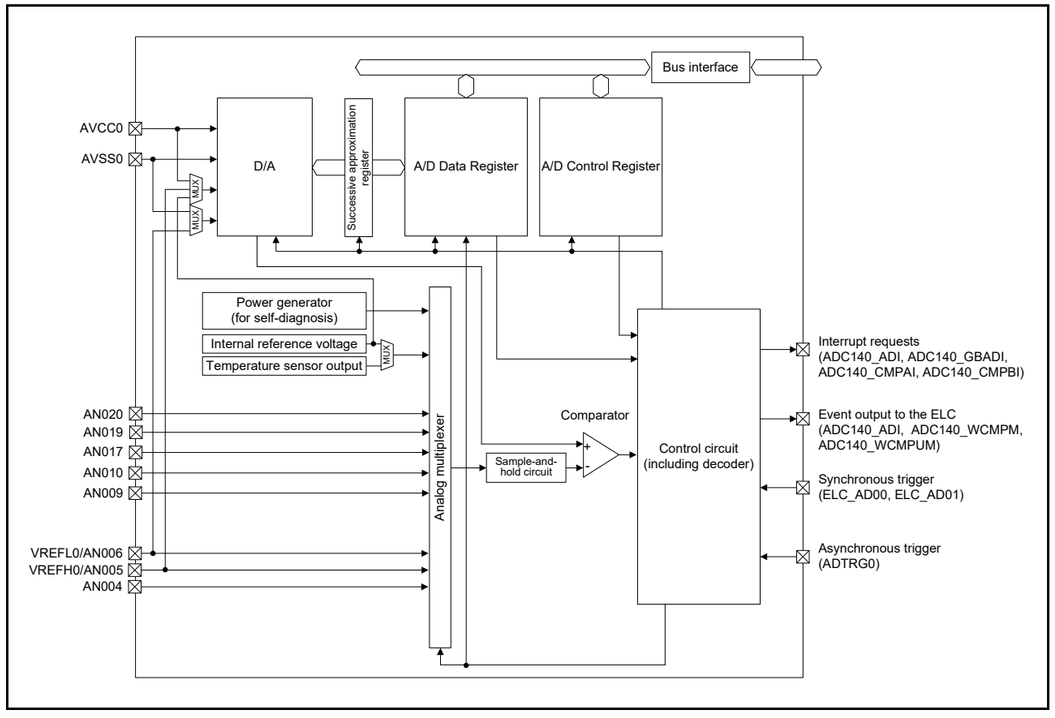


Figure 34.1 ADC14 block diagram

Table 34.3 ADC14 I/O pins

Unit	Pin name	I/O	Function
Unit 0	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
	AN004 to AN006, AN009, AN010, AN017, AN019, and AN020	Input	Analog input pins 4 to 6, 9, 10, 17, 19, and 20
	ADTRG0	Input	External trigger input pin for starting A/D conversion

34.2 Register Descriptions

34.2.1 A/D Data Registers y (ADDRy), A/D Data Duplexing Register (ADDBLDR), A/D Data Duplexing Register A (ADDBLDRA), A/D Data Duplexing Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR), A/D Internal Reference Voltage Data Register (ADOCDR)

The data registers include:

- ADDRy registers (y = 4 to 6, 9, 10, 17, 19, and 20): 16-bit read-only registers for storing the A/D conversion results
- ADDBLDR: 16-bit read-only register for storing the A/D conversion results in response to the second trigger in double trigger mode

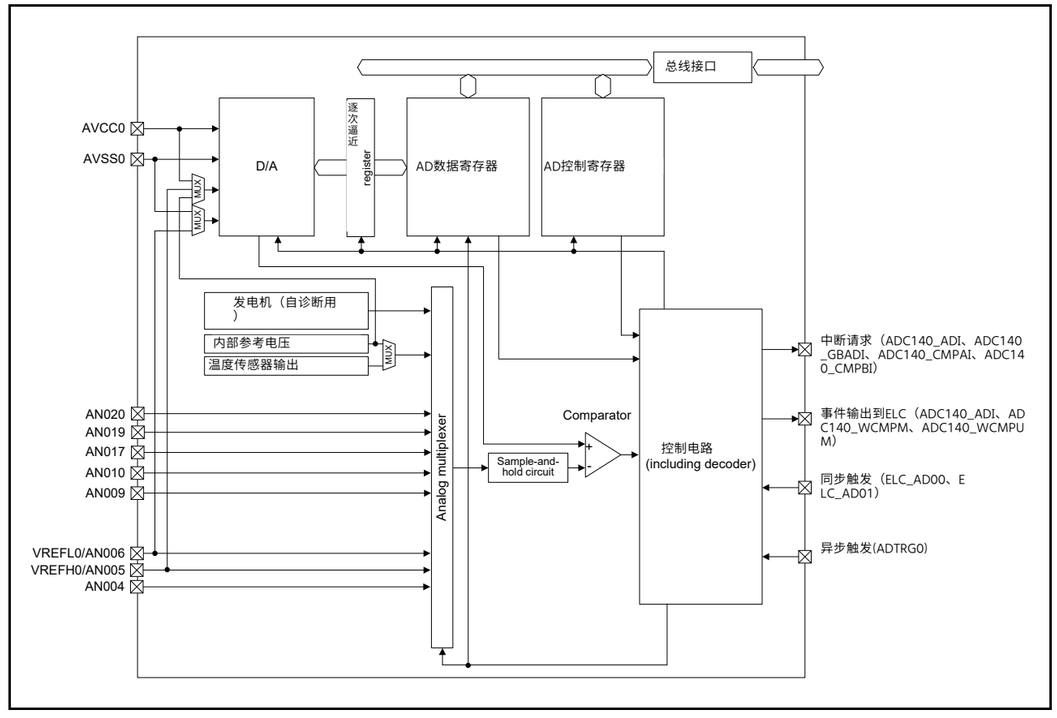


Figure 34.1 ADC14框图

Table 34.3 ADC14 I/O pins

Unit	引脚名称	I/O	Function
Unit 0	AVCC0	Input	模拟模块电源引脚
	AVSS0	Input	模拟模块电源接地引脚
	VREFH0	Input	参考电源引脚
	VREFL0	Input	参考电源接地引脚
	AN004 to AN006, AN009, AN010, AN017, AN019, and AN020	Input	模拟输入引脚4至6、9、10、17、19和20
	ADTRG0	Input	用于启动AD转换的外部触发输入引脚

34.2 注册说明

34.2.1 AD数据寄存器y(ADDRy)、AD数据双工寄存器(ADDBLDR)、AD数据双工寄存器A(ADDBLDRA) AD数据双工寄存器B(ADDBLDRB) AD温度传感器数据寄存器(ADTSDR) AD内部参考电压数据寄存器(ADOCDR)

数据寄存器包括：

- ADDRy寄存器（y=4到6、9、10、17、19和20）：用于存储AD转换结果的16位只读寄存器
- ADDBLDR：16位只读寄存器，用于存储双触发模式下第二次触发的A/D转换结果

- ADDBLDRA and ADDBLDRB: 16-bit read-only registers for storing the A/D conversion results in response to the respective triggers during extended operation in double trigger mode
- ADTSDR: 16-bit read-only register for storing the A/D conversion result of temperature sensor output
- ADOCDR: 16-bit read-only register for storing the A/D result of internal reference voltage.

The following conditions determine the formats for data in these registers:

- The setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right setting)
- The setting in the A/D Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (12-bit or 14-bit setting)
- The setting in the addition/average Count Select bits (ADADC.ADC[2:0]) (once, twice, thrice, four times, or 16 times setting)
- The setting in the Average Mode Enable bit (ADADC.AVEE) (addition or average setting).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

The data formats for each condition are as follows:

Settings for flush-right data with 14-bit accuracy

Address(es): ADC140.ADDR4 4005 C028h to ADC140.ADDR6 4005 C02Ch, ADC140.ADDR9 4005 C032h, ADC140.ADDR10 4005 C034h, ADC140.ADDR17 4005 C042h, ADC140.ADDR19 4005 C046h, ADC140.ADDR20 4005 C048h, ADC140.ADDBLDR 4005 C018h, ADC140.ADDBLDRA 4005 C084h, ADC140.ADDBLDRB 4005 C086h, ADC140.ADTSDR 4005 C01Ah, ADC140.ADOCDR 4005 C01Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AD[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R
b15, b14	—	Reserved	These bits are read as 0	R

Settings for flush-right data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	These bits are read as 0	R

- ADDBLDRA和ADDBLDRB：16位只读寄存器，用于存储双触发模式下扩展操作期间响应各自触发的AD转换结果
- ATSDR：16位只读寄存器，用于存储温度传感器输出的A/D转换结果
- AOCDR：16位只读寄存器，用于存储内部参考电压的AD结果。

以下条件决定了这些寄存器中数据的格式：

- AD数据寄存器格式选择位(ADCER.ADRFMT)中的设置（左对齐或右对齐设置）
- AD转换精度指定位(ADCER.ADPRC[1:0])中的设置（12位或14位设置）
- 加法平均计数选择位(ADADC.ADC[2:0])中的设置（一次、两次、三次、四次或16次设置）
- 平均模式启用位(ADADC.AVEE)中的设置（加法或平均设置）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

每个条件的数据格式如下：

具有14位精度的刷新右数据设置

Address(es): ADC140.ADDR4 4005 C028h to ADC140.ADDR6 4005 C02Ch, ADC140.ADDR9 4005 C032h, ADC140.ADDR10 4005 C034h, ADC140.ADDR17 4005 C042h, ADC140.ADDR19 4005 C046h, ADC140.ADDR20 4005 C048h, ADC140.ADDBLDR 4005 C018h, ADC140.ADDBLDRA 4005 C084h, ADC140.ADDBLDRB 4005 C086h, ADC140.ADTSDR 4005 C01Ah, ADC140.ADOCDR 4005 C01Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AD[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

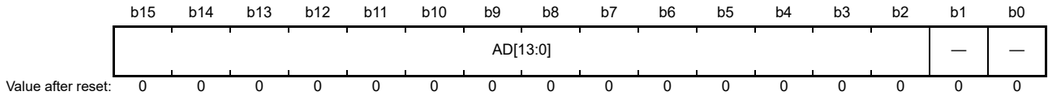
Bit	Symbol	位名称	Description	R/W
b13 to b0	AD[13:0]	将值13转换为0	14-bit A/D-converted value	R
b15, b14	—	Reserved	这些位被读为0	R

具有12位精度的右冲洗数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

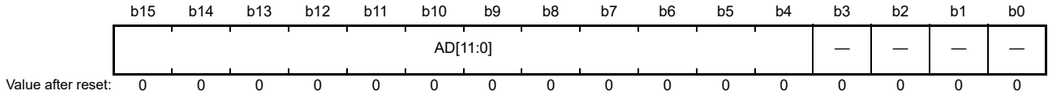
Bit	Symbol	位名称	Description	R/W
b11 to b0	AD[11:0]	将值11转换为0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	这些位被读为0	R

Settings for flush-left data with 14-bit accuracy



Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0	R
b15 to b2	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R

Settings for flush-left data with 12-bit accuracy



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value average mode. When the A/D-converted value average mode is selected, this register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting in the A/D Data Register Format Select bit in the same way as in normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit or 14-bit accuracy (ADPRC bit setting), 1, 2, 3, or 4 times can be selected for A/D -converted value addition. 16 times can also be selected, but only with 12-bit accuracy selected.

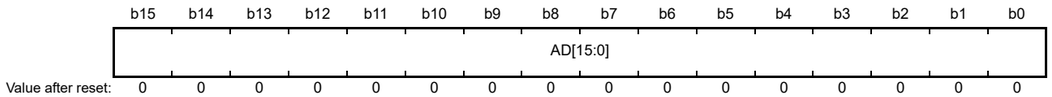
In addition mode, this register indicates the value that is obtained by adding up A/D-converted values on a specific channel. The value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

When converting 1, 2, 3, or 4 times in addition mode with 12-bit or 14-bit accuracy, the conversion result is stored in the A/D data register as a 2-bit extended value of the specified accuracy.

When converting 16 times in addition mode with 12-bit accuracy, the A/D conversion result is stored in the A/D data register as a 4-bit-extended value of the specified accuracy.

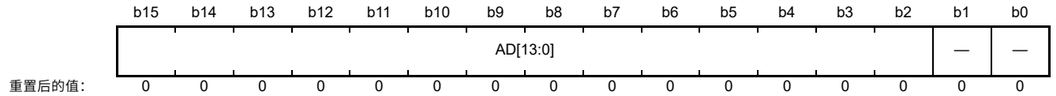
The data formats for each given condition are shown below.

Settings for flush-right data with 14-bit accuracy in A/D-converted value addition mode



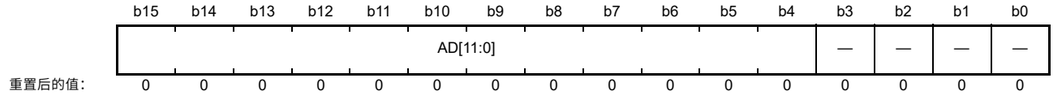
Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]	Added Value 15 to 0	16-bit value obtained by adding the A/D conversion results	R

具有14位精度的左对齐数据的设置



Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读为0	R
b15 to b2	AD[13:0]	将值13转换为0	14-bit A/D-converted value	R

具有12位精度的左对齐数据的设置



Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读为0	R
b15 to b4	AD[11:0]	将值11转换为0	12-bit A/D-converted value	R

(2) 选择AD转换值平均模式时

当在AD转换值平均模式中指定2次或4次时，可以选择D转换值平均模式。WhentheAD-convertedvalueaverag emodeisselected thisregisterindicatesthemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位中的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位或14位精度（ADPRC位设置），可以选择1、2、3或4次用于AD转换值相加。也可以选择16次，但只能选择12位精度。

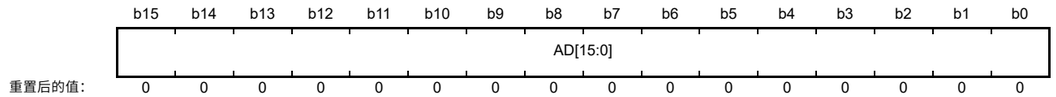
在加法模式下，该寄存器指示通过将特定通道上的AD转换值相加而获得的值。该值根据AD数据寄存器格式选择位的设置存储在AD数据寄存器中。

在加法模式下以12位或14位精度转换1、2、3或4次时，转换结果存储在
作为指定精度的2位扩展值的D数据寄存器。

当以12位精度在加法模式下转换16次时，AD转换结果作为指定精度的4位扩展值存储在AD数据寄存器中。

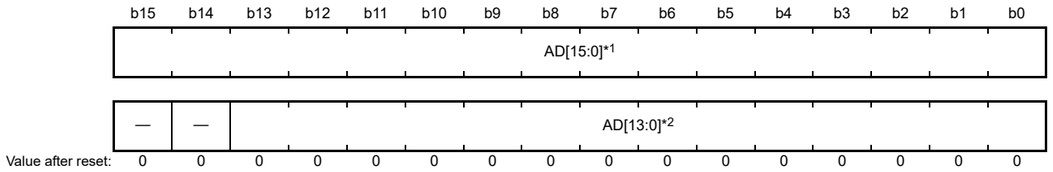
每个给定条件的数据格式如下所示。

在AD转换值相加模式中以14位精度设置右对齐数据



Bit	Symbol	位名称	Description	R/W
b15 to b0	AD[15:0]	附加值15到0	将AD转换结果相加得到的16位值	R

Settings for flush-right data with 12-bit accuracy in A/D-converted value addition mode

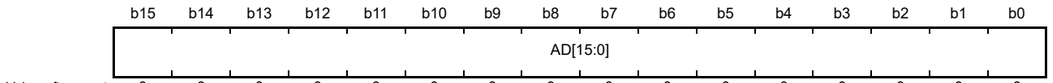


Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16-bit value obtained by adding the A/D conversion results	R

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]*2	Added Value 13 to 0	14-bit value obtained by adding the A/D conversion results	R
b15, b14	—	Reserved	These bits are read as 0	R

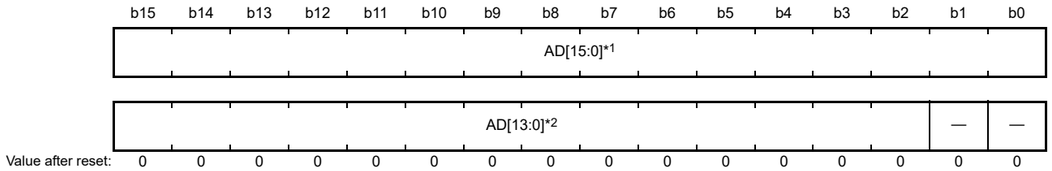
Note 1. Used when 16 conversion times is specified in A/D-converted value addition mode.
Note 2. Used when 1, 2, 3, or 4 conversion times is specified in A/D-converted value addition mode.

Settings for flush-left data with 14-bit accuracy in A/D-converted value addition mode



Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]	Added Value 15 to 0	16-bit value obtained by adding the A/D conversion results	R

Settings for flush-left data with 12-bit accuracy in A/D-converted value addition mode

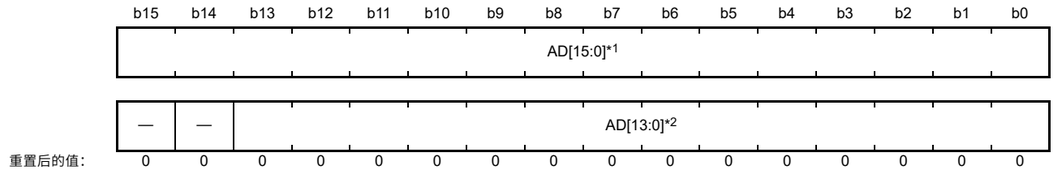


Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16-bit value obtained by adding the A/D conversion results	R

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0	R
b15 to b2	AD[13:0]*2	Added Value 13 to 0	14-bit value obtained by adding the A/D conversion results	R

Note 1. Used when 16 conversion times is specified in A/D-converted value addition mode.
Note 2. Used when 1, 2, 3, or 4 conversion times is specified in A/D-converted value in addition mode.

在AD转换值相加模式下以12位精度设置刷新数据

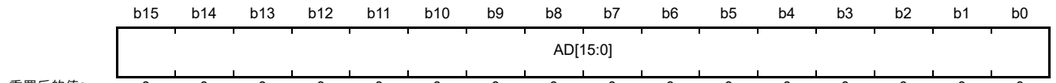


Bit	Symbol	位名称	Description	R/W
b15 to b0	AD[15:0]*1	附加值15到0	将AD转换结果相加得到的16位值	R

Bit	Symbol	位名称	Description	R/W
b13 to b0	AD[13:0]*2	附加值13到0	将AD转换结果相加得到的14位值	R
b15, b14	—	Reserved	这些位被读为0	R

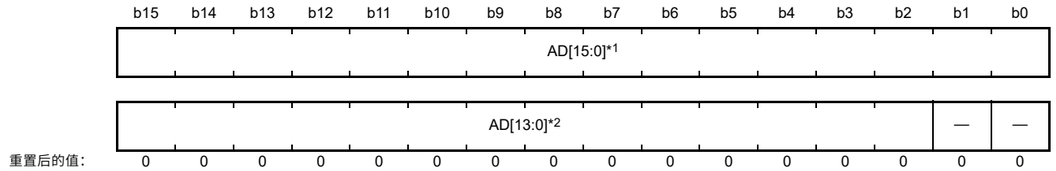
Note 1. 在AD转换值加法模式中指定16次转换时使用。
Note 2. 在AD转换值相加模式中指定1、2、3或4转换时间时使用。

AD转换值加法模式下14位精度的左对齐数据的设置



Bit	Symbol	位名称	Description	R/W
b15 to b0	AD[15:0]	附加值15到0	将AD转换结果相加得到的16位值	R

AD转换值相加模式下12位精度的左对齐数据的设置



Bit	Symbol	位名称	Description	R/W
b15 to b0	AD[15:0]*1	附加值15到0	将AD转换结果相加得到的16位值	R

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读为0	R
b15 to b2	AD[13:0]*2	附加值13到0	将AD转换结果相加得到的14位值	R

Note 1. 在AD转换值加法模式中指定16次转换时使用。
Note 2. 在加法模式下的AD转换值中指定1、2、3或4转换时间时使用。

34.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of ADC14. In addition to the AD[13:0] bits indicating the A/D-converted value, it includes the Self-Diagnosis Status bit (DIAGST).

The following conditions determine the format for data in this register:

- The setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right setting)
- The setting in the A/D Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (12-bit or 14-bit setting).

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 34.2.11, A/D Control Extended Register (ADCER).

This section describes the data formats for each condition.

Settings for flush-right data with 14-bit accuracy

Address(es): ADC140.ADRD 4005 C01Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		AD[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details of self-diagnosis, see section 34.2.11, A/D Control Extended Register (ADCER).	R

Note 1. Reference voltage refers to VREFH0.

Settings for flush-right data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b13, b12	—	Reserved	These bits are read as 0	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details of self-diagnosis, see section 34.2.11, A/D Control Extended Register (ADCER).	R

Note 1. Reference voltage refers to VREFH0.

34.2.2 AD自诊断数据寄存器(ADRD)

ADRD是一个16位只读寄存器，用于保存基于ADC14自诊断的AD转换结果。除了指示AD转换值的AD[13:0]位外，它还包括自诊断状态位(DIAGST)。

以下条件决定了该寄存器中数据的格式：

- AD数据寄存器格式选择位(ADCER.ADRFMT)中的设置（左对齐或右对齐设置）
- AD转换精度指定位(ADCER.ADPRC[1:0])中的设置（12位或14位设置）。

AD转换值加法和平均模式不能应用于AD自诊断功能。有关自诊断的详细信息，请参见第34.2.11节，AD控制扩展寄存器(ADCER)。

本节介绍每个条件的数据格式。

具有14位精度的刷新右数据设置

Address(es): ADC140.ADRD 4005 C01Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		AD[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	AD[13:0]	将值13转换为0	14-bit A/D-converted value	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15b1400：上电后未执行自诊断01：使用0V电压执行自诊断10：使用参考电源电压执行自诊断*1×1211：使用基准电源电压*1执行自诊断。有关自诊断的详细信息，请参阅第34.2.11节，AD控制扩展寄存器(ADCER)。	R

Note 1. 参考电压是指VREFH0。

具有12位精度的右冲洗数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b11 to b0	AD[11:0]	将值11转换为0	12-bit A/D-converted value	R
b13, b12	—	Reserved	这些位被读为0	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15b1400：上电后未执行自诊断01：使用0V电压执行自诊断10：使用参考电源电压执行自诊断*1×1211：使用基准电源电压*1执行自诊断。有关自诊断的详细信息，请参阅第34.2.11节，AD控制扩展寄存器(ADCER)。	R

Note 1. 参考电压是指VREFH0。

Settings for flush-left data with 14-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[13:0]														DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details of self-diagnosis, see section 34.2.11, A/D Control Extended Register (ADCER).	R
b15 to b2	AD[13:0]	Converted Value 13 to 0	14-bit A/D-converted value	R

Note 1. Reference voltage refers to VREFH0.

Settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has not been executed since power-on 0 1: Self-diagnosis was executed using the voltage of 0 V 1 0: Self-diagnosis was executed using the voltage of reference power supply*1 × 1/2 1 1: Self-diagnosis was executed using the voltage of reference power supply*1. For details on self-diagnosis, see section 34.2.11, A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

Note 1. Reference voltage refers to VREFH0.

34.2.3 A/D Control Register (ADCSR)

Address(es): ADC140.ADCSR 4005 C000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		—	—	ADHSC	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DBLANS[4:0]	Double Trigger Channel Select	These bits select one analog input channel for double-triggered operation. The setting is only valid in double trigger mode.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

具有14位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[13:0]														DIAGST[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1b000：上电后未执行自诊断01：使用0V电压执行自诊断10：使用参考电源电压执行自诊断*1×1211：使用基准电源电压*1执行自诊断。有关自诊断的详细信息，请参阅第34.2.11节，AD控制扩展寄存器(ADCER)。	R
b15 to b2	AD[13:0]	将值13转换为0	14-bit A/D-converted value	R

Note 1. 参考电压是指VREFH0。

具有12位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1b000：上电后未执行自诊断01：使用0V电压执行自诊断10：使用参考电源电压执行自诊断*1×1211：使用基准电源电压*1执行自诊断。有关自诊断的详细信息，请参阅第34.2.11节，AD控制扩展寄存器(ADCER)。	R
b3, b2	—	Reserved	这些位被读为0	R
b15 to b4	AD[11:0]	将值11转换为0	12-bit A/D-converted value	R

Note 1. 参考电压是指VREFH0。

34.2.3 AD控制寄存器(ADCSR)

Address(es): ADC140.ADCSR 4005 C000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		—	—	ADHSC	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DBLANS[4:0]	双触发通道Select	这些位选择一个模拟输入通道进行双触发操作。该设置仅在双触发模式下有效。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	GBADIE	Group B Scan End Interrupt Enable	0: Disable ADC140_GBADI interrupt generation on group B scan completion 1: Enable ADC140_GBADI interrupt generation on group B scan completion. Group B scan works only in group scan mode.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselect double trigger mode 1: Select double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: A/D conversion is started by a synchronous trigger (ELC) 1: A/D conversion is started by an asynchronous trigger (ADTRG0).	R/W
b9	TRGE	Trigger Start Enable	0: Disable A/D conversion to be started by a synchronous or asynchronous trigger 1: Enable A/D conversion to be started by a synchronous or asynchronous trigger.	R/W
b10	ADHSC	A/D Conversion Mode Select	0: High-speed A/D conversion mode 1: Low-power A/D conversion mode.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.	R/W
b15	ADST	A/D Conversion Start	0: Stop A/D conversion process 1: Start A/D conversion process.	R/W

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0), write 1 to both the TRGE and EXTRG bits in the ADCSR register and drive the ADTRG0 signal low. With these settings, the scan conversion process starts on detection of the falling edge of ADTRG0. For this configuration, the pulse width of the low-level input must be at least 1.5 clock PCLKB cycles.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results from the specified analog input channel are stored in the A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when started by the second trigger. Table 34.4 shows selection of the channel for double-triggered operation.

In double trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers are invalid, and the channel selected in the DBLANS[4:0] bits is A/D-converted instead.

When double trigger mode is used in group scan mode, double-trigger control is applied only to group A and not to group B. This means that multi-channel analog input can be selected for group B even in double trigger mode.

Only set the DBLANS[4:0] bits when the ADST bit is 0. Do not set these bits at the same time you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double trigger mode, select the channel using the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

Table 34.4 Relationship between DBLANS bit settings and double-trigger enabled channels

DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
00100	AN004	10001	AN017
00101	AN005	10011	AN019
00110	AN006	10100	AN020
01001	AN009		
01010	AN010		

Note: A/D-converted data from the self-diagnosis function, temperature sensor output, and internal reference voltage cannot be used in double trigger mode.

Bit	Symbol	位名称	Description	R/W
b6	GBADIE	B组扫描结束中断使能	0：在B组扫描完成时禁用ADC140_GBADI中断生成1：在B组扫描完成时启用ADC140_GBADI中断生成。B组扫描仅在组扫描模式下工作。	R/W
b7	DBLE	双触发模式 Select	0：取消选择双触发模式1：选择双触发模式。	R/W
b8	EXTRG	触发选择 *1	0：由同步触发(ELC)启动AD转换1：由异步触发(ADTRG0)启动AD转换。	R/W
b9	TRGE	触发启动启用	0：禁止由同步或异步触发启动AD转换1：使能由同步或异步触发启动AD转换。	R/W
b10	ADHSC	AD转换模式 Select	0：高速模数转换模式1：低功耗模数转换模式。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14, b13	ADCS[1:0]	扫描模式选择	b14b1300：单次扫描模式0 1：组扫描模式10：连续扫描模式11：禁止设置。	R/W
b15	ADST	AD转换开始	0：停止AD转换过程1：开始AD转换过程。	R/W

Note 1. 使用外部引脚（异步触发）启动AD转换：
在向外部引脚（ADTRG0）输入高电平信号后，将1写入ADCSR寄存器的TRGE和EXTRG位，并将ADTRG0信号驱动为低电平。通过这些设置，扫描转换过程在检测到ADTRG0的下降沿时开始。对于这种配置，低电平输入的脉冲宽度必须至少为1.5个时钟PCLKB周期。

DBLANS[4:0]位（双触发通道选择）

DBLANS[4:0]位选择通道之一，用于双触发模式下的AD转换数据复制。指定模拟输入通道的AD转换结果在第一次触发开始转换时存储在AD数据寄存器y中，在第二次触发开始时存储在AD数据双工寄存器中。表34.4显示了双触发操作的通道选择。

在双触发模式下，ADANSA0和ADANSA1寄存器中选择的通道无效，DBLANS[4:0]位中选择的通道改为AD转换。

在组扫描模式下使用双触发模式时，双触发控制仅适用于A组，不适用于组B.这意味着即使在双触发模式下，也可以为B组选择多通道模拟输入。

仅当ADST位为0时设置DBLANS[4:0]位。不要在将1写入ADST位的同时设置这些位。

要在双触发模式下进入AD转换值加法平均模式，请使用ADANSA0和ADANSA1寄存器中的DBLANS[4:0]位。

Table 34.4 DBLANS位设置与双触发启用通道之间的关系

DBLANS[4:0]	复制通道	DBLANS[4:0]	复制通道
00100	AN004	10001	AN017
00101	AN005	10011	AN019
00110	AN006	10100	AN020
01001	AN009		
01010	AN010		

Note: 自诊断功能、温度传感器输出和内部参考电压的D转换数据不能用于双触发模式。

GBADIE bit (Group B Scan End Interrupt Enable)

The GBADIE bit enables or disables group B scan end interrupt (ADC140_GBADI) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double trigger mode. Double trigger mode can only be operated by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits.

Double trigger mode operates as follows:

- The ADC140_ADI interrupt is not output on completion of the first conversion but on completion of the second conversion
- The A/D conversion results from the duplication channel (selected in the DBLANS[4:0] bits) started by the first trigger are stored in the A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplication Register.

When DBLE is set (double trigger mode is selected), the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Do not select double trigger mode in continuous scan mode.

Software triggering cannot be used in double trigger mode. Always set the ADST bit to 0 before setting the DBLE bit. In other words, do not set this bit at the same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or asynchronous trigger as the trigger for starting A/D conversion.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous and asynchronous triggers. Set this bit to 1 in group scan mode.

ADHSC bit (A/D Conversion Mode Select)

The ADHSC bit selects either the high-speed or low-current mode for A/D conversion.

For details on how to rewrite this bit, see section 34.8.8, ADHSC Bit Rewriting Procedure.

ADCS[1:0] bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs selected in the ADANSA0 and ADANSA1 registers in ascending order of channel number, for a maximum of 8 channels. When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output or internal reference voltage, in that order.

In continuous scan mode, when the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs selected in the ADANSA0 and ADANSA1 registers in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion is repeated from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion stops even when scanning is in progress. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output or internal reference voltage, in that order.

In group scan mode:

- Group A scanning is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits. A/D conversion is performed on group A analog inputs, up to the maximum number of 8 channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.
- Group B scanning is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits. A/D conversion is performed on group B analog inputs, up to the maximum number of 8 channels selected in the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, conversion stops.

GBADIE位（B组扫描结束中断使能）

GBADIE位在组扫描模式下启用或禁用组B扫描结束中断(ADC140_GBADI)。

DBLE位（双触发模式选择）

DBLE位选择或取消选择双触发模式。双触发模式只能通过在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)操作。

双触发模式操作如下：

- ADC140_ADI中断不是在第一次转换完成时输出，而是在第二次转换完成时输出
- 由第一次触发启动的复制通道（在DBLANS[4:0]位中选择）的AD转换结果存储在AD数据寄存器y中，而由第二次触发启动的数据存储在AD数据复制寄存器中。

设置DBLE时（选择双触发模式），ADANSA0和ADANSA1寄存器中指定的通道无效。在连续扫描模式下不要选择双触发模式。

双触发模式下不能使用软件触发。在设置DBLE位之前，始终将ADST位设置为0。换言之，不要在将1写入ADST位的同时设置该位。

EXTRG位（触发选择）

EXTRG位选择同步触发或异步触发作为启动AD转换的触发。

TRGE位（触发启动使能）

TRGE位通过同步和异步触发启用或禁用AD转换。在组扫描模式下将此位设置为1。

ADHSC位（AD转换模式选择）

ADHSC位选择高速或低电流模式进行AD转换。

有关如何重写该位的详细信息，请参见第34.8.8节，ADHSC位重写过程。

ADCS[1:0]位（扫描模式选择）

ADCS[1:0]位选择扫描模式。

在单次扫描模式下，ADANSA0和ADANSA1寄存器中选择的模拟输入按通道编号升序执行AD转换，最多8个通道。当所有选定通道的1个AD转换周期完成时，扫描转换停止。Whenthetemperaturesensoroutputorinternalreferencevoltageisselected ADconversionofthedesignatedanaloginputchannelsisfollowedbyADconversionofthetemperaturesensoroutputorinternalreferencevoltage inthatorder.

在连续扫描模式下，当ADCSR.ADST位为1时，ADANSA0和ADANSA1寄存器中选择的模拟输入按通道编号升序执行AD转换。当所有选定通道的1个AD转换周期完成时，从第一个通道开始重复AD转换。如果在连续扫描期间将ADCSR.ADST位设置为0，则即使在扫描过程中AD转换也会停止。Whenthetemperaturesensoroutputorinternalreferencevoltageisselected ADconversionofthedesignatedanaloginputchannelsisfollowedbyADconversionofthetemperaturesensoroutputorinternalreferencevoltage inthatorder.

在组扫描模式下：

- A组扫描由在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)启动。AD转换在A组模拟输入上执行，最多可在ADANSA0和ADANSA1寄存器中选择最多8个通道，按通道编号升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。
- B组扫描由在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)启动。对B组模拟输入执行AD转换，最多可在ADANSB0和ADANSB1寄存器中选择8个通道，按通道编号升序排列。当所有选定通道的1个AD转换周期完成时，转换停止。

If the conversion processes in group A and B occur at the same time, those conversions cannot be controlled separately. In this case, set the Group A Priority Control Setting bit (ADGSPCR.PGS) in the A/D Group Scan Priority Control Register (ADGSPCR) to 1, to assign priority to group A conversion.

In group scan mode, select different channels and triggers for group A and group B.

When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

Set the ADST bit to 0 before setting the ADCS[1:0] bits. In other words, do not set both the ADCS[1:0] and ADST bits to 1 at the same time.

Table 34.5 Selectable targets for A/D conversion based on scan mode and double trigger mode settings

Scan mode setting	Double trigger mode setting	Targets for A/D conversion				
		Self-diagnosis	Analog input (including group A)	Analog input (group B)	Temperature sensor output	Internal reference voltage
Single scan	DBLE = 0	✓	✓	×	✓	✓
	DBLE = 1	×	✓ (1 ch only)	×	×	×
Continuous scan	DBLE = 0	✓	✓	×	×	×
	DBLE = 1	×	×	×	×	×
Group scan	DBLE = 0	✓	✓	✓	×	×
	DBLE = 1	×	✓ (1 ch only)	✓	×	×

✓: Selectable. ×: Not selectable.

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and analog inputs to be converted.

[Setting conditions]

- On writing 1 through software
- When the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when ADCSR.EXTRG is 0 and ADCSR.TRGE is 1
- When the synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when ADCSR.TRGE is set to 1 in group scan mode
- When the asynchronous trigger is detected while the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1, and the ADSTRGR.TRSA[5:0] bits are set to 000000b
- When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and each time A/D conversion of group B starts.

如果A组和B组中的转换过程同时发生，则不能单独控制这些转换。
在这种情况下，设置AD组扫描优先级控制中的组A优先级控制设置位(ADGSPCR.PGS)寄存器(ADGSPCR)为1，为A组转换分配优先级。

在组扫描模式下，为A组和B组选择不同的通道和触发。

WhenthetemperaturesensoroutputorinternalreferencevoltageisselectedADconversionofthedesignatedanalo ginputchannelsisfollowedbyADconversionofthetemperaturesensoroutputandtheinternalreferencevoltage int hatorder.

在设置ADCS[1:0]位之前将ADST位设置为0。换言之，不要同时将ADCS[1:0]和ADST位设置为1。

Table 34.5 基于扫描模式和双触发模式设置的AD转换可选目标

扫描模式设置	双触发模式设置	AD转换的目标				
		Self-diagnosis	模拟量输入（包括A组）	模拟输入（B组）	温度传感器输出	内部参考电压
单次扫描	DBLE = 0	✓	✓	×	✓	✓
	DBLE = 1	×	✓ (1 ch only)	×	×	×
连续扫描	DBLE = 0	✓	✓	×	×	×
	DBLE = 1	×	×	×	×	×
组扫描	DBLE = 0	✓	✓	✓	×	×
	DBLE = 1	×	✓ (1 ch only)	✓	×	×

：可选择。×：不可选择。

ADST位（AD转换开始）

ADST位启动或停止AD转换过程。在ADST位设置为1之前，设置AD转换时钟、转换模式和要转换的模拟输入。

[Setting conditions]

- 关于通过软件写1
- 当ADCSR.EXTRG为0且ADCSR.TRGE为1时检测到ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)
- 当在组扫描模式下ADCSR.TRGE设置为1时检测到在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)
- 当ADCSR.TRGE和ADCSR.EXTRG位设置为1时检测到异步触发，并且ADSTRGR.TRSA[5:0]位设置为000000b
- 当A组优先控制操作模式使能时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRP位设置为1，并且每次B组的AD转换开始。

[Clearing conditions]

- When 0 is written by software
- When the A/D conversion of all the selected channels, the temperature sensor output, or the internal reference voltage completes in single scan mode
- When group A scan completes in group scan mode
- When group B scan completes in group scan mode
- When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and each time a scanning of group B completes.

Note: When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.

Note: When group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

Note: If the single scan continuous function is used (ADGSPCR.GBRP = 1) when the group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), the ADST bit is 1.

34.2.4 A/D Channel Select Register A0 (ADANSA0)

Address(es): ADC140.ADANSA0 4005 C004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ANSA10	ANSA09	—	—	ANSA06	ANSA05	ANSA04	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	ANSA06 to ANSA04	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [6] (ANSA06) corresponds to AN006 and bit [4] (ANSA04) corresponds to AN004.	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10, b9	ANSA10, ANSA09	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [10] (ANSA10) corresponds to AN010 and bit [0] (ANSA09) corresponds to AN009.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 04 to 06, 09, and 10) (A/D Conversion Channels Select)

The ANSAn.ADANSA0 bits select the analog input channels for A/D conversion from AN004 to AN006, AN009, and AN010. The selected channels and their number can be set arbitrarily. The ANSA04 bit is associated with AN004 and the ANSA10 bit is associated with AN010.

When performing A/D conversion on the temperature sensor output or internal reference voltage, set the ADANSA0 register to 0000h to deselect all analog input channels.

In double trigger mode, the channel selected in the ADANSA0 register is invalid, and the channel specified in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

In group scan mode, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

Only set the ADANSA0 register when the ADCSR.ADST bit is 0.

[Clearing conditions]

- 软件写入0时
- 当所有选定通道的AD转换、温度传感器输出或内部参考电压在单次扫描模式下完成
- 在组扫描模式下完成A组扫描时
- 在组扫描模式下完成B组扫描时
- 当启用A组优先控制操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRP位设置为1，并且每次完成B组扫描。

Note: 当启用A组优先控制操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为1。

Note: 当启用A组优先控制操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为0。当强制AD转换终止时，请遵循以下步骤清除ADST位。

Note: 如果在启用组优先操作模式（ADCSR.ADCS[1:0]=01b和ADGSPCR.PGS=1）时使用单次扫描连续功能（ADGSPCR.GBRP=1），则ADST位为1。

34.2.4 AD通道选择寄存器A0(ADANSA0)

Address(es): ADC140.ADANSA0 4005 C004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ANSA10	ANSA09	—	—	ANSA06	ANSA05	ANSA04	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	ANSA06 to ANSA04	AD转换通道选择	0：未选择关联输入通道1：选择关联输入通道位[6]（ANSA06）对应AN006，位[4]（ANSA04）对应AN004。	R/W
b8, b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10, b9	ANSA10, ANSA09	AD转换通道选择	0：未选择相关输入通道1：已选择相关输入通道位[10](ANSA10)对应AN010，位[0](ANSA09)对应AN009。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSAN位（n=04到06、09和10）（AD转换通道选择）

ANSan.ADANSA0位选择用于从AN004到AN006、AN009和AN010的AD转换的模拟输入通道。可以任意设置所选通道及其编号。ANSA04位与AN004和
ANSA10位与AN010相关联。

对温度传感器输出或内部参考电压执行AD转换时，将ADANSA0寄存器设置为0000h以取消选择所有模拟输入通道。

双触发模式下，ADANSA0寄存器中选择的通道无效，
改为在A组中选择ADCSR.DBLANS[4:0]位。

在组扫描模式下，不要选择AD通道选择寄存器B0(ADANSB0)和AD中指定的通道
通道选择寄存器B1(ADANSB1)。

仅当ADCSR.ADST位为0时设置ADANSA0寄存器。

34.2.5 A/D Channel Select Register A1 (ADANSA1)

Address(es): ADC140.ADANSA1 4005 C006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSA20	ANSA19	—	ANSA17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ANSA17	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [1] (ANSA17) corresponds to AN017.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	ANSA20, ANSA19	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [4] (ANSA20) corresponds to AN020 and Bit [3] (ANSA19) corresponds to AN019.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 17, 19, and 20) (A/D Conversion Channels Select)

The ADANSA1.ANSAn bits select the analog input channels for A/D conversion from AN017, AN019, and AN020. The selected channels and their number can be set arbitrarily. The ANSA17 bit is associated with AN017 and the AN020 bit is associated with AN020.

When performing A/D conversion on the temperature sensor output or internal reference voltage, set the ADANSA1 register to 0000h to deselect all analog input channels.

In double trigger mode, the channel selected in the ADANSA1 register is invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

In group scan mode, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

Only set the ADANSA1 register when the ADCSR.ADST bit is 0.

34.2.6 A/D Channel Select Register B0 (ADANSB0)

Address(es): ADC140.ADANSB0 4005 C014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ANSB10	ANSB09	—	—	ANSB06	ANSB05	ANSB04	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	ANSB06 to ANSB04	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit[6] (ANSB06) corresponds to AN006 and bit[4] (ANSB04) corresponds to AN004.	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

34.2.5 AD通道选择寄存器A1(ADANSA1)

Address(es): ADC140.ADANSA1 4005 C006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSA20	ANSA19	—	ANSA17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	ANSA17	AD转换通道 Select	0：未选择关联输入通道1：选择关联输入通道Bit[1](ANSA17)对应AN017。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b4, b3	ANSA20, ANSA19	AD转换通道 Select	0：未选择关联输入通道1：选择关联输入通道Bit[4](ANSA20)对应AN020和 位[3](ANSA19)对应于AN019。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSAN位（n=17、19和20）（AD转换通道选择）

ADANSA1.ANSAN位从AN017、AN019和AN020中选择用于AD转换的模拟输入通道。
可以任意设置所选通道及其编号。ANSA17位与AN017相关联，而AN020位与AN020相关联。

对温度传感器输出或内部参考电压进行AD转换时，将ADANSA1寄存器设置为0000h以取消选择所有模拟输入通道。

双触发模式下，ADANSA1寄存器中选择的通道无效，在ADANSA1寄存器中选择的通道无效。
改为在A组中选择ADCSR.DBLANS[4:0]位。

在组扫描模式下，不要选择AD通道选择寄存器B0(ADANSB0)和AD中指定的通道
通道选择寄存器B1(ADANSB1)。

仅当ADCSR.ADST位为0时设置ADANSA1寄存器。

34.2.6 AD通道选择寄存器B0(ADANSB0)

Address(es): ADC140.ADANSB0 4005 C014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ANSB10	ANSB09	—	—	ANSB06	ANSB05	ANSB04	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	ANSB06 to ANSB04	AD转换通道 Select	0：未选择关联输入通道1：选择关联输入通道Bit[6](ANSB06)对应AN006，bit[4](ANSB04)对应AN004。	R/W
b8, b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b10, b9	ANSB10, ANSB09	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [10] (ANSB10) corresponds to AN010 and Bit [0] (ANSB09) corresponds to AN009.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 04 to 06, 09, and 10) (A/D Conversion Channels Select)

The ADANSB0.ANSBn bits select the analog input channels for A/D conversion from AN004 to AN006, AN009, and AN010 in group B when group scan mode is selected. The ADANSB0 register is only used for group scan mode and not for any other modes.

Do not select the channels specified in group A as selected in the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double trigger mode.

The ANSB04 bit is associated with AN004, the ANSB06 bit is associated with AN006, and the ANSB10 bit is associated with AN010.

When performing A/D conversion on the temperature sensor output or internal reference voltage, set the ADANSB0 register to 0000h to deselect all analog input channels.

Only set the ADANSB register while the ADCSR.ADST bit is 0.

34.2.7 A/D Channel Select Register B1 (ADANSB1)

Address(es): ADC140.ADANSB1 4005 C016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSB20	ANSB19	—	ANSB17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ANSB17	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [1] (ANSB17) corresponds to AN017.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	ANSB20, ANSB19	A/D Conversion Channels Select	0: Associated input channel not selected 1: Associated input channel selected Bit [4] (ANSB20) corresponds to AN020 and Bit [3] (ANSB19) corresponds to AN019.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 17, 19, and 20) (A/D Conversion Channels Select)

The ADANSB1.ANSBn bits select the analog input channels for A/D conversion from AN017, AN019, and AN020 in group B when group scan mode is selected. The ADANSB1 register is only used for group scan mode and not for any other modes.

Do not select channels specified in group A as selected with the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits, in double trigger mode.

The ANSB17 bit is associated with AN017, the ANSB19 bit is associated with AN019, and the ANSB20 bit is associated with AN020.

When performing A/D conversion on the temperature sensor output or internal reference voltage, set the ADANSB1 register to 0000h to deselect all analog input channels.

Only set the ADANSB1 register bits when the ADST bit is 0.

Bit	Symbol	位名称	Description	R/W
b10, b9	ANSB10, ANSB09	AD转换通道 Select	0：未选择相关输入通道1：已选择相关输入通道Bit[10](ANSB10)对应AN010和 位[0](ANSB09)对应于AN009。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSBn位（n=04至06、09和10）（AD转换通道选择）

TheADANSB0.ANSBnbitsselecttheanaloginputchannelsforADconversionfromAN004toAN006 AN009 andAN010ingroupBwhengroupscanmodeisselected.ADANSB0寄存器仅用于组扫描模式，不用于任何其他模式。

不要选择在ADANSA0和ADANSA1寄存器中选择的A组中指定的通道，并且双触发模式下的ADCSR.DBLANS[4:0]位。

ANSB04位与AN004相关联，ANSB06位与AN006相关联，ANSB10位与AN010相关联。

在对温度传感器输出或内部参考电压进行AD转换时，将ADANSB0寄存器设置为0000h以取消选择所有模拟输入通道。

仅在ADCSR.ADST位为0时设置ADANSB寄存器。

34.2.7 AD通道选择寄存器B1(ADANSB1)

Address(es): ADC140.ADANSB1 4005 C016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSB20	ANSB19	—	ANSB17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	ANSB17	AD转换通道 Select	0：未选择关联输入通道1：选择关联输入通道Bit[1](ANSB17)对应AN017。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b4, b3	ANSB20, ANSB19	AD转换通道 Select	0：未选择关联输入通道1：选择关联输入通道Bit[4](ANSB20)对应于AN020和 位[3](ANSB19)对应于AN019。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSBn位（n=17、19和20）（AD转换通道选择）

TheADANSB1.ANSBnbitsselecttheanaloginputchannelsforADconversionfromAN017 AN019 andAN020ingroupBwhengroupscanmodeisselected.ADANSB1寄存器仅用于组扫描模式，不用于任何其他模式。

不要选择A组中指定的通道，如使用ADANSA0和ADANSA1寄存器和ADCSR.DBLANS[4:0]位，双触发模式。

ANSB17位与AN017相关联，ANSB19位与AN019相关联，ANSB20位与AN020相关联。

对温度传感器输出或内部参考电压进行AD转换时，将ADANSB1寄存器设置为0000h以取消选择所有模拟输入通道。

仅当ADST位为0时才设置ADANSB1寄存器位。

34.2.8 A/D-Converted Value Addition/Average Channel Select Register 0 (ADADS0)

Address(es): ADC140.ADADS0 4005 C008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ADS10	ADS09	—	—	ADS06	ADS05	ADS04	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	ADS06 to ADS04	A/D-Converted Value Addition/ Average Channel Select	0: Associated input channel not selected 1: Associated input channel selected Bit [6] (ADS06) corresponds to AN006 and Bit [4] (ADS04) corresponds to AN004.	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10, b9	ADS10, ADS09	A/D-Converted Value Addition/ Average Channel Select	0: Associated input channel not selected 1: Associated input channel selected Bit [10] (ADS10) corresponds to AN010 and Bit [0] (ADS09) corresponds to AN009.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 04 to 06, 09, and 10) (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channel selected in the ANSAn bits (n = 04 to 06, 09, and 10) in ADANSA0, or the ADCSR.DBLANS[4:0] bits is subject to A/D-converted value addition or averaging.

When the ANSBn bit (n = 04 to 06, 09, and 10) in ADANSB0 is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D Data Register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D Data Register.

For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D Data Register.

Only set the ADADS0 register bits when the ADCSR.ADST bit is 0.

34.2.9 A/D-Converted Value Addition/Average Channel Select Register 1 (ADADS1)

Address(es): ADC140.ADADS1 4005 C00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ADS20	ADS19	—	ADS17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ADS17	A/D-Converted Value Addition/Average Channel Select	0: Associated input channel not selected 1: Associated input channel selected Bit [1] (ADS17) corresponds to AN017.	
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

34.2.8 D转换值加法平均通道选择寄存器0(ADADS0)

Address(es): ADC140.ADADS0 4005 C008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ADS10	ADS09	—	—	ADS06	ADS05	ADS04	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	ADS06 to ADS04	A/D-Converted Value Addition/ 平均频道选择	0：未选择关联输入通道1：选择关联输入通道Bit[6](ADS06)对应AN006和 位[4](ADS04)对应于AN004。	R/W
b8, b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10, b9	ADS10, ADS09	A/D-Converted Value Addition/ 平均频道选择	0：未选择相关输入通道1：已选择相关输入通道Bit[10](ADS10)对应于AN010和 位[0](ADS09)对应于AN009。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ADSn位（n=04至06、09和10）（AD转换增值平均通道选择）

ADSn位确定在ANSAn位（n=04到06、09和10）中选择哪个AD转换通道ADANSA0或ADCSR.DBLANS[4:0]位受到AD转换值相加或平均。

当ADANSB0中的ANSBn位（n=04到06、09和10）设置为1时，各个通道的模拟输入的AD转换将按照ADC[2:0]的规定连续执行1到16次]ADADC寄存器中的位。

当ADADC.AVEE位为0时，通过加法（积分）获得的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，通过加法（积分）获得的结果的平均值存储在AD数据寄存器中。

对于已执行AD转换且未选择加法平均模式的通道，将执行正常的1次转换并将转换结果存储在AD数据寄存器中。

仅当ADCSR.ADST位为0时设置ADADS0寄存器位。

34.2.9 D转换值加法平均通道选择寄存器1(ADADS1)

Address(es): ADC140.ADADS1 4005 C00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ADS20	ADS19	—	ADS17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	ADS17	A/D-Converted Value Addition/Average Channel Select	0：未选择关联输入通道1：选择关联输入通道Bit[1](ADS17)对应AN017。	
b2	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b4, b3	ADS20, ADS19	A/D-Converted Value Addition/Average Channel Select	0: Associated input channel not selected 1: Associated input channel selected Bit [4] (ADS20) corresponds to AN020 and Bit [3] (ADS19) corresponds to AN019.	
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 17, 19, and 20) (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels selected in the ANSAn bits (n = 17, 19, and 20) in ADANSA1, or ADCSR.DBLANS[4:0] bits are subject to A/D-converted value addition or averaging. When ANSBn bit (n = 17, 19, and 20) in ADANSB1 is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1 to 16 times as determined by the setting of the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register. For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D Data Register.

Only set the ADADS1 register when the ADCSR.ADST bit is 0.

Figure 34.2 shows a scanning operation sequence in which both the ADADS0.ADS06 and ADADS1.ADS19 bits are set to 1. For this example:

- Addition mode is selected (ADADS.AVEE = 0)
- The number of conversions is set to 4 (ADADC.ADC[1:0] = 11b)
- Channels AN004 to AN006, AN009, AN010, AN017, AN019, and AN020 are selected (ADANSA0.ANSA0[15:0] = 0670h, and ADANSA1.ANSA1[15:0] = 001Ah) in continuous scan mode (ADCSR.ADCS[1:0] = 10b).

The conversion process begins with AN004. The AN006 conversion is performed successively 4 times, and the added value is returned to A/D Data Register 6 (ADDR6). Next, the AN009 conversion process is started. The AN019 conversion is performed successively 4 times and the added value is returned to A/D Data Register 19 (ADDR19). After conversion of AN020, the conversion operation repeats in the same sequence starting from AN004.

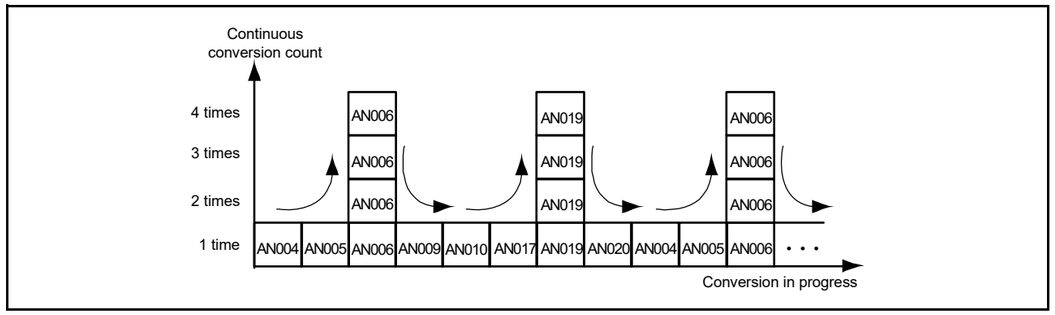


Figure 34.2 Scan conversion sequence with ADADC.ADC[2:0] = 011b, ADADS0.ADS06 = 1, and ADADS1.ADS19 = 1

Bit	Symbol	位名称	Description	R/W
b4, b3	ADS20, ADS19	A/D-Converted Value Addition/Average Channel Select	0：未选择相关输入通道1：已选择相关输入通道Bit[4](ADS20)对应于AN020和 位[3](ADS19)对应于AN019。	
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ADSn位（n=17、19和20）（D转换增值平均通道选择）

ADSn位确定在ADANSA1的ANSAn位（n=17、19和20）或ADCSR.DBLANS[4:0]位中选择的哪些AD转换通道受AD转换值相加或平均。当ADANSB1中的ANSBn位（n=17、19和20）设置为1时，各个通道的模拟输入的A/D转换将根据ADC[2:0]的设置连续执行1到16次ADADC寄存器中的位。

当ADADC.AVEE位为0时，相加得到的值存储在AD数据寄存器中。当。。。的时候ADADC.AVEE位为1，加法所得结果的平均值存入AD数据寄存器。对于已执行AD转换且未选择加法平均模式的通道，将执行正常的1次转换并将转换结果存储在AD数据寄存器中。

仅当ADCSR.ADST位为0时设置ADADS1寄存器。

图34.2显示了扫描操作序列，其中ADADS0.ADS06和ADADS1.ADS19位都设置为1。对于本例：

- 选择加法模式(ADADS.AVEE=0)
- 转换次数设置为4(ADADC.ADC[1:0]=11b)
- 在连续扫描模式（ADCSR.ADCS[1:0]=10b)。

转换过程从AN004开始。AN006转换连续执行4次，相加后的值返回到AD数据寄存器6(ADDR6)。接下来，开始AN009转换过程。AN019转换连续执行4次，相加后的值返回到AD数据寄存器19(ADDR19)。转换AN020后，转换操作从AN004开始以相同的顺序重复。

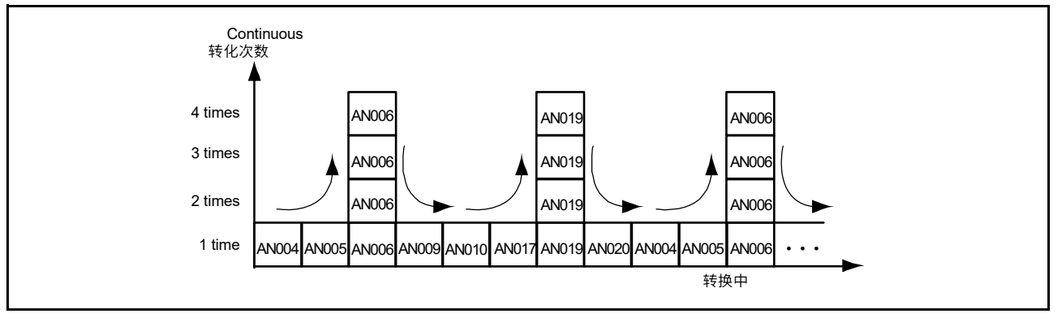


Figure 34.2 使用ADADC.ADC[2:0]=011b、ADADS0.ADS06=1和ADADS1.ADS19 = 1

34.2.10 A/D-Converted Value Addition/Average Count Select Register (ADADC)

Address(es): ADC140.ADADC 4005 C00Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ADC[2:0]	Count Select	b2 b0 0 0 0: 1-time conversion (no addition: same as normal conversion) 0 0 1: 2-time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4-time conversion (three additions) 1 0 1: 16-time conversion (15 additions). Other settings are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AVEE	Average Mode Enable	0: Average mode is disabled*1 1: Average mode is enabled.*2	R/W

Note 1. When average mode is deselected by setting the ADADC.AVEE bit to 0, set the addition count to 1, 2, 3, 4, or 16-time conversion. 16-time conversion can only be used with 12-bit accuracy.

Note 2. When average mode is selected by setting the ADADC.AVEE bit to 1, set the addition count to 2-time or 4-time conversion. Do not set the addition count to 3-time or 16-time conversion (ADC[2:0] = 010b and 101b).

ADC[2:0] bits (Count Select)

The ADC[2:0] bits set the addition count for all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double trigger mode with the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of the temperature sensor output and internal reference voltage.

The following restrictions apply to the setting of the ADC[2:0] bits:

- When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the count to 3-time conversion (ADADC.ADC[2:0] = 010b) or 16-time conversion (ADADC.ADC[2:0] = 101b) with a conversion accuracy setting of 14 bits (ADCER.ADPRC[1:0] = 11b)
- When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b
- When the conversion accuracy is 14 bits (ADCER.ADPRC[1:0] = 11b), do not set the ADC[2:0] bits to 101b.

Only set the ADC[2:0] bits when the ADCSR.ADST bit is 0.

AVEE bit (Average Mode Enable)

The AVEE bit selects addition or average mode for the channels for which A/D conversion and A/D-converted value addition/average mode are selected, including the channel selected for double trigger mode in the ADCSR.DBLANS[4:0] bits, the temperature sensor output, and the internal reference voltage.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to 3-time conversion (ADADC.ADC[2:0] = 010b).

Only set the AVEE bits while the ADCSR.ADST bit is 0.

34.2.10 D转换值加法平均计数选择寄存器(ADADC)

Address(es): ADC140.ADADC 4005 C00Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	ADC[2:0]	计数选择	b2 b0 0 0 0：1次转换（不加：同普通转换） 0 0 1: 2-time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4-time conversion (three additions) 01：16次转换（15次加法）。禁止其他设置。	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	AVEE	平均模式启用	0：禁用平均模式*11：启用平均模式。*2	R/W

Note 1. 通过将ADADC.AVEE位设置为0取消选择平均模式时，将加法计数设置为1、2、3、4或16次转换。16次转换只能用于12位精度。

Note 2. 当通过将ADADC.AVEE位设置为1来选择平均模式时，将加法计数设置为2次或4次转换。不要将加法计数设置为3次或16次转换（ADC[2:0]=010b和101b）。

ADC[2:0]位（计数选择）

ADC[2:0]位设置选择了AD转换和加法平均模式的所有通道的加法计数，包括使用ADCSR.DBLANS[4:0]位在双触发模式中选择的通道。该计数也适用于温度传感器输出和内部参考电压的AD转换。

以下限制适用于ADC[2:0]位的设置：

- 通过将ADADC.AVEE位设置为1来选择平均模式时，不要将计数设置为3次转换(ADADC.ADC[2:0]=010b)或16次转换(ADADC.ADC[2:0]=101b)，转换精度设置为14位(ADCER.ADPRC[1:0]=11b)
- 执行自诊断时(ADCER.DIAGM=1)，请勿将ADC[2:0]位设置为000b以外的任何值
- 当转换精度为14位(ADCER.ADPRC[1:0]=11b)时，请勿将ADC[2:0]位设置为101b。

仅当ADCSR.ADST位为0时设置ADC[2:0]位。

AVEE位（平均模式启用）

AVEE位为选择AD转换和AD转换值加法平均模式的通道选择加法或平均模式，包括在ADCSR.DBLANS[4:0]位中选择双触发模式的通道，温度传感器输出和内部参考电压。

当通过将ADADC.AVEE位设置为1来选择平均模式时，不要将加法计数设置为3次转换(ADADC.ADC[2:0]=010b)。

仅在ADCSR.ADST位为0时设置AVEE位。

34.2.11 A/D Control Extended Register (ADCER)

Address(es): ADC140.ADCER 4005 C00Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D Conversion Accuracy Specify	b2 b1 0 0: 12-bit accuracy 0 1: Setting prohibited 1 0: Setting prohibited 1 1: 14-bit accuracy.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	A/D Data Register Automatic Clearing Enable	0: Automatic clearing disabled 1: Automatic clearing enabled.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: Select 0 V 1 0: Select reference power supply voltage*1 × 1/2 1 1: Select reference power supply voltage*1.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Select rotation mode for self-diagnosis voltage 1: Select fixed mode for self-diagnosis voltage.	R/W
b11	DIAGM	Self-Diagnosis Enable	0: ADC14 self-diagnosis disabled 1: ADC14 self-diagnosis enabled.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Flush-right for the A/D data register format selected 1: Flush-left for the A/D data register format selected.	R/W

Note 1. Reference voltage refers to VREFH0.

ADPRC[1:0] bits (A/D Conversion Accuracy Specify)

The ADPRC[1:0] bits select the A/D conversion accuracy to 12-bits or 14-bits. Changing the A/D conversion accuracy also changes the bit width of valid data stored in the result register and the A/D conversion time.

For details, see section 34.3.6, Analog Input Sampling and Scan Conversion Time. Only set the ADPRC[1:0] bits while the ADCSR.ADST bit is 0.

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0) of the ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR register after any of these registers is read by the CPU, DTC, or DMAC.

DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis fixed voltage mode. For details, see the ADCER.DIAGLD bit description.

Do not execute self-diagnosis when the ADCER.DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated, or the fixed voltage is used in self-diagnosis. Setting DIAGLD to 0 selects conversion of the voltages in rotation mode where 0 V, the reference power supply × 1/2, and the reference power supply are converted in that order. After reset, when the self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The self-diagnosis voltage value does not return to 0 when scan conversion

34.2.11 AD控制扩展寄存器(ADCER)

Address(es): ADC140.ADCER 4005 C00Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b2, b1	ADPRC[1:0]	AD转换精度指定	b2b100：12位精度01：禁止设置10：禁止设置11：14位精度。	R/W
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	ACE	AD数据寄存器自动清零Enable	0：禁止自动清除1：允许自动清除。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	DIAGVAL[1:0]	自诊断转换电压Select	b9b800：自诊断有效时禁止设置01：选择0V10：选择参考电源电压*1×1211：选择参考电源电压*1。	R/W
b10	DIAGLD	自诊断模式选择	0：自诊断电压选择旋转模式1：自诊断电压选择固定模式。	R/W
b11	DIAGM	Self-Diagnosis Enable	0：ADC14自诊断禁用1：ADC14自诊断启用。	R/W
b14 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	ADRFMT	AD数据寄存器格式选择	0：选择AD数据寄存器格式右对齐1：选择AD数据寄存器格式左对齐。	R/W

Note 1. 参考电压是指VREFH0。

ADPRC[1:0]位（AD转换精度指定）

ADPRC[1:0]位选择AD转换精度为12位或14位。更改AD转换精度也会更改存储在结果寄存器中的有效数据的位宽和AD转换时间。

有关详细信息，请参见第34.3.6节，模拟输入采样和扫描转换时间。仅在ADCSR.ADST位为0时设置ADPRC[1:0]位。

ACE位（AD数据寄存器自动清除使能）

在CPU、DTC或DMAC读取这些寄存器中的任何一个后，ACE位启用或禁用ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR或ADOCDR寄存器的自动清除（全为0）。

DIAGVAL[1:0]位（自诊断转换电压选择）

DIAGVAL[1:0]位选择用于自诊断固定电压模式的电压值。有关详细信息，请参阅ADCER.DIAGLD位描述。

当ADCER.DIAGVAL[1:0]位设置为00b时，不执行自诊断。

DIAGLD位（自诊断模式选择）

DIAGLD位选择是轮换三个电压值，还是使用固定电压进行自诊断。
将DIAGLD设置为0选择在旋转模式下转换电压，其中0V、参考电源×12和参考电源按此顺序转换。复位后，选择自诊断电压旋转模式时，从0V开始执行自诊断。扫描转换时自诊断电压值不返回0

completes. When scan conversion is restarted, rotation starts at the voltage value following the previous value.

Setting DIAGLD to 1 selects fixed voltage, in which the fixed voltage specified by the ADCER.DIAGVAL[1:0] bits is converted. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

Only set the DIAGLD bit while the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.

Self-diagnosis is used to detect a failure of the ADC14. In self-diagnosis mode, one of the internally generated voltage values (0 V, the reference power supply × 1/2, or the reference power supply) is converted. When conversion completes, information on the converted voltage and the conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). ADRD can be read by software to determine whether the conversion result falls within the normal or abnormal range.

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. In double trigger mode (ADCSR.DBLE = 1), self-diagnosis (DIAGM = 0) is deselected. When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately for group A and B.

Only set the DIAGM bit when the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for the data to be stored in ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD.

Only set the ADRFMT bit when the ADCSR.ADST bit is 0.

34.2.12 A/D Conversion Start Trigger Select Register (ADSTRGR)

Address(es): ADC140.ADSTRGR 4005 C010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	Select the A/D conversion start trigger for group B in group scan mode	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger in single scan mode and continuous scan mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits are only used in group scan mode and not in any other scan mode. Software trigger or asynchronous trigger cannot be used as the scan conversion start trigger for group B. In group scan mode, set the TRSB[5:0] bits to a value other than 000000b and set the ADCSR.TRGE bit to 1.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 3Fh. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by the trigger might have no effect.

When the GPT module is selected as an A/D conversion start trigger, a delay for synchronization processing occurs. For details, see section 34.3.6, Analog Input Sampling and Scan Conversion Time.

完成。重新开始扫描转换时，从前一个值之后的电压值开始旋转。

将DIAGLD设置为1选择固定电压，其中转换由ADCER.DIAGVAL[1:0]位指定的固定电压。如果将固定模式切换到旋转模式，则从固定电压值开始旋转。

仅在ADCSR.ADST位为0时设置DIAGLD位。

DIAGM位（自诊断使能）

DIAGM位启用或禁用自诊断。

自诊断用于检测ADC14的故障。在自诊断模式下，转换内部产生的电压值之一（0V、参考电源×12或参考电源）。转换完成后，转换电压和转换结果的信息存储在AD自诊断数据寄存器(ADRD)中。ADRD可以通过软件读取来判断转换结果是否在正常或异常范围内。

自诊断在每次扫描开始时执行一次，并转换三个电压之一。在双触发模式(ADCSR.DBLE=1)中，自诊断(DIAGM=0)被取消选择。在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

仅当ADCSR.ADST位为0时设置DIAGM位。

ADRFMT位（AD数据寄存器格式选择）

ADRFMT位指定要存储在ADDRy、ADDBLDR、ADDBLDRA、
ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD.

仅当ADCSR.ADST位为0时才设置ADRFMT位。

34.2.12 AD转换开始触发选择寄存器(ADSTRGR)

Address(es): ADC140.ADSTRGR 4005 C010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	TRSB[5:0]	B组的AD转换开始触发选择	在组扫描模式下选择B组的AD转换启动触发	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13 to b8	TRSA[5:0]	AD转换开始触发选择	在单次扫描模式和连续扫描模式中选择AD转换启动触发。在组扫描模式下，选择A组的AD转换启动触发。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TRSB[5:0]位（B组的AD转换开始触发选择）

TRSB[5:0]位选择触发以开始扫描组B中选择的模拟输入。TRSB[5:0]位仅用于组扫描模式，不用于任何其他扫描模式。软件触发或异步触发不能用作B组的扫描转换开始触发。在组扫描模式下，将TRSB[5:0]位设置为000000b以外的值，并将ADCSR.TRGE位设置为1。

当A组在组扫描模式下具有优先权时，将ADGSPCR.GBRP位设置为1允许B组在单次扫描模式下连续工作。将ADGSPCR.GBRP位设置为1时，将TRSB[5:0]位设置为3Fh。转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发的AD转换可能无效。

WhentheGPTmoduleisselectedasanADconversionstarttrigger adelayforsynchronizationprocessingoccurs.有关详细信息，请参见第34.3.6节，模拟输入采样和扫描转换时间。

Table 34.6 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

Table 34.6 Selection of A/D conversion sources in the TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselection state		1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00/ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. When scanning is executed in group scan mode or double trigger mode, do not use a software trigger or an asynchronous trigger.

When using the synchronous trigger (ELC) as the A/D conversion start source, set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 0.

The software trigger (ADCSR.ADST) is enabled regardless of the setting in the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by the trigger might have no effect. For details, see section 34.3.6, Analog Input Sampling and Scan Conversion Time.

Table 34.7 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Table 34.7 Selection of A/D activation sources in the TRSA[5:0] bits

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselection state		1	1	1	1	1	1
ADTRG0	Input pin for the trigger	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00/ELC_AD01	ELC	0	0	1	0	1	1

34.2.13 A/D Conversion Extended Input Control Register (ADEXICR)

Address(es): ADC140.ADEXICR 4005 C012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select	0: Temperature sensor output A/D-converted value addition/average mode not selected 1: Temperature sensor output A/D-converted value addition/average mode selected.	R/W
b1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select	0: Internal reference voltage A/D-converted value addition/average mode not selected 1: Internal reference voltage A/D-converted value addition/average mode selected.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TSSA	Temperature Sensor Output A/D Conversion Select	0: A/D conversion of temperature sensor output disabled 1: A/D conversion of temperature sensor output enabled.	R/W

表34.6列出了在TRSB[5:0]位中选择的AD转换启动源。

Table 34.6 在TRSB[5:0]位中选择AD转换源

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
触发源取消选择状态		1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00/ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0]位（AD转换开始触发选择）

TRSA[5:0]位选择触发以在单次扫描模式和连续扫描模式下启动AD转换。在组扫描模式下，选择触发开始扫描A组中选择的模拟输入。在组扫描模式或双触发模式下执行扫描时，请勿使用软件触发或异步触发。

使用同步触发(ELC)作为AD转换启动源时，将ADCSR寄存器中的TRGE位设置为1，并将ADCSR寄存器中的EXTRG位设置为0。

无论ADCSR.TRGE位、ADCSR.EXTRG位或TRSA[5:0]位的设置如何，都会启用软件触发(ADCSR.ADST)。转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发的AD转换可能无效。有关详细信息，请参见第34.3.6节，模拟输入采样和扫描转换时间。

表34.7列出了在TRSA[5:0]位中选择的AD转换起始源。

Table 34.7 在TRSA[5:0]位中选择AD激活源

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
触发源取消选择状态		1	1	1	1	1	1
ADTRG0	触发器的输入引脚	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00/ELC_AD01	ELC	0	0	1	0	1	1

34.2.13 AD转换扩展输入控制寄存器(ADEXICR)

Address(es): ADC140.ADEXICR 4005 C012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSSAD	温度传感器输出AD转换后的增值平均值模式选择	0：未选择温度传感器输出AD转换值相加平均模式1：选择温度传感器输出AD转换值相加平均模式。	R/W
b1	OCSAD	内部参考电压AD转换后的增值平均值模式选择	0：未选择内部基准电压AD转换值相加平均模式1：选择内部基准电压AD转换值相加平均模式。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	TSSA	温度传感器输出AD转换选择	0：温度传感器输出AD转换禁止1：温度传感器输出AD转换使能。	R/W

Bit	Symbol	Bit name	Description	R/W
b9	OCSA	Internal Reference Voltage A/D Conversion Select	0: A/D conversion of internal reference voltage disabled 1: A/D conversion of internal reference voltage enabled.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively for the number of times specified in the ADC[2:0] bits in the ADADC register. The maximum addition count depends on the conversion accuracy, as seen in section 34.2.1. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Temperature Sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.

Only set the TSSAD bit while the ADCSR.ADST bit is 0.

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively for the number of times specified by the ADC[2:0] bits in the ADADC register. The maximum addition count depends on the conversion accuracy as seen in section 34.2.1. When the ADADC.AVEE bit is 0, the value obtained by addition is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADOCDR.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output.

When executing the A/D conversion:

1. Set all the bits in the ADANSA0/1 and ADANSB0/1 registers, the ADCSR.DBLE bit, and ADEXICR.OCSA bit to 0.
2. Execute A/D conversion in single scan mode.

When executing the A/D conversion of the temperature sensor output, the ADDISCR register is set to 0Fh and the ADC14 executes discharge (15 ADCLK) before executing sampling. The minimum sampling time is 5 µs. The ADC14 executes discharge each time it executes A/D conversion of the temperature sensor output.

Only set the TSSA bit when the ADCSR.ADST bit is 0.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage.

When executing the A/D conversion:

1. Set all the bits in the ADANSA0/1 and ADANSB0/1 registers, the ADCSR.DBLE bit, and ADEXICR.TSSA bit to 0.
2. Execute A/D conversion in single scan mode.

When executing the A/D conversion of the internal reference voltage, the ADDISCR register is set to 0Fh and the ADC14 executes discharge (15 ADCLK) before executing sampling.The minimum sampling time is 5 µs. The ADC14 executes discharge each time it executes A/D conversion of the internal reference voltage.

Only set the OCSA bit while the ADCSR.ADST bit is 0.

Bit	Symbol	位名称	Description	R/W
b9	OCSA	内部参考电压AD转换选择	0：禁止内部参考电压AD转换1：使能内部参考电压AD转换。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TSSAD位（温度传感器输出AD转换值加法平均模式选择）

当TSSAD位设置为1时，温度传感器输出的AD转换被选择并连续执行ADADC寄存器中ADC[2:0]位指定的次数。最大加法计数取决于转换精度，如第34.2.1节所示。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD温度传感器数据寄存器(ADTSDR)。当ADADC.AVEE位为1时，平均值返回给ADTSDR。

仅在ADCSR.ADST位为0时设置TSSAD位。

OCSAD位（内部参考电压AD转换值加法平均模式选择）

当OCSAD位设置为1时，内部参考电压的AD转换被选择并连续执行ADADC寄存器中ADC[2:0]位指定的次数。最大加法计数取决于第34.2.1节中的转换精度。当ADADC.AVEE位为0时，加法得到的值返回到AD内部参考电压数据寄存器(ADOCDR)。当ADADC.AVEE位为1时，平均值返回给ADOCDR。

仅在ADCSR.ADST位为0时设置OCSAD位。

TSSA位（温度传感器输出AD转换选择）

TSSA位选择温度传感器输出的AD转换。

执行AD转换时：

1. 将ADANSA01和ADANSB01寄存器、ADCSR.DBLE位和ADEXICR.OCSA位中的所有位设置为0。
2. 在单次扫描模式下执行AD转换。

当执行温度传感器输出的AD转换时，ADDISCR寄存器设置为0Fh，并且ADC14在执行采样前执行放电(15ADCLK)。最小采样时间为5µs。ADC14每次执行温度传感器输出的AD转换时执行放电。

仅当ADCSR.ADST位为0时设置TSSA位。

OCSA位（内部参考电压AD转换选择）

OCSA位选择内部参考电压的AD转换。

执行AD转换时：

1. 将ADANSA01和ADANSB01寄存器、ADCSR.DBLE位和ADEXICR.TSSA位中的所有位设置为0。
2. 在单次扫描模式下执行AD转换。

当执行内部参考电压的AD转换时，ADDISCR寄存器设置为0Fh，并且ADC14在执行采样前执行放电（15个ADCLK）。最小采样时间为5µs。ADC14每次执行内部参考电压的AD转换时执行放电。

仅在ADCSR.ADST位为0时设置OCSA位。

34.2.14 A/D Sampling State Register n (ADSSTRn) (n = 00, 04 to 06, 09, 10, L, T, O)

Address(es): ADC140.ADSSTR00 4005 C0E0h, ADC140.ADSSTR04 4005 C0E4h to ADC140.ADSSTR06 4005 C0E6h, ADC140.ADSSTR09 4005 C0E9h, ADC140.ADSSTR10 4005 C0EAh, ADC140.ADSSTRL 4005 C0DDh, ADC140.ADSSTRT 4005 C0DEh, ADC140.ADSSTRO 4005 C0DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
Value after reset:	0	0	0	0	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 5 to 255 states	R/W

The ADSSTRn register sets the sampling time for analog input. If one state is 1 ADCLK (A/D conversion clock) cycle and the ADCLK clock is 64 MHz, then one state is 15.625 ns. The initial value is 13 states.

The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

Only set the SST[7:0] bits while the ADCSR.ADST bit is 0.

The lower limit of the sampling time setting depends on the frequency ratio:

- If the frequency ratio of PCLKB to PCLKC (ADCLK) = 1:1, 2:1, 4:1, or 8:1, the sampling time must be set to a value of more than 5 states
- If the frequency ratio of PCLKB to PCLKC (ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 34.8 shows the relationship between the A/D Sampling State Register and the associated channels. For details, see section 34.3.6, Analog Input Sampling and Scan Conversion Time.

Table 34.8 Relationship between A/D Sampling State Register n and associated channels

Bit name	Associated channels
ADSSTR00.SST[7:0] bits	self-diagnosis function
ADSSTR04.SST[7:0] bits	AN004
ADSSTR05.SST[7:0] bits	AN005
ADSSTR06.SST[7:0] bits	AN006
ADSSTR09.SST[7:0] bits	AN009
ADSSTR10.SST[7:0] bits	AN010
ADSSTRL.SST[7:0] bits	AN017, AN019, AN020
ADSSTRT.SST[7:0] bits	Temperature sensor output*1
ADSSTRO.SST[7:0] bits	Internal reference voltage*1

Note 1. When the temperature sensor output or the internal reference voltage is converted, set the sampling time to more than 5 µs. Because the maximum SST[7:0] value is 255 states, the ADCLK frequency must be such that the resulting sampling time is at least 5 µs.

34.2.14 AD采样状态寄存器n(ADSSTRn)(n=00 04to06 09 10 L T O)

Address(es): ADC140.ADSSTR00 4005 C0E0h, ADC140.ADSSTR04 4005 C0E4h to ADC140.ADSSTR06 4005 C0E6h, ADC140.ADSSTR09 4005 C0E9h, ADC140.ADSSTR10 4005 C0EAh, ADC140.ADSSTRL 4005 C0DDh, ADC140.ADSSTRT 4005 C0DEh, ADC140.ADSSTRO 4005 C0DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
重置后的值:	0	0	0	0	1	1	0	1

Bit	Symbol	位名称	Description	R/W
b7 to b0	SST[7:0]	采样时间设置	这些位在5到255个状态范围内设置采样时间	R/W

ADSSTRn寄存器设置模拟输入的采样时间。如果一种状态是1个ADCLK（AD转换时钟）周期并且ADCLK时钟是64MHz，那么一种状态是15.625ns。初始值为13个状态。

如果模拟输入信号源的阻抗太高而无法保证足够的采样时间，或者如果ADCLK时钟很慢，则可以调整采样时间。

仅在ADCSR.ADST位为0时设置SST[7:0]位。

采样时间设置的下限取决于频率比：

- 如果PCLKB与PCLKC(ADCLK)的频率比=1:1、2:1、4:1或8:1，则必须将采样时间设置为5个以上状态的值
- 如果PCLKB与PCLKC(ADCLK)的频率比=1:2或1:4，则必须将采样时间设置为超过6个状态的值。

表34.8显示了AD采样状态寄存器和相关通道之间的关系。有关详细信息，请参见第34.3.6节，模拟输入采样和扫描转换时间。

Table 34.8 AD采样状态寄存器n与相关通道之间的关系

位名称	关联频道
ADSSTR00.SST[7:0] bits	self-diagnosis function
ADSSTR04.SST[7:0] bits	AN004
ADSSTR05.SST[7:0] bits	AN005
ADSSTR06.SST[7:0] bits	AN006
ADSSTR09.SST[7:0] bits	AN009
ADSSTR10.SST[7:0] bits	AN010
ADSSTRL.SST[7:0] bits	AN017, AN019, AN020
ADSSTRT.SST[7:0] bits	温度传感器输出*1
ADSSTRO.SST[7:0] bits	内部参考电压*1

Note 1. 转换温度传感器输出或内部参考电压时，将采样时间设置为5µs以上。
因为最大SST[7:0]值是255个状态，所以ADCLK频率必须使得得到的采样时间至少为5µs。

34.2.15 A/D Disconnection Detection Control Register (ADDISCR)

Address(es): ADC140.ADDISCR 4005 C07Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ADNDIS[3:0]	Precharge/discharge period	b3 b0 0 0 0 0: The disconnection detection assist function is disabled 0 0 0 1: Setting prohibited Others: The number of states for the discharge or precharge period.	R/W
b4	PCHG	Precharge/discharge select	0: Discharge 1: Precharge.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge, and the period of precharge or discharge for the A/D disconnection detection assist function. Only set the ADDISCR register when the ADCSR.ADST bit is 0.

When the temperature sensor output or internal reference voltage is converted, the A/D converter executes discharge automatically. This operation is achieved by setting the ADDISCR register to 0Fh (15 ADCLK) when ADEXICR.OCSA or TSSA is set to 1. After executing discharge, the A/D converter executes sampling. The required sampling time is 5 µs or more.

Disable the disconnection detection assist function if any of the following functions are used:

- Temperature sensor
- Internal reference voltage
- A/D Self-diagnosis.

ADNDIS[3:0] bits (Precharge/discharge period)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

PCHG bit (Precharge/discharge select)

The PCHG bit selects either precharge or discharge.

34.2.16 A/D Group Scan Priority Control Register (ADGSPCR)

Address(es): ADC140.ADGSPCR 4005 C080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PGS	Group A Priority Control Setting*1	0: Operate without group A priority control 1: Operate with group A priority control.	R/W

34.2.15 AD断线检测控制寄存器(ADDISCR)

Address(es): ADC140.ADDISCR 4005 C07Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCHG	ADNDIS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	ADNDIS[3:0]	Precharge/discharge period	b3b00000：断线检测辅助功能无效0001：设置禁止其他：放电或预充电期间的状态数。	R/W
b4	PCHG	Precharge/discharge select	0: Discharge 1: Precharge.	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ADDISCR寄存器选择预充电或放电，以及AD断线检测辅助功能的预充电或放电周期。仅当ADCSR.ADST位为0时设置ADDISCR寄存器。

当温度传感器输出或内部参考电压转换时，AD转换器自动执行放电。当ADXICR.OCSA或TSSA设置为1时，通过将ADDISCR寄存器设置为0Fh(15ADCLK)来实现此操作。执行放电后，AD转换器执行采样。所需的采样时间为5微秒或更长。

如果使用以下任何功能，请禁用断线检测辅助功能：

- 温度感应器
- 内部参考电压
- A/D Self-diagnosis.

ADNDIS[3:0]位（预充电放电周期）

ADNDIS[3:0]位指定预充电或放电周期。当ADNDIS[3:0]=0000b时，断线检测辅助功能被禁用。禁止将ADNDIS[3:0]位设置为0001b。除了ADNDIS[3:0]=0000b或0001b时，指定值表示预充电或放电期间的状态数。当ADNDIS[3:0]位设置为0000b或0001b以外的任何值时，将启用断线检测辅助功能。

PCHG位（预充电放电选择）

PCHG位选择预充电或放电。

34.2.16 AD组扫描优先控制寄存器(ADGSPCR)

Address(es): ADC140.ADGSPCR 4005 C080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PGS	A组优先控制设置*1	0：无A组优先控制运行1：有A组优先控制运行。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	GBRSCN	Group B Restart Setting	Enabled only when PGS = 1. Reserved when PGS = 0. 0: Do not restart group B scanning after it is stopped by group A priority control 1: Restart group B scanning after it is stopped by group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Group B Single Scan Continuous Start*2	Enabled only when PGS = 1. Reserved when PGS = 0. 0: Single scan for group B is not continuously activated 1: Single scan for group B is continuously activated with priority control.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting PGS to 1. If these bits are set to any other values, proper operation is not guaranteed.
Note 2. When the GBRP bit is set to 1, single scan is performed continuously for group B regardless of the GBRSCN bit.

PGS bit (Group A Priority Control Setting)

Set the PGS bit to 1 to give priority to operation on group A. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. If these bits are set to any other values, proper operation is not guaranteed.

When the PGS bit is set to 0, software must perform a clear operation as described in section 34.8.2, Notes on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings as described in section 34.3.4.3, Operation with group A priority control.

GBRSCN bit (Group B Restart Setting)

The GBRSCN bit controls the restarting of scan operation on group B when operation on group A is given priority. If a scan operation on group B is stopped by a group A trigger input with the GBRSCN bit set to 1, the scan operation is restarted on completion of group A conversion. Also, if a group B trigger is input during A/D conversion on group A, the scan operation on group B is restarted on completion of the group A conversion.

When the GBRSCN bit is set to 0, triggers input during A/D conversion are ignored. Only set the GBRSCN bit while the ADCSR.ADST bit is 0.

The setting of the GBRSCN bit is valid when the PGS bit is 1.

GBRP bit (Group B Single Scan Continuous Start)

Set the GBRP bit to perform a single scan operation continuously on group B.

Setting the GBRP bit to 1 starts a single scan on group B. On completion of the scan, another single scan on group B starts automatically. If a group B conversion stops because of an operation on group A, the group A operation takes priority, and single scan on group B restarts automatically on completion of group A conversion.

Disable group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting in the GBRSCN bit. Only set the GBRP bit while the ADCSR.ADST is 0.

The setting in the GBRP bit is valid when the PGS bit is 1.

Bit	Symbol	位名称	Description	R/W
b1	GBRSCN	B组重启设置	仅在PGS=1时有效。PGS=0时保留。0：B组扫描被A组优先控制停止后不重新启动。1：B组扫描被A组优先控制停止后重新启动。	R/W
b14 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	GBRP	B组单次扫描连续Start*2	仅在PGS=1时启用。在PGS=0时保留。0：B组单次扫描不连续激活1：B组单次扫描连续激活，优先控制。	R/W

Note 1. 在将PGS设置为1之前，必须将ADCSR.ADCS[1:0]位设置为01b（组扫描模式）。如果这些位设置为任何其他值，则无法保证正确操作。
Note 2. 当GBRP位设置为1时，对B组连续执行单次扫描，而与GBRSCN位无关。

PGS位（A组优先控制设置）

将PGS位设置为1，以优先对组A进行操作。在将PGS位设置为1之前，必须将ADCSR.ADCS[1:0]位设置为01b（组扫描模式）。如果这些位设置为任何其他值，不能保证正常运行。

当PGS位设置为0时，软件必须按照第34.8.2节"停止AD转换的注意事项"中的说明执行清除操作。当PGS位设置为1时，使用第34.3.4.3节"A组优先控制操作"中所述的设置。

GBRSCN位（B组重启设置）

当A组操作优先时，GBRSCN位控制B组扫描操作的重新启动。如果B组的扫描操作被GBRSCN位设置为1的A组触发输入停止，则扫描操作在A组转换完成后重新开始。此外，如果在A组的AD转换期间输入了B组触发，则在A组转换完成时重新开始对B组的扫描操作。

当GBRSCN位设置为0时，AD转换期间的触发输入将被忽略。仅设置GBRSCN位，而ADCSR.ADST位为0。

当PGS位为1时GBRSCN位的设置有效。

GBRP位（B组单次扫描连续启动）

设置GBRP位以在B组上连续执行单次扫描操作。

将GBRP位设置为1将启动B组的单次扫描。扫描完成后，自动启动B组的另一次单次扫描。如果B组转换因A组操作而停止，则A组操作优先，B组单次扫描在A组转换完成后自动重新开始。

在将GBRP位设置为1之前禁用B组触发输入。将GBRP位设置为1会使GBRSCN位。仅在ADCSR.ADST为0时设置GBRP位。

GBRP位中的设置在PGS位为1时有效。

34.2.17 A/D Compare Function Control Register (ADCMPCR)

Address(es): ADC140.ADCMPCR 4005 C090h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CMPAB[1:0]	Window A/B Composite Conditions Setting	b1 b0 0 0: Output ADC140_WCMPM when window A OR window B comparison conditions are met. Otherwise, output ADC140_WCMPUM. 0 1: Output ADC140_WCMPM when window A EXOR window B comparison conditions are met. Otherwise, output ADC140_WCMPUM. 1 0: Output ADC140_WCMPM when window A AND window B comparison conditions are met. Otherwise, output ADC140_WCMPUM. 1 1: Setting prohibited. These bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1).	R/W
b8 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	CMPBE	Compare Window B Operation Enable	0: Compare window B operation disabled. ADC140_WCMPM and ADC140_WCMPUM outputs are disabled. 1: Compare window B operation enabled.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	CMPAE	Compare Window A Operation Enable	0: Compare window A operation disabled. ADC140_WCMPM and ADC140_WCMPUM outputs are disabled. 1: Compare window A operation enabled.	R/W
b12	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13	CMPBIE	Compare B Interrupt Enable	0: ADC140_CMPBI interrupt disabled when comparison conditions (window B) are met 1: ADC140_CMPBI interrupt enabled when comparison conditions (window B) are met.	R/W
b14	WCMPE	Window Function Setting	0: Window function disabled. Window A and window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Window function enabled. Window A and window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W
b15	CMPAIE	Compare A Interrupt Enable	0: ADC140_CMPAI interrupt disabled when comparison conditions (window A) are met 1: ADC140_CMPAI interrupt enabled when comparison conditions (window A) are met.	R/W

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCONB.

Only set the CMPAB[1:0] bits when the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare window B operation. Only set the CMPBE bit when the ADCSR.ADST bit is 0.

34.2.17 AD比较功能控制寄存器(ADCMPCR)

Address(es): ADC140.ADCMPCR 4005 C090h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CMPAB[1:0]	窗口AB复合条件设定	b1 b0 0 0：当窗口AOR窗口B比较条件满足时输出ADC140_WCMPM。否则，输出ADC140_WCMPUM。 0 1：当窗口AEXOR窗口B比较条件满足时输出ADC140_WCMPM。否则，输出ADC140_WCMPUM。 1 0：当窗口A和窗口B比较条件满足时，输出ADC140_WCMPM。否则，输出ADC140_WCMPUM。 11：禁止设置。当窗口A和窗口B都使能（CMPAE=1和CMPBE=1）时，这些位有效。	R/W
b8 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9	CMPBE	比较窗口B操作启用	0：禁止比较窗口B操作。ADC140_WCMPM和ADC140_WCMPUM输出被禁用。1：比较窗口B操作使能。	R/W
b10	—	Reserved	该位读取为0。写入值应为0。	R/W
b11	CMPAE	比较窗口A操作启用	0：禁止比较窗口A操作。ADC140_WCMPM和ADC140_WCMPUM输出被禁用。1：启用比较窗口A操作。	R/W
b12	—	Reserved	该位读取为0。写入值应为0。	R/W
b13	CMPBIE	比较B中断Enable	0：满足比较条件（窗口B）时禁用ADC140_CMPBI中断1：满足比较条件（窗口B）时启用ADC140_CMPBI中断。	R/W
b14	WCMPE	窗口功能设置	0：窗口功能禁用。窗口A和窗口B用作比较器，将下侧的单个值与AD转换结果进行比较。1：使能窗口功能。 窗口A和窗口B用作比较器，将上下两个值与AD转换结果进行比较。	R/W
b15	CMPAIE	比较中断Enable	0：满足比较条件（窗口A）时禁用ADC140_CMPAI中断1：满足比较条件（窗口A）时启用ADC140_CMPAI中断。	R/W

CMPAB[1:0]位（窗口AB复合条件设置）

当窗口A和窗口B在单次扫描模式下启用（CMPAE=1和CMPBE=1）时，CMPAB[1:0]位有效。这些位指定比较函数匹配不匹配事件输出条件和ADWINMON.MONCONB的监视条件。

仅当ADCSR.ADST位为0时设置CMPAB[1:0]位。

CMPBE位（比较窗口B操作使能）

CMPBE位启用或禁用比较窗口B操作。仅当ADCSR.ADST位为0时设置CMPBE位。

Set this bit to 0 before setting the following registers and bits:

- A/D Channel Select Registers A0/A1/B0/B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSA or TSSA bit in the A/D Conversion Extended Input Control Register (ADEXICR)
- CMPCHB[5:0] bits in the Window B Channel Select Register (ADCMPBNSR).

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare window A operation. Only set the CMPAE bit when the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers and bits:

- A/D Channel Select Registers A0/A1/B0/B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSA or TSSA bit in the A/D Conversion Extended Input Control Register (ADEXICR)
- Window A Channel Select Registers 0/1 (ADCMPANSR0, ADCMPANSR1)
- Window A Extended Input Select Register (ADCMPANSER).

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC140_CMPBI interrupt output when the comparison conditions (window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Only set the WCMPE bit when the ADCSR.ADST bit is 0.

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC140_CMPAI interrupt output when the comparison conditions (window A) are met.

34.2.18 A/D Compare Function Window A Channel Select Register 0 (ADCMPANSR0)

Address(es): ADC140.ADCMPANSR0 4005 C094h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPCHA10	CMPCHA09	—	—	CMPCHA06	CMPCHA05	CMPCHA04	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	CMPCHA06 to CMPCHA04	Compare Window A Channel Select	0: Compare function disabled for the associated input channel 1: Compare function enabled for the associated input channel. Bit [6] (CMPCHA06) corresponds to AN006 and Bit [4] (CMPCHA04) corresponds to AN004.	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10, b9	CMPCHA10, CMPCHA09	Compare Window A Channel Select	0: Compare function disabled for the associated input channel 1: Compare function enabled for the associated input channel. Bit [10] (CMPCHA10) corresponds to AN010 and Bit [9] (CMPCHA09) corresponds to AN009.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

在设置以下寄存器和位之前将此位设置为0：

- AD通道选择寄存器A0A1B0B1(ADANSA0 ADANSA1 ADANSB0 ADANSB1)
- AD转换扩展输入控制寄存器(ADEXICR)中的OCSA或TSSA位
- 窗口B通道选择寄存器(ADCMPBNSR)中的CMPCHB[5:0]位。

CMPAE位（比较窗口A操作使能）

CMPAE位启用或禁用比较窗口A操作。仅当ADCSR.ADST位为0时设置CMPAE位。

在设置以下寄存器和位之前将此位设置为0：

- AD通道选择寄存器A0A1B0B1(ADANSA0 ADANSA1 ADANSB0 ADANSB1)
- AD转换扩展输入控制寄存器(ADEXICR)中的OCSA或TSSA位
- 窗口A通道选择寄存器01(ADCMPANSR0 ADCMPANSR1)
- 窗口A扩展输入选择寄存器(ADCMPANSER)。

CMPBIE位（比较B中断使能）

当满足比较条件（窗口B）时，CMPBIE位启用或禁用ADC140_CMPBI中断输出。

WCMPE位（窗口功能设置）

WCMPE位启用或禁用窗口功能。仅当ADCSR.ADST位为0时设置WCMPE位。

CMPAIE位（比较中断使能）

当满足比较条件（窗口A）时，CMPAIE位启用或禁用ADC140_CMPAI中断输出。

34.2.18 AD比较功能窗口A通道选择寄存器0(ADCMPANSR0)

Address(es): ADC140.ADCMPANSR0 4005 C094h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPCHA10	CMPCHA09	—	—	CMPCHA06	CMPCHA05	CMPCHA04	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	CMPCHA06 to CMPCHA04	比较窗口A通道 Select	0：关联输入通道的比较功能禁用1：关联输入通道的比较功能启用。位[6](CMPCHA06)对应于AN006和 位[4](CMPCHA04)对应于AN004。	R/W
b8, b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10, b9	CMPCHA10, CMPCHA09	比较窗口A通道 Select	0：关联输入通道的比较功能禁用1：关联输入通道的比较功能启用。位[10](CMPCHA10)对应于AN010和 位[9](CMPCHA09)对应于AN009。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPCHAn bits (n = 04 to 06, 09, and 10) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA0.ANSAn bits (n = 04 to 06, 09, and 10) and the ADANSB0.ANSBn bits (n = 04 to 06, 09, and 10).

Only set the CMPCHAn bits when the ADCSR.ADST bit is 0.

34.2.19 A/D Compare Function Window A Channel Select Register 1 (ADCMPANSR1)

Address(es): ADC140.ADCMPANSR1 4005 C096h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPCHA20	CMPCHA19	—	CMPCHA17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	CMPCHA17	Compare Window A Channel Select	0: Compare function disabled for the associated input channel 1: Compare function enabled for the associated input channel Bit [1] (CMPCHA17) corresponds to AN017.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	CMPCHA20, CMPCHA19	Compare Window A Channel Select	0: Compare function disabled for the associated input channel 1: Compare function enabled for the associated input channel Bit [4] (CMPCHA20) corresponds to AN020 and Bit [3] (CMPCHA19) corresponds to AN019.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 17, 19, and 20) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA1.ANSAn bits (n = 17, 19, and 20) and the ADANSB1.ANSBn bits (n = 17, 19, and 20).

Only set the CMPCHAn bits while the ADCSR.ADST bit is 0.

34.2.20 A/D Compare Function Window A Extended Input Select Register (ADCMPANSER)

Address(es): ADC140.ADCMPANSER 4005 C092h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPTSA	Temperature Sensor Output Compare Select	0: Exclude the temperature sensor output from the compare window A target range 1: Include the temperature sensor output in the compare window A target range.	R/W
b1	CMPOCA	Internal Reference Voltage Compare Select	0: Exclude the internal reference voltage from the compare window A target range 1: Include the internal reference voltage in the compare window A target range.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn位（n=04到06、09和10）（比较窗口A通道选择）

通过将1写入CMPCHAn位来启用比较功能，该位与在ADANSA0.ANSAN位（n=04至06、09和10）和ADANSB0.ANSBn位（n=04）中选择的AD转换通道的编号相同到06、09和10）。

仅当ADCSR.ADST位为0时设置CMPCHAn位。

34.2.19 AD比较功能窗口A通道选择寄存器1(ADCMPANSR1)

Address(es): ADC140.ADCMPANSR1 4005 C096h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPCHA20	CMPCHA19	—	CMPCHA17	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	CMPCHA17	比较窗口A通道 Select	0：禁用相关输入通道的比较功能1：启用相关输入通道的比较功能Bit[1](CMPCHA17)对应于AN017。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b4, b3	CMPCHA20, CMPCHA19	比较窗口A通道 Select	0：禁用相关输入通道的比较功能1：启用相关输入通道的比较功能Bit[4](CMPCHA20)对应于AN020和 位[3](CMPCHA19)对应于AN019。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPCHAn位（n=17、19和20）（比较窗口A通道选择）

通过将1写入CMPCHAn位来启用比较功能，该位与在ADANSA1.ANSAn位（n=17、19和20）和ADANSB1.ANSBn位（n=17、19）中选择的AD转换通道的编号相同 和20)。

仅在ADCSR.ADST位为0时设置CMPCHAn位。

34.2.20 AD比较功能窗口A扩展输入选择寄存器(ADCMPANSER)

Address(es): ADC140.ADCMPANSER 4005 C092h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPOCA	CMPTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPTSA	温度感应器输出比较选择	0：将温度传感器输出排除在比较窗口A目标范围内1：将温度传感器输出包括在比较窗口A目标范围内。	R/W
b1	CMPOCA	内部参考电压比较选择	0：在比较窗口A目标范围内排除内部参考电压1：在比较窗口A目标范围内包括内部参考电压。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare window A function is enabled by setting the CMPTSA bit to 1 when the ADEXICR.TSSA bit is 1.

Only set the CMPTSA bit when the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare window A function is enabled by setting the CMPOCA bit to 1 when the ADEXICR.OCSA bit is 1.

Only set the CMPOCA bit when the ADCSR.ADST bit is 0.

34.2.21 A/D Compare Function Window A Comparison Condition Setting Register 0 (ADCMPLR0)

Address(es): ADC140.ADCMPLR0 4005 C098h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPLCHA10	CMPLCHA09	—	—	CMPLCHA06	CMPLCHA05	CMPLCHA04	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	CMPLCHA06 to CMPLCHA04	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels AN004 to AN006 to which window A comparison conditions are applied. Comparison conditions are shown in Figure 34.3. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10, b9	CMPLCHA10, CMPLCHA09	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels AN009, and AN010 to which window A comparison conditions are applied. Comparison conditions are shown in Figure 34.3. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ACMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 04 to 06, 09, and 10) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels AN004 to AN006, AN009, and AN010 to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. CMPLCHA04, CMPLCHA06, CMPLCHA10 correspond to AN004, AN006, and AN010, respectively. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

CMPTSA位（温度传感器输出比较选择）

当ADEXICR.TSSA位为1时，通过将CMPTSA位设置为1来启用比较窗口A功能。

仅当ADCSR.ADST位为0时设置CMPTSA位。

CMPOCA位（内部参考电压比较选择）

当ADEXICR.OCSA位为1时，通过将CMPOCA位设置为1来启用比较窗口A功能。

仅当ADCSR.ADST位为0时设置CMPOCA位。

34.2.21 AD比较功能窗口A比较条件设置寄存器0(ADCMPLR0)

Address(es): ADC140.ADCMPLR0 4005 C098h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPLCHA10	CMPLCHA09	—	—	CMPLCHA06	CMPLCHA05	CMPLCHA04	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	CMPLCHA06 to CMPLCHA04	比较窗口A比较条件 Select	这些位设置应用窗口A比较条件的通道AN004到AN006的比较条件。比较条件如图34.3所示。 当窗口功能被禁用时（ADCMPCR.WCMPE=0）：0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。启用窗口功能时(ADCMPCR.WCMPE=1)：0：D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W
b8, b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10, b9	CMPLCHA10, CMPLCHA09	比较窗口A比较条件 Select	这些位设置应用窗口A比较条件的通道AN009和AN010的比较条件。 比较条件如图34.3所示。 当窗口功能被禁用时（ADCMPCR.WCMPE=0）：0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。启用窗口功能时(ADCMPCR.WCMPE=1)：0：D转换值<ACMPDR0值，或ADCMPDR1值<AD转换值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPLCHAn位（n=04到06、09和10）（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的通道AN004到AN006、AN009和AN010的比较条件。可以为要比较的每个模拟输入设置这些位。CMPLCHA04、CMPLCHA06、CMPLCHA10分别对应AN004、AN006和AN010。当每个模拟输入的比较结果满足设置条件时，ADCMPSR0.CMPSTCHAn位设置为1，并产生比较中断（ADC140_CMPAI）。

Comparison conditions when the window function is disabled

CMPLCHAn = 0

ADCMPDR0 value ≤ A/D converted value	Not met
ADCMPDR0 value > A/D converted value	Met

CMPLCHAn = 1

ADCMPDR0 value < A/D converted value	Met
ADCMPDR0 value ≥ A/D converted value	Not met

Comparison conditions when the window function is enabled

CMPLCHAn = 0

ADCMPDR1 value < A/D converted value	Met
ADCMPDR0 value ≤ A/D converted value ≤ ADCMPDR1 value	Not met
A/D converted value < ADCMPDR0 value	Met

CMPLCHAn = 1

ADCMPDR1 value ≤ A/D converted value	Not met
ADCMPDR0 value < A/D converted value < ADCMPDR1 value	Met
A/D converted value ≤ ADCMPDR0 value	Not met

Figure 34.3 Comparison conditions for compare function window A

34.2.22 A/D Compare Function Window A Comparison Condition Setting Register 1 (ADCMPLR1)

Address(es): ADC140.ADCMPLR1 4005 C09Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPLCHA20	CMPLCHA19	—	CMPLCHA17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

禁用窗口功能时的比较条件

CMPLCHAn = 0

ACMPDDR0值 AD转换值	没见过
ACMPDDR0值>AD转换值	Met

CMPLCHAn = 1

ACMPDDR0值<AD转换值	Met
ACMPDDR0值 AD转换值	没见过

启用窗口功能时的比较条件

CMPLCHAn = 0

ADCMPDDR1值<AD转换值	Met
ADCMPDR0值 AD转换值 ADCMPDR1值	没见过
AD转换值<ADCMPDR0值	Met

CMPLCHAn = 1

ACMPDDR1值 AD转换值	没见过
ADCMPDR0值<AD转换值<ADCMPDR1值	Met
AD转换值 ADCMPDR0值	没见过

Figure 34.3 比较功能窗口A的比较条件

34.2.22 AD比较功能窗口A比较条件设置寄存器1(ADCMPLR1)

Address(es): ADC140.ADCMPLR1 4005 C09Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPLCHA20	CMPLCHA19	—	CMPLCHA17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	CMPLCHA17	Compare Window A Comparison Condition Select	This bit sets comparison conditions for channel AN017 to which window A comparison conditions are applied. Comparison conditions are shown in Figure 34.3. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ACMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	CMPLCHA20, CMPLCHA19	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels AN019, and AN020 to which window A comparison conditions are applied. Comparison conditions are shown in Figure 34.3. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ACMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 17, 19, and 20) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels AN017, AN019, and AN020 to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. CMPLCHA17, CMPLCHA19, and CMPLCHA20 correspond to AN017, AN019, and AN020, respectively. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

34.2.23 A/D Compare Function Window A Extended Input Comparison Condition Setting Register (ADCMPLER)

Address(es): ADC140.ADCMPLER 4005 C093h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select	Comparison conditions are shown in Figure 34.3. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE bit = 1): 0: A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select	Comparison conditions are shown in Figure 34.3. • When the window function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE bit = 1): 0: A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	位名称	Description	R/W
b1	CMPLCHA17	比较窗口A比较条件Select	该位设置应用窗口A比较条件的通道AN017的比较条件。比较条件如图34.3所示。 当窗口功能被禁用时（ADCMPCR.WCMPE=0）：0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)：0：D转换值<ACMPDR0值，或ADCMPDR1值<AD转换值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b4, b3	CMPLCHA20, CMPLCHA19	比较窗口A比较条件Select	这些位设置应用窗口A比较条件的通道AN019和AN020的比较条件。 比较条件如图34.3所示。 当窗口功能被禁用时（ADCMPCR.WCMPE=0）：0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)：0：D转换值<ACMPDR0值，或ADCMPDR1值<AD转换值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPLCHAn位（n=17、19和20）（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的通道AN017、AN019和AN020的比较条件。可以为要比较的每个模拟输入设置这些位。CMPLCHA17、CMPLCHA19和CMPLCHA20分别对应于AN017、AN019和AN020。当每个模拟输入的比较结果满足设置条件时，ADCMPSR1.CMPSTCHAn位设置为1，并产生比较中断（ADC140_CMPAI）。

34.2.23 AD比较功能窗口A扩展输入比较条件设置寄存器(ADCMPLER)

Address(es): ADC140.ADCMPLER 4005 C093h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPLOCA	CMPLTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPLTSA	比较窗口A温度传感器输出比较条件选择	比较条件如图34.3所示。 当窗口功能被禁用时（ADCMPCR.WCMPE=0）：0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 当窗口功能启用时（ADCMPCR.WCMPE位=1）：0：D转换值<ADCMPDR0值，或D转换值>ADCMPDR1值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W
b1	CMPLOCA	比较窗口A内部参考电压比较条件选择	比较条件如图34.3所示。 当窗口功能被禁用时（ADCMPCR.WCMPE位=0）：0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 当窗口功能启用时（ADCMPCR.WCMPE位=1）：0：D转换值<ADCMPDR0值，或D转换值>ADCMPDR1值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies comparison conditions when the temperature sensor output is the target of the window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA flag is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies comparison conditions when the internal reference voltage is the target of the window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA flag is set to 1 and a compare interrupt (ADC140_CMPAI) is generated.

34.2.24 A/D Compare Function Window A Lower-Side Level Setting Register (ADCMPDR0), A/D Compare Function Window A Upper-Side Level Setting Register (ADCMPDR1), A/D Compare Function Window B Lower-Side Level Setting Register (ADWINLLB), A/D Compare Function Window B Upper-Side Level Setting Register (ADWINULB)

Address(es): ADC140.ADCMPDR0 4005 C09Ch, ADC140.ADCMPDR1 4005 C09Eh, ADC140.ADWINLLB 4005 C0A8h, ADC140.ADWINULB 4005 C0AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	Reference value	R/W

The ADCMPDRy (y = 0, 1) register specifies the reference data when the compare window A function is used. ADCMPDR0 sets the lower reference for window A, and ADCMPDR1 sets the upper reference for window A.

The ADWINULB and ADWINLLB registers specify the reference data when the compare window B function is used. ADWINLLB sets the lower reference for window B, and ADWINULB sets the upper reference for window B.

ADCMPDRy, ADWINULB, and ADWINLLB are read/write registers.

ADCMPDRy, ADWINULB, and ADWINLLB are writable even during A/D conversion. The reference data can be dynamically modified by rewriting register values during A/D conversion.*1

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0, ADWINULB ≥ ADWINLLB). ADCMPDR1 and ADWINULB are not used when the window function is disabled.

Note 1. The lower and the upper reference values are changed when each register is written. For example, when the upper reference value and the lower reference value are changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 34.4. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) is 0.

CMPLTSA位（比较窗口A温度传感器输出比较条件选择）

当温度传感器输出是窗口A比较条件的目标时，CMPLTSA位指定比较条件。当温度传感器输出比较结果满足设置条件时，ADCMPSER.CMPSTTSA标志置1并产生比较中断（ADC140_CMPAI）。

CMPLOCA位（比较窗口A内部参考电压比较条件选择）

当内部参考电压是窗口A比较条件的目标时，CMPLOCA位指定比较条件。当内部参考电压比较结果满足设置条件时，ADCMPSER.CMPSTOCA标志置1并产生比较中断（ADC140_CMPAI）。

34.2.24 AD比较功能窗口A低端电平设置寄存器(ADCMPDR0) AD比较功能窗口A高端电平设置寄存器(ADCMPDR1) AD比较功能窗口B低端电平设置寄存器(ADWINLLB) AD比较功能窗口B上侧

电平设置寄存器(ADWINULB)

Address(es): ADC140.ADCMPDR0 4005 C09Ch, ADC140.ADCMPDR1 4005 C09Eh, ADC140.ADWINLLB 4005 C0A8h, ADC140.ADWINULB 4005 C0AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	参考值	R/W

ADCMPDRy(y=0 1)寄存器指定使用比较窗口A功能时的参考数据。ADCMPDDR0设置窗口A的下参考值，而ADCMPDR1设置窗口A的上参考值。

ADWINULB和ADWINLLB寄存器指定使用比较窗口B功能时的参考数据。
ADWINLLB设置窗口B的下参考，ADWINULB设置窗口B的上参考。

ADCMPDRy、ADWINULB和ADWINLLB是读写寄存器。

ADCMPDRy、ADWINULB和ADWINLLB即使在AD转换期间也是可写的。参考数据可以通过在AD转换期间重写寄存器值来动态修改。*1

设置这些寄存器，使参考上限不小于参考下限(ADCMPDR1　ADCMPDR0
ADWINULB　ADWINLLB）。禁用窗口功能时不使用ACMPDDR1和ADWINULB。

注1.写入每个寄存器时，下限和上限参考值会发生变化。例如，当
改变上参考值和下参考值，MCU将上参考（重写后）和下参考（重写前）与AD转换结果进行比较。请参见图34.4。如果在重写这两个参考时比较错误，则在ADCSR.ADST和目标比较窗口操作使能位（ADCMPCR.CMPAE或ADCMPCR.CMPBE）均为0时重写这些参考值。

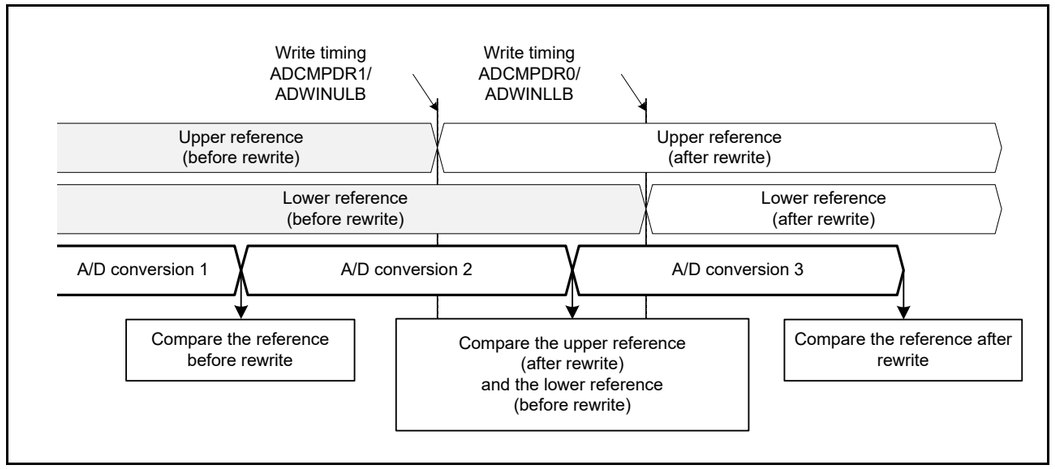


Figure 34.4 Comparison between upper reference and lower reference before and after a rewrite

The ADCMPDRy, ADWINLLB, and ADWINULB registers use different formats depending on the following conditions:

- The value of the A/D Data Register Format Select bit (flush-right or flush-left)
- The value of the A/D Conversion Accuracy Specify bit (14-bit or 12-bit)
- The value of the A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each given condition are as follows:

(1) When A/D-converted value addition mode is not selected

- Flush-right data with 14-bit accuracy: Lower 14 bits [13:0] are valid
- Flush-right data with 12-bit accuracy: Lower 12 bits [11:0] are valid
- Flush-left data with 14-bit accuracy: Upper 14 bits [15:2] are valid
- Flush-left data with 12-bit accuracy: Upper 12 bit [15:4] are valid.

(2) When A/D-converted value addition mode is selected

- Flush-right data with 14-bit accuracy: All bits [15:0] are valid
- Flush-right data with 12-bit accuracy: Lower 14 bits [13:0] are valid
- Flush-left data with 14-bit accuracy: All bits [15:0] are valid
- Flush-left data with 12-bit accuracy: Upper 14 bits [15:2] are valid.

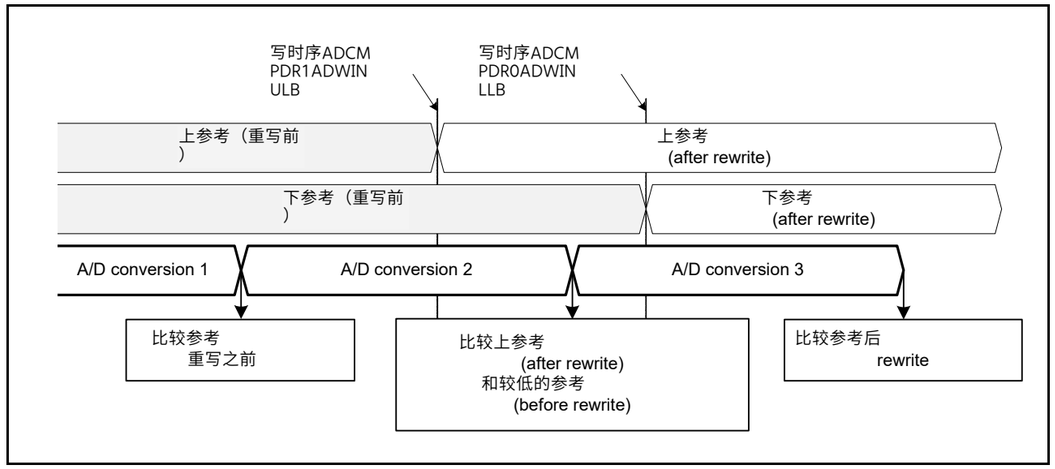


Figure 34.4 重写前后上参考和下参考的比较

ADCMPDRy、ADWINLLB和ADWINULB寄存器根据以下条件使用不同的格式：

- AD数据寄存器格式选择位的值（右对齐或左对齐）
- AD转换精度指定位的值（14位或12位）
- AD转换值相加平均通道选择位的值（选择或未选择AD转换值相加模式）。

每个给定条件的数据格式如下：

(1) 未选择AD转换值相加模式时

- 14位精度的右冲洗数据：低14位[13:0]有效
- 12位精度的右冲洗数据：低12位[11:0]有效
- 14位精度的左刷新数据：高14位[15:2]有效
- 12位精度的左刷新数据：高12位[15:4]有效。

(2) 选择AD转换值相加模式时

- 具有14位精度的右刷新数据：所有位[15:0]均有效
- 12位精度的右冲洗数据：低14位[13:0]有效
- 14位精度的左刷新数据：所有位[15:0]均有效
- 12位精度的左刷新数据：高14位[15:2]有效。

34.2.25 A/D Compare Function Window A Channel Status Register 0 (ADCMPSR0)

Address(es): ADC140.ADCMPSR0 4005 C0A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPSTCHA10	CMPSTCHA09	—	—	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	CMPSTCHA06 to CMPSTCHA04	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result for channels AN004 to AN006, to which window A comparison conditions are applied: 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10, b9	CMPSTCHA10, CMPSTCHA09	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result for channels AN009 and AN010, to which window A comparison conditions are applied: 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn bits (n = 04 to 06, 09, and 10) (Compare Window A Flag)

The CMPSTCHAn bits are comparison result status flags for channels AN004 to AN006, AN009, and AN010 to which window A comparison conditions are applied. When the comparison condition set in ADCMPLR0.CMPLCHAn is met at the end of A/D conversion, the corresponding bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when this bit is set to 1. CMPSTCHA04, CMPSTCHA06, and CMPSTCHA10 correspond to AN004, AN006, and AN010, respectively.

Writing 1 to the CMPSTCHAn bits is invalid.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

34.2.26 A/D Compare Function Window A Channel Status Register 1 (ADCMPSR1)

Address(es): ADC140.ADCMPSR1 4005 C0A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPSTCHA20	CMPSTCHA19	—	CMPSTCHA17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	CMPSTCHA17	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), this bit indicates the comparison result for channels AN017, to which window A comparison conditions are applied: 0: Comparison conditions not met 1: Comparison conditions met.	R/W

34.2.25 AD比较功能窗口A通道状态寄存器0(ADCMPSR0)

Address(es): ADC140.ADCMPSR0 4005 C0A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPSTCHA10	CMPSTCHA09	—	—	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	CMPSTCHA06 to CMPSTCHA04	比较窗口A标志	当窗口A操作使能（ADCMPCR.CMPAE=1b）时，这些位指示通道AN004到AN006的比较结果，窗口A比较条件应用于该通道：0：不满足比较条件1：满足比较条件。	R/W
b8, b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10, b9	CMPSTCHA10, CMPSTCHA09	比较窗口A标志	当窗口A操作使能（ADCMPCR.CMPAE=1b）时，这些位指示通道AN009和AN010的比较结果，窗口A比较条件适用于该通道：0：不满足比较条件1：满足比较条件。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTCHAn位（n=04到06、09和10）（比较窗口A标志）

CMPSTCHAn位是应用窗口A比较条件的通道AN004到AN006、AN009和AN010的比较结果状态标志。当ADCMPLR0.CMPLCHAn中设置的比较条件在AD转换结束时满足，相应位设置为1。当ADCMPCR.CMPAIE位为1时，当该位设置为时产生比较中断（ADC140_CMPAI）请求1.CMPSTCHA04、CMPSTHA06、CMPSTTCHA10分别对应AN004、AN006、AN010。

向CMPSTCHAn位写入1无效。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLR0.CMPLCHAn中设置的条件。

[Clearing condition]

- 读1后写0。

34.2.26 AD比较功能窗口A通道状态寄存器1(ADCMPSR1)

Address(es): ADC140.ADCMPSR1 4005 C0A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPSTCHA20	CMPSTCHA19	—	CMPSTCHA17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	CMPSTCHA17	比较窗口A标志	当窗口A操作使能时（ADCMPCR.CMPAE=1b），该位指示通道AN017的比较结果，应用窗口A比较条件：0：不满足比较条件1：满足比较条件。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	CMPSTCHA20, CMPSTCHA19	Compare Window A Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result for channels AN019 and AN020, to which window A comparison conditions are applied: 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn bits (n = 17, 19, and 20) (Compare Window A Flag)

The CMPSTCHAn bits are comparison result status flags for channels AN017, AN019, and AN020, to which window A comparison conditions are applied. When the comparison condition set in ADCMPLR1.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when this bit is set to 1. CMPSTCHA17, CMPSTCHA19, and CMPSTCHA20 correspond to AN017, AN019, and AN020, respectively.

Writing 1 to the CMPSTCHAn bits is invalid.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

34.2.27 A/D Compare Function Window A Extended Input Channel Status Register (ADCMPSER)

Address(es): ADC140.ADCMPSER 4005 C0A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result: 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag	When window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result: 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTTSA bit (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA bit is a status flag that indicates the temperature sensor output comparison result. When the comparison condition set in ADCMPLER.CMPLTSA is met at the end of A/D conversion, this bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when this bit is set to 1.

Writing 1 to the CMPSTTSA bit is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

Bit	Symbol	位名称	Description	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b4, b3	CMPSTCHA20, CMPSTCHA19	比较窗口A标志	当窗口A操作使能时（ADCMPCR.CMPAE=1b），这些位指示通道AN019和AN020的比较结果，窗口A比较条件适用于：0：不满足比较条件1：满足比较条件。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTCHAn位（n=17、19和20）（比较窗口A标志）

CMPSTCHAn位是通道AN017、AN019和AN020的比较结果状态标志，应用窗口A比较条件。当ADCMPLR1.CMPLCHAn中设置的比较条件在AD转换结束时满足，相关的CMPSTCHAn位被设置为1。当ADCMPCR.CMPAIE位为1时，当该位置位时产生比较中断（ADC140_CMPAI）请求到1.CMPSTCHA17、CMPSTCHA19和CMPSTTCHA20分别对应于AN017、AN019和AN020。

向CMPSTCHAn位写入1无效。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLR1.CMPLCHAn中设置的条件。

[Clearing condition]

- 读1后写0。

34.2.27 AD比较功能窗口A扩展输入通道状态寄存器(ADCMPSER)

Address(es): ADC140.ADCMPSER 4005 C0A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPSTTSA	比较窗口A 温度传感器输出 比较标志	当窗口A操作使能（ADCMPCR.CMPAE=1）时，该位指示温度传感器输出比较结果：0：不满足比较条件1：满足比较条件。	R/W
b1	CMPSTOCA	比较窗口A内部参考电压比较 Flag	当窗口A操作使能（ADCMPCR.CMPAE=1）时，该位指示内部参考电压比较结果：0：不满足比较条件1：满足比较条件。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTTSA位（比较窗口A温度传感器输出比较标志）

CMPSTTSA位是指示温度传感器输出比较结果的状态标志。当ADCMPLER.CMPLTSA中设置的比较条件在AD转换结束时满足，该位设置为1。当ADCMPCR.CMPAIE位为1时，当该位设置为1时产生比较中断（ADC140_CMPAI）请求.

将1写入CMPSTTSA位无效。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLTSA中设置的条件。

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA bit (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA bit is a status flag that indicates the internal reference voltage comparison result. When the comparison condition set in ADCMPLER.CMPLOCA is met at the end of A/D conversion, this bit is set to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt (ADC140_CMPAI) request is generated when this bit is set to 1.

Writing 1 to the CMPSTOCA bit is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

34.2.28 A/D Compare Function Window B Channel Select Register (ADCMPBNSR)

Address(es): ADC140.ADCMPBNSR 4005 C0A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CMPCHB[5:0]	Compare Window B Channel Select	These bits select channels to be compared with the compare window B conditions: b5 b0 0 0 0 1 0 0: AN004 0 0 0 1 0 1: AN005 0 0 0 1 1 0: AN006 0 0 1 0 0 1: AN009 0 0 1 0 1 0: AN010 0 1 0 0 0 1: AN017 0 1 0 0 1 1: AN019 0 1 0 1 0 0: AN020 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage 1 1 1 1 1 1: Not select. Other settings are prohibited.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	CMPLB	Compare Window B Comparison Condition Setting	This bit sets comparison conditions for channels for window B. The comparison conditions are shown in Figure 34.5. • When the window function is disabled (ADCMPCR.WCMPE = 0): 0: ADWINLLB value > A/D-converted value 1: ADWINLLB value < A/D-converted value. • When the window function is enabled (ADCMPCR.WCMPE = 1): 0: A/D-converted value < ADWINLLB value, or ADWINULB value < A/D-converted value 1: ADWINLLB value < A/D-converted value < ADWINULB value.	R/W

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits select channels to be compared with the compare window B conditions AN004 to AN006, AN009, AN010, AN017, AN019, and AN020, the temperature sensor, and the internal reference voltage. The compare window B function is enabled by specifying the hexadecimal number of the A/D conversion channel selected in the following bits:

- ADANSA0.ANSAn bits (n = 04 to 06, 09, and 10)

[Clearing condition]

- 读1后写0。

CMPSTOCA位（比较窗口A内部参考电压比较标志）

CMPSTOCA位是指示内部参考电压比较结果的状态标志。当ADCMPLER.CMPLOCA中设置的比较条件在AD转换结束时满足，该位设置为1。当ADCMPCR.CMPAIE位为1时，该位设置为1时产生比较中断（ADC140_CMPAI）请求.

将1写入CMPSTOCA位无效。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLOCA中设置的条件。

[Clearing condition]

- 读1后写0。

34.2.28 AD比较功能窗口B通道选择寄存器(ADCMPBNSR)

Address(es): ADC140.ADCMPBNSR 4005 C0A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPLB	—	CMPCHB[5:0]					
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	CMPCHB[5:0]	比较窗口B 频道选择	这些位选择要与比较窗口进行比较的通道 B conditions: b5 b0 0 0 0 1 0 0: AN004 0 0 0 1 0 1: AN005 0 0 0 1 1 0: AN006 0 0 1 0 0 1: AN009 0 0 1 0 1 0: AN010 0 1 0 0 0 1: AN017 0 1 0 0 1 1: AN019 0 1 0 1 0 0: AN020 1 0 0 0 0 0：温度传感器 1 0 0 0 0 1：内部参考电压 11：不选择。禁止其他设置。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	CMPLB	比较窗口B 比较条件 Setting	该位设置窗口B的通道比较条件。比较条件如图34.5所示。 禁用窗口功能时(ADCMPCR.WCMPE=0)：0：ADWINLLB值>AD转换值1：ADWINLLB值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)：0：D转换值<ADWINLLB值，或ADWINULB值<AD转换值1：ADWINLLB值<AD转换值<ADWINULB值。	R/W

CMPCHB[5:0]位（比较窗口B通道选择）

CMPCHB[5:0]位选择要与比较窗口B条件AN004至AN006、AN009、AN010、AN017、AN019和AN020、温度传感器和内部参考电压进行比较的通道。通过指定在以下位中选择的AD转换通道的十六进制数来启用比较窗口B功能：

- ADANSA0.ANSan位（n=04到06、09和10）

- ADANSA1.ANSAn bits (n = 17, 19, and 20)
- ADANSB0.ANSBn bits (n = 04 to 06, 09, and 10)
- ADANSB1.ANSBn bits (n = 17, 19, and 20).

Set CMPCHB[5:0] bits while the ADCSR.ADST bit is 0.

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit selects the comparison conditions for channels for window B. When the comparison result of each analog input meets the set condition, the ADCMPBSR.CMPSTB bit is set to 1 and a compare interrupt (ADC140_CMPBI) request is generated.

Compare conditions when the window function is disabled

CMPLB = 0		CMPLB = 1	
ADWINLLB value ≤ A/D converted value	Not met	ADWINLLB value < A/D converted value	Met
ADWINLLB value > A/D converted value	Met	ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value < A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 34.5 Compare conditions for compare function window B

- ADANSA1.ANSAN位（n=17、19和20）
- ADANSB0.ANSBn位（n=04到06、09和10）
- ADANSB1.ANSBn位（n=17、19和20）。

当ADCSR.ADST位为0时，设置CMPCHB[5:0]位。

CMPLB位（比较窗口B比较条件设置）

CMPLB位选择窗口B的通道比较条件。当每个模拟输入的比较结果满足设置条件时，ADCMPBSR.CMPSTB位设置为1，并产生比较中断（ADC140_CMPBI）请求。

比较禁用窗口功能时的条件

CMPLB = 0		CMPLB = 1	
ADWINLLB值　AD转换值	没见过	ADWINLLB值<AD转换值	Met
ADWINLLB值>AD转换值	Met	ADWINLLB值　AD转换值	没见过

启用窗口功能时比较条件

CMPLB = 0

AD转换值>ADWINULB值	Met
ADWINLLB值　AD转换值　ADWINULB值	没见过
AD转换值<ADWINLLB值	Met

CMPLB = 1

AD转换值　ADWINULB值	没见过
ADWINLLB值<AD转换值<ADWINULB值	Met
AD转换值　ADWINLLB值	没见过

Figure 34.5 比较功能窗口B的比较条件

34.2.29 A/D Compare Function Window B Status Register (ADCMPBSR)

Address(es): ADC140.ADCMPBSR 4005 C0ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTB	Compare Window B Flag	When window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result for channels AN004 to AN006, AN009, AN010, AN017, AN019, and AN020, temperature sensor output, and internal reference voltage, to which window B comparison conditions are applied: 0: Comparison conditions not met 1: Comparison conditions met.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTB bit (Compare Window B Flag)

The CMPSTB bit is a status flag that indicates the comparison result for channels AN004 to AN006, AN009, AN010, AN017, AN019, and AN020, the temperature sensor, and the internal reference voltage, to which window B comparison conditions are applied. When the comparison condition set in ADCMPBNSR.CMPLB is met at the end of A/D conversion, this bit is set to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt (ADC140_CMPBI) request is generated when this bit is set to 1.

Writing 1 to the CMPSTB bit is invalid.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

34.2.30 A/D Compare Function Window A/B Status Monitor Register (ADWINMON)

Address(es): ADC140.ADWINMON 4005 C08Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MONCOMB	Combination Result Monitor	This bit indicates the combination result. This bit is valid when both window A and window B operations are enabled: 0: Window A/window B composite conditions not met 1: Window A/window B composite conditions met.	R
b3 to b1	—	Reserved	These bits are read as 0.	R
b4	MONCMPA	Comparison Result Monitor A	0: Window A comparison conditions not met 1: Window A comparison conditions met.	R
b5	MONCMPB	Comparison Result Monitor B	0: Window B comparison conditions not met 1: Window B comparison conditions met.	R
b7, b6	—	Reserved	These bits are read as 0.	R

34.2.29 AD比较功能窗口B状态寄存器(ADCMPBSR)

Address(es): ADC140.ADCMPBSR 4005 C0ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTB
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPSTB	比较窗口B标志	当窗口B操作使能（ADCMPCR.CMPBE=1）时，该位指示通道AN004到AN006、AN009、AN010、AN017、AN019和AN020、温度传感器输出和内部参考电压的比较结果，窗口B应用比较条件：0：不满足比较条件1：满足比较条件。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTB位（比较窗口B标志）

CMPSTB位是一个状态标志，指示通道AN004到AN006、AN009、AN010、AN017、AN019和AN020、温度传感器和内部参考电压，应用窗口B比较条件。当ADCMPBNSR.CMPLB中设置的比较条件在AD转换结束时满足，该位设置为1。当ADCMPCR.CMPBIE位为1时，该位设置为1时产生比较中断（ADC140_CMPBI）请求.

将1写入CMPSTB位无效。

[Setting condition]

- 当ADCMPCR.CMPBE=1时，满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing condition]

- 读1后写0。

34.2.30 AD比较功能窗口AB状态监控寄存器(ADWINMON)

Address(es): ADC140.ADWINMON 4005 C08Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MONCOMB	组合结果监视器	该位指示组合结果。当窗口A和窗口B操作都使能时，该位有效：0：不满足窗口A窗口B复合条件1：满足窗口A窗口B复合条件。	R
b3 to b1	—	Reserved	这些位读为0。	R
b4	MONCMPA	比较结果监视器A	0：不满足窗口A比较条件1：满足窗口A比较条件。	R
b5	MONCMPB	比较结果监视器B	0：不满足窗口B比较条件1：满足窗口B比较条件。	R
b7, b6	—	Reserved	这些位读为0。	R

MONCOMB bit (Combination Result Monitor)

The read-only MONCOMB bit indicates the combined result of comparison condition results A and B with the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only MONCMPA bit is read as 1 when the A/D-converted value of the window A target channel meets the condition set in ADCMPLR0/ADCMPLR1 and ADCMPLER. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPLR0.CMPLCHAn when ADCMPCR.CMPAE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPLR0.CMPLCHAn when ADCMPCR.CMPAE = 1
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only MONCMPB bit is read as 1 when the A/D-converted value of the window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

34.2.31 A/D High-Potential/Low-Potential Reference Voltage Control Register (ADHVREFCNT)

Address(es): ADC140.ADHVREFCNT 4005 C08Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ADSLP	—	—	LVSEL	—	—	HVSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	HVSEL[1:0]	High-Potential Reference Voltage Select	b1 b0 0 0: AVCC0 is selected as the high-potential reference voltage 0 1: VREFH0 is selected as the high-potential reference voltage 1 0: Internal reference voltage is selected as the high-potential reference voltage 1 1: Internal node discharge. No reference voltage pin is selected.	R/W

MONCOMB位（组合结果监视器）

只读MONCOMB位指示比较条件结果A和B与ADCMPCR.CMPAB[1:0]位中设置的组合条件的组合结果。

[Setting condition]

- 当组合结果满足ADCMPCR.CMPAB[1:0]位中设置的组合条件时
  ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- 组合结果不满足ADCMPCR.CMPAB[1:0]位中设置的组合条件
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA位（比较结果监视器A）

当窗口A目标通道的AD转换值满足ADCMPLR0ADCMPLR1和ADCMPLER中设置的条件时，只读MONCMPA位被读取为1。否则，读为0。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，AD转换后的值满足ADCMPLR0.CMPLCHAn中设置的条件。

[Clearing conditions]

- 当ADCMPCR.CMPAE=1时，AD转换后的值不满足ADCMPLR0.CMPLCHAn中设置的条件
- ADCMPCR.CMPAE=0（ADCMPCR.CMPAE值从1变为0时自动清零）。

MONCMPB位（比较结果监视器B）

当窗口B目标通道的AD转换值满足ADCMPBNSR.CMPLB位中设置的条件时，只读MONCMPB位被读取为1。否则，读为0。

[Setting condition]

- 当ADCMPCR.CMPBE=1时，AD转换后的值满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing conditions]

- 当ADCMPCR.CMPBE=
  1
- ADCMPCR.CMPBE=0（ADCMPCR.CMPBE值从1变为0时自动清零）。

34.2.31 AD高电位低电位参考电压控制寄存器(ADHVREFCNT)

Address(es): ADC140.ADHVREFCNT 4005 C08Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ADSLP	—	—	LVSEL	—	—	HVSEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	HVSEL[1:0]	High-Potential Reference 电压选择	b1 b0 0 0：选择AVCC0作为高电位参考电压 0 1：选择VREFH0作为高电位参考电压 1 0：选择内部参考电压作为高电位参考电压 1 1：内部节点放电。未选择参考电压引脚。	R/W

Bit	Symbol	Bit name	Description	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	LVSEL	Low-Potential Reference Voltage Select	0: AVSS0 is selected as the low-potential reference voltage 1: VREFL0 is selected as the low-potential reference voltage.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ADSLP	Sleep	0: Normal operation 1: Standby state.	R/W

HVSEL[1:0] bits (High-Potential Reference Voltage Select)

The HVSEL[1:0] bits specify the high-potential reference voltage as AVCC0, VREFH0, or the internal reference voltage (1.45 V).

Before selecting the internal reference voltage by setting these bits to 10b, set HVSEL[1:0] = 11b to discharge the path of the high-potential reference voltage. After the discharge completes, set HVSEL[1:0] = 10b and start the A/D conversion.

When the internal reference voltage is selected as the high-potential reference voltage (HVSEL[1:0] = 10b), A/D conversion is possible for channels AN004 to AN006, AN009, AN010, AN017, AN019, and AN020, but A/D conversion of the internal reference voltage and the temperature sensor output is prohibited.

LVSEL bit (Low-Potential Reference Voltage Select)

The LVSEL bit specifies the low-potential reference voltage as AVSS0 or VREFL0.

ADSLP bit (Sleep)

The ADSLP bit transitions the ADC14 to the standby state. Set the ADSLP bit to 1 only when modifying the ADCSR.ADHSC bit. In other cases, setting the ADSLP bit to 1 is prohibited.

After the ADSLP bit is set to 1, wait at least 5 µs before clearing it to 0. Also, after the ADSLP bit is set to 0, wait at least 1 µs, then start the A/D conversion.

For the ADHSC bit rewriting procedure, see section 34.8.8, ADHSC Bit Rewriting Procedure.

34.3 Operation

34.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

Scan conversion is performed in any of the three operating modes and two conversion modes.

The three operating modes are:

- Single scan mode
- Continuous scan mode
- Group scan mode.

The two conversion modes are:

- High-speed A/D conversion mode
- Low-power A/D conversion mode.

In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until software sets the ADCSR.ADST bit to 0 from 1. In group scan mode, the selected channels of group A and the selected channels of group B are scanned once after scan starts in response to the respective synchronous trigger (ELC).

In single scan mode and continuous scan mode, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed on the ANn channels in group A selected in the ADANSA0 and ADANSA1 registers first, and on the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers, respectively, starting from the channel with the smallest number n.

Bit	Symbol	位名称	Description	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	LVSEL	Low-Potential Reference 电压选择	0：选择AVSS0作为低电位参考电压1：选择VREFL0作为低电位参考电压。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	ADSLP	Sleep	0：正常运行1：待机状态。	R/W

HVSEL[1:0]位（高电位参考电压选择）

HVSEL[1:0]位将高电位参考电压指定为AVCC0、VREFH0或内部参考电压(1.45V)。

在通过将这些位设置为10b来选择内部参考电压之前，设置HVSEL[1:0]=11b以对高电位参考电压的路径进行放电。放电完成后，设置HVSEL[1:0]=10b并开始AD转换。

Whentheinternalreferencevoltageisselectedasthehigh-potentialreferencevoltage(HVSEL[1:0]=10b) AD conversionispossibleforchannelsAN004toAN006 AN009 AN010 AN017 AN019 andAN020 butADconversionof内部参考电压和温度传感器输出被禁止。

LVSEL位（低电位参考电压选择）

LVSEL位指定低电位参考电压为AVSS0或VREFL0。

ADSLP位（休眠）

ADLP位将ADC14转换为待机状态。仅在修改时将ADLP位设置为1 ADCSR.ADHSC位。在其他情况下，禁止将ADSLP位设置为1。

ADSLP位设置为1后，至少等待5微秒再将其清除为0。此外，在ADSLP位设置为0后，至少等待1微秒，然后开始AD转换。

有关ADHSC位重写过程，请参见第34.8.8节，ADHSC位重写过程。

34.3 Operation

34.3.1 扫描操作

扫描时，对指定通道的模拟输入依次进行AD转换。

扫描转换在三种操作模式和两种转换模式中的任何一种中执行。

三种操作模式是：

- 单次扫描模式
- 连续扫描模式
- 组扫描模式。

两种转换模式是：

- 高速模数转换模式
- 低功耗模数转换模式。

在单次扫描模式下，一个或多个指定通道被扫描一次。在连续扫描模式下，重复扫描一个或多个指定通道，直到软件将ADCSR.ADST位从1设置为0。在组扫描模式下，在扫描开始后，对A组的选定通道和B组的选定通道进行一次扫描响应相应的同步触发(ELC)。

在单次扫描模式和连续扫描模式下，在ADANSA0和ADANSA1寄存器，从编号n最小的通道开始。在组扫描模式下，首先对ADANSA0和ADANSA1寄存器中选择的A组ANn通道进行AD转换，然后分别对ADANSB0和ADANSB1寄存器中选择的B组ANn通道进行AD转换，从最小的通道开始号码n.

When self-diagnosis is selected, it is executed once at the beginning of each scan, and one of the three voltages internally generated in the ADC14 is converted.

Simultaneous selection of both temperature sensor output and internal reference voltage is prohibited. If the internal reference voltage is selected as the reference voltage on the high potential side, A/D conversion of the temperature sensor or the internal reference voltage is also prohibited. When temperature sensor output or internal reference voltage is selected, single scan mode should be used.

Double trigger mode can be used with single scan mode or group scan mode. With double trigger mode enabled (ADCSR.DBLE is 1), A/D conversion data of a channel selected in the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits. In group scan mode, only group A can use the double trigger mode.

In the extended operation of double trigger mode, the A/D conversion operation is generated from the synchronous trigger combination selected in the ADSTRGR.TRSA[5:0] bits. In addition to normal double trigger mode operation, A/D conversion data with odd number triggers (ELC_AD00) is stored into the A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data with even number triggers (ELC_AD01) is stored into the A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double trigger mode, when a combination of triggers occurs at the same time, data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored into the A/D Data Duplexing Register B (ADDBLDRB). The ADC14 ignores a synchronous trigger that occurs during the A/D conversion started by another synchronous trigger.

34.3.2 Single scan Mode

34.3.2.1 Basic operation

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as follows:

1. When the ADCSR.ADST bit is set to 1 (starting A/D conversion) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated.
4. The ADST bit remains 1 (starting A/D conversion) during A/D conversion, and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC14 then enters a wait state.

选择自诊断时，在每次扫描开始时执行一次，并转换ADC14内部产生的三个电压之一。

禁止同时选择温度传感器输出和内部参考电压。如果选择内部参考电压作为高电位侧的参考电压，温度传感器或内部参考电压的AD转换也被禁止。Whentemperaturesensoroutputorinternalreferencevoltageisselected singlescanmodeshouldbeused.

双触发模式可与单扫描模式或组扫描模式一起使用。启用双触发模式（ADCSR.DBLE为1）时，仅当转换由ADSTRGR中选择的同步触发(ELC)启动时，ADCSR.DBLANS[4:0]位中选择的通道的AD转换数据才会被复制.TRSA[5:0]位。在组扫描模式下，只有A组可以使用双触发模式。

在双触发模式的扩展操作中，ADSTRGR.TRSA[5:0]位中选择的同步触发组合产生AD转换操作。除了正常的双触发模式操作外，奇数触发的AD转换数据(ELC_AD00)存储到AD数据双工寄存器A(ADDBLDRA)，偶数触发的AD转换数据(ELC_AD01)存储到AD数据双工寄存器B(ADDBLDRB)。在双触发模式的扩展操作中，当同时发生触发组合时，指定触发的数据双工寄存器设置不起作用，AD转换数据存储到AD数据双工寄存器B（ADDBLDRB）中。ADC14忽略由另一个同步触发启动的AD转换期间发生的同步触发。

34.3.2 单次扫描模式

34.3.2.1 基本操作

在单扫描模式的基本操作中，对指定通道的模拟输入进行一次AD转换，如下所示：

1. 当ADCSR.ADST位通过软件触发、同步触发输入(ELC)或异步触发输入设置为1（开始AD转换）时，在ADANSA0和ADANSA1寄存器中选择的ANn通道上执行AD转换，从具有最小编号n的通道开始。
2. 每次单个通道的AD转换完成时，AD转换结果都会存储在相关的AD数据寄存器(ADDRy)中。
3. 当所有选定通道的AD转换完成时，会产生ADC140_ADI中断请求。
4. ADST位在AD转换期间保持为1（开始AD转换），并在所有选定通道的AD转换完成时自动设置为0。ADC14然后进入等待状态。

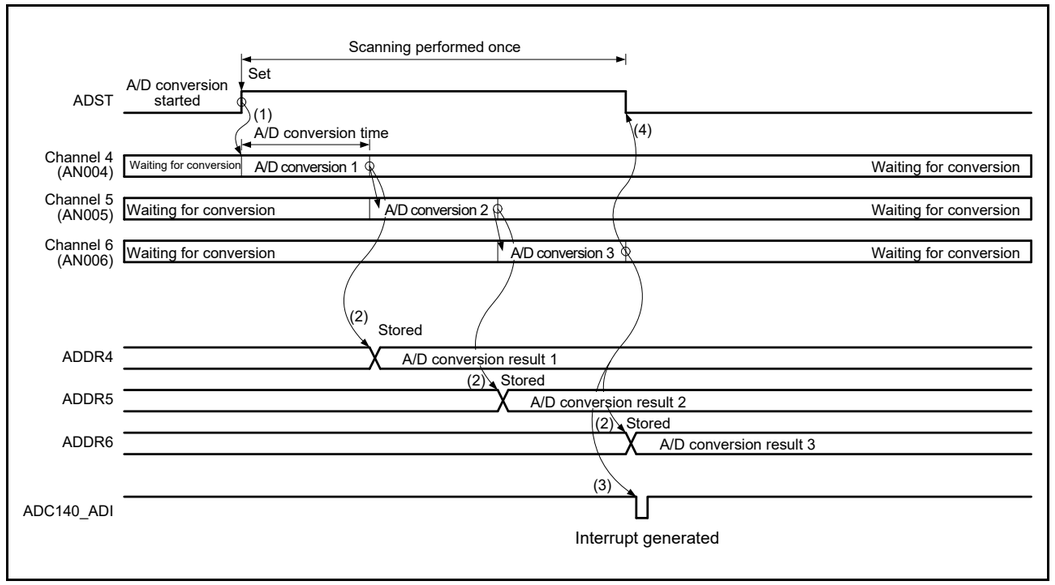


Figure 34.6 Example of basic operation in single scan mode when AN004 to AN006 are selected

34.3.2.2 Channel selection and self-diagnosis

When channels and self-diagnosis are selected, A/D conversion is first performed on the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to ADC14. A/D conversion is then performed once on the analog input of the selected channels as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated.
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC14 then enters a wait state.

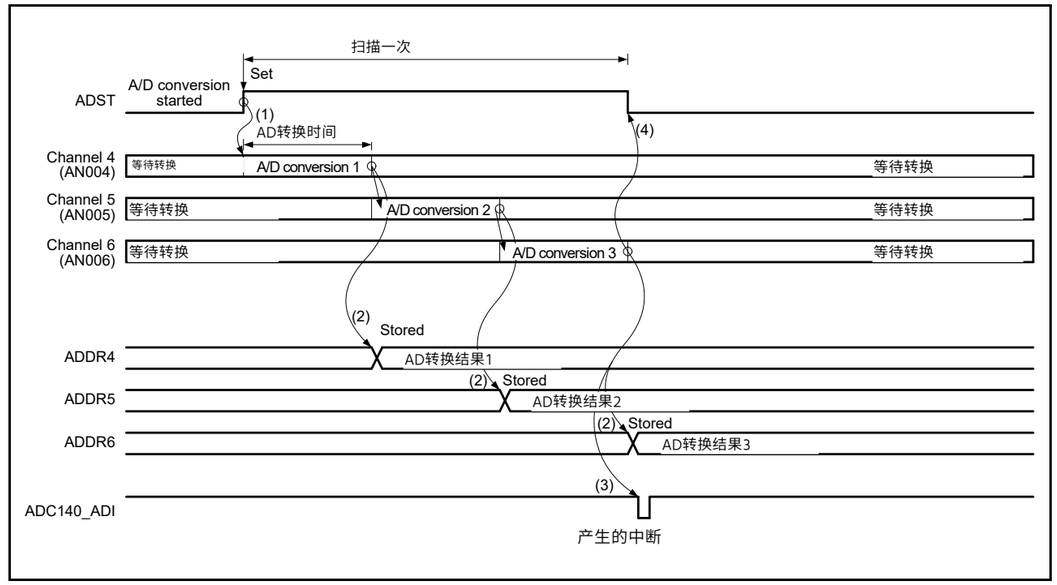


Figure 34.6 选择AN004至AN006时单次扫描模式的基本操作示例

34.3.2.2 频道选择和自诊断

Whenchannelsandself-diagnosisareselected ADconversionisfirstperformedonthereferencevoltageVREFH0(×0 ×12 or×1)suppliedtoADC14.然后在所选通道的模拟输入上执行一次D转换，如下所示：

1. 通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。
2. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中数据寄存器(ADRD)。然后在ADANSA0中选择的ANn通道上执行D转换，并ADANSA1寄存器，从编号n最小的通道开始。
3. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器(ADDRy)。
4. 当所有选定通道的AD转换完成时，会产生ADC140_ADI中断请求。
5. ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动设置为0。ADC14然后进入等待状态。

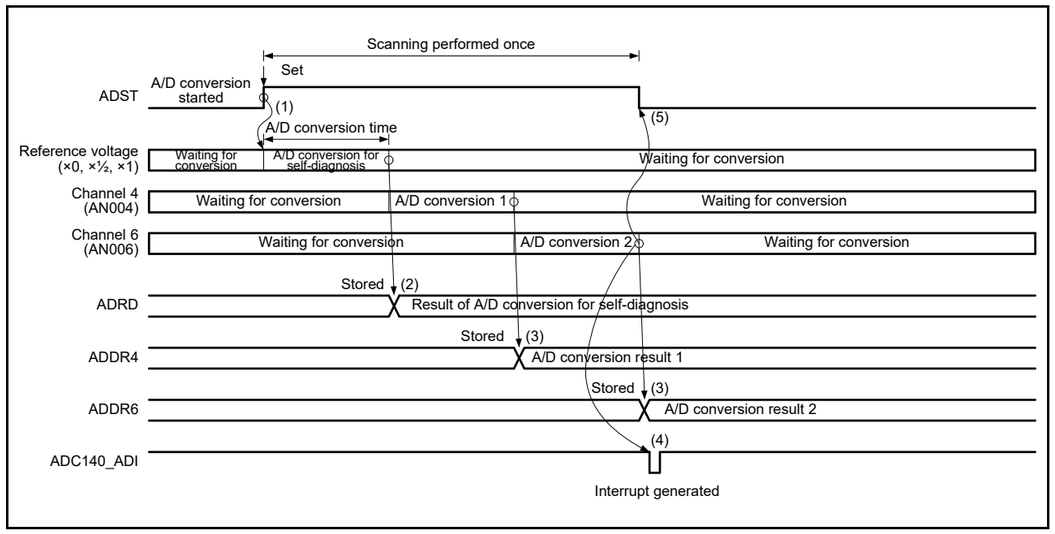


Figure 34.7 Example of basic operation in single scan mode when AN004 and AN006 selected with self-diagnosis

34.3.2.3 A/D conversion of temperature sensor output or internal reference voltage

A/D conversion is performed on the temperature sensor output or the internal reference voltage in single scan mode as described in this section.

When selecting A/D conversion of the temperature sensor output or the internal reference voltage, deselect all channels by setting the ADANSA0 and ADANSA01 registers to all 0's, and the ADCSR.DBLE bit to 0.

When selecting A/D conversion of temperature sensor output, set the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0 (deselected). When selecting A/D conversion of internal reference voltage, set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA) to 0 (deselected).

The operation is as follows:

1. Set the sampling time to 5 µs or longer. Take note of the A/D Sampling State Register T and A/D Sampling State Register O (ADSSTRT/ADSSTRO) settings, and ADCLK frequency.
2. After switching to A/D conversion of internal reference voltage or temperature sensor output, set the ADST bit to 1 to start conversion.
3. On completion of A/D conversion, the result is stored in the Temperature Sensor Data Register (ADTSDR) or the A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC140_ADI interrupt request is generated.
4. The ADST bit remains 1 during A/D conversion and is automatically set to 0 on completion of the A/D conversion. The ADC14 then enters a wait state.

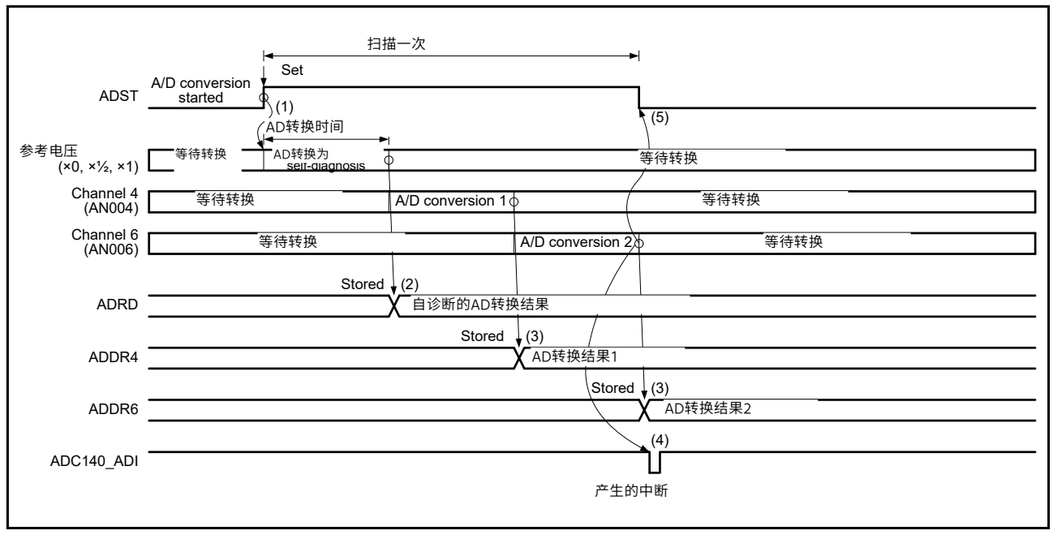


Figure 34.7 自诊断选择AN004和AN006时单次扫描模式的基本操作示例

34.3.2.3 温度传感器输出或内部参考电压的AD转换

如本节所述，在单次扫描模式下对温度传感器输出或内部参考电压执行D转换。

WhenselectingADconversionofthetemperaturesensoroutputortheinternalreferencevoltage deselectallchannelsbysettingtheADANSA0andADANSA01registerstoall0's andtheADCSR.DBLEbitto0.

选择温度传感器输出的AD转换时，将内部参考电压AD转换选择位(ADEXICR.OCSA)设置为0（取消选择）。选择内部参考电压的AD转换时，将温度传感器输出AD转换选择位(ADEXICR.TSSA)设置为0（取消选择）。

操作如下：

1. 将采样时间设置为5µs或更长。记下AD采样状态寄存器T和AD采样状态寄存器O(ADSSTRTADSSTRO)设置，以及ADCLK频率。
2. 切换到内部参考电压或温度传感器输出的AD转换后，将ADST位设置为1以开始转换。
3. 完成AD转换后，结果将存储在温度传感器数据寄存器(ADTSDR)或AD内部参考电压数据寄存器(AOCDR)，并产生ADC140_ADI中断请求。
4. ADST位在AD转换期间保持为1，并在AD转换完成时自动设置为0。ADC14然后进入等待状态。

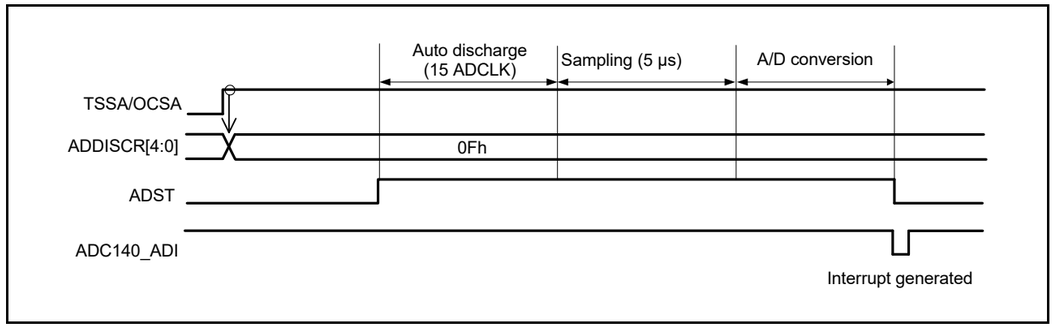


Figure 34.8 Example of basic operation in single scan mode when AN004 and temperature sensor output or internal reference voltage is selected

34.3.2.4 A/D conversion in double trigger mode

When double trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence as described in this section.

Deselect self-diagnosis, and set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA) and the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel number to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double trigger mode, select a synchronous trigger (ELC) with the ADSTRGR.TRSA[5:0] bits. Additionally, set the ADCSR.EXTRG bit to 0 and the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. The ADST bit is automatically set to 0 and the ADC14 enters a wait state. An ADC140_ADI interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the A/D conversion result is stored into the A/D Data Duplexing Register (ADDBLDR), which is only used in double trigger mode.
6. An ADC140_ADI interrupt request is generated.
7. The ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion completes. The ADC14 then enters a wait state.

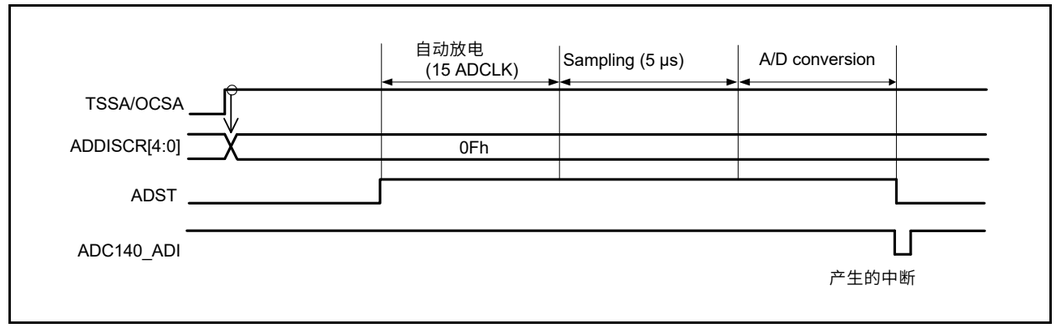


Figure 34.8 选择AN004和温度传感器输出或内部参考电压时单次扫描模式下的基本操作示例

34.3.2.4 双触发模式下的AD转换

在单次扫描模式下选择双触发模式时，由同步触发(ELC)启动的两轮单次扫描操作按本节所述顺序执行。

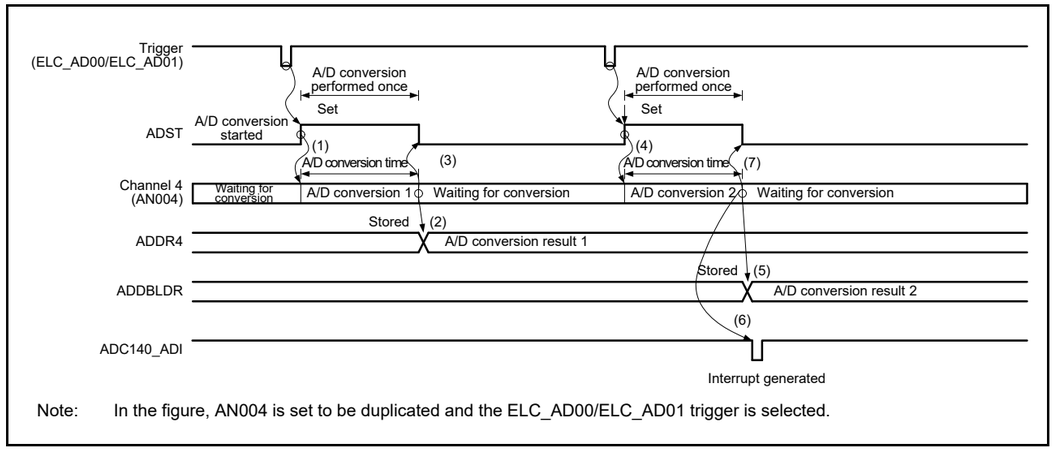
取消选择自诊断，并设置温度传感器输出AD转换选择位(ADEXICR.TSSA)和内部参考电压AD转换选择位(ADEXICR.OCSA)为0。

AD转换数据的复制通过在ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。当ADCSR.DBLE位设置为1时，使用ADANSA0和ADANSA1寄存器的通道选择无效。

在双触发模式下，使用ADSTRGR.TRSA[5:0]位选择同步触发(ELC)。此外，设置ADCSR.EXTRG位为0，ADCSR.TRGE位为1。不要使用软件触发。

操作如下：

1. 当同步触发输入(ELC)将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。
2. 当单个通道的AD转换完成时，AD转换结果存储在关联的ADData中Register (ADDRy).
3. ADST位自动设置为0，ADC14进入等待状态。不会产生ADC140_ADI中断请求。
4. 当第二个触发输入将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。
5. 当AD转换完成后，AD转换结果存入AD数据双工寄存器(ADDBLDR)，该寄存器仅用于双触发模式。
6. 产生一个ADC140_ADI中断请求。
7. ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动设置为0。ADC14然后进入等待状态。



Note: In the figure, AN004 is set to be duplicated and the ELC_AD00/ELC_AD01 trigger is selected.

Figure 34.9 Example of operation in single scan mode with double trigger mode selected when AN004 is duplicated

34.3.2.5 Extended operations when double trigger mode is selected

When double trigger mode is selected in single scan mode, and a synchronous trigger ELC_AD00/ELC_AD01 is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

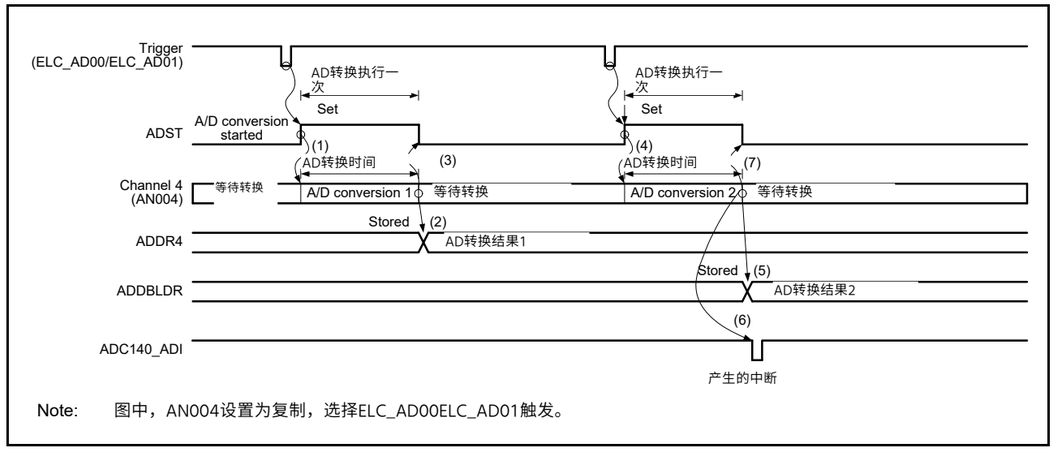
Deselect self-diagnosis, and set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA) and the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double trigger mode, select a synchronous trigger ELC_AD00/ELC_AD01 by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, set the ADCSR.EXTRG bit to 0, and set the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00/ ELC_AD01), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion of a single channel completes, the conversion result is stored in the associated A/D Data Register (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_AD00 or ELC_AD01 is input, respectively.
3. The ADCSR.ADST bit is automatically set to 0 and the ADC14 enters a wait state. An ADC140_ADI interrupt is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input (ELC_AD00/ ELC_AD01), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_AD00 or ELC_AD01 is input, respectively.
6. An ADC140_ADI interrupt request is generated.
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when the A/D conversion completes. The ADC14 then enters a wait state.



Note: 图中，AN004设置为复制，选择ELC_AD00ELC_AD01触发。

Figure 34.9 复制AN004时选择双触发模式的单扫描模式操作示例

34.3.2.5 选择双触发模式时的扩展操作

当在单扫描模式下选择双触发模式，并选择一个同步触发ELC_AD00ELC_AD01作为开始AD转换的触发，执行两轮单扫描操作。

取消选择自诊断，并设置温度传感器输出AD转换选择位(ADEXICR.TSSA)和内部参考电压AD转换选择位(ADEXICR.OCSA)为0。

AD转换数据的复制通过将要复制的通道号设置为ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。当ADCSR.DBLE位设置为1时，使用ADANSA0和ADANSA1寄存器的通道选择无效。

在扩展双触发模式下，选择同步触发ELC_AD00ELC_AD01通过设置ADSTRGR.TRSA[5:0]位为0Bh，将ADCSR.EXTRG位设置为0，并将ADCSR.TRGE位设置为1。不要使用软件触发。

操作如下：

1. 通过同步触发输入(ELC_AD00)将ADCSR.ADST位设置为1（AD转换开始）时ELC_AD01)，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。
2. 当单通道的AD转换完成时，当ELC_AD00或ELC_AD01的触发为分别输入。
3. ADCSR.ADST位自动设置为0，ADC14进入等待状态。不会产生ADC140_ADI中断。
4. 当第二个触发输入（ELC_AD00）将ADCSR.ADST位设置为1（AD转换开始）时ELC_AD01)，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。
5. 当AD转换完成时，结果存储在AD数据双工寄存器(ADDBLDR)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中。
   分别输入ELC_AD00或ELC_AD01。
6. 产生一个ADC140_ADI中断请求。
7. ADCSR.ADST位在AD转换期间保持为1（AD转换开始），并在AD转换完成时自动设置为0。ADC14然后进入等待状态。

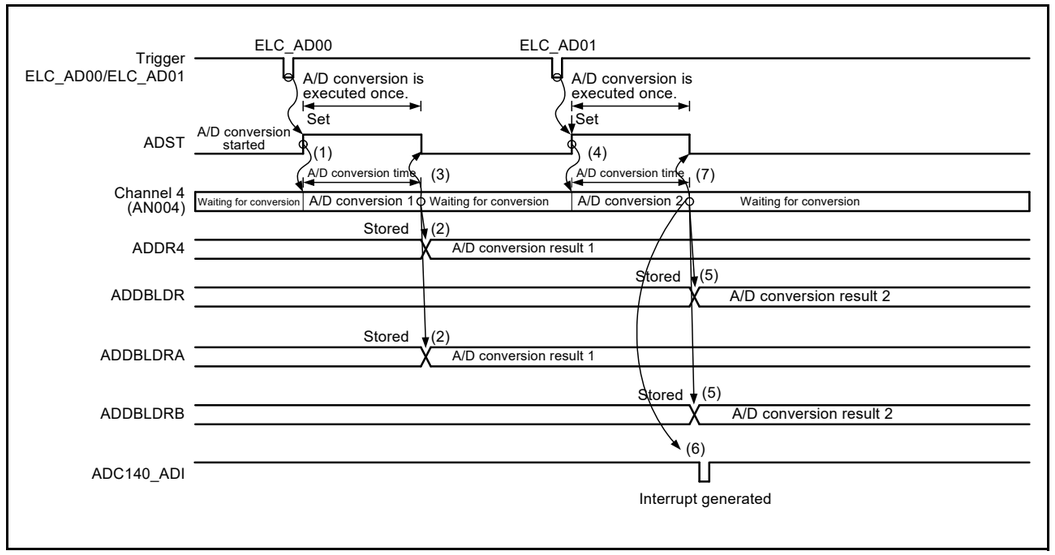


Figure 34.10 Example of extended operation in double trigger mode (1) with duplication selected for AN004, and ELC_AD00/ELC_AD01 selected

34.3.3 Continuous Scan Mode

34.3.3.1 Basic operation

In continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels as described in this section.

In this mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. When A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated without register setting. The ADC14 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADCSR.ADST bit is not automatically cleared and steps 2. and 3. are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC14 enters a wait state.
5. When the ADST bit is then set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.

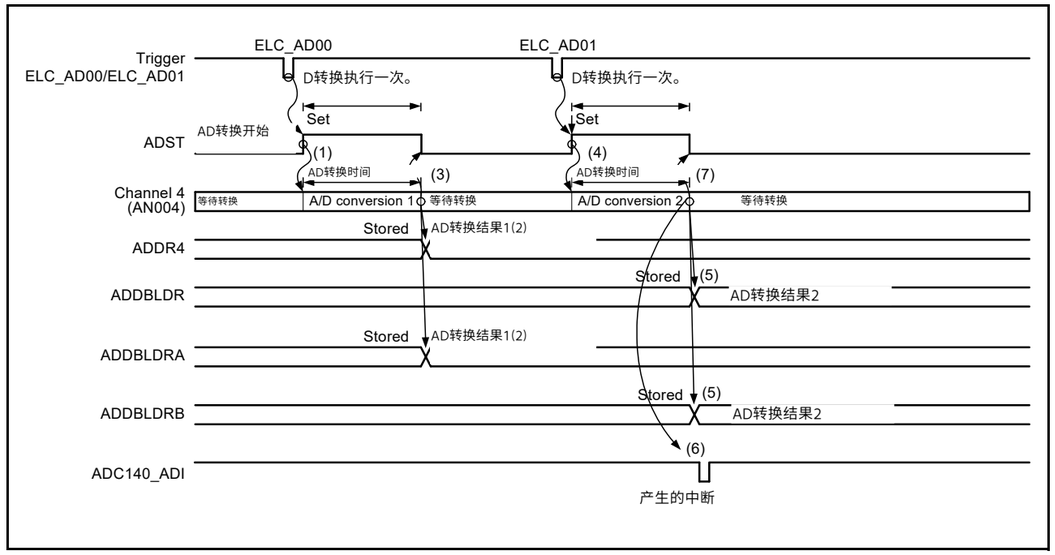


Figure 34.10 双触发模式下的扩展操作示例(1)为AN004选择了重复，并选择了ELC_AD00ELC_AD01

34.3.3 连续扫描模式

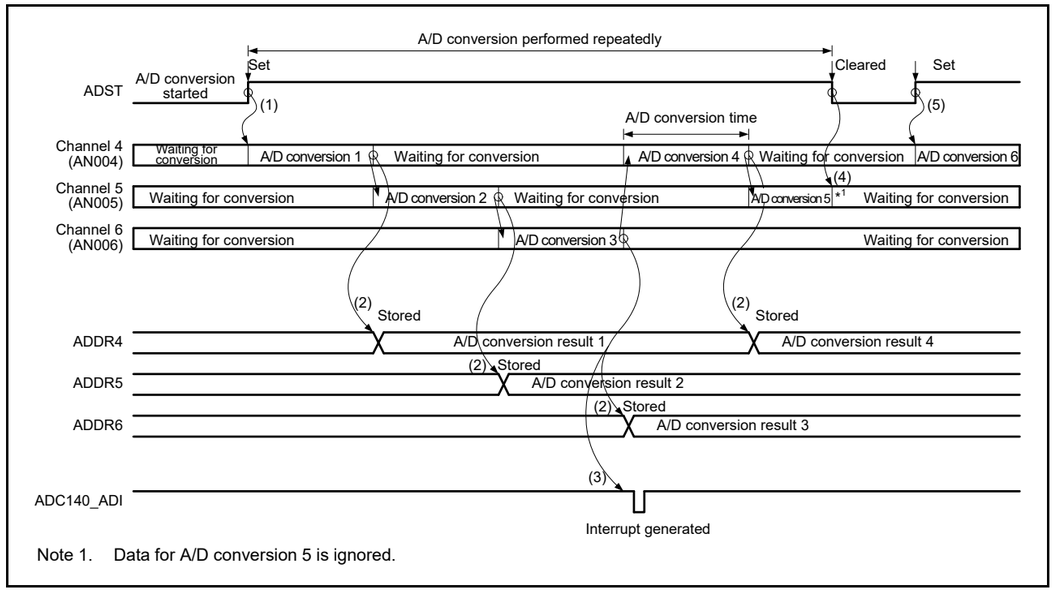
34.3.3.1 基本操作

在连续扫描模式下，如本节所述，对指定通道的模拟输入重复执行AD转换。

在此模式下，通过将ADEXICR.TSSA和ADEXICR.OCSA位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。

操作如下：

1. 当ADCSR.ADST位通过软件触发、同步触发输入(ELC)或异步触发输入设置为1（AD转换开始）时，在ADANSA0和ADANSA1寄存器中选择的ANn通道上执行AD转换，从具有最小编号n的通道开始。
2. 当单个通道的AD转换完成时，AD转换结果存储在关联的ADData中Register (ADDRy).
3. 当所有选定通道的AD转换完成时，会产生一个ADC140_ADI中断请求，无需寄存器设置。ADC14从编号n最小的通道开始依次启动ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换。
4. ADCSR.ADST位不会自动清零，只要该位保持为1（AD转换开始）。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止并且ADC14进入等待状态。
5. 然后当ADST位设置为1（AD转换开始）时，AD转换再次开始在ADANSA0和ADANSA1寄存器中选择的ANn通道，从具有最小编号n的通道开始。



Note 1. Data for A/D conversion 5 is ignored.

Figure 34.11 Example of basic operation in continuous scan mode with AN004 to AN006 selected

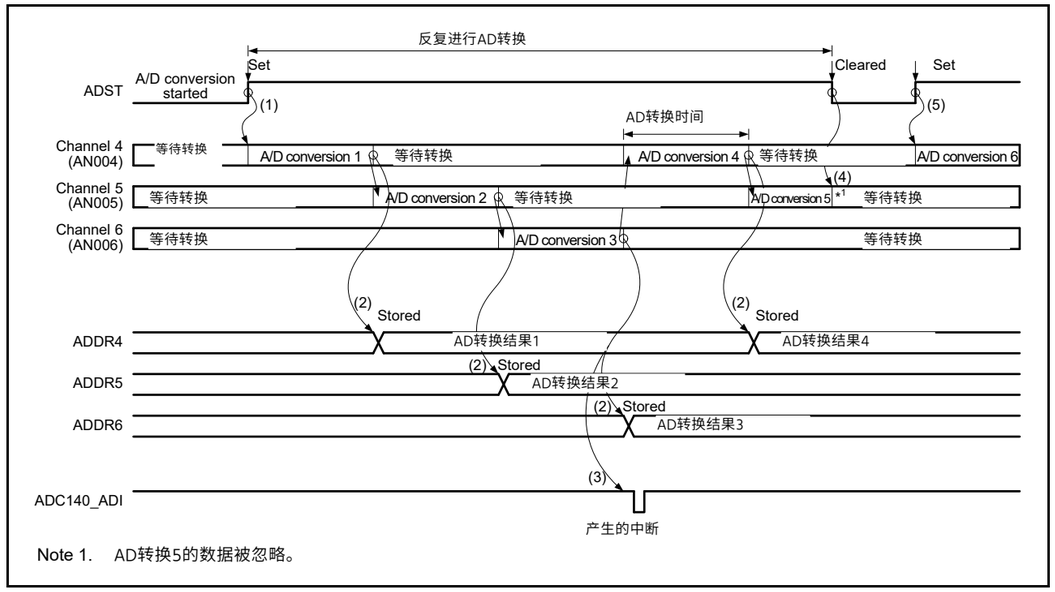
34.3.3.2 Channel selection and self-diagnosis

When channels are selected together with self-diagnosis, A/D conversion is first performed on the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the ADC14, then A/D conversion is performed on the analog input of the selected channels. This sequence is repeated as described in this section.

In continuous scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored into the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored into the associated A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC140_ADI interrupt request is generated (without register setting). At the same time, the ADC14 starts A/D conversion for self-diagnosis and then on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADST bit is not automatically cleared and steps 2. to 4. are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC14 enters a wait state.
6. When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis starts again.



Note 1. AD转换5的数据被忽略。

Figure 34.11 选择AN004至AN006的连续扫描模式下的基本操作示例

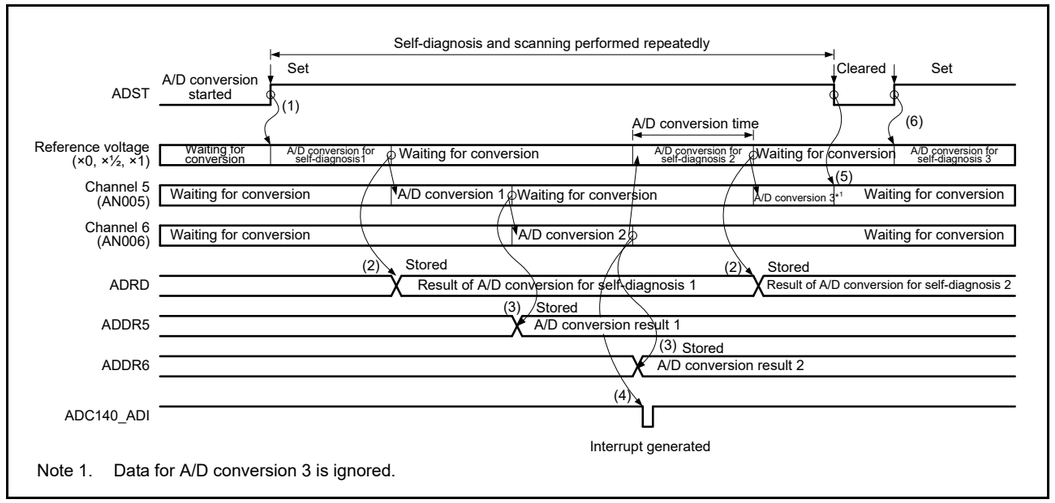
34.3.3.2 频道选择和自诊断

选择通道同时进行自诊断时，首先对参考电压进行A/D转换
VREFH0（×0、×12或×1）提供给ADC14，然后对所选通道的模拟输入执行AD转换。如本节所述，重复此序列
。

在连续扫描模式下，通过将ADEXICR.TSSA和ADEXICR.OCSA位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。

操作如下：

1. 通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。
2. 自诊断用AD转换完成后，将AD转换结果存入AD自诊断
数据寄存器(ADRD)。然后在ADANSA0中选择的ANn通道上执行D转换，并
ADANSA1寄存器，从编号n最小的通道开始。
3. 每次完成单个通道的AD转换，将AD转换结果存储到关联的A
D数据寄存器(ADDRy)。
4. 当所有选定通道的AD转换完成时，会产生一个ADC140_ADI中断请求（无需寄存器设置）。同时，ADC14启动AD转换进行自诊断，然后在ADANSA0和ADANSA1寄存器中选择的ANn通道上，从编号n最小的通道开始。
5. ADST位不会自动清零，只要该位保持1，就会重复步骤2.到4.。当
ADST位设置为0（AD转换停止），AD转换停止，ADC14进入等待状态。
6. 当ADST位稍后设置为1（AD转换开始）时，用于自诊断的AD转换再次开始。



Note 1. Data for A/D conversion 3 is ignored.

Figure 34.12 Example of basic operation in continuous scan mode when AN005 and AN006 are selected with self-diagnosis

34.3.4 Group Scan Mode

34.3.4.1 Basic operation

In group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in group A and group B after scanning is started by a synchronous trigger (ELC) as described in this section. The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers for group A and group B can be selected with the ADSTRGR.TRSA[5:0] bits for group A and with the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

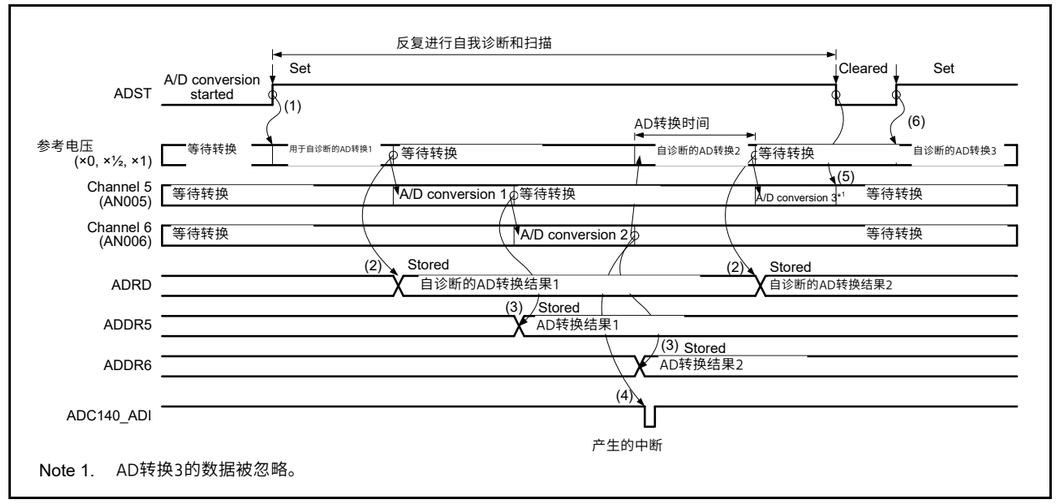
The group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers, while the group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A and group B cannot use the same channels.

In group scan mode, set the Temperature Sensor Output A/D Conversion Select bit (ADEXICR.TSSA) and the Internal Reference Voltage A/D Conversion Select bit (ADEXICR.OCSA) to 0. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.

The following sequence describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger from the ELC is used to start conversion of group A and the ELC_AD01 trigger from the ELC is used to start conversion of group B. Also, the ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group A is started by ELC_AD00.
2. When group A scanning completes, an ADC140_ADI interrupt is generated without register setting.
3. Scanning of group B is started by ELC_AD01.
4. When group B scanning completes, an ADC140_GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (ADC140_GBADI interrupt is enabled).



Note 1. AD转换3的数据被忽略。

Figure 34.12 使用自诊断选择AN005和AN006时连续扫描模式下的基本操作示例

34.3.4 组扫描模式

34.3.4.1 基本操作

在组扫描模式下，如本节所述，在通过同步触发器(ELC)启动扫描后，对A组和B组中所有指定通道的模拟输入执行一次AD转换。每组的扫描操作类似于单次扫描模式下的扫描操作。

A组和B组的同步触发可以通过A组的ADSTRGR.TRSA[5:0]位和B组的ADSTRGR.TRSB[5:0]位选择。A组和B组使用不同的触发B防止两组同时进行AD转换。不要使用软件触发。

使用ADANSA0和ADANSA1寄存器选择要进行AD转换的A组通道，而组
使用ADANSB0和ADANSB1寄存器选择要进行AD转换的B通道。A组和B组不能使用相同的通道。

在组扫描模式下，设置温度传感器输出AD转换选择位(ADEXICR.TSSA)和内部
参考电压AD转换选择位(ADEXICR.OCSA)为0。当在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

以下序列描述了使用来自ELC的同步触发在组扫描模式下的操作。在此示例中，来自ELC的ELC_AD00触发器用于启动A组转换，来自ELC的ELC_AD01触发器用于启动B组转换。此外，为关联ELC中的GPT事件选择ELC_AD00和ELC_AD01.ELSRn寄存器。

操作如下：

1. A组的扫描由ELC_AD00启动。
2. 当A组扫描完成时，会产生一个ADC140_ADI中断，无需设置寄存器。
3. B组的扫描由ELC_AD01启动。
4. 当B组扫描完成时，如果ADCSR.GBADIE位为1（使能ADC140_GBADI中断），则会产生ADC140_GBADI中断。

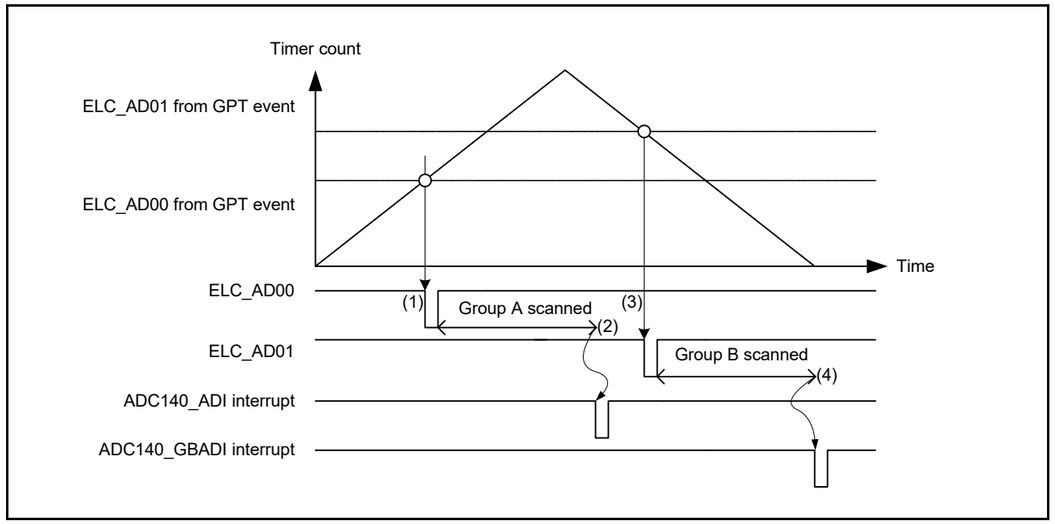


Figure 34.13 Example of basic operation in group scan mode with synchronous triggers from ELC

34.3.4.2 A/D conversion in double trigger mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence for group A. For group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, select synchronous triggers for group A and B with the ADSTRGR.TRSA[5:0] bits for group A and the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger (ADTRG0).

When ELC_AD00/ELC_AD01 is selected as the group A synchronous trigger by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, operation proceeds in extended double trigger mode.

The group A channel to be A/D-converted is selected with the ADCSR.DBLANS[4:0] bits and the group B channel to be A/D converted is selected in the ADANSB0 and ADANSB1 registers. Group A and group B cannot use the same channels.

In group scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

When double trigger mode is selected in group scan mode, self-diagnosis cannot be selected.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE to 1.

The following sequence describes operation in group scan mode with double trigger mode using synchronous triggers from the ELC. In this example, the ELC_AD00 trigger is used to start conversion of group A and the ELC_AD01 trigger is used to start conversion of group B. In addition, ELC_AD00 and ELC_AD01 are selected for the GPT event by the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group B is started by the ELC_AD00 trigger from the ELC.
2. When group B scanning completes, an ADC140_GBADI interrupt is generated if the GBADIE bit in the ADCSR register is 1 (group B scan end interrupt is enabled).
3. The first scan of group A is started by the first ELC_AD01 trigger.
4. When the first scan of group A completes, the conversion result is stored in the associated A/D Data Register (ADDRy). An ADC140_ADI interrupt request is not generated.

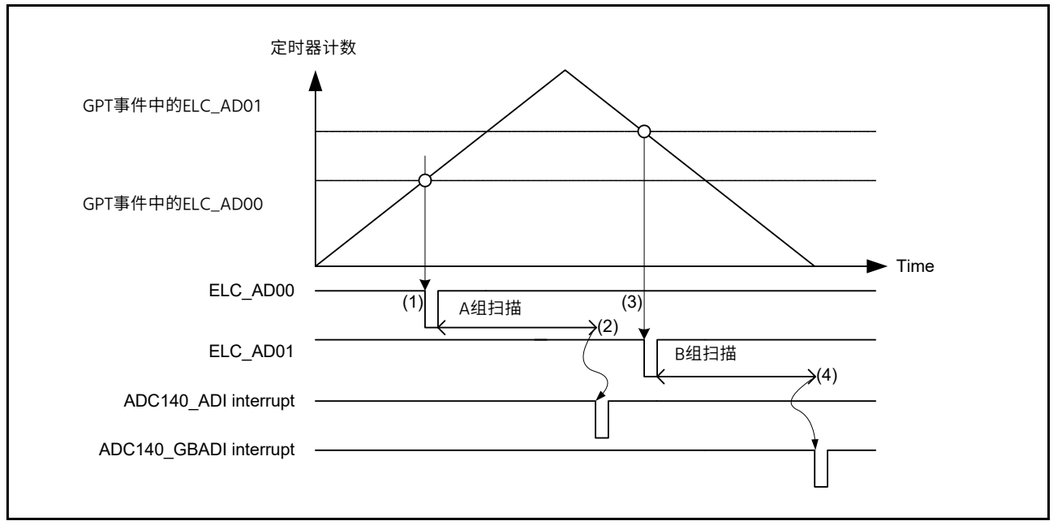


Figure 34.13 使用ELC同步触发的组扫描模式下的基本操作示例

34.3.4.2 双触发模式下的AD转换

在组扫描模式中选择双触发模式时，A组依次执行由同步触发（ELC）启动的两轮单扫描操作。对于B组，执行由同步触发（ELC）启动的单扫描操作一次。

在组扫描模式下，使用A组的ADSTRGR.TRSA[5:0]位和B组的ADSTRGR.TRSB[5:0]位为A组和B组选择同步触发。为A组和组使用不同的触发B防止两组同时进行AD转换。不要使用软件触发或异步触发(ADTRG0)。

当通过将ADSTRGR.TRSA[5:0]位设置为0Bh选择ELC_AD00ELC_AD01作为A组同步触发时，操作在扩展双触发模式下进行。

使用ADCSR.DBLANS[4:0]位选择要进行AD转换的A组通道，而要进行AD转换的B组通道在ADANSB0和ADANSB1寄存器中选择D转换。A组和B组不能使用相同的通道。

在组扫描模式下，通过将ADEXICR.TSSA和ADEXICR.OCSA位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。

在组扫描模式下选择双触发模式时，不能选择自诊断。

AD转换数据的复制通过将要复制的通道号设置为ADCSR.DBLANS[4:0]位并将ADCSR.DBLE设置为1。

以下序列描述了使用来自ELC的同步触发在双触发模式下的组扫描模式下的操作。在本例中，ELC_AD00触发器用于启动A组转换，ELC_AD01触发器用于启动B组转换。此外，ELC_AD00和ELC_AD01由关联的ELC.ELSRn寄存器选择用于GPT事件。

操作如下：

1. 组B的扫描由来自ELC的ELC_AD00触发器启动。
2. 当B组扫描完成时，如果ADCSR寄存器中的GBADIE位为1（使能B组扫描结束中断），则产生ADC140_GBADI中断。
3. A组的第一次扫描由第一个ELC_AD01触发器启动。
4. 当A组的第一次扫描完成时，转换结果存储在相关的AD数据寄存器(ADDRy)中。不会产生ADC140_ADI中断请求。

5. The second scan of group A is started by the second ELC_AD01 trigger.
6. When the second scan of group A completes, the conversion result is stored in the ADDBLDR register. An ADC140_ADI interrupt is generated without register setting.

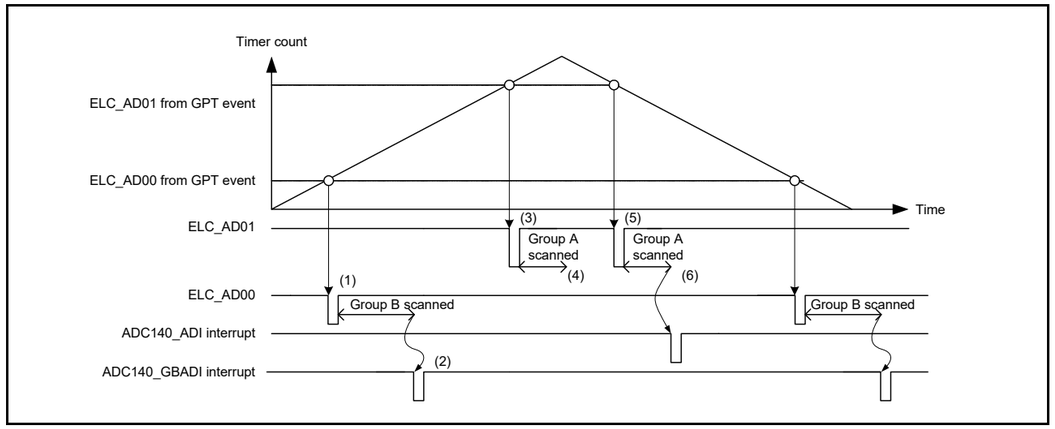


Figure 34.14 Example of operation in group scan mode with double trigger mode using synchronous triggers from the ELC

34.3.4.3 Operation with group A priority control

Setting the ADGSPCR.PGS bit to 1 in group scan mode makes the operation proceed with group A priority control. When setting the PGS bit in the ADGSPCR register to 1, follow the procedure described in Figure 34.15. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

In basic group scan mode, while A/D conversion is in progress for group A or group B, input of the trigger for A/D conversion for the other group is ignored. With group A priority control, if a group A trigger is input during A/D conversion for group B, A/D conversion for group B is discontinued and A/D conversion for group A proceeds. If the ADGSPCR.GBRSCN bit is 0, the ADC14 enters wait state on completion of the A/D conversion for group A. If ADGSPCR.GBRSCN bit is 1, the ADC14 automatically restarts group B scanning from the head of the group after completion of the A/D conversion for group A. Table 34.9 summarizes operations in response to the input of a trigger during A/D conversion with the ADGSPCR.GBRSCN bit.

Scan operations in group A or group B are the same in single scan mode. Additionally, single scanning continues to proceed when the ADGSPCR.GBRP bit is set to 1 during scanning operations for group B.

For the trigger settings in group scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits and select a synchronous trigger for group B, different from that of group A, using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1.

Additionally, as targets for A/D conversion, select channels for group A using the ADANSA0 and ADANSA1 registers, and for group B, select channels different from those for group A, using the ADANSB0 and ADANSB1 registers.

5. A组的第二次扫描由第二个ELC_AD01触发器启动。
6. 当A组的第二次扫描完成时，转换结果存储在ADDBLDR寄存器中。一个ADC140_ADI中断在没有寄存器设置的情况下产生。

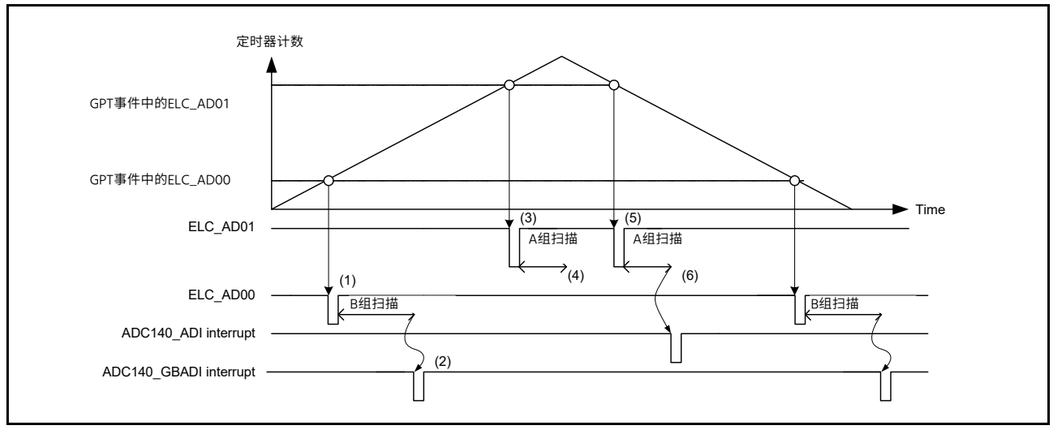


Figure 34.14 使用ELC同步触发的双触发模式的组扫描模式操作示例

34.3.4.3 A组优先控制操作

在组扫描模式中将ADGSPCR.PGS位设置为1会使操作继续进行A组优先级控制。
将ADGSPCR寄存器中的PGS位设置为1时，请遵循图34.15中描述的过程。如果不遵循该程序，则无法保证AD转换操作和存储数据。

在基本组扫描模式下，当A组或B组正在进行AD转换时，忽略其他组的AD转换触发输入。使用A组优先控制时，如果在B组AD转换期间输入A组触发，则B组AD转换中断，A组AD转换继续。如果ADGSPCR.GBRSCN位为0，则ADC14在A组的AD转换完成时进入等待状态。如果

ADGSPCR.GBRSCN位为1，ADC14在A组的AD转换完成后自动从组头重新开始B组扫描。表34.9总结了在ADGSPCR.GBRSCN的AD转换过程中响应触发输入的操作少量。

A组或B组的扫描操作在单次扫描模式下是相同的。此外，在B组扫描操作期间，当ADGSPCR.GBRP位设置为1时，单次扫描将继续进行。

对于组扫描模式下的触发设置，使用ADSTRGR.TRSA[5:0]位为A组选择一个同步触发，并使用ADSTRGR.TRSB[5为B组选择一个不同于A组的同步触发:0]位。将ADGSPCR.GBRP位设置为1时，将ADSTRGR.TRSB[5:0]位设置为3Fh。

此外，作为AD转换的目标，使用ADANSA0和ADANSA1寄存器为A组选择通道，对于B组，使用ADANSB0和ADANSB1寄存器选择与A组不同的通道。

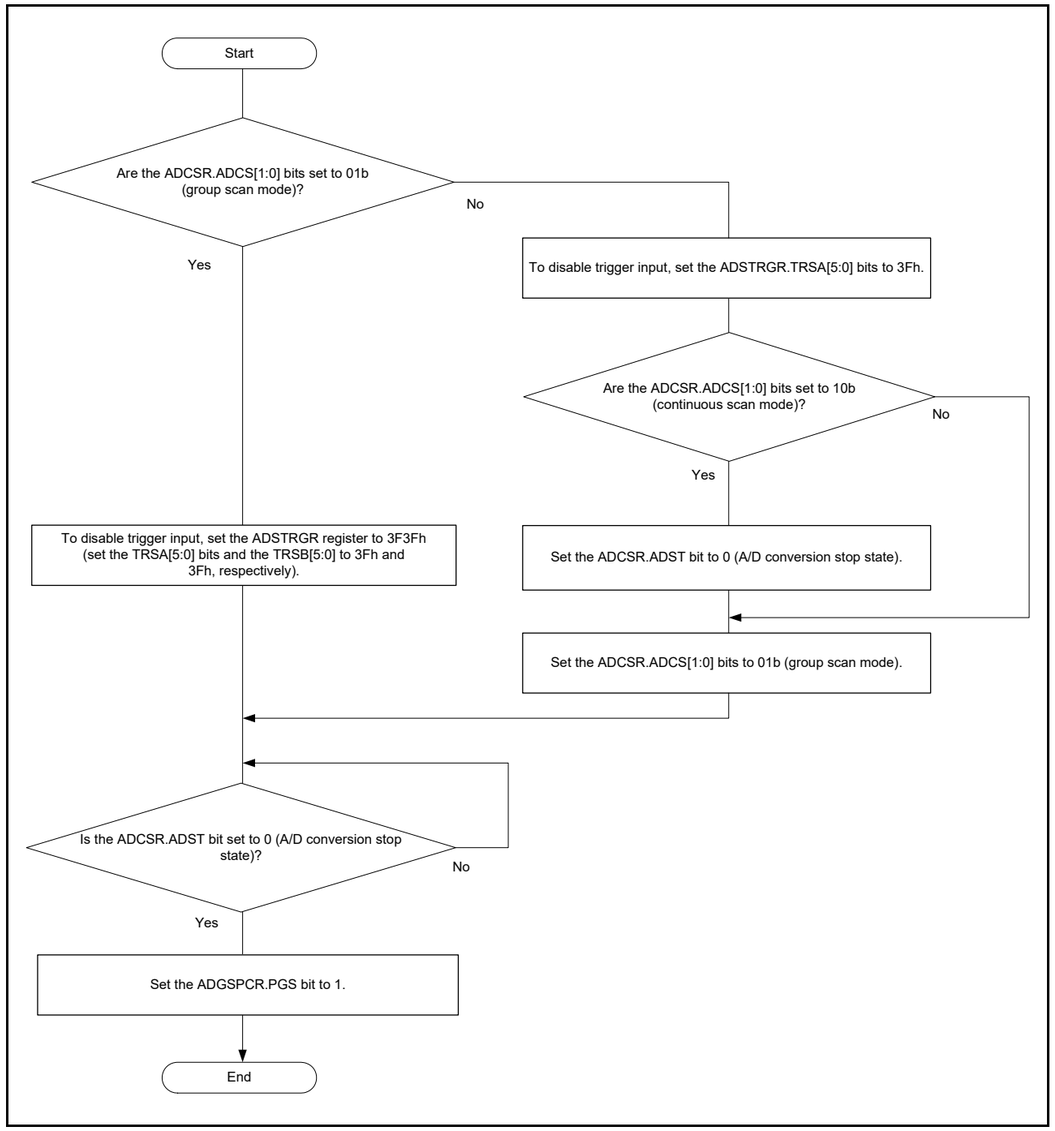


Figure 34.15 Flow for ADGSPCR.PGS bit setting

Table 34.9 Control of A/D conversion operations based on the ADGSPCR.GBRSCN bit settings (1 of 2)

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ignored	Trigger input is ignored
	Input of trigger for group B	Trigger input is ignored	A/D conversion is performed on group B after A/D conversion on group A completes

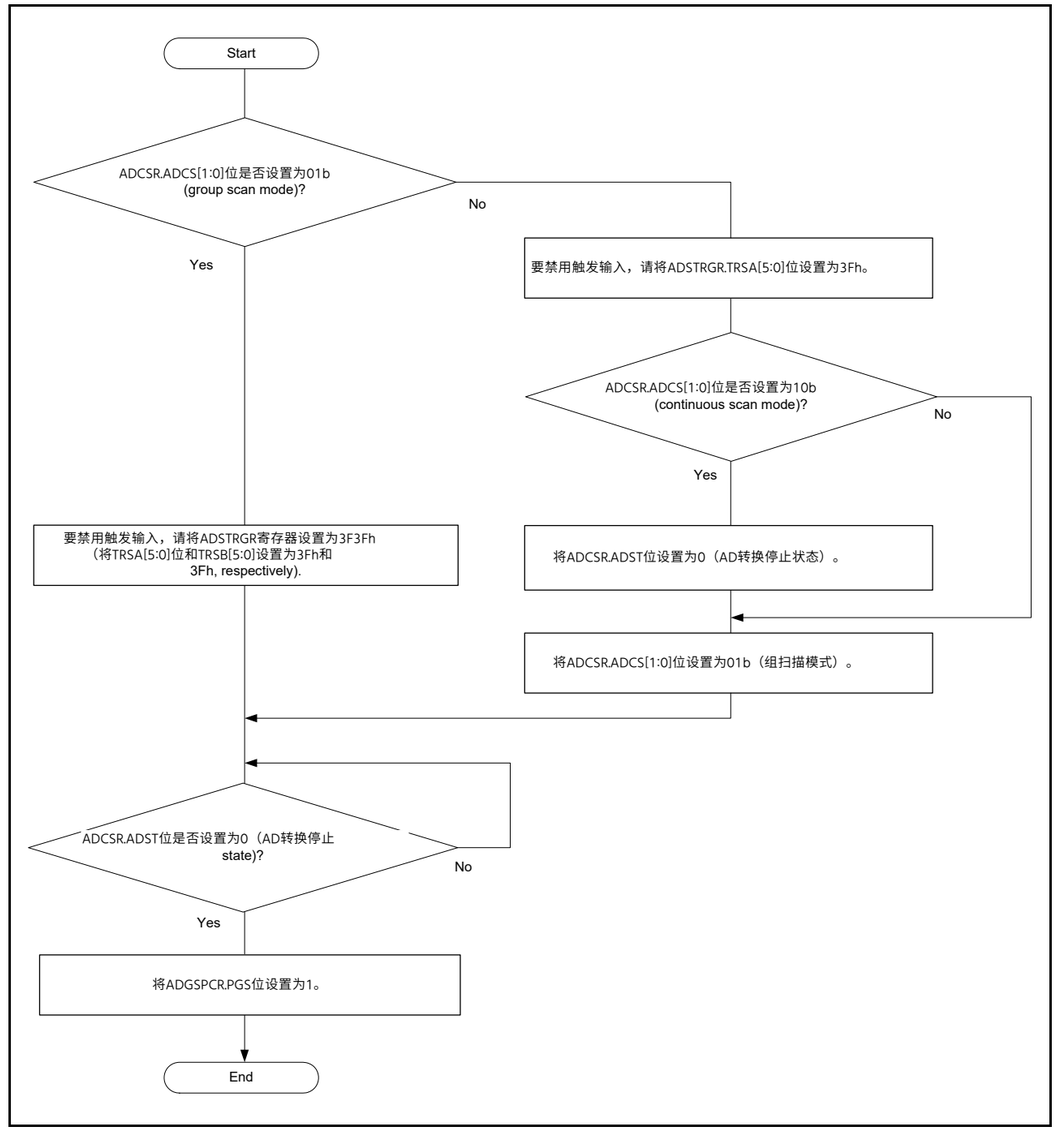


Figure 34.15 ADGSPCR.PGS位设置流程

Table 34.9 基于ADGSPCR.GBRSCN位设置（1of2）控制AD转换操作

AD转换操作	触发输入	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
正在进行A组的AD转换时	A组触发器输入	触发输入被忽略	触发输入被忽略
	B组触发器输入	触发输入被忽略	在A组的AD转换完成后，对B组执行AD转换

Table 34.9 Control of A/D conversion operations based on the ADGSPCR.GBRSCN bit settings (2 of 2)

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group B is in progress	Input of trigger for group A	Group B conversion stops and group A conversion starts	• Group B conversion stops and group A conversion starts • Group B conversion starts after group A conversion completes.
	Input of trigger for group B	Trigger input is ignored	Trigger input is ignored

The following sequence describes operations in group scan mode with group A priority control (for example, ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 4 is selected for group A and channel 5, 6, and 9 are selected for group B.

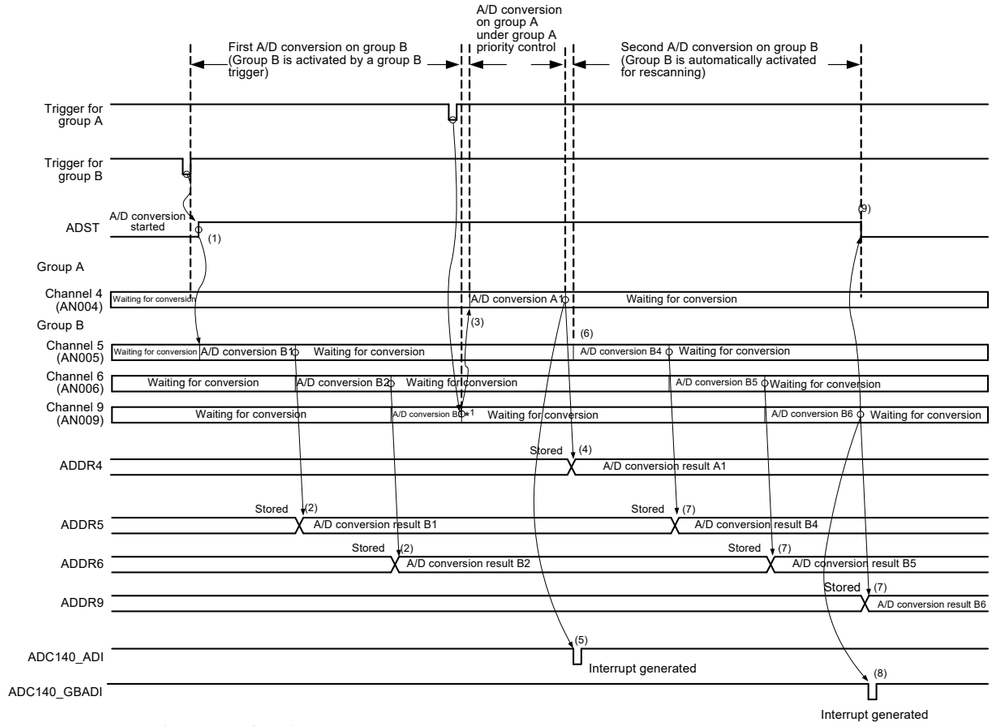
1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion for each group B channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n. If A/D conversion is not complete when the conversion of group B is interrupted, the A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
5. An ADC140_ADI interrupt request is generated without register setting.
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n with the ADCSR.ADST bit remains 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
8. On completion of A/D conversion of all group B channels, an ADC140_GBADI interrupt request is generated if the ADCSR.GBADIE bit is 1 (ADC140_GBADI interrupt on group B scan end is enabled).
9. The ADCSR.ADST bit is automatically cleared and the ADC14 enters the wait state when A/D conversion is complete.

Table 34.9 基于ADGSPCR.GBRSCN位设置的AD转换操作控制(2of2)

AD转换操作	触发输入	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
正在进行B组的AD转换时	A组触发器输入	B组转换停止，A组转换开始	B组转换停止，A组转换开始 B组转换在A组转换完成后开始。
	B组触发器输入	触发输入被忽略	触发输入被忽略

以下序列描述了具有A组优先级控制的组扫描模式下的操作（例如，ADGSPCR.GBRSCN=1和ADGSPCR.GBRP=0)当为A组选择通道4并且为B组选择通道5、6和9时。

1. 当B组的触发输入将ADCSR.ADST位设置为1（AD转换开始）时，ADANSB0和ADANSB1寄存器中选择的ANn通道的转换从编号n最小的通道开始按顺序开始。
2. 每个B组通道的AD转换完成后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在B组的AD转换正在进行时输入A组触发，并且B组的AD转换在ADCSR.ADST位保持为1的情况下中断，则在ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换按顺序开始从具有最小编号n的通道。如果B组转换中断时AD转换未完成，则AD转换结果不会存储在AD数据寄存器(ADDRy)中。
4. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器(ADDRy)中。
5. 无需寄存器设置即可生成ADC140_ADI中断请求。
6. 在ADANSB0和ADANSB1寄存器中选择的B组ANn通道的AD转换从具有最小编号n的通道开始按顺序重新启动，ADCSR.ADST位保持为1。
7. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
8. 完成所有B组通道的AD转换后，如果ADCSR.GBADIE位为1（启用B组扫描结束时的ADC140_GBADI中断）。
9. ADCSR.ADST位自动清零，ADC14在AD转换完成后进入等待状态。

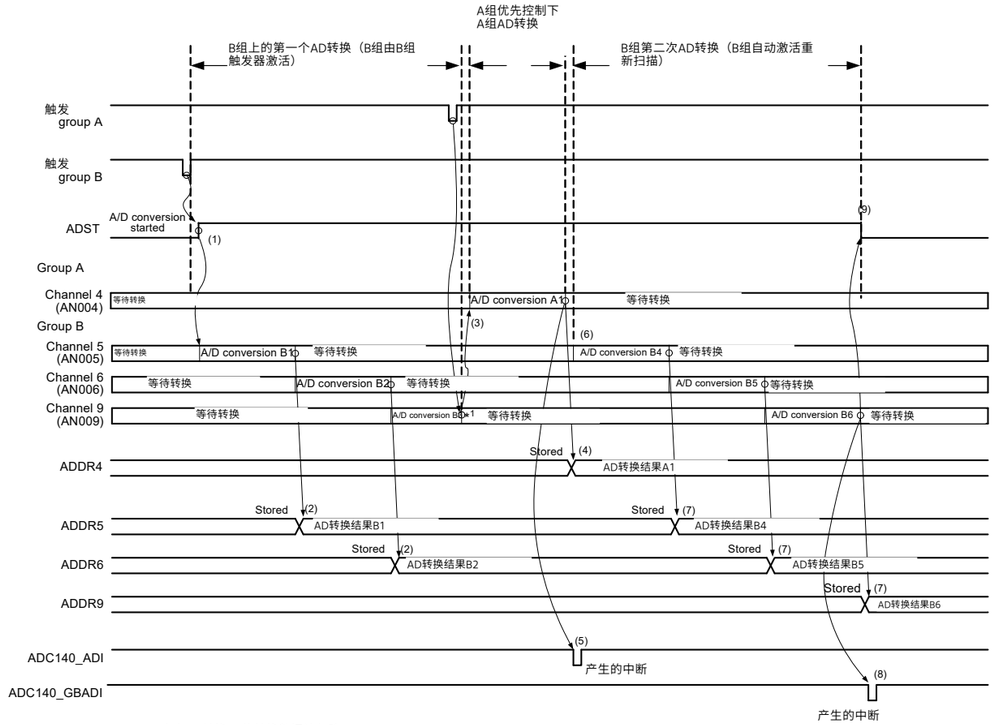


Note 1. Converted data from A/D conversion B3 is ignored.

Figure 34.16 Example operation with group A priority control (1), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example operation when a group A trigger is input again during rescanning operation on group B. In this example, channel 4 is selected for group A and channels 5, 6, and 9 are selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

1. When a group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register (ADDRy).
3. When a group A trigger is input during A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. If A/D conversion is not complete when the AD conversion of group B is interrupted, A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
5. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
6. An ADC140_ADI interrupt request is generated without register setting.
7. If the ADGSPCR.GBRSCN bit is 1, when the A/D conversion of group A is complete, the ADCSR.ADST bit remains 1 and group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
8. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y



Note 1. 来自AD转换B3的转换数据被忽略。

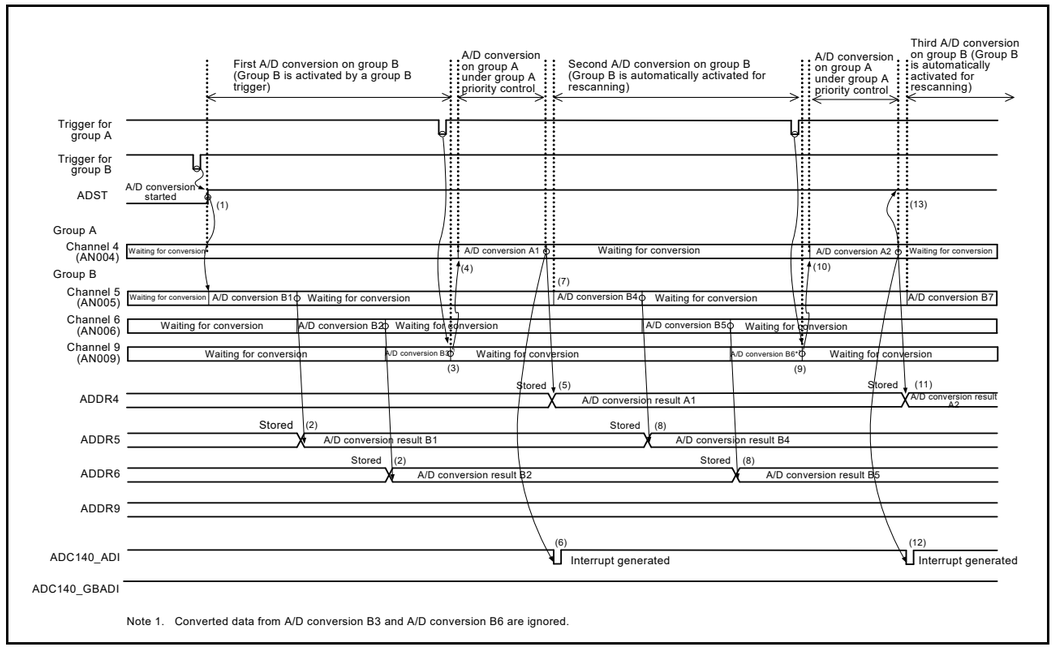
Figure 34.16 使用A组优先级控制(1)的示例操作，当ADGSPCR.GBRSCN=1并且ADGSPCR.GBRP = 0

以下序列是在对B组进行重新扫描操作期间再次输入A组触发时的示例操作。在此示例中，当对组进行操作时，为A组选择通道4，为组B选择通道5、6和9A被赋予优先级(ADGSPCR.GBRSCN=1 ADGSPCR.GBRP=0)。

1. 当B组触发输入将ADCSR.ADST位设置为1（AD转换开始）时，ADANSB0和ADANSB1寄存器中选择的B组ANn通道的转换从编号最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器(ADDRy)中。
3. 当B组的AD转换正在进行期间输入A组触发，并且B组的AD转换中断且ADCSR.ADST位保持1。如果B组的AD转换中断时AD转换未完成，AD转换结果不存储在AD数据寄存器(ADDRy)中。
4. 在ADANSA0和ADANSA1寄存器中选择的ANn组A通道的D转换从编号n最小的通道开始。
5. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
6. 无需寄存器设置即可生成ADC140_ADI中断请求。
7. 如果ADGSPCR.GBRSCN位为1，则当A组的AD转换完成时，ADCSR.ADST位保持为1，并重新扫描B组。ADANSB0和ADANSB1寄存器中选择的ANnB组通道的AD转换从编号n最小的通道重新开始。
8. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器中

(ADDRy).

9. If a group A trigger is input during A/D conversion on group B for rescanning, the ADCSR.ADST bit remains 1 and the ongoing A/D conversion on group B is discontinued.
10. A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
11. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
12. An ADC140_ADI interrupt request is generated without register setting.
13. If the ADGSPCR.GBRSCN bit is 1, when A/D conversion of group A is complete, the ADCSR.ADST bit remains 1 and group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
14. If a group A trigger is input during A/D conversion on group B for rescanning, steps 9. to 13. are repeated. If a group A trigger is not input, the ADCSR.ADST bit is cleared automatically on completion of A/D conversion on group B and the ADC14 enters a wait state.



Note 1. Converted data from A/D conversion B3 and A/D conversion B6 are ignored.

Figure 34.17 Example operation with group A priority control (2), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example of a rescanning operation in which a group B trigger is input during A/D conversion on group A. In this example, channels 5, 6, and 9 are selected for group A and channel 4 is selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

1. When input of a group A trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group B trigger is input during A/D conversion on group A, group B conversion can be performed after the group A conversion completes. However, if group A triggers are input continuously, the scan operation on group B

(ADDRy).

9. 如果在B组的AD转换期间输入A组触发以进行重新扫描，则ADCSR.ADST位保持为1，并且停止B组正在进行的AD转换。

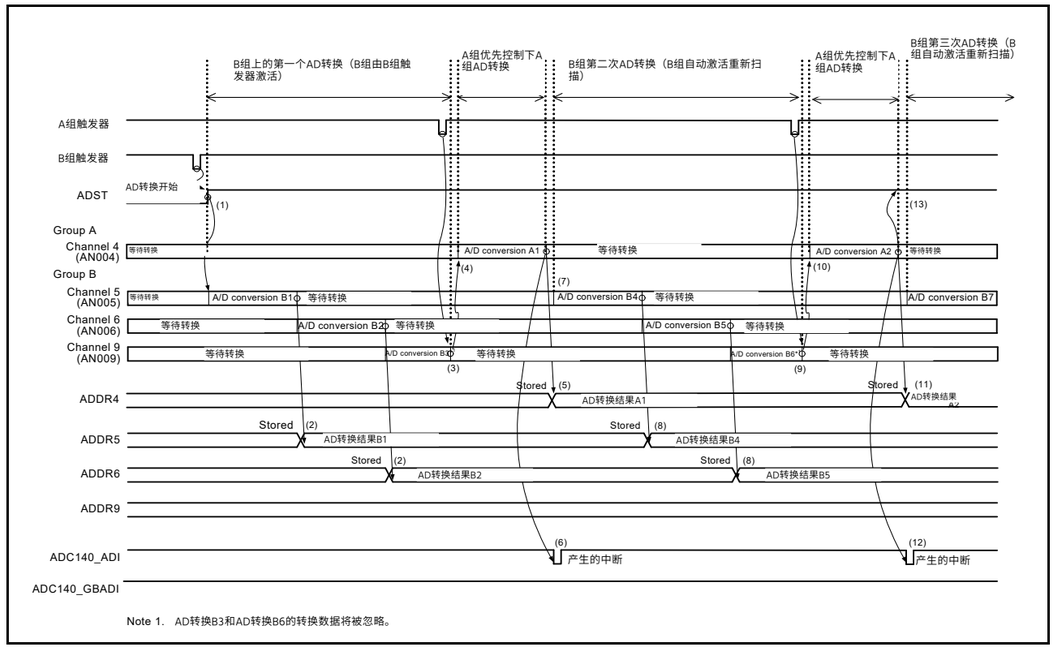
10.在ADANSA0和ADANSA1寄存器中选择的ANn组A通道的AD转换从编号n最小的通道开始。

11.在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。

12.ADC140_ADI中断请求在没有寄存器设置的情况下产生。

13.如果ADGSPCR.GBRSCN位为1，当A组的AD转换完成后，ADCSR.ADST位保持为1，重新扫描B组。ADANSB0和ADANSB1寄存器中选择的ANnB组通道的AD转换从编号n最小的通道重新开始。

14.如果在B组的AD转换期间输入A组触发以重新扫描，则重复步骤9.至13.。如果未输入A组触发，ADCSR.ADST位在B组AD转换完成后自动清零，ADC14进入等待状态。



Note 1. AD转换B3和AD转换B6的转换数据将被忽略。

Figure 34.17 使用A组优先级控制(2)的示例操作，当ADGSPCR.GBRSCN=1并且ADGSPCR.GBRP = 0

以下序列是重新扫描操作的示例，其中在A组AD转换期间输入B组触发。在此示例中，为A组选择通道5、6和9，为B组选择通道4。对A组的操作给予优先级（ADGSPCR.GBRSCN=1，ADGSPCR.GBRP=0）。

1. 当输入A组触发器将ADCSR.ADST位设置为1（AD转换开始）时，ADANSA0和ADANSA1寄存器中选择的ANn通道的转换从编号n最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在A组AD转换期间输入B组触发，则可以在A组转换完成后执行B组转换。但是，如果连续输入A组触发器，则B组的扫描操作

is canceled by group A and is not performed.

4. On completion of group A conversion, an ADC140_ADI interrupt request is generated without the register setting.
5. On completion of group A conversion, the ADCSR.ADST bit remains 1 and group B is rescanned. Then, A/D conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
6. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
7. On completion of the rescanning operation on group B, an ADC140_GBADI interrupt request is generated if the ADCSR.GBADIE bit is 1 (ADC140_GBADI scan end interrupt is enabled).
8. The ADCSR.ADST bit is automatically cleared and the ADC14 enters the wait state when A/D conversion is complete.

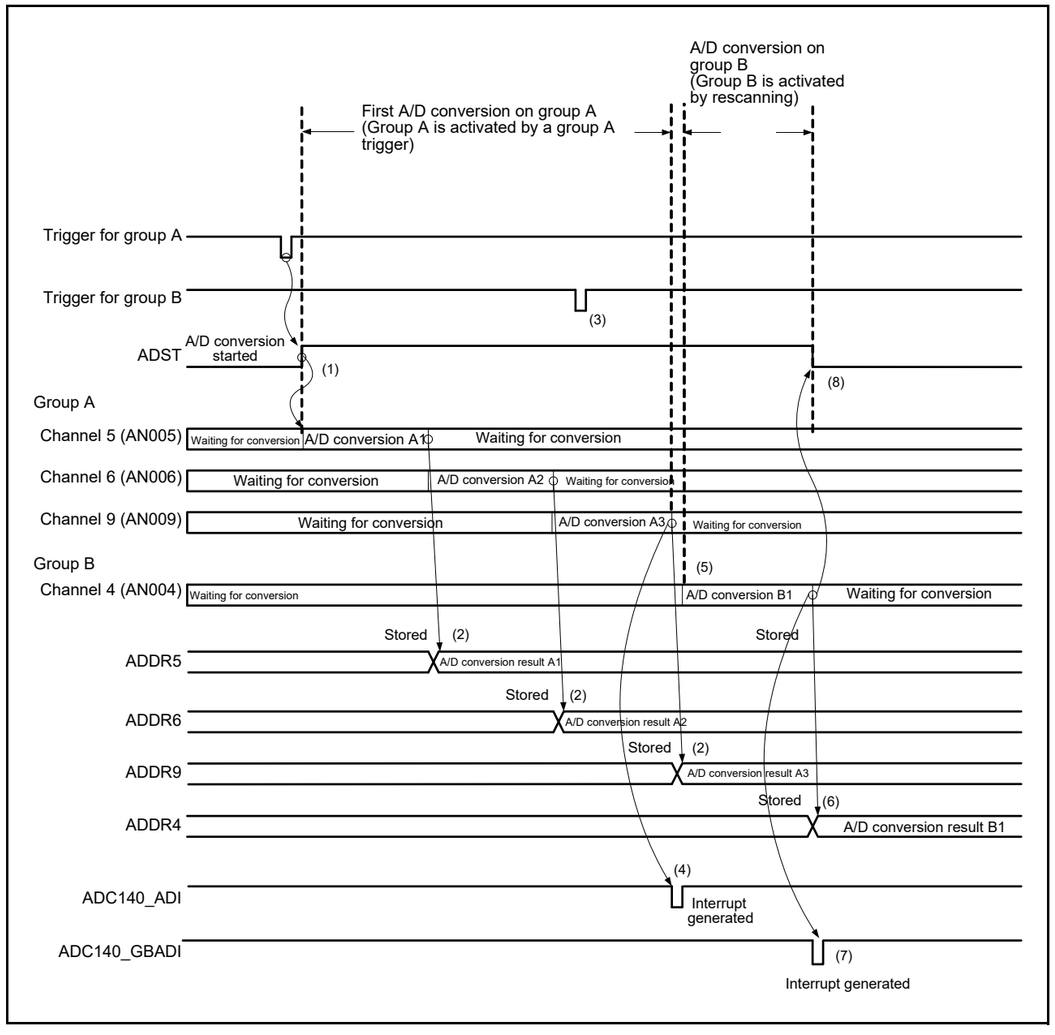


Figure 34.18 Example operation with group A priority control (3), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

The following sequence is an example of operation with group A priority control in which channel 4 is selected for group

被A组取消且不执行。

4. 完成A组转换后，无需设置寄存器即可生成ADC140_ADI中断请求。
5. 完成A组转换后，ADCSR.ADST位保持为1，并重新扫描B组。然后，在ADANSB0和ADANSB1寄存器中选择的B组ANn通道的AD转换从编号n最小的通道开始按顺序开始。
6. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
7. 对B组的重新扫描操作完成后，如果ADCSR.GBADIE位为1（启用ADC140_GBADI扫描结束中断）。
8. ADCSR.ADST位自动清零，ADC14在AD转换完成后进入等待状态。

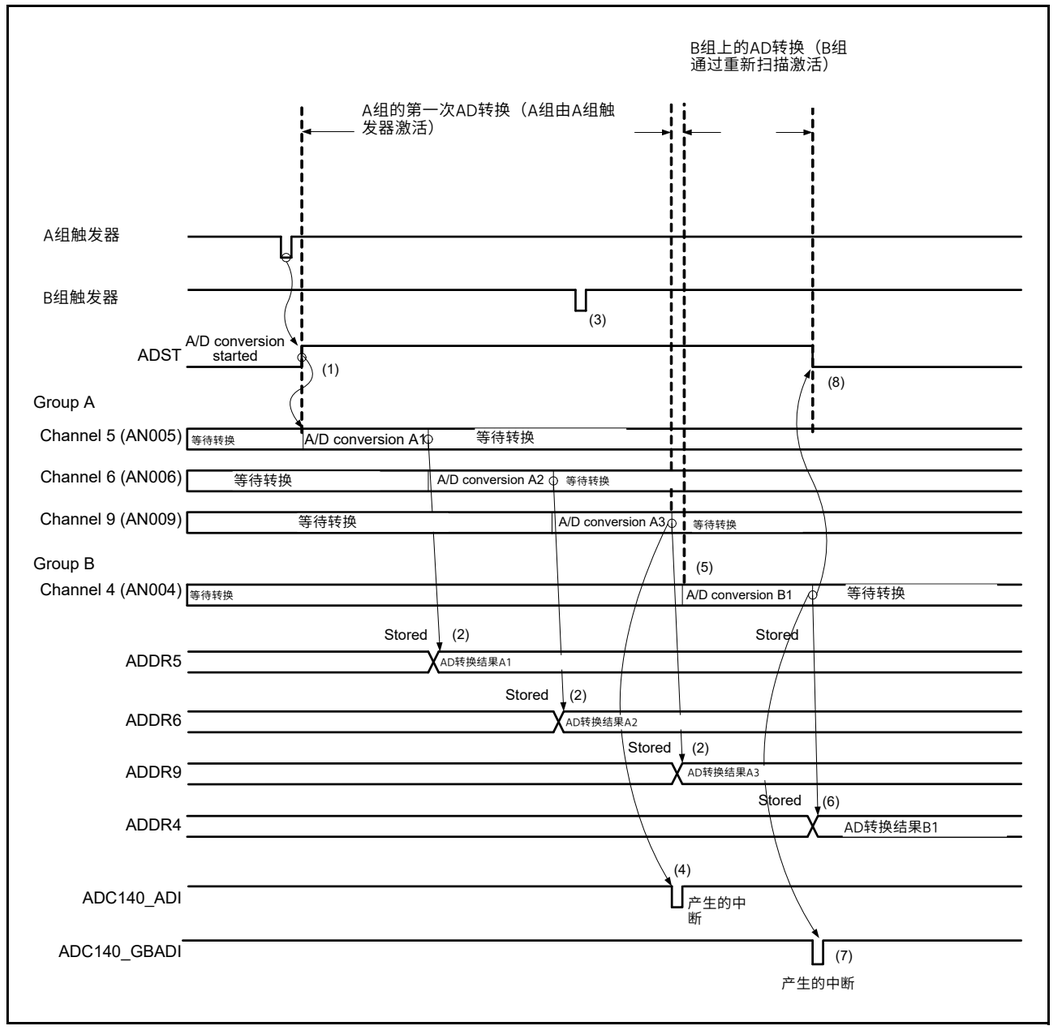


Figure 34.18 使用A组优先级控制(3)的示例操作，当ADGSPCR.GBRSCN=1并且ADGSPCR.GBRP = 0

以下序列是使用A组优先控制的操作示例，其中通道4被选为组

A and channels 5, 6, and 9 are selected for group B (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0):

1. When input of a group B trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. Then, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
5. An ADC140_ADI interrupt request is generated without register setting.
6. The ADCSR.ADST bit is automatically cleared and the ADC14 enters the wait state when A/D conversion is complete.

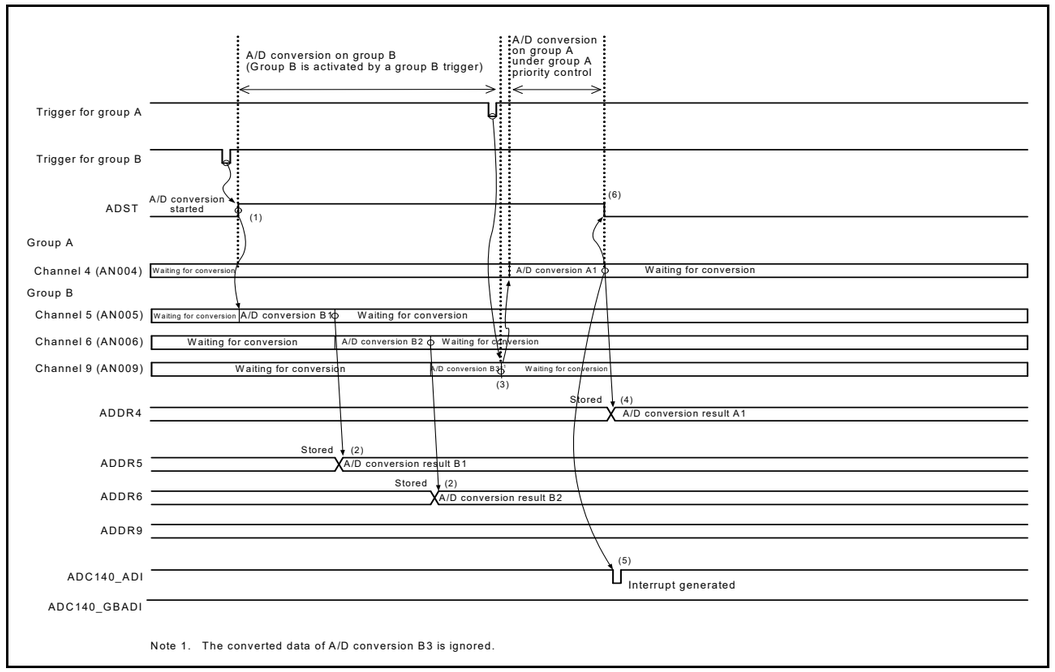


Figure 34.19 Example operation with group A priority control (4), when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0

The following sequence is an example of operation with group A priority control in which channel 4 is selected for group A and channels 5, 6, and 9 are selected for group B (ADGSPCR.GBRP = 1):

1. The ADCSR.ADST bit is set to 1 (A/D conversion start) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. Then, A/D conversion for the ANn channels selected in the

为B组选择A和通道5、6和9(ADGSPCR.GBRSCN=0 ADGSPCR.GBRP=0)：

1. 当B组触发器的输入将ADCSR.ADST位设置为1（AD转换开始）时，ADANSB0和ADANSB1寄存器中选择的ANn通道的转换从编号n最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在B组的AD转换正在进行时输入A组触发，并且B组的AD转换中断且ADCSR.ADST位保持为1。然后，在ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换开始从编号n最小的通道开始。
4. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
5. 无需寄存器设置即可生成ADC140_ADI中断请求。
6. ADCSR.ADST位自动清零，ADC14在AD转换完成后进入等待状态。

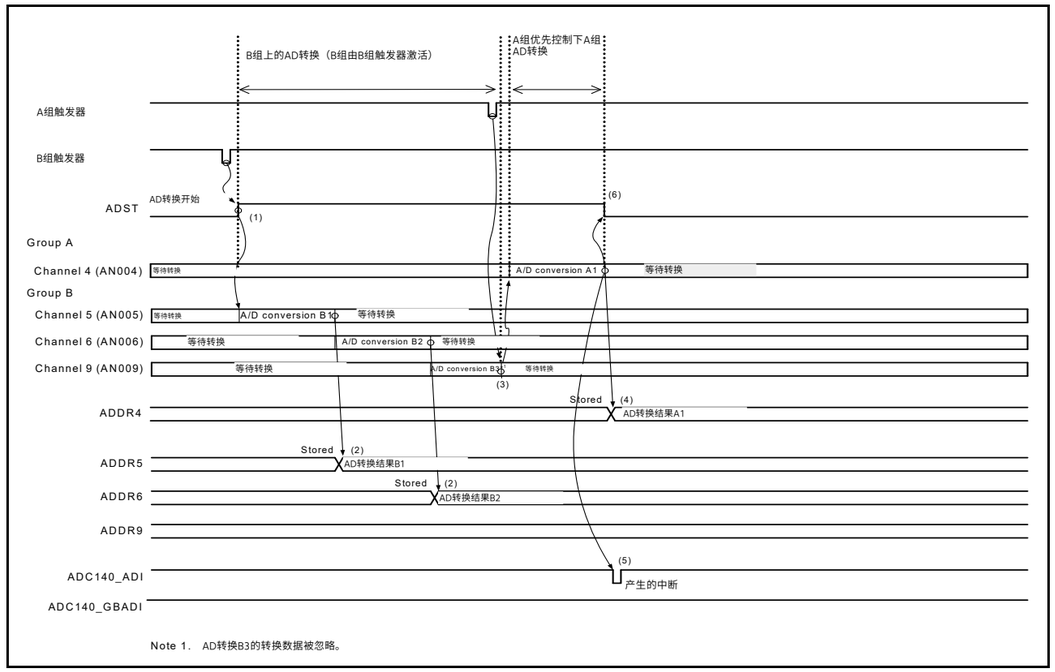


Figure 34.19 当ADGSPCR.GBRSCN=0且A组优先级控制(4)的示例操作 ADGSPCR.GBRP = 0

以下序列是使用A组优先控制的操作示例，其中通道4被选为组为B组选择A和通道5、6和9(ADGSPCR.GBRP=1)：

1. 当ADGSPCR.GBRP设置为1时，ADCSR.ADST位设置为1（AD转换开始），并且ADANSB0和ADANSB1寄存器中选择的ANn通道的转换从编号最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在B组的AD转换正在进行时输入A组触发，并且B组的AD转换中断且ADCSR.ADST位保持为1。那么，在

ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.

4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
5. An ADC140_ADI interrupt request is generated without the register setting.
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n with the ADCSR.ADST bit remains 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
8. An ADC140_GBADI interrupt request is generated if the ADCSR.GBADIE bit is 1.
9. A/D conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n. Steps 6. to 9. are repeated as long as the ADGSPCR.GBRP bit remains 1. Setting the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1. To forcibly stop A/D conversion while ADGSPCR.GBRP = 1, follow the procedure for clearing the ADCSR.ADST bit operation by software, shown in Figure 34.31.

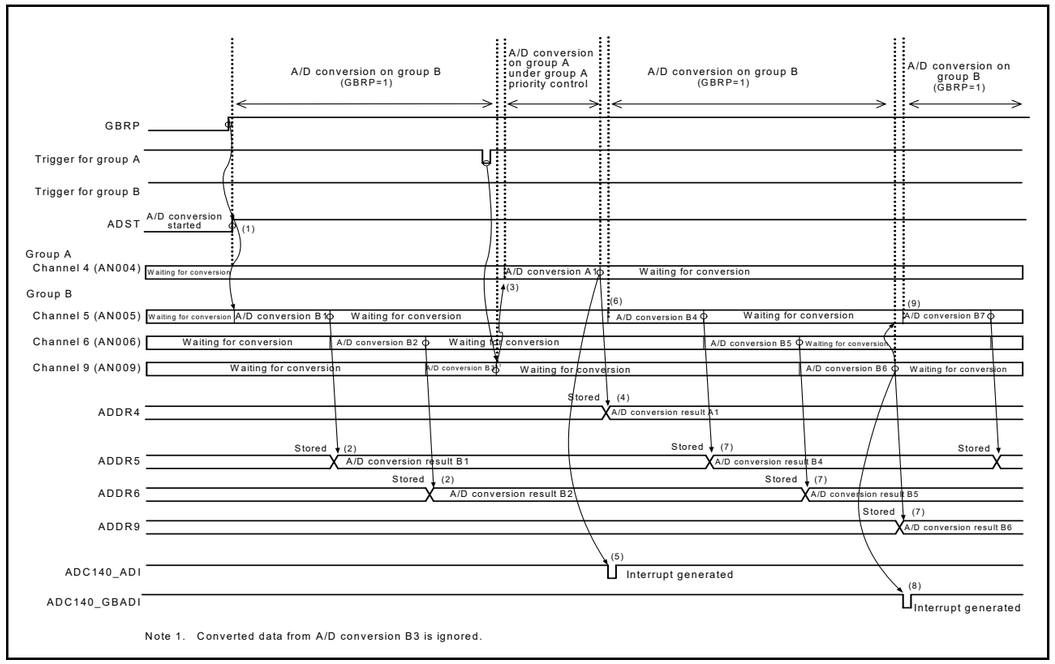


Figure 34.20 Example operation with group A priority control (5) when ADGSPCR.GBRP = 1

34.3.5 Compare Function for Window A and Window B

34.3.5.1 Compare function

The compare function compares a reference value with the A/D conversion result. The reference value can be set for window A and window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. The main differences between window A and window B are their different interrupt output signals and the restriction on window B to select only one channel.

The following sequence describes an example operation that combines continuous scan mode and the compare function.

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC), or an asynchronous trigger, A/D conversion starts for the selected channel. Do not select the temperature sensor and

ADANSA0和ADANSA1寄存器从编号n最小的通道开始。

4. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
5. 无需寄存器设置即可生成ADC140_ADI中断请求。
6. 在ADANSB0和ADANSB1寄存器中选择的B组ANn通道的AD转换从具有最小编号n的通道开始按顺序重新启动，ADCSR.ADST位保持为1。
7. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
8. 如果ADCSR.GBADIE位为1，则会产生ADC140_GBADI中断请求。
9. ADANSB0和ADANSB1寄存器中选择的ANn通道的D转换从编号n最小的通道开始按顺序开始。只要ADGSPCR.GBRP位保持为1，就重复步骤6到9。当ADGSPCR.GBRP位设置为1时，禁止将ADCSR.ADST位设置为0。当ADGSPCR.GBRP=时强制停止AD转换1、按照软件清零ADCSR.ADST位操作流程，如图34.31所示。

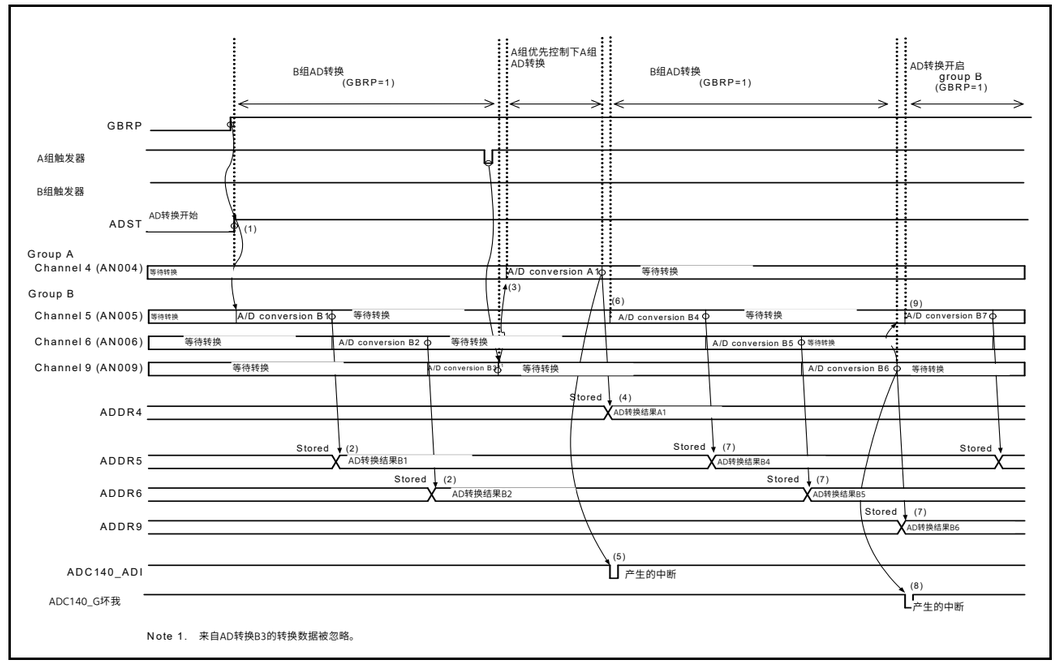


Figure 34.20 ADGSPCR.GBRP=1时A组优先级控制(5)的示例操作

34.3.5 比较窗口A和窗口B的功能

34.3.5.1 比较功能

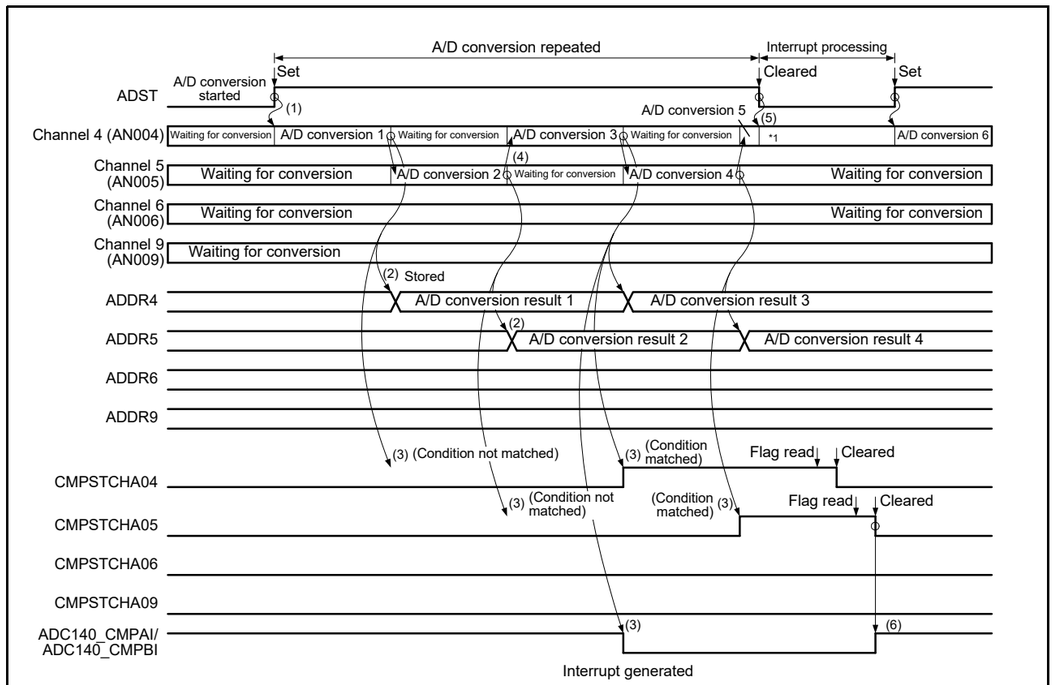
比较功能将参考值与AD转换结果进行比较。可以分别为窗口A和窗口B设置参考值。使用比较功能时，不能使用自诊断功能和双触发模式。窗口A和窗口B的主要区别在于它们不同的中断输出信号以及窗口B只能选择一个通道的限制。

以下序列描述了结合连续扫描模式和比较功能的示例操作。

1. 当ADCSR.ADST位通过软件、同步触发(ELC)或异步触发设置为1（AD转换开始）时，所选通道的AD转换开始。不要选择温度传感器和

internal reference voltage at the same time. Additionally, when the internal reference voltage is selected as the high-potential reference voltage, A/D conversion of the temperature sensor or internal reference voltage is prohibited.

2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE = 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for window A, the A/D conversion result is compared with the set ADCMPDR0/1 register value. When ADCMPCR.CMPBE = 1, if bits in the ADCMPBNSR register are set for window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register value.
3. As a result of the comparison, when window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Window A flag (ADCMPSR0.CMPSTCHAn, ADCMPSR1.CMPSTCHAn, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) is set to 1. If the ADCMPCR.CMPAIE bit is 1, an ADC140_CMPAI interrupt request is generated. In the same way, when window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Window B flag (ADCMPBSR.CMPSTB) is set to 1. If the ADCMPCR.CMPBIE bit is 1, an ADC140_CMPBI interrupt request is generated.
4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC140_CMPAI and ADC140_CMPBI interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed on channels for which the compare flag is set to 1.
6. When all compare flags of window A are cleared, an ADC140_CMPAI interrupt request is canceled. In the same way, when all compare flags of window B are cleared, an ADC140_CMPBI interrupt request is canceled. To perform comparison again, restart the A/D conversion.



Note 1. Data on conversion is ignored.

Figure 34.21 Example of compare function operation, when AN004 to AN006, and AN009 are compared

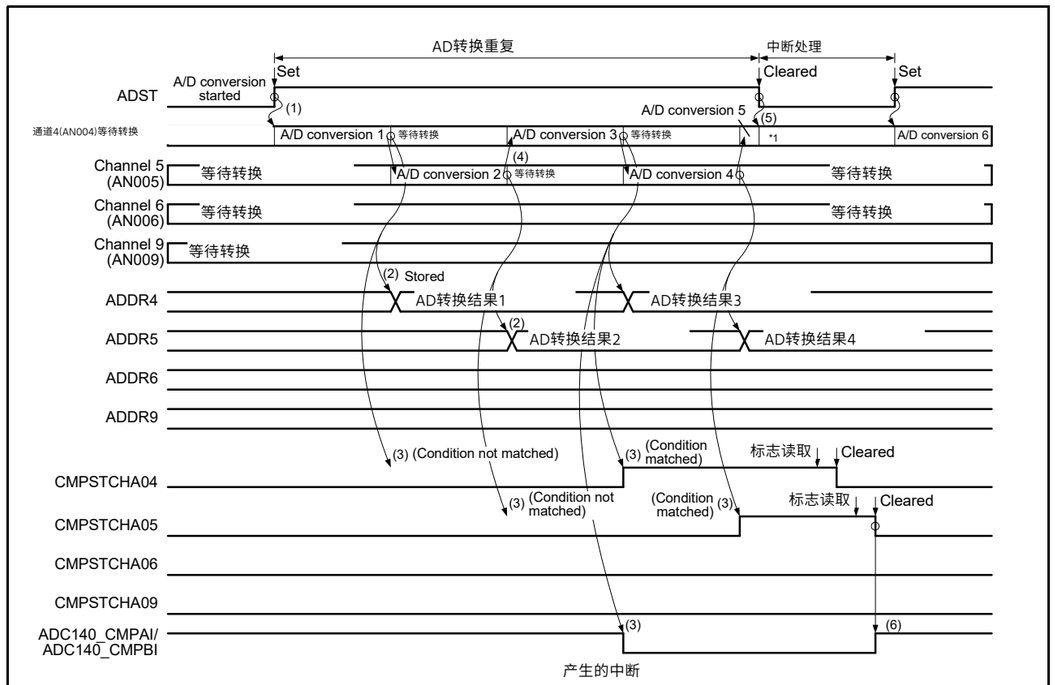
34.3.5.2 Event output of compare function

The event output of the compare function specifies the upper reference voltage value for window A and the lower reference voltage value for window B, compares the A/D-converted value of the selected channel with the upper and

同时内部参考电压。Additionally whentheinternalreferencevoltageisselectedasthehighpotentialreference voltage ADconversionofthetemperaturesensororinternalreferencevoltageisprohibited.

2. 完成AD转换后，AD转换结果存储在相关的AD数据寄存器（ADDRy、ADTSDR或ADOCDR）中。当ADCMPCR.CMPAE=1时，如果ADCMPANSRy寄存器或ADCMPANSER寄存器中的位为窗口A设置，则AD转换结果与设置的ADCMPDR01寄存器值进行比较。当ADCMPCR.CMPBE=1时，如果ADCMPBNSR寄存器中的位为窗口B设置，则AD转换结果与ADWINULBADWINLLB寄存器值进行比较。
3. 作为比较的结果，当窗口A满足ADCMPLR01或ADCMPLER中设置的条件时，比较窗口A标志（ADCMPSR0.CMPSTCHAn、ADCMPSR1.CMPSTCHAn、ADCMPSER.CMPSTTSA或ADCMPSER.CMPSTOCA）设置为1。如果ADCMPCR.CMPAIE位为1，产生ADC140_CMPAI中断请求。同样，当窗口B满足ADCMPBNSR.CMPLB中设置的条件时，比较窗口B标志（ADCMPBSR.CMPSTB）设置为1。如果ADCMPCR.CMPBIE位为1，则

   ADC140_CMPBI中断请求产生。
4. 完成所有选定的AD转换和比较后，扫描重新开始。
5. 接受ADC140_CMPAI和ADC140_CMPBI中断后，ADCSR.ADST位设置为0（AD转换停止），并对比较标志设置为1的通道执行处理。
6. 当窗口A的所有比较标志都被清除时，ADC140_CMPAI中断请求被取消。同理，当窗口B的所有比较标志都被清除时，一个ADC140_CMPBI中断请求被取消。要再次进行比较，请重新开始AD转换。



Note 1. 转换数据被忽略。

Figure 34.21 比较功能操作示例，当比较AN004到AN006和AN009时

34.3.5.2 比较函数的事件输出

比较功能的事件输出指定窗口A的上参考电压值和窗口B的下参考电压值，将所选通道的AD转换值与上、下比较

lower side reference voltage values, and outputs the ADC140_WCMPM/ADC140_WCMPUM events according to event conditions (A OR B, A AND B, A XOR B) and comparison result of window A and window B.

If more than one channel is selected for window A, and even one channel in window A meets the comparison condition, the comparison result of window A is met. When using this function, perform A/D conversion in single scan mode.

Any channels from AN004 to AN006, AN009, AN010, AN017, AN019, and A020, internal reference voltage, and temperature sensor output are selectable for window A. However, neither the internal reference voltage nor the temperature sensor output can be selected together with any other channel. In addition, if the internal reference voltage is selected as the high-potential reference voltage of the ADC14, the internal reference voltage or the temperature sensor output cannot be A/D-converted.

A single channel from AN004 to AN006, AN009, AN010, AN017, AN019, and A020, internal reference voltage, and temperature sensor output is selectable for window B. However, neither the internal reference voltage nor the temperature sensor output can be selected together with any other channel. In addition, if the internal reference voltage is selected as the high-potential reference voltage, the internal reference voltage or the temperature sensor output cannot be A/D-converted.

The following sequence describes the setting procedure and example when using event output of the compare function:

1. Confirm that the ADCSR.ADCS[1:0] bits are 00b (single scan mode).
2. Select the channel for window A in ADCMPANSR0/1 and ADCMPANSER. Set the window comparison conditions in ADCMPLR0/1, ADCMPLER registers. Set the upper and lower reference values in the ADCMPDR0/1 registers.
3. Select the channel and comparison conditions for window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB and ADWINLLB registers.
4. Set the composite conditions for window A/B, window A/B operation enable, and interrupt output enable in the ADCMPCR register.

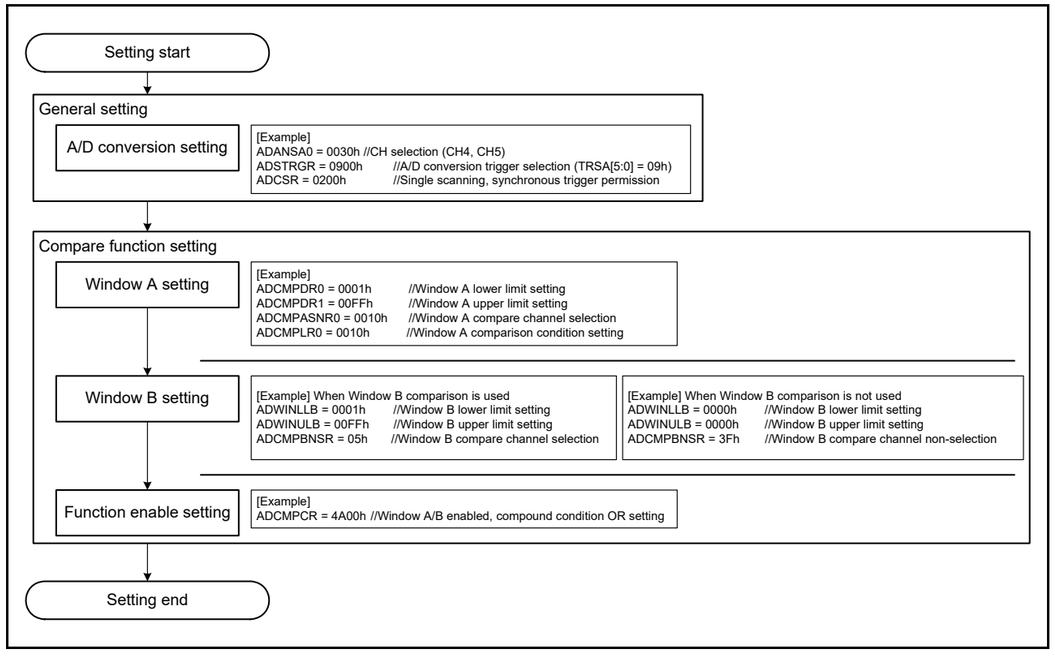


Figure 34.22 Setting example when using event output of the compare function

For event output usage when using only window A for the compare function, note the following:

- Enable both window A and window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)

下侧参考电压值，并根据事件条件（AORB、AANDB、AXORB）和窗口A和窗口B的比较结果输出ADC140_WCMPMADC140_WCMPUM事件。

如果为窗口A选择了多个通道，即使窗口A中的一个通道满足比较条件，也满足窗口A的比较结果。使用此功能时，请在单次扫描模式下进行AD转换。

窗口A可选择从AN004到AN006、AN009、AN010、AN017、AN019和A020的任何通道、内部参考电压和温度传感器输出。但是，不能同时选择内部参考电压和温度传感器输出。其他频道。此外，如果选择内部参考电压作为ADC14的高电位参考电压，则内部参考电压或温度传感器输出不能进行AD转换。

窗口B可选择从AN004到AN006、AN009、AN010、AN017、AN019和A020的单通道、内部参考电压和温度传感器输出。但是，不能同时选择内部参考电压和温度传感器输出任何其他频道。此外，如果选择内部参考电压作为高电位参考电压，则内部参考电压或温度传感器输出不能进行AD转换。

以下序列描述了使用比较功能的事件输出时的设置过程和示例：

1. 确认ADCSR.ADCS[1:0]位为00b（单次扫描模式）。
2. 在ADCMPANSR01和ADCMPANSER中选择窗口A的通道。在ADCMPLR01，ADCMPLER寄存器中设置窗口比较条件。在ADCMPDDR01寄存器中设置参考值上限和下限。
3. 在ADCMPBNSR寄存器中选择窗口B的通道和比较条件，并在ADWINULB和ADWINLLB寄存器中设置上下参考值。
4. 设置窗口AB、窗口AB操作使能和中断输出使能的复合条件
ADCMPCR register.

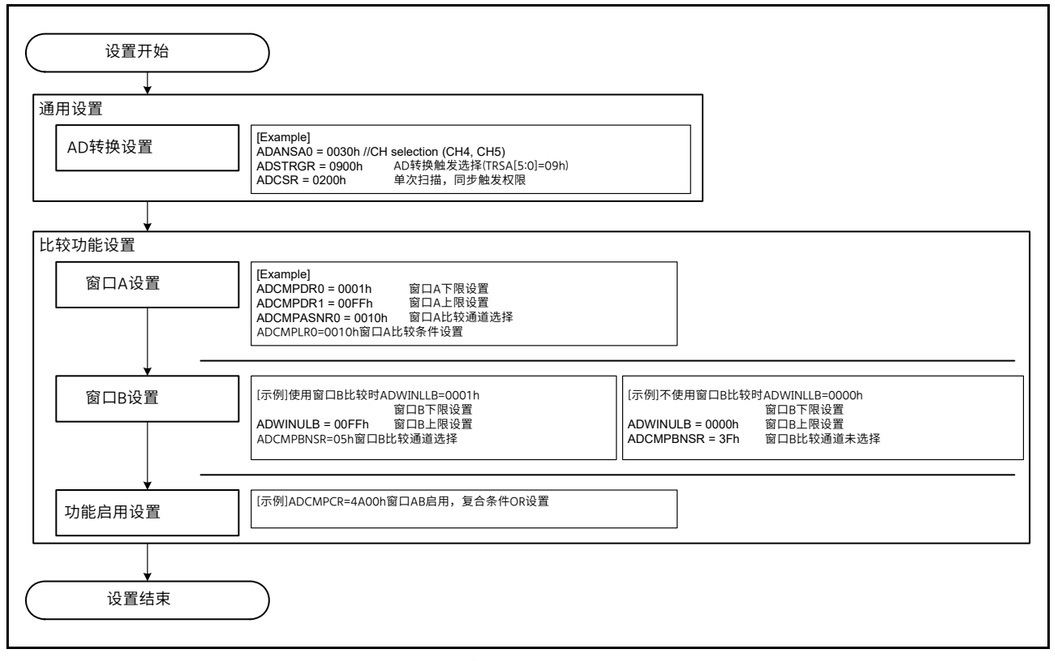


Figure 34.22 使用比较功能的事件输出时的设置示例

对于仅将窗口A用于比较功能时的事件输出用法，请注意以下几点：

- 启用窗口A和窗口B(ADCMPCR.CMPAE=1 ADCMPCR.CMPBE=1)

- Set the compound condition of window A and B to OR condition (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of window B to "Do not select" (ADCMPBNSR.CMPCHB[5:0] = 111111b)
- Set the compare condition of window B to 0 < results < 0 means mismatch always (ADCMPCR.WCMPE = 1, ADWINLLB[15:0] = ADWINULB[15:0] = 0000h, ADCMPBNSR.CMPLB = 1).

Figure 34.23 shows an example event output operation of the compare function.

A scan end event (ADC140_ADI) is output at the same time as a one-time single scan completion. A match or mismatch event (ADC140_WCMPM/ADC140_WCMPUM) is output with a clock delay of 1 PCLKB cycle set in ADCMPCR.CMPAB[1:0].

Note: The match and mismatch events are exclusive, so both events do not output simultaneously.

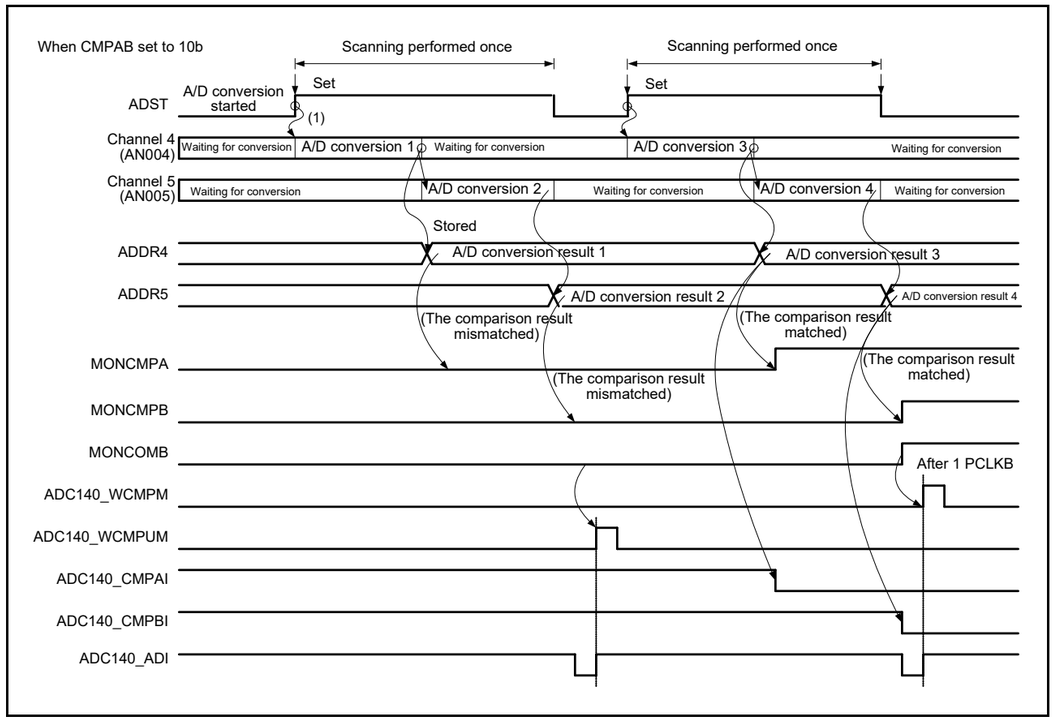


Figure 34.23 Event output operation example of compare function when AN004 to AN005 are compared

Note: Event output of the compare function outputs match/mismatch from the comparison results of window A and window B, as set in ADCMPCR.CMPAB[1:0].

Note: The comparison result of window A is the logical addition of the comparison results of the comparison target channels of window A. The comparison results of window A and B are updated by each A/D conversion, and are kept even when single scan ends. To clear the comparison results to 0, set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0.

34.3.5.3 Restrictions on the compare function

The following restrictions apply to the compare function:

- The compare function cannot be used together with the self-diagnosis function or double trigger mode. The compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.
- Specify single scan mode when using match/mismatch event outputs

- 将窗口A和B的复合条件设置为OR条件(ADCMPCR.CMPAB[1:0]=00b)
- 将窗口B的比较通道设置为"不选择"（ADCMPBNSR.CMPCHB[5:0]=111111b）
- 将窗口B的比较条件设置为0<结果<0表示始终不匹配(ADCMPCR.WCMPE=1 ADWINLLB[15:0] = ADWINULB[15:0] = 0000h, ADCMPBNSR.CMPLB = 1).

图34.23显示了比较函数的示例事件输出操作。

扫描结束事件(ADC140_ADI)与一次性单次扫描完成同时输出。匹配或不匹配事件(ADC140_WCMPMADC140_WCMPUM)以在ADCMPCR.CMPAB[1:0]中设置的1个PCLKB周期的时钟延迟输出。

Note: match和mismatch事件是互斥的，因此两个事件不会同时输出。

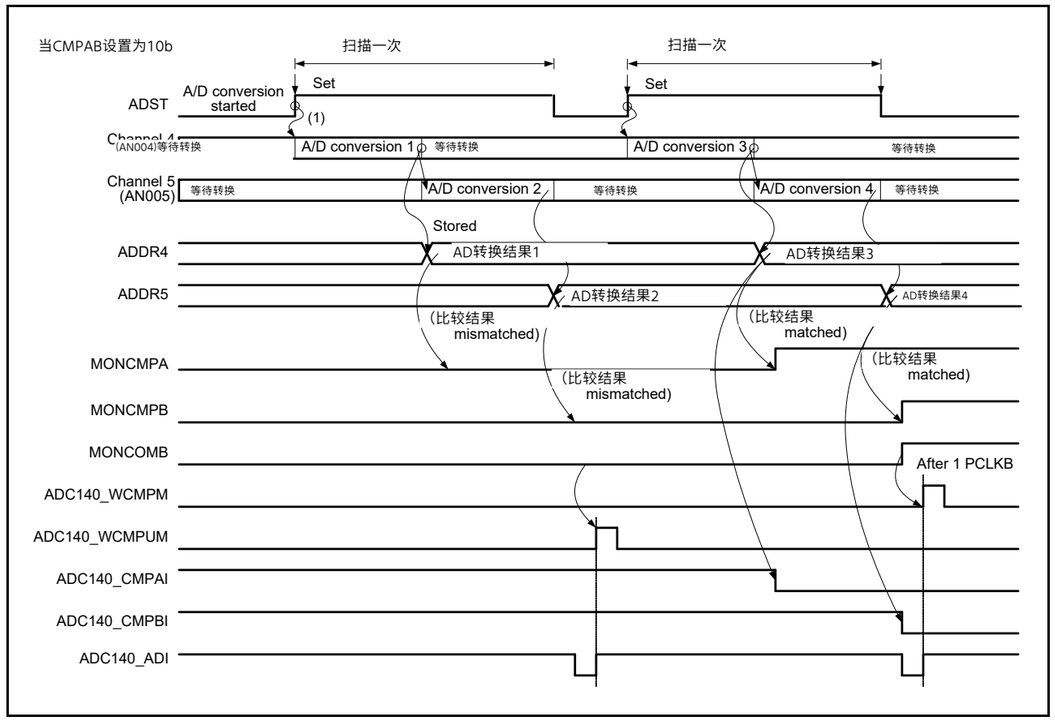


Figure 34.23 比较AN004和AN005时比较功能的事件输出操作示例

Note: 比较函数的事件输出从窗口A和窗口B的比较结果输出匹配不匹配，如ADCMPCR.CMPAB[1:0]中设置的那样。

Note: 窗口A的比较结果是窗口A的比较目标通道的比较结果的逻辑相加。窗口A和窗口B的比较结果在每次AD转换时更新，即使单次扫描结束也保持不变。要将比较结果清除为0，请将ADCMPCR.CMPAE和ADCMPCR.CMPBE设置为0。

34.3.5.3 比较功能的限制

以下限制适用于比较功能：

- 比较功能不能与自诊断功能或双触发模式一起使用。比较功能不适用于ADRD、ADDBLDR、ADDBLDRA和ADDBLDRB。
- 使用匹配不匹配事件输出时指定单次扫描模式

- When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled
- When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled
- Setting the same channel for window A and window B is prohibited
- Set the reference voltage values so that the high-potential reference voltage value is equal to or larger than the low-potential reference voltage value.

34.3.6 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRG0). After the start-of-scanning-delay time (t_D) elapses, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed, followed by processing for A/D conversion.

Figure 34.24 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 34.25 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger, ADTRG0. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), disconnection detection assistance processing time (t_{DIS})*1, self-diagnosis A/D conversion processing time (t_{DIAG} and t_{DSD})*2, A/D conversion processing time (t_{CONV}), and end-of-scanning-delay time (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the ADC14. If the sampling time is not sufficient because of the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTR register.

The time for conversion by successive approximation (t_{SAM}) is 37.5 ADCLK states with 14-bit accuracy and High-speed mode selected, 46.5 ADCLK states with 14-bit accuracy and low-current mode selected, 31.5 ADCLK states with 12-bit accuracy and High-speed mode selected, and 40.5 ADCLK states with 12-bit accuracy and low-current mode selected. Table 34.10 shows the times for conversion during scanning.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV}{}^{*3} \times n) + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED}. The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed at $(t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV}{}^{*3} \times n)$.

Note 1. When disconnection detection assistance is not selected, $t_{DIS} = 0$.
Only when the temperature sensor or internal reference voltage is A/D-converted, the auto-discharge period of 15 ADCLK states is inserted.
Note 2. When the self-diagnosis function is not used, $t_{DIAG} = 0$, $t_{DSD} = 0$.
Note 3. When input sampling time (tSPL) of all selected channels are the same, this element equals tCONV × n. If each channel has a different sampling time, this element equals the sum of tSPL and tSAM for each selected channel.

- 当为窗口A选择温度传感器或内部参考电压时，窗口B操作被禁用
- 当为窗口B选择温度传感器或内部参考电压时，窗口A操作被禁用
- 禁止将窗口A和窗口B设置为同一通道
- 设置参考电压值，使高电位参考电压值等于或大于低电位参考电压值。

34.3.6 模拟输入采样和扫描转换时间

扫描转换可以通过软件触发、同步触发(ELC)或异步触发(ADTRG0)来激活。在经过扫描开始延迟时间(tD)之后，断线检测辅助处理和自诊断转换处理全部进行，接着进行AD转换处理。

图34.24显示了扫描转换时序，其中扫描转换由软件触发或同步触发(ELC)激活。图34.25显示了扫描转换时序，其中扫描转换由异步触发器ADTRG0激活。扫描转换时间(tSCAN)包括扫描开始延迟时间(tD)、断线检测辅助处理时间(tDIS)*1、自诊断AD转换处理时间(tDIAG和tDSD)*如图2所示，AD转换处理时间(tCONV)和扫描结束延迟时间(tED)。

AD转换处理时间(tCONV)由输入采样时间(tSPL)和逐次逼近转换时间(tSAM)组成。采样时间(tSPL)用于为ADC14中的采样保持电路充电。如果由于模拟输入信号源的高阻抗而导致采样时间不足，或者如果AD转换时钟(ADCLK)很慢，则可以使用ADSSTR寄存器调整采样时间。

逐次逼近转换时间(tSAM)为37.5个ADCLK状态，14位精度和高速模式选择，46.5个ADCLK状态，14位精度和低电流模式，31.5个ADCLK状态，12位精度选择高速模式，选择40.5ADCLK状态，12位精度和低电流模式。表34.10显示了扫描期间的转换时间。

选择通道数为n的单次扫描模式下的扫描转换时间(tSCAN)可以确定如下：

tSCAN=tD+(tDIS×n)+tDIAG+tDSD+(tCONV*3×n)+tED

连续扫描模式下第一个周期的扫描转换时间是单次扫描的tSCAN减去tED。连续扫描模式下第二个和后续周期的扫描转换时间固定为(tDIS×n)+tDIAG+tDSD+(tCONV*3×n)。

注1.未选择断线检测辅助时，tDIS=0。
只有当温度传感器或内部参考电压经过AD转换时，才会插入15个ADCLK状态的自动放电周期。注2.不使用自诊断功能时，tDIAG=0，tDSD=0。

注3.当所有选定通道的输入采样时间(tSPL)相同时，该元素等于tCONV×n。如果每个通道具有不同的采样时间，则该元素等于每个选定通道的tSPL和tSAM之和。

Table 34.10 Times for conversion during scanning (in number of ADCLK and PCLKB cycles)

Parameter			Symbol		Type/Conditions: Synchronous trigger*6	Type/Conditions: Asynchronous trigger	Type/Conditions: Software trigger	Unit
Scan start processing time*1, *2	A/D conversion on group A with group A priority control	Group B is to be stopped. (group A is activated after group B is stopped due to an A/D conversion source from group A.)	t_D		3 PCLKB + 6 ADCLK, 5 PCLKB + 3 ADCLK*5	—	—	Cycle
		Group B is not to be stopped. (Activation by an A/D conversion source from group A.)			2 PCLKB + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started.			2 PCLKB + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	Other than above				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
Disconnection detection assistance processing time			t_{DIS}		The setting of ADNDIS[3:0] (initial value = 00h) × ADCLK*3			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	The setting of ADSSTR00 (initial value = 0Dh) × ADCLK*4 + 0.5 ADCLK*4			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	31.5 ADCLK at High-speed mode 40.5 ADCLK at Low-current mode			
		14-bit conversion accuracy			37.5 ADCLK at High-speed mode 46.5 ADCLK at Low-current mode			
	Wait time between self-diagnosis conversion end and analog channel sampling start			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode			t_{DSD}	2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	The setting of ADSSTRn (n = 0 to 15, L, T, O) (initial value = 0Dh) x ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	31.5 ADCLK at High-speed mode 40.5 ADCLK at Low-current mode			
		14-bit conversion			37.5 ADCLK at High-speed mode 46.5 ADCLK at Low-current mode			
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK, 2 PCLKB + 3 ADCLK*5			

Note 1. See Figure 34.24 and Figure 34.25 for illustration of times t_D, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to starting A/D conversion.
Note 3. The value is fixed to 0Fh (15 ADCLK) when the temperature sensor output or internal reference voltage is A/D-converted.
Note 4. The required sampling time (ns) is specified according to the voltage conditions. The sampling time setting must satisfy the electrical characteristics.
Note 5. If ADCLK is faster than PCLKB (PCLKB to ADCLK frequency ratio = 1:2 or 1:4).
Note 6. This does not include the time consumed in the path from timer output to trigger input.

Table 34.10 扫描期间的转换时间（以ADCLK和PCLKB周期数计）

Parameter			Symbol		Type/Conditions: 同步触发*6	Type/Conditions: 异步触发	Type/Conditions: 软件触发	Unit
扫描开始处理时间*1、*2	A组AD转换，A组优先控制	B组将被停止。（由于A组的AD转换源，B组停止后，A组激活。）	t_D		3 PCLKB + 6 ADCLK, 5 PCLKB + 3 ADCLK*5	—	—	Cycle
		B组不要停止。（由A组的AD转换源激活。）			2 PCLKB + 4 ADCLK	—	—	
	启用自诊断时的AD转换	将启动用于自诊断的D转换。			2 PCLKB + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	上述以外				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
断线检测辅助处理时间			t_{DIS}		ADNDIS[3:0]的设置（初始值=00h）×ADCLK*3			
自诊断转换处理时间*1	采样时间		t_{DIAG}	t_{SPL}	ADSSTR00的设置（初始值=0Dh）×ADCLK*4+0.5ADCLK*4			
	逐次逼近转换时间	12位转换精度		t_{SAM}	高速模式下为31.5ADCLK低电流模式下为40.5ADCLK			
		14位转换精度			高速模式下为37.5ADCLK低电流模式下为46.5ADCLK			
	自诊断转换结束与模拟通道采样开始之间的等待时间			t_{DED}	2 ADCLK			
	连续扫描模式下最后一次通道转换结束和自诊断采样开始之间的等待时间			t_{DSD}	2 ADCLK			
AD转换处理时间*1	采样时间		t_{CONV}	t_{SPL}	ADSSTRn(n=0to15 L T O)(初始值=0Dh)xADCLK+0.5ADCLK的设置			
	逐次逼近转换时间	12位转换精度		t_{SAM}	高速模式下为31.5ADCLK低电流模式下为40.5ADCLK			
		14-bit conversion			高速模式下为37.5ADCLK低电流模式下为46.5ADCLK			
扫描结束处理时间*1			t_{ED}		1 PCLKB + 3 ADCLK, 2 PCLKB + 3 ADCLK*5			

Note 1. 有关时间tD、tDIAG、tCONV和tED的说明，请参见图34.24和图34.25。
Note 2. 这是从软件写入或触发输入到开始AD转换所需的最长时间。
Note 3. 当温度传感器输出或内部参考电压经过AD转换时，该值固定为0Fh(15ADCLK)。
Note 4. 所需的采样时间(ns)根据电压条件指定。采样时间设置必须满足电气特性。
Note 5. 如果ADCLK比PCLKB快（PCLKB与ADCLK频率比=1:2或1:4）。
Note 6. 这不包括从定时器输出到触发输入的路径中消耗的时间。

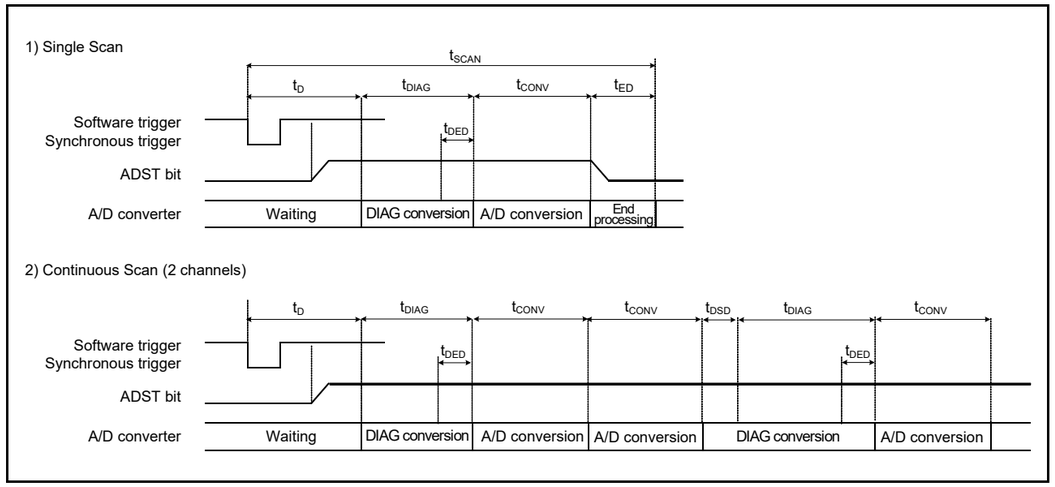


Figure 34.24 Scan conversion timing when activated by software or synchronous trigger input (ELC)

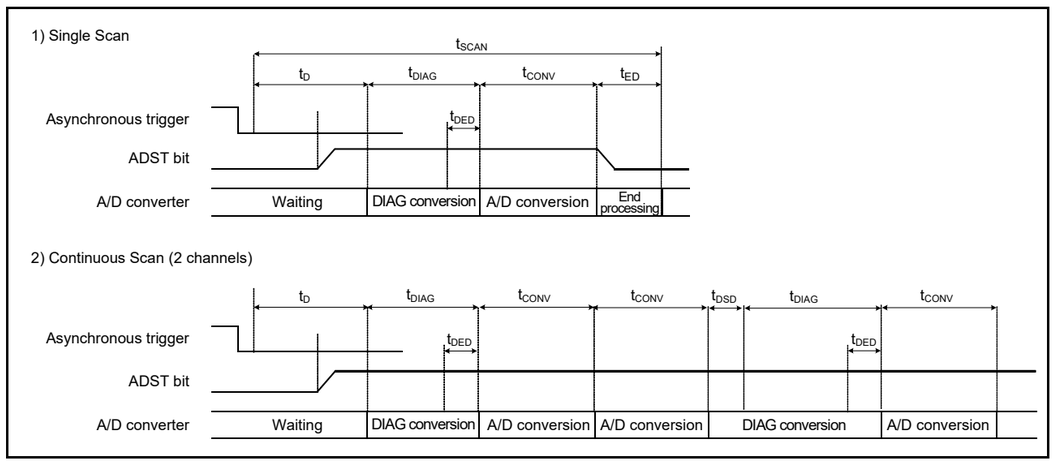


Figure 34.25 Scan conversion timing when activated by asynchronous trigger input (ADTRG0)

34.3.7 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ACE bit in ADCER to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR) to 0000h when the A/D data registers are read by the CPU, DTC, or DMAC.

This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR). In the following examples, the function to automatically clear the ADDRy register is enabled and disabled:

- When the ACE bit in ADCER is 0 (automatic clearing disabled) and, for some reason, if the A/D conversion result (0222h) is not written to the ADDRy register, the ADDRy value retains the old data (0111h). In addition, if this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0111h) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.
- When the ACE bit in ADCER is 1 (automatic clearing enabled), if ADDRy = 0111h is read by the CPU, DTC, or DMAC, ADDRy is automatically set to 0000h. If the A/D conversion result of 0222h cannot be transferred to

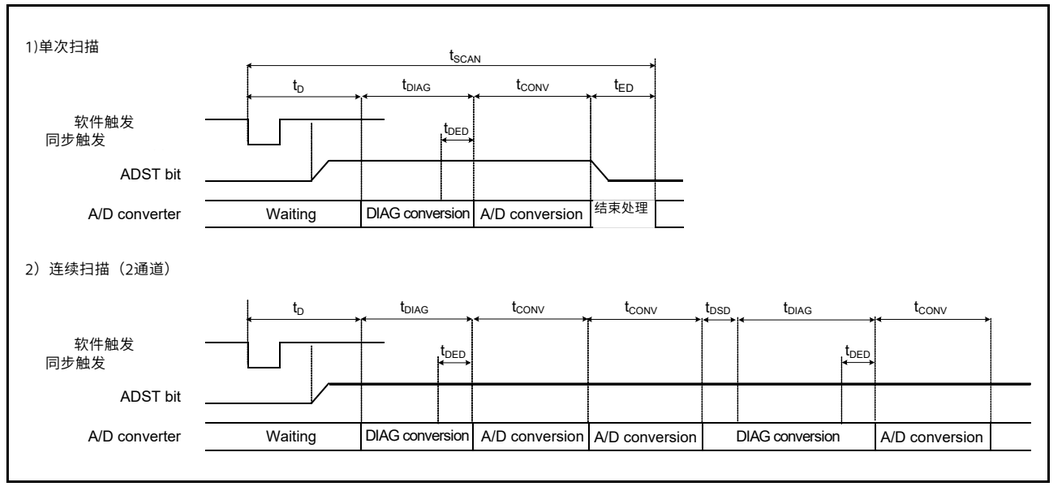


Figure 34.24 由软件或同步触发输入(ELC)激活时的扫描转换时序

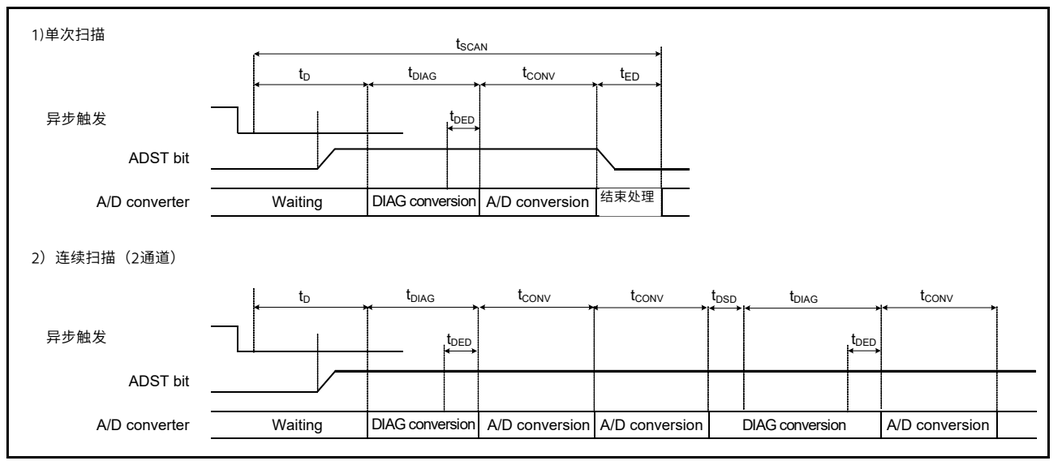


Figure 34.25 由异步触发输入(ADTRG0)激活时的扫描转换时序

34.3.7 AD数据寄存器自动清除功能的使用示例

将ADCER中的ACE位设置为1会自动清除AD数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR）到0000h，当CPU、DTC或DMAC.

该功能可以检测AD数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR）。在以下示例中，自动清除ADDRy寄存器启用和禁用：

- 当ADCER中的ACE位为0（禁止自动清除），并且由于某种原因，如果AD转换结果（0222h）没有写入ADDRy寄存器，则ADDRy值保留旧数据（0111h）。此外，如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则可以将旧数据（0111h）保存在通用寄存器中。在检查是否有更新失败时，需要经常将旧数据保存在SRAM或通用寄存器中。
- 当ADCER中的ACE位为1（使能自动清除）时，如果CPU读取ADDRy=0111h，则DTC或DMAC ADDRy自动设置为0000h。如果0222h的AD转换结果不能传送到

ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, 0000h is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0000h.

34.3.8 A/D-Converted Value Addition/Average Mode

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, A/D conversion of the temperature sensor output, or A/D conversion of the internal reference voltage is selected.

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16*1 consecutive times and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted 2 or 4 consecutive times and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. However, this function cannot always guarantee an improvement in A/D conversion accuracy.

The A/D-converted value addition or average mode can be specified for A/D conversion of the channel select analog input, temperature sensor output, or internal reference voltage.

Note 1. The addition count can be set to 16 only when 12-bit accuracy is selected.

34.3.9 Disconnection Detection Assist Function

The ADC14 incorporates the disconnection detection assist function to fix the charge for sampling capacitance to the specified state VREFH0 or VREFL0 before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

If any of the following functions are used, the disconnection detection assist function must be disabled:

- The temperature sensor
- The internal reference voltage
- The A/D self-diagnosis.

Figure 34.26 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 34.27 shows an example of disconnection detection when precharge is selected. Figure 34.28 shows an example of disconnection detection when discharge is selected.

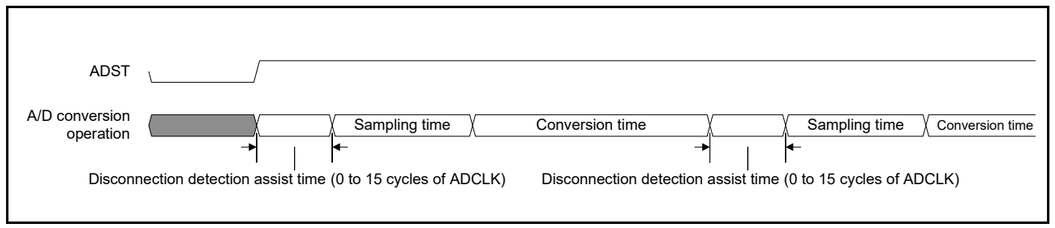


Figure 34.26 A/D conversion operation when the disconnection detection assist function is used

ADDRy由于某种原因，清除的数据(0000h)仍保留为ADDRy值。如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则将0000h保存在通用寄存器中。ADDRy更新失败的发生可以通过检查读取的数据值为0000h来确定。

34.3.8 一种D转换的增值平均模式

选择通道的模拟输入的AD转换、温度传感器输出的AD转换或内部参考电压的AD转换时，可以使用D转换值加法平均模式。

在AD转换值加法模式下，同一通道连续进行1、2、3、4或16*1次AD转换，并将转换值的总和存储在数据寄存器中。在AD转换值平均模式下，同一通道连续进行2或4次AD转换，转换值的平均值存储在数据寄存器中。根据存在的噪声成分的类型，使用这些结果的平均值可以提高AD转换的精度。但是，该功能不能始终保证AD转换精度的提高。

可以为通道选择模拟输入、温度传感器输出或内部参考电压的AD转换指定AD转换值加法或平均模式。

注1.只有选择12位精度时，才能将加法计数设置为16。

34.3.9 断线检测辅助功能

ADC14包含断线检测辅助功能，可在AD转换开始前将采样电容的电荷固定到指定状态VREFH0或VREFL0。此功能可在模拟输入接线中进行断线检测。

如果使用以下任何功能，则必须禁用断线检测辅助功能：

- 温度传感器
- 内部参考电压
- The A/D self-diagnosis.

图34.26显示了使用断线检测辅助功能时的AD转换操作。图34.27显示了选择预充电时的断线检测示例。图34.28显示了选择放电时的断线检测示例。

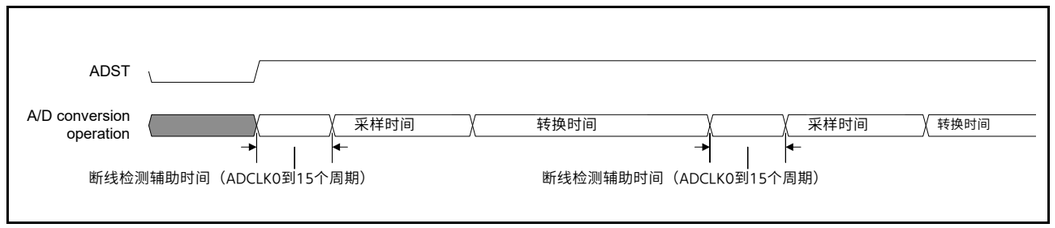
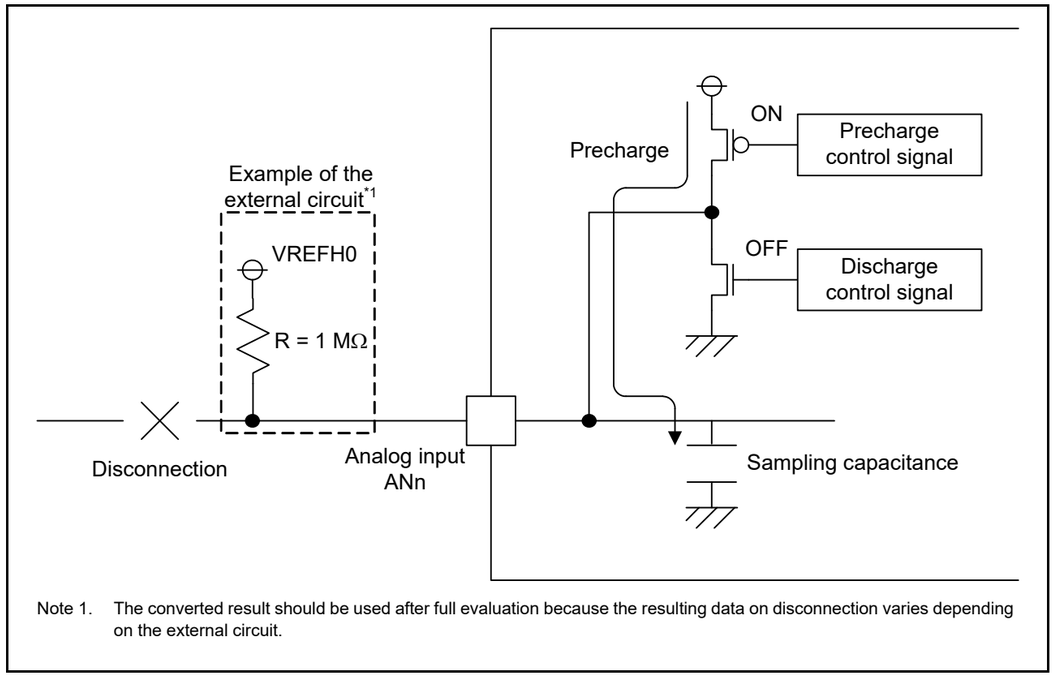
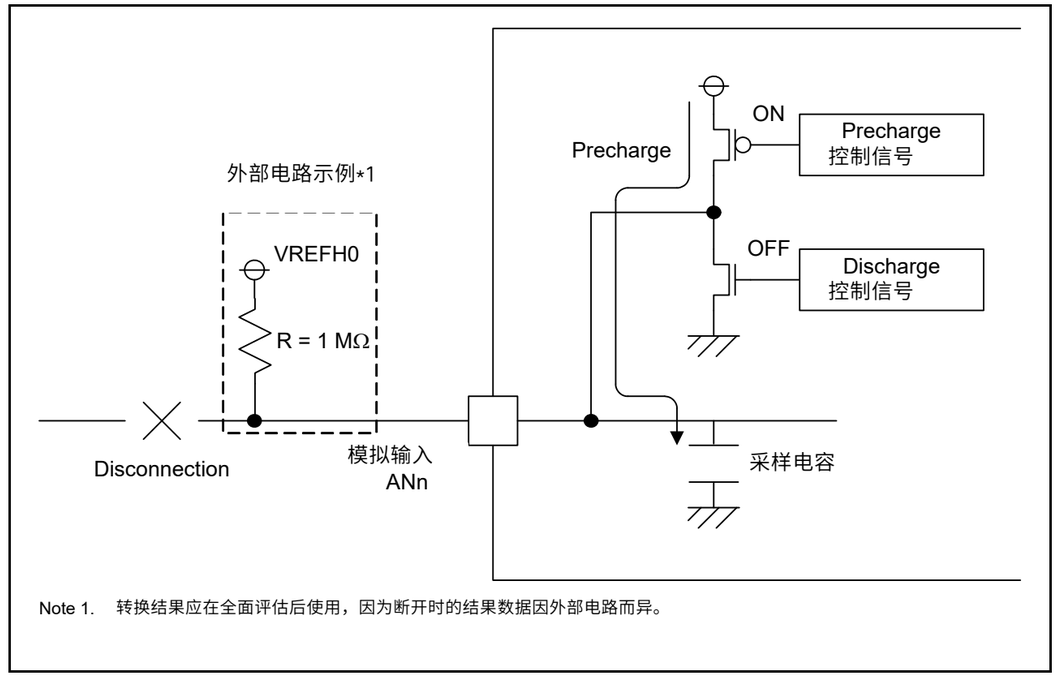


Figure 34.26 使用断线检测辅助功能时的D转换动作



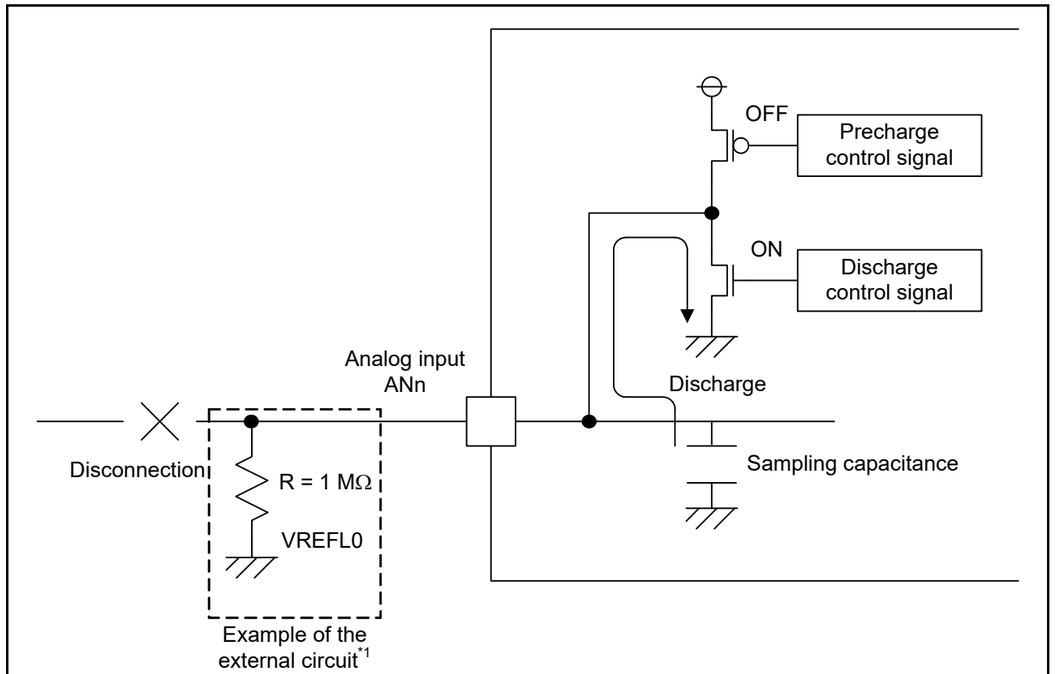
Note 1. The converted result should be used after full evaluation because the resulting data on disconnection varies depending on the external circuit.

Figure 34.27 Example of disconnection detection when precharge is selected



Note 1. 转换结果应在全面评估后使用，因为断开时的结果数据因外部电路而异。

Figure 34.27 选择预充电时的断线检测示例



Note 1. The converted result should be used after full evaluation because the resulting data on disconnection varies depending on the external circuit.

Figure 34.28 Example of disconnection detection when discharge is selected

34.3.10 Starting A/D Conversion with an Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start the A/D conversion by an asynchronous trigger:

1. Set the pin function in the PmnPFS register.
2. Set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 000000b.
3. Input a high-level signal to the asynchronous trigger (ADTRG0 pin).
4. Set the ADCSR.TRGE and ADCSR.EXTRG bits to 1.

Figure 34.29 shows the timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected in the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSB[5:0]) for group B in group scan mode. For details on setting the pin function, see section 20, I/O Ports.

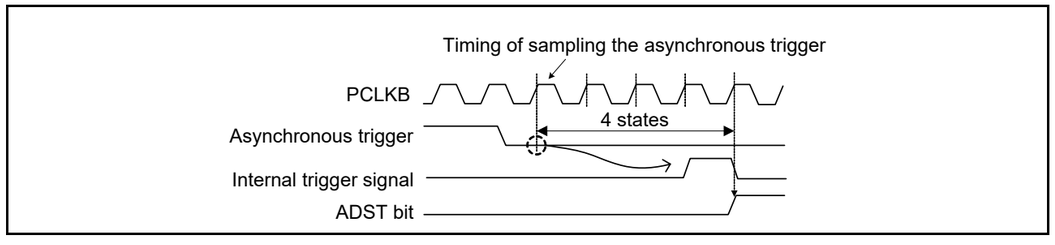
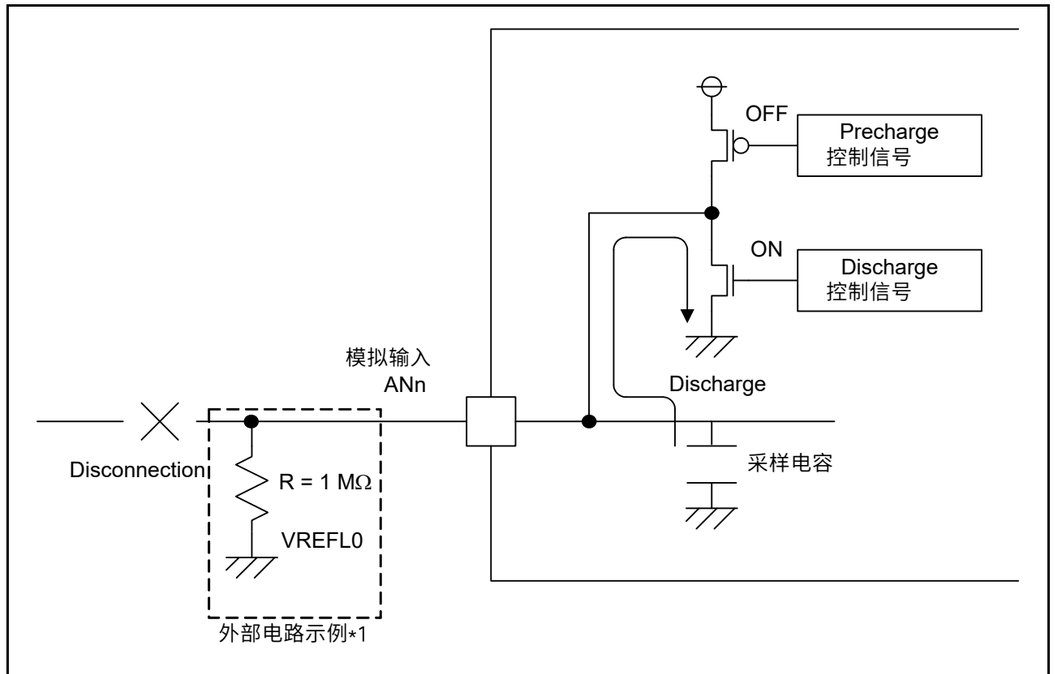


Figure 34.29 Asynchronous trigger input timing



Note 1. 转换结果应在全面评估后使用，因为断开时的结果数据因外部电路而异。

Figure 34.28 选择放电时的断线检测示例

34.3.10 使用异步触发启动AD转换

AD转换可以通过输入一个异步触发器来启动。通过异步触发启动AD转换：

1. 在PmnPFS寄存器中设置引脚功能。
2. 将AD转换开始触发选择位(ADSTRGR.TRSA[5:0])设置为000000b。
3. 向异步触发器（ADTRG0引脚）输入高电平信号。
4. 将ADCSR.TRGE和ADCSR.EXTRG位设置为1。

图34.29显示了异步触发输入的时序。

在组扫描模式下，无法在组B的AD转换开始触发选择位(ADSTRGR.TRSB[5:0])中选择异步触发。有关设置引脚功能的详细信息，请参见第20节，IO端口。

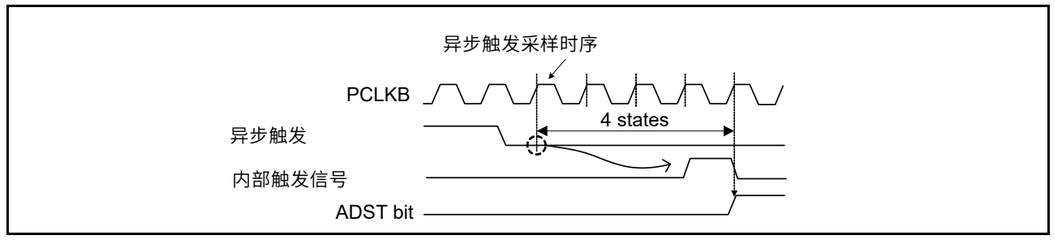


Figure 34.29 异步触发输入时序

34.3.11 Starting A/D Conversion with a Synchronous Trigger from Peripheral Module

The A/D conversion can be started by a synchronous trigger (ELC). To start the A/D conversion by a synchronous trigger:

1. Set the ADCSR.TRGE bit to 1.
2. Set the ADCSR.EXTRG bit to 0.
3. Select the relevant sources in the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

34.4 Interrupt Sources and DTC or DMAC Transfer Requests

34.4.1 Interrupt Requests

The ADC14 can send scan end interrupt requests, ADC140_ADI and ADC140_GBADI, to the CPU. The ADC14 also generates the ADC140_CMPAI and ADC140_CMPBI interrupts to the CPU in response to matches with a comparison condition.

An ADC140_ADI interrupt is always generated. An ADC140_GBADI interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC140_CMPAI and ADC140_CMPBI interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bits to 1.

In addition, the DTC or DMAC can be started when an ADC140_ADI or ADC140_GBADI interrupt is generated. Using these interrupts to activate the DTC or DMAC to read the converted data enables continuous conversion without burdening software.

For details on DTC settings, see section 18, Data Transfer Controller (DTC), and for details on DMAC settings, see section 17, DMA Controller (DMAC).

Table 34.11 describes the interrupt sources and ELC events available for the ADC14.

Table 34.11 ADC14 interrupt sources and ELC events (1 of 2)

Operation							
Scan mode	Double-trigger mode	Compare function window A and window B	Interrupt request or ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
Single scan mode	Deselect	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of single scan
		Select	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of single scan
			ADC140_CMPAI	✓	×	×	ADC140_CMPAI is generated in the match comparison condition of window A
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI is generated in the match comparison condition of window B
			ADC140_WCMPM	×	✓	✓	ADC140_WCMPM is generated in the match conditions of the window A/B compare function
			ADC140_WCMPUM	×	✓	✓	ADC140_WCMPUM is generated in the mismatch conditions of the window A/B compare function
	Select	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of scans in the even-numbered times
Continuous scan mode	Deselect	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of all the selected channels scan
		Select	ADC140_CMPAI	✓	×	×	ADC140_CMPAI is generated in the match comparison condition of window A
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI is generated in the match comparison condition of window B

34.3.11 使用外设模块的同步触发启动AD转换

AD转换可以通过同步触发器(ELC)启动。通过同步触发启动AD转换：

1. 将ADCSR.TRGE位设置为1。
2. 将ADCSR.EXTRG位设置为0。
3. 在ADSTRGR.TRSA[5:0]和ADSTRGR.TRSB[5:0]位中选择相关源。

34.4 中断源和DTC或DMAC传输请求

34.4.1 中断请求

ADC14可以向CPU发送扫描结束中断请求ADC140_ADI和ADC140_GBADI。ADC14还向CPU生成ADC140_CMPAI和ADC140_CMPBI中断，以响应与比较条件的匹配。

始终会产生ADC140_ADI中断。一个ADC140_GBADI中断可以通过设置产生ADCSR.GBADIE位为1。类似地，ADC140_CMPAI和ADC140_CMPBI中断可以通过设置ADCMPCR.CMPAIE和ADCMPCR.CMPBIE位为1。

此外，当产生ADC140_ADI或ADC140_GBADI中断时，可以启动DTC或DMAC。使用这些中断来激活DTC或DMAC来读取转换后的数据，可以在不增加软件负担的情况下实现连续转换。

有关DTC设置的详细信息，请参阅第18节，数据传输控制器(DTC)，有关DMAC设置的详细信息，请参阅第17节，DMA控制器(DMAC)。

表34.11描述了ADC14可用的中断源和ELC事件。

Table 34.11 ADC14中断源和ELC事件(1of2)

Operation							
扫描模式	双触发模式	比较函数窗口A和窗口B	中断请求或ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
单次扫描模式	Deselect	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI在单次扫描结束时生成
		Select	ADC140_ADI	✓	✓	✓	ADC140_ADI在单次扫描结束时生成
			ADC140_CMPAI	✓	×	×	ADC140_CMPAI在窗口A的匹配比较条件下产生
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI在窗口B的匹配比较条件下产生
			ADC140_WCMPM	×	✓	✓	ADC140_WCMPM在窗口AB比较函数的匹配条件下产生
			ADC140_WCMPUM	×	✓	✓	ADC140_WCMPUM在窗口AB比较函数的失配条件下产生
	Select	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI在偶数次扫描结束时生成
连续扫描模式	Deselect	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI在所有选定通道扫描结束时生成
		Select	ADC140_CMPAI	✓	×	×	ADC140_CMPAI在窗口A的匹配比较条件下产生
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI在窗口B的匹配比较条件下产生

Table 34.11 ADC14 interrupt sources and ELC events (2 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
Scan mode	Double-trigger mode	Compare function window A and window B					
Group scan mode	Deselect	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of group A scan
			ADC140_GBADI	✓	✓	×	ADC140_GBADI dedicated to group B is generated at the end of group B scan
		Select	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of group A scan
			ADC140_GBADI	✓	✓	×	ADC140_GBADI dedicated to group B is generated at the end of group B scan
			ADC140_CMPAI	✓	×	×	ADC140_CMPAI is generated in the match comparison condition of window A
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI is generated in the match comparison condition of window B
	Select	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI is generated at the end of group A scans in the even-numbered times
			ADC140_GBADI	✓	✓	×	ADC140_GBADI dedicated to group B is generated at the end of group B scan

✓: available, ×: unavailable.

34.5 Event Link Function

34.5.1 Event Output to the ELC

The ELC uses the ADC140_ADI interrupt request signal as an event signal, enabling link operation for the preset module. The ADC140_GBADI and ADC140_CMPAI/ADC140_CMPBI interrupts cannot be used as event signals. For details, see Table 34.11, ADC14 interrupt sources and ELC events.

34.5.2 ADC14 Operation through an Event from the ELC

The ADC14 can start A/D conversion by the preset event specified in the ELSRn settings of the ELC as follows:

- Select the ELC_AD00 signal in the ELC.ELSR8 register
- Select the ELC_AD01 signal in the ELC.ELSR9 register.

If an ELC_AD00 or ELC_AD01 event occurs during A/D conversion, the event is disabled.

34.6 Selecting Reference Voltage

The ADC14 can select VREFH0 or AVCC0 as the high-potential reference voltage, and VREFL0 or AVSS0 as the internal reference voltage and the low-potential reference voltage. Set these before starting A/D conversion. For details of this setting, see the ADHVREFCNT register description.

34.7 A/D Conversion Procedure when Selecting Internal Reference Voltage as High-Potential Reference Voltage

This section describes the A/D conversion procedure after selecting the internal reference voltage as the high-potential reference voltage. In this case, A/D conversion is possible for channels AN004 to AN006, AN009, AN010, AN017, AN019, and AN020, but A/D conversion of the internal reference voltage and the temperature sensor output is prohibited.

The A/D conversion procedure is as follows:

1. Set ADHVREFCNT.HVSEL[1:0] to 11b to discharge the high-potential reference voltage path in ADC14.
2. Wait for a 1 µs discharge period in software.
3. Set ADHVREFCNT.HVSEL[1:0] to 10b to select internal reference voltage as the high-potential reference voltage.

Note: The ADC14 has a protection function that disables selection of internal reference voltage (ADHVREFCNT.HVSEL[1:0] = 10b) without discharge (ADHVREFCNT.HVSEL[1:0] = 11b) from the selection of VREFH0 (ADHVREFCNT.HVSEL[1:0] = 01b) or AVCC0 (ADHVREFCNT.HVSEL[1:0] = 00b). If the internal reference voltage is selected without discharge, discharge is set forcibly. Select the internal reference voltage

Table 34.11 ADC14中断源和ELC事件(2of2)

Operation			中断请求或 ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
扫描模式	双触发模式	比较函数窗口A和窗口B					
组扫描模式	Deselect	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI在A组扫描结束时生成
			ADC140_GBADI	✓	✓	×	在B组扫描结束时生成B组专用的ADC140_GBADI
		Select	ADC140_ADI	✓	✓	✓	ADC140_ADI在A组扫描结束时生成
			ADC140_GBADI	✓	✓	×	在B组扫描结束时生成B组专用的ADC140_GBADI
			ADC140_CMPAI	✓	×	×	ADC140_CMPAI在窗口A的匹配比较条件下产生
			ADC140_CMPBI	✓	×	×	ADC140_CMPBI在窗口B的匹配比较条件下产生
	Select	Deselect	ADC140_ADI	✓	✓	✓	ADC140_ADI在偶数次A组扫描结束时生成
			ADC140_GBADI	✓	✓	×	在B组扫描结束时生成B组专用的ADC140_GBADI

：可用，×：不可用。

34.5 事件链接功能

34.5.1 事件输出到ELC

ELC使用ADC140_ADI中断请求信号作为事件信号，为预设模块启用链接操作。ADC140_GBADI和ADC140_CMPAIADC140_CMPBI中断不能用作事件信号。有关详细信息，请参见表34.11，ADC14中断源和ELC事件。

34.5.2 ADC14通过来自ELC的事件进行操作

ADC14可以通过ELC的ELSRn设置中指定的预设事件启动AD转换，如下所示：

- 选择ELC.ELSR8寄存器中的ELC_AD00信号
- 选择ELC.ELSR9寄存器中的ELC_AD01信号。

如果在AD转换期间发生ELC_AD00或ELC_AD01事件，则该事件被禁用。

34.6 选择参考电压

ADC14可以选择VREFH0或AVCC0作为高电位参考电压，VREFL0或AVSS0作为内部参考电压和低电位参考电压。在开始AD转换之前设置这些。有关此设置的详细信息，请参见ADHVREFCNT寄存器说明。

34.7 选择内部参考电压为高时的AD转换过程 潜在参考电压

本节介绍选择内部参考电压作为高电位参考电压后的AD转换过程。在这种情况下，通道AN004至AN006、AN009、AN010、AN017、AN019和AN020可以进行AD转换，但禁止内部参考电压和温度传感器输出的AD转换。

AD转换过程如下：

1. 将ADHVREFCNT.HVSEL[1:0]设置为11b，以对ADC14中的高电位参考电压路径进行放电。
2. 在软件中等待1µs的放电周期。
3. 将ADHVREFCNT.HVSEL[1:0]设置为10b以选择内部参考电压作为高电位参考电压。

Note: ADC14有一个保护功能，它禁止通过选择VREFH0(ADHVREFCNT.HVSEL[1:0]=01b)或AVCC0(ADHVREFCNT.HVSEL[1:0]=00b)。如果选择内部参考电压而不放电，则强制设置放电。选择内部参考电压

again after 1 µs.

4. Wait until the internal reference voltage is stabilized (for 5 µs) in software, and then perform A/D conversion.

Figure 34.30 shows a waveform for the procedure to select internal reference voltage as the high-potential reference voltage.

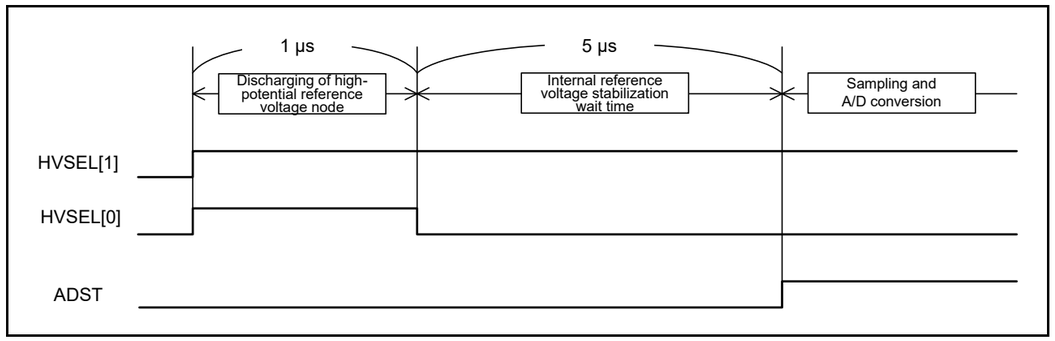


Figure 34.30 Procedure to select internal reference voltage as the high-potential reference voltage

34.8 Usage Notes

34.8.1 Notes on Reading Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register.

If a register is read twice in byte units, that is, the upper byte and lower byte are separately read, the A/D-converted value initially read might conflict with the subsequent A/D-converted value read. To prevent this, do not read the data registers in byte units.

34.8.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure in Figure 34.31.

1微秒后再次。

4. 等待内部参考电压在软件中稳定（5µs），然后执行AD转换。

图34.30显示了选择内部参考电压作为高电位参考电压的过程的波形。

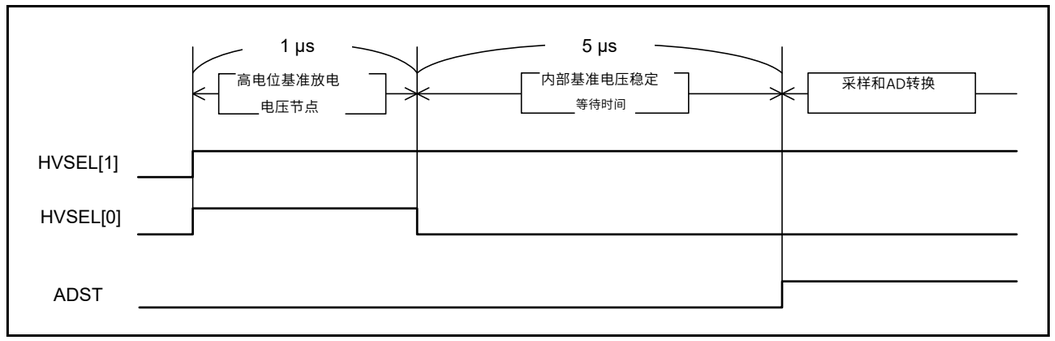


Figure 34.30 选择内部参考电压作为高电位参考电压的步骤

34.8 使用说明

34.8.1 读取数据寄存器的注意事项

以下寄存器必须以半字为单位读取：

- AD数据寄存器
- AD数据双工寄存器A
- AD数据双工寄存器B
- AD温度传感器数据寄存器
- AD内部参考电压寄存器
- AD自诊断数据寄存器。

如果以字节为单位读取寄存器两次，即分别读取高字节和低字节，则最初读取的AD转换值可能与后续读取的AD转换值冲突。为防止这种情况，请勿以字节为单位读取数据寄存器。

34.8.2 停止AD转换的注意事项

选择异步触发或同步触发作为启动条件时停止AD转换
AD转换，请按照图34.31中的程序进行。

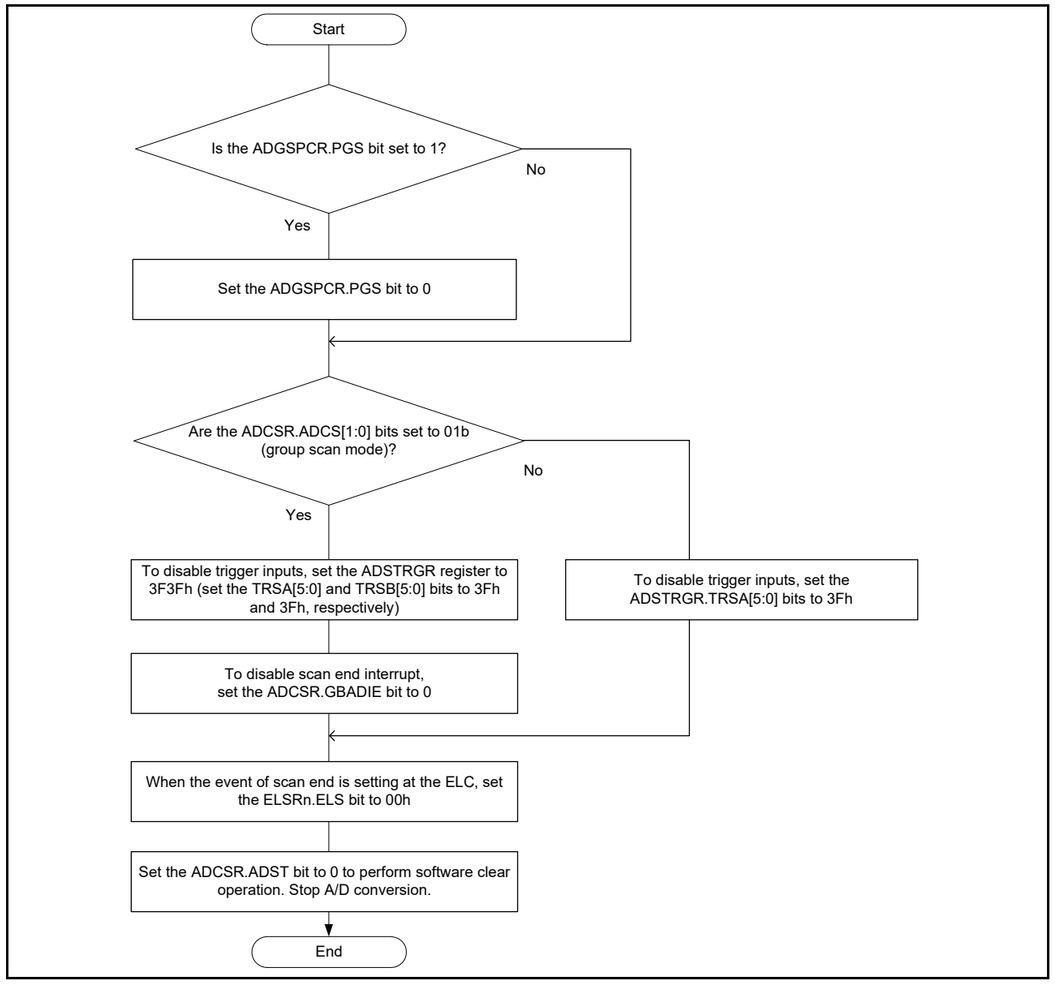


Figure 34.31 Procedure for clearing the ADCSR.ADST bit through software

34.8.3 A/D Conversion Restarting Timing and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit in the ADC14 to restart on setting the ADCSR.ADST bit to 1. A maximum of 3 ADCLK cycles is required for the operating analog unit in the ADC14 to terminate on setting the ADCSR.ADST bit to 0.

34.8.4 Restrictions on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data. This occurs when the CPU does not complete the reading of the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

34.8.5 Settings for the Module-Stop State

The Module Stop Control Register can enable or disable the ADC14 operation. The ADC14 is initially stopped after a reset. Releasing the module-stop state enables access to the registers. After release from the module-stop state, wait for at least 1 µs before starting A/D conversion. For details, see section 11, Low Power Modes.

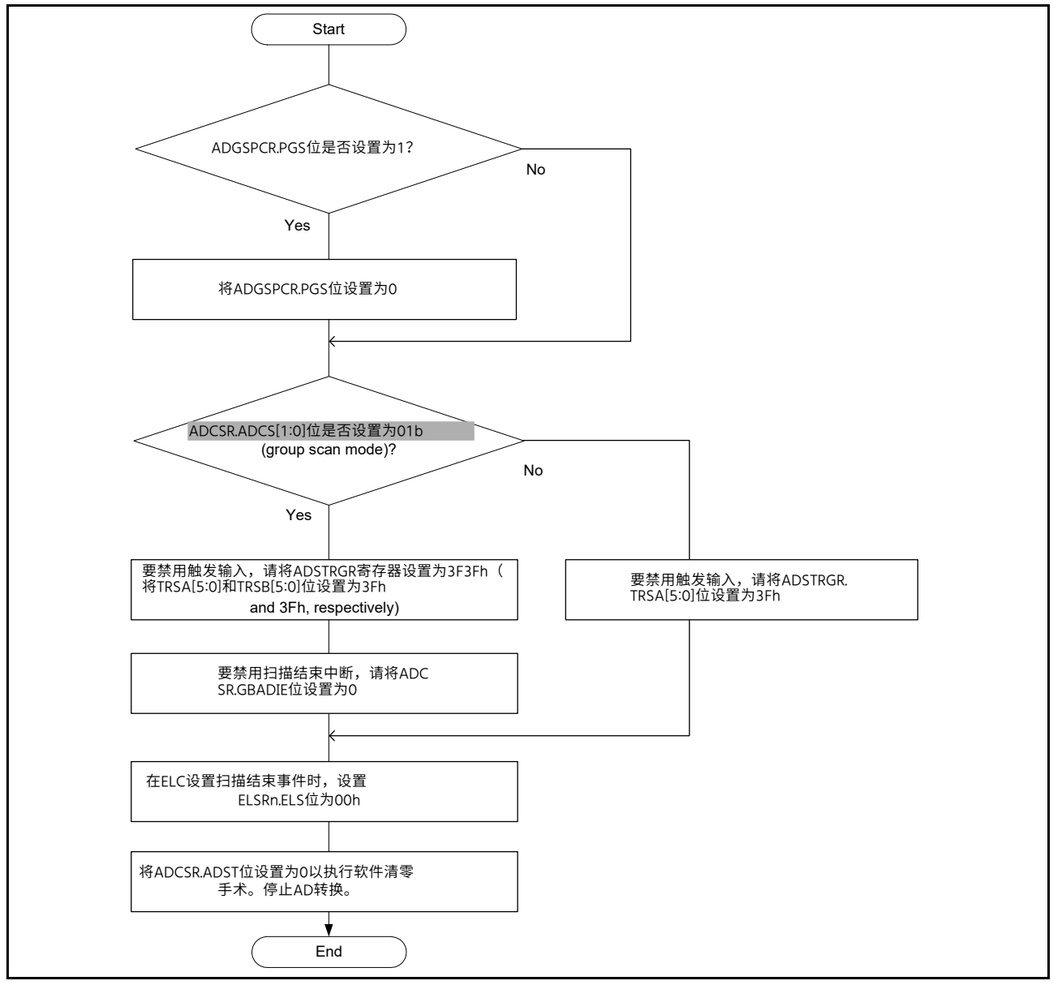


Figure 34.31 通过软件清除ADCSR.ADST位的过程

34.8.3 AD转换重启时序和终止时序

ADC14中的空闲模拟单元最多需要6个ADCLK周期才能在设置
ADCSR.ADST位为1。ADC14中的操作模拟单元最多需要3个ADCLK周期才能在将ADCSR.ADST位设置为0时终止。

34.8.4 扫描结束中断处理的限制

当使用任何触发器扫描相同的模拟输入两次时，第一个AD转换数据将被第二个AD转换数据覆盖。当CPU在

在产生第一次扫描结束中断后，第二次扫描的第一个模拟输入的D转换结束。

34.8.5 模块停止状态的设置

模块停止控制寄存器可以启用或禁用ADC14操作。ADC14在复位后最初停止。释放模块停止状态可以访问寄存器。从模块停止状态释放后，在开始AD转换之前至少等待1微秒。有关详细信息，请参阅第11节，低功耗模式。

34.8.6 Restrictions on Entering Low Power States

Before entering the module-stop state or Software Standby mode, be sure to stop A/D conversion. Set the ADCSR.ADST bit to 0 and secure a period of time until the analog unit of the ADC14 stops. Follow the procedure shown in Figure 34.31 to clear the ADCSR.ADST bit through software. Then, wait for 3 clock cycles of ADCLK before entering the module-stop state or Software Standby mode.

34.8.7 Error in Absolute Accuracy when Disconnection Detection Assistance is in Use

Using the disconnection detection assistance function leads to an error in absolute accuracy of the ADC14. This error arises because an erroneous voltage is input to the analog input pins because of the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated using the following formula.

Maximum error in absolute accuracy (LSB) = 4095 × Rs / (Rs + Rp)

Only use disconnection detection assistance after thorough evaluation.

34.8.8 ADHSC Bit Rewriting Procedure

Before changing the A/D Conversion Select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the ADC14 must be in the standby state. Use the following procedure to modify the ADCSR.ADHSC bit. After clearing the Sleep bit (ADHVREFCNT.ADSLP) to 0, wait for at least 1 µs and then start A/D conversion.

The procedure to modify the ADCSR.ADHSC bit is as follows:

1. Set the Sleep bit (ADHVREFCNT.ADSLP) to 1.
2. Wait for at least 0.2 µs, and then modify the A/D Conversion Select bit (ADCSR.ADHSC).
3. Wait for at least 4.8 µs, and then set the Sleep bit (ADHVREFCNT.ADSLP) to 0.

Note: Setting the Sleep bit (ADHVREFCNT.ADSLP) to 1 is prohibited except when modifying the A/D Conversion Select bit (ADCSR.ADHSC).

Note: Do not reset the Sleep bit when the A/D Conversion Select bit (ADCSR.ADHSC) is 1. After this bit is set to 0 or the operating mode transitions to module-stop mode, reset the Sleep bit based on the ADCSR.ADHSC bit rewriting procedure.

34.8.9 Notes on Operating Modes and Status Bits

Initialize or set again individually, if necessary, the voltage values in self-diagnosis, the determination of the first scan or second scan in double trigger mode, the data buffer pointer, and status monitor in the compare function.

- Select the voltage values in self-diagnosis (ADCER.DIAGVAL[1:0]) after setting ADCER.DIAGLD to 1
- Double trigger mode operates as the first scan after setting ADCSR.DBLE to 1 from 0
- The status monitor bits (MONCMPA, MONCMPB, MONCOMB) in the compare function are initialized after the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits are set to 0.

34.8.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or be placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog input pins (AN004 to AN006, AN009, AN010, AN017, AN019, and AN020), reference power supply pin (VREFH0), reference ground pin (VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

34.8.11 Notes on Noise Reduction

To prevent the analog input pins (AN004 to AN006, AN009, AN010, AN017, AN019, and AN020) from being destroyed by abnormal voltage such as excessive surges, insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0. Additionally, connect a protection circuit to protect the analog input pins (AN004 to AN006, AN009, AN010, AN017, AN019, and AN020) as shown in Figure 34.32.

34.8.6 进入低功耗状态的限制

在进入模块停止状态或软件待机模式之前，请务必停止AD转换。将ADCSR.ADST位设置为0并确保一段时间，直到ADC14的模拟单元停止。按照图34.31所示的过程通过软件清除ADCSR.ADST位。然后，等待ADCLK的3个时钟周期后进入模块停止状态或软件待机模式。

34.8.7 使用断线检测辅助时的绝对精度误差

使用断线检测辅助功能会导致ADC14的绝对精度出现误差。由于上拉或下拉电阻(Rp)与信号源电阻(Rs)之间的电阻分压，导致错误电压输入到模拟输入引脚，因此会出现此错误。使用以下公式计算此绝对精度误差。

绝对精度的最大误差(LSB)=4095　Rs(Rs+Rp)

仅在全面评估后使用断线检测辅助。

34.8.8 ADHSC位重写程序

在将AD转换选择位(ADCSR.ADHSC)从0更改为1或从1更改为0之前，ADC14必须处于待机状态。使用以下过程修改ADCSR.ADHSC位。将休眠位(ADHVREFCNT.ADSLP)清0后，等待至少1μs，然后开始AD转换。

修改ADCSR.ADHSC位的过程如下：

1. 将休眠位(ADHVREFCNT.ADSLP)设置为1。
2. 等待至少0.2µs，然后修改AD转换选择位(ADCSR.ADHSC)。
3. 等待至少4.8µs，然后将休眠位(ADHVREFCNT.ADSLP)设置为0。

Note: 禁止将休眠位(ADHVREFCNT.ADSLP)设置为1，除非在修改AD转换时选择位(ADCSR.ADHSC)。

Note: 当AD转换选择位(ADCSR.ADHSC)为1时，请勿复位休眠位。该位设置为0或工作模式转换为模块停止模式后，根据ADCSR.ADHSC位重写复位休眠位程序。

34.8.9 操作模式和状态位注意事项

必要时单独初始化或重新设置自诊断中的电压值、双触发模式下第一次扫描或第二次扫描的确定、数据缓冲区指针和比较功能中的状态监视器。

- 设置ADCER.DIAGLD为1后，选择自诊断中的电压值（ADCER.DIAGVAL[1:0]）
- 双触发模式在将ADCSR.DBLE从0设置为1后作为第一次扫描运行
- 比较功能中的状态监控位（MONCMPA、MONCMPB、MONCOMB）在ADCMPCR.CMPAE和ADCMPCR.CMPBE位设置为0。

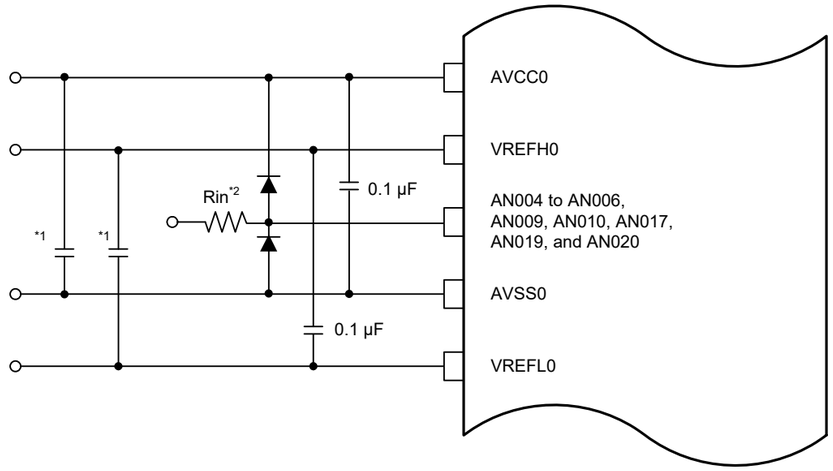
34.8.10 电路板设计注意事项

电路板的设计应使数字电路和模拟电路尽可能分开。此外，数字电路信号线和模拟电路信号线不应交叉或靠近。如果不遵守这些规则，模拟信号上可能会出现噪声，影响AD转换精度。模拟输入引脚（AN004至AN006、AN009、AN010、AN017、AN019和AN020）、参考电源引脚(VREFH0)、参考接地引脚(VREFL0)和模拟电源(AVCC0)应与数字电路分开使用模拟地（AVSS0）。模拟接地(AVSS0)应连接到板上的稳定数字接地(VSS)（单点接地层连接）。

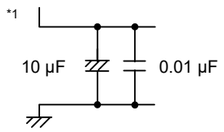
34.8.11 降噪注意事项

为防止模拟输入引脚（AN004至AN006、AN009、AN010、AN017、AN019和AN020）被异常电压（如过大浪涌）损坏，请在AVCC0和AVSS0之间以及VREFH0和VREFL0之间插入一个电容器。此外，连接保护电路以保护模拟输入引脚（AN004至AN006，

AN009、AN010、AN017、AN019和AN020）如图34.32所示。



Note 1. The values shown here are reference values.



Note 2. Rin: Signal source impedance.

Figure 34.32 Example protection circuit for analog inputs

34.8.12 Port Settings when Using the 14-bit A/D Converter Input

When using the high precision channels, do not use PORT0 as general I/O, IRQ2, IRQ3 inputs, and TS transmission. Renesas recommends that you do not use the digital output that is also used as the A/D analog input, if normal precision channels are used. If the digital output that is also used as the A/D analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

34.8.13 Relationship between the ADC14, OPAMP, and ACMPLP

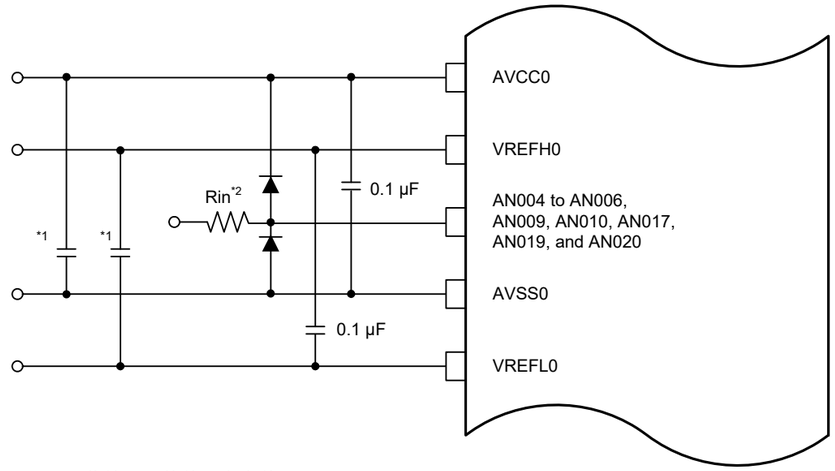
Table 34.12 lists the A/D conversion targets that should not be selected as an OPAMP and ACMPLP input during A/D conversion.

Table 34.12 OPAMP and ACMPLP pins that should not be selected during A/D conversion

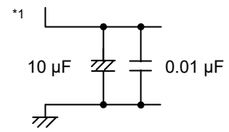
Target of 14-bit A/D conversion	OPAMP	ACMPLP
AN005	AMP2-	-
AN006	AMP2+	-
AN017	-	CMPIN1
AN019	-	CMPREF1
AN020	-	CMPIN1

34.8.14 Notes on Canceling Software Standby Mode

After transitioning from Software Standby mode to Normal mode, wait for 1 µs before starting A/D conversion.



Note 1. 此处显示的值是参考值。



Note 2. Rin：信号源阻抗。

Figure 34.32 模拟输入保护电路示例

34.8.12 使用14位AD转换器输入时的端口设置

使用高精度通道时，请勿将PORT0用作通用IO、IRQ2、IRQ3输入和TS传输。
如果使用普通精密通道，瑞萨建议您不要使用同时用作AD模拟输入的数字输出。如果将同时用作AD模拟输入的数字输出用于输出信号，则进行几次AD转换，消除最大值和最小值，取其他结果的平均值。

34.8.13 ADC14、OPAMP和ACMPLP之间的关系

表34.12列出了在AD转换期间不应选择作为OPAMP和ACMPLP输入的AD转换目标。

Table 34.12 在AD转换期间不应选择的OPAMP和ACMPLP引脚

14位AD转换的目标	OPAMP	ACMPLP
AN005	AMP2-	-
AN006	AMP2+	-
AN017	-	CMPIN1
AN019	-	CMPREF1
AN020	-	CMPIN1

34.8.14 关于取消软件待机模式的注意事项

从软件待机模式转换到正常模式后，等待1µs再开始AD转换。

35. 12-Bit D/A Converter (DAC12)

35.1 Overview

The MCU provides a 12-bit D/A Converter (DAC12).

Table 35.1 lists the DAC12 specifications, Figure 35.1 shows the block diagram, and Table 35.2 lists the I/O pins.

Table 35.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
Output channels	1 channel
Interference reduction between analog modules	Reduces interference between D/A and A/D conversion circuits. D/A-converted data update timing is controlled by the synchronous D/A conversion enable input signal from the ADC14, which reduces the effect of DAC12 inrush current on A/D conversion accuracy.
Module-stop function	The module-stop state can be set to reduce power consumption
Event link function (input)	DA0 conversion can be started on input of an event signal

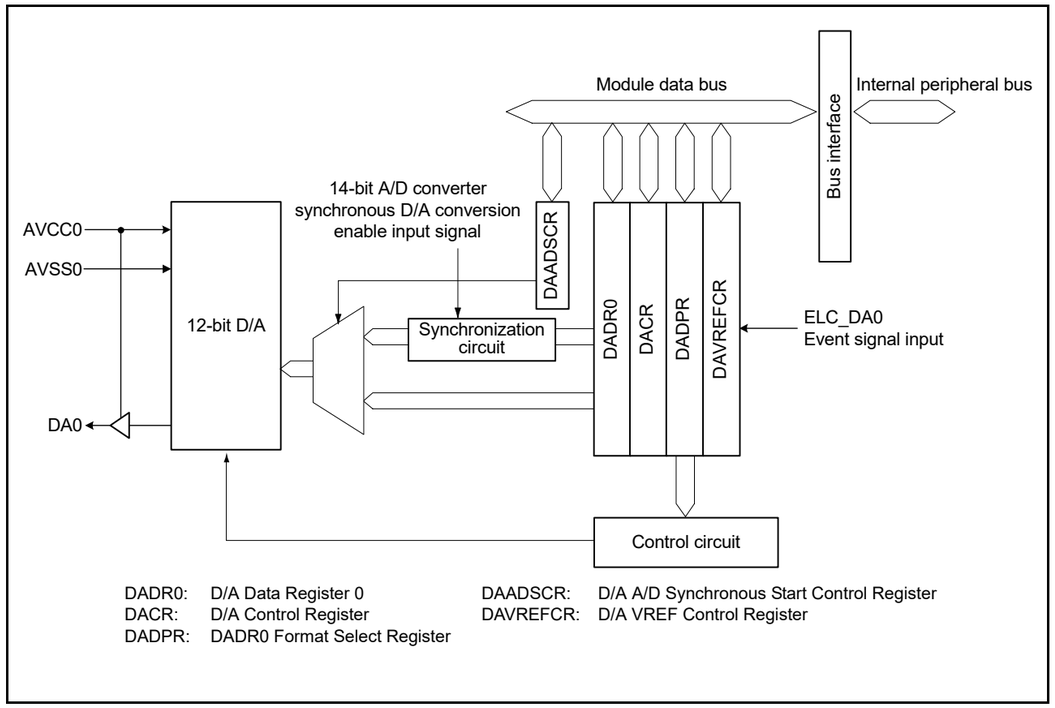


Figure 35.1 DAC12 block diagram

Table 35.2 DAC12 pin configuration (1 of 2)

Pin name	I/O	Function
AVCC0	Input	Analog power supply pin for ADC14, DAC12, comparator, and OPAMP. Connect to VCC when these modules are not used.
AVSS0	Input	Analog ground pin for ADC14, DAC12, comparator, and OPAMP. Connect to VSS when these modules are not used.

35. 12-Bit D/A Converter (DAC12)

35.1 Overview

MCU提供一个12位DA转换器(DAC12)。

表35.1列出了DAC12规格，图35.1显示了框图，表35.2列出了IO引脚。

Table 35.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
输出通道	1 channel
减少模拟模块之间的干扰	减少DA和AD转换电路之间的干扰。 DA转换数据更新时序由来自ADC14的同步DA转换使能输入信号控制，从而降低了DAC12浪涌电流对AD转换精度的影响。
Module-stop function	可设置模块停止状态以降低功耗
事件链接功能（输入）	DA0转换可以在输入事件信号时启动

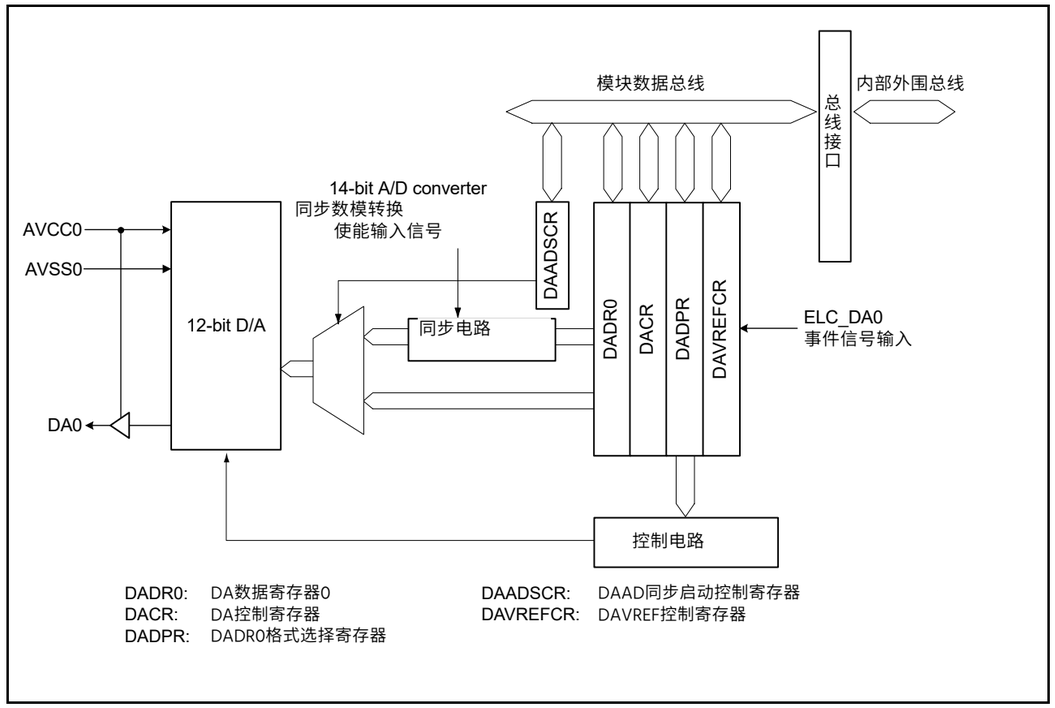


Figure 35.1 DAC12框图

Table 35.2 DAC12引脚配置（2个中的1个）

引脚名称	I/O	Function
AVCC0	Input	ADC14、DAC12、比较器和运算放大器的模拟电源引脚。 不使用这些模块时连接到VCC。
AVSS0	Input	ADC14、DAC12、比较器和OPAMP的模拟接地引脚。 不使用这些模块时连接到VSS。

Table 35.2 DAC12 pin configuration (2 of 2)

Pin name	I/O	Function
DA0	Output	Channel 0 analog output pin

35.2 Register Descriptions

35.2.1 D/A Data Register 0 (DADR0)

Address(es): DAC12.DADR0 4005 E000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DADR0 register is a 16-bit read/write register that stores data for D/A conversion. When an analog output is enabled, the values in DADR0 are converted and output to the analog output pins.

The 12-bit data can be formatted as left- or right-justified by setting the DADPR.DPSEL bit. In right-justified format (DADPR.DPSEL = 0), the lower 12 bits, [11:0], are valid. In left-justified format (DADPR.DPSEL = 1), the upper 12 bits, [15:4], are valid.

35.2.2 D/A Control Register (DACR)

Address(es): DAC12.DACR 4005 E004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DAOE0	—	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	DAOE0	D/A Output Enable 0	0: Disable analog output of channel 0 (DA0) 1: Enable D/A conversion of channel 0 (DA0).	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Only set this register while the ADC14 is halted when the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversions is enabled). Only set DACR while the ADCSR.ADST bit is 0, and after selecting the software trigger as the ADC14 trigger to securely stop the ADC14.

DAOE0 bit (D/A Output Enable 0)

The DAOE0 bit controls D/A conversion and analog output.

When interference reduction between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), only set the DAOE0 bit while the ADC14 is halted (ADCSR.ADST = 0), and the software trigger is selected as the ADC14 trigger to securely stop the ADC14.

The event link function can be used to set the DAOE0 bit to 1. The DAOE0 bit becomes 1 when the event specified in the ELSR12 register for the ELC_DA0 event occurs, and output of the D/A conversion results starts.

Table 35.2 DAC12引脚配置（2个中的2个）

引脚名称	I/O	Function
DA0	Output	通道0模拟输出引脚

35.2 注册说明

35.2.1 DA数据寄存器0(DADR0)

Address(es): DAC12.DADR0 4005 E000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADR0寄存器是一个16位读写寄存器，用于存储用于DA转换的数据。当模拟输出使能时，DADR0中的值被转换并输出到模拟输出引脚。

通过设置DADPR.DPSEL位，可以将12位数据格式化为左对齐或右对齐。在右对齐格式(DADPR.DPSEL=0)中，低12位[11:0]有效。在左对齐格式(DADPR.DPSEL=1)中，高12位[15:4]有效。

35.2.2 DA控制寄存器(DACR)

Address(es): DAC12.DACR 4005 E004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DAOE0	—	—	—	—	—	—
重置后的值：	0	0	0	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	DAOE0	DA输出使能0	0：禁用通道0（DA0）的模拟输出1：启用通道0（DA0）的DA转换。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

仅当DAADSCR.DAADST位为1（启用DA和AD转换之间的干扰减少）时ADC14停止时设置该寄存器。仅在ADCSR.ADST位为0时设置DACR，并在选择软件触发作为ADC14触发后才能安全地停止ADC14。

DAOE0位（DA输出使能0）

DAOE0位控制DA转换和模拟输出。

当启用DA和AD转换之间的干扰降低(DAADSCR.DAADST=1)时，只需设置当ADC14停止时（ADCSR.ADST=0），DAOE0位，选择软件触发作为ADC14触发以安全停止ADC14。

事件链接功能可用于将DAOE0位设置为1。当在发生ELC_DA0事件的ELSR12寄存器，并开始输出DA转换结果。

35.2.3 DADR0 Format Select Register (DADPR)

Address(es): DAC12.DADPR 4005 E005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSEL	DADR0 Format Select	0: Right-justified format 1: Left-justified format.	R/W

35.2.4 D/A A/D Synchronous Start Control Register (DAADSCR)

Address(es): DAC12.DAADSCR 4005 E006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0: Do not synchronize DAC12 operation with ADC14 operation (disable interference reduction between D/A and A/D conversion) 1: Synchronize DAC12 operation with ADC14 operation (enable interference reduction between D/A and A/D conversion).	R/W

To reduce interference between the D/A and A/D conversion, the DAADSCR register switches on or off the synchronization of the D/A conversion with the synchronous D/A conversion enable input signal from the ADC14 trigger.

Only set this register while the ADC14 is halted (ADCSR.ADST = 0) and the software trigger is selected as the ADC14 trigger.

Select unit 1 as the target ADC14 unit before setting the DAADST bit to 1.

DAADST bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADR0 register value to be converted into analog data at any time. Setting the DAADST bit to 1 allows synchronous D/A conversion with the synchronous D/A conversion enable input signal from ADC14. When the DADR0 register value is modified, D/A conversion does not start until the ADC14 completes A/D conversion.

Set this bit only while the ADC14 is halted (ADCSR.ADST bit is set to 0) and the software trigger is selected as the ADC14 trigger to securely stop the ADC14. The event link function cannot be used when the DAADST bit is set to 1. Stop the event link function by setting the ELSR12 register of the ELC. The setting of the DAADST bit is shared by channels 0 and 1 of the DAC12.

35.2.3 DADR0格式选择寄存器(DADPR)

Address(es): DAC12.DADPR 4005 E005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	DPSEL	DADR0格式选择	0: Right-justified format 1: Left-justified format.	R/W

35.2.4 DAAD同步启动控制寄存器(DAADSCR)

Address(es): DAC12.DAADSCR 4005 E006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0：DAC12操作不与ADC14操作同步（禁用DA和AD转换之间的干扰降低）1：DAC12操作与ADC14操作同步（启用DA和AD转换之间的干扰降低）。	R/W

为了减少DA和AD转换之间的干扰，DAADSCR寄存器打开或关闭DA转换与来自ADC14触发器的同步DA转换使能输入信号的同步。

仅在ADC14停止(ADCSR.ADST=0)并且选择软件触发作为ADC14触发时设置该寄存器。

在将DAADST位设置为1之前，选择单元1作为目标ADC14单元。

DAADST位（DAAD同步转换）

将DAADST位设置为0可以随时将DADR0寄存器值转换为模拟数据。将DAADST位设置为1允许使用来自ADC14的同步DA转换使能输入信号进行同步DA转换。修改DADR0寄存器值时，直到ADC14完成AD转换后才开始DA转换。

仅当ADC14停止（ADCSR.ADST位设置为0）并且选择软件触发作为ADC14触发以安全停止ADC14时设置该位。当DAADST位设置为1时，不能使用事件链接功能。
通过设置ELC的ELSR12寄存器来停止事件链接功能。DAADST位的设置由DAC12的通道0和1共享。

35.2.5 D/A VREF Control Register (DAVREFCR)

Address(es): DAC12.DAVREFCR 4005 E007h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	REF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	REF[2:0]	D/A Reference Voltage Select	b2 b0 0 0 0: No reference voltage selected 0 0 1: AVCC0/AVSS0 selected 0 1 1: Internal reference voltage/AVSS0 selected Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The D/A VREF Control Register (DAVREFCR) selects the reference voltage of the DAC12.

REF[2:0] bits (D/A Reference Voltage Select)

The REF[2:0] bits select the reference voltage of the DAC12. When changing the value of these bits, write 000b to these bits in advance. Read the REF[2:0] bits after changing their value, and confirm that they are changed. When selecting the internal reference voltage, set the DADR0 register to 0000h and discharge the VREF path before switching the voltage. As the path remains discharged after the reset is released, the internal reference voltage can be selected. For details on discharging, see section 35.3.2, Notes on Using the Internal Reference Voltage as the Reference Voltage. Do not rewrite this register during A/D conversion using the ADC14. If this register is rewritten, the accuracy of A/D conversion is not guaranteed. When the internal reference voltage is selected, the voltage generation circuit operates and current increases. This circuit does not automatically turn off even when the MCU enters Software Standby mode with the internal reference voltage selected.

35.3 Operation

When the DAOE0 bit in the DACR register is set to 1, the DAC12 is enabled and the conversion result is output.

The following example shows D/A conversion on channel 0. Figure 35.2 shows the timing of this operation.

1. Set the data for D/A conversion in the DADPR.DPSEL bit and the DADR0 register.
2. Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time tDCONV elapses. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is set to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Setting value of DADR0}}{4096} \times \text{Reference voltage}$$

3. To start another conversion, write another value to DADR0. The conversion result is output after the conversion time tDCONV elapses.
   When the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled), a maximum of one A/D conversion time is required for D/A conversion to start. When ADCLK is faster than the peripheral clock, a longer time than one A/D conversion time might be required.
4. To disable analog input, set the DAOE0 bit to 0.

35.2.5 DAVREF控制寄存器(DAVREFCR)

Address(es): DAC12.DAVREFCR 4005 E007h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	REF[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	REF[2:0]	DA参考电压 Select	b2b0000：未选择参考电压001：选择AVCC0AVSS 0011：选择内部参考电压AVSS0禁止其他设置。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DAVREF控制寄存器(DAVREFCR)选择DAC12的参考电压。

REF[2:0]位（DA参考电压选择）

REF[2:0]位选择DAC12的参考电压。更改这些位的值时，请预先将000b写入这些位。更改值后读取REF[2:0]位，并确认它们已更改。选择内部参考电压时，将DADR0寄存器设置为0000h，并在切换电压之前对VREF路径进行放电。由于复位释放后路径保持放电状态，因此可以选择内部参考电压。有关放电的详细信息，请参见第35.3.2节"使用内部参考电压作为参考电压的注意事项"。请勿在使用ADC14进行AD转换期间重写此寄存器。如果重写此寄存器，则无法保证AD转换的准确性。Whentheinternalreferencevoltageisselected thevoltagegeneratio ncircuitoperatesandcurrentincreases.即使MCU进入软件待机模式并选择内部参考电压，该电路也不会自动关闭。

35.3 Operation

当DACR寄存器中的DAOE0位设置为1时，DAC12使能并输出转换结果。

以下示例显示通道0上的DA转换。图35.2显示了此操作的时序。

1. 在DADPR.DPSEL位和DADR0寄存器中设置用于DA转换的数据。
2. 将DACR.DAOE0位设置为1以启动DA转换。转换结果从模拟输出引脚输出
   转换时间tDCONV过后的DA0。转换结果继续输出，直到再次写入DADR0或将DAOE0位设置为0。输出值（参考值）由以下公式表示：

$$\frac{\text{DADR0设定值}}{4096} \times \text{参考电压}$$

3. 要开始另一次转换，请将另一个值写入DADR0。经过转换时间tDCONV后输出转换结果。当DAADSCR.DAADST位为1时（启用DA和AD转换之间的干扰降低），最多需要一个AD转换时间才能启动DA转换。当ADCLK比外设时钟快时，可能需要比一次AD转换时间更长的时间。
4. 要禁用模拟输入，请将DAOE0位设置为0。

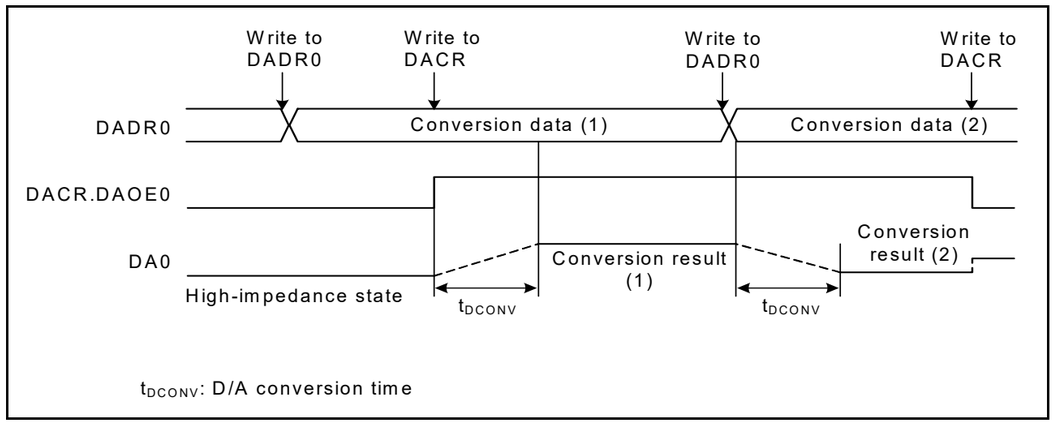


Figure 35.2 Example DAC12 operation

35.3.1 Reducing Interference between D/A and A/D Conversion

When D/A conversion starts, the DAC12 generates inrush current. Because the DAC12 and ADC14 share the same analog power supply, the generated inrush current can interfere with ADC14 operation.

While the DAADSCR.DAADST bit is 1, D/A conversion does not start immediately on updating the DADR0 register. Instead:

- If the DADR0 register data is modified while the ADC14 is halted, D/A conversion starts in 1 PCLKB cycle
- If the DADR0 register data is modified when the ADC14 is in progress, D/A conversion starts on A/D conversion completion. Therefore, it takes up to one A/D conversion time period for the DADR0 register data update to reflect as the D/A conversion circuit output. Until the D/A conversion completes, the DADR0 register value does not correspond to the analog output value.

When the DAADSCR.DAADST bit is 1, it is not possible to check through any software means whether the DADR0 register value was D/A-converted.

The following sequence provides an example of D/A conversion, in which the DAC12 is synchronized with the ADC14. Figure 35.3 shows the timing of this operation.

To perform D/A conversion in synchronization with the ADC14:

1. Confirm that the ADC14 is halted and set the DAADSCR.DAADST bit to 1.
2. Confirm that the ADC14 is halted and set the DACR.DAOE0 bit to 1.
3. Set the DADR0 register. If ADCLK is faster than the peripheral clock, D/A conversion might be delayed for longer than one A/D conversion time.

- If the ADC14 is halted (ADCSR.ADST bit = 0) when the DADR0 register is modified, D/A conversion starts in 1 PCLKB cycle.
- If the ADC14 is in progress (ADCSR.ADST bit = 1) when the DADR0 register is modified, D/A conversion starts on A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update might not be converted.

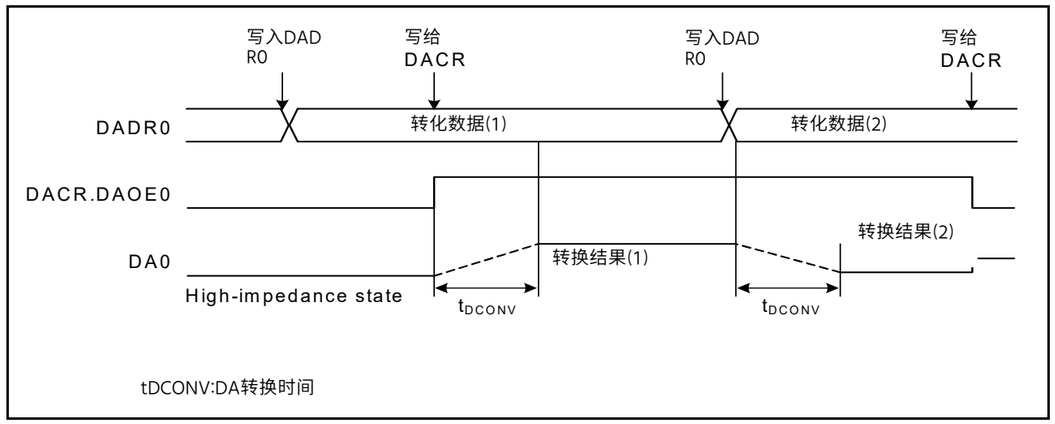


Figure 35.2 DAC12操作示例

35.3.1 减少DA和AD转换之间的干扰

当DA转换开始时，DAC12会产生浪涌电流。由于DAC12和ADC14共用同一个模拟电源，产生的浪涌电流会干扰ADC14的运行。

当DAADSCR.DAADST位为1时，DA转换不会在更新DADR0寄存器时立即开始。
Instead:

- 如果在ADC14停止时修改了DADR0寄存器数据，则DA转换在1个PCLKB周期内开始
- 如果在ADC14正在进行时修改了DADR0寄存器数据，则DA转换在AD转换完成时开始。因此，DADR0寄存器数据更新最多需要一个AD转换时间周期才能反映为DA转换电路输出。在DA转换完成之前，DADR0寄存器的值与模拟输出值不对应。

当DAADSCR.DAADST位为1时，无法通过任何软件方式检查DADR0寄存器值是否经过DA转换。

以下序列提供了一个DA转换示例，其中DAC12与ADC14同步。
图35.3显示了该操作的时序。

要与ADC14同步执行DA转换：

1. 确认ADC14已停止并将DAADSCR.DAADST位设置为1。
2. 确认ADC14已停止并将DACR.DAOE0位设置为1。
3. 设置DADR0寄存器。如果ADCLK比外设时钟快，则DA转换可能会延迟超过一次AD转换时间。

- 如果在修改DADR0寄存器时ADC14停止（ADCSR.ADST位=0），则DA转换从1开始
PCLKB cycle.
- 如果修改DADR0寄存器时ADC14正在进行（ADCSR.ADST位=1），则DA转换在AD转换完成时开始。如果在AD转换期间DADR0寄存器被修改两次，第一次更新可能不会被转换。

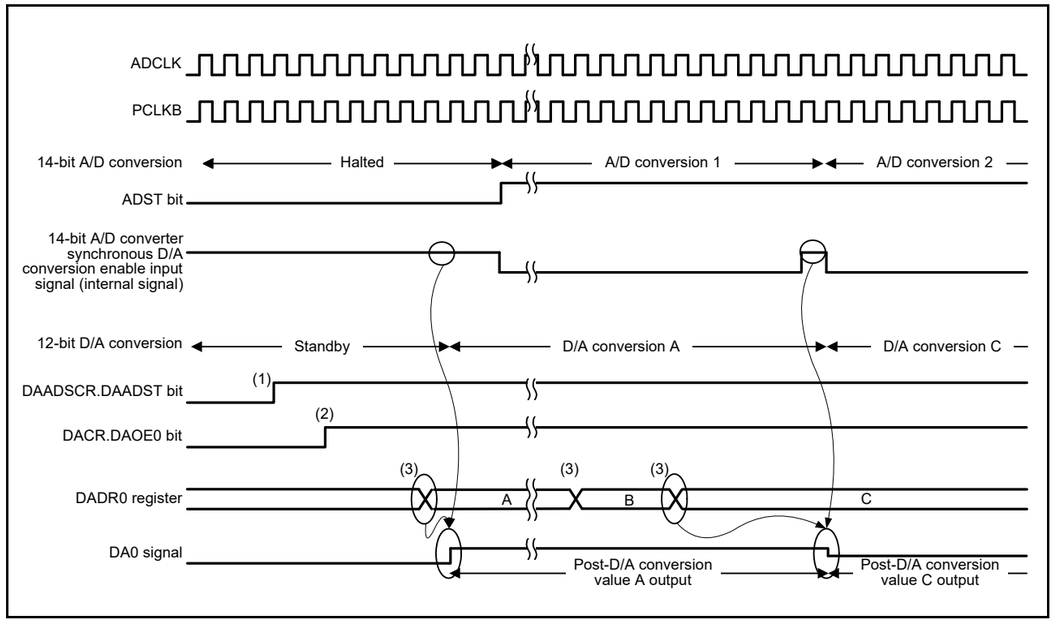


Figure 35.3 Example of conversion when DAC12 is synchronized with ADC14

When ADCLK is faster than PCLKB, the DAC12 might not be able to capture the synchronous D/A conversion enable input signal from the ADC14 during the 1 ADCLK output cycle between A/D conversion 1 and A/D conversion 2, as shown in Figure 35.4. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

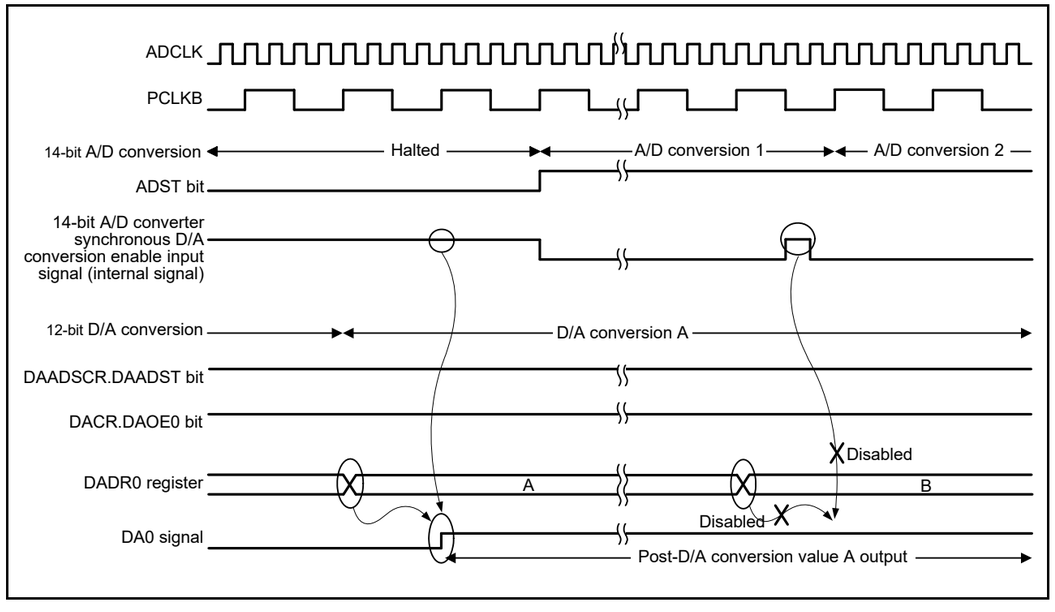


Figure 35.4 Example when DAC12 cannot capture ADC14 synchronous D/A conversion enable input signal

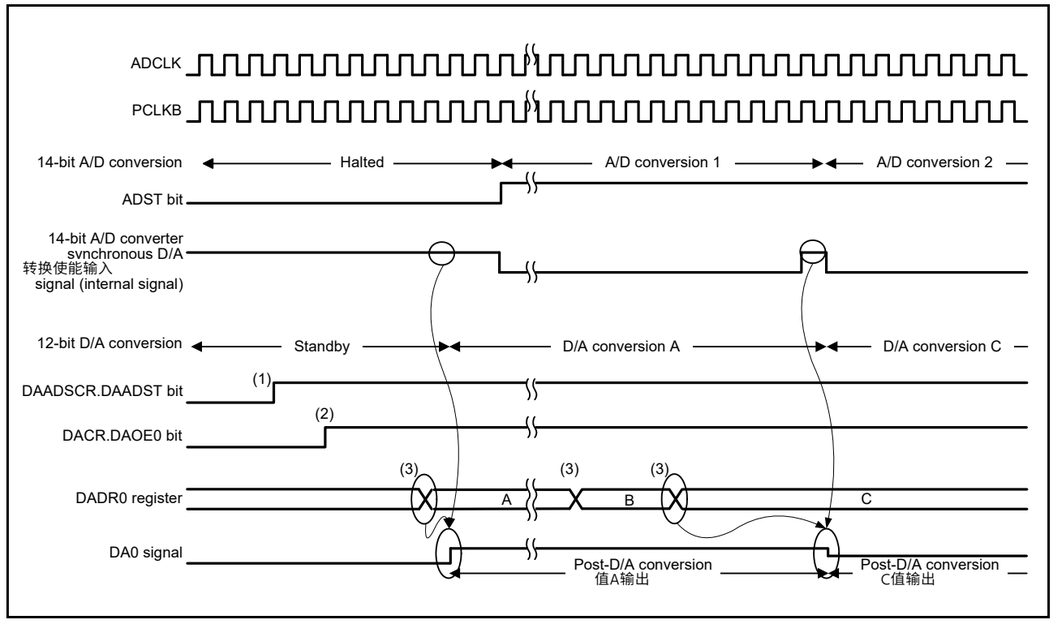


Figure 35.3 DAC12与ADC14同步时的转换示例

当ADCLK快于PCLKB时，DAC12可能无法在AD转换1和AD转换2之间的1个ADCLK输出周期内捕获来自ADC14的同步DA转换使能输入信号，如图35.4所示。在这种情况下，后DA转换值A作为DA0信号连续输出。

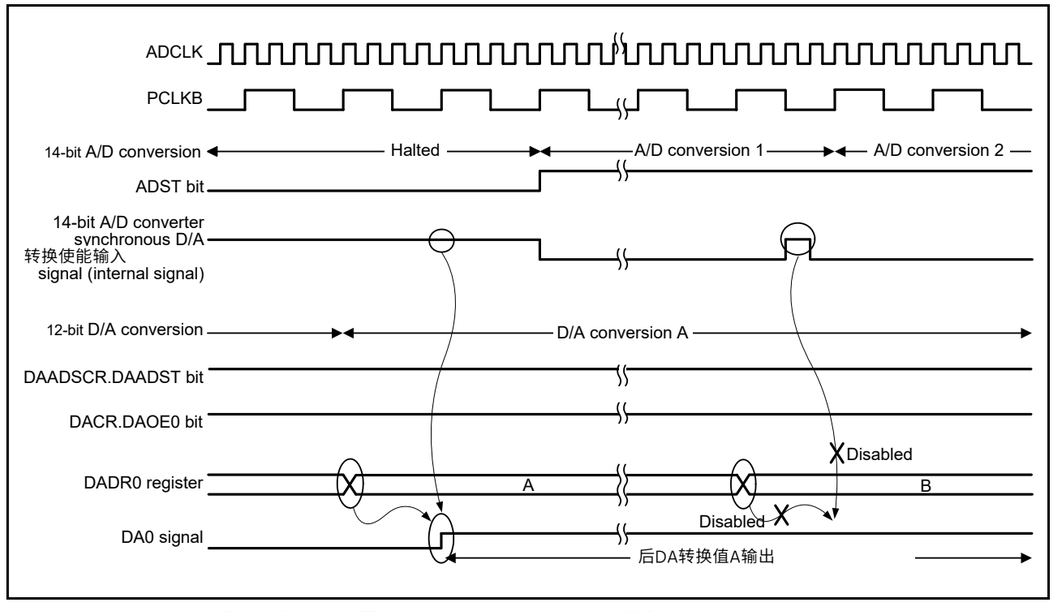


Figure 35.4 DAC12无法捕获ADC14同步DA转换使能输入信号时的示例

35.3.2 Notes on Using the Internal Reference Voltage as the Reference Voltage

When setting the DAVREFCR.REF[2:0] bits to 011b to use the internal reference voltage/AVSS0 as the reference voltage, the VREF path must be discharged before selecting the voltage. The following shows the discharging procedure:

1. Write 000b to the REF[2:0] bits.
2. Set the DADR0 register to 0000h.
3. Keep the state of (2) for 10 µs (discharging).
4. After discharging is complete, write 011b to the DAVREFCR.REF[2:0] bits and select the internal reference voltage/AVSS0.
5. Set the DACR.DAOE0 bit to 1 and wait 5 µs, the stabilization wait time of the internal reference voltage.
6. Write data to the DADR0 register and start D/A conversion.

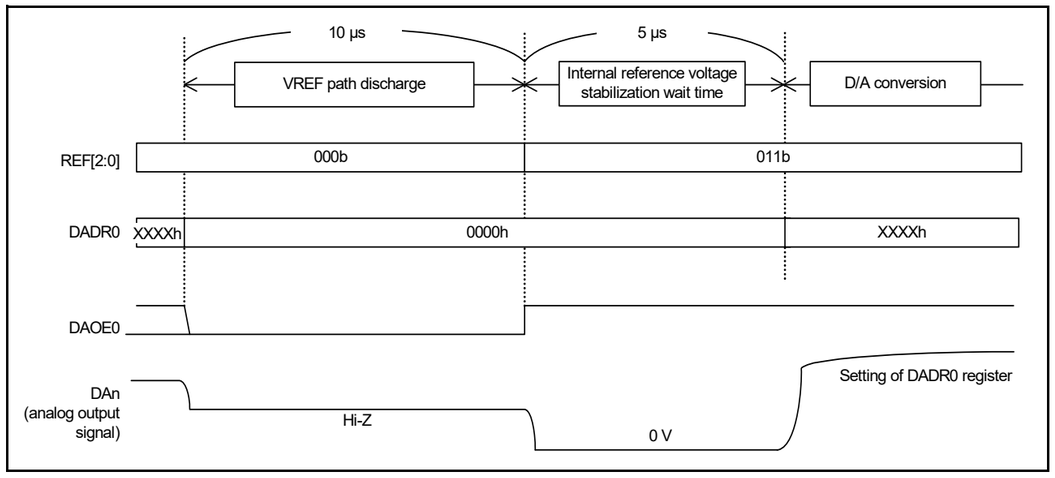


Figure 35.5 Procedure for selecting the internal reference voltage as the reference voltage

35.4 Event Link Operation Setting Procedure

To set up an event link operation (for DA0):

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA0 event signal to be linked to each peripheral module in the ELSR12 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit becomes 1, and D/A conversion starts on channel 0.
5. Set the ELSR12.ELS[7:0] bits to 00h to stop event link operation of the DAC12 channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

35.5 Usage Notes on Event Link Operation

- When the event specified by the ELC_DA0 event signal is generated while a write cycle to the DACR.DAOE0 bit is processed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1
- Use of the event link function is prohibited when the DAADSCR.DAADST bit is set to 1, to reduce interference between D/A and A/D conversions.

35.3.2 使用内部参考电压作为参考电压的注意事项

当将DAVREFCR.REF[2:0]位设置为011b以使用内部参考电压AVSS0作为参考电压时，必须在选择电压之前对VREF路径进行放电。放电过程如下：

1. 将000b写入REF[2:0]位。
2. 将DADR0寄存器设置为0000h。
3. 保持（2）状态10µs（放电）。
4. 放电完成后，将011b写入DAVREFCR.REF[2:0]位并选择内部参考电压AVSS0。
5. 将DACR.DAOE0位设置为1并等待5µs，即内部参考电压的稳定等待时间。
6. 将数据写入DADR0寄存器并启动DA转换。

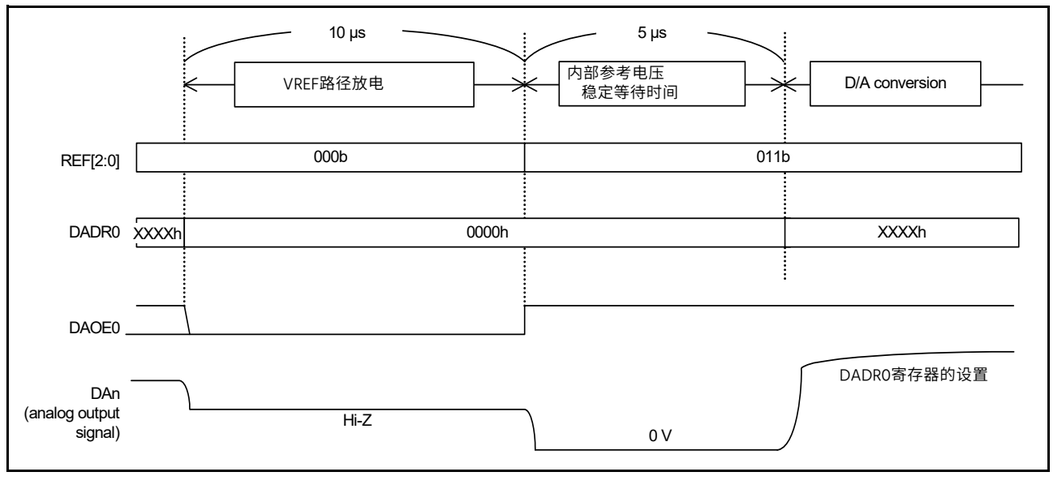


Figure 35.5 选择内部参考电压作为参考电压的步骤

35.4 事件链接操作设置步骤

要设置事件链接操作（对于DA0）：

1. 设置DADPR.DPSEL位并在DADR0寄存器中设置用于DA转换的数据。
2. 将ELC_DA0事件信号设置为链接到ELSR12寄存器中的每个外围模块。
3. 将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。
4. 设置事件输出源模块以激活事件链接。事件从模块输出后，DACR.DAOE0位变为1，通道0开始DA转换。
5. 将ELSR12.ELS[7:0]位设置为00h以停止DAC12通道0的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

35.5 事件链接操作使用说明

- 当在处理DACR.DAOE0位的写周期时产生由ELC_DA0事件信号指定的事件时，写周期停止，并且产生的事件优先将该位设置为1
- 当DAADSCR.DAADST位设置为1时，禁止使用事件链接功能，以减少DA和AD转换之间的干扰。

35.6 Usage Notes

35.6.1 Settings for the Module-Stop Function

The Module Stop Control register can enable or disable DAC12 operation. The DAC12 is stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

35.6.2 DAC12 Operation in Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, the D/A output is saved, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in the module-stop state, disable D/A conversion by setting the DACR.DAOE0 bit to 0.

35.6.3 DAC12 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, the D/A output is saved, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DACR.DAOE0 bit to 0.

35.6.4 Restriction on Usage when Interference Reduction between D/A and A/D Conversion is Enabled

When the DAADSCR.DAADST bit is 1, enabling interference reduction between D/A and A/D conversion do not place the ADC14 in the module-stop state. Doing so can halt D/A conversion in addition to A/D conversion.

35.6 使用说明

35.6.1 模块停止功能的设置

模块停止控制寄存器可以启用或禁用DAC12操作。DAC12在复位后停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

35.6.2 DAC12在模块停止状态下的操作

当单片机进入模数停止状态并开启数模转换时，数模输出被保存，模拟电源电流与数模转换时相同。如果必须在模块停止状态下降低模拟电源电流，则通过将DACR.DAOE0位设置为0来禁用DA转换。

35.6.3 DAC12在软件待机模式下的操作

当MCU进入软件待机模式且DA转换使能时，DA输出被保存，模拟电源电流与DA转换时相同。如果在软件待机模式下必须降低模拟电源电流，则通过将DACR.DAOE0位设置为0来禁用DA转换。

35.6.4 DA和AD之间减少干扰时的使用限制转换已启用

当DAADSCR.DAADST位为1时，启用DA和AD转换之间的干扰降低不会将ADC14置于模块停止状态。除了AD转换之外，这样做还可以停止DA转换。

36. Temperature Sensor (TSN)

36.1 Overview

The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can also be used by the end application.

Table 36.1 lists the temperature sensor specifications, and Figure 36.1 shows a block diagram.

Table 36.1 Temperature sensor specifications

Parameter	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the ADC14

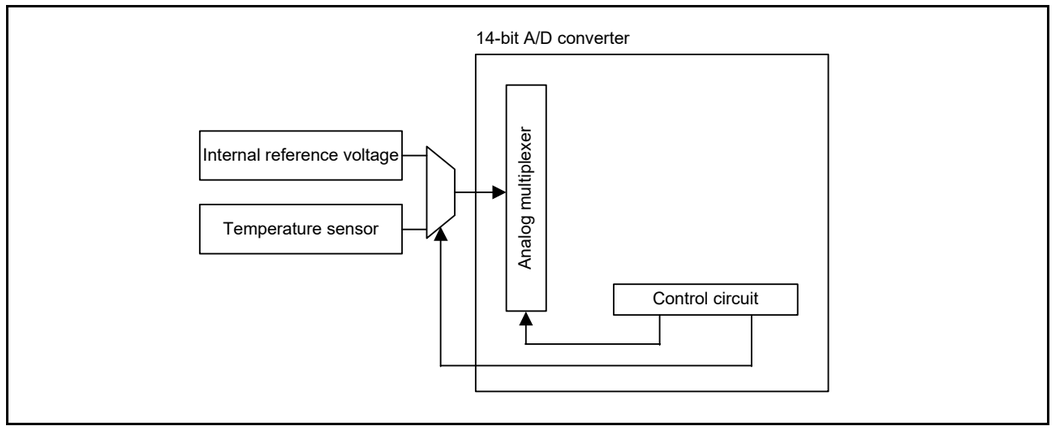
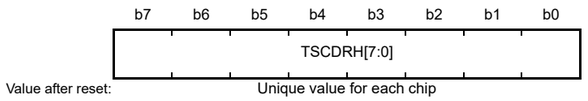


Figure 36.1 Temperature sensor block diagram

36.2 Register Descriptions

36.2.1 Temperature Sensor Calibration Data Register H (TSCDRH)

Address(es): TSN.TSCDRH 407E C229h



Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSCDRH[7:0]	Temperature Sensor Calibration Data	The calibration data stores the upper 4 bits of the converted value	R

36. 温度传感器(TSN)

36.1 Overview

片上温度传感器确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压呈线性关系。输出电压提供给ADC14进行转换，也可供最终应用使用。

表36.1列出了温度传感器规格，图36.1显示了框图。

Table 36.1 温度传感器规格

Parameter	Description
温度传感器电压输出	温度传感器向ADC14输出电压

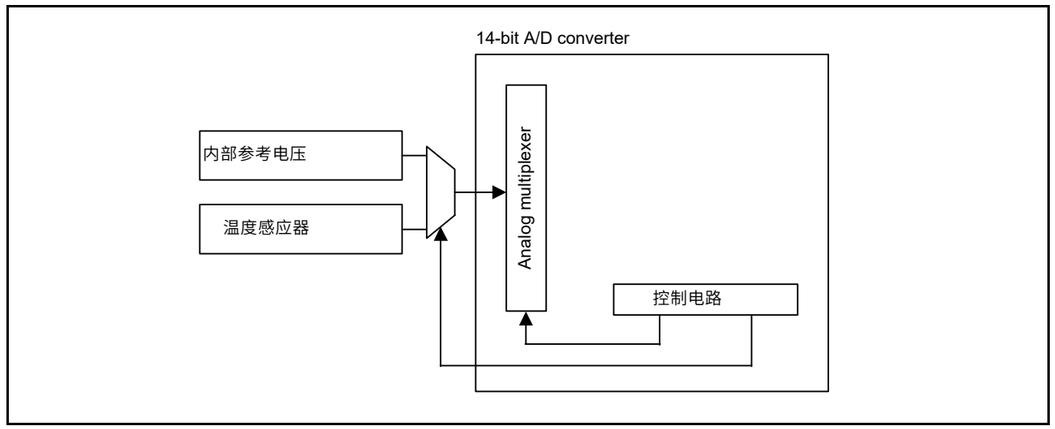
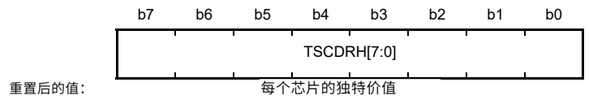


Figure 36.1 温度传感器框图

36.2 注册说明

36.2.1 温度传感器校准数据寄存器H(TSCDRH)

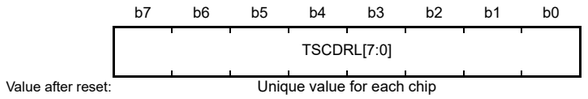
Address(es): TSN.TSCDRH 407E C229h



Bit	Symbol	位名称	Description	R/W
b7 to b0	TSCDRH[7:0]	温度感应器 校准数据	校准数据存储转换值的高4位	R

36.2.2 Temperature Sensor Calibration Data Register L (TSCDRL)

Address(es): TSN.TSCDRL 407E C228h



Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSCDRL[7:0]	Temperature Sensor Calibration Data	The calibration data stores the lower 8 bits of the converted value	R

The TSCDRH and TSCDRL registers store temperature sensor calibration data measured for each chip at factory shipment.

Temperature sensor calibration data is a digital value obtained using the ADC14 to convert the voltage output by the temperature sensor under the condition Ta = Tj = 125°C and AVCC0 = 3.3 V. The TSCDRH register stores the upper 4 bits of the converted value, and the TSCDRL register stores the lower 8 bits.

36.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the ADC14. To obtain the die temperature, convert this value into the temperature.

36.3.1 Preparation for Using Temperature Sensor

The temperature (T) is proportional to the sensor voltage output (Vs), so temperature is calculated with the following formula:

T = (Vs – V1)/slope + T1

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor on temperature measurement (V)

T1: Temperature experimentally measured at one point (°C)

V1: Voltage output by the temperature sensor on measurement of T1 (V)

T2: Temperature experimentally measured at a second point (°C)

V2: Voltage output by the temperature sensor on measurement of T2 (V)

Slope: Temperature gradient of the temperature sensor (V/°C). Slope = (V2 – V1)/(T2 – T1)

Characteristics vary between sensors. Therefore, Renesas recommends measuring two different sample temperatures as follows:

1. Use the ADC14 to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Use the ADC14 to measure the voltage V2 output by the temperature sensor at a different temperature T2. Obtain the temperature gradient (slope = (V2 - V1)/(T2 - T1)) from these results.
3. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs -V1)/Slope + T1).

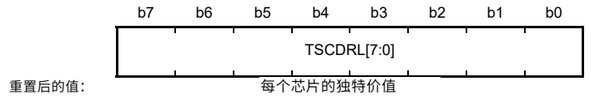
If you are using the temperature gradient given in section 48, Electrical Characteristics, only one experimental measurement is required to determine V1 and T1. However, this method gives less accurate temperature results than measurement at two points.

The TSCDRH and TSCDRL registers store the temperature value (CAL125) of the temperature sensor measured under the condition Ta = Tj = 125°C and AVCC0 = 3.3 V. If you use this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

This measured value CAL125 can be calculated as follows:

36.2.2 温度传感器校准数据寄存器L(TSCDRL)

Address(es): TSN.TSCDRL 407E C228h



Bit	Symbol	位名称	Description	R/W
b7 to b0	TSCDRL[7:0]	温度传感器校准 Data	校准数据存储转换值的低8位	R

TSCDRH和TSCDRL寄存器存储在出厂时为每个芯片测量的温度传感器校准数据。

温度传感器校准数据是在Ta=Tj=125°C和AVCC0=3.3V条件下，使用ADC14转换温度传感器输出的电压得到的数字值。TSCDRH寄存器存储转换值的高4位，TSCDRL寄存器存储低8位。

36.3 使用温度传感器

温度传感器输出随温度变化的电压。该电压由ADC14转换为数字值。要获得芯片温度，请将该值转换为温度。

36.3.1 使用温度传感器的准备工作

温度(T)与传感器电压输出(Vs)成正比，因此使用以下公式计算温度：

T = (Vs – V1)/slope + T1

T:测量温度(°C)

Vs：温度传感器测温时的电压输出（V）

T1：在某一点实验测量的温度(°C)

V1：温度传感器在测量T1(V)时输出的电压

T2：在第二点实验测量的温度(°C)

V2：温度传感器在测量T2(V)时输出的电压

斜率：温度传感器的温度梯度(V°C)。斜率=(V2 V1)(T2 T1)

特性因传感器而异。因此，瑞萨推荐测量两种不同的样品温度，如下所示：

1. 使用ADC14测量温度T1时温度传感器输出的电压V1。
2. 使用ADC14测量温度传感器在不同温度T2下输出的电压V2。从这些结果中获得温度梯度（斜率=(V2V1)(T2T1)）。
3. 随后，通过将斜率代入温度特性公式(T=(Vs-V1)Slope+T1)来获得温度。

如果您使用第48节"电气特性"中给出的温度梯度，则只需进行一次实验测量即可确定V1和T1。然而，这种方法给出的温度结果不如两点测量准确。

TSCDRH和TSCDRL寄存器存储在Ta=Tj=125°C和AVCC0=3.3V条件下测量的温度传感器的温度值（CAL125）。如果将此值用作第一点的样本测量结果，则可以省略使用温度传感器前的准备工作。

这个测量值CAL125可以计算如下：

CAL125 = TSCDRH register value << 8 + TSCDRL register value

V1 is calculated from CAL125 as follows:

V1 = 3.3 × CAL125/4096 [V]

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1)/Slope + 125 [°C]

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when the temperature is measured (V)

V1: Voltage output by the temperature sensor when Ta = Tj = 125°C and AVCC0 = 3.3 V (V)

Slope: Temperature gradient of the temperature sensor ÷ 1,000 (V/°C)

Figure 36.2 shows the error in the measured temperature. The variation range is 3σ.

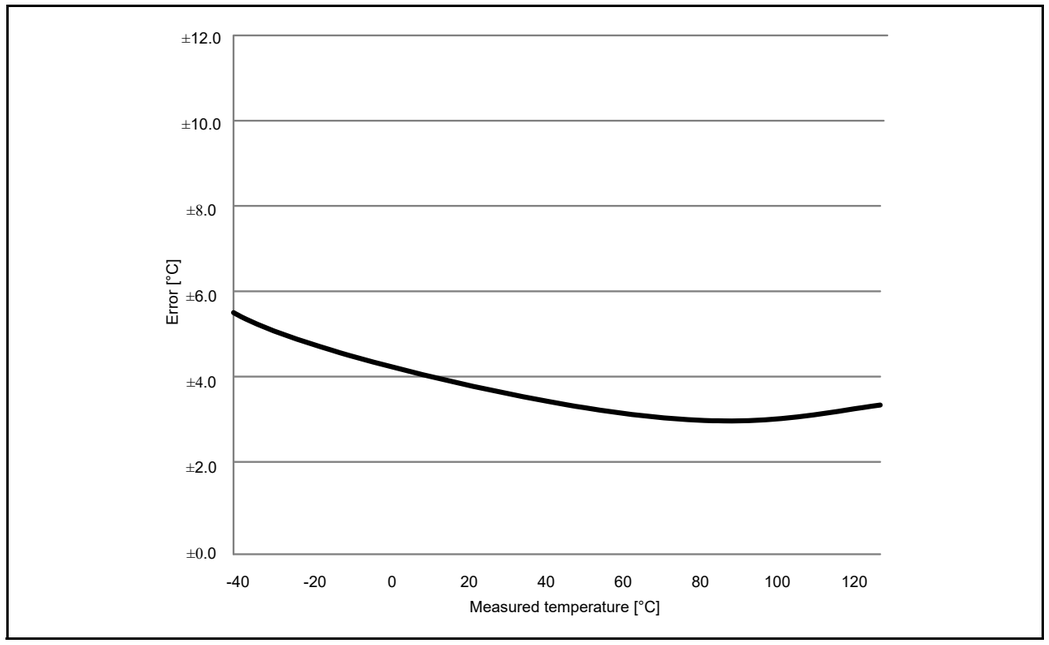


Figure 36.2 Error in the measured temperature (designed values)

36.3.2 Procedure for Using the Temperature Sensor

For details, see section 34, 14-Bit A/D Converter (ADC14).

CAL125=TSCDRH寄存器值<<8+TSCDRL寄存器值

V1从CAL125计算如下：

V1 = 3.3 × CAL125/4096 [V]

使用该值，可根据以下公式计算测得的温度：

T = (Vs - V1)/Slope + 125 [°C]

T:测量温度(°C)

Vs：测温时温度传感器输出的电压（V）

V1：Ta=Tj=125°C且AVCC0=3.3V(V)时温度传感器输出的电压

斜率：温度传感器的温度梯度÷1 000(V°C)

图36.2显示了测量温度的误差。变化范围为3 。

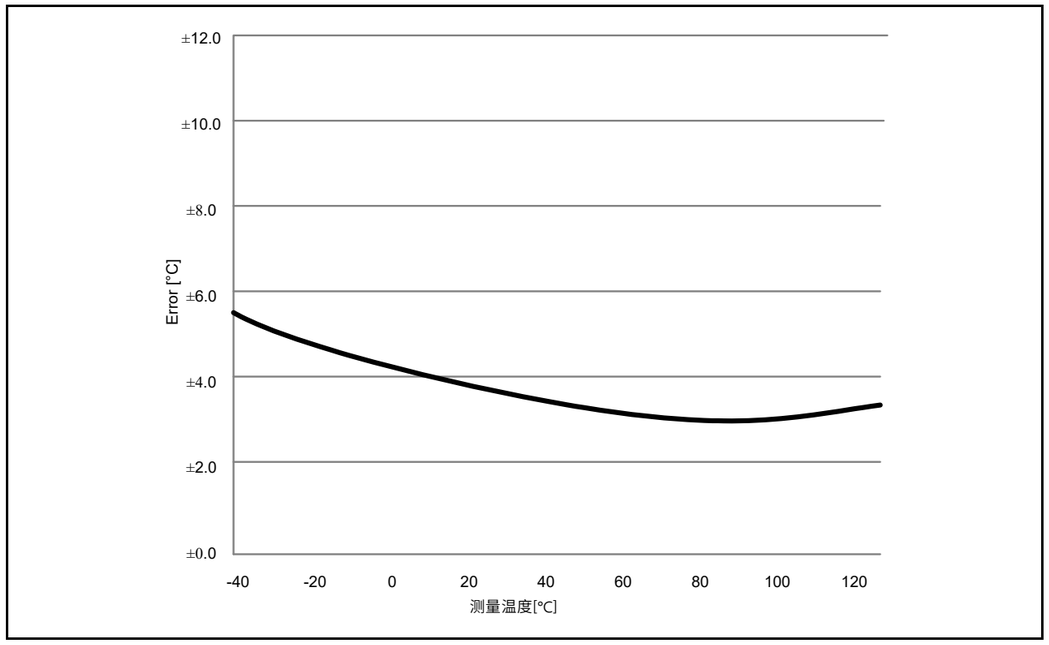


Figure 36.2 测量温度误差（设计值）

36.3.2 使用温度传感器的步骤

有关详细信息，请参阅第34节，14位AD转换器(ADC14)。

37. Operational Amplifier (OPAMP)

37.1 Overview

Operational amplifiers can be used to amplify small analog input voltages and output the amplified voltages. The MCU has an operational amplifier unit with two input pins and one output pin.

The operational amplifiers have the following functions:

- The output signal from a unit can be used for the input signal to the A/D converter
- High-speed mode (high-current consumption) and low-power mode (slow-speed response) are supported and either mode can be selected based on trade-offs between the response speed and current consumption
- Operation can be started by each trigger from the Asynchronous General purpose Timer (AGT)
- Operation can be stopped by an A/D conversion end trigger.

Figure 37.1 shows a block diagram of the operational amplifier, and Table 37.1 lists the unit configuration.

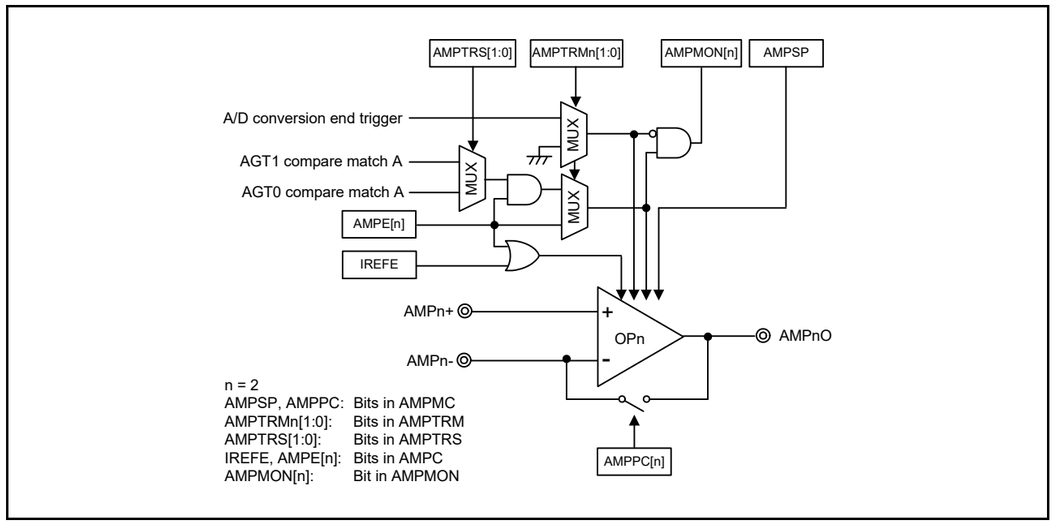


Figure 37.1 Operational amplifier block diagram

Table 37.1 OPAMP unit configuration

Unit	I/O pin	I/O	Function
Unit 2 (Operational amplifier 2)	AMP2+, AMP2-	Input	Input pin of operational amplifier 2 (+, -)
	AMP2O	Output	Output pin of operational amplifier 2

37. 运算放大器(OPAMP)

37.1 Overview

运算放大器可用于放大小的模拟输入电压并输出放大的电压。MCU有一个运算放大器单元，带有两个输入引脚和一个输出引脚。

运算放大器具有以下功能：

- 一个单元的输出信号可用作模数转换器的输入信号
- 支持高速模式（大电流消耗）和低功耗模式（慢速响应），可以根据响应速度和电流消耗之间的权衡选择任一模式
- 操作可由异步通用定时器(AGT)的每个触发器启动
- 可以通过AD转换结束触发器停止操作。

图37.1显示了运算放大器的框图，表37.1列出了单元配置。

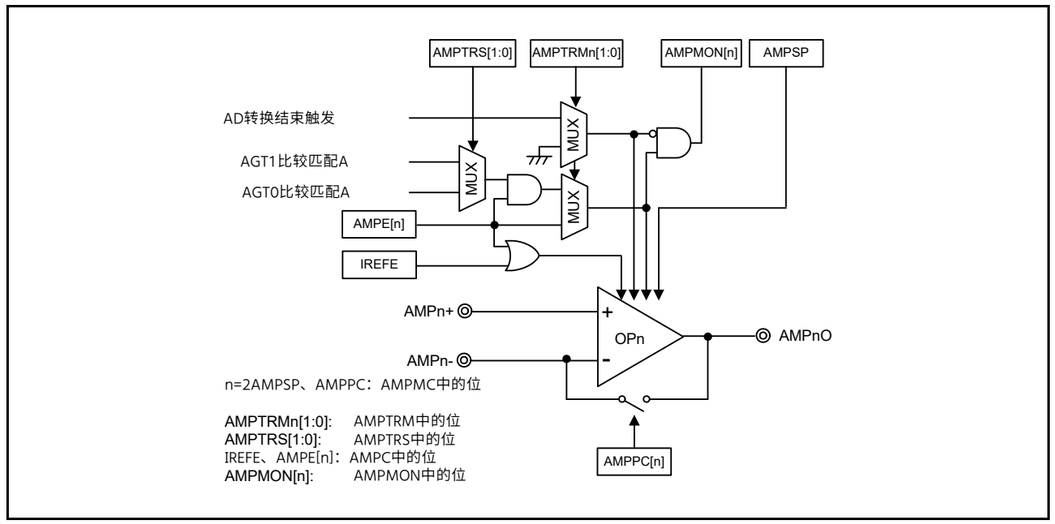


Figure 37.1 运算放大器框图

Table 37.1 运算放大器单元配置

Unit	I/O pin	I/O	Function
单元2（运算放大器2）	AMP2+, AMP2-	Input	运算放大器2的输入引脚（+，−）
	AMP2O	Output	运算放大器2的输出引脚

37.2 Register Descriptions

37.2.1 Operational Amplifier Mode Control Register (AMPMC)

Address(es): OPAMP.AMPMC 4008 6008h

	b7	b6	b5	b4	b3	b2	b1	b0
	AMPSP	—	—	—	—	AMPPC[2]	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	AMPPC[2]	Operational Amplifier Precharge Control	0: Precharging of operational amplifier 2 is stopped. 1: Precharging of operational amplifier 2 is enabled.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AMPSP	Operational Amplifier Operation Mode Selection	0: Low-power mode (low-speed) 1: High-speed mode.	R/W

Note: Set AMPSP bit while the AMPC register is 00h (operational amplifier and reference current generator are stopped).
Note: Be sure to set bits that are not used in this register to the initial value.

37.2 注册说明

37.2.1 运算放大器模式控制寄存器(AMPMC)

Address(es): OPAMP.AMPMC 4008 6008h

	b7	b6	b5	b4	b3	b2	b1	b0
	AMPSP	—	—	—	—	AMPPC[2]	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	AMPPC[2]	运算放大器 Precharge Control	0：停止运算放大器2的预充电。1：使能运算放大器2的预充电。	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	AMPSP	运算放大器 操作模式选择	0: Low-power mode (low-speed) 1: High-speed mode.	R/W

Note: 当AMPC寄存器为00h时设置AMPSP位（运算放大器和参考电流发生器停止）。
Note: 请务必将此寄存器中未使用的位设置为初始值。

37.2.2 Operational Amplifier Trigger Mode Control Register (AMPTRM)

Address(es): OPAMP.AMPTRM 4008 6009h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AMPTRM2[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	AMPTRM2[1:0]	OPAMP Function Activation/ Stop Trigger Control *2	AMPTRM2[1] AMPTRM2[0] 0 0: Software trigger mode: •The operational amplifier can be activated/ stopped by setting the AMPC register •The operational amplifier cannot be activated by an activation trigger •The operational amplifier cannot be controlled by an A/D conversion end trigger. 0 1: Activation trigger mode: •The operational amplifier can be set to wait for an activation trigger or stopped by setting the AMPC register •The operational amplifier can be activated by an activation trigger*1 •The operational amplifier cannot be controlled by an A/D conversion end trigger. 1 0: Setting prohibited 1 1: Activation and A/D trigger mode: •The operational amplifier can be set to wait for an activation trigger or stopped by setting the AMPC register •The operational amplifier can be activated by an activation trigger*1 •The operational amplifier can be stopped by an A/D conversion end trigger. An A/D conversion end trigger is always generated at the end of A/D conversion.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: An A/D conversion end trigger is always generated at the end of A/D conversion.
Note 1. When using an activation trigger to activate the operational amplifier, first specify settings related to the AGT, set the AMPTRS register, and then use the AMPC register to set the OPAMP Operation Control bit to be activated to 1 (operational amplifier wait state is enabled).
Note 2. When changing the set values of AMPTRM2[1:0], make sure that the AMPE[2] bit in the AMPC register is 0 (operation amplifier is stopped).

37.2.2 运算放大器触发模式控制寄存器(AMPTRM)

Address(es): OPAMP.AMPTRM 4008 6009h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AMPTRM2[1:0]		—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	AMPTRM2[1:0]	OPAMP Function Activation/ 停止触发控制*2	AMPTRM2[1] AMPTRM2[0] 00：软件触发方式： 运算放大器可以通过设置AMPC寄存器来激活停止 运算放大器不能由激活触发器激活 运算放大器不能由AD转换结束触发器控制。01：激活触发方式： 通过设置AMPC寄存器，可以将运算放大器设置为等待激活触发或停止。 可以通过激活触发器激活运算放大器*1 运算放大器不能由AD转换结束触发器控制。10：设置禁止11：激活和AD触发方式： 运算放大器可以通过设置AMPC寄存器设置为等待激活触发或停止 运算放大器可以通过激活触发器激活*1 运算放大器可以通过AD转换结束触发器停止。AD转换结束触发总是在AD转换结束时产生。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: AD转换结束触发总是在AD转换结束时产生。
Note 1. 使用激活触发器激活运算放大器时，首先指定与AGT相关的设置，设置AMPTRS寄存器，然后使用AMPC寄存器将要激活的OPAMP操作控制位设置为1（启用运算放大器等待状态）.
Note 2. 更改AMPTRM2[1:0]的设定值时，请确保AMPC寄存器中的AMPE[2]位为0（运算放大器停止）。

37.2.3 Operational Amplifier Activation Trigger Select Register (AMPTRS)

Address(es): OPAMP.AMPTRS 4008 600Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AMPTRS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	AMPTRS[1:0]	Activation Trigger Selection*1	b1 b0 0 0: Operational amplifier 2: Operational amplifier activation trigger 2 0 1: Operational amplifier 2: Operational amplifier activation trigger 1 1 0: Setting prohibited 1 1: Operational amplifier 2: Operational amplifier activation trigger 0	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Be sure to set bits that are not used in this register to the initial value.
Note 1. Do not change the value of the AMPTRS register after setting the AMPTRM register.

37.2.4 Operational Amplifier Control Register (AMPC)

Address(es): OPAMP.AMPC 4008 600Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IREFE	—	—	—	—	AMPE[2]	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	AMPE[2]	OPAMP Operation Control	0: Operation amplifier 2 is stopped 1: Software trigger mode: Operation of operational amplifier 2 is enabled.*1 Activation trigger mode or activation and A/D trigger mode: Wait until AGT is enabled.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	IREFE	OPAMP Reference Current Circuit Operation Control	0: Operational amplifier reference current circuit is stopped 1: Operation of operational amplifier reference current circuit is enabled.	R/W

Note: Be sure to set bits that are not used in this register to the initial value.
Note 1. Operation of the operational amplifier reference current circuit is also enabled regardless of the IREFE bit setting. Be sure to set the bits to 0 for a unit that is not to be used.

Table 37.2 shows the operational amplifier activation triggers associated with events.

Table 37.2 Operational amplifier activation triggers associated with events

Trigger	Event
Operational Amplifier activation trigger 0	AGT1 compare match A
Operational Amplifier activation trigger 1	AGT0 compare match A
Operational Amplifier activation trigger 2	AGT1 compare match A

37.2.3 运算放大器激活触发选择寄存器(AMPTRS)

Address(es): OPAMP.AMPTRS 4008 600Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AMPTRS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	AMPTRS[1:0]	激活触发器选择*1	b1b000：运算放大器2：运算放大器启动触发201：运算放大器2：运算放大器启动触发110：设置禁止11：运算放大器2：运算放大器启动触发0	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 请务必将此寄存器中未使用的位设置为初始值。
Note 1. 设置AMPTRM寄存器后不要更改AMPTRS寄存器的值。

37.2.4 运算放大器控制寄存器(AMPC)

Address(es): OPAMP.AMPC 4008 600Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IREFE	—	—	—	—	AMPE[2]	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	AMPE[2]	运算放大器操作控制	0：运算放大器2停止1：软件触发模式：运算放大器2运行。*1 激活触发模式或激活和AD触发模式： 等到启用AGT。	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	IREFE	运算放大器参考电流电路运行控制	0：运算放大器参考电流电路停止1：运算放大器参考电流电路工作使能。	R/W

Note: 请务必将此寄存器中未使用的位设置为初始值。
Note 1. 无论IREFE位设置如何，运算放大器参考电流电路的操作也会启用。对于不使用的单元，请务必将位设置为0。

表37.2显示了与事件相关的运算放大器激活触发器。

Table 37.2 与事件相关的运算放大器激活触发器

Trigger	Event
运算放大器激活触发器0	AGT1比较匹配A
运算放大器激活触发器1	AGT0比较匹配A
运算放大器激活触发器2	AGT1比较匹配A

37.2.5 Operational Amplifier Monitor Register (AMPMON)

Address(es): OPAMP.AMPMON 4008 600Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	AMPMON[2]	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0	R
b2	AMPMON[2]	Operational Amplifier 2 Status	0: Operational amplifier 2 is stopped 1: Operational amplifier 2 is operating.	R
b7 to b3	—	Reserved	These bits are read as 0	R

Note: This register is used to asynchronously reflect whether each operational amplifier is operating or stopped. To determine the operational amplifier state, read this register continuously to determine when the bit state changes.
When an activation trigger or A/D conversion end trigger synchronized with the clock or a software trigger in the other interrupt routine is used to control the operational amplifier, the timing to operate or stop the operational amplifier can be estimated, such as for checking normal operation. In this case, read this register after 1 CPU/peripheral clock cycle when the associated trigger or interrupt affecting the operational amplifier state occurs. Be sure to set bits that are not used in this register to the initial value.

37.3 Operation

37.3.1 State Transitions

Figure 37.2 shows state transitions when the operational amplifier and reference current circuit are activated or stopped using the operational amplifier control circuit.

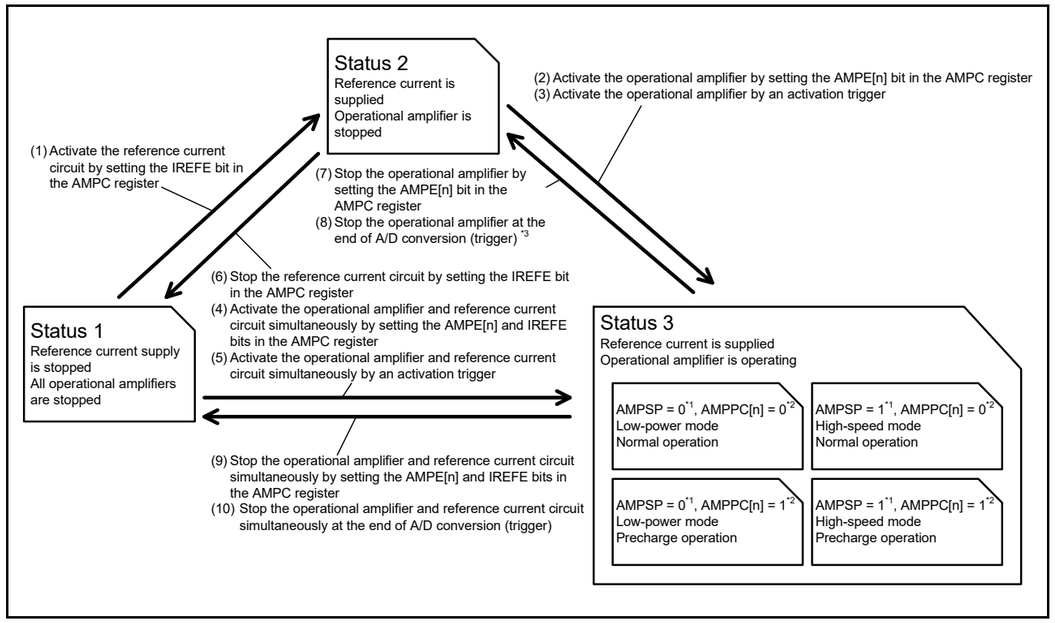


Figure 37.2 Operational amplifier state transitions

Note 1. Set the AMPSP bit in the AMPMC register and the AMPTRS and AMPTRM registers in status 1.

37.2.5 运算放大器监控寄存器(AMPMON)

Address(es): OPAMP.AMPMON 4008 600Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	AMPMON[2]	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读为0	R
b2	AMPMON[2]	运算放大器2状态	0：运算放大器2停止1：运算放大器2正在运行。	R
b7 to b3	—	Reserved	这些位被读为0	R

Note: 该寄存器用于异步反映每个运算放大器是在工作还是停止。要确定运算放大器的状态，请连续读取该寄存器以确定位状态何时发生变化。当使用与时钟同步的激活触发器或AD转换结束触发器或其他中断程序中的软件触发器来控制运算放大器时，可以估计操作或停止运算放大器的时序，例如检查正常操作。在这种情况下，当影响运算放大器状态的相关触发或中断发生时，在1个CPU外设时钟周期后读取该寄存器。请务必将此寄存器中未使用的位设置为初始值。

37.3 Operation

37.3.1 状态转换

图37.2显示了使用运算放大器控制电路激活或停止运算放大器和参考电流电路时的状态转换。

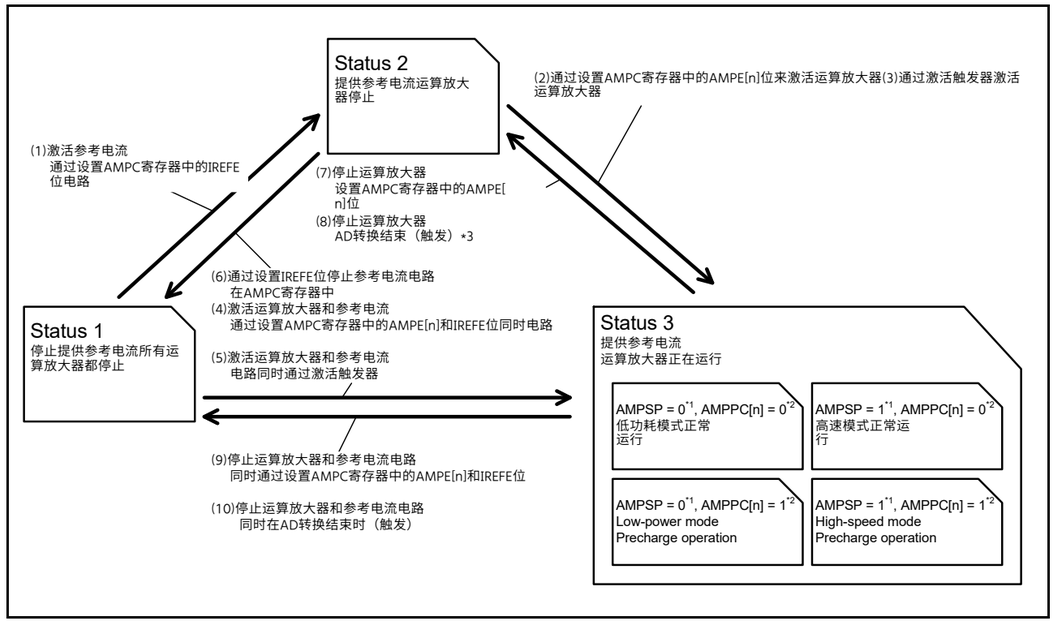


Figure 37.2 运算放大器状态转换

注1.设置AMPMC寄存器中的AMPSP位，并将AMPTRS和AMPTRM寄存器设置为状态1。

Note 2. Set the AMPPC[2] bit in the AMPMC register in status 3.
Note 3. To stop only the operational amplifier at the end of A/D conversion, it is required to preset operation of the reference current circuit to be enabled (operate the operational amplifier by status 2).

A stabilization wait time is required after supply of the reference current and operation of the operational amplifier are set before each operation actually starts. For details on the stabilization wait time, see section 48, Electrical Characteristics.

The operational amplifier cannot be activated/stopped continuously in steps (2) → (8), (2) → (10), (3) → (10), and (4) → (10).

An activation trigger and end of A/D conversion can be used to activate or stop only the operational amplifier that is preset to be used by setting the AMPTRM register.

注2.在状态3中设置AMPMC寄存器中的AMPPC[2]位。
注3.若要在AD转换结束时仅停止运算放大器，需要预先设置要启用的基准电流电路的操作（以状态2操作运算放大器）。

在基准电流的供应和运算放大器的操作设置之后，在每个操作实际开始之前需要稳定等待时间。有关稳定等待时间的详细信息，请参阅第48节，电气特性。

运算放大器不能在步骤(2) (8) (2) (10) (3) (10)和(4) (10)中连续激活停止。

激活触发和AD转换结束可用于激活或停止仅通过设置AMPTRM寄存器预设要使用的运算放大器。

37.3.2 Operational Amplifier Control Operation

Figure 37.3 to Figure 37.6 show operational amplifier control operation.

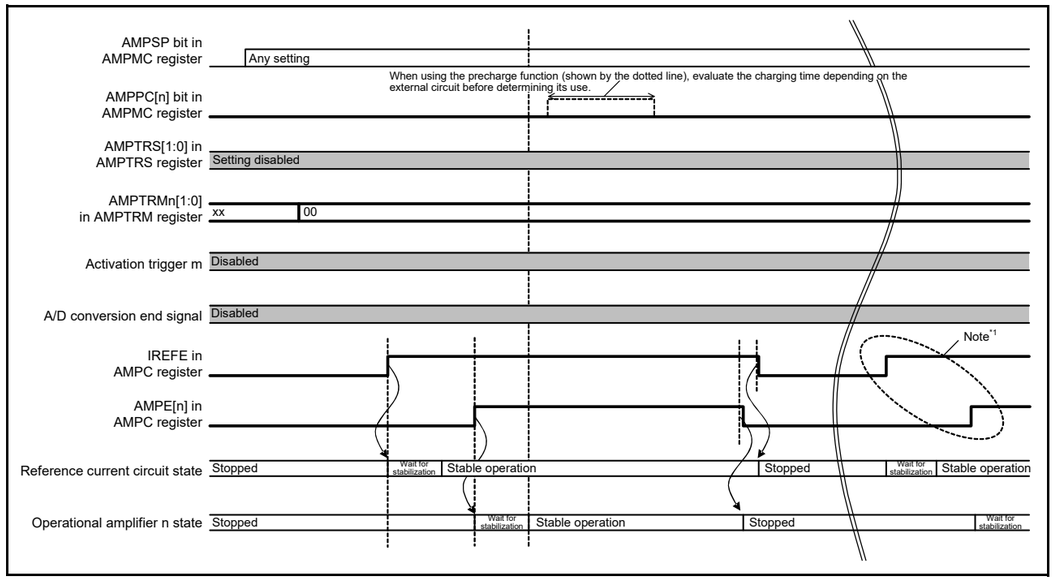


Figure 37.3 Operational amplifier control operation in software trigger mode used for control when the reference current circuit and operational amplifier are activated/stopped by software trigger mode

Note: n: Unit number (n = 2).
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.
Note 1. When operating or stopping the operational amplifier continuously, set the IREFE and AMPE[n] bits again as in the first setting after the operational amplifier is stopped.

37.3.2 运算放大器控制操作

图37.3至图37.6显示了运算放大器的控制操作。

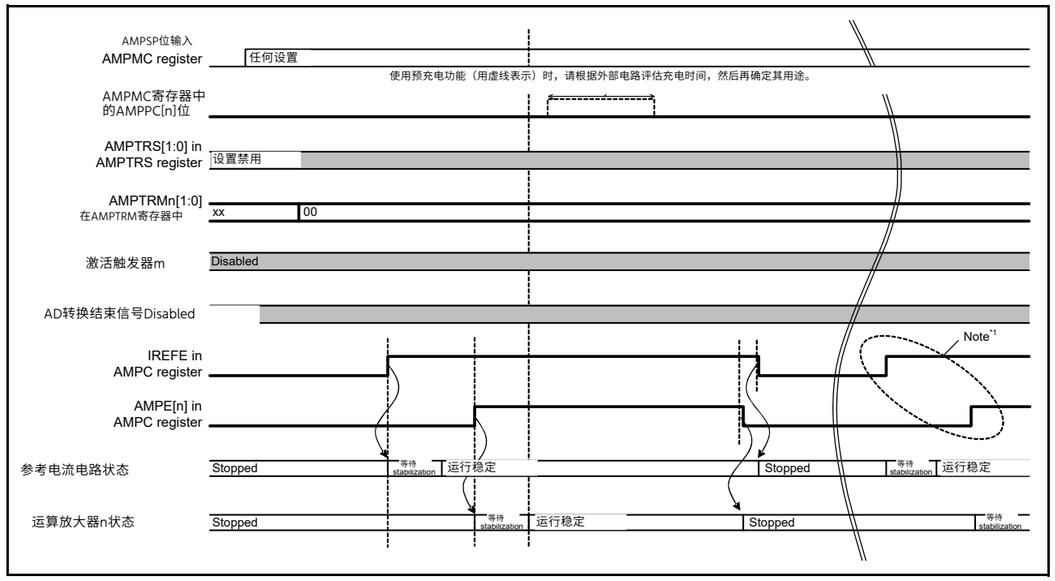


Figure 37.3 软件触发模式下的运算放大器控制操作，用于在软件触发模式下激活参考电流电路和运算放大器时进行控制

注：n：单元号（n=2）。m：激活触发器，用于控制由AMPTRS寄存器选择的运算放大器单元n。注1.连续操作或停止运算放大器时，在运算放大器停止后再次设置IREFE和AMPE[n]位，如第一次设置一样。

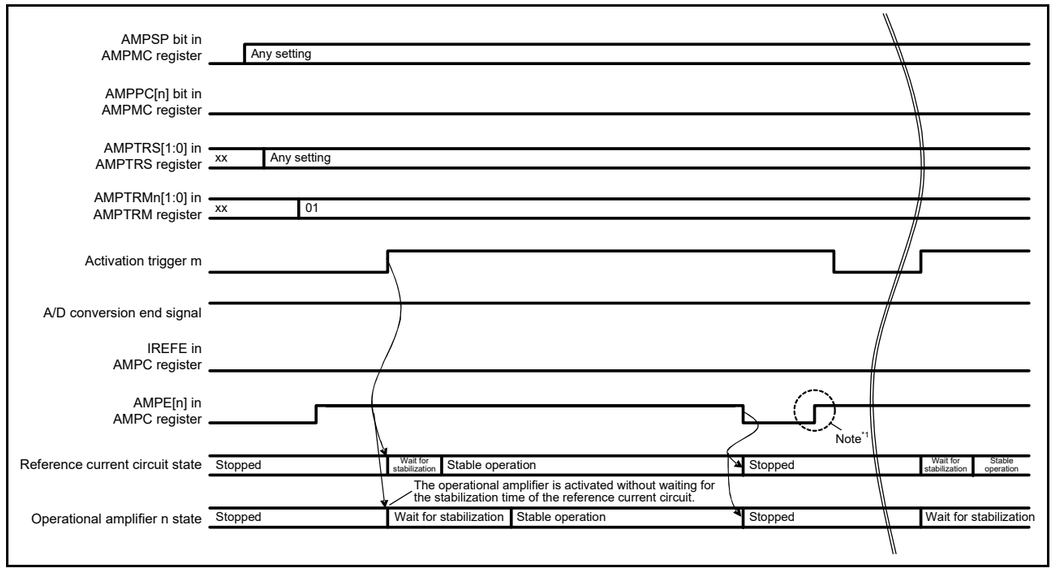


Figure 37.4 Operational amplifier control operation when activation trigger mode is used for activation with the reference current circuit and operational amplifier activated by an activation trigger and stopped by setting the AMPC register

Note: n: Unit number (n = 2).
m: An activation trigger used to control operational amplifier unit n selected in the AMPTRS register.
Set the AGT function.

Note 1. When operating or stopping the operational amplifier continuously, use the AMPE[n] bit again as in the first setting, and set the operational amplifier to wait for an activation trigger after it is stopped.

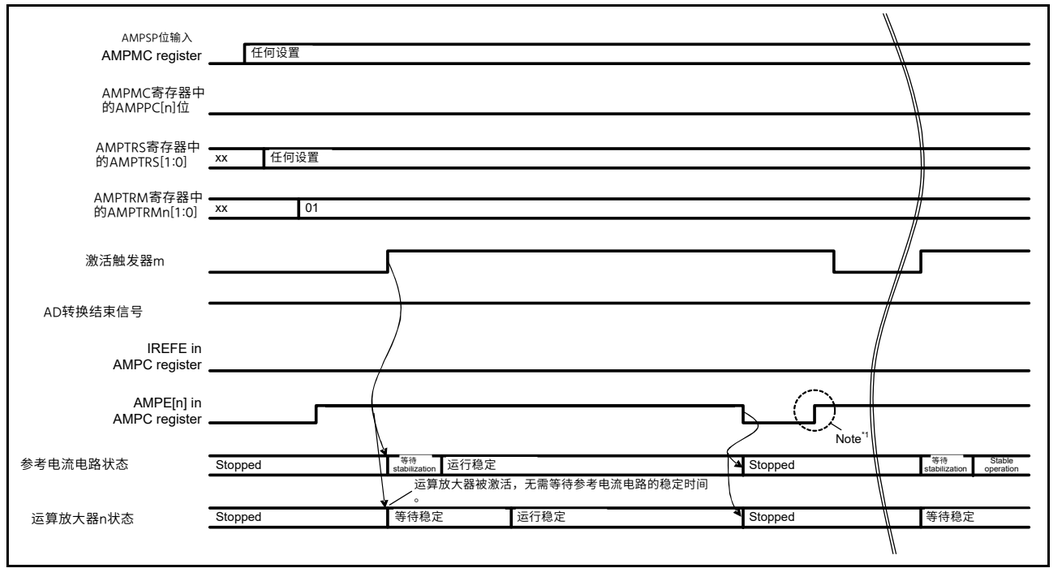


Figure 37.4 当参考电流电路和运算放大器由激活触发器激活并通过设置AMPC寄存器停止时使用激活触发模式进行激活时的运算放大器控制操作

Note: n：单元编号（n=2）。m：激活触发器，用于控制在AMPTRS寄存器中选择的运算放大器单元n。设置AGT功能。

注1.连续操作或停止运算放大器时，再次使用AMPE[n]位，与第一次设置一样，并设置运算放大器在停止后等待激活触发。

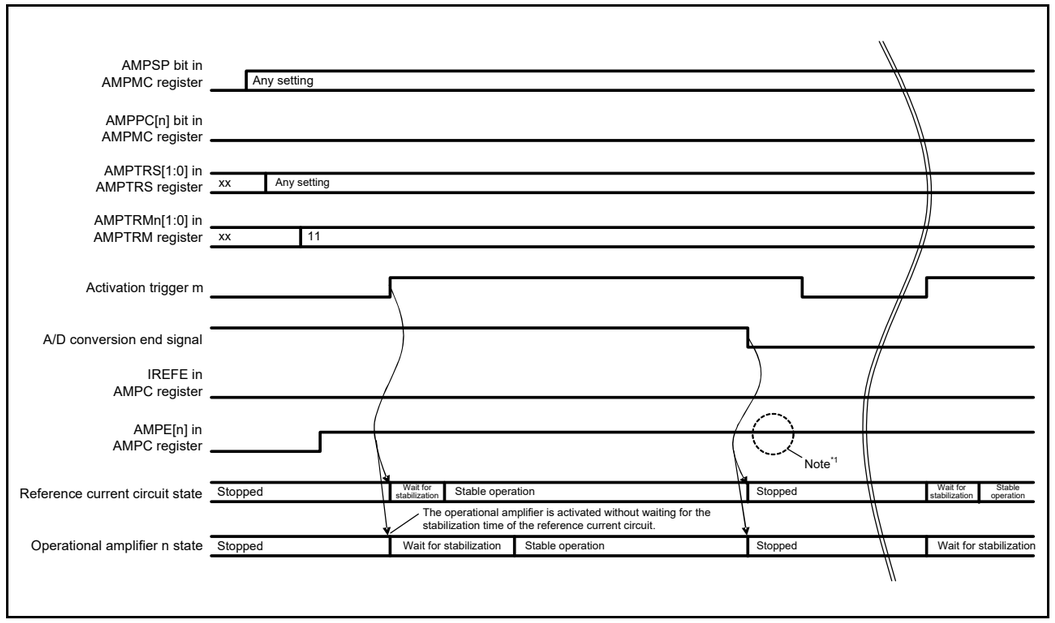


Figure 37.5 Operational amplifier control operation in activation and A/D trigger mode (1) with the reference current circuit and operational amplifier activated by an activation trigger and stopped by an A/D conversion end (trigger)

Note: n: Unit number (n = 2).
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.
Set the AGT function.

Note 1. When operating or stopping the operational amplifier continuously, it is not required to set the registers again because the operational amplifier waits for an activation trigger after it is stopped.

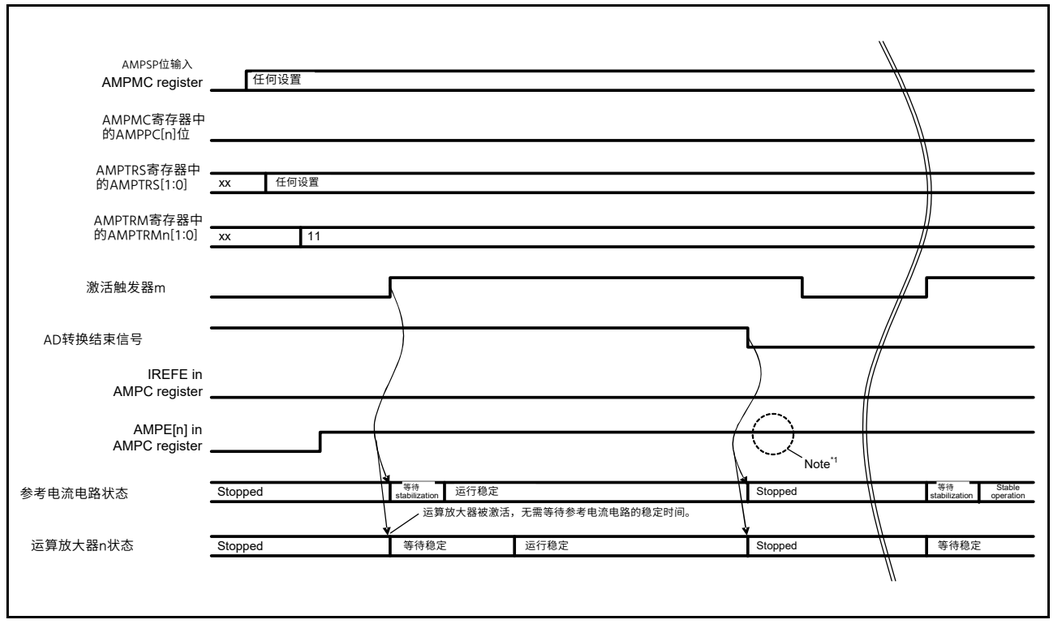


Figure 37.5 激活和AD触发模式下的运算放大器控制操作(1)参考电流电路和运算放大器由激活触发器激活并由AD转换结束(触发器)停止

Note: n：单元编号（n=2）。m：激活触发器，用于控制由AMPTRS寄存器选择的运算放大器单元n。设置AGT功能。

注1.当运算放大器连续运行或停止时，不需要重新设置寄存器，因为运算放大器在停止后等待激活触发。

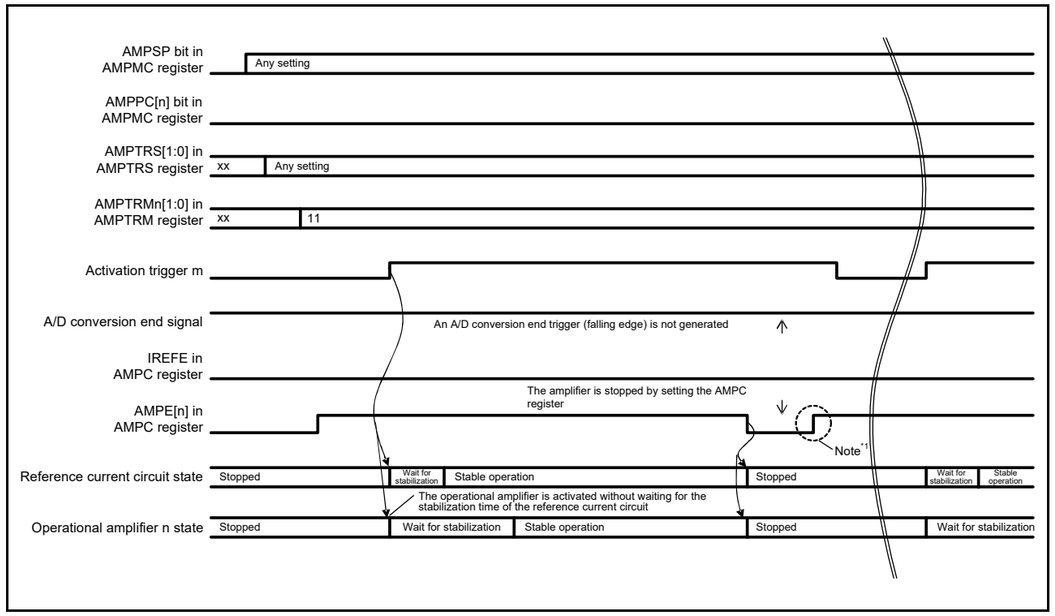


Figure 37.6 Operational amplifier control operation in activation and A/D trigger mode (2) with the reference current circuit and operational amplifier stopped by setting the AMPC register to be activated by an activation trigger and stopped by an A/D conversion end (trigger)

Note: n: Unit number (n = 2).
m: An activation trigger used to control operational amplifier unit n selected by the AMPTRS register.
Set the AGT function. See section 37.4, Software Trigger Mode for the procedure to activate the operational amplifier with an activation trigger.

Note 1. When operating or stopping the operational amplifier continuously, use the AMPE[n] bit again as in the first setting, and set the operational amplifier to wait for an activation trigger after it is stopped.

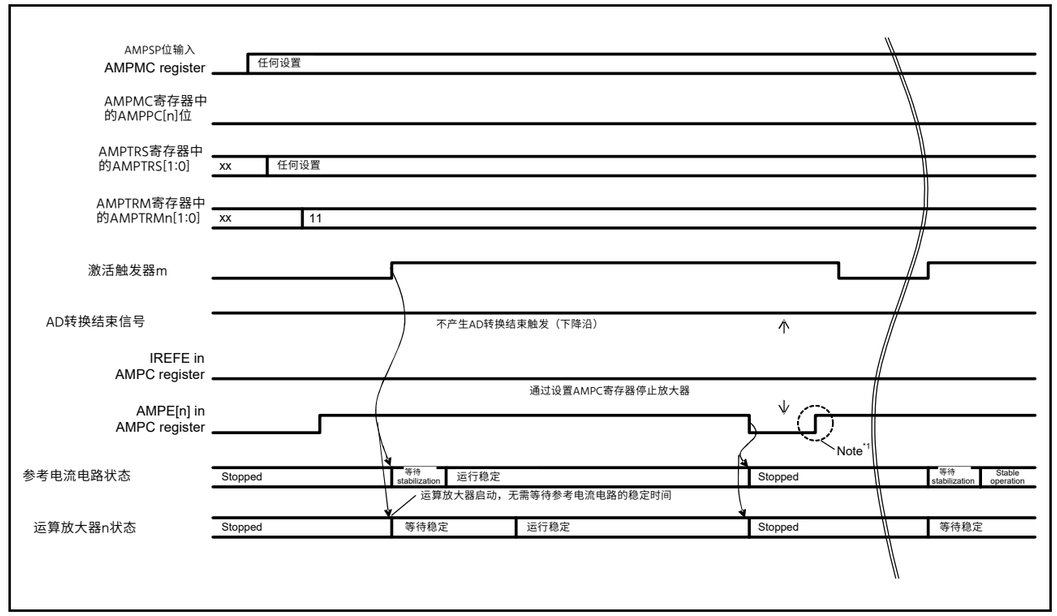
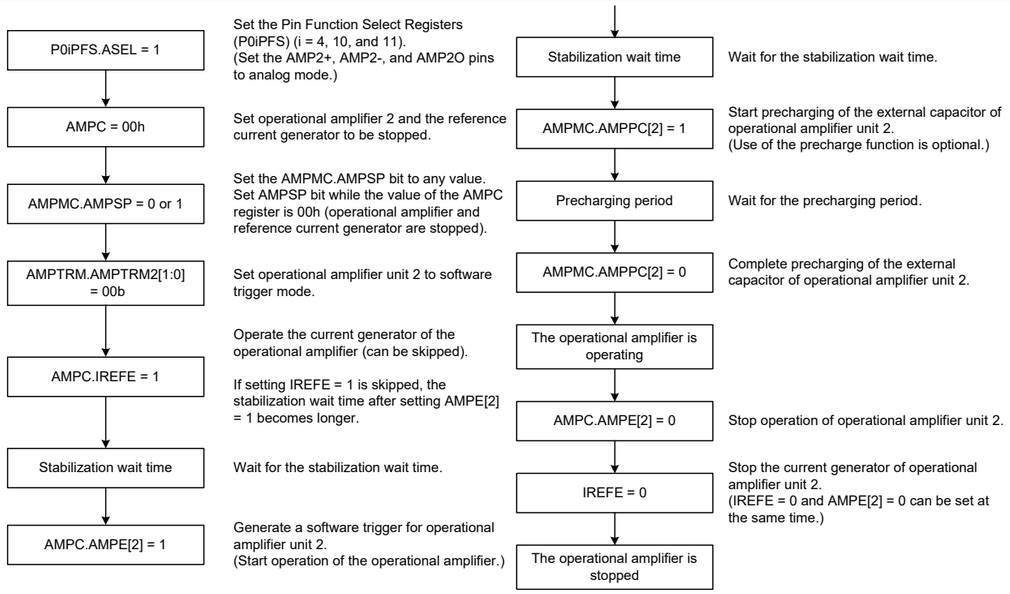


Figure 37.6 激活和AD触发模式下的运算放大器控制操作(2)通过将AMPC寄存器设置为由激活触发器激活并由AD转换结束（触发器）停止，从而停止参考电流电路和运算放大器

注：n：单元号（n=2）。m：激活触发器，用于控制由AMPTRS寄存器选择的运算放大器单元n。设置AGT功能。有关使用激活触发器激活运算放大器的程序，请参见第37.4节，软件触发模式。注1.连续操作或停止运算放大器时，再次使用AMPE[n]位，与第一次设置一样，并设置运算放大器在停止后等待激活触发。

37.4 Software Trigger Mode

This section describes the procedure to activate and stop the operational amplifier using a software trigger. Figure 37.7 shows an example of each register setting.

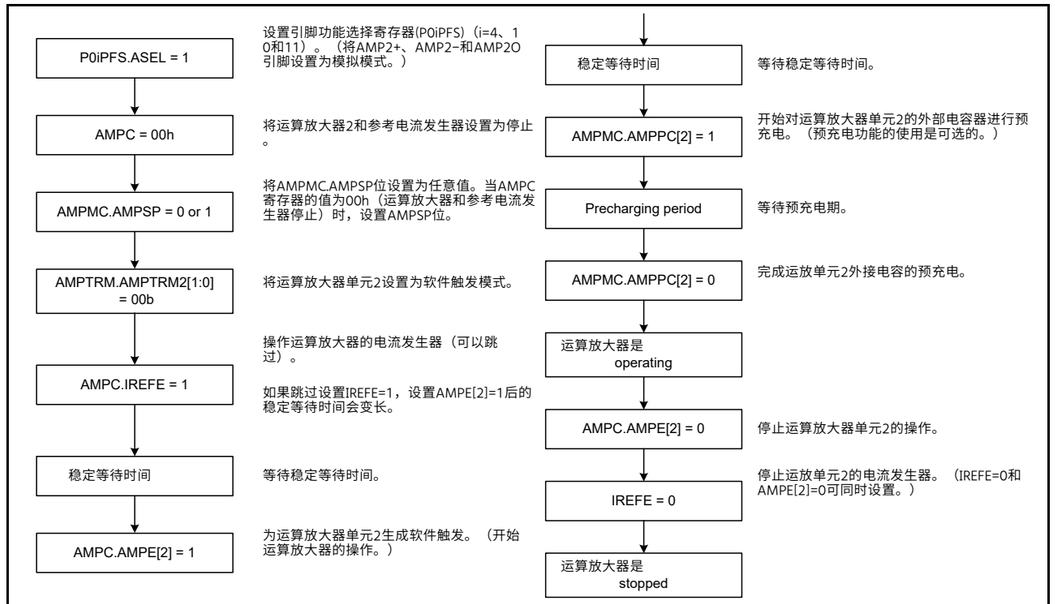


Note: For details on the stabilization wait time, see section 48, Electrical Characteristics

Figure 37.7 Procedure to start and stop OPAMP in software trigger mode

37.4 软件触发模式

本节介绍使用软件触发激活和停止运算放大器的过程。图37.7显示了每个寄存器设置的示例。



Note: 有关稳定等待时间的详细信息，请参阅第48节，电气特性

Figure 37.7 在软件触发模式下启动和停止OPAMP的程序

37.5 Activation Trigger Mode

This section describes the procedure to activate the operational amplifier using an activation trigger and to stop the amplifier with software. Figure 37.8 shows an example of each register setting.

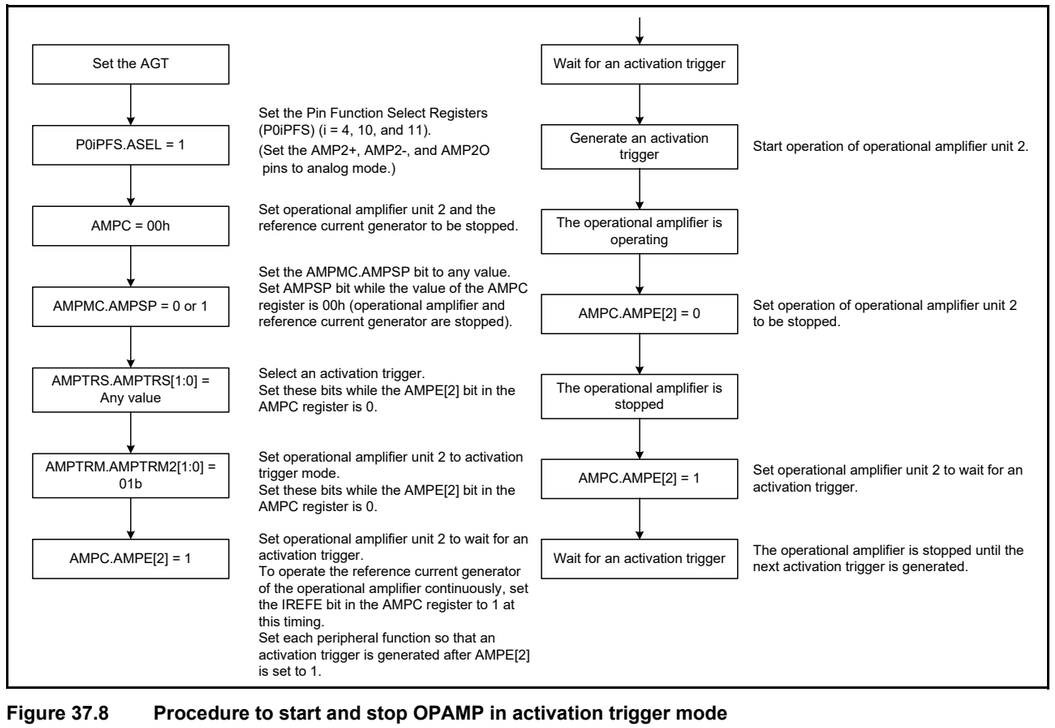


Figure 37.8 Procedure to start and stop OPAMP in activation trigger mode

37.5 激活触发模式

本节介绍使用激活触发器激活运算放大器和使用软件停止放大器的过程。图37.8显示了每个寄存器设置的示例。

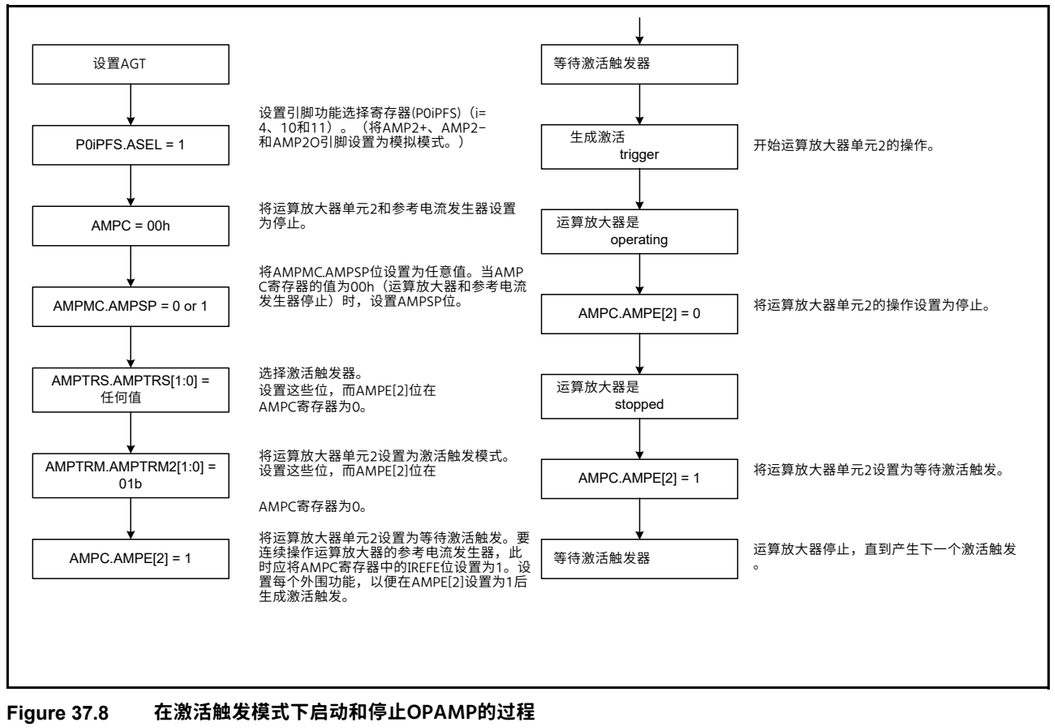


Figure 37.8 在激活触发模式下启动和停止OPAMP的过程

37.6 Activation and A/D Trigger Mode

This section describes the procedure to activate the operational amplifier using an activation trigger and to stop the amplifier with an A/D conversion end trigger. Figure 37.9 shows an example of each register setting.

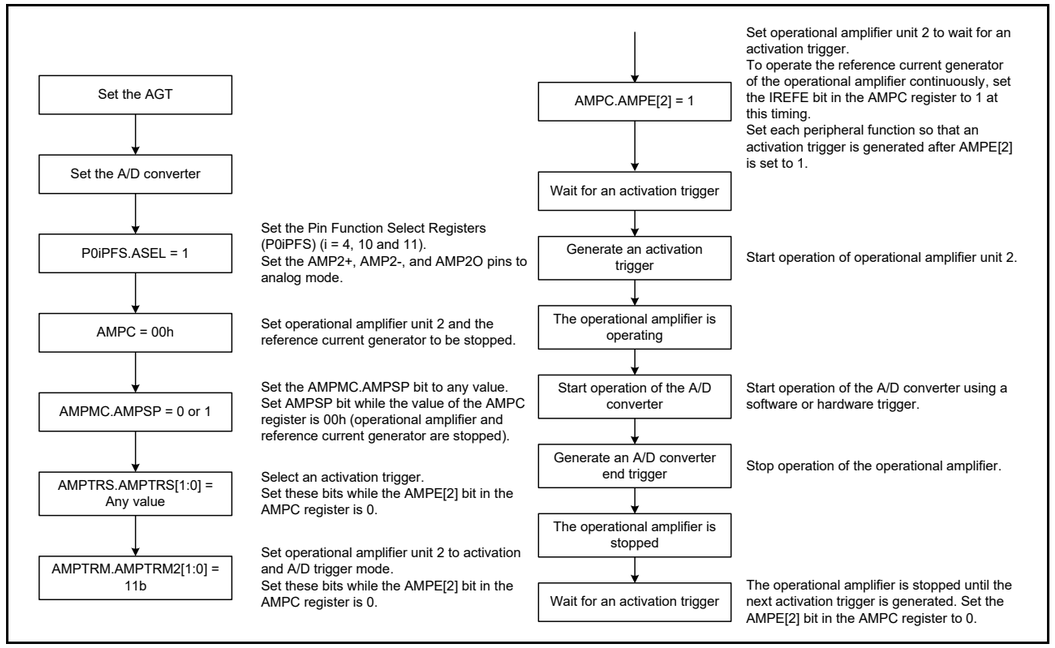


Figure 37.9 Procedure to activate the operational amplifier using an activation trigger and to stop the operational amplifier with an A/D conversion end trigger

37.7 Usage Notes

In addition to the AMPC register settings, the operational amplifier function can be activated by an activation trigger and stopped at the end of the A/D conversion. The reference current circuit can be stopped at the end of the A/D conversion. Application sequences must prevent these asynchronous triggers from causing conflicts between the activation and stop control.

Do not perform A/D conversion on pins that are used for the positive and negative input of the operational amplifier because these pins are multiplexed with analog input for the A/D converter.

37.6 激活和AD触发模式

本节介绍使用激活触发器激活运算放大器和使用AD转换结束触发器停止放大器的步骤。图37.9显示了每个寄存器设置的示例。

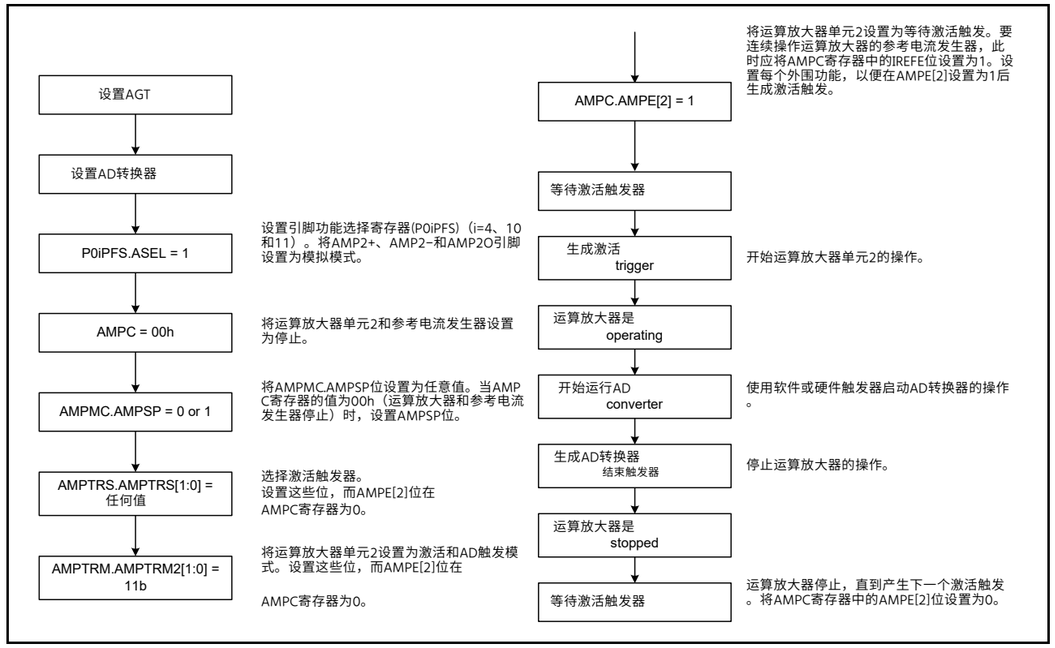


Figure 37.9 使用激活触发器激活运算放大器和使用A/D转换结束触发器停止运算放大器的过程

37.7 使用说明

除了AMPC寄存器设置之外，运算放大器功能还可以通过激活触发器激活，并在AD转换结束时停止。参考电流电路可以在AD转换结束时停止。应用程序序列必须防止这些异步触发器导致激活和停止控制之间的冲突。

不要在用于运算放大器正负输入的引脚上执行AD转换，因为这些引脚与AD转换器的模拟输入复用。

38. Low Power Analog Comparator (ACMPLP)

38.1 Overview

The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage with an analog input voltage. Comparator channels ACMPLP0 and ACMPLP1 are independent of each other.

The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from an input to the CMPREFi (i = 0, 1) pin, an output from the internal 8-bit D/A converter, and the internal reference voltage (Vref) generated internally in the MCU.

The ACMPLP response speed can be set before starting an operation. Setting High-speed mode decreases the response delay time, but increases current consumption. Setting Low-speed mode increases the response delay time, but decreases current consumption.

Table 38.1 lists the ACMPLP specifications, Figure 38.1 shows a block diagram of the ACMPLP when the window function is disabled, and Figure 38.2 shows a block diagram of the ACMPLP when the window function is enabled. Table 38.2 lists the I/O pins of the ACMPLP.

Table 38.1 ACMPLP specifications

Parameter	Specifications
Number of channels	2 channels: ACMPLP0 and ACMPLP1
Analog input voltage	Input from CMPINi (i = 0, 1) pin
Reference voltage	• Standard mode One of the following can be selected: - Internal reference voltage (Vref) - Input from CMPREFi (i = 0, 1) pin - Output from internal 8-bit D/A converter. • Window mode One of the following can be selected: - Input from CMPREFi (i = 0, 1) pin (CMPREF0: low reference, CMPREF1: high reference) - Output from internal 8-bit D/A converter.
Comparator output	• Comparison result • Generation of ELC event output • Monitor output from register.
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Rising edge, falling edge, or both edges can be selected.
Selectable functions	• Noise filter function - One of three sampling frequencies can be selected - Not using the filter function can be selected. • Window function - Window function is used or not used can be selected. • Low-Power Analog Comparator response speed - High-speed mode or low-speed mode can be selected.

38. 低功耗模拟比较器(ACMPLP)

38.1 Overview

低功耗模拟比较器(ACMPLP)将参考输入电压与模拟输入电压进行比较。
比较器通道ACMPLP0和ACMPLP1相互独立。

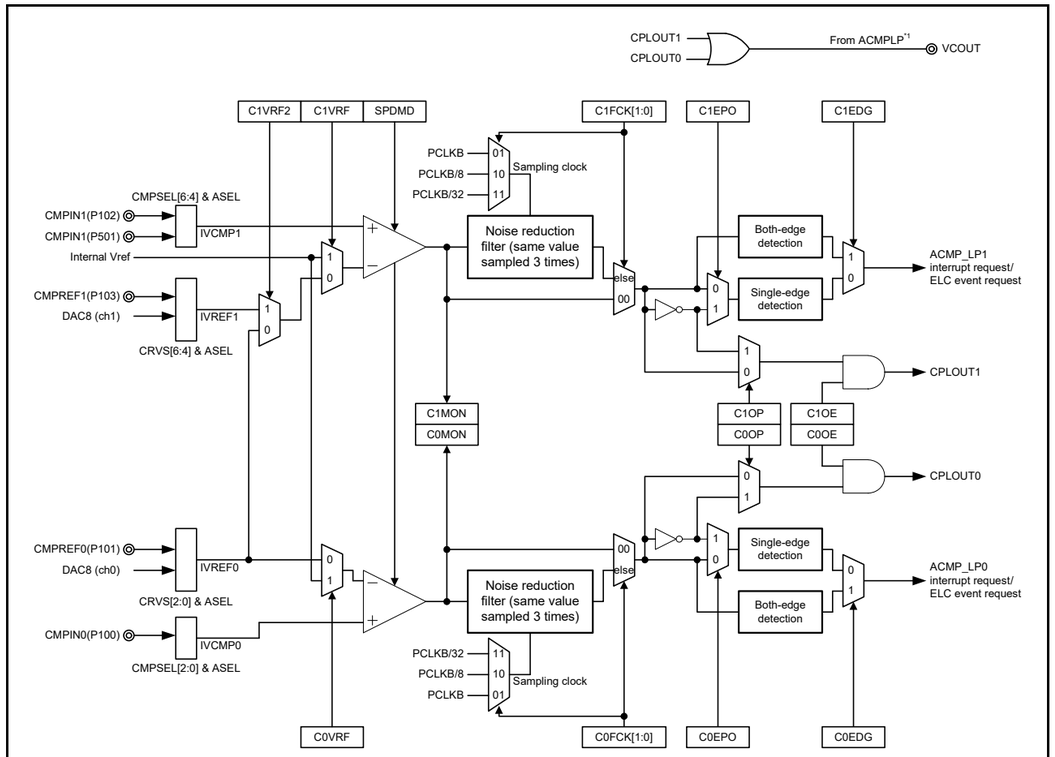
参考输入电压和模拟输入电压的比较结果可以通过软件读取。比较结果也可以对外输出。参考输入电压可以从CMPREFi(i=0 1)引脚的输入、内部8位DA转换器的输出以及MCU内部生成的内部参考电压(Vref)中选择。

可以在开始操作之前设置ACMPLP响应速度。设置高速模式会减少响应延迟时间，但会增加电流消耗。设置低速模式会增加响应延迟时间，但会降低电流消耗。

表38.1列出了ACMPLP规范，图38.1显示了禁用窗口功能时的ACMPLP框图，图38.2显示了启用窗口功能时的ACMPLP框图。表38.2列出了ACMPLP的IO引脚。

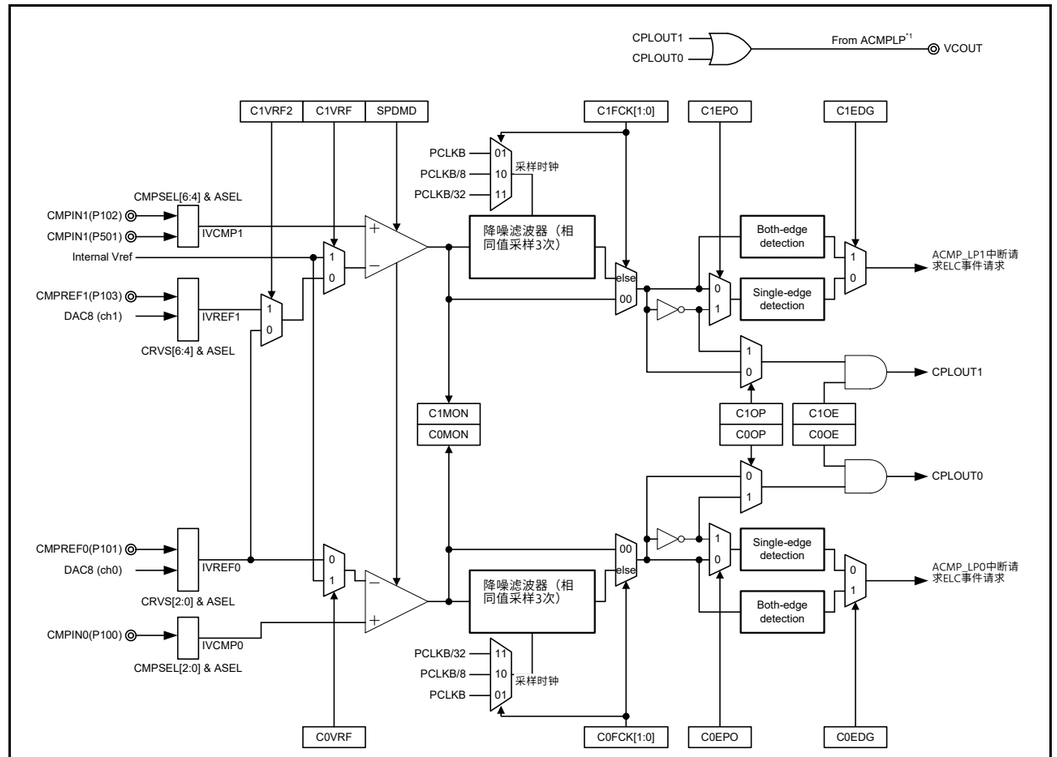
Table 38.1 ACMPLP specifications

Parameter	Specifications
通道数	2 channels: ACMPLP0 and ACMPLP1
模拟输入电压	来自CMPINi(i=0 1)引脚的输入
参考电压	标准模式 可以选择以下之一：内部参考电压(Vref)来自CMPREFi(i=0 1)引脚的输入从内部8位DA转换器输出。 窗口模式 可以选择以下之一：从CMPREFi(i=0 1)引脚输入（CMPREF0：低参考，CMPREF1：高参考）从内部8位DA转换器输出。
比较器输出	比较结果 生成ELC事件输出 监控寄存器的输出。
中断请求信号	从比较结果中检测到有效边沿时产生中断请求 可以选择上升沿、下降沿或两个沿。
可选择的功能	噪音过滤功能 可以选择三个采样频率之一可以选择不使用滤波器功能。 窗口功能 可以选择使用或不使用窗口功能。 低功耗模拟比较器响应速度 可选择高速模式或低速模式。



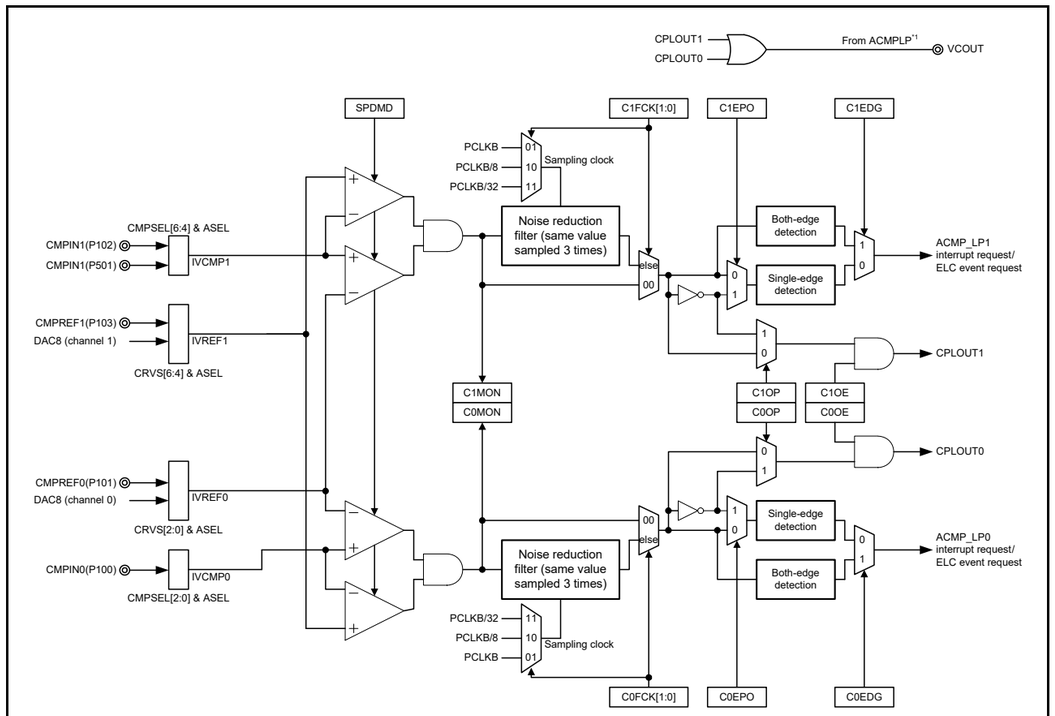
Note 1. ACMPLP results are output to the VCOUT pin.

Figure 38.1 ACMPLP block diagram when window function is disabled



Note 1. ACMPLP结果输出到VCOUT引脚。

Figure 38.1 禁用窗口功能时的ACMPLP框图



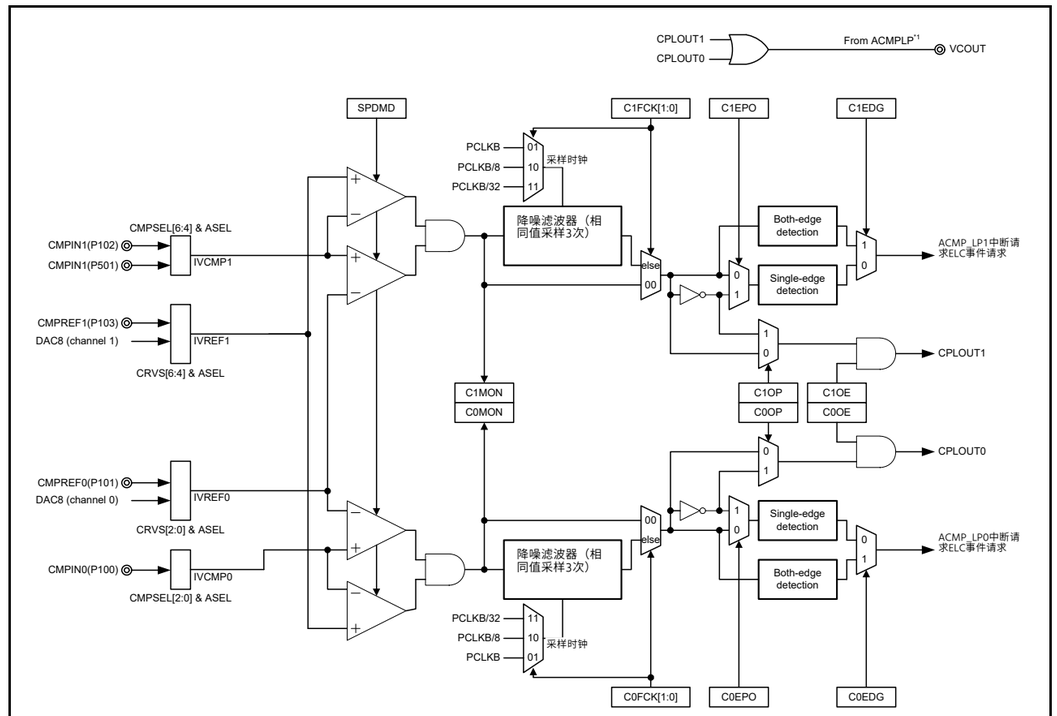
Note 1. ACMPLP results are output to the VCOUT pin.

Figure 38.2 ACMPLP block diagram when window function is enabled

Table 38.2 Comparator pin configuration

Comparator	Reference voltage input pin		Analog voltage input pin		Output pin
	Standard mode	Window function mode	Standard mode	Window function mode	
ACMPLP0	• IVREF0 (CMPREF0 (P101)/DAC8 (channel 0)) • Internal Vref (Selectable)	Low reference voltage: • IVREF0 (CMPREF0(P101)/ DAC8 (channel 0)) High reference voltage: • IVREF1 (CMPREF1 (P103)/DAC8 (channel 1))	• IVCMP0 (CMPIN0 (P100)		VCOUT*1
ACMPLP1	• IVREF0 (CMPREF0(P101)/ DAC8 (channel 0)) • IVREF1 (CMPREF1 (P103)/DAC8 (channel 1)) • Internal Vref (Selectable)		• IVCMP1 (CMPIN1 (P102)/CMPIN1 (P501)		

Note 1. ACMPLP0 and ACMPLP1 compare outputs are output to the VCOUT pin.



Note 1. ACMPLP结果输出到VCOUT引脚。

Figure 38.2 启用窗口功能时的ACMPLP框图

Table 38.2 比较器引脚配置

Comparator	参考电压输入引脚		模拟电压输入引脚		输出引脚
	标准模式	窗口功能模式	标准模式	窗口功能模式	
ACMPLP0	• IVREF0 (CMPREF0 (P101)/DAC8 (channel 0)) • Internal Vref (Selectable)	低参考电压： IVREF0(CMPREF0(P101)DAC8(通道0)) 高参考电压： IVREF1(CMPREF1 (P103)/DAC8 (channel 1))	• IVCMP0 (CMPIN0 (P100)		VCOUT*1
ACMPLP1	• IVREF0 (CMPREF0(P101)/ DAC8 (channel 0)) • IVREF1 (CMPREF1 (P103)/DAC8 (channel 1)) • Internal Vref (Selectable)		• IVCMP1 (CMPIN1 (P102)/CMPIN1 (P501)		

Note 1. ACMPLP0和ACMPLP1比较输出输出到VCOUT引脚。

38.2 Register Descriptions

38.2.1 ACMPLP Mode Setting Register (COMPMDR)

Address(es): ACMPLP.COMPMDR 4008 5E00h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	C0ENB	ACMPLP0 Operation Enable	0: Disable comparator channel ACMPLP0 1: Enable comparator channel ACMPLP0.	R/W
b1	C0WDE	ACMPLP0 Window Function Mode Enable*1,*2,*6	0: Disable window function for ACMPLP0 1: Enable window function for ACMPLP0.	R/W
b2	C0VRF	ACMPLP0 Reference Voltage Selection*6	0: IVREF0 1: Internal reference voltage (Vref).*4	R/W
b3	C0MON	ACMPLP0 Monitor Flag*3	When the window function is disabled: 0: IVCMP0 < ACMPLP0 reference voltage 1: IVCMP0 > ACMPLP0 reference voltage. When the window function is enabled: 0: IVCMP0 < IVREF0 or IVCMP0 > IVREF1 1: IVREF0 < IVCMP0 < IVREF1.	R
b4	C1ENB	ACMPLP1 Operation Enable	0: Disable ACMPLP1 operation 1: Enable ACMPLP1 operation.	R/W
b5	C1WDE	ACMPLP1 Window Function Mode Enable*1,*2,*5	0: Disable ACMPLP1 window function mode 1: Enable ACMPLP1 window function mode.	R/W
b6	C1VRF	ACMPLP1 Reference Voltage Selection*5	0: IVREF0 or IVREF1 1: Internal reference voltage (Vref).*4	R/W
b7	C1MON	ACMPLP1 Monitor Flag*3	When the window function is disabled: 0: IVCMP1 < ACMPLP1 reference voltage 1: IVCMP1 > ACMPLP1 reference voltage. When the window function is enabled: 0: IVCMP1 < IVREF0 or IVCMP1 > IVREF1 1: IVREF0 < IVCMP1 < IVREF1.	R

Note 1. Window function mode cannot be set when Low-speed mode is selected (the SPDMD bit in the COMPOCR register is 0).
Note 2. In window function mode, the reference voltage in the comparator is selected regardless of the setting of this bit.
Note 3. The initial value is 0 immediately after a reset is released. However, the value is undefined when C0ENB is set to 0 and C1ENB is set to 0 after operation of the comparator is enabled once.
Note 4. The setting is valid only when in standard mode. When in window function mode, IVREF0 or IVREF1 is selected regardless of the setting of this bit.
Note 5. To change C1WDE and C1VRF, the CRV[6:4] and CRV[2:0] bits must be 000b.
Note 6. To change C0WDE and C0VRF, the CRV[2:0] bits must be 000b.

38.2 注册说明

38.2.1 ACMPLP模式设置寄存器(COMPMDR)

Address(es): ACMPLP.COMPMDR 4008 5E00h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	C0ENB	ACMPLP0操作使能	0：禁用比较器通道ACMPLP01：启用比较器通道ACMPLP0。	R/W
b1	C0WDE	ACMPLP0窗口函数模式 Enable*1,*2,*6	0：禁用ACMPLP0的窗口功能1：启用ACMPLP0的窗口功能。	R/W
b2	C0VRF	ACMPLP0参考电压 Selection*6	0：IVREF01：内部参考电压（Vref）。*4	R/W
b3	C0MON	ACMPLP0 Monitor Flag*3	当窗口功能被禁用时： 0：IVCMP0<ACMPLP0参考电压1：IVCMP0>ACMPLP0参考电压。启用窗口功能时： 0: IVCMP0 < IVREF0 or IVCMP0 > IVREF1 1: IVREF0 < IVCMP0 < IVREF1.	R
b4	C1ENB	ACMPLP1操作使能	0：禁止ACMPLP1操作1：使能ACMPLP1操作。	R/W
b5	C1WDE	ACMPLP1窗口函数模式 Enable*1,*2,*5	0：禁用ACMPLP1窗口功能模式1：启用ACMPLP1窗口功能模式。	R/W
b6	C1VRF	ACMPLP1参考电压 Selection*5	0：IVREF0或IVREF11：内部参考电压(Vref)。*4	R/W
b7	C1MON	ACMPLP1 Monitor Flag*3	当窗口功能被禁用时： 0：IVCMP1<ACMPLP1参考电压1：IVCMP1>ACMPLP1参考电压。启用窗口功能时： 0: IVCMP1 < IVREF0 or IVCMP1 > IVREF1 1: IVREF0 < IVCMP1 < IVREF1.	R

Note 1. 选择低速模式时（COMPOCR寄存器中的SPDMD位为0）不能设置窗口功能模式。
Note 2. 在窗口函数模式下，无论该位的设置如何，都会选择比较器中的参考电压。
Note 3. 释放复位后，初始值为0。然而，当C0ENB设置为0且C1ENB设置为0后，比较器的操作使能一次后，该值未定义。
Note 4. 该设置仅在标准模式下有效。在窗口功能模式下，无论该位的设置如何，都会选择IVREF0或IVREF1。
Note 5. 要更改C1WDE和C1VRF，CRV[6:4]和CRV[2:0]位必须为000b。
Note 6. 要更改C0WDE和C0VRF，CRV[2:0]位必须为000b。

38.2.2 ACMPLP Filter Control Register (COMPFIR)

Address(es): ACMPLP.COMPFIR 4008 5E01h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1EDG	C1EPO	C1FCK[1:0]		C0EDG	C0EPO	C0FCK[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	C0FCK[1:0]	ACMPLP0 Filter Select*1	b1 b0 0 0: No Sampling (bypass) 0 1: Sampling at PCLKB 1 0: Sampling at PCLKB/8 1 1: Sampling at PCLKB/32.	R/W
b2	C0EPO	ACMPLP0 Edge Polarity Switching*1	0: Interrupt and ELC event request on the rising edge 1: Interrupt and ELC event request on the falling edge.	R/W
b3	C0EDG	ACMPLP0 Edge Detection Selection*1	0: Interrupt and ELC event request by one-edge detection 1: Interrupt and ELC event request by both-edge detection.	R/W
b5, b4	C1FCK[1:0]	ACMPLP1 Filter Select*1	b5 b4 0 0: No Sampling (bypass) 0 1: Sampling at PCLKB 1 0: Sampling at PCLKB/8 1 1: Sampling at PCLKB/32.	R/W
b6	C1EPO	ACMPLP1 Edge Polarity Switching*1	0: Interrupt and ELC event request on the rising edge 1: Interrupt and ELC event request on the falling edge.	R/W
b7	C1EDG	ACMPLP1 Edge Detection Selection*1	0: Interrupt and ELC event request by one-edge detection 1: Interrupt and ELC event request by both-edge detection.	R/W

Note 1. If bits CiFCK[1:0], CiEPO, and CiEDG (i = 0, 1) are changed, an ACMPLP interrupt request and an ELC event request can be generated. Change these bits only after setting event link to deselect. Also, be sure to clear the associated interrupt request flag.

38.2.3 ACMPLP Output Control Register (COMPOCR)

Address(es): ACMPLP.COMPOCR 4008 5E02h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPDMD	C1OP	C1OE	—	—	C0OP	C0OE	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	C0OE	ACMPLP0 VCOUT Pin Output Enable*1	0: Disable ACMPLP0 VCOUT pin output 1: Enable ACMPLP0 VCOUT pin output.	R/W
b2	C0OP	ACMPLP0 VCOUT Output Polarity Selection*1	0: Non-inverted 1: Inverted.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	C1OE	ACMPLP1 VCOUT Pin Output Enable*1	0: Disable ACMPLP1 VCOUT pin output 1: Enable ACMPLP1 VCOUT pin output.	R/W
b6	C1OP	ACMPLP1 VCOUT Output Polarity Selection*1	0: Non-inverted 1: Inverted.	R/W
b7	SPDMD	ACMPLP0/ACMPLP1 Speed Selection*2	0: Select comparator Low-speed mode 1: Select comparator High-speed mode.	R/W

38.2.2 ACMPLP滤波器控制寄存器(COMPFIR)

Address(es): ACMPLP.COMPFIR 4008 5E01h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1EDG	C1EPO	C1FCK[1:0]		C0EDG	C0EPO	C0FCK[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	C0FCK[1:0]	ACMPLP0 Filter Select*1	b1b000：无采样（旁路）01：在PCLKB1采样0：在PCLKB8采样11：在PCLKB32采样。	R/W
b2	C0EPO	ACMPLP0边缘极性Switching*1	0：上升沿中断和ELC事件请求1：下降沿中断和ELC事件请求。	R/W
b3	C0EDG	ACMPLP0边缘检测Selection*1	0：通过单边沿检测请求中断和ELC事件1：通过双沿检测请求中断和ELC事件。	R/W
b5, b4	C1FCK[1:0]	ACMPLP1 Filter Select*1	b5b400：无采样（旁路）01：在PCLKB1采样0：在PCLKB8采样11：在PCLKB32采样。	R/W
b6	C1EPO	ACMPLP1边缘极性Switching*1	0：上升沿中断和ELC事件请求1：下降沿中断和ELC事件请求。	R/W
b7	C1EDG	ACMPLP1边缘检测Selection*1	0：通过单边沿检测请求中断和ELC事件1：通过双沿检测请求中断和ELC事件。	R/W

Note 1. 如果位CiFCK[1:0]、CiEPO和CiEDG(i=0 1)发生变化，则会产生ACMPLP中断请求和ELC事件请求。仅在将事件链接设置为取消选择后更改这些位。此外，请务必清除相关的中断请求标志。

38.2.3 ACMPLP输出控制寄存器(COMPOCR)

Address(es): ACMPLP.COMPOCR 4008 5E02h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPDMD	C1OP	C1OE	—	—	C0OP	C0OE	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	C0OE	ACMPLP0VCOUT引脚输出Enable*1	0：禁止ACMPLP0VCOUT引脚输出1：使能ACMPLP0VCOUT引脚输出。	R/W
b2	C0OP	ACMPLP0VCOUT输出极性Selection*1	0: Non-inverted 1: Inverted.	R/W
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	C1OE	ACMPLP1VCOUT引脚输出Enable*1	0：禁止ACMPLP1VCOUT引脚输出1：使能ACMPLP1VCOUT引脚输出。	R/W
b6	C1OP	ACMPLP1VCOUT输出极性Selection*1	0: Non-inverted 1: Inverted.	R/W
b7	SPDMD	ACMPLP0/ACMPLP1 Speed Selection*2	0：选择比较器低速模式1：选择比较器高速模式。	R/W

Note 1. ACMPLP0 and ACMPLP1 result outputs are output to the VCOUT pin.
Note 2. Set the CiENB bit (i = 0, 1) in the COMPMDR register to 0 before rewriting the SPDMD bit.

38.2.4 Comparator Input Select Register (COMPSEL0)

Address(es): ACMPLP.COMPSEL0 4008 5E04h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	CMPSEL[6:4]			—	CMPSEL[2:0]		
Value after reset:	0	0	0	1	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CMPSEL[2:0]	ACMPLP0 Input (IVCMP0) Selection*1	b2 b0 0 0 0: No input 0 0 1: CMPIN0 (P100) Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CMPSEL[6:4]	ACMPLP1 Input (IVCMP1) Selection*2	b6 b4 0 0 0: No input 0 0 1: CMPIN1 (P102) 1 0 0: CMPIN1 (P501) Other settings are prohibited.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Writing a value other than 000b is prohibited while CMPSEL[2:0] is not 000b.
Note 2. Writing a value other than 000b is prohibited while CMPSEL[6:4] is not 000b.

38.2.5 Comparator Reference Voltage Select Register (COMPSEL1)

Address(es): ACMPLP.COMPSEL1 4008 5E05h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1VRF2	CRVS[6:4]			—	CRVS[2:0]		
Value after reset:	1	0	0	1	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CRVS[2:0]	ACMPLP0 Reference Voltage (IVREF0) Selection*1	b2 b0 0 0 0: No input 0 0 1: CMPREF0 (P101) 0 1 0: DAC8 (channel 0) output Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b04	CRVS[6:4]	ACMPLP1 Reference Voltage (IVREF1) Selection*2	b6 b4 0 0 0: No input 0 0 1: CMPREF1 (P103) 0 1 0: DAC8 (channel 1) output Other settings are prohibited.	R/W
b7	C1VRF2	ACMPLP1 Reference Voltage Selection 2*3	0: IVREF0 selected 1: IVREF1 selected.	R/W

Note 1. Writing a value other than 000b is prohibited while CRVS[2:0] is not 000b.
Note 2. Writing a value other than 000b is prohibited while CRVS[6:4] is not 000b.
Note 3. To change C1VRF2, bits CRVS[6:4] and CRVS[2:0] must be 000b.

Note 1. ACMPLP0和ACMPLP1结果输出输出到VCOUT引脚。
Note 2. 在重写SPDMD位之前，将COMPMDR寄存器中的CiENB位(i=0 1)设置为0。

38.2.4 比较器输入选择寄存器(COMPSEL0)

Address(es): ACMPLP.COMPSEL0 4008 5E04h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	CMPSEL[6:4]			—	CMPSEL[2:0]		
重置后的值：	0	0	0	1	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	CMPSEL[2:0]	ACMPLP0 Input (IVCMP0) Selection*1	b2 b0 0 00：无输入 001：CMPIN0(P100)禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	CMPSEL[6:4]	ACMPLP1 Input (IVCMP1) Selection*2	b6 b4 0 00：无输入 0 0 1: CMPIN1 (P102) 100：CMPIN1(P501)禁止其他设置。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 当CMPSEL[2:0]不是000b时，禁止写入000b以外的值。
Note 2. 当CMPSEL[6:4]不是000b时，禁止写入000b以外的值。

38.2.5 比较器参考电压选择寄存器(COMPSEL1)

Address(es): ACMPLP.COMPSEL1 4008 5E05h

	b7	b6	b5	b4	b3	b2	b1	b0
	C1VRF2	CRVS[6:4]			—	CRVS[2:0]		
重置后的值：	1	0	0	1	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	CRVS[2:0]	ACMPLP0参考电压(IVREF0)选择*1	b2 b0 0 00：无输入 0 0 1: CMPREF0 (P101) 010：DAC8（通道0）输出禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b04	CRVS[6:4]	ACMPLP1参考电压(IVREF1)选择*2	b6 b4 0 00：无输入 0 0 1: CMPREF1 (P103) 010：DAC8（通道1）输出禁止其他设置。	R/W
b7	C1VRF2	ACMPLP1参考电压 Selection 2*3	0: IVREF0 selected 1: IVREF1 selected.	R/W

Note 1. 当CRVS[2:0]不是000b时，禁止写入000b以外的值。
Note 2. 当CRVS[6:4]不是000b时，禁止写入000b以外的值。
Note 3. 要更改C1VRF2，位CRVS[6:4]和CRVS[2:0]必须为000b。

38.3 Operation

ACMPLP0 and ACMPLP1 operate independently, and their operations are the same. Operation is not guaranteed when the values of their associated registers are changed during the comparator operation. Table 38.3 shows the procedure for setting the ACMPLP registers.

Table 38.3 Procedure for setting the ACMPLP associated registers (i = 0, 1)

Step	Register	Bit	Setting	
1	MSTPCRD	MSTPD29	0: Input clock supply.	
2	Corresponding Port mn Pin Function Select Register (PmnPFS)	ASEL	Select the analog input.	
	COMPSEL0	CMPSEL[2:0], CMPSEL[6:4]		
3	COMPOCR	SPDMD	Select the comparator response speed 0: Low-speed mode 1: High-speed mode.*1	
4	COMPMDR	CiWDE	0: Disable window function mode	1: Enable window function mode.*2
		CiVRF*5	Select the reference voltage.	Window comparator operation (reference = IVREF0 and IVREF1*3).
	COMPSEL1	CRVS[2:0], CRVS[6:4], C1VRF2		
	COMPMDR	CiENB	1: Operation enabled.	
5	Waiting for the comparator stabilization time T_{cmp} (minimum 100 µs).			
6	COMPFIR	CiFCK[1:0]	Select whether the digital filter is used or not and the sampling clock.	
		CiEPO, CiEDG	Select the edge detection condition for an interrupt request (rising edge/ falling edge/both edges).	
7	COMPOCR	CiOP, CiOE	Set the VCOUT output (select the polarity and set output enabled or disabled).	
	Corresponding Port mn Pin Function Select Register (PmnPFS)	PSEL, PMR	Select the VCOUT port function.	
8	IELSRn	IR, IELS[7:0]	When using an interrupt: select the interrupt status flag, ICU event link select.*3	
9	ELSRn	ELS[7:0]	When using an ELC: Select the Event Link Select.*4	
10	Operation started			

Note 1. ACMPLP0 and ACMPLP1 cannot be set independently.
Note 2. Can only be set in High-speed mode (SPDMD = 1).
Note 3. After the comparator setting, an unnecessary interrupt might occur until operation becomes stable, so initialize the interrupt flag.
Note 4. After the comparator setting, an unnecessary interrupt might occur until operation becomes stable, so initialize the event link select.
Note 5. To change to internal reference voltage (Vref), follow the procedure in section 38.2.1, ACMPLP Mode Setting Register (COMPMDR).

Figure 38.3 shows an operating example of the ACMPLPi (i = 0, 1) when window function is disabled. The reference input voltage (IVREFi) or internal reference voltage (Vref) and the analog input voltage (IVCMPi) are compared as follows:

- If the analog input voltage is higher than the reference input voltage, the COMPMDR.CiMON bit is set to 1
- If the analog input voltage is lower than the reference input voltage, the CiMON bit is set to 0.

ACMPLPi outputs an interrupt to the ICU. For details on the interrupt, see section 38.5, ACMPLP Interrupts. ACMPLPi also outputs an event signal to the ELC to activate other modules. For details on the ELC, see section 38.6, ELC Event Output. Do not change the values of the registers during the comparison.

38.3 Operation

ACMPLP0和ACMPLP1独立运行，操作相同。如果在比较器操作期间其相关寄存器的值发生变化，则无法保证操作。表38.3显示了设置ACMPLP寄存器的过程。

Table 38.3 设置ACMPLP相关寄存器的过程(i=0 1)

Step	Register	Bit	Setting	
1	MSTPCRD	MSTPD29	0：输入时钟电源。	
2	对应端口mn 引脚功能选择寄存器(PmnPFS)	ASEL	选择模拟输入。	
	COMPSEL0	CMPSEL[2:0], CMPSEL[6:4]		
3	COMPOCR	SPDMD	选择比较器响应速度0：低速模式1：高速模式。*1	
4	COMPMDR	CiWDE	0：禁用窗口功能模式	1：启用窗口功能模式。*2
		CiVRF*5	选择参考电压。	窗口比较器操作（参考=IVREF0和IVREF1*3）。
	COMPSEL1	CRVS[2:0], CRVS[6:4], C1VRF2		
	COMPMDR	CiENB	1：操作使能。	
5	等待比较器稳定时间Tcmp（最小100µs）。			
6	COMPFIR	CiFCK[1:0]	选择是否使用数字滤波器和采样时钟。	
		CiEPO, CiEDG	选择中断请求的边沿检测条件（上升沿下降沿两个沿）。	
7	COMPOCR	CiOP, CiOE	设置VCOUT输出（选择极性并设置输出启用或禁用）。	
	对应端口mn 引脚功能选择寄存器(PmnPFS)	PSEL, PMR	选择VCOUT端口功能。	
8	IELSRn	IR, IELS[7:0]	使用中断时：选择中断状态标志，ICU事件链接选择。*3	
9	ELSRn	ELS[7:0]	使用ELC时：选择EventLinkSelect。*4	
10	操作开始			

Note 1. ACMPLP0和ACMPLP1不能单独设置。
Note 2. 只能在高速模式下设置(SPDMD=1)。
Note 3. 比较器设置后，在运行稳定之前可能会发生不必要的中断，因此请初始化中断标志。
Note 4. 比较器设置后，在运行稳定之前可能会发生不必要的中断，因此请初始化事件链接选择。
Note 5. 要更改为内部参考电压(Vref)，请按照第38.2.1节，ACMPLP模式设置寄存器(COMPMDR)中的程序进行操作。

图38.3显示了禁用窗口功能时ACMPLPi(i=0 1)的操作示例。参考输入电压(IVREFi)或内部参考电压(Vref)与模拟输入电压(IVCMPi)的比较如下：

- 如果模拟输入电压高于参考输入电压，则COMPMDR.CiMON位设置为1
- 如果模拟输入电压低于参考输入电压，则CiMON位设置为0。

ACMPLPi向ICU输出中断。有关中断的详细信息，请参见第38.5节，ACMPLP中断。ACMPLPi还向ELC输出事件信号以激活其他模块。有关ELC的详细信息，请参阅第38.6节，ELC事件输出。在比较期间不要更改寄存器的值。

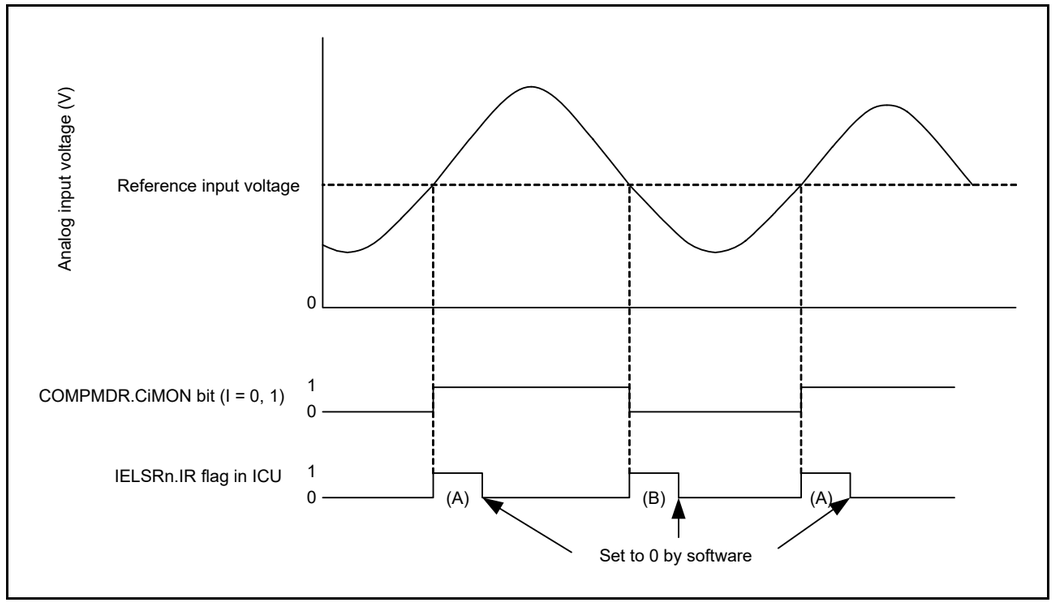


Figure 38.3 Operating example of ACMPLPi (i = 0, 1) when window function is disabled

Figure 38.3 applies when the following conditions are met:

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- When CiEDG = 0 and CiEPO = 0 (rising edge), IELSRn.IR changes as shown by (A) only
- When CiEDG = 0 and CiEPO = 1 (falling edge), IELSRn.IR changes as shown by (B) only.

Figure 38.4 shows an operation example of ACMPLPi (i = 0, 1) when the window function is enabled.

The reference voltage (IVREF0/IVREF1) and the analog input voltage are compared. The CiMON bit:

- Is set to 1 when IVREF0 < the analog input voltage < IVREF1
- Is set to 0 when the analog input voltage < IVREF0 or IVREF1 < the analog input voltage.

ACMPLPi outputs an interrupt to the ICU. For details on the interrupt, see section 38.5, ACMPLP Interrupts. ACMPLPi also outputs an event signal to the ELC to activate other modules. For details on the ELC, see section 38.6, ELC Event Output. Do not change the values of the registers during the comparison.

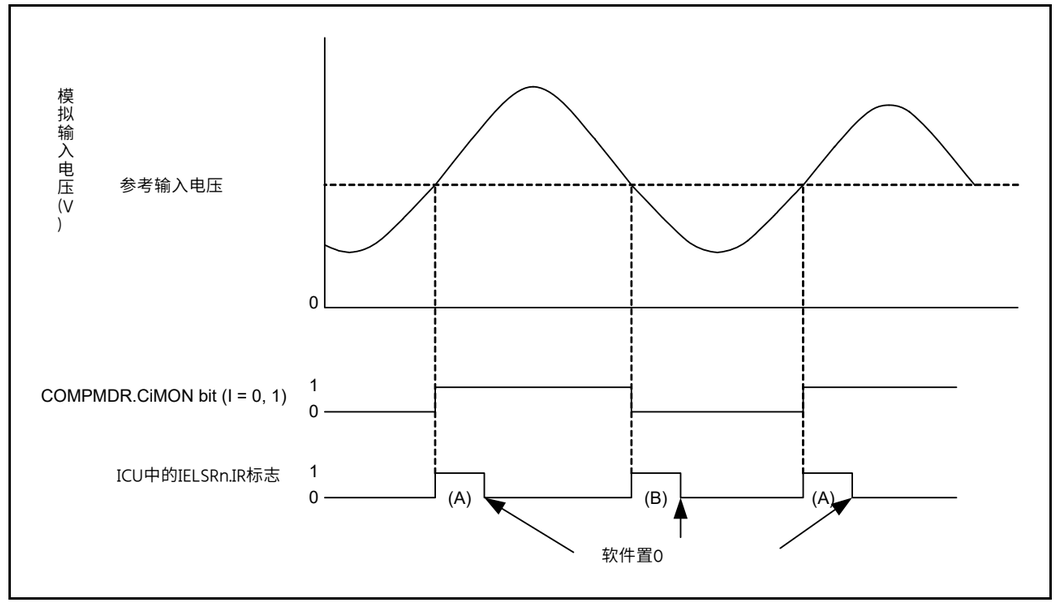


Figure 38.3 禁用窗口功能时ACMPLPi(i=0 1)的操作示例

当满足以下条件时，适用图38.3：

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- 当CiEDG=0且CiEPO=0（上升沿）时，IELSRn.IR仅如(A)所示变化
- 当CiEDG=0且CiEPO=1（下降沿）时，IELSRn.IR仅如(B)所示变化。

图38.4显示了启用窗口功能时ACMPLPi(i=0 1)的操作示例。

比较参考电压(IVREF0IVREF1)和模拟输入电压。CiMON位：

- 当IVREF0<模拟输入电压<IVREF1时设置为1
- 当模拟输入电压<IVREF0或IVREF1<模拟输入电压时设置为0。

ACMPLPi向ICU输出中断。有关中断的详细信息，请参见第38.5节，ACMPLP中断。ACMPLPi还向ELC输出事件信号以激活其他模块。有关ELC的详细信息，请参阅第38.6节，ELC事件输出。在比较期间不要更改寄存器的值。

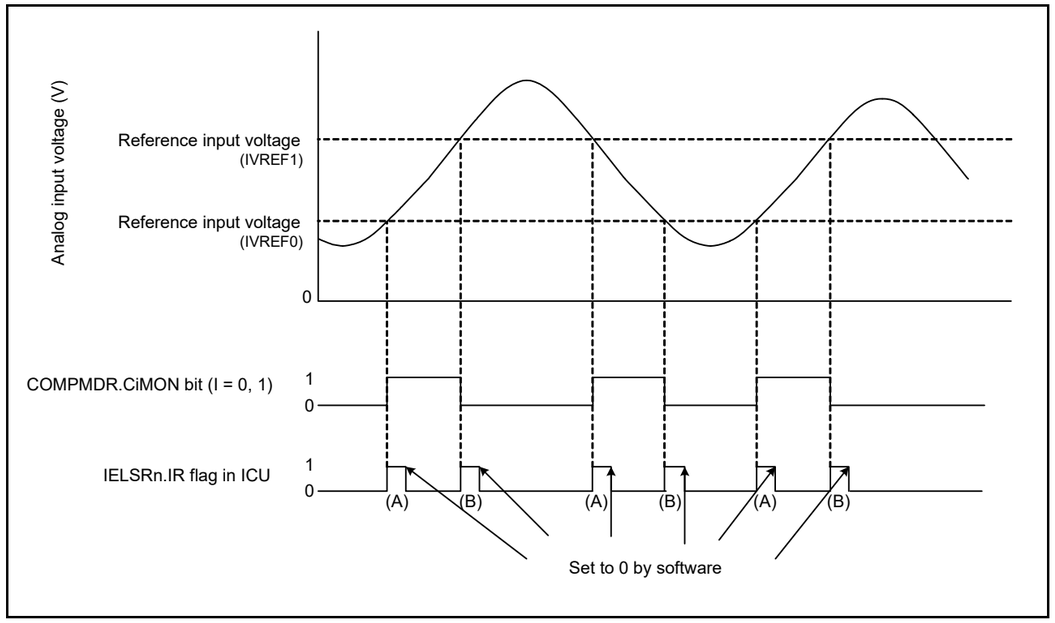


Figure 38.4 Operating example of ACMPLPi (i = 0, 1) when window function is enabled

Figure 38.4 applies when the following conditions are met:

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- When CiEDG = 0 and CiEPO = 0 (rising edge), IELSRn.IR changes as shown by (A) only
- When CiEDG = 0 and CiEPO = 1 (falling edge), IELSRn.IR changes as shown by (B) only.

38.4 Noise Filter

Figure 38.5 shows the configuration of the ACMPLPi noise filter, and Figure 38.6 shows an operating example of the ACMPLPi noise filter.

The sampling clock can be selected in the COMPFIR.CiFCK[1:0] bits. The ACMP_LPi signal (internal signal) output from ACMPLPi is sampled at every sampling clock cycle. When the level matches three times, the corresponding IELSRn.IR bit is set to 1 (interrupt requested) and an ELC event is output.

When using an interrupt in Software Standby mode, set the COMPFIR.CiFCK[1:0] bits to 00b (bypass).

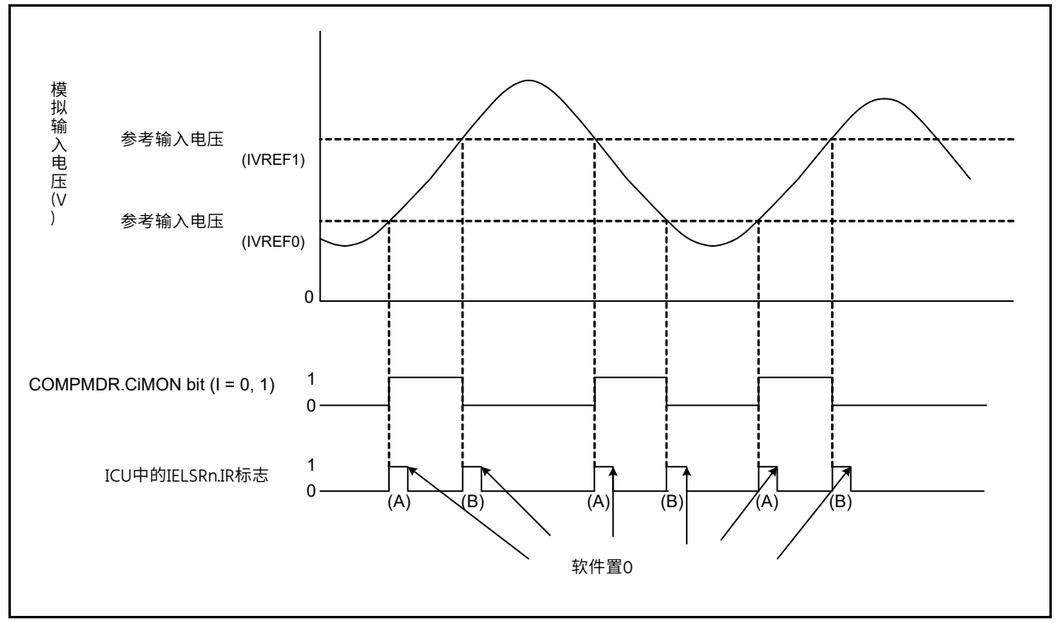


Figure 38.4 启用窗口功能时ACMPLPi(i=0 1)的操作示例

当满足以下条件时，适用图38.4：

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- 当CiEDG=0且CiEPO=0（上升沿）时，IELSRn.IR仅如(A)所示变化
- 当CiEDG=0且CiEPO=1（下降沿）时，IELSRn.IR仅如(B)所示变化。

38.4 噪声过滤器

图38.5显示了ACMPLPi噪声滤波器的配置，图38.6显示了ACMPLPi噪声滤波器的操作示例
ACMPLPi噪声滤波器。

可以在COMPFIR.CiFCK[1:0]位中选择采样时钟。ACMPLPi输出的ACMP_LPi信号（内部信号）在每个采样时钟周期进行采样。当电平匹配3次时，相应的IELSRn.IR位设置为1（请求中断）并输出ELC事件。

在软件待机模式下使用中断时，将COMPFIR.CiFCK[1:0]位设置为00b（旁路）。

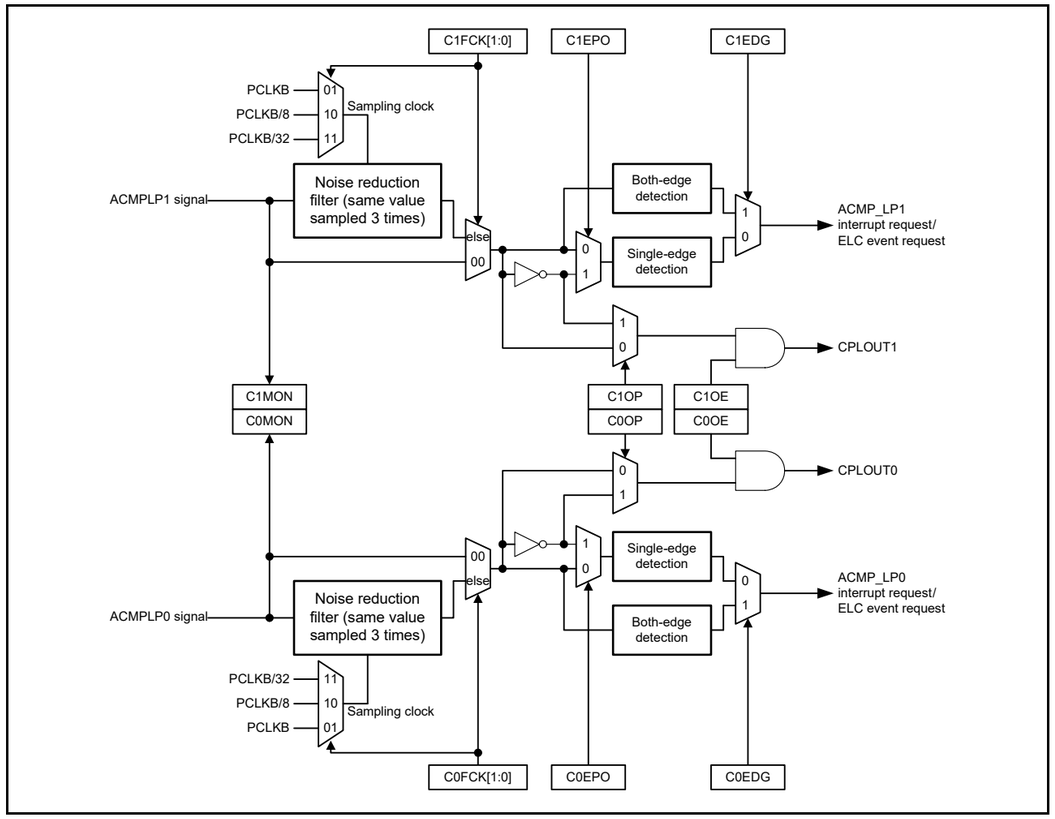


Figure 38.5 Noise filter and edge detection configuration

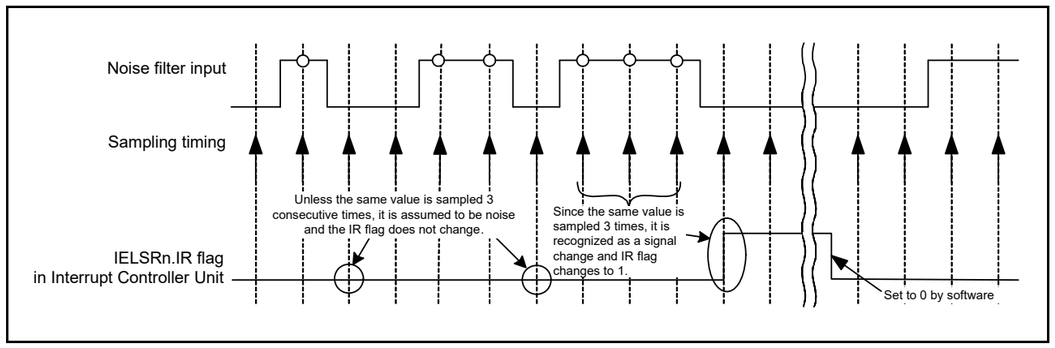


Figure 38.6 Noise filter and interrupt operation example

38.5 ACMPLP Interrupts

The ACMPLP generates interrupt requests from the ACMPLP0 and ACMPLP1 sources. To use the ACMPLPi (i = 0 and 1) interrupt, select it in the IELSRn register in the ICU. You can select either single-edge detection or both-edge detection using the COMPFIR.CiEDG bit. When single-edge detection is selected, select the polarity using the CiEPO bit.

The interrupt output can also be passed through the noise filter, which uses one of the three different sampling clocks, as

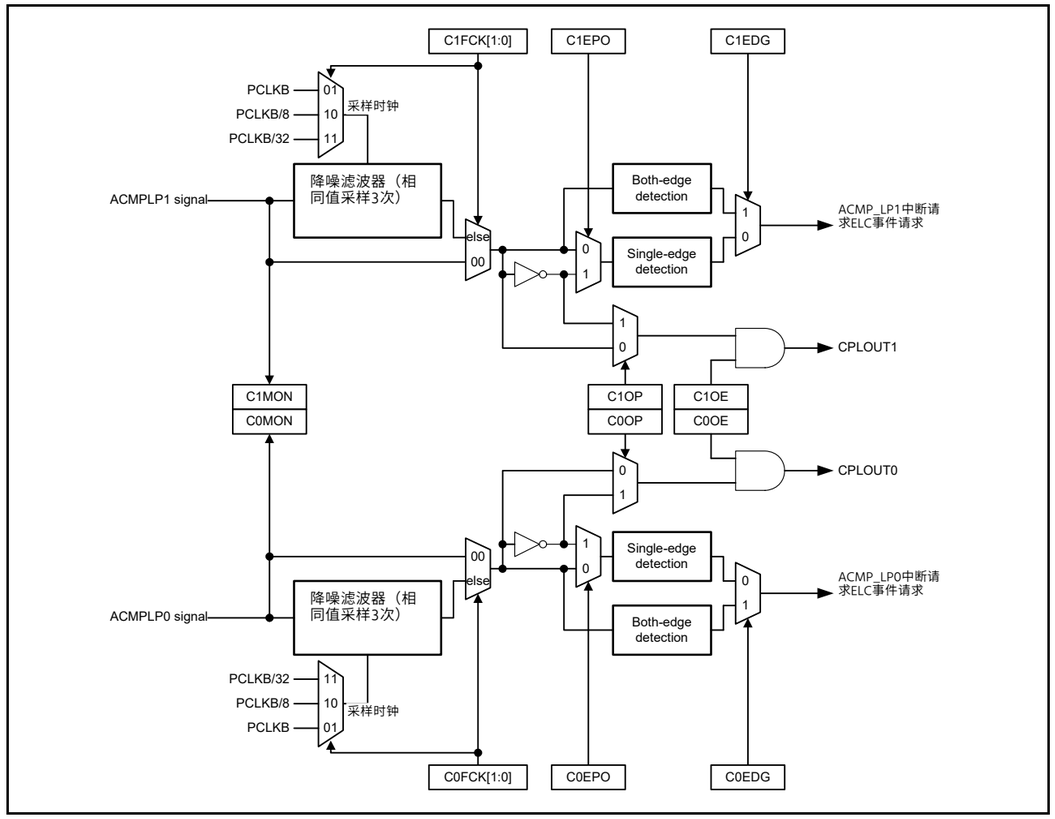


Figure 38.5 噪声过滤器和边缘检测配置

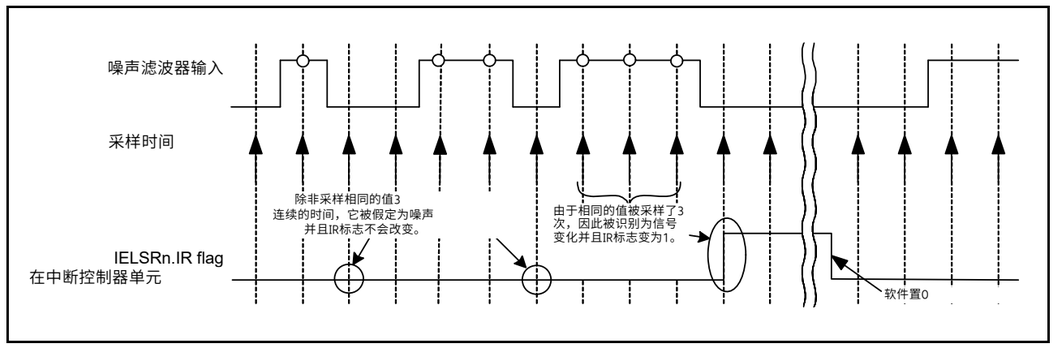


Figure 38.6 噪声滤波器和中断操作示例

38.5 ACMPLP Interrupts

ACMPLP从ACMPLP0和ACMPLP1源产生中断请求。要使用ACMPLPi（i=0和1）中断，请在ICU的IELSRn寄存器中选择它。您可以使用COMPFIR.CiEDG位选择单边沿检测或双边沿检测。选择单边检测时，请使用CIEPO位选择极性。

中断输出也可以通过噪声滤波器，它使用三种不同的采样时钟之一，如

selected in the COMPFIR.CiFCK[1:0] bits. Set the COMPFIR.CiFCK[1:0] bits to 01b, 10b, or 11b to select the respective sampling clock. To use the ACMPLP0 interrupt request to release Software Standby mode or Snooze mode, set COMPFIR.C0FCK[1:0] to 00b (no sampling). The ACMPLP1 interrupt request cannot be used to release Software Standby mode or Snooze mode.

38.6 ELC Event Output

The ELC uses the ACMPLP interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ELC events of the ACMPLP, select them in the ELSRn register in the ELC. When using ELC event request, set the COMPFIR.CiFCK[1:0] bits to 01b, 10b, or 11b.

38.7 Interrupt Handling and ELC Linking

ACMPLPi outputs event signals to the ELC to initiate operations of other modules selected in advance. In the same way as for the interrupt sources, the conditions for generation of the event signals output from ACMPLPi to the ELC can be selected as a single-edge detection or both-edge detection by setting the COMPFIR.CiEDG bit. When the single-edge detection is selected, the polarity can be selected in the CiEPO bit.

38.8 Comparator Pin Output

The comparison result from ACMPLPi can be output to external pins. Use the COMPOCR.CiOP and CiOE bits to set the output polarity (non-inverted output or inverted output) and to enable or disable the comparison output.

To output the ACMPLP comparison result to the VCOUT output pin by the CPLOUTi, set the corresponding Port mn Pin Function Select Register (PmnPFS) in the I/O registers.

For the register settings and the associated comparator output, see section 38.2.3, ACMPLP Output Control Register (COMPOCR).

38.9 Usage Notes

38.9.1 Settings for the Module-Stop State

The Module Stop Control Register can enable or disable the ACMPLP operation. The ACMPLP is initially stopped after reset. c. For details, see section 11, Low Power Modes.

38.9.2 Relationship with A/D converter

Constraints apply on the simultaneous use of ACMPLP analog input and A/D converter analog input. For details, see section 34.8.13, Relationship between the ADC14, OPAMP, and ACMPLP.

在COMPFIR.CiFCK[1:0]位中选择。将COMPFIR.CiFCK[1:0]位设置为01b、10b或11b以选择相应的采样时钟。要使用ACMPLP0中断请求来释放软件待机模式或贪睡模式，请将COMPFIR.C0FCK[1:0]设置为00b（无采样）。ACMPLP1中断请求不能用于释放软件待机模式或贪睡模式。

38.6 ELC事件输出

ELC使用ACMPLP中断请求信号作为ELC事件信号，为预设模块启用链接操作。要使用ACMPLP的ELC事件，请在ELC的ELSRn寄存器中选择它们。使用ELC事件请求时，将COMPFIR.CiFCK[1:0]位设置为01b、10b或11b。

38.7 中断处理和ELC链接

ACMPLPi向ELC输出事件信号，以启动预先选择的其他模块的操作。与中断源相同，通过设置COMPFIR.CiEDG位，可以选择从ACMPLPi输出到ELC的事件信号的产生条件为单边沿检测或双边沿检测。Whenthesingle-edge detectionisselected thepolaritycanbeselectedintheCiEPObit.

38.8 比较器引脚输出

ACMPLPi的比较结果可以输出到外部引脚。使用COMPOCR.CiOP和CiOE位设置输出极性（非反相输出或反相输出）并启用或禁用比较输出。

要通过CPLOUTi将ACMPLP比较结果输出到VCOUT输出引脚，请设置相应的PortmnPin IO寄存器中的功能选择寄存器(PmnPFS)。

有关寄存器设置和相关的比较器输出，请参见第38.2.3节，ACMPLP输出控制寄存器(COMPOCR)。

38.9 使用说明

38.9.1 模块停止状态的设置

模块停止控制寄存器可以启用或禁用ACMPLP操作。ACMPLP在复位后最初停止。C。有关详细信息，请参阅第11节，低功耗模式。

38.9.2 与AD转换器的关系

同时使用ACMPLP模拟输入和AD转换器模拟输入的限制条件。有关详细信息，请参阅第34.8.13节，ADC14、OPAMP和ACMPLP之间的关系。

39. 8-Bit D/A Converter (DAC8)

39.1 Overview

Table 39.1 lists the specifications of the 8-bit D/A converter, and Figure 39.1 shows a block diagram.

Table 39.1 8-bit D/A converter specifications

Parameter	Specifications
Resolution	8 bits
Output channels	2 channels
Module-stop function	The module-stop state can be set to reduce power consumption.

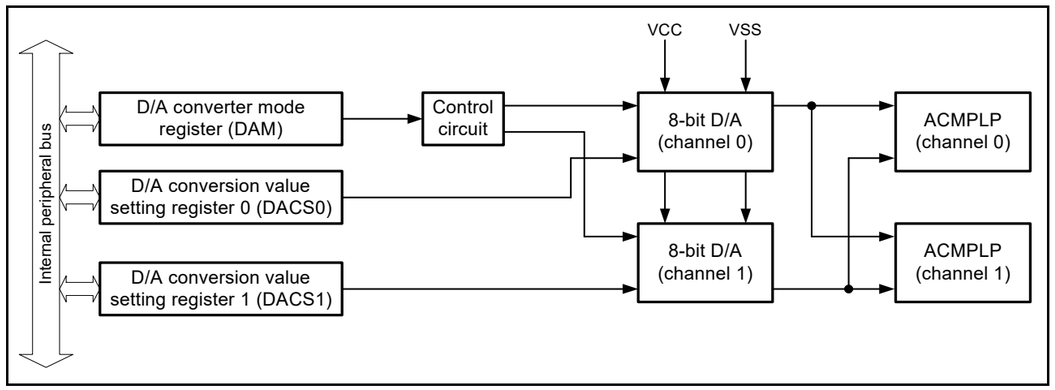


Figure 39.1 8-bit D/A converter block diagram

39.2 Register Descriptions

39.2.1 D/A Conversion Value Setting Register n (DACSn) (n = 0, 1)

Address(es): DAC8.DACS0 4009 E000h, DAC8.DACS1 4009 E001h

	b7	b6	b5	b4	b3	b2	b1	b0
	DACS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

The DACSn register is an 8-bit read/write register that stores data for D/A conversion. When D/A conversion is enabled, the value in the DACSn register is converted and output to an ACMPLP.

When 8-bit D/A converter output is selected as the reference input for the ACMPLP in the COMPSEL1 register, and ACMPLP operation is enabled (COMPMDR.CnENB = 1), changing the DACS[7:0] bits for the channel in use is prohibited.

39. 8-Bit D/A Converter (DAC8)

39.1 Overview

表39.1列出了8位DA转换器的规格，图39.1显示了框图。

Table 39.1 8位DA转换器规格

Parameter	Specifications
Resolution	8 bits
输出通道	2 channels
Module-stop function	可设置模块停止状态以降低功耗。

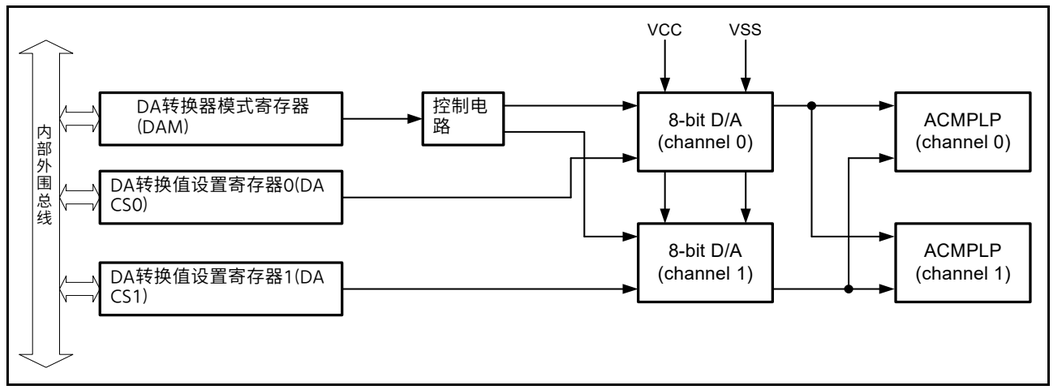


Figure 39.1 8位DA转换器框图

39.2 注册说明

39.2.1 DA转换值设置寄存器n(DACSn)(n=0 1)

Address(es): DAC8.DACS0 4009 E000h, DAC8.DACS1 4009 E001h

	b7	b6	b5	b4	b3	b2	b1	b0
	DACS[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

DACSn寄存器是一个8位读写寄存器，用于存储用于DA转换的数据。当DA转换使能时，DACSn寄存器中的值被转换并输出到ACMPLP。

当8位D选择转换器输出作为Compsel1寄存器中ACMPLP的参考输入，并且
ACMPLP操作使能（COMPMDR.CnENB=1），禁止更改正在使用的通道的DACS[7:0]位。

39.2.2 D/A Converter Mode Register (DAM)

Address(es): DAC8.DAM 4009 E003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DACE1	DACE0	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DACE0	D/A Operation Enable 0	0: D/A conversion disabled for channel 0 1: D/A conversion enabled for channel 0.	R/W
b5	DACE1	D/A Operation Enable 1	0: D/A conversion disabled for channel 1 1: D/A conversion enabled for channel 1.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DACEn bit (D/A Operation Enable n) (n = 0, 1)

The DACEn bit enables or disables D/A conversion.

When an 8-bit D/A converter output is selected as the reference input for the ACMPLP in the COMPSEL1 register, and ACMPLP operation is enabled (COMPMDR.CnENB = 1), changing the DACEn bits for the channel in use is prohibited.

39.3 Operation

The 8-bit D/A converter includes D/A conversion circuits for two channels, each of which can operate independently. When the DAM.DACEn bit (n = 0, 1) is set to 1, the 8-bit D/A converter is enabled and the conversion result is output to the ACMPLP.

The following sequence describes an operation example when performing D/A conversion for channel 0:

1. Set the data for D/A conversion to the DACS0 register.
2. Set the DAM.DACE0 bit to 1 to start D/A conversion. The conversion result is output to ACMPLP. The conversion result is continuously being output until the DACS0 is rewritten or the DAM.DACE0 bit is set to 0 (D/A conversion disabled).
   The output value (reference) is calculated with the following formula:

$$\frac{\text{DACS0 register}}{256} \times \text{VCC}$$

3. Set the COMPSEL1 register, and select the 8-bit D/A converter as the reference voltage.
4. Set the COMPMDR.CiENB bit to 1.
5. Wait for the comparator stabilization time T_{cmp} (min. 100 µs). For details, see section 38, Low Power Analog Comparator (ACMPLP).

39.4 Usage Notes

39.4.1 Module-Stop State

The Module Stop Control Register can enable or disable operation of the 8-bit D/A converter. The 8-bit D/A converter is stopped after a reset. The registers become accessible when the module-stop state is canceled. For details, see section 11, Low Power Modes.

39.4.2 Operation of the 8-bit D/A Converter in Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, D/A outputs are saved. The power supply current is the same as the one during D/A conversion. If the power supply current must be reduced in the module-stop

39.2.2 DA转换器模式寄存器(DAM)

Address(es): DAC8.DAM 4009 E003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DACE1	DACE0	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DACE0	DA操作使能0	0：通道0禁止DA转换1：通道0允许DA转换。	R/W
b5	DACE1	DA操作使能1	0：通道1禁止DA转换1：通道1允许DA转换。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DACEn位（DA操作使能n）（n=0 1）

DACEn位启用或禁用DA转换。

当在COMPSEL1寄存器中选择8位DA转换器输出作为ACMPLP的参考输入，并且启用ACMPLP操作（COMPMDR.CnENB=1）时，禁止更改正在使用的通道的DACEn位。

39.3 Operation

8位DA转换器包括两个通道的DA转换电路，每个通道可以独立工作。
当DAM.DACEn位(n=0 1)设置为1时，8位DA转换器使能，转换结果输出到ACMPLP。

以下序列描述了对通道0进行DA转换时的操作示例：

1. 将用于DA转换的数据设置到DACS0寄存器。
2. 将DAM.DACE0位设置为1以启动DA转换。转换结果输出到ACMPLP。转换结果将持续输出，直到DACS0被重写或DAM.DACE0位设置为0（禁用DA转换）。输出值（参考）使用以下公式计算：

$$\frac{\text{DACS0 register}}{256} \times \text{VCC}$$

3. 设置COMPSEL1寄存器，选择8位DA转换器作为参考电压。
4. 将COMPMDR.CiENB位设置为1。
5. 等待比较器稳定时间Tcmp（最少100µs）。有关详细信息，请参阅第38节，低功耗模拟Comparator (ACMPLP).

39.4 使用说明

39.4.1 Module-Stop State

模块停止控制寄存器可以启用或禁用8位DA转换器的操作。8位DA转换器在复位后停止。当模块停止状态被取消时，寄存器变得可访问。有关详细信息，请参阅第11节，低功耗模式。

39.4.2 模块停止状态下8位DA转换器的操作

当MCU进入模块停止状态并启用DA转换时，将保存DA输出。电源电流与DA转换时相同。如果必须在模块停止中减小电源电流

state, disable D/A conversion by setting the DAM.DACEn bits to 0.

39.4.3 8-bit D/A Converter in Software Standby Mode Operation

When the MCU enters Software Standby mode with D/A conversion enabled, D/A outputs are saved. The power supply current is the same as the one during D/A conversion. If the power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DAM.DACEn bits to 0.

39.4.4 When Not Using the D/A Converter

When not using the 8-bit D/A converter, set the DAM.DACEn bit to 0 (output disabled), and the DACSn register to 00h, so that current does not flow and the current consumption can be reduced.

状态，通过将DAM.DACEn位设置为0来禁用DA转换。

39.4.3 软件待机模式操作中的8位DA转换器

当MCU进入软件待机模式并启用DA转换时，将保存DA输出。电源电流与DA转换时相同。如果在软件待机模式下必须降低电源电流，则通过将DAM.DACEn位设置为0来禁用DA转换。

39.4.4 不使用数模转换器时

不使用8位DA转换器时，将DAM.DACEn位设置为0（禁用输出），将DACSn寄存器设置为00h，这样电流就不会流过，可以降低电流消耗。

40. Capacitive Touch Sensing Unit (CTSU)

40.1 Overview

The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode.

As Figure 40.1 shows, electrostatic capacitance (parasitic capacitance) exists between the electrode and the surrounding insulators. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the electrostatic capacitance increases.

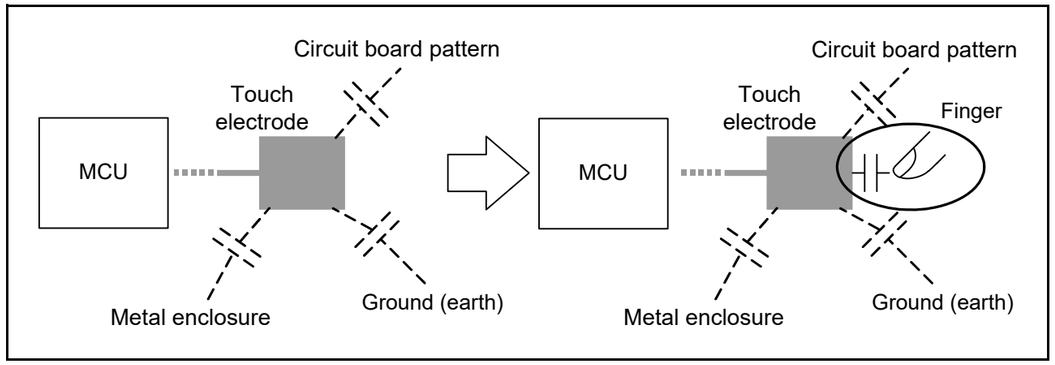


Figure 40.1 Increased electrostatic capacitance because of the presence of a finger

Electrostatic capacitance is detected by the self-capacitance and mutual-capacitance methods. In the self-capacitance method, the CTSU detects electrostatic capacitance generated between a finger and a single electrode. In the mutual-capacitance method, two electrodes are used as a transmit electrode and a receive electrode, and the CTSU detects the change in the electrostatic capacitance generated between the two when a finger is placed close to them.

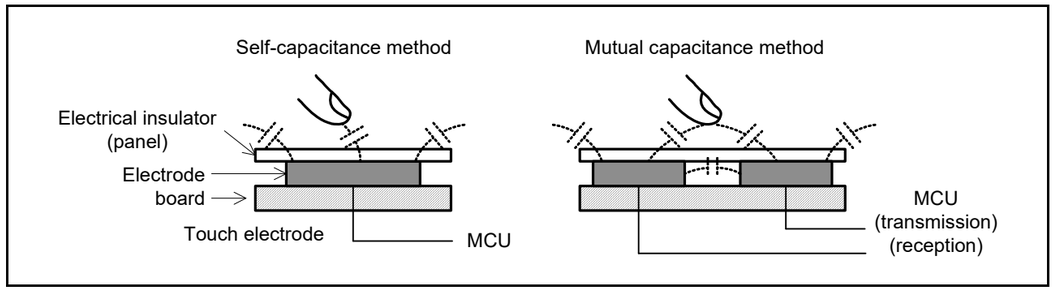


Figure 40.2 Self-capacitance and mutual-capacitance methods

Electrostatic capacitance is measured by counting a clock signal whose frequency changes according to the amount of charged or discharged current, for a specified period. For details on the measurement principles of the CTSU, see section 40.3.1, Principles of Measurement Operation. Table 40.1 lists the CTSU specifications and Figure 40.3 shows a block diagram.

40. 电容式触控感应单元(CTSU)

40.1 Overview

电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，该软件使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围，因此手指不会直接接触电极。

如图40.1所示，静电电容（寄生电容）存在于电极和周围绝缘体之间。因为人体是电导体，当手指靠近电极时，静电电容会增加。

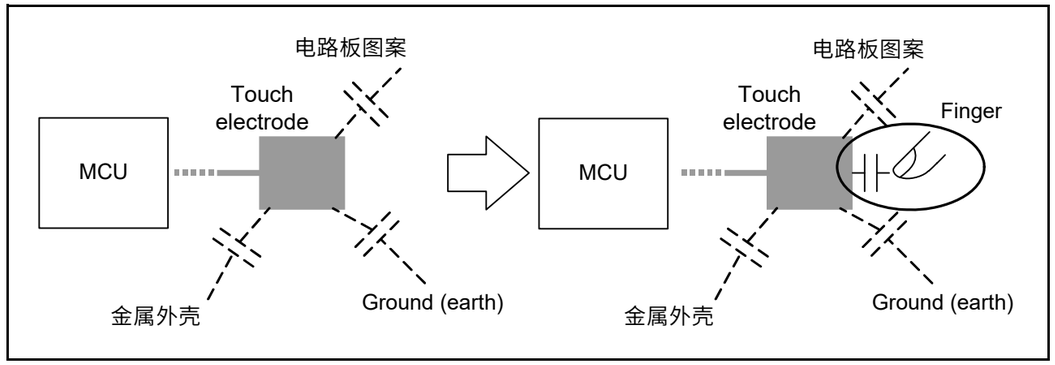


Figure 40.1 由于手指的存在而增加了静电电容

静电电容的检测方法有自电容法和互电容法。在自电容法中，CTSU检测手指和单个电极之间产生的静电电容。在互电容法中，两个电极用作发射电极和接收电极，当手指靠近它们时，CTSU会检测两者之间产生的静电电容的变化。

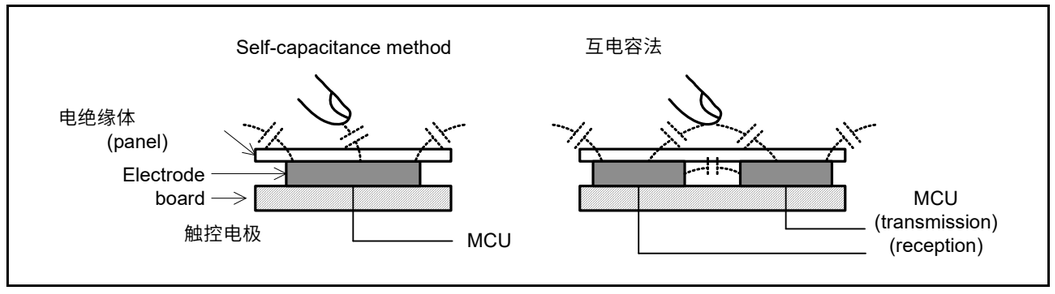


Figure 40.2 自电容和互电容方法

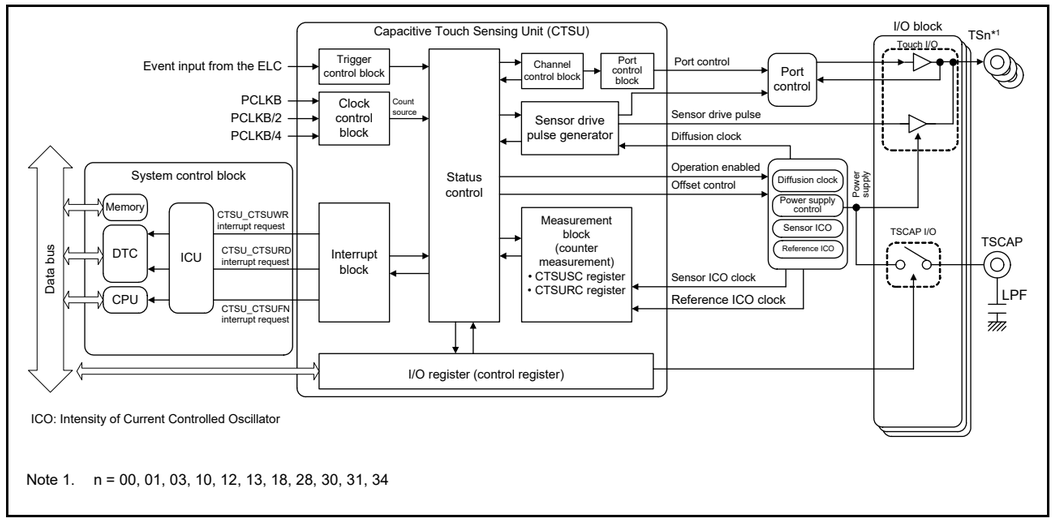
静电电容是通过对时钟信号进行计数来测量的，该时钟信号的频率根据充电或放电电流的大小而变化，在指定的时间段内。CTSU的测量原理详见40.3.1测量操作原理。表40.1列出了CTSU规格，图40.3显示了框图。

Table 40.1 CTSU specifications

Parameter		Description
Operating clocks		PCLKB, PCLKB/2, or PCLKB/4
Pins	Electrostatic capacitance measurement	11 channels (TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34)
	TSCAP	Low Pass Filter (LPF) connection pin
Measurement modes	Self-capacitance single scan mode	Electrostatic capacitance is measured on one channel using the self-capacitance method
	Self-capacitance multi-scan mode	Electrostatic capacitance is measured successively on multiple channels using the self-capacitance method
	Mutual-capacitance full-scan mode	Electrostatic capacitance is measured successively on multiple channels using the mutual-capacitance method
Noise prevention		Synchronous noise prevention, high-pass noise prevention
Measurement start conditions		• Software trigger • External trigger (ELC_CTSU from the Event Link Controller (ELC))

As Figure 40.3 shows, the CTSU consists of the following components:

- Status control block
- Trigger control block
- Clock control block
- Channel control block
- Port control block
- Sensor drive pulse generator
- Measurement block
- Interrupt block
- I/O registers.



Note 1. n = 00, 01, 03, 10, 12, 13, 18, 28, 30, 31, 34

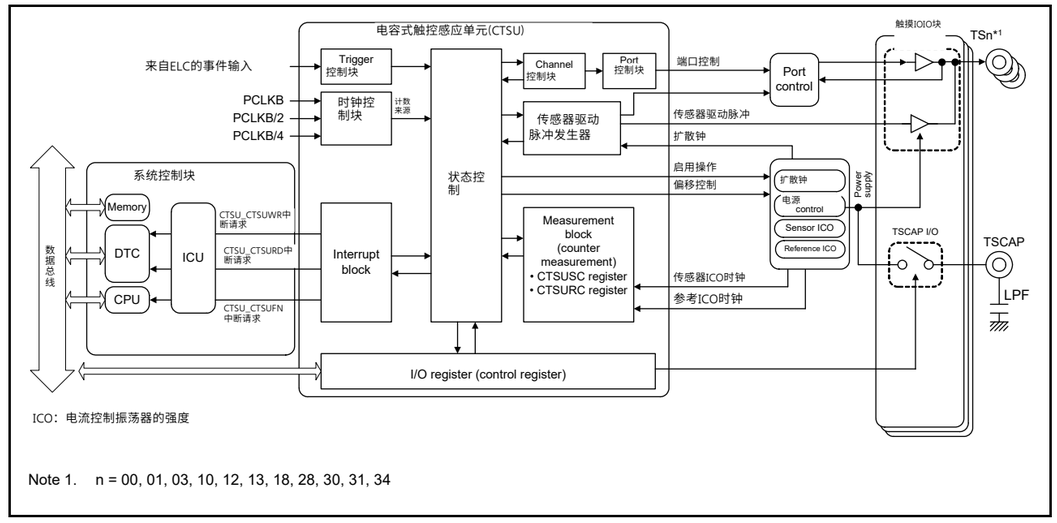
Figure 40.3 CTSU block diagram

Table 40.1 CTSU specifications

Parameter		Description
工作时钟		PCLKB, PCLKB/2, or PCLKB/4
Pins	静电电容测量	11 channels (TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34)
	TSCAP	低通滤波器(LPF)连接引脚
测量模式	自电容单次扫描模式	使用自电容法在一个通道上测量静电电容
	Self-capacitance multi-scan mode	使用自电容法在多个通道上连续测量静电电容
	Mutual-capacitance full-scan mode	使用互电容法在多个通道上连续测量静电电容
噪音预防		同步防噪、防高通防噪
测量开始条件		软件触发 外部触发（来自事件链接控制器(ELC)的ELC_CTSU）

如图40.3所示，CTSU由以下组件组成：

- 状态控制块
- 触发控制块
- 时钟控制块
- 通道控制块
- 端口控制块
- 传感器驱动脉冲发生器
- 测量块
- 中断块
- I/O registers.



Note 1. n = 00, 01, 03, 10, 12, 13, 18, 28, 30, 31, 34

Figure 40.3 CTSU框图

Table 40.2 CTSU pin configuration

Pin name	I/O	Function
TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34	Input	Electrostatic capacitive measurement pins (touch pins)
TSCAP	-	LPF connection pin

40.2 Register Descriptions

40.2.1 CTSU Control Register 0 (CTSUCR0)

Address(es): CTSU.CTSUCR0 4008 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CTSUINIT	—	CTSUSNZ	CTSUCAP	CTSUSTRT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CTSUSTRT	CTSU Measurement Operation Start	0: Stop measurement operation*1 1: Start measurement operation.	R/W
b1	CTSUCAP	CTSU Measurement Operation Start Trigger Select	0: Software trigger 1: External trigger.	R/W
b2	CTSUSNZ	CTSU Wait State Power-Saving Enable	This bit sets the power-saving function during a wait state: 0: Disable power-saving function during wait state 1: Enable power-saving function during wait state.	R/W
b3	—	Reserved	This bit read as 0. The write value should be 0.	R/W
b4	CTSUINIT	CTSU Control Block Initialization	Writing 1 to this bit initializes the CTSU control block and the CTSUSC, CTSURC, CTSUMCH0, CTSUMCH1, and CTSUST registers. This bit is read as 0.	W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the CTSU is not used, fix this bit to 0.

Only set the CTSUCAP and CTSUSNZ bits when the CTSUSTRT bit is 0. These bits can be set at the same time when measurement operation starts.

CTSUSTRT bit (CTSU Measurement Operation Start)

The CTSUSTRT bit specifies whether CTSU operation starts or stops. When the CTSUCAP bit is 0, measurement starts when software writes 1 to the CTSUSTRT bit (software trigger), and stops when hardware clears the CTSUSTRT bit to 0. When the CTSUCAP bit is 1, the CTSU waits for an external trigger by writing 1 to the CTSUSTRT bit, and measurement starts on the rising edge of the external trigger. When measurement is stopped, the CTSU waits for the next external trigger and operation continues.

Table 40.3 lists the CTSU states.

Table 40.3 CTSU states

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUST.CTSUSTC[2:0] flags as follows:

Table 40.2 CTSU引脚配置

引脚名称	I/O	Function
TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34	Input	静电电容测量引脚（触摸引脚）
TSCAP	-	LPF连接引脚

40.2 注册说明

40.2.1 CTSU控制寄存器0(CTSUCR0)

Address(es): CTSU.CTSUCR0 4008 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CTSUINIT	—	CTSUSNZ	CTSUCAP	CTSUSTRT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CTSUSTRT	CTSU测量操作 Start	0：停止测量操作*11：开始测量操作。	R/W
b1	CTSUCAP	CTSU测量操作 开始触发选择	0：软件触发1：外部触发。	R/W
b2	CTSUSNZ	CTSU等待状态省电 Enable	该位设置等待状态下的省电功能：0：等待状态下禁用省电功能1：等待状态下启用省电功能。	R/W
b3	—	Reserved	该位读为0。写入值应为0。	R/W
b4	CTSUINIT	CTSU控制块 Initialization	向该位写入1初始化CTSU控制块和CTSUSC、CTSURC、CTSUMCH0、CTSUMCH1和CTSUST寄存器。该位读为0。	W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 不使用CTSU时，将该位固定为0。

仅当CTSUSTRT位为0时设置CTSUCAP和CTSUSNZ位。这些位可以在测量操作开始时同时设置。

CTSUSTRT位（CTSU测量操作开始）

CTSUSTRT位指定CTSU操作是开始还是停止。当CTSUCAP位为0时，软件将1写入CTSUSTRT位（软件触发）时开始测量，并在硬件将CTSUSTRT位清0时停止。当CTSUCAP位为1时，CTSU通过写入1等待外部触发到CTSUSTRT位，并在外部触发的上升沿开始测量。当测量停止时，CTSU等待下一个外部触发并继续操作。

表40.3列出了CTSU状态。

Table 40.3 CTSU states

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	测量中
1	1	正在进行测量并等待外部触发*1

Note 1. 可以从CTSUST.CTSUSTC[2:0]标志读取状态，如下所示：

During measurement: CTSUST.CTSUSTC[2:0] flags ≠ 000b
While waiting for an external trigger: CTSUST.CTSUSTC[2:0] flags = 000b

If software sets the CTSUSTRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through software when the CTSUSTRT bit is 1, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time.

CTSUCAP bit (CTSU Measurement Operation Start Trigger Select)

The CTSUCAP bit specifies the measurement start condition. For details, see CTSUSTRT bit (CTSU Measurement Operation Start).

CTSUSNZ bit (CTSU Wait State Power-Saving Enable)

The CTSUSNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU power supply, which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 40.4 shows the CTSU power supply state control.

Table 40.4 CTSU power supply state control

CTSUCR1.CTSUPON bit	CTSUSNZ bit	CTSUCAP bit	CTSUSTRT bit	CTSU power supply state
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: Settings other than those listed in the table are prohibited.

To start measurement from the suspended state, set the CTSUSNZ bit to 0, and then set the CTSUSTRT bit to 1. To suspend the module after measurement stops, set the CTSUSNZ bit to 1.

CTSUINIT bit (CTSU Control Block Initialization)

Write 1 to the CTSUINIT bit to initialize the control registers. To force the current operation to stop, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time. This stops the operation and initializes the internal control registers.

Do not write 1 to the CTSUINIT bit when the CTSUSTRT bit is 1.

40.2.2 CTSU Control Register 1 (CTSUCR1)

Address(es): CTSU.CTSUCR1 4008 1001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUMD[1:0]		CTSUCLK[1:0]		CTSUATUNE1	CTSUATUNE0	CTSUCSW	CTSUPON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CTSUPON	CTSU Power Supply Enable	This bit controls the CTSU power supply: 0: Power off 1: Power on.	R/W
b1	CTSUCSW	CTSU LPF Capacitance Charging Control	This bit controls charging of the LPF capacitance connected to the TSCAP pin: 0: Turn off capacitance switch 1: Turn on capacitance switch.	R/W

测量期间：CTSUST.CTSUSTC[2:0]flags≠000b
等待外部触发时：CTSUST.CTSUSTC[2:0]flags=000b

如果在CTSUSTRT位已经为1时软件将该位设置为1，则忽略写入并继续操作。要在CTSUSTRT位为1时通过软件强制停止操作，请同时将CTSUSTRT位设置为0并将CTSUINIT位设置为1。

CTSUCAP位（CTSU测量操作开始触发选择）

CTSUCAP位指定测量开始条件。有关详细信息，请参阅CTSUSTRT位（CTSU测量Operation Start).

CTSUSNZ位（CTSU等待状态省电使能）

CTSUSNZ位在等待状态期间启用或禁用省电操作。它还可以暂停CTSU电源，从而降低等待状态下的功耗。在挂起状态下，CTSU电源关闭，而外部TSCAP仍在充电。

CTSU电源状态控制如表40.4所示。

Table 40.4 CTSU电源状态控制

CTSUCR1.CTSUPON bit	CTSUSNZ bit	CTSUCAP bit	CTSUSTRT bit	CTSU供电状态
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: 禁止在表中列出以外的设置。

要从暂停状态开始测量，请将CTSUSNZ位设置为0，然后将CTSUSTRT位设置为1。要在测量停止后暂停模块，请将CTSUSNZ位设置为1。

CTSUINIT位（CTSU控制块初始化）

向CTSUINIT位写入1以初始化控制寄存器。要强制停止当前操作，同时将CTSUSTRT位设置为0并将CTSUINIT位设置为1。这将停止操作并初始化内部控制寄存器。

当CTSUSTRT位为1时，不要将1写入CTSUINIT位。

40.2.2 CTSU控制寄存器1(CTSUCR1)

Address(es): CTSU.CTSUCR1 4008 1001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUMD[1:0]		CTSUCLK[1:0]		CTSUATUNE1	CTSUATUNE0	CTSUCSW	CTSUPON
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CTSUPON	CTSU电源使能	该位控制CTSU电源：0：关机1：开机。	R/W
b1	CTSUCSW	CTSULPF电容充电Control	该位控制连接到TSCAP引脚的LPF电容的充电：0：关闭电容开关1：打开电容开关。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	CTSUATUNE0	CTSU Power Supply Operating Mode Setting	VCC ≥ 2.4 V 0: Normal operating mode 1: Low-voltage operating mode. VCC < 2.4 V 0: Setting prohibited 1: Low-voltage operating mode.	R/W
b3	CTSUATUNE1	CTSU Power Supply Capacity Adjustment	0: Normal output 1: High-current output.	R/W
b5, b4	CTSUCLK[1:0]	CTSU Operating Clock Select	These bits select the operating clock: b5 b4 0 0: PCLKB 0 1: PCLKB/2 (PCLKB divided by 2) 1 0: PCLKB/4 (PCLKB divided by 4) 1 1: Setting prohibited.	R/W
b7, b6	CTSUMD[1:0]	CTSU Measurement Mode Select	These bits select the measurement mode: b7 b6 0 0: Self-capacitance single scan mode 0 1: Self-capacitance multi-scan mode 1 0: Setting prohibited 1 1: Mutual capacitance full-scan mode.	R/W

Only set the CTSUCR1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPON bit (CTSU Power Supply Enable)

The CTSUPON bit controls the power supply to the CTSU. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUCSW bit (CTSU LPF Capacitance Charging Control)

The CTSUCSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off. After the capacitance switch is turned on, wait until the capacitance connected to the TSCAP pin is charged for the specified time before starting measurement by setting CTSUCR0.CTSUSTRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUATUNE0 bit (CTSU Power Supply Operating Mode Setting)

The CTSUATUNE0 bit sets the power supply operating mode. Set this bit to the lower limit of VCC to operate the CTSU. As an example, when performing touch measurement in a system where VCC varies depending on battery operation, set this bit to 1 regardless of the initial VCC voltage. The VCC voltage range is 2 to 3 V.

CTSUATUNE1 bit (CTSU Power Supply Capacity Adjustment)

The CTSUATUNE1 bit sets the capacity of the CTSU power supply. In general, set this bit to 0.

CTSUCLK[1:0] bits (CTSU Operating Clock Select)

The CTSUCLK[1:0] bits select the operating clock.

CTSUMD[1:0] bits (CTSU Measurement Mode Select)

The CTSUMD bits set the measurement mode. For details, see section 40.3.2, Measurement Modes.

Bit	Symbol	位名称	Description	R/W
b2	CTSUATUNE0	CTSU电源运行模式设置	VCC≥2.4V0：正常工作模式1：低电压工作模式。VCC<2.4V0：禁止设置1：低电压工作模式。	R/W
b3	CTSUATUNE1	CTSU电源容量Adjustment	0：正常输出1：大电流输出。	R/W
b5, b4	CTSUCLK[1:0]	CTSU工作时钟选择	这些位选择工作时钟：b5b4 0 0: PCLKB 0 1：PCLKB2（PCLKB除以2） 1 0：PCLKB4（PCLKB除以4） 1 1：禁止设置。	R/W
b7, b6	CTSUMD[1:0]	CTSU测量模式选择	这些位选择测量模式：b7b6 0 0：自电容单扫描模式 0 1: Self-capacitance multi-scan mode 1 0：禁止设定 1 1：互电容全扫描模式。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCR1寄存器。

CTSUPON位（CTSU电源使能）

CTSUPON位控制CTSU的电源。将CTSUPON和CTSUCSW位设置为相同的值。

CTSUCSW位（CTSULPF电容充电控制）

CTSUCSW位通过打开或关闭电容开关来控制连接到TSCAP引脚的LPF电容的充电。电容开关打开后，通过将CTSUCR0.CTSUSTRT设置为1，等到连接到TSCAP引脚的电容充电指定时间后再开始测量。开始测量之前，使用IO端口向TSCAP引脚输出低电平，并对现有的LPF电容进行放电。将CTSUPON和CTSUCSW位设置为相同的值。

CTSUATUNE0位（CTSU电源工作模式设置）

CTSUATUNE0位设置电源工作模式。将此位设置为VCC的下限以操作CTSU。例如，在VCC随电池运行而变化的系统中执行触摸测量时，无论初始VCC电压如何，都将该位设置为1。VCC电压范围为2至3V。

CTSUATUNE1位（CTSU电源容量调整）

CTSUATUNE1位设置CTSU电源的容量。一般情况下，将此位设置为0。

CTSUCLK[1:0]位（CTSU工作时钟选择）

CTSUCLK[1:0]位选择工作时钟。

CTSUMD[1:0]位（CTSU测量模式选择）

CTSUMD位设置测量模式。有关详细信息，请参阅第40.3.2节，测量模式。

40.2.3 CTSU Synchronous Noise Reduction Setting Register (CTSUSDPRS)

Address(es): CTSU.CTSUSDPRS 4008 1002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUSOFF	CTSUPRMODE[1:0]		CTSUPRRATIO[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CTSUPRRATIO[3:0]	CTSU Measurement Time and Pulse Count Adjustment	These bits set the measurement time and the pulse count. The recommended setting is 3 (0011b).	R/W
b5, b4	CTSUPRMODE[1:0]	CTSU Base Period and Pulse Count Setting	These bits set the base pulse count: b5 b4 0 0: 510 pulses 0 1: 126 pulses 1 0: 62 pulses (recommended setting value) 1 1: Setting prohibited.	R/W
b6	CTSUSOFF	CTSU High-Pass Noise Reduction Function Off Setting	This bit controls spectrum diffusion, which can be used to reduce high-pass noise: 0: Turn spectrum diffusion on 1: Turn spectrum diffusion off.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Only set the CTSUSDPRS register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPRRATIO[3:0] bits (CTSU Measurement Time and Pulse Count Adjustment)

The CTSUPRRATIO[3:0] bits set the measurement time and the number of measurement pulses using the following formulas, where the number of base pulses is determined by the CTSUPRMODE[1:0] setting:

Measurement pulse count = base pulse count × (CTSUPRRATIO[3:0] bits + 1)
Measurement time = (base pulse count × (CTSUPRRATIO[3:0] bits + 1) + base pulse count - 2) × 0.25 × base clock cycle

Note: For details on the base clock cycle, see section 40.2.21, CTSU Sensor Offset Register 1 (CTSUSO1).

CTSUPRMODE[1:0] bits (CTSU Base Period and Pulse Count Setting)

The CTSUPRMODE[1:0] bits select the number of base pulses that occur during measurement.

CTSUSOFF bit (CTSU High-Pass Noise Reduction Function Off Setting)

The CTSUSOFF bit turns on or off the function for reducing high-pass noise. Set this bit to 1 to turn the function off.

40.2.4 CTSU Sensor Stabilization Wait Control Register (CTSUSST)

Address(es): CTSU.CTSUSST 4008 1003h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUSST[7:0]	CTSU Sensor Stabilization Wait Control	Set these bits to 00010000b	R/W

Only set the CTSUSST register when the CTSUCR0.CTSUSTRT bit is 0.

40.2.3 CTSU同步降噪设置寄存器(CTSUSDPRS)

Address(es): CTSU.CTSUSDPRS 4008 1002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUSOFF	CTSUPRMODE[1:0]		CTSUPRRATIO[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CTSUPRRATIO[3:0]	CTSU测量时间和脉冲计数调整	这些位设置测量时间和脉冲计数。推荐设置为3(0011b)。	R/W
b5, b4	CTSUPRMODE[1:0]	CTSU基本周期和脉冲计数Setting	这些位设置基本脉冲计数：b5b4 0 0: 510 pulses 0 1: 126 pulses 1 0：62脉冲（推荐设定值） 1 1：禁止设置。	R/W
b6	CTSUSOFF	CTSU高通降噪功能关闭设置	该位控制频谱扩散，可用于降低高通噪声：0：打开频谱扩散1：关闭频谱扩散。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUSDPRS寄存器。

CTSURRATIO[3:0]位（CTSU测量时间和脉冲计数调整）

CTSUPRATIO[3:0]位使用以下公式设置测量时间和测量脉冲数，其中基本脉冲数由CTSUPRMODE[1:0]设置确定：

测量脉冲数=基本脉冲数×(CTSUPRRATIO[3:0]位+1)
测量时间=(基本脉冲计数×(CTSUPRRATIO[3:0]位+1)+基本脉冲计数2)×0.25×基本时钟周期

Note: 有关基本时钟周期的详细信息，请参见第40.2.21节，CTSU传感器偏移寄存器1(CTSUSO1)。

CTSUPRMODE[1:0]位（CTSU基本周期和脉冲计数设置）

CTSUPRMODE[1:0]位选择测量期间出现的基本脉冲数。

CTSUSOFF位（CTSU高通降噪功能关闭设置）

CTSUSOFF位打开或关闭降低高通噪声的功能。将此位设置为1可关闭该功能。

40.2.4 CTSU传感器稳定等待控制寄存器(CTSUSST)

Address(es): CTSU.CTSUSST 4008 1003h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSST[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUSST[7:0]	CTSU传感器稳定等待Control	将这些位设置为00010000b	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUSST寄存器。

CTSUSST[7:0] bits (CTSU Sensor Stabilization Wait Control)

The CTSUSST[7:0] bits set the stabilization wait time for the TSCAP pin voltage. Always set these bits to 00010000b. If these bits are not set, the TSCAP voltage becomes unstable at the start of measurement, and the CTSU is unable to obtain correct touch measurement results.

40.2.5 CTSU Measurement Channel Register 0 (CTSUMCH0)

Address(es): CTSU.CTSUMCH0 4008 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUMCH0[5:0]					
Value after reset:	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CTSUMCH0[5:0]	CTSU Measurement Channel 0	In self-capacitance single scan mode, these bits set a channel to be measured: b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 1: TS03 0 0 1 0 1 0: TS10 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 0 1 0: TS18 0 1 1 1 0 0: TS28 0 1 1 1 1 0: TS30 0 1 1 1 1 1: TS31 1 0 0 0 1 0: TS34 Other than those specified, the starting measurement operation when CTSUCR0.CTSUSTRT = 1 is prohibited after these bits are set.	R/W*1
			In other measurement modes, these bits indicate the channel that is currently being measured: b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 1: TS03 0 0 1 0 1 0: TS10 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 0 1 0: TS18 0 1 1 1 0 0: TS28 0 1 1 1 1 0: TS30 0 1 1 1 1 1: TS31 1 0 0 0 1 0: TS34 1 1 1 1 1 1: Measure is being stopped.	
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is enabled only in self-capacitance single scan mode (CTSUCR1.CTSUMD[1:0] bits = 00b).

Only set the CTSUMCH0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUMCH0[5:0] bits (CTSU Measurement Channel 0)

In self-capacitance single scan mode, the CTSUMCH0[5:0] bits set the channel to be measured. In this mode, only specify enabled channels (000000b, 000001b, 000011b, 001010b, 001100b, 001101b, 010010b, 011100b, 011110b, 011111b, and 100010b). In other modes, these indicate the receive channel that is being measured and writing to these bits has no effect.

CTSUSST[7:0]位（CTSU传感器稳定等待控制）

CTSUSST[7:0]位设置TSCAP引脚电压的稳定等待时间。始终将这些位设置为00010000b。如果未设置这些位，则TSCAP电压在测量开始时变得不稳定，CTSU无法获得正确的触摸测量结果。

40.2.5 CTSU测量通道寄存器0(CTSUCH0)

Address(es): CTSU.CTSUMCH0 4008 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUMCH0[5:0]					
重置后的值：	0	0	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b5 to b0	CTSUMCH0[5:0]	CTSU测量通道0	在自电容单次扫描模式下，这些位设置要测量的通道：b5b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 1: TS03 0 0 1 0 1 0: TS10 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 0 1 0: TS18 0 1 1 1 0 0: TS28 0 1 1 1 1 0: TS30 0 1 1 1 1 1: TS31 1 0 0 0 1 0: TS34 除指定以外，在这些位设置后禁止CTSUCR0.CTSUSTRT=1时的开始测量操作。	R/W*1
			在其他测量模式下，这些位指示当前正在测量的通道：b5b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 1: TS03 0 0 1 0 1 0: TS10 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 0 1 0: TS18 0 1 1 1 0 0: TS28 0 1 1 1 1 0: TS30 0 1 1 1 1 1: TS31 1 0 0 0 1 0: TS34 1 1 1 1 11：正在停止测量。	
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只有在自电容单次扫描模式下才能写入这些位（CTSUCR1.CTSUMD[1:0]位=00b）。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUMCH0寄存器。

CTSUCH0[5:0]位（CTSU测量通道0）

在自电容单次扫描模式下，CTSUMCH0[5:0]位设置要测量的通道。在此模式下，仅指定启用的通道（000000b、000001b、000011b、001010b、001100b、001101b、010010b、011100b、011110b、011111b和100010b）。在其他模式下，这些表示正在测量的接收通道，写入这些位无效。

40.2.6 CTSU Measurement Channel Register 1 (CTSUMCH1)

Address(es): CTSU.CTSUMCH1 4008 1005h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUMCH1[5:0]					
Value after reset:	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CTSUMCH1[5:0]	CTSU Measurement Channel 1	b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 1: TS03 0 0 1 0 1 0: TS10 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 0 1 0: TS18 0 1 1 1 0 0: TS28 0 1 1 1 1 0: TS30 0 1 1 1 1 1: TS31 1 0 0 0 1 0: TS34 1 1 1 1 1 1: Measurement is stopped.	R
b7, b6	—	Reserved	These bits are read as 0.	R

CTSUMCH1[5:0] bits (CTSU Measurement Channel 1)

In full-scan mode, the CTSUMCH1[5:0] bits indicate the transmit channel that is being measured. The value of these bits is 111111b when measurement is stopped, or when in self-capacitance single scan or multi-scan mode.

40.2.7 CTSU Channel Enable Control Register 0 (CTSUCHAC0)

Address(es): CTSU.CTSUCHAC0 4008 1006h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC0[7:0]*1							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC0[7:0] *1	CTSU Channel Enable Control 0	These bits select whether the associated TS pin is measured: 0: Do not measure 1: Measure. These bits specify the TS00, TS01, and TS03 pins.	R/W

Note 1. The MCU does not support TS02 and TS04 to TS07 pins. Therefore, CTSUCHAC0[2] and CTSUCHAC0[4:7] are read as 0. The write value should be 0.

Only set the CTSUCHAC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC0[7:0]*1 bits (CTSU Channel Enable Control 0)

The CTSUCHAC0[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC0[0] is associated with TS00 and CTSUCHAC0[3] with TS03.

40.2.6 CTSU测量通道寄存器1(CTSUCH1)

Address(es): CTSU.CTSUMCH1 4008 1005h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUMCH1[5:0]					
重置后的值：	0	0	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b5 to b0	CTSUMCH1[5:0]	CTSU测量通道1	b5 b0 0 0 0 0 0 0: TS00 0 0 0 0 0 1: TS01 0 0 0 0 1 1: TS03 0 0 1 0 1 0: TS10 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 0 1 0: TS18 0 1 1 1 0 0: TS28 0 1 1 1 1 0: TS30 0 1 1 1 1 1: TS31 1 0 0 0 1 0: TS34 1 1 1 1 11：停止测量。	R
b7, b6	—	Reserved	这些位读为0。	R

CTSUCH1[5:0]位（CTSU测量通道1）

在全扫描模式下，CTSUMCH1[5:0]位指示正在测量的发送通道。当测量停止时，或在自电容单次扫描或多次扫描模式下，这些位的值为111111b。

40.2.7 CTSU通道使能控制寄存器0(CTSUCHAC0)

Address(es): CTSU.CTSUCHAC0 4008 1006h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC0[7:0]*1							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHAC0[7:0] *1	CTSU通道使能控制0	这些位选择是否测量相关的TS引脚：0：不测量1：测量。这些位指定TS00、TS01和TS03引脚。	R/W

注1.MCU不支持TS02和TS04到TS07引脚。因此，CTSUCHAC0[2]和CTSUCHAC0[4:7]读为0。写入值应为0。仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC0寄存器。

CTSUCHAC0[7:0]*1位（CTSU通道使能控制0）

CTSUCHAC0[7:0]位选择要测量其静电电容的接收和发送引脚。
CTSUCHAC0[0]与TS00相关联，CTSUCHAC0[3]与TS03相关联。

40.2.8 CTSU Channel Enable Control Register 1 (CTSUCHAC1)

Address(es): CTSU.CTSUCHAC1 4008 1007h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC1[7:0]*1							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC1[7:0] *1	CTSU Channel Enable Control 1	These bits select whether the associated TS pin is measured. 0: Do not measure 1: Measure. These bits specify the TS10, TS12, and TS13 pins.	R/W

Note 1. The MCU does not support TS08, TS09, TS11, TS14 and TS15 pins. Therefore, CTSUCHAC1[0], CTSUCHAC1[1], CTSUCHAC1[3], and CTSUCHAC[7:6] are read as 0. The write value should be 0.

Only set the CTSUCHAC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC1[7:0]*1 bits (CTSU Channel Enable Control 1)

The CTSUCHAC1[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC1[2] is associated with TS10 and CTSUCHAC1[5] with TS13.

40.2.9 CTSU Channel Enable Control Register 2 (CTSUCHAC2)

Address(es): CTSU.CTSUCHAC2 4008 1008h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC2[7:0]*1							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC2[7:0] *1	CTSU Channel Enable Control 2	These bits select whether the associated TS pin is measured. 0: Do not measure 1: Measure. This bit specifies the TS18 pin.	R/W

Note 1. The MCU does not support TS16, TS17 and TS19 to TS23 pins. Therefore, CTSUCHAC2[7:3] and CTSUCHAC2[1:0] are read as 0. The write value should be 0.

Only set the CTSUCHAC2 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC2[7:0]*1 bits (CTSU Channel Enable Control 2)

The CTSUCHAC2[7:0] bits select the receive and transmit pins for which electrostatic capacitance is to be measured. CTSUCHAC2[2] is associated with TS18.

40.2.8 CTSU通道使能控制寄存器1(CTSUCHAC1)

Address(es): CTSU.CTSUCHAC1 4008 1007h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC1[7:0]*1							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHAC1[7:0] *1	CTSU通道使能控制1	这些位选择是否测量相关的TS引脚。0：不测量1：测量。这些位指定TS10、TS12和TS13引脚。	R/W

Note 1. MCU不支持TS08、TS09、TS11、TS14和TS15引脚。因此，CTSUCHAC1[0]、CTSUCHAC1[1]、CTSUCHAC1[3]和CTSUCHAC[7:6]读为0。写入值应为0。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC1寄存器。

CTSUCHAC1[7:0]*1位（CTSU通道使能控制1）

CTSUCHAC1[7:0]位选择要测量其静电电容的接收和发送引脚。
CTSUCHAC1[2]与TS10相关联，CTSUCHAC1[5]与TS13相关联。

40.2.9 CTSU通道使能控制寄存器2(CTSUCHAC2)

Address(es): CTSU.CTSUCHAC2 4008 1008h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC2[7:0]*1							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHAC2[7:0] *1	CTSU通道启用控制2	这些位选择是否测量相关的TS引脚。0：不测量1：测量。该位指定TS18引脚。	R/W

Note 1. MCU不支持TS16、TS17和TS19到TS23引脚。因此，CTSUCHAC2[7:3]和CTSUCHAC2[1:0]被读取为0。写入值应为0。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC2寄存器。

CTSUCHAC2[7:0]*1位（CTSU通道使能控制2）

CTSUCHAC2[7:0]位选择要测量静电电容的接收和发送引脚。
CTSUCHAC2[2]与TS18相关联。

40.2.10 CTSU Channel Enable Control Register 3 (CTSUCHAC3)

Address(es): CTSU.CTSUCHAC3 4008 1009h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC3[7:0]*1							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC3[7:0] *1	CTSU Channel Enable Control 3	These bits select whether the associated TS pins is measured: 0: Do not measure 1: Measure. These bits specify the TS28, TS30, and TS31 pins.	R/W

Note 1. The MCU does not support TS24 to TS27 and TS29 pins. Therefore, CTSUCHAC3[3:0] and CTSUCHAC3[5] are read as 0. The write value should be 0.

Only set the CTSUCHAC3 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC3[7:0]*1 bits (CTSU Channel Enable Control 3)

The CTSUCHAC3[7:0] bits select the receive and transmit pins for which electrostatic capacitance is to be measured. CTSUCHAC3[4] is associated with TS28 and CTSUCHAC3[7] with TS31.

40.2.11 CTSU Channel Enable Control Register 4 (CTSUCHAC4)

Address(es): CTSU.CTSUCHAC4 4008 100Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUCHAC4[3:0]*1			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CTSUCHAC4[3:0] *1	CTSU Channel Enable Control 4	These bits select whether the associated TS pin is measured: 0: Do not measure 1: Measure. This bit specifies the TS34 pin.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The MCU does not support TS32, TS33, and TS35 pins. Therefore, CTSUCHAC4[3] and CTSUCHAC4[1:0] are read as 0. The write value should be 0.

Only set the CTSUCHAC4 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC4[3:0]*1 bits (CTSU Channel Enable Control 4)

The CTSUCHAC4[3:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC4[2] is associated with TS34.

40.2.10 CTSU通道使能控制寄存器3(CTSUCHAC3)

Address(es): CTSU.CTSUCHAC3 4008 1009h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC3[7:0]*1							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHAC3[7:0] *1	CTSU通道启用控制3	这些位选择是否测量相关的TS引脚：0：不测量1：测量。这些位指定TS28、TS30和TS31引脚。	R/W

Note 1. MCU不支持TS24到TS27和TS29引脚。因此，CTSUCHAC3[3:0]和CTSUCHAC3[5]被读取为0。写入值应为0。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC3寄存器。

CTSUCHAC3[7:0]*1位（CTSU通道使能控制3）

CTSUCHAC3[7:0]位选择要测量静电电容的接收和发送引脚。
CTSUCHAC3[4]与TS28相关，CTSUCHAC3[7]与TS31相关。

40.2.11 CTSU通道使能控制寄存器4(CTSUCHAC4)

Address(es): CTSU.CTSUCHAC4 4008 100Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUCHAC4[3:0]*1			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CTSUCHAC4[3:0] *1	CTSU通道启用控制4	这些位选择是否测量相关的TS引脚：0：不测量1：测量。该位指定TS34引脚。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. MCU不支持TS32、TS33和TS35引脚。因此，CTSUCHAC4[3]和CTSUCHAC4[1:0]被读取为0。写入值应为0。

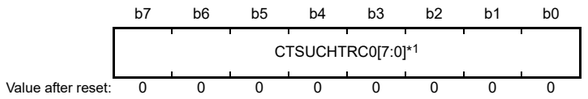
仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC4寄存器。

CTSUCHAC4[3:0]*1位（CTSU通道使能控制4）

CTSUCHAC4[3:0]位选择要测量其静电电容的接收和发送引脚。
CTSUCHAC4[2]与TS34相关联。

40.2.12 CTSU Channel Transmit/Receive Control Register 0 (CTSUCHTRC0)

Address(es): CTSU.CTSUCHTRC0 4008 100Bh



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC0[7:0] *1	CTSU Channel Transmit/Receive Control 0	0: Reception 1: Transmission. These bits specify the TS00, TS01, TS03 pins.	R/W

Note 1. The MCU does not support TS02 and TS04 to TS07 pins. Therefore, CTSUCHTRC0[2] and CTSUCHTRC0[4:7] are read as 0. The write value should be 0.

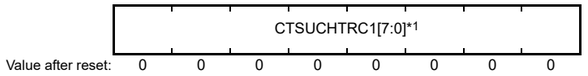
Only set the CTSUCHTRC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC0[7:0]*1 bits (CTSU Channel Transmit/Receive Control 0)

In full-scan mode, the CTSUCHTRC0[7:0] bits allocate reception or transmission to the associated TS pins. The setting of these bits is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC0[0] is associated with TS00 and CTSUCHTRC0[3] with TS03.

40.2.13 CTSU Channel Transmit/Receive Control Register 1 (CTSUCHTRC1)

Address(es): CTSU.CTSUCHTRC1 4008 100Ch



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC1[7:0]*1	CTSU Channel Transmit/Receive Control 1	0: Reception 1: Transmission. These bits specify the TS10, TS12, and TS13 pins.	R/W

Note 1. The MCU does not support TS08, TS09, TS11, TS14, and TS15 pins. Therefore, CTSUCHTRC1[0], CTSUCHTRC1[1], CTSUCHTRC1[3], and CTSUCHTRC[7:6] are read as 0. The write value should be 0.

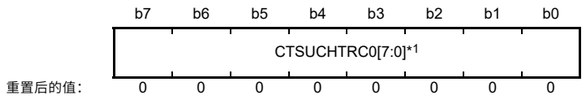
Only set the CTSUCHTRC1 when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC1[7:0]*1 bits (CTSU Channel Transmit/Receive Control 1)

In full-scan mode, the CTSUCHTRC1[7:0] bits allocate reception or transmission to the associated TS pins. The setting of these bits is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC1[2] is associated with TS10 and CTSUCHTRC1[5] with TS13.

40.2.12 CTSU通道发送接收控制寄存器0(CTSUCHTRC0)

Address(es): CTSU.CTSUCHTRC0 4008 100Bh



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHTRC0[7:0] *1	CTSU Channel Transmit/Receive Control 0	0：接收1：发送。这些位指定TS00、TS01、TS03引脚。	R/W

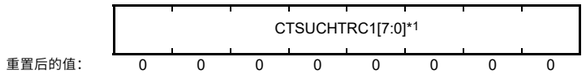
注1.MCU不支持TS02和TS04到TS07引脚。因此，CTSUCR0[2]和CTSUCHTRC0[4:7]读为0。写入值应为0。仅当CTSUCR0.CTSUSTRT位为0时才设置CTSUCR0寄存器。

CTSUCHTRC0[7:0]*1位（CTSU通道发送接收控制0）

在全扫描模式下，CTSUCHTRC0[7:0]位将接收或发送分配给相关的TS引脚。这些位的设置在自电容单扫描和多扫描模式下被忽略。CTSUCHTRC0[0]与TS00相关联，CTSUCHTRC0[3]与TS03相关联。

40.2.13 CTSU通道发送接收控制寄存器1(CTSUCHTRC1)

Address(es): CTSU.CTSUCHTRC1 4008 100Ch



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHTRC1[7:0]*1	CTSU Channel Transmit/Receive Control 1	0：接收1：发送。这些位指定TS10、TS12和TS13引脚。	R/W

Note 1. MCU不支持TS08、TS09、TS11、TS14和TS15引脚。因此，CTSUCHTRC1[0]、CTSUHTRC1[1]、CTSUCHTRC1[3]和CTSUCHTRC[7:6]读为0。写入值应为0。

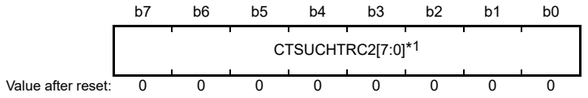
仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC1。

CTSUCHTRC1[7:0]*1位（CTSU通道发送接收控制1）

在全扫描模式下，CTSUHTRC1[7:0]位将接收或发送分配给相关的TS引脚。这些位的设置在自电容单扫描和多扫描模式下被忽略。CTSUCHTRC1[2]与TS10相关联，CTSUCHTRC1[5]与TS13相关联。

40.2.14 CTSU Channel Transmit/Receive Control Register 2 (CTSUCHTRC2)

Address(es): CTSU.CTSUCHTRC2 4008 100Dh



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC2[7:0]*1	CTSU Channel Transmit/Receive Control 2	0: Reception 1: Transmission. These bits specifies the TS18 pin.	R/W

Note 1. The MCU does not support TS16, TS17, and TS19 to TS23 pins. Therefore, CTSUCHTRC2[7:3] and CTSUCHTRC2[1:0] are read as 0. The write value should be 0.

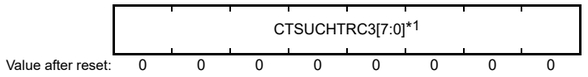
Only set the CTSUCHTRC2 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC2[7:0]*1 bits (CTSU Channel Transmit/Receive Control 2)

In full-scan mode, the CTSUCHTRC2[7:0] bits allocate reception or transmission to the associated TS pins. The setting of these bits is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC2[2] is associated with TS18.

40.2.15 CTSU Channel Transmit/Receive Control Register 3 (CTSUCHTRC3)

Address(es): CTSU.CTSUCHTRC3 4008 100Eh



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC3[7:0]*1	CTSU Channel Transmit/Receive Control 3	0: Reception 1: Transmission. These bits specify the TS28, TS30, and TS31 pins.	R/W

Note 1. The MCU does not support TS24 to TS27, and TS29 pins. Therefore, CTSUCHTRC3[3:0] and CTSUCHTRC3[5] are read as 0. The write value should be 0.

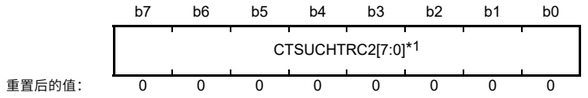
Only set the CTSUCHTRC3 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC3[7:0]*1 bits (CTSU Channel Transmit/Receive Control 3)

In full-scan mode, the CTSUCHTRC3[7:0] bits allocate reception or transmission to the associated TS pins. The setting of these bits is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC3[4] is associated with TS28 and CTSUCHTRC3[7] with TS31.

40.2.14 CTSU通道发送接收控制寄存器2(CTSUCHTRC2)

Address(es): CTSU.CTSUCHTRC2 4008 100Dh



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHTRC2[7:0]*1	CTSU Channel Transmit/Receive Control 2	0：接收1：发送。这些位指定TS18引脚。	R/W

Note 1. MCU不支持TS16、TS17和TS19到TS23引脚。因此，CTSUCHTRC2[7:3]和CTSUCHTRC2[1:0]被读取为0。写入值应为0。

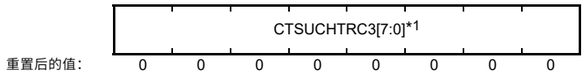
仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC2寄存器。

CTSUCHTRC2[7:0]*1位（CTSU通道发送接收控制2）

在全扫描模式下，CTSUCHTRC2[7:0]位将接收或发送分配给相关的TS引脚。这些位的设置在自电容单扫描和多扫描模式下被忽略。CTSUCHTRC2[2]与TS18相关联。

40.2.15 CTSU通道发送接收控制寄存器3(CTSUCHTRC3)

Address(es): CTSU.CTSUCHTRC3 4008 100Eh



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHTRC3[7:0]*1	CTSU Channel Transmit/Receive Control 3	0：接收1：发送。这些位指定TS28、TS30和TS31引脚。	R/W

Note 1. MCU不支持TS24到TS27和TS29引脚。因此，CTSUCHTRC3[3:0]和CTSUCHTRC3[5]被读取为0。写入值应为0。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC3寄存器。

CTSUCHTRC3[7:0]*1位（CTSU通道发送接收控制3）

在全扫描模式下，CTSUCHTRC3[7:0]位将接收或发送分配给相关的TS引脚。这些位的设置在自电容单扫描和多扫描模式下被忽略。CTSUCHTRC3[4]与TS28相关联，CTSUCHTRC3[7]与TS31相关联。

40.2.16 CTSU Channel Transmit/Receive Control Register 4 (CTSUCHTRC4)

Address(es): CTSU.CTSUCHTRC4 4008 100Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUCHTRC4[3:0]*1			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CTSUCHTRC4[3:0] *1	CTSU Channel Transmit/ Receive Control 4	0: Reception 1: Transmission. This bit specifies the TS34 pin.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The MCU does not support TS32, TS33, and TS35 pins. Therefore, CTSUCHTRC4[3] and CTSUCHTRC4[1:0] are read as 0. The write value should be 0.

Only set the CTSUCHTRC4 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC4[3:0]*1 bits (CTSU Channel Transmit/Receive Control 4)

In full-scan mode, the CTSUCHTRC4[3:0] bits allocate reception or transmission to the associated TS pins. The setting of these bits is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC4[2] is associated with TS34.

40.2.17 CTSU High-Pass Noise Reduction Control Register (CTSUDCLKC)

Address(es): CTSU.CTSUDCLKC 4008 1010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CTSUSSMOD[1:0]	CTSU Diffusion Clock Mode Select	Set these bits to 00b	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	CTSUSSCNT[1:0]	CTSU Diffusion Clock Mode Control	Set these bits to 11b	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUDCLKC register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSSMOD[1:0] bits (CTSU Diffusion Clock Mode Select)

The CTSUSSMOD[1:0] bits set the mode of the spectrum diffusion clock for high-pass noise reduction. When using the high-pass function, always fix these bits to 00b. If these bits are not set, the CTSU is unable to effectively reduce high-pass noise.

CTSUSSCNT[1:0] bits (CTSU Diffusion Clock Mode Control)

The CTSUSSCNT[1:0] bits adjust the amount of spectrum diffusion applied to reduce high-pass noise. When using the high-pass noise reduction function, always fix these bits to 11b. If these bits are not set, touch measurement might be performed incorrectly.

40.2.16 CTSU通道发送接收控制寄存器4(CTSUCHTRC4)

Address(es): CTSU.CTSUCHTRC4 4008 100Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUCHTRC4[3:0]*1			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CTSUCHTRC4[3:0] *1	CTSU Channel Transmit/ 接收控制4	0：接收1：发送。该位指定TS34引脚。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. MCU不支持TS32、TS33和TS35引脚。因此，CTSUCHTRC4[3]和CTSUCHTRC4[1:0]被读取为0。写入值应为0。

仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC4寄存器。

CTSUCHTRC4[3:0]*1位（CTSU通道发送接收控制4）

在全扫描模式下，CTSUCHTRC4[3:0]位将接收或发送分配给相关的TS引脚。这些位的设置在自电容单扫描和多扫描模式下被忽略。CTSUCHTRC4[2]与TS34相关联。

40.2.17 CTSU高通降噪控制寄存器(CTSUDCLKC)

Address(es): CTSU.CTSUDCLKC 4008 1010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CTSUSSMOD[1:0]	CTSU扩散时钟模式选择	将这些位设置为00b	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	CTSUSSCNT[1:0]	CTSU扩散时钟模式控制	将这些位设置为11b	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUDCLKC寄存器。

CTSUSSMOD[1:0]位（CTSU扩散时钟模式选择）

CTSUSSMOD[1:0]位设置频谱扩散时钟的模式以降低高通噪声。使用高通功能时，请始终将这些位固定为00b。如果未设置这些位，则CTSU无法有效降低高通噪声。

CTSUSSCNT[1:0]位（CTSU扩散时钟模式控制）

CTSUSSCNT[1:0]位调整应用的频谱扩散量以减少高通噪声。使用高通降噪功能时，请始终将这些位固定为11b。如果未设置这些位，则可能会错误地执行触摸测量。

40.2.18 CTSU Status Register (CTSUST)

Address(es): CTSU.CTSUST 4008 1011h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSUSTC[2:0]	CTSU Measurement Status Counter	These counters indicate the current measurement status: b2 b0 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5.	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CTSUDTSR	CTSU Data Transfer Status Flag	This flag indicates whether the measurement result stored in the sensor counter and the reference counter was read: 0: Read 1: Not read.	R
b5	CTSUSOVF	CTSU Sensor Counter Overflow Flag	This flag indicates an overflow on the sensor counter: 0: No overflow occurred 1: Overflow occurred.	R/W
b6	CTSUROVF	CTSU Reference Counter Overflow Flag	This flag indicates an overflow on the reference counter: 0: No overflow occurred 1: Overflow occurred.	R/W
b7	CTSUPS	CTSU Mutual Capacitance Status Flag	This flag indicates the measurement status in mutual-capacitance full-scan mode: 0: First measurement 1: Second measurement.	R

When using the CTSUCR0.CTSUINIT bit to clear an overflow flag, make sure that the CTSUCR0.CTSUSTRT bit is 0.

CTSUSTC[2:0] flags (CTSU Measurement Status Counter)

The CTSUSTC[2:0] flags are a counter indicating the current measurement status. For details on each status, see section 40.3.2.2, Status counter.

CTSUDTSR flag (CTSU Data Transfer Status Flag)

The CTSUDTSR flag indicates whether the measurement result stored in the sensor counter and the reference counter was read. This flag is set to 1 when measurement completes and 0 when the reference counter is read by software or the DTC. This flag can also be cleared with the CTSUCR0.CTSUINIT bit.

CTSUSOVF flag (CTSU Sensor Counter Overflow Flag)

The CTSUSOVF flag indicates when the sensor counter, CTSUSC, overflows. On overflow, the counter value reads as FFFFh. Measurement processing continues for the specified period.

No interrupt is generated when an overflow occurs. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. This flag can also be cleared with the CTSUCR0.CTSUINIT bit.

40.2.18 CTSU状态寄存器(CTSUST)

Address(es): CTSU.CTSUST 4008 1011h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CTSUSTC[2:0]	CTSU测量状态计数器	这些计数器指示当前测量状态：b2 b0 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5.	R
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	CTSUDTSR	CTSU数据传输状态标志	该标志指示存储在传感器计数器和参考计数器中的测量结果是否被读取：0：读取1：未读取。	R
b5	CTSUSOVF	CTSU传感器计数器溢出标志	该标志表示传感器计数器发生溢出：0：未发生溢出1：发生溢出。	R/W
b6	CTSUROVF	CTSU参考计数器溢出Flag	该标志表示参考计数器发生溢出：0：未发生溢出1：发生溢出。	R/W
b7	CTSUPS	CTSU互电容状态Flag	该标志指示互电容全扫描模式下的测量状态：0：第一次测量1：第二次测量。	R

使用CTSUCR0.CTSUINIT位清除溢出标志时，请确保CTSUCR0.CTSUSTRT位为0。

CTSUSTC[2:0]标志（CTSU测量状态计数器）

CTSUSTC[2:0]标志是指示当前测量状态的计数器。有关每个状态的详细信息，请参阅第40.3.2.2节，状态计数器。

CTSUDTSR标志（CTSU数据传输状态标志）

CTSUDTSR标志指示存储在传感器计数器和参考计数器中的测量结果是否被读取。此标志在测量完成时设置为1，当参考计数器由软件或DTC读取时设置为0。该标志也可以通过CTSUCR0.CTSUINIT位清零。

CTSUSOVF标志（CTSU传感器计数器溢出标志）

CTSUSOVF标志指示传感器计数器CTSUSC何时溢出。溢出时，计数器值读取为FFFFh。测量处理持续指定的时间。

发生溢出时不产生中断。要确定发生溢出的通道，请在测量完成后读取每个通道的测量结果，由测量结束中断发出信号。

当软件读取1后写入0时清除该标志。这个标志也可以用CTSUCR0.CTSUINIT bit.

CTSUROVF flag (CTSU Reference Counter Overflow Flag)

The CTSUROVF flag indicates when the reference counter, CTSURC, overflows. On overflow, the counter value reads as FFFFh. Measurement processing continues for the specified period.

No interrupt is generated even when an overflow occurs. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. This flag can also be cleared with the CTSUCR0.CTSUINIT bit.

CTSUPS flag (CTSU Mutual Capacitance Status Flag)

In mutual-capacitance full-scan mode, when CTSUCR1.CTSUMD[1:0] bits = 11b, the CTSUPS flag indicates whether the measurement is the first or second of two measurements for each channel. When measurement is stopped or in other measurement modes, this flag is always 0.

40.2.19 CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register (CTSUSSC)

Address(es): CTSU.CTSUSSC 4008 1012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	CTSUSSDIV[3:0]	CTSU Spectrum Diffusion Frequency Division Setting	These bits specify the spectrum diffusion frequency division setting based on the base clock frequency division setting	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CTSUSSDIV[3:0] bits (CTSU Spectrum Diffusion Frequency Division Setting)

The CTSUSSDIV[3:0] bits specify the spectrum diffusion frequency derived from the base clock frequency division setting. To calculate the correct setting for CTSUSSDIV[3:0], see the relationship between base clock frequencies and the settings in Table 40.5.

Table 40.5 Relationship between base clock frequencies and CTSUSSDIV[3:0] bit settings (1 of 2)

Base clock frequency fb (MHz)	CTSUSSDIV[3:0] bit setting
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b

CTSUROVF标志（CTSU参考计数器溢出标志）

CTSUROVF标志指示参考计数器CTSURC何时溢出。溢出时，计数器值读取为FFFFh。测量处理持续指定的时间。

即使发生溢出也不会产生中断。要确定发生溢出的通道，请在测量完成后读取每个通道的测量结果，由测量结束中断发出信号。

当软件读取1后写入0时清除该标志。这个标志也可以用
CTSUCR0.CTSUINIT bit.

CTSUPS标志（CTSU互电容状态标志）

在互电容全扫描模式下，当CTSUCR1.CTSUMD[1:0]位=11b时，CTSUPS标志指示测量是每个通道的两次测量中的第一个还是第二个。当测量停止或处于其他测量模式时，该标志始终为0。

40.2.19 CTSU高通降噪频谱扩散控制寄存器(CTSUSSC)

Address(es): CTSU.CTSUSSC 4008 1012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11 to b8	CTSUSSDIV[3:0]	CTSU频谱扩散频分设置	这些位指定基于基本时钟分频设置的频谱扩散分频设置	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CTSUSSDIV[3:0]位（CTSU频谱扩散频分设置）

CTSUSSDIV[3:0]位指定从基本时钟分频设置得出的频谱扩散频率。要计算CTSUSSDIV[3:0]的正确设置，请参见表40.5中基本时钟频率和设置之间的关系。

Table 40.5 基本时钟频率和CTSUSSDIV[3:0]位设置之间的关系(1of2)

基本时钟频率fb(MHz)	CTSUSSDIV[3:0]位设置
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b

Table 40.5 Relationship between base clock frequencies and CTSUSSDIV[3:0] bit settings (2 of 2)

Base clock frequency fb (MHz)	CTSUSSDIV[3:0] bit setting
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

40.2.20 CTSU Sensor Offset Register 0 (CTSUSO0)

Address(es): CTSU.CTSUSO0 4008 1014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSNUM[5:0]						CTSUSO[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	CTSUSO[9:0]	CTSU Sensor Offset Adjustment	These bits adjust the electronic capacitance when the electrode is not being touched: b9 b0 0 0 0 0 0 0 0 0 0 0: Current offset is 0 0 0 0 0 0 0 0 0 0 1: Current offset is 1 0 0 0 0 0 0 0 0 1 0: Current offset is 2 : : 1 1 1 1 1 1 1 1 1 0: Current offset is 1022 1 1 1 1 1 1 1 1 1 1: Current offset is maximum.	R/W
b15 to b10	CTSUSNUM[5:0]	CTSU Measurement Count Setting	These bits set the number of measurements	R/W

CTSUSO[9:0] bits (CTSU Sensor Offset Adjustment)

The CTSUSO[9:0] bits offset the sensor ICO input current generated from electrostatic capacitance during touch measurement when the electrode is not being touched. This prevents the CTSU sensor counter from overflowing. Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt is generated.

CTSUSNUM[5:0] bits (CTSU Measurement Count Setting)

The CTSUSNUM[5:0] bits specify how many times the measurement pulse count specified in the CTSUSDPRS.CTSUPRRATIO[3:0] and CTSUSDPRS.CTSUPRMODE[1:0] bits is repeated during the measurement time. The measurement pulse count is repeated (CTSUSNUM[5:0] bits + 1) times. Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt is generated.

Table 40.5 基本时钟频率和CTSUSSDIV[3:0]位设置之间的关系(2of2)

基本时钟频率fb(MHz)	CTSUSSDIV[3:0]位设置
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

40.2.20 CTSU传感器偏移寄存器0(CTSUSO0)

Address(es): CTSU.CTSUSO0 4008 1014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSNUM[5:0]						CTSUSO[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	CTSUSO[9:0]	CTSU传感器偏移调整	这些位在电极未被触摸 时调整电子电容：b9 b000000000000：当前偏移量为00000000001 ：当前偏移量为10000000010：当前偏移量为 2::1111111110：当前偏移为1022111111111 1：当前偏移最大。	R/W
b15 to b10	CTSUSNUM[5:0]	CTSU测量计数 Setting	这些位设置测量次数	R/W

CTSUSO[9:0]位（CTSU传感器偏移调整）

CTSUSO[9:0]位在电极未被触摸 时在触摸测量期间抵消由静电电容产生的传感器ICO输入电流。这可以防止CTSU传感器计数器溢出。在产生CTSU_CTSUWR中断后设置接下来要测量的TS引脚。

CTSUSNUM[5:0]位（CTSU测量计数设置）

CTSUSNUM[5:0]位指定测量脉冲计数的次数
CTSUSDPRS.CTSUPRRATIO[3:0]和CTSUSDPRS.CTSUPRMODE[1:0]位在测量期间重复。测量脉冲计数重复(CTSUSNUM[5:0]位+1)次。在产生CTSU_CTSUWR中断后设置接下来要测量的TS引脚。

40.2.21 CTSU Sensor Offset Register 1 (CTSUSO1)

Address(es): CTSU.CTSUSO1 4008 1016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSURICOA[7:0]	CTSU Reference ICO Current Adjustment	These bits adjust the input current of the reference ICO: b7 b0 0 0 0 0 0 0 0 0: Current offset is 0 0 0 0 0 0 0 0 1: Current offset is 1 0 0 0 0 0 0 1 0: Current offset is 2. : : 1 1 1 1 1 1 1 0: Current offset is 254 1 1 1 1 1 1 1 1: Current offset is maximum.	R/W
b12 to b8	CTSUSDPA[4:0]	CTSU Base Clock Setting	These bits are used to generate the base clock: b12 b8 0 0 0 0 0: Operating clock divided by 2*1 0 0 0 0 1: Operating clock divided by 4 0 0 0 1 0: Operating clock divided by 6 0 0 0 1 1: Operating clock divided by 8 0 0 1 0 0: Operating clock divided by 10 0 0 1 0 1: Operating clock divided by 12 0 0 1 1 0: Operating clock divided by 14 0 0 1 1 1: Operating clock divided by 16 0 1 0 0 0: Operating clock divided by 18 0 1 0 0 1: Operating clock divided by 20 0 1 0 1 0: Operating clock divided by 22 0 1 0 1 1: Operating clock divided by 24 0 1 1 0 0: Operating clock divided by 26 0 1 1 0 1: Operating clock divided by 28 0 1 1 1 0: Operating clock divided by 30 0 1 1 1 1: Operating clock divided by 32 1 0 0 0 0: Operating clock divided by 34 1 0 0 0 1: Operating clock divided by 36 1 0 0 1 0: Operating clock divided by 38 1 0 0 1 1: Operating clock divided by 40 1 0 1 0 0: Operating clock divided by 42 1 0 1 0 1: Operating clock divided by 44 1 0 1 1 0: Operating clock divided by 46 1 0 1 1 1: Operating clock divided by 48 1 1 0 0 0: Operating clock divided by 50 1 1 0 0 1: Operating clock divided by 52 1 1 0 1 0: Operating clock divided by 54 1 1 0 1 1: Operating clock divided by 56 1 1 1 0 0: Operating clock divided by 58 1 1 1 0 1: Operating clock divided by 60 1 1 1 1 0: Operating clock divided by 62 1 1 1 1 1: Operating clock divided by 64.	R/W
b14, b13	CTSUICOG[1:0]	CTSU ICO Gain Adjustment	These bits adjust the output frequency gain of the sensor ICO and the reference ICO: b14 b13 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not set the CTSUSDPA[4:0] bits to 00000b while the high-pass noise reduction function is turned off (CTSUSDPRS.CTSUSOFF bit = 1) in mutual-capacitance full-scan mode (CTSUCR1.CTSUMD[1:0] bits = 11b).

After a CTSU_CTSUWR interrupt is generated, write first to the CTSUSSC register, then to the CTSUSO0 register, and

40.2.21 CTSU传感器偏移寄存器1(CTSUSO1)

Address(es): CTSU.CTSUSO1 4008 1016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSURICOA[7:0]	CTSU参考ICO电流 Adjustment	这些位调整参考ICO的输入电流：b7 b000000000：当前偏移为000000001：当前偏移为100000010：当前偏移为2。::111 11110：当前偏移量为25411111111：当前偏移量最大。	R/W
b12 to b8	CTSUSDPA[4:0]	CTSU基本时钟设置	这些位用于生成基本时钟：b12 b800000：运行时钟除以2*100001：运行时钟除以400010：运行时钟除以600011：运行时钟除以800100：工作时钟除以1000101：工作时钟除以1200110：工作时钟除以1400111：工作时钟除以1601000：工作时钟分频by1801001：运行时钟除以2001010：运行时钟除以2201011：运行时钟除以2401100：运行时钟除以2601101：运行时钟除以2801110：运行时钟除以3001111：运行时钟除以3210000：运行时钟除以3410001：运行时钟除以3610010：运行时钟除以3810011：运行时钟除以4010100：运行时钟除以4210101：运行时钟除以4410110:工作时钟除以4610111：运行时钟除以4811000：运行时钟除以5011001：运行时钟除以5211010：运行时钟除以5411011：运行时钟除以5611100：运行时钟除以5811101：运行时钟除以6011110：运行时钟除以6211111：运行时钟除以64。	R/W
b14, b13	CTSUICOG[1:0]	CTSUICO增益调整	这些位调整传感器ICO和参考ICO的输出频率增益：b14b13 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain.	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 在互电容全扫描模式（CTSUCR1.CTSUMD[1:0]位）关闭高通降噪功能（CTSUSDPRS.CTSUSOFF位=1）时，请勿将CTSUSDPA[4:0]位设置为00000b=11b)。

产生CTSU_CTSUWR中断后，先写入CTSUSSC寄存器，再写入CTSUSO0寄存器，然后

then to the CTSUSO1 register. The write to the CTSUSO1 register causes a transition to Status 3 (see Table 40.6 and Table 40.7). Set all the bits in a single operation when writing to the CTSUSO1 register.

CTSURICOA[7:0] bits (CTSU Reference ICO Current Adjustment)

The CTSURICOA[7:0] bits adjust the oscillation frequency using the input current of the reference ICO.

CTSUSDPA[4:0] bits (CTSU Base Clock Setting)

The CTSUSDPA[4:0] bits select a base clock used as the source for the sensor drive pulse by dividing the operating clock. For details on the setting procedure, see section 40.3.2.1, Initial setting flow.

CTSUICOG[1:0] bits (CTSU ICO Gain Adjustment)

The CTSUICOG[1:0] bits adjust the output frequency gain of the sensor ICO and the reference ICO. In general, set these bits to 00b for the maximum gain. If changes in the capacitance between when the electrode is touched and when it is not touched greatly exceed the dynamic range of the sensor ICO, adjust the gain appropriately with this setting.

40.2.22 CTSU Sensor Counter (CTSUSC)

Address(es): CTSU.CTSUSC 4008 1018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	CTSUSC[15:0]	CTSU Sensor Counter	These bits indicate the measurement result of the sensor ICO. These bits read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt is generated, read first from the CTSUSC counter, then from the CTSURC counter.

CTSUSC[15:0] bits (CTSU Sensor Counter)

The CTSUSC[15:0] bits are configured as an increment counter for the sensor ICO clock. Read these bits after a CTSU_CTSURD interrupt is generated. After the CTSURC counter is read, these bits are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags change to 100b) in the next measurement. These bits can also be cleared using the CTSUCR0.CTSUINIT bit.

40.2.23 CTSU Reference Counter (CTSURC)

Address(es): CTSU.CTSURC 4008 101Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSURC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	CTSURC[15:0]	CTSU Reference Counter	These bits indicate the measurement result of the reference ICO. These bits read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt is generated, read first from the CTSUSC counter, then from the CTSURC counter. Status 3 continues until the CTSURC counter is read, even if the stabilization time specified for Status 3 elapses.

然后到CTSUSO1寄存器。写入CTSUSO1寄存器会导致转换到状态3（参见表40.6和表40.7）。写入CTSUSO1寄存器时，在一次操作中设置所有位。

CTSURICOA[7:0]位（CTSU参考ICO电流调整）

CTSURICOA[7:0]位使用参考ICO的输入电流调整振荡频率。

CTSUSDPA[4:0]位（CTSU基本时钟设置）

CTSUSDPA[4:0]位通过对工作时钟进行分频来选择用作传感器驱动脉冲源的基本时钟。有关设置步骤的详细信息，请参阅第40.3.2.1节，初始设置流程。

CTSUICOG[1:0]位（CTSUICO增益调整）

CTSUICOG[1:0]位调整传感器ICO和参考ICO的输出频率增益。通常，将这些位设置为00b以获得最大增益。如果触摸电极和未触摸电极之间的电容变化大大超过传感器ICO的动态范围，请使用此设置适当调整增益。

40.2.22 CTSU传感器计数器(CTSUSC)

Address(es): CTSU.CTSUSC 4008 1018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSC[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	CTSUSC[15:0]	CTSU传感器计数器	这些位表示传感器ICO的测量结果。当发生溢出时，这些位读取FFFFh。	R

在产生CTSU_CTSURD中断后，首先从CTSUSC计数器读取，然后从CTSURC计数器读取。

CTSUSC[15:0]位（CTSU传感器计数器）

CTSUSC[15:0]位配置为传感器ICO时钟的增量计数器。后读取这些位
产生CTSU_CTSURD中断。读取CTSURC计数器后，这些位会在CTSU测量状态计数器值在下一次测量中立即变为状态4（CTSUST.CTSUSTC[2:0]标志变为100b）之前被清除。这些位也可以使用CTSUCR0.CTSUINIT位清零。

40.2.23 CTSU参考计数器(CTSURC)

Address(es): CTSU.CTSURC 4008 101Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSURC[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	CTSURC[15:0]	CTSU参考计数器	这些位表示参考ICO的测量结果。当发生溢出时，这些位读取FFFFh。	R

在产生CTSU_CTSURD中断后，首先从CTSUSC计数器读取，然后从CTSURC计数器读取。
状态3一直持续到读取CTSURC计数器为止，即使为状态3指定的稳定时间已过。

CTSURC[15:0] bits (CTSU Reference Counter)

The CTSURC[15:0] bits are configured as an increment counter for the reference ICO clock. The reference ICO optimizes touch measurement performed by the sensor ICO. There is some deviation depending on the internal sensor ICO and the reference ICO in the CTSU, but both ICOs have almost the same characteristics, including the dynamic range and the current-to-frequency characteristics. The range of current amount that can be set in the reference ICO current adjustment bits is about the same as the dynamic range of both ICOs, and the current amount input to the sensor ICO must be within this dynamic range. To ensure this, use the reference ICO to check the differences between the ICOs and measure the current-to-oscillation frequency characteristics. The reference ICO oscillation frequency can be obtained from the reference ICO counter, and the ICO oscillation frequency (counter value/measurement time) for the input current amount can be measured by setting the value in the reference ICO current adjustment bits and measuring the reference ICO counter. The reference ICO counter value measured using the maximum value in the reference ICO current adjustment bits is the maximum value of the ICO dynamic range. The current to the sensor ICO must be offset in the offset adjustment bits so that the sensor ICO counter value does not exceed this value.

Read the CTSURC[15:0] bits after a CTSU_CTSURD interrupt occurs. After these bits are read, they are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags change to 100b) in the next measurement. These bits can also be cleared with the CTSUCR0.CTSUINIT bit.

40.2.24 CTSU Error Status Register (CTSUERRS)

Address(es): CTSU.CTSUERRS 4008 101Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0.	R
b15	CTSUICOMP	TSCAP Voltage Error Monitor	This bit monitors the error status of the TSCAP voltage: 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage.	R

CTSUICOMP bit (TSCAP Voltage Error Monitor)

If the offset current amount set in the CTSUSO1 register exceeds the sensor ICO input current during touch measurement, the TSCAP voltage becomes abnormal and touch measurement cannot be performed correctly. This bit monitors the TSCAP voltage and is set to 1 if the voltage becomes abnormal.

If the TSCAP voltage becomes abnormal, the sensor ICO counter value is undefined, but touch measurement completes normally, therefore it is difficult to detect an abnormality by reading the sensor ICO counter value. If the CTSU reference ICO current adjustment bits (CTSURICOA[7:0]) in the CTSUSO1 register are set to a value other than 0, check this bit when touch measurement completes.

This bit is cleared by writing 0 to the CTSUCR1.CTSUPON bit and turning off the power supply.

40.3 Operation

40.3.1 Principles of Measurement Operation

Figure 40.4 shows the measurement circuit.

CTSURC[15:0]位（CTSU参考计数器）

CTSURC[15:0]位配置为参考ICO时钟的增量计数器。参考ICO优化了传感器ICO执行的触摸测量。CTSU中的内部传感器ICO和参考ICO存在一些偏差，但两种ICO具有几乎相同的特性，包括动态范围和电流频率特性。参考ICO电流调整位可设置的电流量范围与两个ICO的动态范围大致相同，输入到传感器ICO的电流量必须在此动态范围内。为确保这一点，请使用参考ICO检查ICO之间的差异并测量电流–振荡频率特性。参考ICO振荡频率可以从参考ICO计数器获得，通过设置参考ICO电流调整位中的值并测量参考ICO计数器，可以测量输入电流量的ICO振荡频率（计数器值测量时间）.使用参考ICO电流调整位中的最大值测量的参考ICO计数器值是ICO动态范围的最大值。传感器ICO的电流必须在偏移调整位中进行偏移，以使传感器ICO计数器值不超过此值。

在CTSU_CTSURD中断发生后读取CTSURC[15:0]位。读取这些位后，在CTSU测量状态计数器值在下一次测量中立即变为状态4（CTSUST.CTSUSTC[2:0]标志变为100b）之前将它们清零。这些位也可以通过CTSUCR0.CTSUINIT位清零。

40.2.24 CTSU错误状态寄存器(CTSUERRS)

Address(es): CTSU.CTSUERRS 4008 101Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b14 to b0	—	Reserved	这些位读为0。	R
b15	CTSUICOMP	TSCAP电压错误监视器	该位监控TSCAP电压的错误状态：0：正常TSCAP电压1：异常TSCAP电压。	R

CTSUICOMP位（TSCAP电压错误监视器）

如果CTSUSO1寄存器中设置的偏移电流量在触摸测量期间超过传感器ICO输入电流，则TSCAP电压会异常，无法正确执行触摸测量。该位监控TSCAP电压，如果电压异常则设置为1。

如果TSCAP电压异常，则传感器ICO计数器值未定义，但触摸测量正常完成，因此很难通过读取传感器ICO计数器值来检测异常。如果CTSUSO1寄存器中的CTSU参考ICO电流调整位(CTSURICOA[7:0])设置为0以外的值，则在触摸测量完成时检查该位。

通过向CTSUCR1.CTSUPON位写入0并关闭电源来清除该位。

40.3 Operation

40.3.1 测量操作原理

图40.4显示了测量电路。

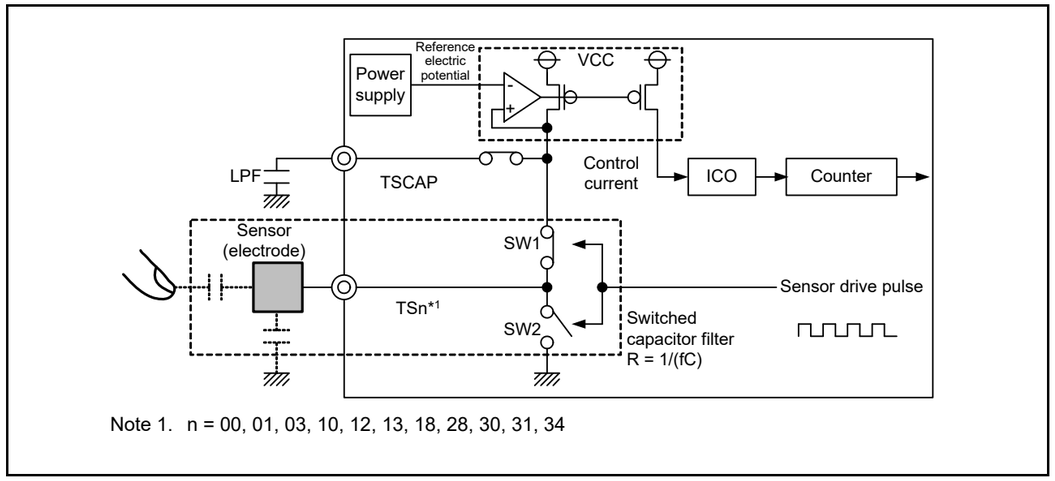


Figure 40.4 Measurement circuit

Figure 40.5 to Figure 40.7 explain the electrostatic capacitance measurement operation principles of the CTSU current frequency conversion method. The operation is as follows:

1. The electrostatic capacitance of the electrode is charged by turning SW1 on and SW2 off (Figure 40.5).
2. The charged capacitance is discharged by turning SW1 off and SW2 on (See Figure 40.6).
3. Current flows to the switched capacitor filter by repeatedly charging and discharging the electrodes as in step 1. and step 2.. At this point, if a finger is in close proximity, the capacitance and the flowing current change. A clock is generated by supplying the control current, a current that is proportional to the amount of the current flowing through the switched capacitor filter, from the circuit that generates the TSCAP power supply to the ICO. The counter measures the clock frequency that changes depending on whether a finger is in close proximity. Software uses the value read from the counter to determine contact with a finger (Figure 40.7).

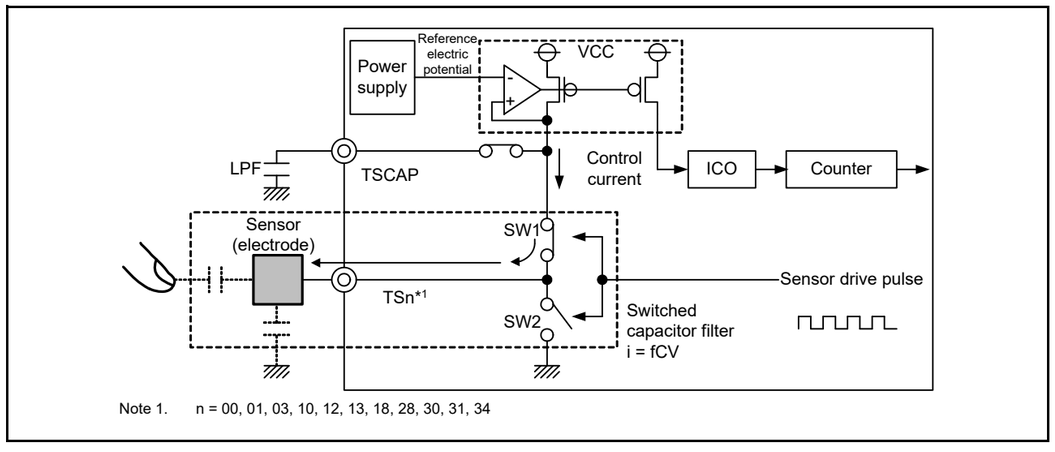


Figure 40.5 Charging operation

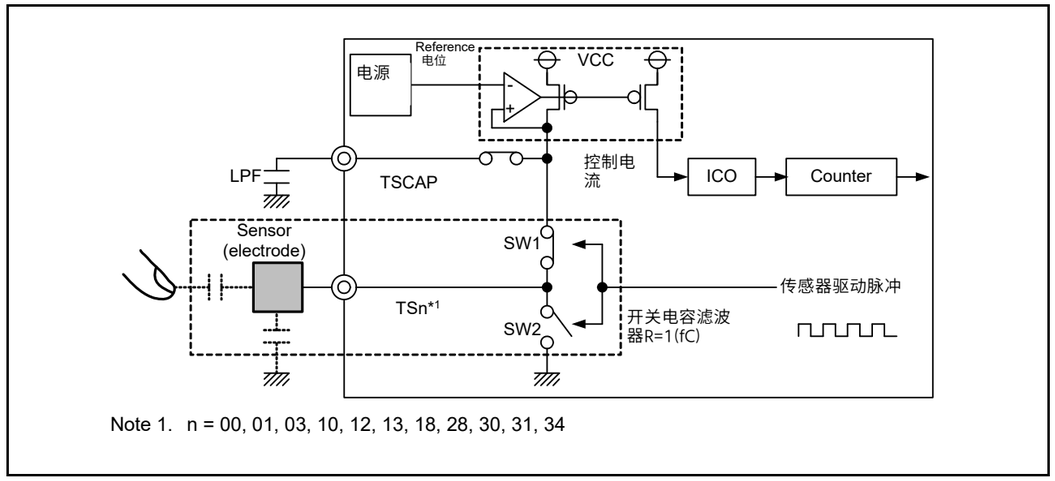


Figure 40.4 测量电路

图40.5至图40.7说明了CTSU电流变频方式的静电电容测量操作原理。操作如下：

1. 通过打开SW1和关闭SW2对电极的静电电容进行充电（图40.5）。
2. 通过关闭SW1和打开SW2对充电的电容进行放电（参见图40.6）。
3. 电流通过如步骤1.和步骤2.中的电极反复充电和放电而流向开关电容器滤波器。此时，如果手指靠近，则电容和流动电流会发生变化。通过从产生TSCAP电源的电路向ICO提供控制电流来产生时钟，该电流与流过开关电容滤波器的电流量成正比。计数器测量时钟频率，该频率根据手指是否靠近而变化。软件使用从计数器读取的值来确定与手指的接触（图40.7）。

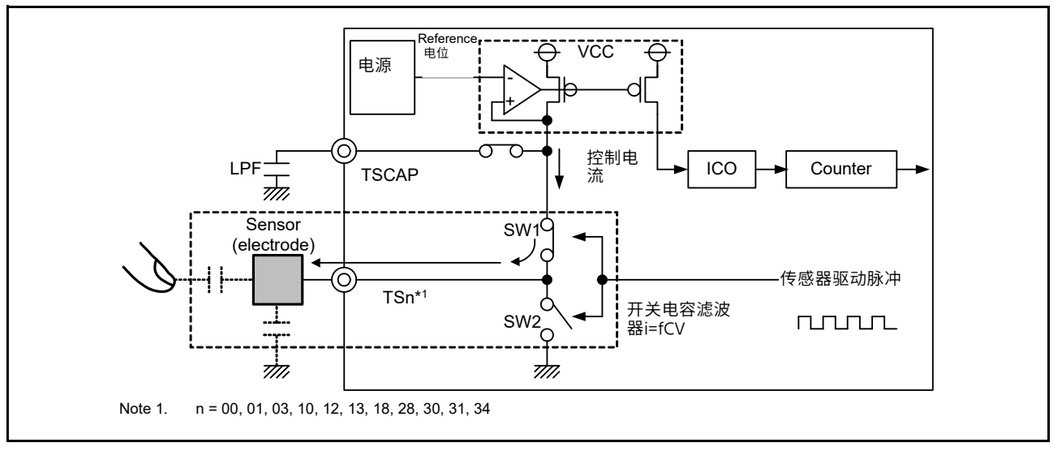


Figure 40.5 充电操作

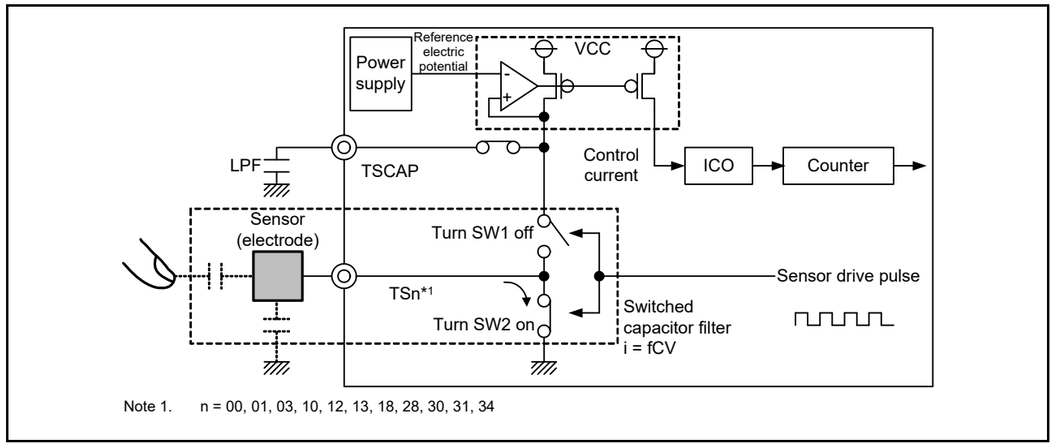


Figure 40.6 Discharging operation

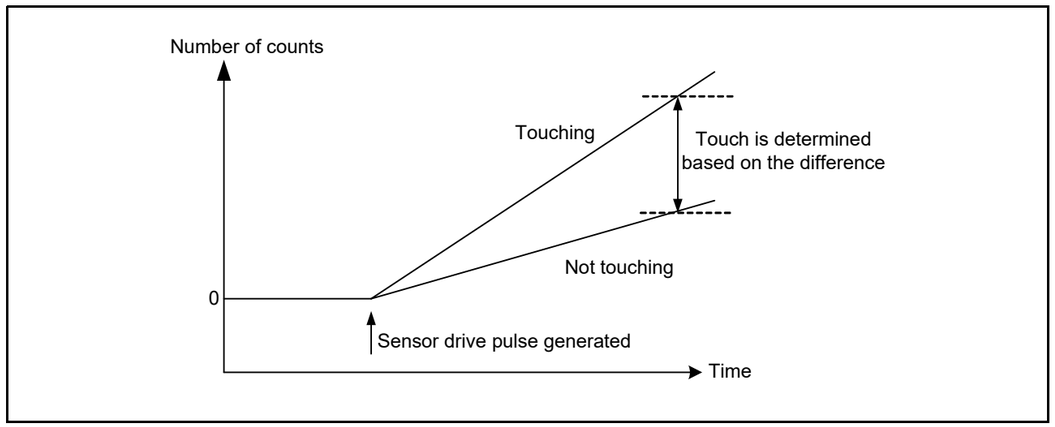


Figure 40.7 Change in measured value when finger is touching and not touching

40.3.2 Measurement Modes

The CTSU supports self-capacitance and mutual-capacitance methods. Figure 40.8 shows these methods.

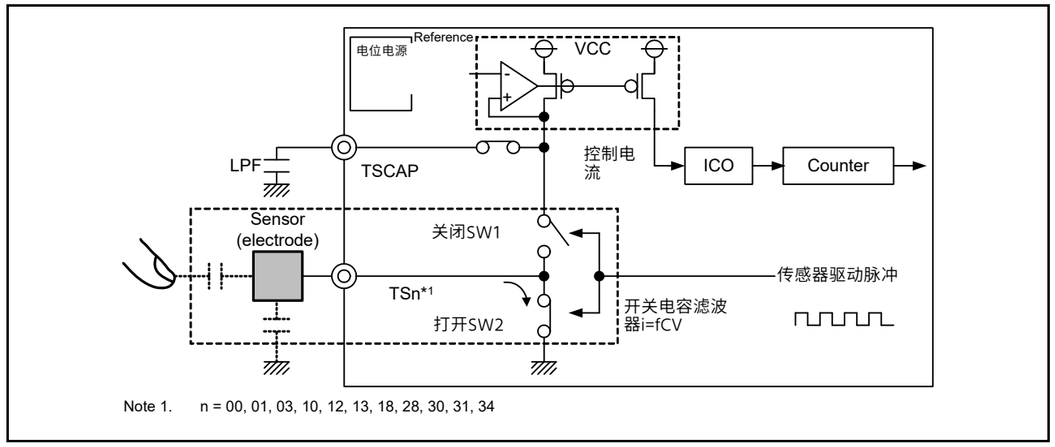


Figure 40.6 卸料作业

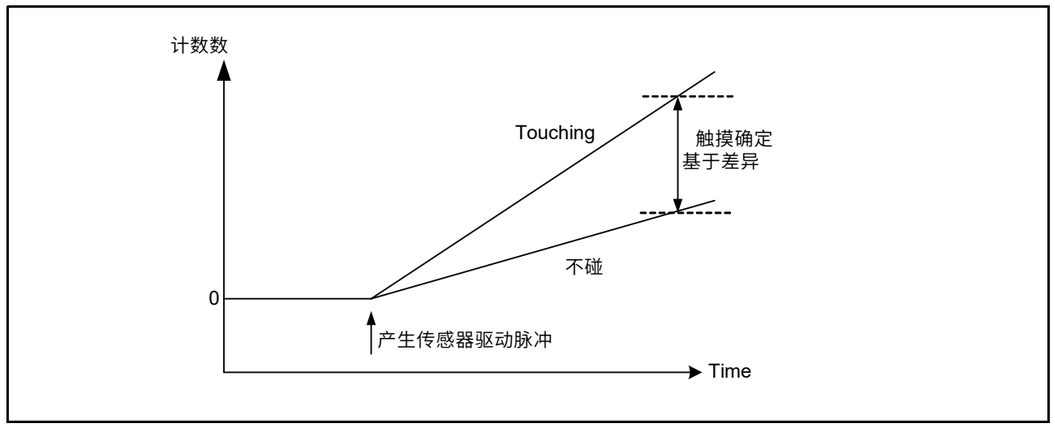


Figure 40.7 手指接触和不接触时测量值的变化

40.3.2 测量模式

CTSU支持自电容和互电容方法。图40.8显示了这些方法。

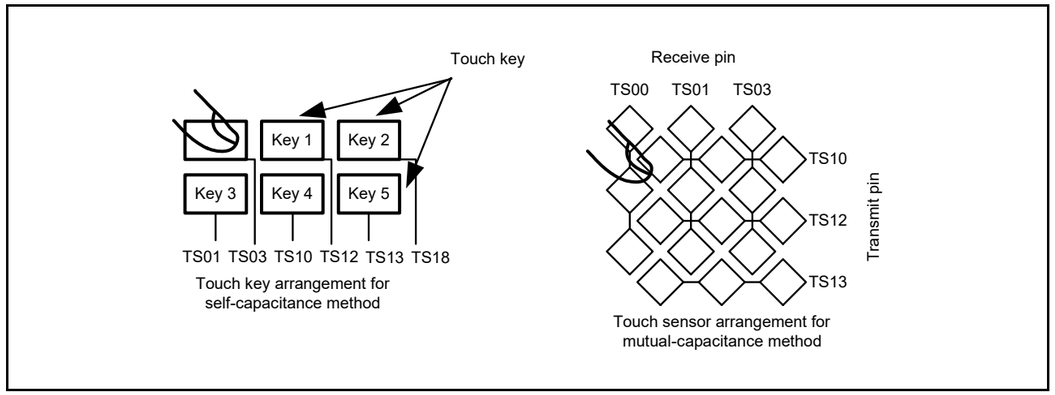


Figure 40.8 Overview of self-capacitance method and mutual-capacitance method

In the self-capacitance method, a single touch pin is allocated to a single touch key to measure individual electrostatic capacitance when a finger is in close proximity. In this method, single scan and multi-scan can be used as measurement modes. In the mutual-capacitance method, the capacitance between two opposing electrodes (transmit and receive pins) is measured.

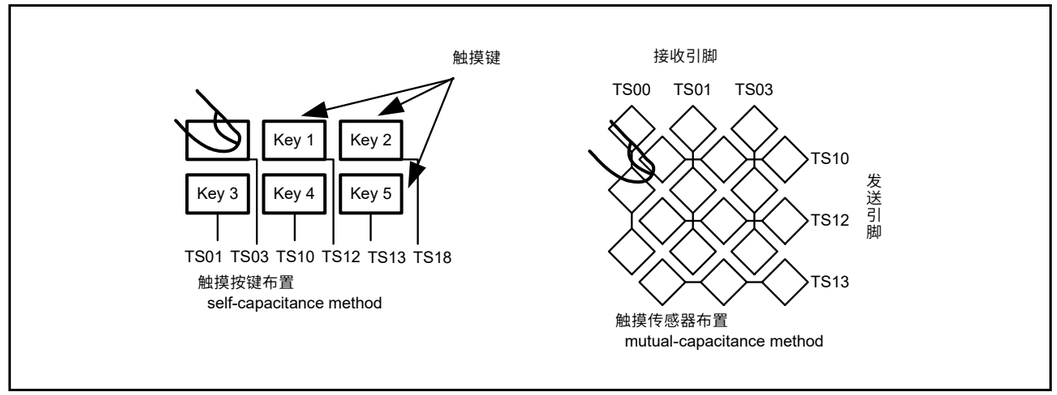


Figure 40.8 自电容法和互电容法概述

在自电容法中，将单个触摸引脚分配给单个触摸键，以在手指靠近时测量单个静电电容。在这种方法中，可以使用单次扫描和多次扫描作为测量模式。在互电容法中，测量两个相对电极（发送和接收引脚）之间的电容。

40.3.2.1 Initial setting flow

Figure 40.9 shows the flow for the CTSU initial setting.

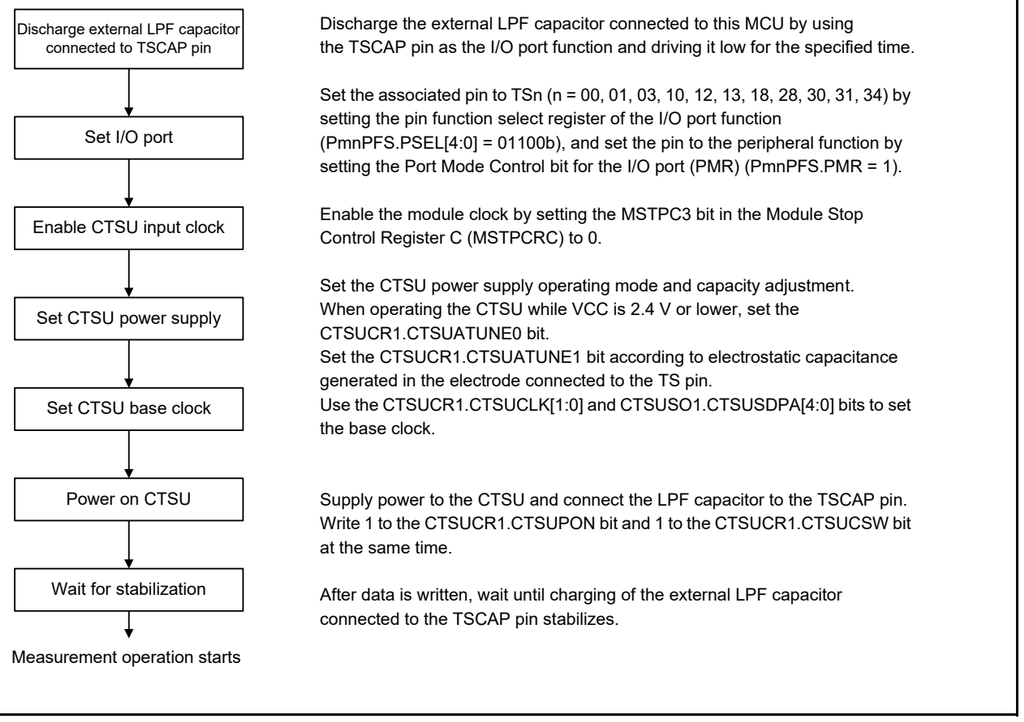


Figure 40.9 CTSU initial setting flow

Figure 40.10 shows the flow for stopping CTSU operation and invoking the standby state.

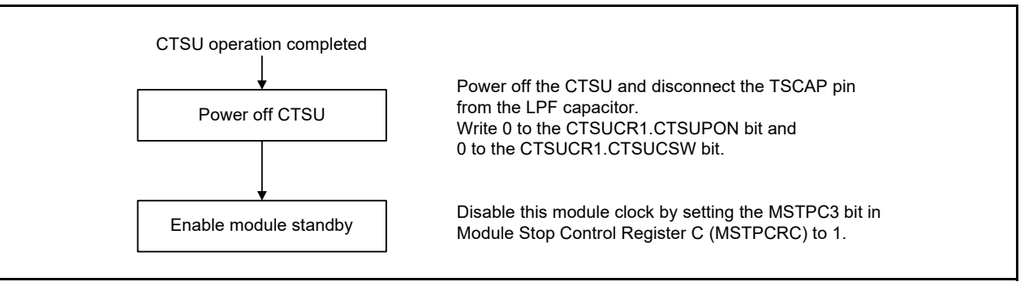


Figure 40.10 CTSU stopping flow

To restart operation, follow the initial setting flow shown in Figure 40.9.

40.3.2.1 初始设定流程

图40.9显示了CTSU初始设置的流程。

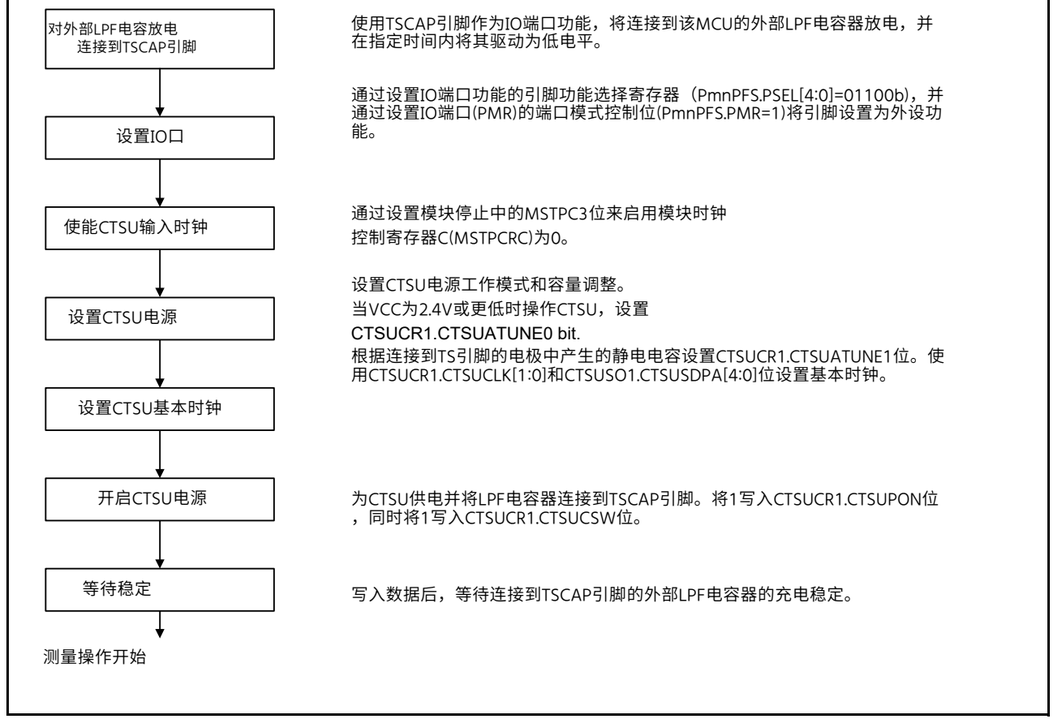


Figure 40.9 CTSU初始设定流程

图40.10显示了停止CTSU操作并调用待机状态的流程。

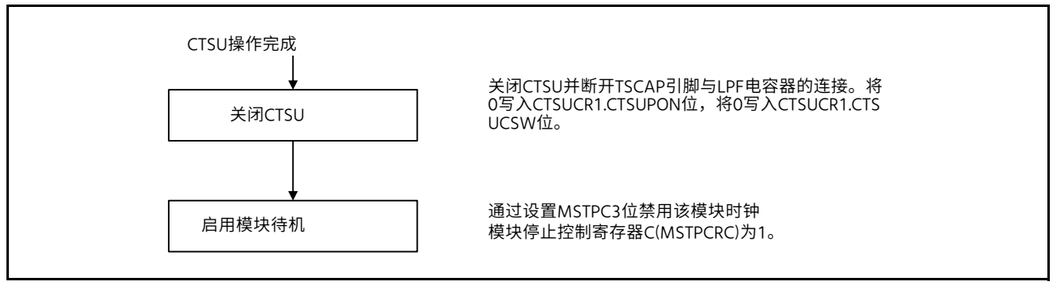
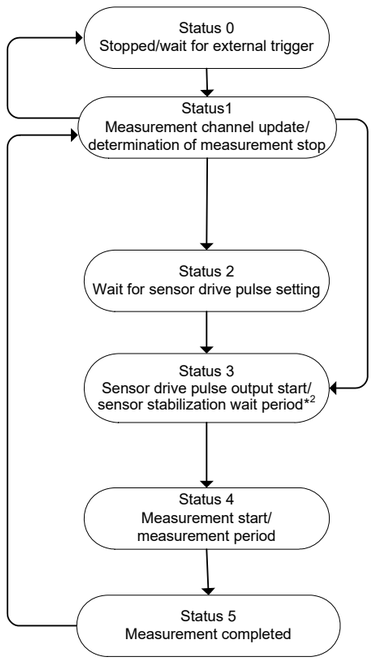


Figure 40.10 CTSU停止流量

要重新开始运行，请按照图40.9所示的初始设置流程进行操作。

40.3.2.2 Status counter

The measurement status counter of the CTSU Status Register (CTSUST) indicates the current measurement status. The measurement status applies to all three modes. Figure 40.11 shows the status operation transitions.



Conditions for transition to Status 1:
- CTSUCR0.CTSUCAP bit = 0: CTSUCR0.CTSUSTRT bit = 1
- CTSUCR0.CTSUCAP bit = 1: CTSUCR0.CTSUSTRT bit = 1 and the rising edge of the external trigger is detected.

Condition for transition to Status 0:
- There is no channel to be measured next.
(A CTSU_CTSUFN interrupt is generated and measurement is stopped.)

Condition for transition to Status 2:
- Update of the measurement channel is completed.

Condition for transition to Status 3:
- CTSUST.CTSUPS = 1 (second measurement) in mutual capacitance full-scan mode.

Condition for transition to Status 3:
- Write access to the CTSUSO1 register.*1

Condition for transition to Status 4:
- CTSUST.CTSUDTSR flag = 0 when the sensor stabilization elapses after supply of the sensor drive pulse starts.

Condition for transition to Status 5:
- The measurement time elapses after measurement is started.
For details on the measurement time, see section 40.3.3.1, Sensor stabilization wait time and measurement time.

Condition for transition to Status 1:
- After two clocks of the operating clock elapse.

Note 1. When using the DTC/ICU to set the registers in the CTSU_CTSUWR interrupt handling, write to the CTSUSO1 register last.
Note 2. If the CTSUST.CTSUDTSR flag = 1, wait until the previous measurement result is transferred.

Figure 40.11 Status operation transitions

The status counter transitions to Status 0 when all of the specified measurement channels are measured.

The CTSUCR0.CTSUSTRT bit is set to 0 by hardware when a software trigger is used. When an external trigger is used, the value 1 is retained, and the CTSU waits for the next trigger.

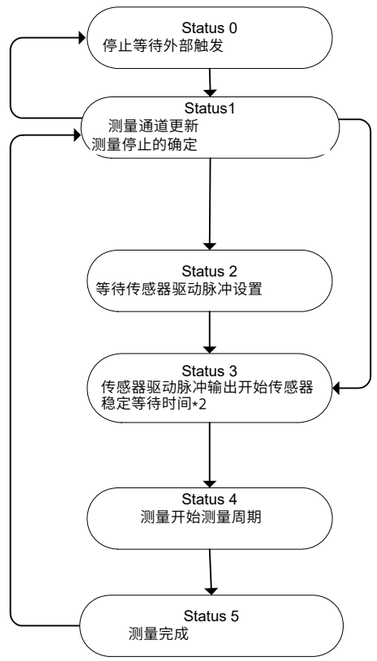
When operation is forced to stop during measurement or the trigger wait state, by a simultaneous 0 write to the CTSUCR0.CTSUSTRT bit and a 1 write to the CTSUCR0.CTSUINIT bit, the status transitions to Status 0 and measurement stops.

If the channel to be measured is not set in the CTSUMCH0, CTSUCHAC0 to CTSUCHAC4, and CTSUCHTRC0 to CTSUCHTRC4 registers, a CTSU_CTSUFN interrupt is generated immediately after a transition to Status 1, then the status transitions to Status 0. The following are cases when there is no channel to be measured:

- No measurement target channel is specified in the CTSUCHAC0 to CTSUCHAC4 registers
- In self-capacitance single scan mode, the channel specified in the CTSUMCH0 register is not a measurement target in the CTSUCHAC0 to CTSUCHAC4 registers
- In full-scan modes, there is no transmit channel or receive channel to be measured based on the combined settings of the CTSUCHAC0 to CTSUCHAC4, and CTSUCHTRC0 to CTSUCHTRC4 registers.

40.3.2.2 状态计数器

CTSU状态寄存器(CTSUST)的测量状态计数器指示当前测量状态。测量状态适用于所有三种模式。图40.11显示了状态操作转换。



过渡到状态1的条件：
CTSUCR0.CTSUCAP位=0：CTSUCR0.CTSUSTRT位=1 CTSUCR0.CTSUCAP位=1：CTSUCR0.CTSUSTRT位=1，并且检测到外部触发的上升沿。

转换到状态0的条件：
接下来没有要测量的通道。
（产生CTSU_CTSUFN中断并停止测量。）转换到状态2的条件：

测量通道更新完成。转换到状态3的条件：

CTSUST.CTSUPS=1（第二次测量）在互电容全扫描模式下。

转换到状态3的条件：
对CTSUSO1寄存器的写访问。*1

转换到状态4的条件：
CTSUST.CTSUDTSR标志=0，当传感器驱动脉冲开始供应后传感器稳定结束时。

转换到状态5的条件：
测量开始后测量时间已过。
有关测量时间的详细信息，请参阅第40.3.3.1节，传感器稳定等待时间和测量时间。

转换到状态1的条件：
在运行时钟的两个时钟过去之后。

Note 1. 使用DTCICU设置CTSU_CTSUWR中断处理中的寄存器时，最后写入CTSUSO1寄存器。
Note 2. 如果CTSUST.CTSUDTSR标志=1，则等待前一个测量结果被传输。

Figure 40.11 状态操作转换

当测量所有指定的测量通道时，状态计数器转换为状态0。

当使用软件触发时，CTSUCR0.CTSUSTRT位由硬件设置为0。当使用外部触发时，值1保持不变，CTSU等待下一次触发。

在测量或触发等待状态期间强制停止操作时，通过同时向CTSUCR0.CTSUSTRT位写入0和向CTSUCR0.CTSUINIT位写入1，状态转换为状态0并停止测量。

如果要测量的通道未在CTSUCH0、CTSUCHAC0至CTSUCHAC4和CTSUCHTC0至CTSUCHTC4寄存器中设置，则在转换为状态1后立即产生CTSU_CTSUFN中断，然后状态转换为状态0。是没有要测量的通道：

- CTSUCHAC0至CTSUCHAC4寄存器中未指定测量目标通道
- 在自电容单次扫描模式下，CTSUCH0寄存器中指定的通道不是CTSUCHAC0至CTSUCHAC4寄存器中的测量目标
- 在全扫描模式下，根据CTSUCHAC0至CTSUCHAC4和CTSUCHAC0至CTSUCHTC4寄存器的组合设置，没有要测量的发送通道或接收通道。

40.3.2.3 Self-capacitance single scan mode operation

In self-capacitance single scan mode, electrostatic capacitance is measured on one channel. Figure 40.12 shows the software flow and an operation example, and Figure 40.13 shows the timing.

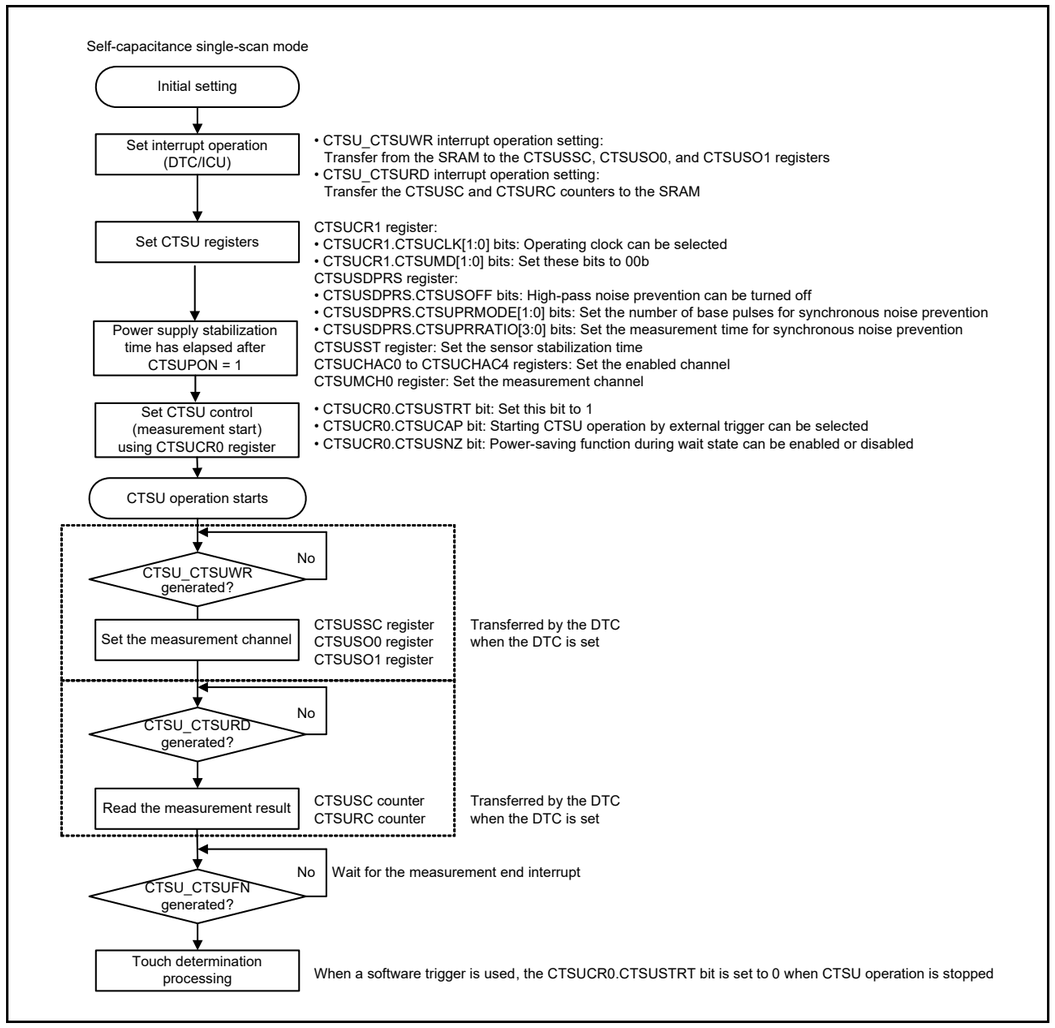


Figure 40.12 Software flow and operation example for self-capacitance single scan mode

40.3.2.3 自电容单次扫描模式操作

在自电容单次扫描模式下，在一个通道上测量静电电容。图40.12显示了软件流程和操作示例，图40.13显示了时序。

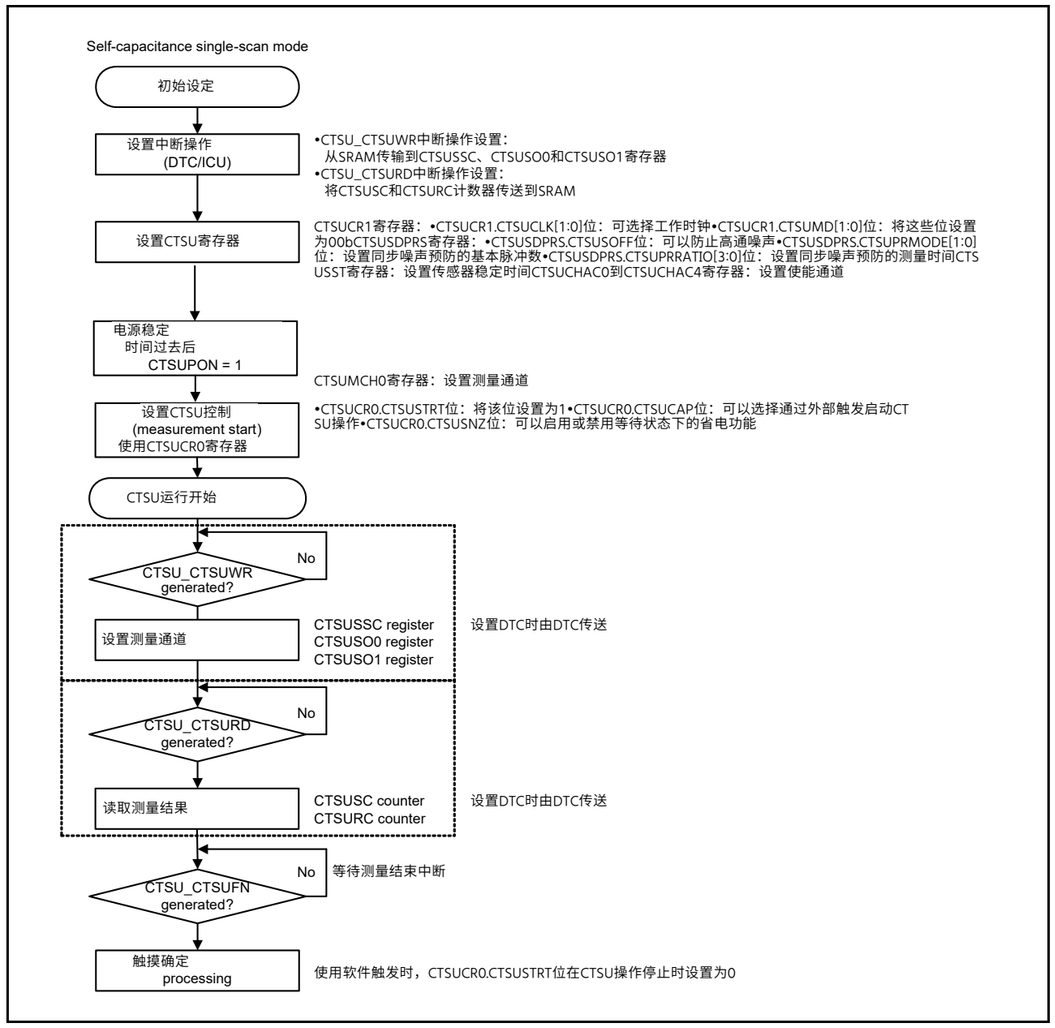


Figure 40.12 自电容单次扫描模式的软件流程和操作示例

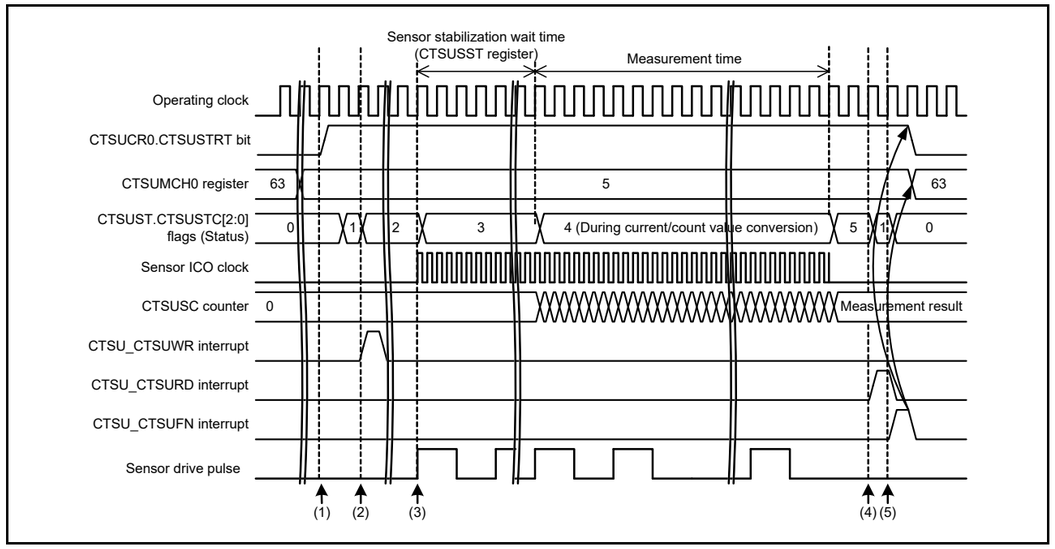


Figure 40.13 Timing of self-capacitance single scan mode when the measurement start condition is a software trigger

The following sequence describes the operation shown in Figure 40.13:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined according to the preset conditions, a request to set the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time elapse, and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. A measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

Table 40.6 lists the touch pin states in self-capacitance single scan mode.

Table 40.6 Touch pin states in self-capacitance single scan mode

	Touch pin	
Status	**Measured channel**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

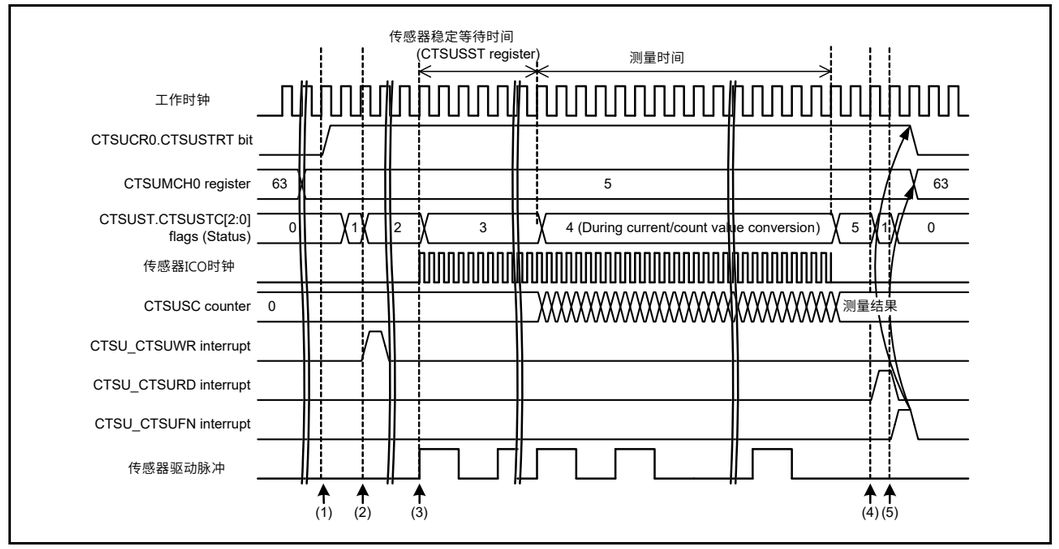


Figure 40.13 测量开始条件为软件触发时的自电容单次扫描模式时序

以下序列描述了图40.13所示的操作：

1. 进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。
2. 根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。
3. 写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。
4. 在传感器稳定等待时间和测量时间过去，测量停止后，输出测量结果读取请求（CTSU_CTSURD）。
5. 输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

表40.6列出了自电容单次扫描模式下的触摸引脚状态。

Table 40.6 自电容单次扫描模式下的触摸引脚状态

	触摸针	
Status	**测量通道**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

40.3.2.4 Self-capacitance multi-scan mode operation

In self-capacitance multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets in the CTSUCHAC0 to CTSUCHAC4 registers is measured sequentially in ascending order. Figure 40.14 shows the software flow and an operation example, and Figure 40.15 shows the timing.

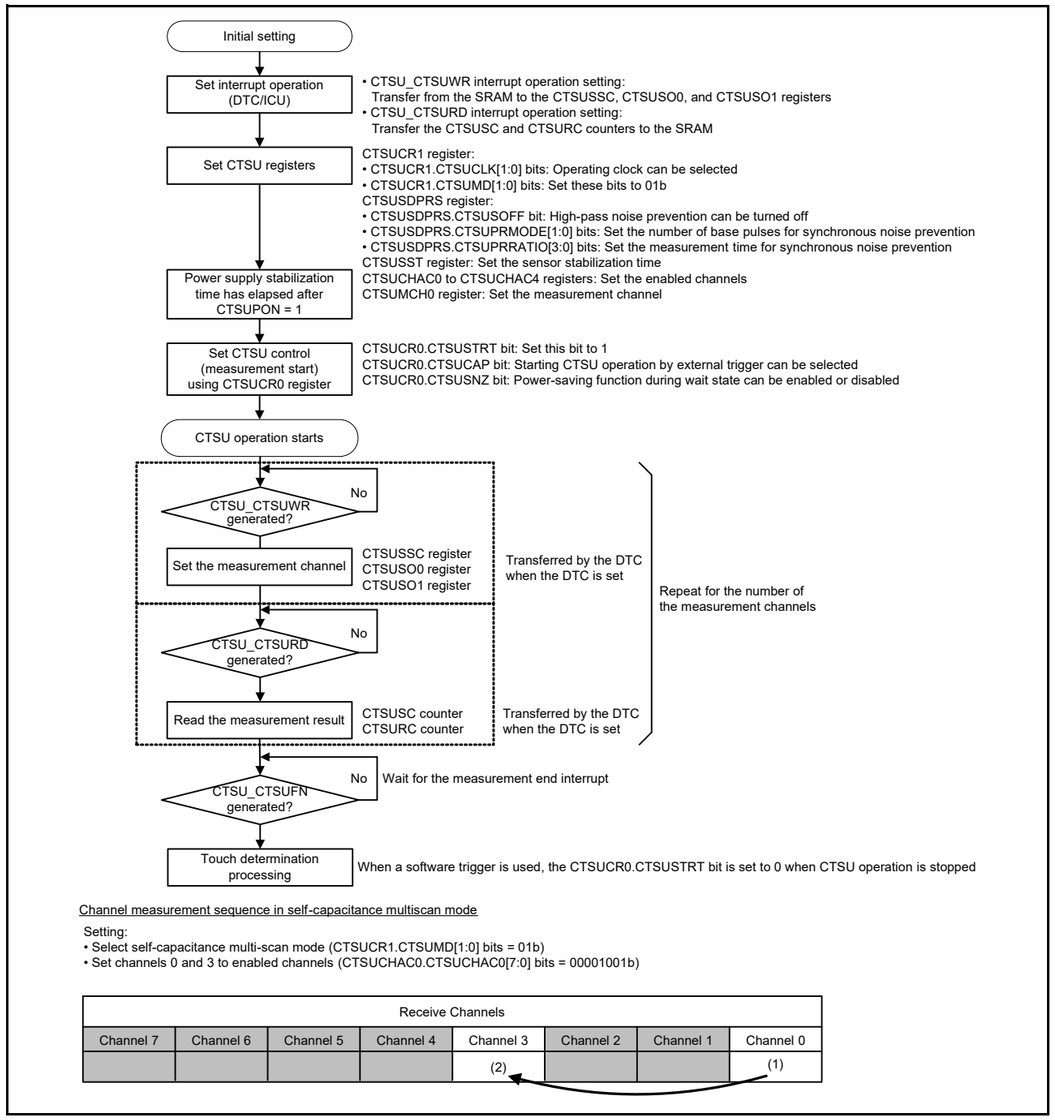


Figure 40.14 Software flow and example operation for self-capacitance multi-scan mode

40.3.2.4 自电容多扫描模式操作

在自电容多重扫描模式下，CTSUCHAC0至CTSUCHAC4寄存器中指定为测量目标的所有通道上的静电电容按升序顺序测量。图40.14显示了软件流程和操作示例，图40.15显示了时序。

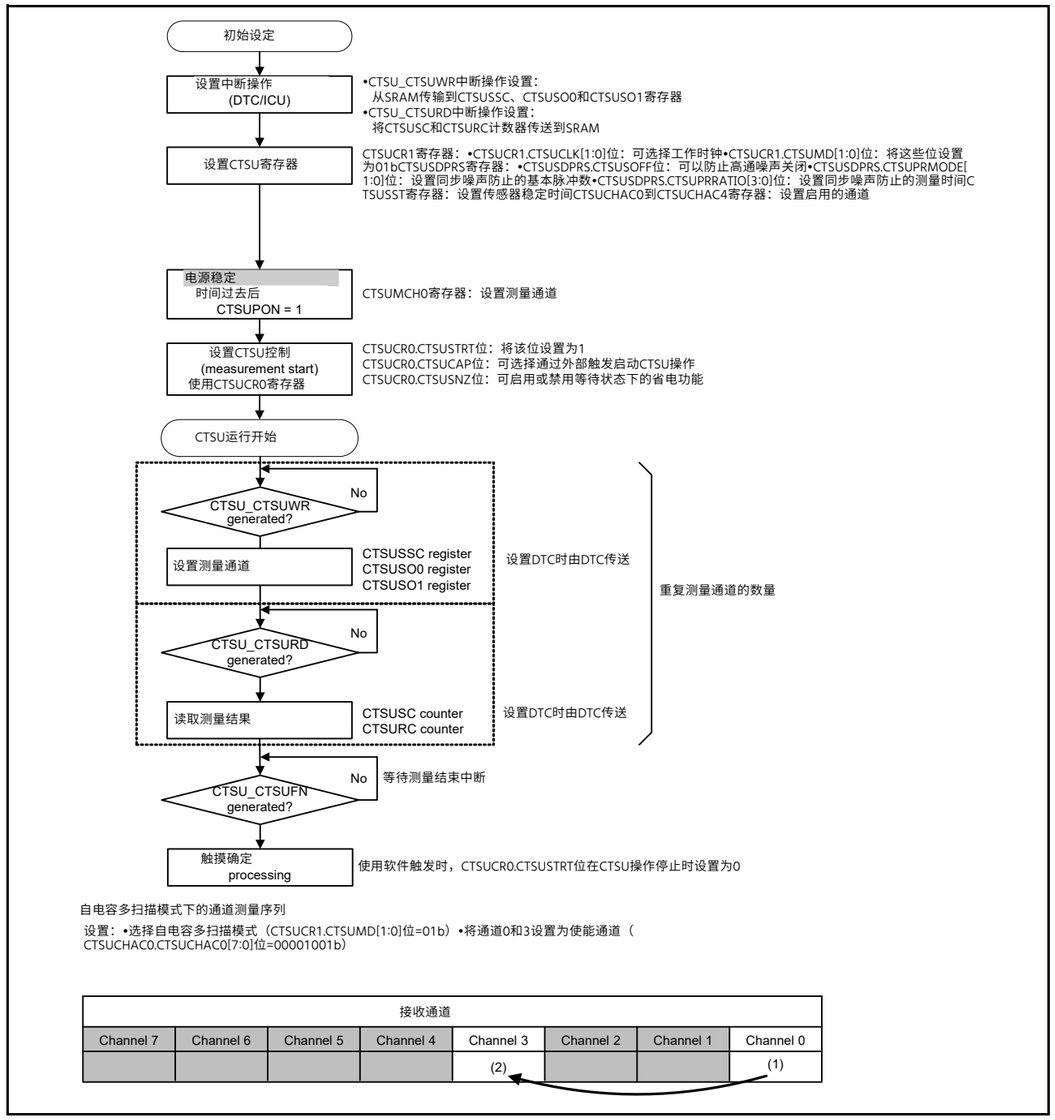


Figure 40.14 自电容多扫描模式的软件流程和示例操作

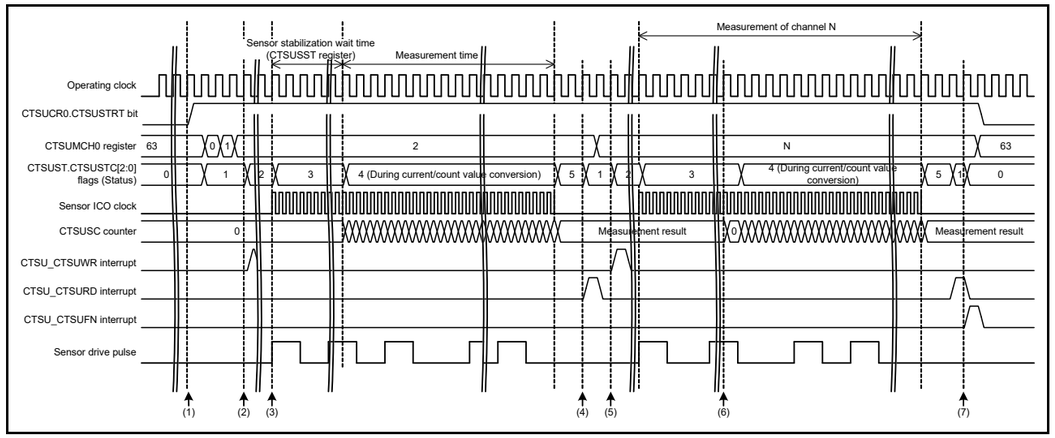


Figure 40.15 Timing of self-capacitance multi-scan mode when the measurement start condition is a software trigger

The following sequence describes the operation shown in Figure 40.15:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined according to the preset conditions, a request to set the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time elapse, and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. After the channel to be measured next is determined, a request to set the channel (CTSU_CTSUWR) is output.
6. After the stabilization wait time elapses and when the previous measurement is read, the result is cleared and measurement starts.
7. On completion of all measurement channels, a measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

Table 40.7 lists the touch pin states in self-capacitance multi-scan mode.

Table 40.7 Touch pin states in self-capacitance multi-scan mode

	Touch pin	
Status	**Measured channel**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

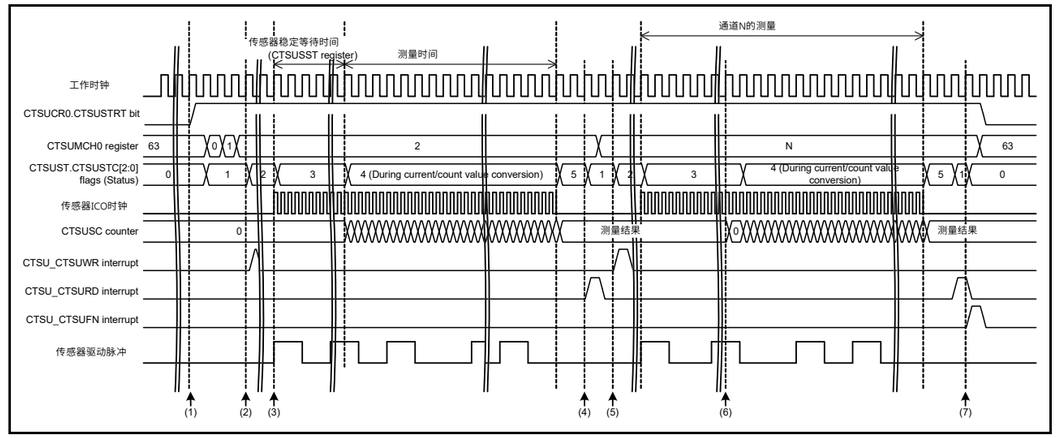


Figure 40.15 测量开始条件为软件触发时的自电容多次扫描模式时序

以下序列描述了图40.15所示的操作：

1. 进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。
2. 根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。
3. 写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。
4. 在传感器稳定等待时间和测量时间过去，测量停止后，输出测量结果读取请求（CTSU_CTSURD）。
5. 在确定下一个要测量的通道后，输出设置通道的请求（CTSU_CTSUWR）。
6. 稳定等待时间过去后，当读取前一次测量时，结果将被清除并开始测量。
7. 所有测量通道完成后，将输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

表40.7列出了自电容多扫描模式下的触摸引脚状态。

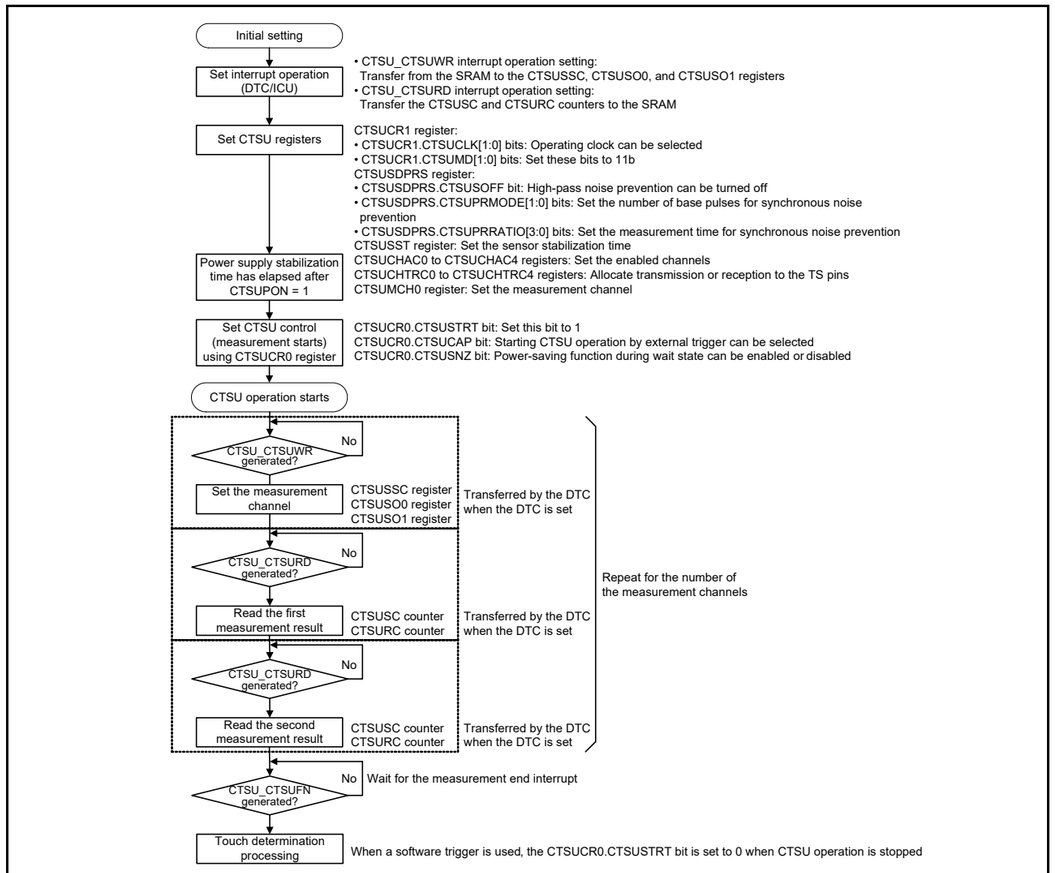
Table 40.7 自电容多扫描模式下的触摸引脚状态

	触摸针	
Status	**测量通道**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

40.3.2.5 Mutual capacitance full scan mode operation

In mutual capacitance full-scan mode, measurement is performed during the high-level period of the sensor drive pulse on the receive channel by applying the edge to the target transmit channel to be measured. A single measurement target is measured twice, on the rising and falling edges. The difference between the data of these two measurements determines whether or not the electrode was touched. This creates higher touch sensitivity.

Electrostatic capacitance is measured sequentially on channels set to transmission or reception in the CTSUCHTRC0 to CTSUCHTRC4 registers, and specified as measurement targets in the CTSUCHAC0 to CTSUCHAC4 registers. The capacitance is measured by combining these signals. Figure 40.16 shows the software flow and an operation example, and Figure 40.17 shows the timing.



Channel measurement sequence in mutual capacitance full scan mode
Setting:
• Select mutual-capacitance full-scan mode (CTSUCR1.CTSUMD[1:0] = 11b)
• Set channels 0, 3, 12, and 13 to enabled channels (CTSUCHAC0.CTSUCHAC0[7:0] bits = 00001001b, CTSUCHAC1.CTSUCHAC1[7:0] bits = 00110000b)
• Set channels 0 and 3 to receive channels and channels 12 and 13 to transmit channels (CTSUCHTRC0.CTSUCHTRC0[7:0] bits = 00000000b, CTSUCHTRC1.CTSUCHTRC1[7:0] bits = 00110000b)

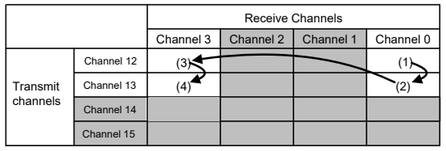
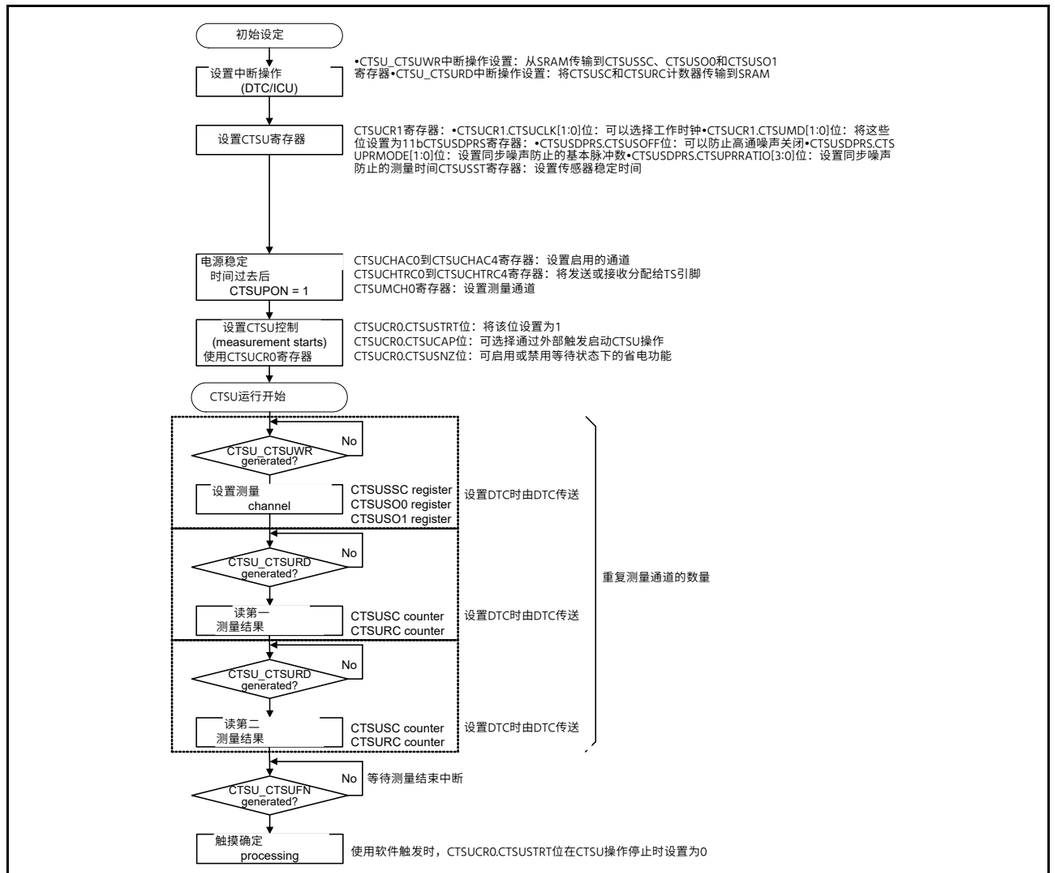


Figure 40.16 Software flow and operation example for mutual capacitance full-scan mode

40.3.2.5 互电容全扫描模式操作

在互电容全扫描模式下，在接收通道上的传感器驱动脉冲的高电平期间通过将边沿施加到要测量的目标发送通道来执行测量。在上升沿和下降沿对单个测量目标进行两次测量。这两次测量的数据之间的差异决定了电极是否被触摸。这会产生更高的触摸灵敏度。

在CTSUCHTRC0中设置为发送或接收的通道上依次测量静电电容
CTSUCHAC4寄存器，并在CTSUCHAC0至CTSUCHAC4寄存器中指定为测量目标。通过组合这些信号来测量电容。图40.16显示了软件流程和操作示例，图40.17显示了时序。



互电容全扫描模式下的通道测量序列
设置：•选择互电容全扫描模式（CTSUCR1.CTSUMD[1:0]=11b）•将通道0、3、12和13设置为启用通道（CTSUCHAC0.CTSUCHAC0[7:0]位=00001001b，CTSUCHAC1.CTSUCHAC1[7:0]位=00110000b)•将通道0和3设置为接收通道，将通道12和13设置为发送通道（CTSUCHTRC0.CTSUCHTRC0[7:0]位=00000000b，CTSUCHTRC1.CTSUCHTRC1[7:0]位=00110000b)

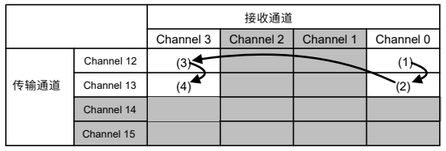


Figure 40.16 互电容全扫描模式的软件流程和操作示例

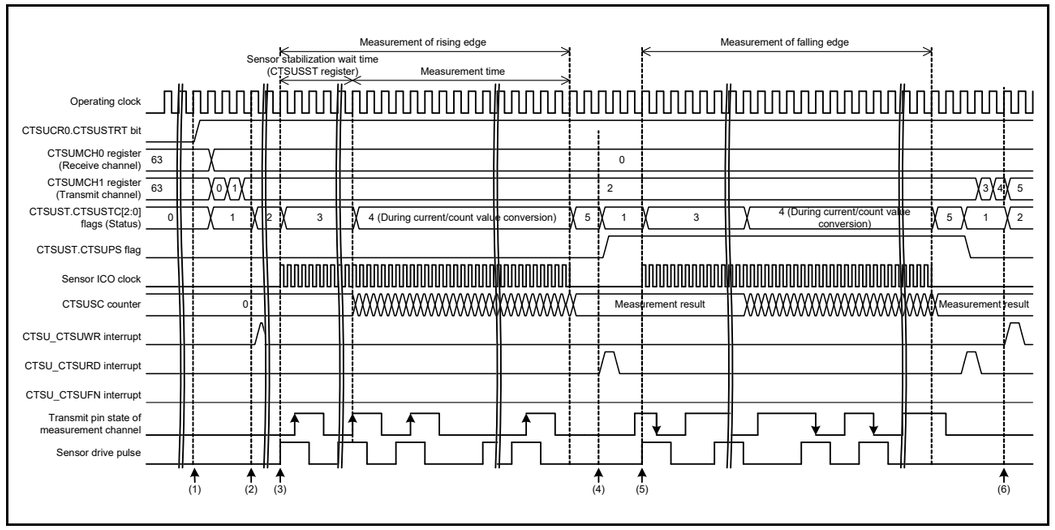


Figure 40.17 Timing of mutual capacitance full-scan mode when the measurement start condition is a software trigger

The following sequence describes the operation shown in Figure 40.17:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined according to the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate. At the same time, a pulse detected on the rising edge is output to the transmit pin on the measurement channel during the high-level period of the sensor drive pulse.
4. After the sensor stabilization wait time and the measurement time elapse and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. The same channel is measured by outputting a pulse detected on the falling edge during the high-level period of the sensor drive pulse.
6. After the same channel is measured twice, the channel to be measured next is determined and measured in the same way.
7. On completion of all measurement channels, a measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

The CTSU mutual capacitance status flag (CTSUST.CTSUPS bit) changes when Status 5 transitions to Status 1.

Table 40.8 lists the touch pin states in mutual capacitance full-scan mode.

Table 40.8 Touch pin states in mutual capacitance full-scan mode (1 of 2)

Status	Touch pin for receive channels		Touch pin for transmit channels		Remarks
	Measured channel	Non-measured channel	Measured channel	Non-measured channel	
0	Low	Low	Low	Low	-
1	Low	Low	Low/High	Low	-
2	Low	Low	Low	Low	-

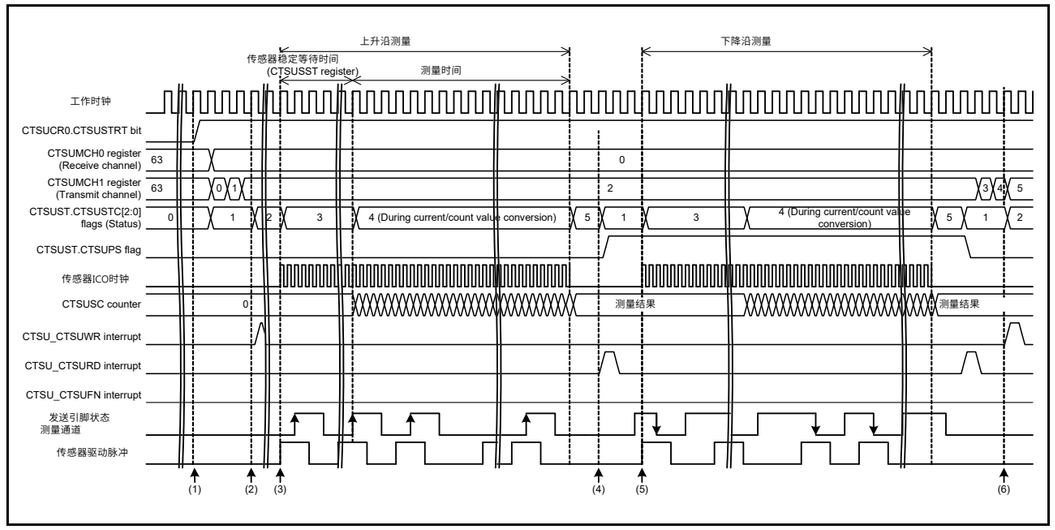


Figure 40.17 测量开始条件为软件触发时的互电容全扫描模式时序

以下序列描述了图40.17所示的操作：

1. 进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。
2. 根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。
3. 写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。同时，在传感器驱动脉冲的高电平期间，将在上升沿检测到的脉冲输出到测量通道的发送引脚。
4. 在传感器稳定等待时间和测量时间过去并停止测量后，输出测量结果读取请求(CTSU_CTSURD)。
5. 通过在传感器驱动脉冲的高电平期间输出在下降沿检测到的脉冲来测量同一通道。
6. 同一通道测量两次后，确定下一个要测量的通道，以同样的方式进行测量。
7. 所有测量通道完成后，将输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

当状态5转换为状态1时，CTSU互电容状态标志（CTSUST.CTSUPS位）发生变化。

表40.8列出了互电容全扫描模式下的触摸引脚状态。

Table 40.8 互电容全扫描模式下的触摸引脚状态（1of2）

Status	接收通道的触摸针		发送通道的触摸引脚		Remarks
	测量通道	Non-measured channel	测量通道	Non-measured channel	
0	Low	Low	Low	Low	-
1	Low	Low	Low/High	Low	-
2	Low	Low	Low	Low	-

Table 40.8 Touch pin states in mutual capacitance full-scan mode (2 of 2)

Status	Touch pin for receive channels		Touch pin for transmit channels		Remarks
	Measured channel	Non-measured channel	Measured channel	Non-measured channel	
3	Pulse	Low	Pulse	Low	The phase pulse is the same as that of the receive channel on the first measurement and opposite on the second measurement
4	Pulse	Low	Pulse	Low	-
5	Low	Low	Low	Low	-

40.3.3 Parameters Common to Multiple Modes

40.3.3.1 Sensor stabilization wait time and measurement time

Figure 40.18 shows the timing of the sensor stabilization wait and measurement.

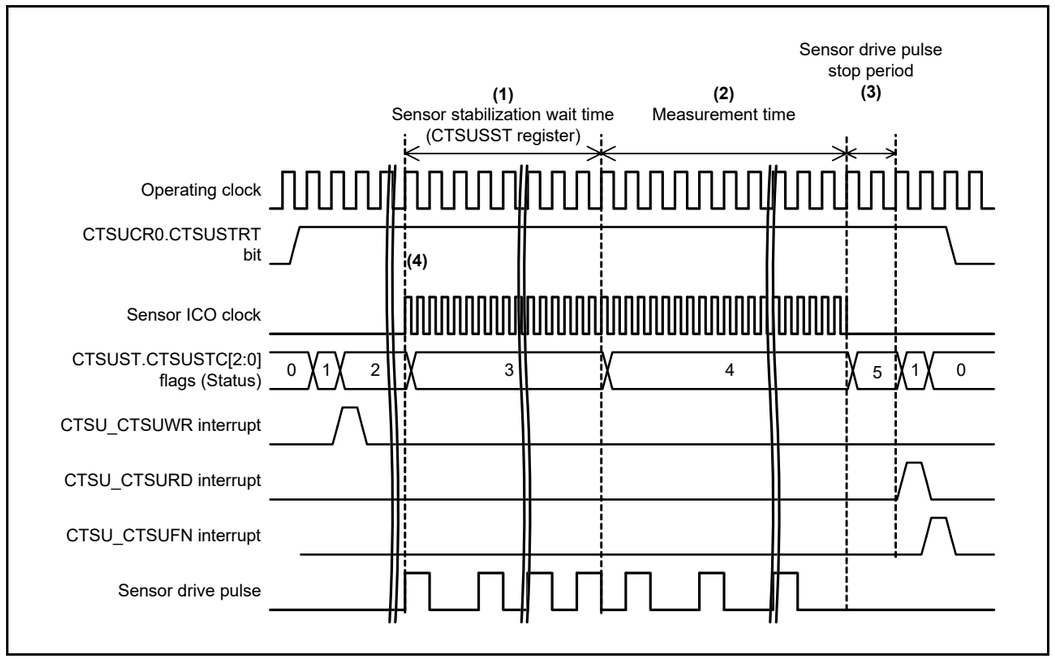


Figure 40.18 Sensor stabilization wait and measurement timing

1. In response to the CTSU_CTSUWR interrupt request, output of the sensor drive pulse is started by a write access to the CTSUSO1 register. The CTSU waits for the stabilization time set in the CTSUSST register.
2. When the sensor stabilization time elapses and the CTSUST.CTSUDTSR flag is set to 0, measurement starts on transition to Status 4. The measurement time is determined by the base clock cycle setting and the CTSUSDPRS.CTSUPRMODE[1:0], CTSUPRRATIO[3:0], and CTSUSO0.CTSUSNUM[5:0] bits. When the measurement time elapses, measurement of the channel stops.
3. After the measurement time elapses, the status transitions to Status 1 after 2 operating clock cycles, and a CTSU_CTSURD interrupt is generated. Read the data from the CTSUSC and CTSURC counters. At this time, the sensor drive pulse is output low. When measurement of all specified channels is completed, the CTSUCR0.CTSUSTRT bit is set to 0.
4. The sensor ICO clock oscillates while the CTSUST.CTSUSTC[2:0] flags = 011b (Status 3) or 100b (Status 4).

Table 40.8 互电容全扫描模式下的触摸引脚状态（2个中的2个）

Status	接收通道的触摸针		发送通道的触摸引脚		Remarks
	测量通道	Non-measured channel	测量通道	Non-measured channel	
3	Pulse	Low	Pulse	Low	相位脉冲在第一次测量时与接收通道相同，在第二次测量时相反
4	Pulse	Low	Pulse	Low	-
5	Low	Low	Low	Low	-

40.3.3 多种模式共有的参数

40.3.3.1 传感器稳定等待时间和测量时间

图40.18显示了传感器稳定等待和测量的时序。

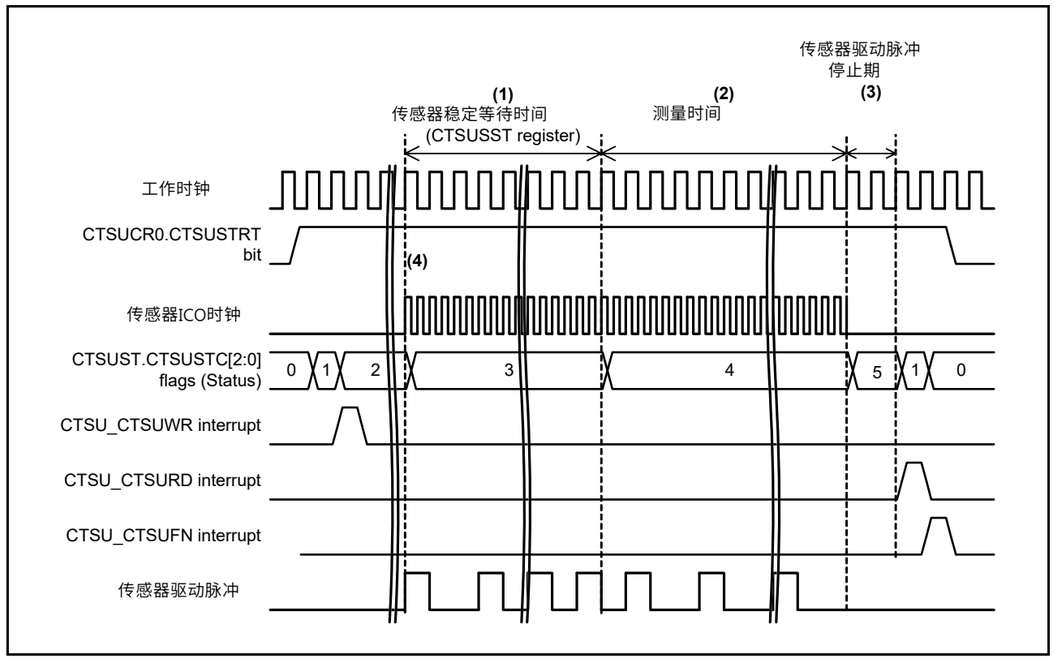


Figure 40.18 传感器稳定等待和测量定时

1. 响应CTSU_CTSUWR中断请求，通过对CTSUSO1寄存器的写访问开始输出传感器驱动脉冲。CTSU等待CTSUSST寄存器中设置的稳定时间。
2. 当传感器稳定时间过去且CTSUST.CTSUDTSR标志设置为0时，测量开始转换到状态4。测量时间由基本时钟周期设置和CTSUSDPRS.CTSUPRMODE[1:0]、CTSUPRATIO[3:0]和CTSUSO0.CTSUSNUM[5:0]位。当测量时间过去时，通道的测量将停止。
3. 测量时间过去后，状态在2个工作时钟周期后转换为状态1，并且产生CTSU_CTSURD中断。从CTSUSC和CTSURC计数器读取数据。此时，传感器驱动脉冲输出低电平。完成所有指定通道的测量后，CTSUCR0.CTSUSTRT位设置为0。
4. 传感器ICO时钟在CTSUST.CTSUSTC[2:0]标志=011b（状态3）或100b（状态4）时振荡。

40.3.3.2 Interrupts

The CTSU supports the following interrupts:

- Write request interrupt for setting registers for each channel (CTSU_CTSUWR)
- Measurement data transfer request interrupt (CTSU_CTSURD)
- Measurement end interrupt (CTSU_CTSUFN).

(1) Write request interrupt for setting registers for each channel (CTSU_CTSUWR)

Store the settings for each measurement channel in the SRAM, and set up the DTC or ICU transfer associated with the CTSU_CTSUWR interrupt in advance. The CTSU_CTSUWR interrupt is output when Status 1 transitions to Status 2. Write the channel settings from the SRAM to the associated CTSUSSC, CTSUSO0, and CTSUSO1 registers (Figure 40.19). Because write access to the CTSUSO1 register controls the transition to the next status, be sure to set this register last.

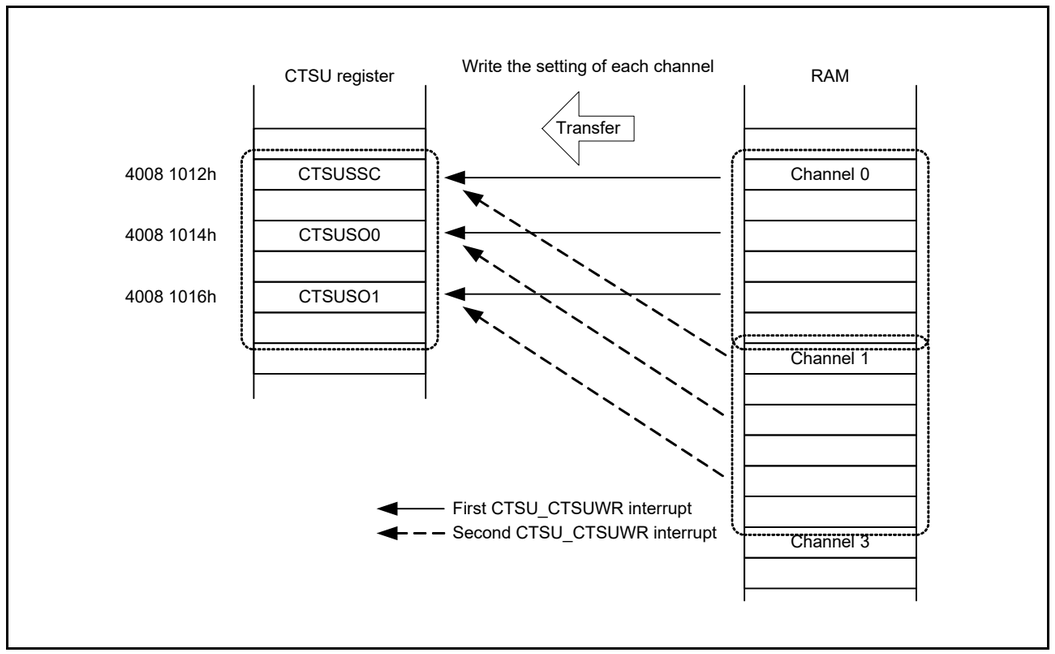


Figure 40.19 Example DTC transfer operation using the CTSU_CTSUWR interrupt

The registers to be set (CTSUSSC, CTSUSO0, and CTSUSO1) are allocated at sequential addresses. On CTSU_CTSUWR interrupt generation, set up the operation as follows:

- Transfer destination address: CTSUSSC register address
- Handling at the transfer destination address: Transfer 2-byte data three times for a single interrupt. The address of the start byte is fixed
- Transfer source address: CTSUSSC register data storage address for the lowest channel in the settings stored in the SRAM
- Handling at the transfer source address: Transfer 2-byte data three times for a single interrupt. The address of the first byte is continued from the previous interrupt handling.
- Number of transfers per interrupt: Specify the number of measurements.

40.3.3.2 Interrupts

CTSU支持以下中断：

- 为每个通道设置寄存器的写请求中断(CTSU_CTSUWR)
- 测量数据传输请求中断(CTSU_CTSURD)
- 测量结束中断(CTSU_CTSUFN)。

(1) 为每个通道设置寄存器的写请求中断(CTSU_CTSUWR)

将每个测量通道的设置存储在SRAM中，并提前设置与CTSU_CTSUWR中断相关的DTC或ICU传输。当状态1转换到状态2时输出CTSU_CTSUWR中断。

将SRAM中的通道设置写入相关的CTSUSSC、CTSUSO0和CTSUSO1寄存器（图40.19）。因为对CTSUSO1寄存器的写访问控制到下一个状态的转换，所以一定要最后设置这个寄存器。

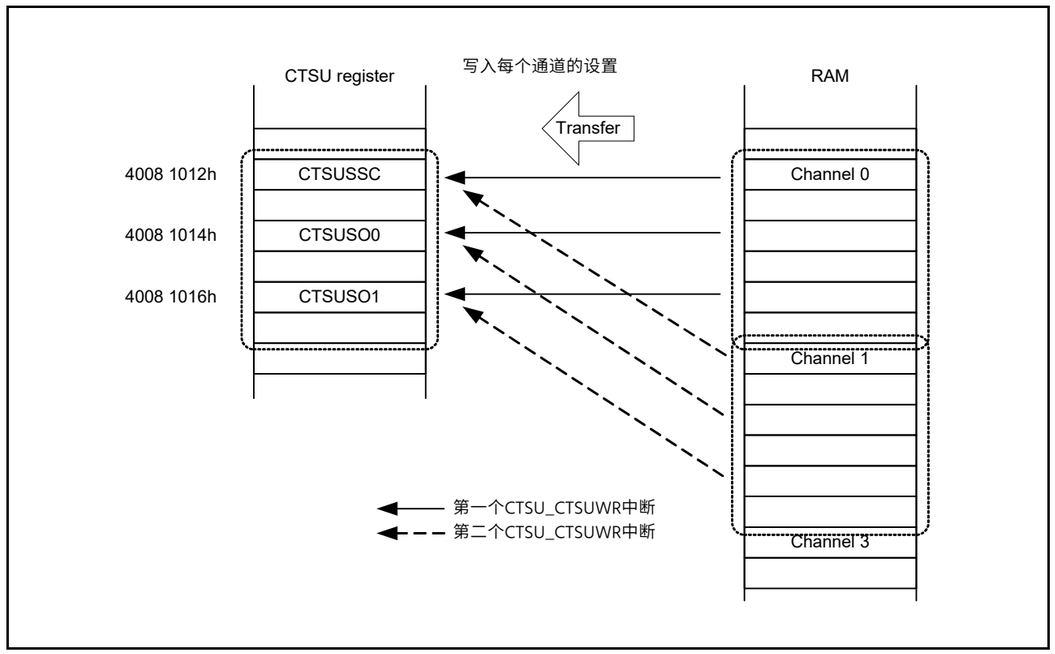


Figure 40.19 使用CTSU_CTSUWR中断的示例DTC传输操作

要设置的寄存器（CTSUSSC、CTSUSO0和CTSUSO1）分配在顺序地址。上CTSU_CTSUWR中断产生，设置操作如下：

- 传输目标地址：CTSUSSC寄存器地址
- 传送目标地址处的处理：一次中断传送3次2字节数据。起始字节的地址是固定的
- 传输源地址：CTSUSSC寄存器数据存储地址为设置中存储的最低通道SRAM
- 在传输源地址处处理：一次中断传输3次2字节数据。第一个字节的地址从先前的中断处理继续。
- 每次中断的传输次数：指定测量次数。

(2) Measurement data transfer request interrupt (CTSU_CTSURD)

Set up the DTC or ICU transfer associated with the CTSU_CTSURD interrupt in advance. The CTSU_CTSURD interrupt is output when Status 5 transitions to Status 1. Read the measurement result from the CTSUSC and CTSURC counters in Figure 40.20.

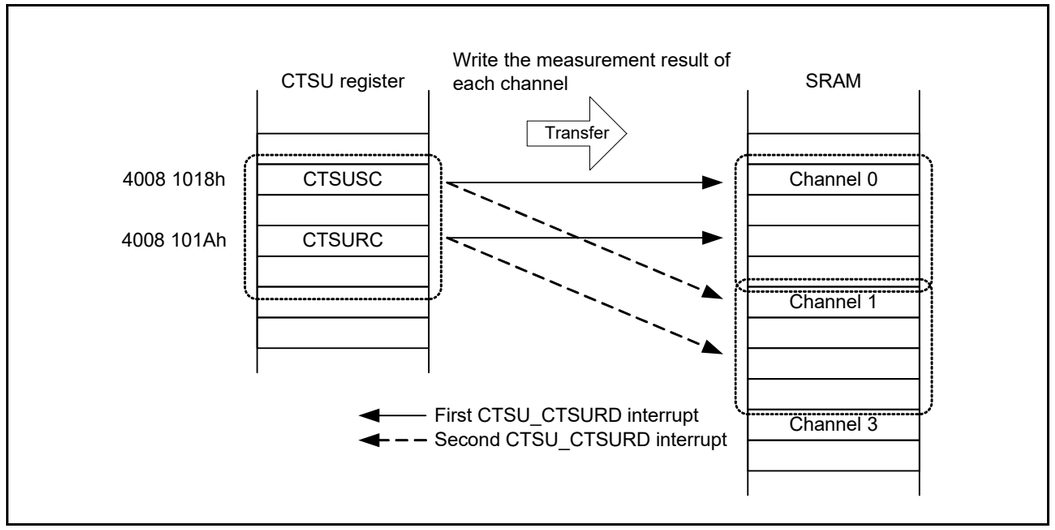


Figure 40.20 Example of DTC transfer operation using the CTSU_CTSURD interrupt

The measurement result registers (CTSUSC and CTSURC counters) used as transfer sources are allocated at sequential addresses. On CTSU_CTSURD interrupt generation, set up the operation as follows:

- Transfer source address: CTSUSC counter address
- Handling at the transfer source address: Transfer 2-byte data twice for a single interrupt. The start address is fixed.
- Transfer destination address: CTSUSC counter data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer destination address: Transfer 2-byte data twice for a single interrupt. The start address is continued from the previous interrupt handling.
- Number of transfers by an interrupt: Specify the number of measurements.

(3) Measurement end interrupt (CTSU_CTSUFN)

After all channels are measured, an interrupt is generated when Status 1 transitions to Status 0. Use software to check the overflow flags (CTSUST.CTSUSOVF and CTSUROVF flags) and read the measurement results to determine whether the electrode was touched. Interrupt requests are accepted or disabled in the interrupt control block.

40.4 Usage Notes

40.4.1 Measurement Result Data (CTSUSC and CTSURC Counters)

Read access during measurement is prohibited. If the measurement result data is accessed, an incorrect value might be read because of an asynchronous operation.

40.4.2 Constraints on Software Trigger

When 10b (PCLKB/4) is selected in the CTSUCR1.CTSUCLK[1:0] bits, to restart measurement by writing 1 to the CTSUR0.CTSUSTRT bit after measurement completes, wait for at least 3 cycles to elapse after an interrupt is generated, then write to the CTSUCR0.CTSUSTRT bit.

(2) 测量数据传输请求中断(CTSU_CTSURD)

提前设置与CTSU_CTSURD中断相关的DTC或ICU传输。当状态5转换为状态1时输出CTSU_CTSURD中断。从图40.20中的CTSUSC和CTSURC计数器读取测量结果。

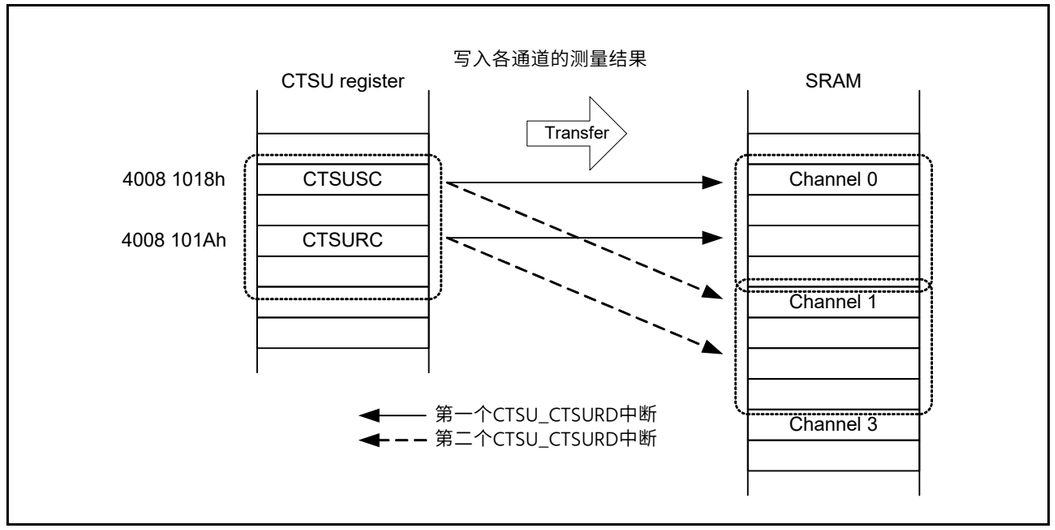


Figure 40.20 使用CTSU_CTSURD中断的DTC传输操作示例

用作传输源的测量结果寄存器（CTSUSC和CTSURC计数器）按顺序分配。在CTSU_CTSURD中断生成时，按如下方式设置操作：

- 传输源地址：CTSUSC计数器地址
- 传输源地址处的处理：一次中断传输2字节数据两次。起始地址是固定的。
- 传送目标地址：SRAM中存储的设置中最小编号通道的CTSUSC计数器数据存储地址
- 传送目标地址处的处理：一次中断传送2字节数据两次。起始地址从先前的中断处理继续。
- 中断传输次数：指定测量次数。

(3) 测量结束中断(CTSU_CTSUFN)

测量完所有通道后，当状态1转换为状态0时会产生中断。使用软件检查溢出标志（CTSUST.CTSUSOVF和CTSUROVF标志）并读取测量结果以确定电极是否被触摸。在中断控制块中接受或禁用中断请求。

40.4 使用说明

40.4.1 测量结果数据（CTSUSC和CTSURC计数器）

禁止在测量期间进行读取访问。如果访问测量结果数据，可能会因为异步操作而读取到不正确的值。

40.4.2 软件触发的约束

当在CTSUCR1.CTSUCLK[1:0]位中选择10b(PCLKB4)时，通过将1写入
测量完成后CTSUR0.CTSUSTRT位，在产生中断后至少等待3个周期，然后写入CTSUCR0.CTSUSTRT位。

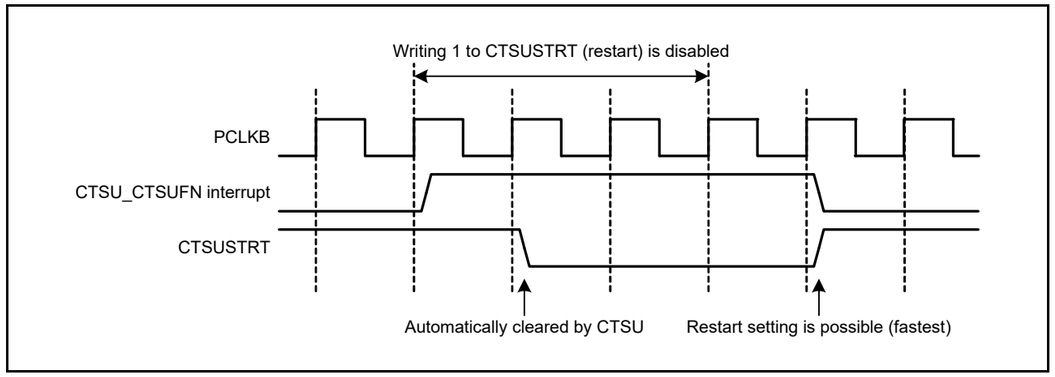


Figure 40.21 Notes on restarting measurement

40.4.3 Constraints on External Trigger

- If an external trigger is input during the measurement time, measurement does not start. The next external event is enabled after 1 cycle of the operating clock when a CTSU_CTSUFN interrupt is generated.
- To stop external trigger mode, write 0 to the CTSUCR0.CTSUSTRT bit and 0 to the CTSUCR0.CTSUINIT bit at the same time (forced stop).

40.4.4 Constraints on Forced Stops

To force the current operation to stop, write 0 to the CTSUCR0.CTSUSTRT bit and 1 to the CTSUCR0.CTSUINIT bit at the same time. After this setting, the operation is stopped and the internal control registers are initialized.

When the CTSUCR0.CTSUINIT bit is used for initialization, the following registers are initialized in addition to the initialization of the internal measurement state:

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter.

If operation is forced to stop, an interrupt request might be generated depending on the internal state. After a forced stop, also perform the processing for stopping and disabling the DTC or ICU. If a DTC transfer is stopped in an installed system for some reason, also perform the processing to force the stop and to initialize the CTSU.

40.4.5 TSCAP Pin

The TSCAP pin requires an external decoupling capacitor to stabilize CTSU internal voltage. The traces between the TSCAP pin and the capacitor, and the capacitor and ground should be as short and wide as physically possible. The capacitor connected to the TSCAP pin should be fully discharged using the I/O port control to output a low level, before turning on the switch (CTSUCR1.CTSUCSW bit = 1) to establish a connection.

40.4.6 Constraints on Measurement Operation (CTSUCR0.CTSUSTRT Bit = 1)

During measurement (CTSUCR0.CTSUSTRT bit = 1), do not use settings for stopping the peripheral clock or changing the port settings related to the touch pins (TSn and TSCAP pins) in the higher layers of the system.

If control settings non-compliant with these constraints are made, after operation is forced to stop (CTSUCR0.CTSUSTRT bit = 0 and CTSUCR0.CTSUINIT bit = 1), write 0 to the CTSUCR1.CTSUPON bit and 0 to the CTSUCR1.CTSUCSW bit at the same time, and set the CTSUCR0.CTSUSNZ bit to 0. Then, restart from the initial settings flow shown in Figure 40.9.

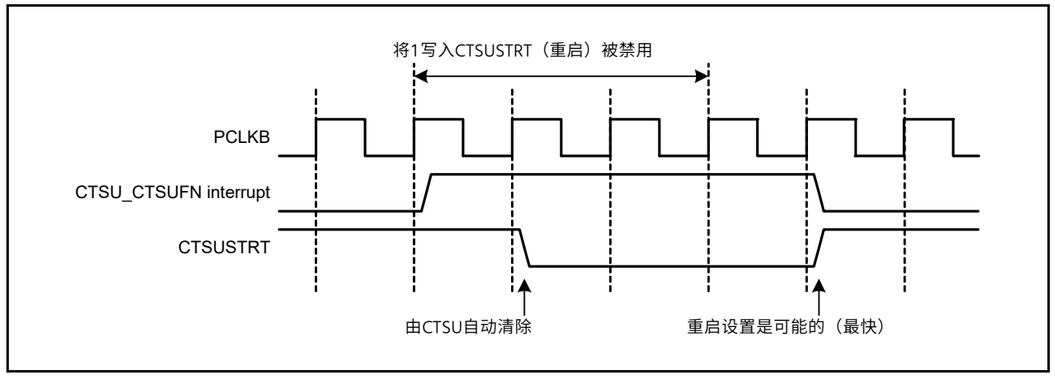


Figure 40.21 重新开始测量的注意事项

40.4.3 外部触发约束

- 如果在测量期间输入外部触发，测量不会开始。当产生CTSU_CTSUFN中断时，下一个外部事件在工作时钟的1个周期后启用。
- 要停止外部触发模式，同时向CTSUCR0.CTSUSTRT位写入0和向CTSUCR0.CTSUINIT位写入0（强制停止）。

40.4.4 强制停止的约束

要强制停止当前操作，请同时向CTSUCR0.CTSUSTRT位写入0，向CTSUCR0.CTSUINIT位写入1。设置完成后，操作停止，内部控制寄存器初始化。

当使用CTSUCR0.CTSUINIT位进行初始化时，除了初始化内部测量状态之外，还会初始化以下寄存器：

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter.

如果操作被强制停止，根据内部状态可能会产生中断请求。强制停止后，还要执行停止和禁用DTC或ICU的处理。如果由于某种原因在已安装的系统中停止了DTC传输，则还要执行强制停止和初始化CTSU的处理。

40.4.5 TSCAP Pin

TSCAP引脚需要一个外部去耦电容来稳定CTSU内部电压。之间的痕迹
TSCAP引脚和电容器，以及电容器和地线应尽可能短且宽。在打开开关（CTSUCR1.CTSUCSW位=1）建立连接之前，应使用IO端口控制将连接到TSCAP引脚的电容器完全放电以输出低电平。

40.4.6 测量操作的限制（CTSUCR0.CTSUSTRT位=1）

在测量期间（CTSUCR0.CTSUSTRT位=1），请勿使用设置来停止外设时钟或更改系统较高层中与触摸引脚（TSn和TSCAP引脚）相关的端口设置。

如果进行了不符合这些约束的控制设置，则在强制停止操作后（CTSUCR0.CTSUSTRT位=0且CTSUCR0.CTSUINIT位=1），将0写入CTSUCR1.CTSUPON位并将0写入CTSUCR1.CTSUCSW位同时，将CTSUCR0.CTSUSNZ位设置为0。然后，从图40.9所示的初始设置流程重新启动。

41. Data Operation Circuit (DOC)

41.1 Overview

The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. An interrupt can be generated when a selected condition applies.

Table 41.1 lists the DOC specifications and Figure 41.1 shows a block diagram.

Table 41.1 DOC specifications

Parameter	Description
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	The module-stop state can be set to reduce power consumption
Interrupts and event link function (DOC_DOPCI)	An interrupt is generated on the following conditions: • The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h.

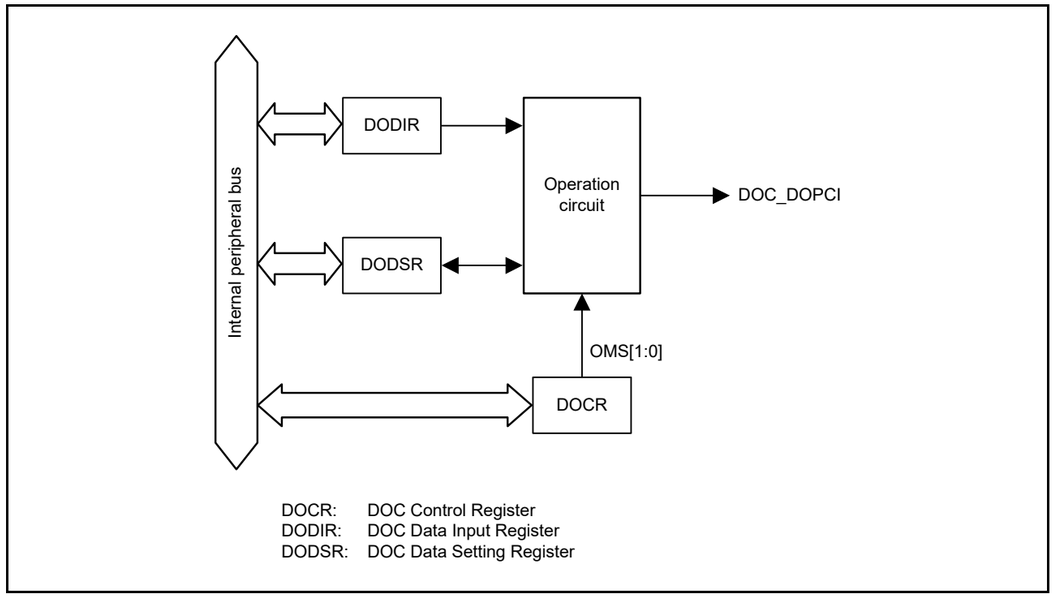


Figure 41.1 DOC block diagram

41. 数据运算电路(DOC)

41.1 Overview

数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，可以生成中断。

表41.1列出了DOC规范，图41.1显示了框图。

Table 41.1 文档规范

Parameter	Description
数据运算功能	16位数据比较、加法和减法
Module-stop function	可设置模块停止状态以降低功耗
中断和事件链接功能（DOC_DOPCI）	在以下情况下会产生中断： 比较值匹配或不匹配 数据加法的结果大于FFFFh 数据减法的结果小于0000h。

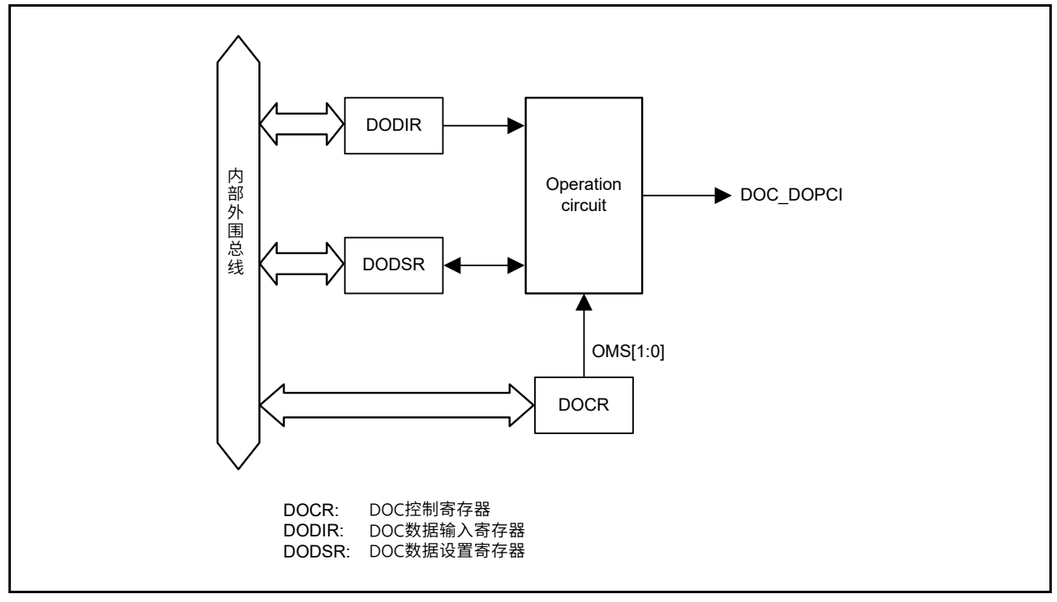


Figure 41.1 文档框图

41.2 Register Descriptions

41.2.1 DOC Control Register (DOCR)

Address(es): DOC.DOCR 4005 4100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited.	R/W
b2	DCSEL*1	Detection Condition Select	0: Set DOPCF when data mismatch is detected 1: Set DOPCF when data match is detected.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	DOPCF	Data Operation Circuit Flag	Indicates the result of an operation	R
b6	DOPCFCL	DOPCF Clear	0: Save DOPCF flag state 1: Clear DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (Data Operation Circuit Flag)

The DOPCF flag indicates the result of an operation.

[Setting conditions]

- The condition selected in the DCSEL bit is met
- A data addition result is greater than FFFFh
- A data subtraction result is less than 0000h.

[Clearing condition]

- Writing 1 to the DOPCFCL bit.

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

41.2 注册说明

41.2.1 DOC控制寄存器(DOCR)

Address(es): DOC.DOCR 4005 4100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	OMS[1:0]	操作模式选择	b1b000：数据比较模式01： 数据加法模式10：数据减法 模式11：禁止设置。	R/W
b2	DCSEL*1	检测条件选择	0：检测到数据不匹配时置位DOPCF1：检测到 数据匹配时置位DOPCF。	R/W
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	DOPCF	数据运算电路标志	表示操作的结果	R
b6	DOPCFCL	DOPCF Clear	0：保存DOPCF标志状态1 ：清除DOPCF标志。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 仅在选择数据比较模式时有效。

OMS[1:0]位（操作模式选择）

OMS[1:0]位选择DOC的工作模式。

DCSEL位（检测条件选择）

DCSEL位选择数据比较模式下的检测条件。该位仅在选择数据比较模式时有效。

DOPCF标志（数据操作电路标志）

DOPCF标志指示操作的结果。

[Setting conditions]

- 满足在DCSEL位中选择的条件
- 数据相加结果大于FFFFh
- 数据减法结果小于0000h。

[Clearing condition]

- 将1写入DOPCFCL位。

DOPCFCL位（DOPCF清除）

将DOPCFCL位设置为1会清除DOPCF标志。该位读为0。

41.2.2 DOC Data Input Register (DODIR)

Address(es): DOC.DODIR 4005 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR is a 16-bit read/write register that stores 16-bit data used in all operations.

41.2.3 DOC Data Setting Register (DODSR)

Address(es): DOC.DODSR 4005 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR is a 16-bit read/write register that stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.

41.3 Operation

41.3.1 Data Comparison Mode

Figure 41.2 shows an example DOC operation in data comparison mode. The following sequence is an example of operation when DCSEL is set to 0, that is, when data mismatch is detected as a result of a data comparison:

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set 16-bit reference data in the DODSR register.
3. Write 16-bit data for comparison to the DODIR register.
4. Continue writing 16-bit data until all data to be compared is written to DODIR.
5. If a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1.

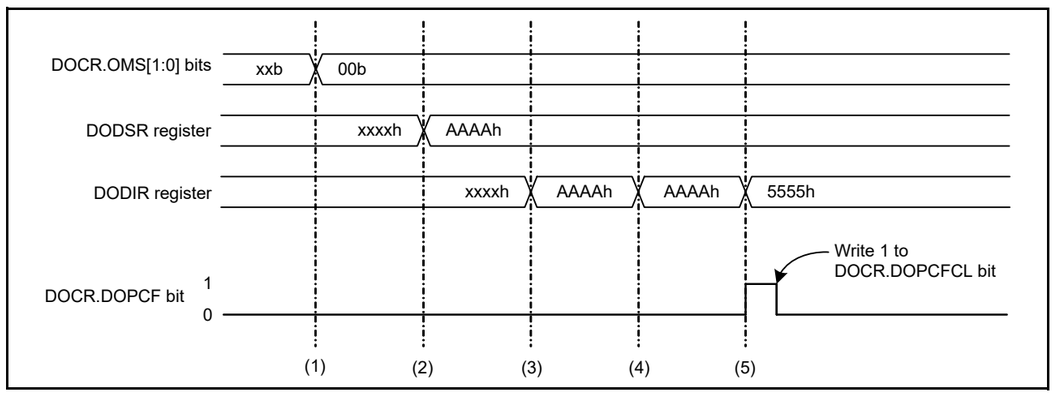


Figure 41.2 Example operation in data comparison mode

41.2.2 DOC数据输入寄存器(DODIR)

Address(es): DOC.DODIR 4005 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR是一个16位读写寄存器，用于存储所有操作中使用的16位数据。

41.2.3 DOC数据设置寄存器(DODSR)

Address(es): DOC.DODSR 4005 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR是一个16位读写寄存器，用于存储16位数据，在数据比较模式下用作参考。该寄存器还存储数据加法和减法模式下的运算结果。

41.3 Operation

41.3.1 数据比较模式

图41.2显示了数据比较模式下的示例DOC操作。以下序列是DCSEL设置为0时的操作示例，即当数据比较结果检测到数据不匹配时：

1. 将00b写入DOCR.OMS[1:0]位以选择数据比较模式。
2. 在DODSR寄存器中设置16位参考数据。
3. 将16位数据写入DODIR寄存器进行比较。
4. 继续写入16位数据，直到所有要比较的数据都写入DODIR。
5. 如果写入DODIR的值与DODSR中的值不匹配，则DOCR.DOPCF标志设置为1。

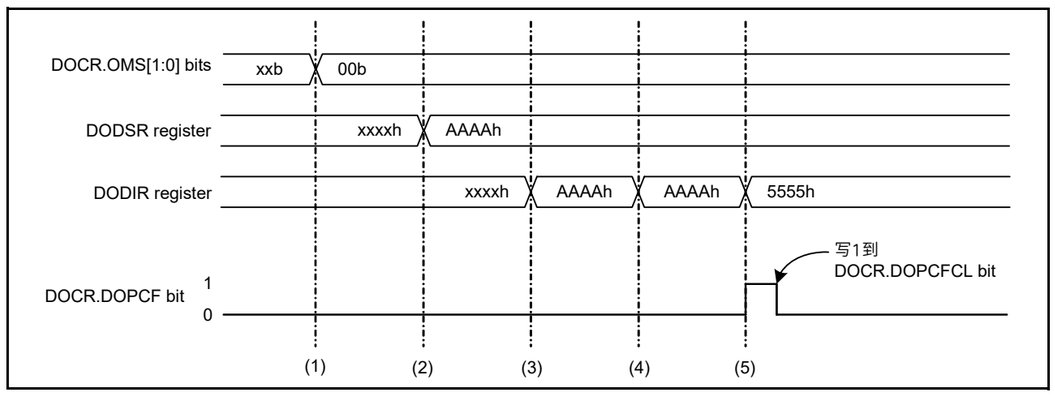


Figure 41.2 数据比较模式下的示例操作

41.3.2 Data Addition Mode

Figure 41.3 shows an example for DOC operation in data addition mode. The steps are as follows:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set the 16-bit data in the DODSR register as the initial value.
3. Write the 16-bit data to be added to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing 16-bit data until all data to be added is written to DODIR.
5. If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag is set to 1.

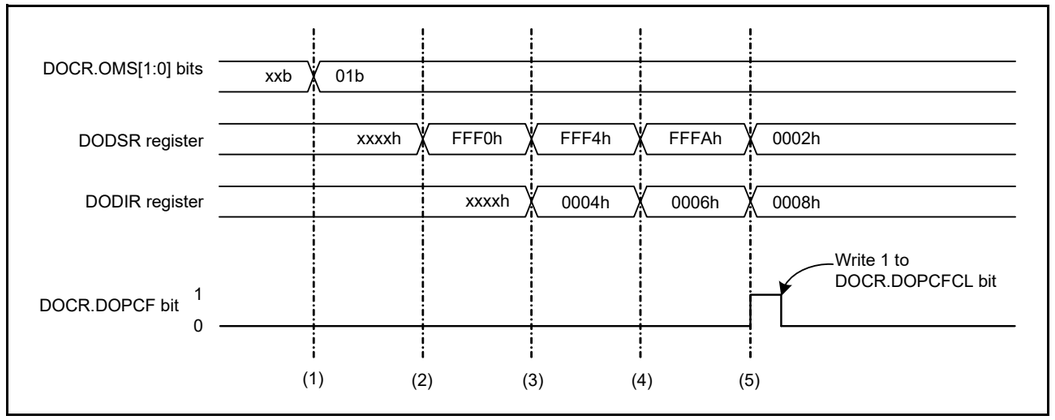


Figure 41.3 Example operation in data addition mode

41.3.3 Data Subtraction Mode

Figure 41.4 shows an example for DOC operation in data subtraction mode. The steps are as follows:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be subtracted to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing 16-bit data to the DODIR register until all data to be subtracted is written.
5. If the result of an operation is less than 0000h, the DOCR.DOPCF flag is set to 1.

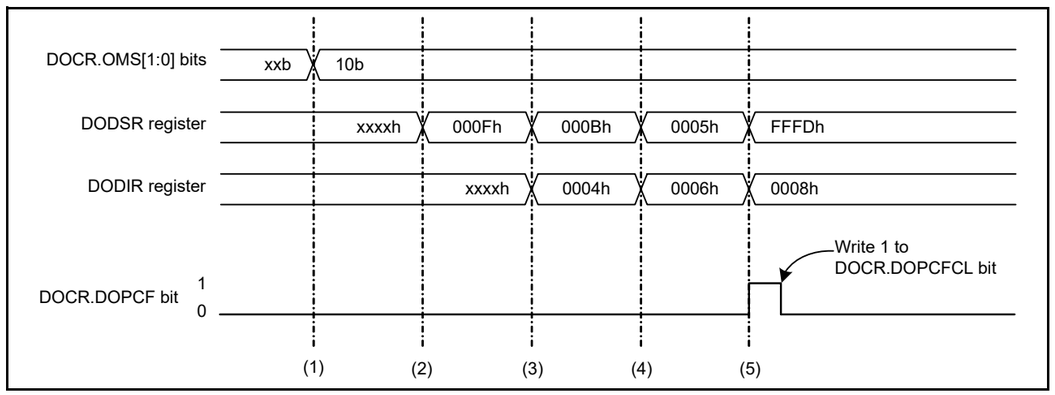


Figure 41.4 Example operation in data subtraction mode

41.3.2 数据加法模式

图41.3显示了数据添加模式下的DOC操作示例。步骤如下：

1. 将01b写入DOCR.OMS[1:0]位以选择数据添加模式。
2. 将DODSR寄存器中的16位数据设置为初始值。
3. 将要添加的16位数据写入DODIR寄存器。操作结果存储在DODSR中。
4. 继续写入16位数据，直到所有要添加的数据都写入DODIR。
5. 如果运算结果大于FFFFh，则DOCR.DOPCF标志设置为1。

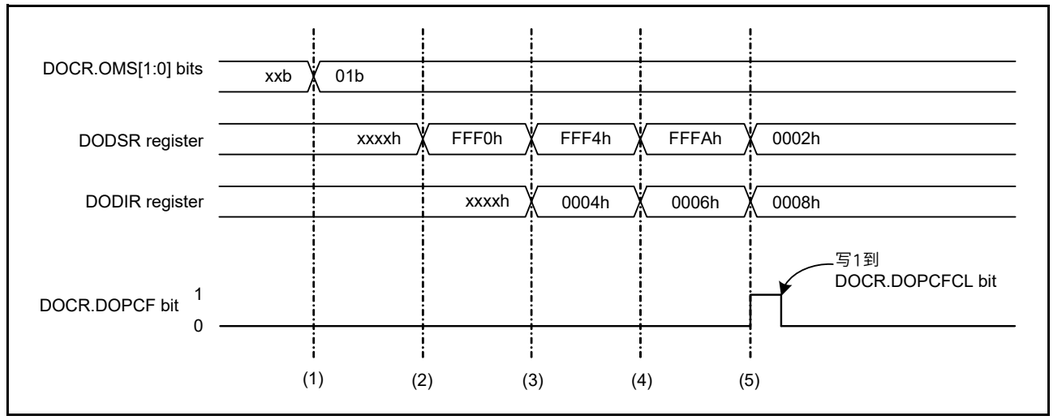


Figure 41.3 数据添加模式下的示例操作

41.3.3 数据减法模式

图41.4显示了数据减法模式下的DOC操作示例。步骤如下：

1. 将10b写入DOCR.OMS[1:0]位以选择数据减法模式。
2. 在DODSR寄存器中设置16位数据作为初始值。
3. 将要减去的16位数据写入DODIR寄存器。操作结果存储在DODSR中。
4. 继续向DODIR寄存器写入16位数据，直到写入所有要减去的数据。
5. 如果运算结果小于0000h，则DOCR.DOPCF标志设置为1。

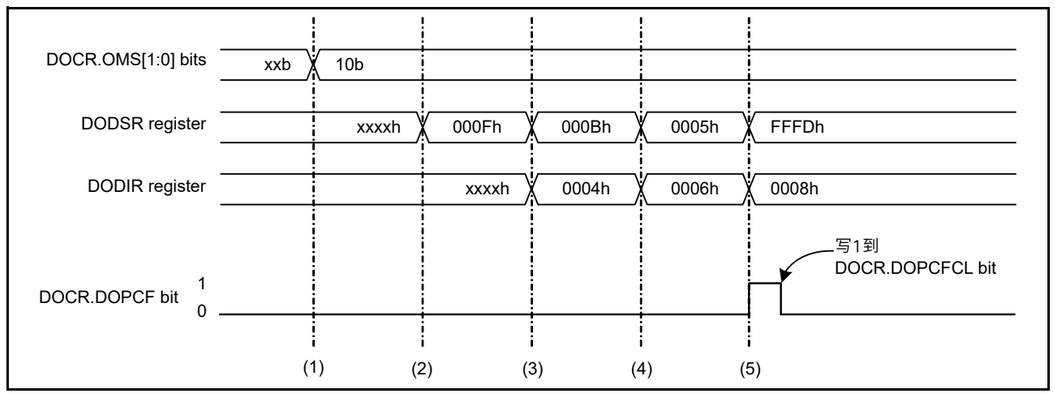


Figure 41.4 数据减法模式下的示例操作

41.4 Interrupt Request and Output to the Event Link Controller (ELC)

The DOC outputs an event signal to the ELC under the following conditions:

- The compared values either match or mismatch
- The data addition result is greater than FFFFh
- The data subtraction result is less than 0000h.

This signal can be used to initiate operations by other modules selected in advance and can also be used as an interrupt request. When an event signal is generated, the Data Operation Circuit Flag (DOCR.DOPCF) is set to 1.

41.5 Usage Notes

41.5.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable the DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

41.4 中断请求和输出到事件链接控制器(ELC)

DOC在以下条件下向ELC输出事件信号：

- 比较的值匹配或不匹配
- 数据相加结果大于FFFFh
- 数据减法结果小于0000h。

该信号可用于启动其他预先选择的模块的操作，也可用作中断请求。产生事件信号时，数据操作电路标志(DOCR.DOPCF)设置为1。

41.5 使用说明

41.5.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用DOC操作。DOC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

42. SRAM

42.1 Overview

The MCU provides an on-chip high-speed SRAM module with either parity-bit checking or Error Correction Code (ECC). The first 16-KB area of SRAM0 is the ECC. Parity check is performed on the other areas.

Table 42.1 lists the SRAM specifications.

Table 42.1 SRAM specifications

Parameter	Without ECC	With ECC
SRAM capacity	SRAM0: 80 KB	SRAM0 (ECC area): 16 KB
SRAM address	SRAM0: 2000 4000h to 2001 7FFFh	SRAM0 (ECC area): 2000 0000h to 2000 3FFFh
Access*1	0 wait	
Module-stop function	Available	
Parity	Even-parity with 8-bit data and 1-bit parity	No parity
Error checking	Even-parity error check	1-bit error correction and up to 2-bit error detection

Note 1. For details, see section 42.3.7, Access Cycle.

42.2 Register Descriptions

42.2.1 SRAM Parity Error Operation After Detection Register (PARIOAD)

Address(es): SRAM.PARIOAD 4000 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation After Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writes. Enable the SRAMPRCR bit in the SRAMPRCR register before writing to this register. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit specifies either a reset or non-maskable interrupt when a parity error is detected. The OAD bit is used for SRAM0 (without ECC).

42. SRAM

42.1 Overview

MCU提供片上高速SRAM模块，具有奇偶校验位检查或纠错码(ECC)。SRAM0的第一个16KB区域是ECC。对其他区域执行奇偶校验。

表42.1列出了SRAM规格。

Table 42.1 SRAM specifications

Parameter	Without ECC	With ECC
SRAM capacity	SRAM0: 80 KB	SRAM0 (ECC area): 16 KB
SRAM address	SRAM0: 2000 4000h to 2001 7FFFh	SRAM0 (ECC area): 2000 0000h to 2000 3FFFh
Access*1	0 wait	
Module-stop function	Available	
Parity	8位数据和1位奇偶校验的偶校验	无平价
错误检查	偶校验错误检查	1位纠错和高达2位的错误检测

Note 1. 有关详细信息，请参阅第42.3.7节，访问周期。

42.2 注册说明

42.2.1 检测寄存器后的SRAM奇偶校验错误操作(PARIOAD)

Address(es): SRAM.PARIOAD 4000 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后的操作	1：复位0：不可屏蔽中断 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

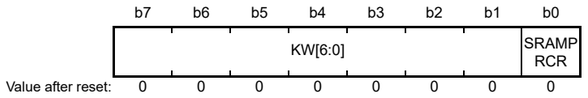
PARIOAD寄存器控制检测奇偶校验错误时的操作。SRAM保护寄存器(SRAMPRCR)保护该寄存器不被写入。在写入该寄存器之前启用SRAMPRCR寄存器中的SRAMPRCR位。访问SRAM时不要写入PARIOAD寄存器。

OAD位（检测后操作）

当检测到奇偶校验错误时，OAD位指定复位或不可屏蔽中断。OAD位用于SRAM0 (without ECC).

42.2.2 SRAM Protection Register (SRAMPRCR)

Address(es): SRAM.SRAMPRCR 4000 2004h



Bit	Symbol	Bit name	Description	R/W
b0	SRAMPRCR	Register Write Control	0: Disable writes to protected registers 1: Enable writes to protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writing to the SRAMPRCR bit.	R/W

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD register. When this bit is set to 1, writing to the PARIOAD register is enabled. When you write to this bit, write 78h to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, write 78h to the KW[6:0] bits simultaneously. When a value other than 78h is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 00h.

42.2.3 ECC Operating Mode Control Register (ECCMODE)

Address(es): SRAM.ECCMODE 4000 20C0h

Bit	Symbol	Bit name	Description	R/W
b1, b0	ECCMOD[1:0]	ECC Operating Mode Select	b1 b0 0 0: Disable ECC function 0 1: Setting prohibited 1 0: Enable ECC function without error checking 1 1: Enable ECC function with error checking.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

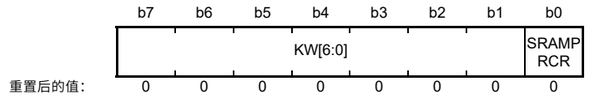
The ECCMODE register specifies the ECC operating mode. The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this register, set the ECCPRCR bit in the ECCPRCR register to 1. Do not write to the ECCMODE register while accessing the SRAM.

ECCMOD[1:0] bits (ECC Operating Mode Select)

The ECCMOD[1:0] bits set the access mode to the ECC area in SRAM.

42.2.2 SRAM保护寄存器(SRAMPRCR)

Address(es): SRAM.SRAMPRCR 4000 2004h



Bit	Symbol	位名称	Description	R/W
b0	SRAMPRCR	寄存器写控制	0：禁止写入受保护寄存器1：允许写入受保护寄存器。	R/W
b7 to b1	KW[6:0]	编写关键代码	这些位启用或禁用对SRAMPRCR位的写入。	R/W

SRAMPRCR位（寄存器写控制）

SRAMPRCR位控制PARIOAD寄存器的写模式。当该位设置为1时，写入启用PARIOAD寄存器。写入该位时，同时将78h写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对SRAMPRCR位的写入。写入SRAMPRCR位时，同时将78h写入KW[6:0]位。当78h以外的值写入KW[6:0]时，SRAMPRCR位不会更新。KW[6:0]位总是读为00h。

42.2.3 ECC操作模式控制寄存器(ECCMODE)

Address(es): SRAM.ECCMODE 4000 20C0h

Bit	Symbol	位名称	Description	R/W
b1, b0	ECCMOD[1:0]	ECC操作模式选择	b1b000：禁用ECC功能01：设置禁止10：启用ECC功能不进行错误检查11：启用ECC功能并进行错误检查。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECCMODE寄存器指定ECC工作模式。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该寄存器之前，将ECPCRR寄存器中的ECPCRR位设置为1。不要在访问SRAM时写入ECCMODE寄存器。

ECCMOD[1:0]位（ECC操作模式选择）

ECCMOD[1:0]位将访问模式设置为SRAM中的ECC区域。

42.2.4 ECC 2-Bit Error Status Register (ECC2STS)

Address(es): SRAM.ECC2STS 4000 20C1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC2ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECC2ERR	ECC 2-Bit Error Status	0: No 2-bit ECC error occurred 1: 2-bit ECC error occurred.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

ECC2ERR bit (ECC 2-Bit Error Status)

The ECC2ERR bit indicates whether a 2-bit ECC error occurred in the ECC area of the SRAM. When a 2-bit error is detected while ECC operations are enabled and error checking is selected, the ECC2ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 2-bit ECC error can be cleared by writing 0 to the ECC2ERR bit. The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in the SRAM while writing 0 to this register.

42.2.5 ECC 1-Bit Error Information Update Enable Register (ECC1STSEN)

Address(es): SRAM.ECC1STSEN 4000 20C2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	E1STSEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	E1STSEN	ECC 1-Bit Error Information Update Enable	0: Disable updating of 1-bit ECC error information 1: Enable updating of 1-bit ECC error information.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC1STSEN register enables or disables updating of the ECC 1-bit Error Status Register (ECC1STS) in response to a 1-bit ECC error in the SRAM (ECC area). The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled).

E1STSEN bit (ECC 1-Bit Error Information Update Enable)

The E1STSEN bit enables or disables updating of the SRAM (ECC area) 1-Bit Error Status Register (ECC1STS) in response to a 1-bit error in the ECC area of SRAM. This register also functions as an interrupt or reset mask.

42.2.4 ECC2位错误状态寄存器(ECC2STS)

Address(es): SRAM.ECC2STS 4000 20C1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC2ERR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECC2ERR	ECC2位错误状态	0：未发生2位ECC错误1：发生2位ECC错误。	R(/W)*1
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0以清除该位。

ECC2ERR位（ECC2位错误状态）

ECC2ERR位指示SRAM的ECC区域是否发生2位ECC错误。当启用ECC操作并选择错误检查时检测到2位错误时，ECC2ERR位设置为1。此时SRAM错误信号也被置位。将0写入ECC2ERR位可清除2位ECC错误。SRAM错误可以指定为不可屏蔽中断或ECCOAD寄存器中的复位。向该寄存器写入0时不要访问SRAM中的ECC区域。

42.2.5 ECC1位错误信息更新使能寄存器(ECC1STSEN)

Address(es): SRAM.ECC1STSEN 4000 20C2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	E1STSEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	E1STSEN	ECC1位错误信息更新启用	0：禁止更新1-bitECC错误信息1：允许更新1-bit ECC错误信息。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECC1STSEN寄存器启用或禁用ECC1位错误状态寄存器(ECC1STS)的更新，以响应SRAM（ECC区域）中的1位ECC错误。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。

E1STSEN位（ECC1位错误信息更新使能）

E1STSEN位启用或禁用SRAM（ECC区域）1位错误状态寄存器(ECC1STS)的更新，以响应SRAM的ECC区域中的1位错误。该寄存器还用作中断或复位掩码。

42.2.6 ECC 1-Bit Error Status Register (ECC1STS)

Address(es): SRAM.ECC1STS 4000 20C3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC1ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECC1ERR	ECC 1-Bit Error Status	0: No 1-bit ECC error occurred 1: 1-bit ECC error occurred.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

ECC1ERR bit (ECC 1-Bit Error Status)

The ECC1ERR bit indicates whether a 1-bit ECC error occurred in the ECC area of the SRAM. When a 1-bit error is detected while ECC operations are enabled, error correction is selected, and updating of the 1-bit error information is enabled. The ECC1ERR bit is set to 1 and the SRAM error signal is asserted at this time. The 1-bit ECC error can be cleared by writing 0 to the ECC1ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in the SRAM while writing 0 to this register.

42.2.7 ECC Protection Register (ECCPRCR)

Address(es): SRAM.ECCPRCR 4000 20C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							ECCPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECCPRCR	Register Write Control	0: Disable writes to the protected registers 1: Enable writes to the protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writes to the ECCPRCR bit.	R/W

ECCPRCR bit (Register Write Control)

The ECCPRCR bit controls the write mode of the ECCMODE, ECC1STSEN, and ECCOAD registers. When this bit is set to 1, writing to the ECCMODE, ECC1STSEN, and ECCOAD registers is enabled. When writing to this bit, write 78h to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the ECCPRCR bit. When writing to the ECCPRCR bit, write 78h to the KW[6:0] bits simultaneously. When a value other than 78h is written to KW[6:0], the ECCPRCR bit is not updated. The KW[6:0] bits are always read as 00h.

42.2.6 ECC1位错误状态寄存器(ECC1STS)

Address(es): SRAM.ECC1STS 4000 20C3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC1ERR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECC1ERR	ECC1位错误状态	0：未发生1位ECC错误1：发生1位ECC错误。	R(/W)*1
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0以清除该位。

ECC1ERR位（ECC1位错误状态）

ECC1ERR位指示SRAM的ECC区域是否发生1位ECC错误。如果在启用ECC操作时检测到1位错误，则选择纠错，并启用1位错误信息的更新。ECC1ERR位设置为1，此时SRAM错误信号有效。将0写入ECC1ERR位可清除1位ECC错误。

SRAM错误可以指定为不可屏蔽中断或ECCOAD寄存器中的复位。向该寄存器写入0时不要访问SRAM中的ECC区域。

42.2.7 ECC保护寄存器(ECPCRR)

Address(es): SRAM.ECCPRCR 4000 20C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							ECCPRCR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECCPRCR	寄存器写控制	0：禁止写入受保护寄存器1：允许写入受保护寄存器。	R/W
b7 to b1	KW[6:0]	编写关键代码	这些位启用或禁用对ECPCRR位的写入。	R/W

ECPCRR位（寄存器写控制）

ECPCRR位控制ECCMODE、ECC1STSEN和ECCOAD寄存器的写模式。当该位设置为1时，允许写入ECCMODE、ECC1STSEN和ECCOAD寄存器。写入该位时，同时将78h写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对ECPCRR位的写入。当写入ECPCRR位时，将78h写入KW[6:0]位同时进行。当向KW[6:0]写入78h以外的值时，不会更新ECPCRR位。这KW[6:0]位总是读为00h。

42.2.8 ECC Protection Register 2 (ECCPRCR2)

Address(es): SRAM.ECCPRCR2 4000 20D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW2[6:0]							ECCPRCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECCPRCR2	Register Write Control	0: Disable writes to the protected registers 1: Enable writes to the protected registers.	R/W
b7 to b1	KW2[6:0]	Write Key Code	These bits enable or disable writes to the ECCPRCR2 bit.	R/W

ECCPRCR2 bit (Register Write Control)

The ECCPRCR2 bit controls the write mode of the ECCETST register. When the ECCPRCR2 bit is set to 1, writes to the ECCETST register is enabled. When writing to this bit, write 78h to the KW2[6:0] bits simultaneously.

KW2[6:0] bits (Write Key Code)

The KW2[6:0] bits enable or disable writing to the ECCPRCR2 bit. When writing to the ECCPRCR2 bit, write 78h to KW2[6:0] simultaneously. When a value other than 78h is written to KW2[6:0], the ECCPRCR2 bit is not updated. The KW2[6:0] bits are always read as 00h.

42.2.9 ECC Test Control Register (ECCETST)

Address(es): SRAM.ECCETST 4000 20D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TSTBYP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSTBYP	ECC Bypass Select	0: Disable ECC bypass 1: Enable ECC bypass.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC Protection Register 2 (ECCPRCR2) protects this register against writes. Before writing to this bit, set the ECCPRCR2 bit in the ECCPRCR2 register to 1 (write protection disabled). Do not write to the ECCETST register while accessing the SRAM.

TSTBYP bit (ECC Bypass Select)

The TSTBYP bit enables direct access to the ECC code by bypassing the ECC function. When the ECC bypass function is used, the ECCMOD[1:0] bits in the ECCMODE register are set to 00b. The ECC must be accessed in 32 bits using the same address for 32-bit data. The ECC code is assigned to the lower 7 bits of the 32-bit data. When writing the ECC code, the upper 25 bits are ignored. When reading the ECC code, the upper 25 bits are undefined.

Note: For details on the ECC test, see section 42.3.4, ECC Decoder Testing.

42.2.8 ECC保护寄存器2(ECPCRR2)

Address(es): SRAM.ECCPRCR2 4000 20D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW2[6:0]							ECCPRCR2
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECCPRCR2	寄存器写控制	0：禁止写入受保护寄存器1：允许写入受保护寄存器。	R/W
b7 to b1	KW2[6:0]	编写关键代码	这些位启用或禁用对ECPCRR2位的写入。	R/W

ECPCRR2位（寄存器写控制）

ECPCRR2位控制ECCETST寄存器的写模式。当ECPCRR2位设置为1时，写入ECCETST寄存器使能。写入该位时，同时将78h写入KW2[6:0]位。

KW2[6:0]位（写入密钥代码）

KW2[6:0]位启用或禁用写入ECPCRR2位。当写入ECPCRR2位时，将78h写入KW2[6:0]同时。当向KW2[6:0]写入78h以外的值时，不会更新ECPCRR2位。这KW2[6:0]位总是读为00h。

42.2.9 ECC测试控制寄存器(ECCETST)

Address(es): SRAM.ECCETST 4000 20D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TSTBYP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSTBYP	ECC旁路选择	0：禁用ECC旁路1：启用ECC旁路。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECC保护寄存器2(ECCPRCR2)保护该寄存器不被写入。在写入该位之前，将ECPCRR2寄存器中的ECPCRR2位为1（写保护禁用）。访问SRAM时不要写入ECCETST寄存器。

TSTBYP位（ECC旁路选择）

TSTBYP位允许通过绕过ECC功能直接访问ECC代码。使用ECC旁路功能时，ECCMODE寄存器中的ECCMOD[1:0]位设置为00b。必须使用32位数据的相同地址以32位访问ECC。ECC代码分配给32位数据的低7位。写入ECC代码时，忽略高25位。读取ECC码时，高25位未定义。

Note: 有关ECC测试的详细信息，请参阅第42.3.4节，ECC解码器测试。

42.2.10 SRAM ECC Error Operation After Detection Register (ECCOAD)

Address(es): SRAM.ECCOAD 4000 20D8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation After Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit selects whether to generate a reset or a non-maskable interrupt when an ECC error is detected. The OAD bit in the ECCOAD register is used for SRAM (ECC area).

42.3 Operation

42.3.1 Low Power Consumption Function

Power consumption can be reduced by setting the Module Stop Control Register A (MSTPCRA) to stop the supply of the clock signal to the SRAM. When both the MSTPA0 and the MSTPA6 bits in MSTPCRA are set to 1, supply of the clock signal to SRAM0 is stopped*1.

Note 1. The MSTPA0 bit and MSTPA6 bit in MSTPCRA must be set to the same value.

Stopping the clock signal supply places the SRAM in the module-stop state. The SRAM is not accessible in the module-stop state. Do not transition to the module-stop state while access to the SRAM is in progress. Access to the SRAM in the module-stop state is prohibited. If access is attempted, correct operation is not guaranteed.

For details on the MSTPCRA register, see section 11, Low Power Modes.

Power consumption can be further reduced in Software Standby mode as the supply voltage for SRAM0 can be off except for the 48 KB in the head area of SRAM0 (2000 0000h to 2000 BFFFh). For details on Software Standby mode, see section 11, Low Power Modes.

42.3.2 ECC Function

You can enable or disable the ECC function by setting the ECCMODE register. By default, the ECC function is disabled and the ECC check type is SEC-DED (Single-Error Correction and Double-Error Detection).

When the ECC function is enabled, 7-bit check bits are appended to the 32-bit data for writes. For reads, 39-bit data (32-bit data and 7-bit check bits) is read from the SRAM (ECC area).

When the ECC function and error checking are both enabled, an error correction is performed if a 1-bit error occurs, and the ECC1ERR bit in the ECC1STS register is set to 1 if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, the error is detected without error correction, and the ECC2ERR bit in the ECC2STS register is set to 1.

When the ECC function is enabled and the error checking is disabled, error correction is performed if a 1-bit error occurs but the ECC1ERR bit in the ECC1STS register is not updated even if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, the error is detected but the ECC2ERR bit in the ECC2STS register is not updated, and error correction is not performed.

When the ECC function is disabled, neither error correction nor error detection is performed even when a 1-bit or 2-bit

42.2.10 SRAMECC检测后错误操作寄存器(ECCOAD)

Address(es): SRAM.ECCOAD 4000 20D8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后的操作	1：复位0：不可屏蔽中断 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将
ECPCRR寄存器中的ECPCRR位为1（写保护禁用）。访问SRAM时不要写入ECCOAD寄存器。

OAD位（检测后操作）

OAD位选择在检测到ECC错误时是否产生复位或不可屏蔽中断。ECCOAD寄存器中的OAD位用于SRAM（ECC区域）。

42.3 Operation

42.3.1 低功耗功能

通过设置模块停止控制寄存器A(MSTPCRA)以停止向SRAM提供时钟信号，可以降低功耗。当MSTPCRA中的MSTPA0和MSTPA6位都设置为1时，停止向SRAM0提供时钟信号*1。

注1.MSTPCRA中的MSTPA0位和MSTPA6位必须设置为相同的值。

停止时钟信号供应会将SRAM置于模块停止状态。SRAM在模块停止状态下不可访问。在访问SRAM的过程中不要转换到模块停止状态。禁止在模块停止状态下访问SRAM。如果尝试访问，则无法保证正确操作。

有关MSTPCRA寄存器的详细信息，请参见第11节，低功耗模式。

在软件待机模式下，功耗可以进一步降低，因为除了SRAM0头部区域的48KB（20000000h到2000BFFFh）之外，SRAM0的电源电压可以关闭。有关软件待机模式的详细信息，请参见第11节，低功耗模式。

42.3.2 ECC Function

您可以通过设置ECCMODE寄存器来启用或禁用ECC功能。默认情况下，ECC功能关闭，ECC检查类型为SEC-DED（Single-ErrorCorrectionandDouble-ErrorDetection）。

当ECC功能使能时，7位校验位会附加到32位数据以进行写入。对于读取，从SRAM（ECC区域）读取39位数据（32位数据和7位校验位）。

当ECC功能和错误检查都使能时，如果发生1位错误，则执行错误纠正，如果ECC1STSEN寄存器中的E1STSEN位为1，则ECC1STS寄存器中的ECC1ERR位设置为1。如果2位错误，检测到错误而不进行纠错，ECC2STS寄存器中的ECC2ERR位设置为1。

当启用ECC功能且禁用错误检查时，如果发生1位错误，但即使ECC1STSEN寄存器中的E1STSEN位为1，ECC1STS寄存器中的ECC1ERR位也不会更新，则执行纠错。如果2-位错误，检测到错误但ECC2STS寄存器中的ECC2ERR位没有更新，也没有执行错误纠正。

禁用ECC功能时，即使是1位或2位，也不会执行纠错或错误检测

error occurs. Therefore, the ECC1ERR or ECC2ERR bit is not updated.

It is not possible to confirm the location where the error is detected. Therefore, after an error occurred, update all the data by writing 32-bit data to the SRAM.

When a read access is performed consecutively after a write access, the read access has priority. Therefore, during initialization, do not perform a read access successively after a write access.

42.3.3 ECC Error Generation

When the ECC function is enabled and error checking is applied to the SRAM (ECC area), an ECC error occurs when either the ECC2ERR bit in the ECC2STS register or the ECC1ERR bit in the ECC1STS register becomes 1 to indicate that a 2-bit error or a 1-bit error has occurred.

To mask ECC 1-bit errors, set the ECC1STSEN.E1STSEN bit to 0 to disable the ECC1ERR bit update. An ECC error is not generated when the ECC function is disabled or enabled without error checking.

An ECC error can generate a non-maskable interrupt or a reset, as selected in the ECCOAD register. When the OAD bit in the ECCOAD register is set to 1, an ECC error is output to the reset function. When the OAD bit in the ECCOAD register is set to 0, an ECC error is output to the ICU as a non-maskable interrupt.

42.3.4 ECC Decoder Testing

Figure 42.1 shows the ECC decoder testing.

发生错误。因此，ECC1ERR或ECC2ERR位不会更新。

无法确认检测到错误的位置。因此，发生错误后，通过将32位数据写入SRAM来更新所有数据。

当在写访问之后连续执行读访问时，读访问具有优先权。因此，在初始化过程中，不要在写访问之后再进行读访问。

42.3.3 ECC错误生成

当启用ECC功能并对SRAM（ECC区域）应用错误检查时，当ECC2STS寄存器中的ECC2ERR位或ECC1STS寄存器中的ECC1ERR位变为1时，将发生ECC错误，指示2位错误或发生1位错误。

要屏蔽ECC1位错误，请将ECC1STSEN.E1STSEN位设置为0以禁用ECC1ERR位更新。当ECC功能被禁用或启用而不进行错误检查时，不会产生ECC错误。

根据ECCOAD寄存器的选择，ECC错误会产生不可屏蔽的中断或复位。当ECCOAD寄存器中的OAD位设置为1时，向复位功能输出ECC错误。当ECCOAD寄存器中的OAD位设置为0时，ECC错误作为不可屏蔽中断输出到ICU。

42.3.4 ECC解码器测试

图42.1显示了ECC解码器测试。

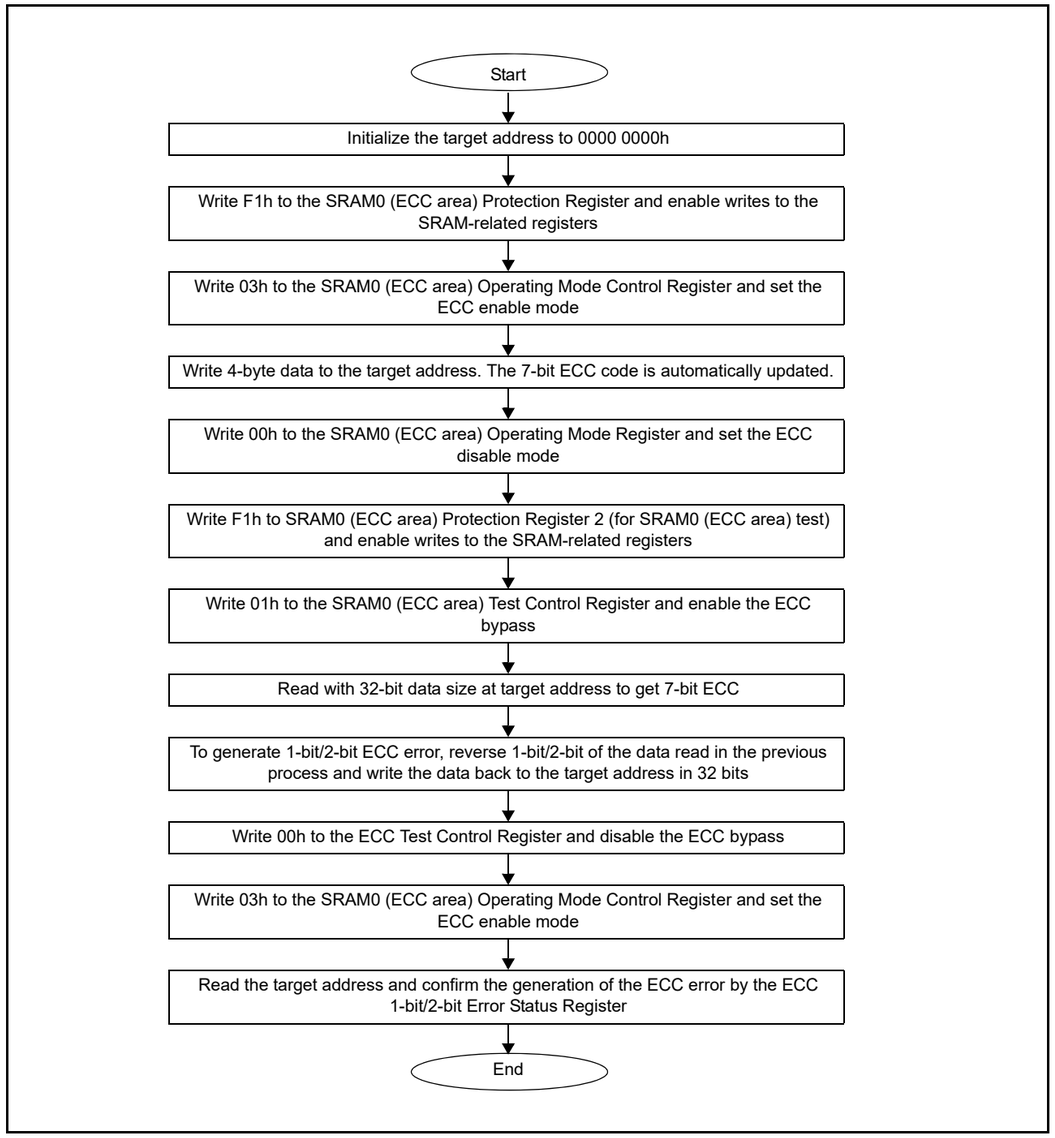


Figure 42.1 ECC decoder testing

42.3.5 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. When data is written, a parity bit is added to every 8-bit data in the SRAM which has 32-bit data width, and when data is read, the parity is checked. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset. The specification of SRAM0 without ECC is even parity.

The parity error notification can be specified as a non-maskable interrupt or a reset in the OAD bit in the PARIOAD register. When the OAD bit is set to 1, a parity error is output to the reset function. When the OAD bit is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause of the parity error is noise or corruption, follow

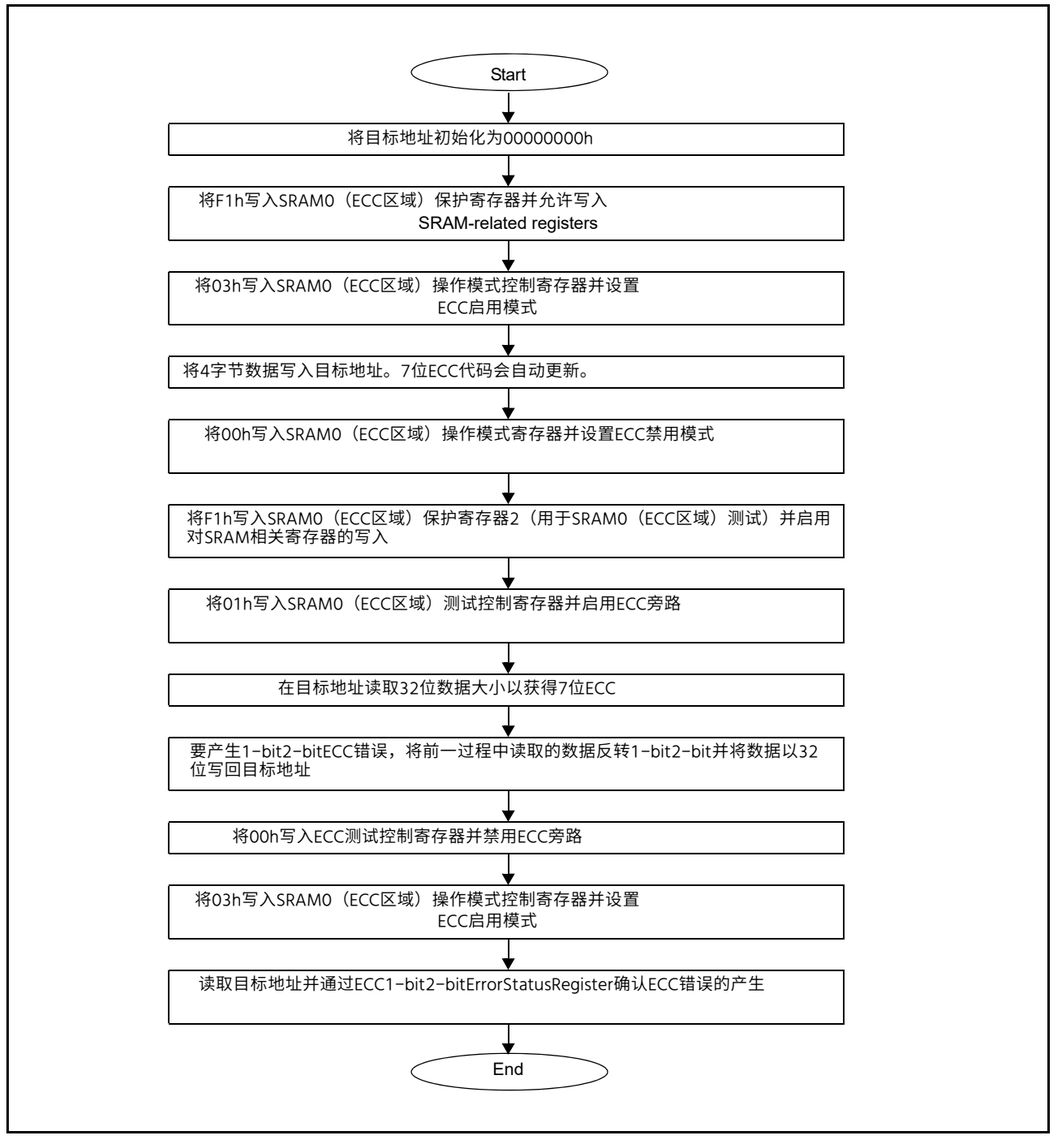


Figure 42.1 ECC解码器测试

42.3.5 奇偶校验计算功能

IEC60730标准要求检查SRAM数据。写入数据时，对32位数据宽度的SRAM中的每8位数据添加一个奇偶校验位，读取数据时检查奇偶校验位。发生奇偶校验错误时，会生成奇偶校验错误通知。此功能也可用于触发复位。没有ECC的SRAM0的规格是偶校验。

奇偶校验错误通知可以在PARIOAD寄存器的OAD位中指定为不可屏蔽中断或复位。当OAD位设置为1时，奇偶校验错误输出到复位功能。当OAD位设置为0时，奇偶校验错误作为不可屏蔽中断输出到ICU。

奇偶校验错误经常因噪声而发生。要确认奇偶校验错误的原因是噪音还是损坏，请按照

the parity check flows shown in Figure 42.2 and Figure 42.3.

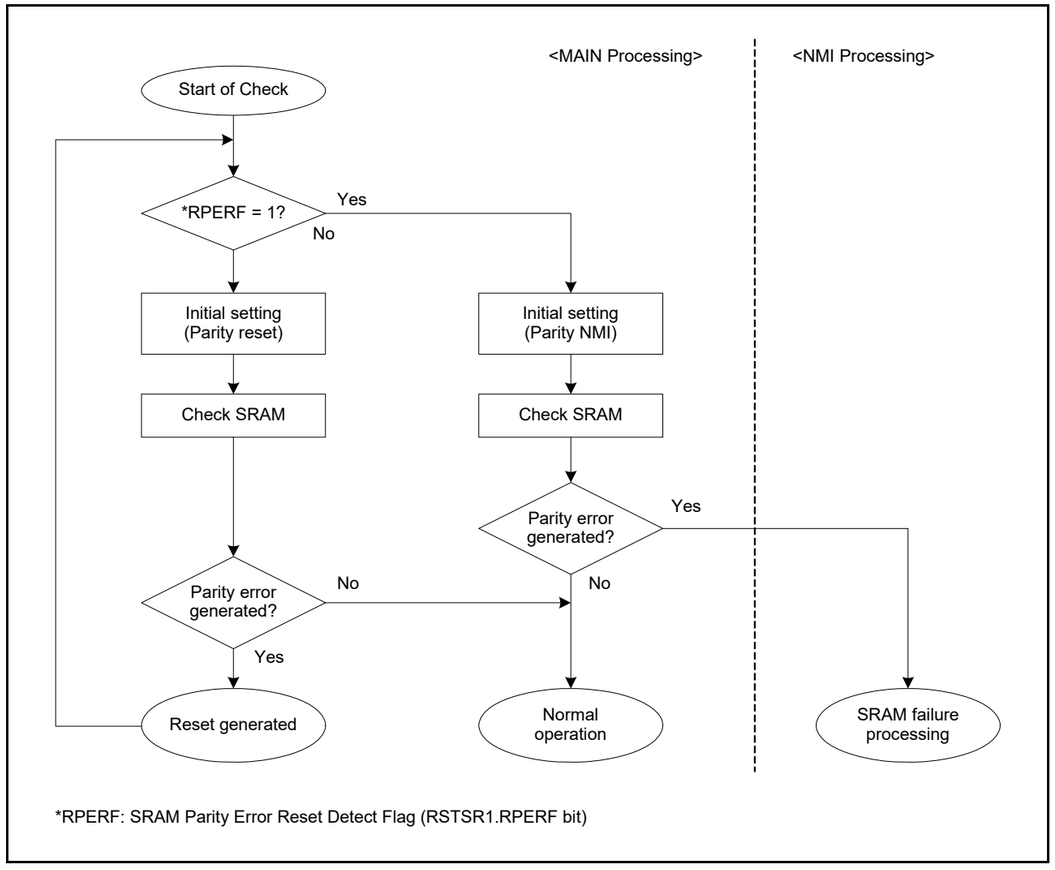


Figure 42.2 Flow of SRAM parity check when SRAM parity reset is enabled

奇偶校验流程如图42.2和图42.3所示。

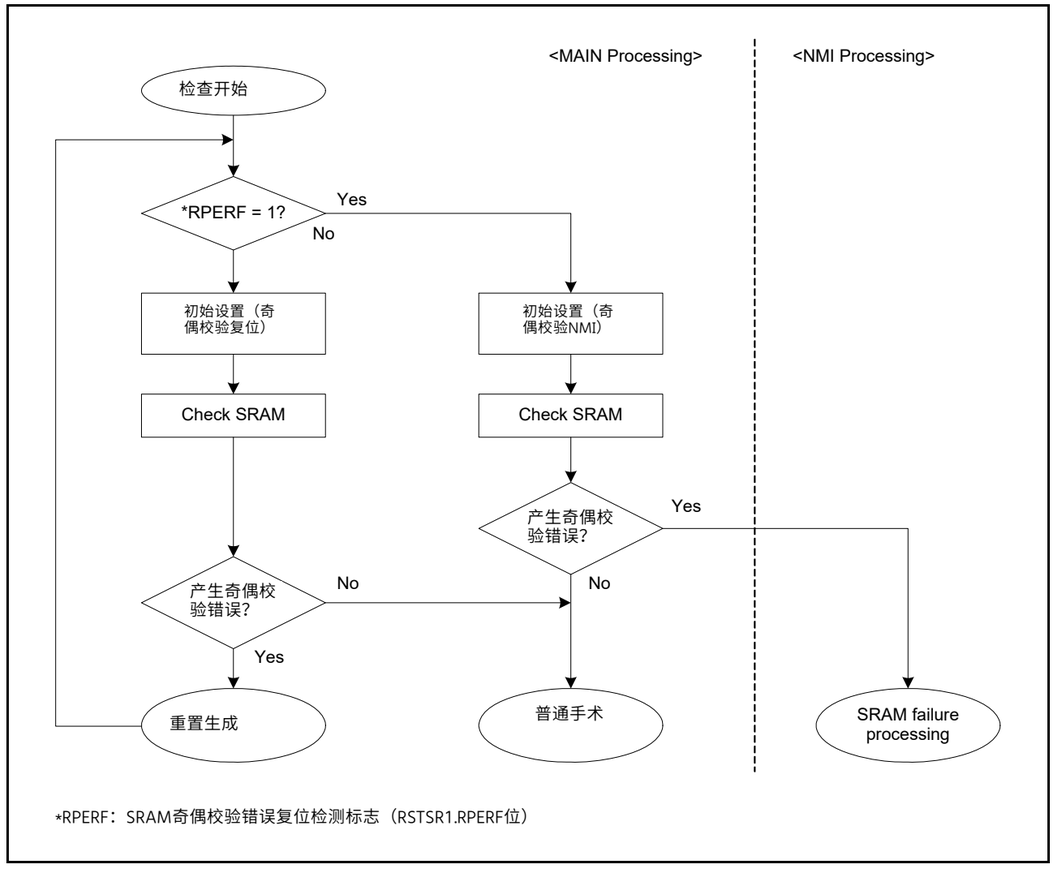


Figure 42.2 启用SRAM奇偶校验复位时的SRAM奇偶校验流程

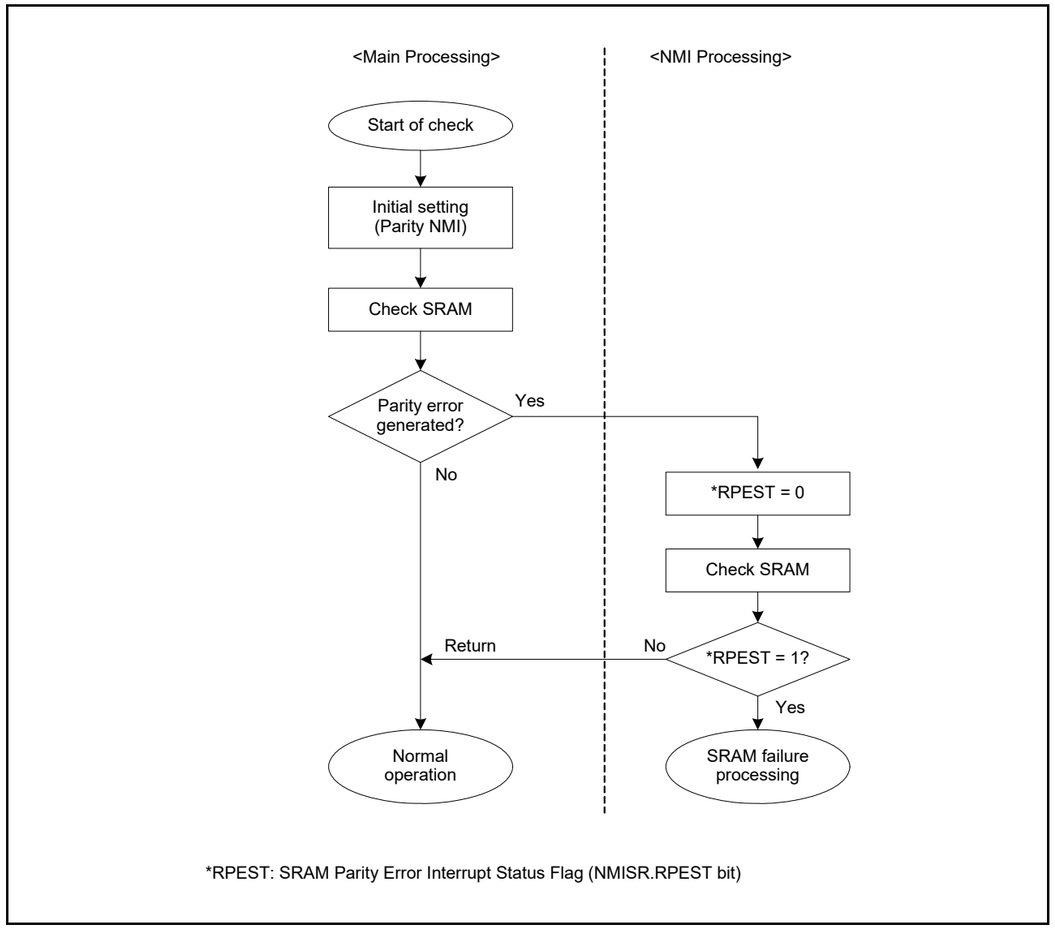


Figure 42.3 Flow of SRAM parity check when SRAM parity interrupt is enabled

42.3.6 SRAM Error Sources

An SRAM error source is either an ECC error or a parity error. ECC error or parity error can generate either a non-maskable interrupt or a reset, as selected with the OAD bit in the ECCOAD register for ECC error, or PARIOAD register for parity error.

Table 42.2 SRAM error sources

Error source	DTC activation	DMAC activation
ECC error (SRAM0 area with ECC)	Not possible	Not possible
Parity error (SRAM0 area without ECC)	Not possible	Not possible

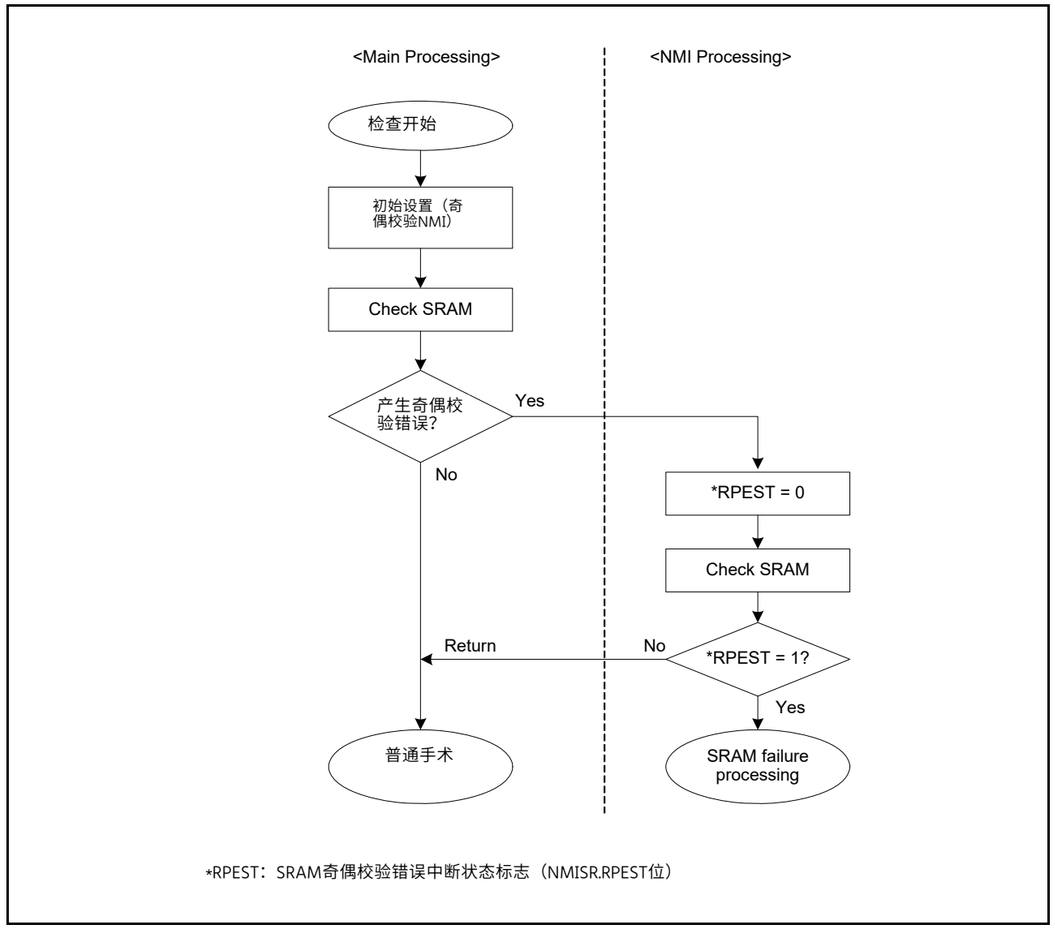


Figure 42.3 启用SRAM奇偶校验中断时的SRAM奇偶校验流程

42.3.6 SRAM错误源

SRAM错误源是ECC错误或奇偶校验错误。ECC错误或奇偶校验错误可以产生不可屏蔽的中断或复位，由ECCOAD寄存器中的OAD位选择用于ECC错误，或PARIOAD寄存器用于奇偶校验错误。

Table 42.2 SRAM错误源

错误来源	DTC activation	DMAC activation
ECC错误（带ECC的SRAM0区域）	不可能	不可能
奇偶校验错误（没有ECC的SRAM0区域）	不可能	不可能

42.3.7 Access Cycle

Table 42.3 SRAM0 (ECC area 2000 0000h to 2000 3FFFh)

	Read (cycle)		Write (cycle)	
Bit setting	**Word access**	**Halfword/Byte access**	**Word access**	**Halfword/Byte access**
ECC Off ECCMOD[1] = 0	2		2	
ECC On ECCMOD[1] = 1	2		2	4

Table 42.4 SRAM0 (Parity area 2000 4000h to 2001 7FFFh)

Read (cycle)		Write (cycle)	
Word Access	**Halfword/Byte access**	**Word access**	**Halfword/Byte access**
2		2	

42.4 Usage Notes

42.4.1 Instruction Fetch from SRAM area

When using SRAM0 to operate a program, initialize the SRAM area so that the CPU can correctly prefetch data. If the CPU prefetches data from an SRAM area that is not initialized, an ECC error or a parity error might occur. Initialize the additional 12-byte area from the end address of a program with a 4-byte boundary.

42.4.2 Store Buffer of SRAM

For fast access between SRAM and CPU, a store buffer is used. When a load instruction is executed from the same address after a store instruction to SRAM, the load instruction might read data from the buffer instead of data on the SRAM. To read data on the SRAM correctly, use either of the following procedures:

- After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A)
- After writing to the SRAM (address = A), read data from area other than SRAM (address = A), then read the SRAM (address = A).

42.3.7 访问周期

Table 42.3 SRAM0（ECC区域20000000h到20003FFFh）

	Read (cycle)		Write (cycle)	
位设置	**字访问**	**Halfword/Byte access**	**字访问**	**Halfword/Byte access**
ECC Off ECCMOD[1] = 0	2		2	
ECC On ECCMOD[1] = 1	2		2	4

Table 42.4 SRAM0（奇偶校验区20004000h到20017FFFh）

Read (cycle)		Write (cycle)	
字访问	**Halfword/Byte access**	**字访问**	**Halfword/Byte access**
2		2	

42.4 使用说明

42.4.1 从SRAM区域取指令

使用SRAM0操作程序时，初始化SRAM区域，以便CPU可以正确预取数据。如果CPU从未初始化的SRAM区域预取数据，则可能会发生ECC错误或奇偶校验错误。用4字节边界从程序的结束地址初始化额外的12字节区域。

42.4.2 SRAM的存储缓冲区

对于SRAM和CPU之间的快速访问，使用了存储缓冲区。如果在对SRAM执行存储指令之后从同一地址执行加载指令，则加载指令可能会从缓冲区读取数据，而不是从SRAM中读取数据。要正确读取SRAM上的数据，请使用以下任一过程：

- 写入SRAM（地址=A）后，使用NOP指令，然后读取SRAM（地址=A）
- 写入SRAM（地址=A）后，从SRAM以外的区域（地址=A）读取数据，然后读取SRAM（地址=A）。

43. Flash Memory

43.1 Overview

The MCU provides up to 512-KB code flash memory and 8-KB data flash memory. The Flash Control Block (FCB) controls the flash memory programming commands. This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

Table 43.1 lists the specifications of the code flash memory and data flash memory, and Figure 43.1 shows a block diagram of the related modules. Figure 43.2 shows the configuration of the code flash memory, and Figure 43.3 shows the configuration of the data flash memory.

Table 43.1 Specifications of code flash memory and data flash memory

Parameter	Code flash memory	Data flash memory
Memory capacity	512 KB of user area	8 KB of data area
Read cycle	• 32 MHz < ICLK frequency ≤ 48 MHz Cache hit: 1 cycle Cache miss: 2, 3 cycles • ICLK frequency ≤ 32 MHz Cache hit: 1 cycle Cache miss: 1 cycle	A read operation takes 6 FCLK cycles in bytes (FCLK frequency ≤ 32 MHz)
Value after erasure	FFh	FFh
Programming/erasing method	• Programming and erasure of code and data flash memory through the FCB commands specified in the registers • Programming by dedicated flash-memory programmer through a serial interface (serial programming) • Programming of flash memory by user program (self-programming).	
Security function	Protection against illicit tampering or reading of data in flash memory	
Protection	Protection against erroneous overwriting of flash memory	
Background operations (BGOs)	Code flash memory can be read during data flash memory programming	
Units of programming and erasure	• 64-bit units for programming in user area • 2-KB units for erasure in user area.	• 8-bit units for programming in data area • 1-KB units for erasure in data area.
Other functions	Interrupts accepted during self-programming	
	An expansion area of flash memory (option bytes) can be set in the initial MCU settings	
On-board programming	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically. Programming in serial programming mode (USB boot mode): • USBFS used • Dedicated hardware not required, so direct connection to a PC is possible. Programming in on-chip debug mode: • JTAG or SWD interface used • Dedicated hardware not required. Programming by a routine for code and data flash memory programming within the user program: • Allows code and data flash memory programming without resetting the system.	

43. 闪存

43.1 Overview

MCU提供高达512-KB的代码闪存和8-KB的数据闪存。闪存控制块(FCB)控制闪存编程命令。本产品使用SiliconStorageTechnology Inc.许可的SuperFlash®技术。

表43.1列出了代码闪存和数据闪存的规格，图43.1给出了相关模块的框图。图43.2显示了代码闪存的配置，图43.3显示了数据闪存的配置。

Table 43.1 代码闪存和数据闪存的规格

Parameter	代码闪存	数据闪存
内存容量	512KB的用户区	8KB数据区
读周期	32MHz<ICLK频率≤48MHz高速缓存命中：1个周期 缓存未命中：2、3个周期 ICLK频率≤32MHz缓存命中：1个周期 缓存未命中：1个周期	读取操作需要6个FCLK周期（以字节为单位）（FCLK频率≤32MHz）
擦除后的值	FFh	FFh
Programming/erasing method	通过寄存器中指定的FCB命令对闪存代码和数据进行编程和擦除 由专用闪存编程器通过串行接口进行编程（串行编程） 通过用户程序对闪存进行编程（自编程）。	
安全功能	防止非法篡改或读取闪存中的数据	
Protection	防止错误覆盖闪存	
后台操作(BGO)	在数据闪存编程期间可以读取代码闪存	
编程和擦除单元	用于用户区编程的64位单元 用于用户区擦除的2KB单元。	用于数据区编程的8位单元 用于数据区擦除的1-KB单元。
其他功能	自编程期间接受的中断	
	可在初始MCU设置中设置闪存的扩展区域（选项字节）	
On-board programming	在串行编程模式（SCI引导模式）下编程： 使用异步串行接口(SCI9) 自动调整传输速率。 在串行编程模式（USB引导模式）下编程： 使用USBFS 不需要专用硬件，因此可以直接连接到PC。在片上调试模式下编程： 使用JTAG或SWD接口 不需要专用硬件。通过用户程序中的代码和数据闪存编程例程进行编程： 允许在不重置系统的情况下对代码和数据闪存进行编程。	

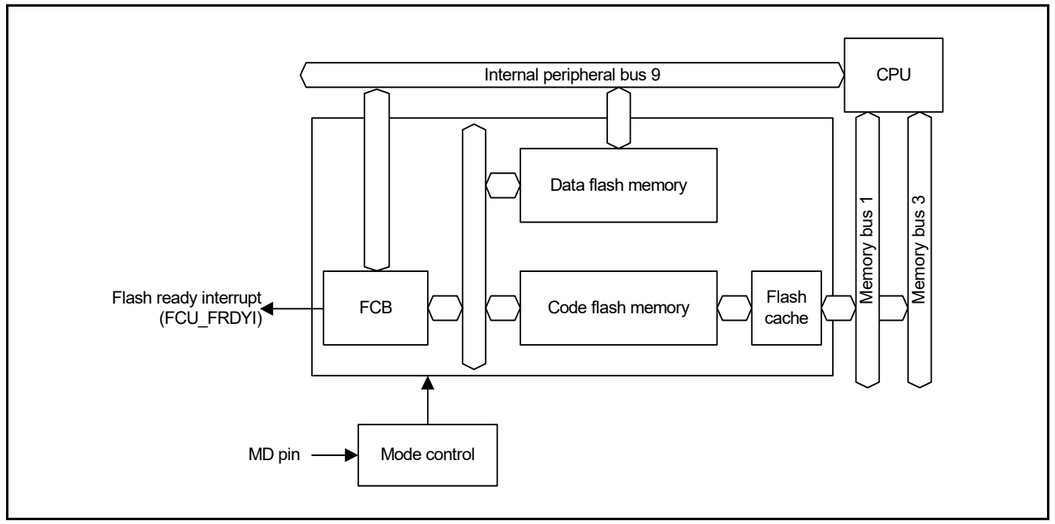


Figure 43.1 Flash memory-related modules block diagram

43.2 Memory Structure

Figure 43.2 shows the mapping of the code flash memory, and Table 43.2 shows the read and programming and erasure (P/E) addresses of the code flash memory. The user space of the code flash memory is divided into 2-KB blocks that serve as the units of erasure. The user area is available for storing the user program.

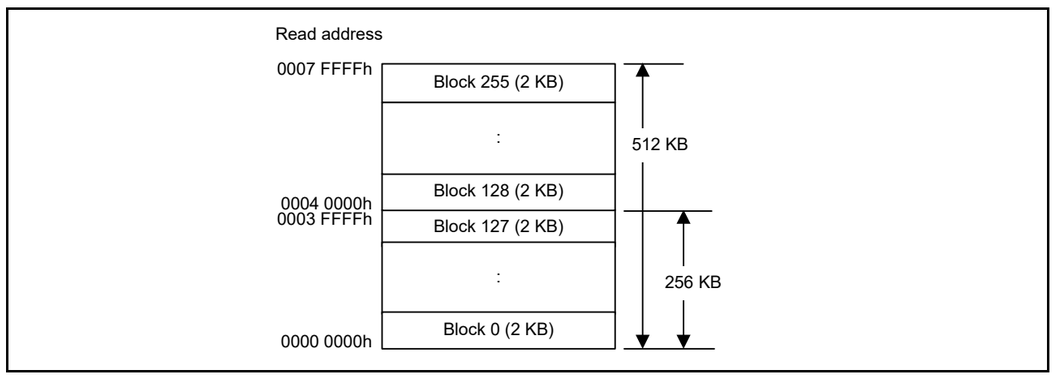


Figure 43.2 Mapping of the code flash memory

Table 43.2 Read and P/E addresses of the code flash memory

Size of code flash memory	Read address	P/E address	Number of blocks
512 KB	0000 0000h to 0007 FFFFh	0000 0000h to 0007 FFFFh	0 to 255

The data area of the data flash memory is divided into 1-KB blocks, with each being a unit for erasure. Figure 43.3 shows the mapping of the data flash memory, and Table 43.3 shows the read, programming and erasure addresses of the data flash memory.

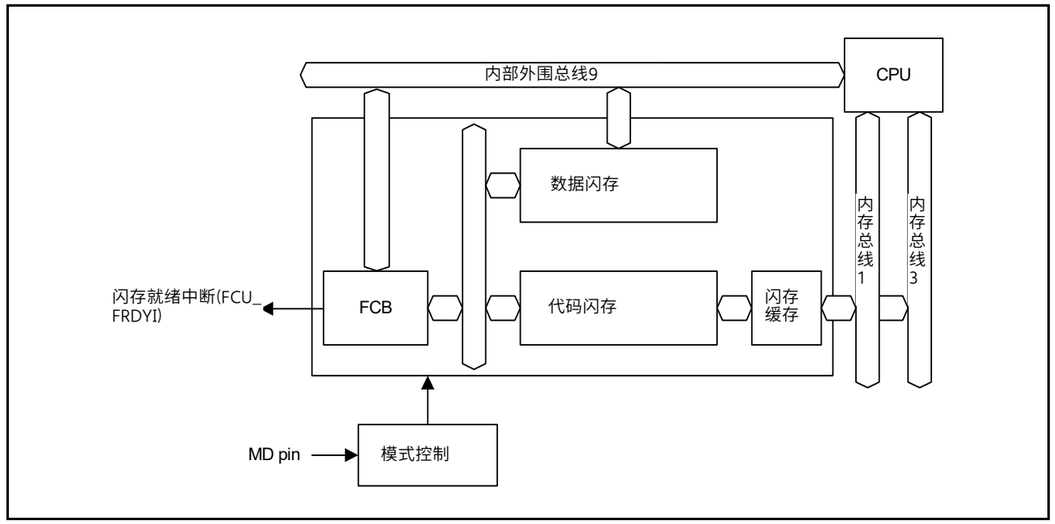


Figure 43.1 闪存相关模块框图

43.2 内存结构

图43.2显示了代码闪存的映射，表43.2显示了代码闪存的读取和编程和擦除(PE)地址。代码闪存的用户空间被划分为2KB的块，作为擦除单元。用户区可用于存储用户程序。

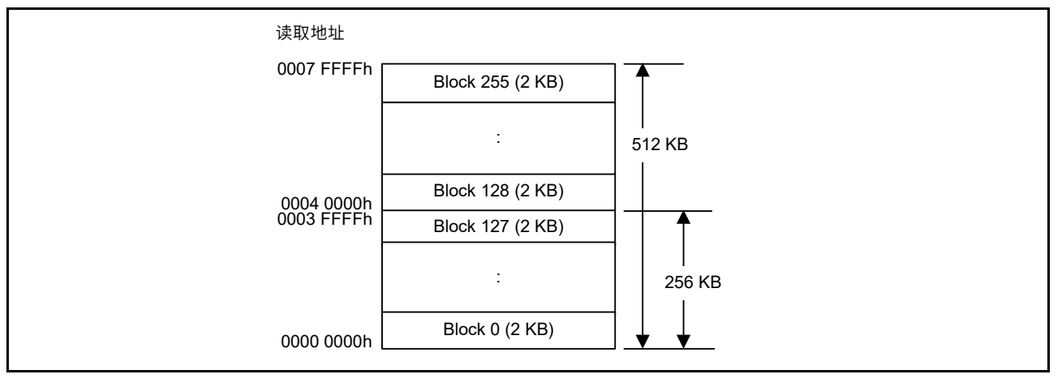


Figure 43.2 代码闪存的映射

Table 43.2 代码闪存的读取和PE地址

代码闪存大小	读取地址	P/E address	块数
512 KB	0000 0000h to 0007 FFFFh	0000 0000h to 0007 FFFFh	0 to 255

数据闪存的数据区域被划分为1-KB块，每个块为一个擦除单元。图43.3显示了数据闪存的映射，表43.3显示了数据闪存的读取、编程和擦除地址。

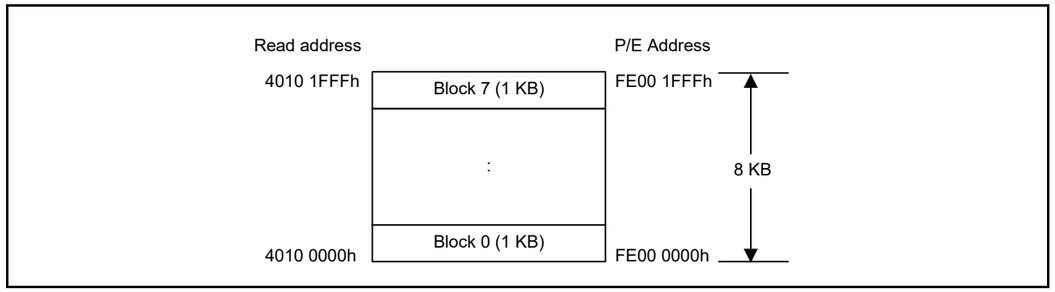


Figure 43.3 Mapping of the data flash memory

Table 43.3 Read and P/E addresses of the data flash memory

Size of data flash memory	Read address	P/E address	Number of blocks
8 KB	4010 0000h to 4010 1FFFh	FE00 0000h to FE00 1FFFh	0 to 7

43.3 Flash Cache

43.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access of CPU instruction fetch.

Table 43.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	• 64 bits/entry (64-bit aligned data) • 8 entries/ways.	• 64 bits/entry (64-bit aligned data) • 1 entry.	• 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction.
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

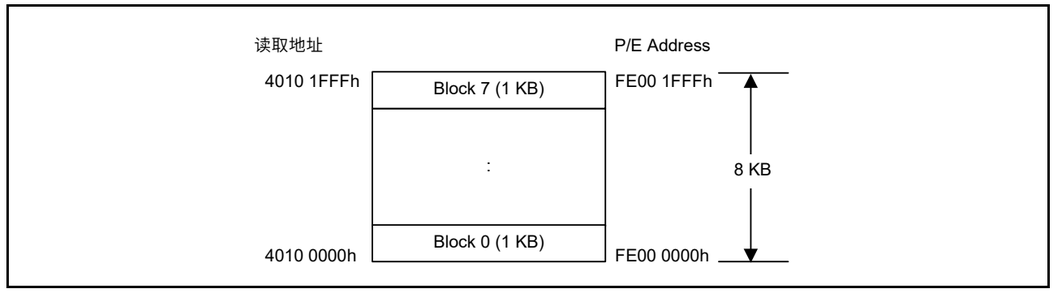


Figure 43.3 数据闪存的映射

Table 43.3 数据闪存的读取和PE地址

数据闪存大小	读取地址	P/E address	块数
8 KB	4010 0000h to 4010 1FFFh	FE00 0000h to FE00 1FFFh	0 to 7

43.3 闪存缓存

43.3.1 Overview

闪存高速缓存(FCACHE)加快了从总线主机到闪存的读取访问。FCACHE包括：

- FCACHE1，用于CPU取指
- FCACHE2，用于CPU操作数访问和DMA
- FLPF，用于CPU取指的预取访问。

Table 43.4 闪存缓存概述

Parameter	闪存缓存1(FCACHE1)	闪存缓存2(FCACHE2)	Prefetch buffer (FLPF)
缓存目标区域	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
目标总线主机	CPU指令获取	CPU操作数访问和非CPU访问	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2路组关联	完全关联	-
	• 64 bits/entry (64-bit aligned data) • 8 entries/ways.	64位条目（64位对齐数据） 1个条目。	64位条目（64位对齐数据） 2个条目 上一个CPU指令的下一个地址。
访问周期	缓存命中：0等待 缓存未命中：根据SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT=1：1或2次等待	缓存命中：0等待 缓存未命中：根据SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT=1：1或2次等待	缓存命中：0等待 缓存未命中：根据SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT=1：1或2次等待

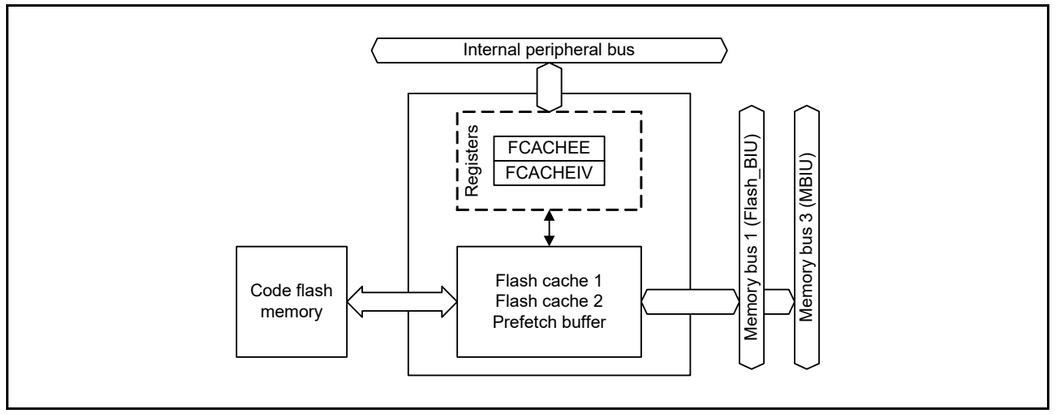


Figure 43.4 FCACHE block diagram

43.3.2 Register Descriptions

43.3.2.1 Flash Cache Enable Register (FCACHEE)

Address(es): FCACHE.FCACHEE 4001 C100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FCACHEEN	FCACHE Enable	0: Disable FCACHE 1: Enable FCACHE.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FCACHEE.FCACHEEN bit enables or disables the flash cache function for FCACHE1, FCACHE2, and FLPF. This bit does not affect FCACHEIV.FCACHEIV. When FCACHE is enabled, the HPROT[3] bit setting determines whether it is cacheable or non-cacheable. See section 15.5, Notes on using Flash Cache.

43.3.2.2 Flash Cache Invalidate Register (FCACHEIV)

Address(es): FCACHE.FCACHEIV 4001 C104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FCACHEIV	Flash Cache Invalidate	• Reads: 0: Do not invalidate 1: Invalidate. • Writes: When the write value is 1, FCACHE is invalidated. When the write value is 0, this setting is ignored.	R/W

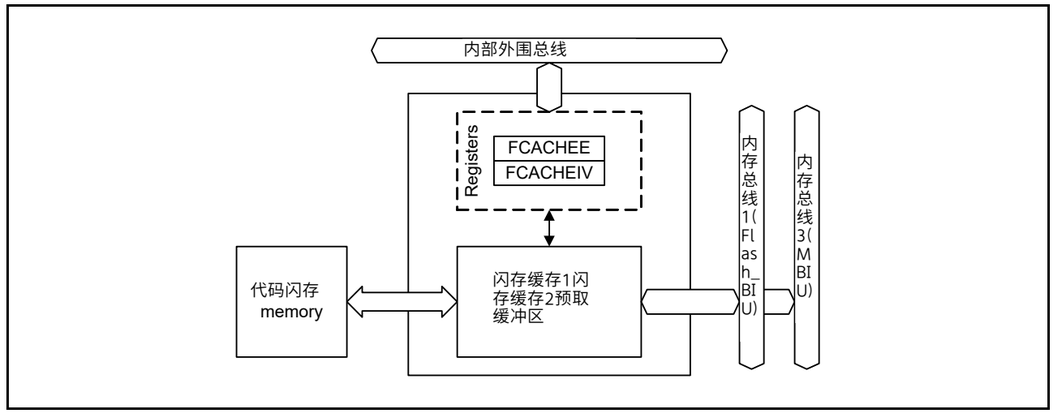


Figure 43.4 FCACHE框图

43.3.2 注册说明

43.3.2.1 闪存缓存启用寄存器(FCACHEE)

Address(es): FCACHE.FCACHEE 4001 C100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FCACHEEN	FCACHE Enable	0：禁用FCACHE1： 启用FCACHE。	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FCACHEE.FCACHEEN位启用或禁用FCACHE1、FCACHE2和FLPF的闪存缓存功能。该位不影响FCACHEIV.FCACHEIV。当启用FCACHE时，HPROT[3]位设置确定它是可缓存的还是不可缓存的。请参阅第15.5节，使用FlashCache的注意事项。

43.3.2.2 闪存缓存无效寄存器(FCACHEIV)

Address(es): FCACHE.FCACHEIV 4001 C104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FCACHEIV	闪存缓存失效	读取：0：不无效1：无效。 写入：当写入值为1时，FCACHE无效。当写入值为0时，忽略此设置。	R/W

Bit	Symbol	Bit name	Description	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

When 1 is written to the FCACHEIV.FCACHEIV bit, flash cache data in FCACHE1, FCACHE2, and FLPF is invalidated.

43.3.2.3 Data Flash Control Resister (DFLCTL)

Address(es): FLCN.DFLCTL 407E C090h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DFLEN	Data Flash Access Enable	0: Access to the data flash is disabled 1: Access to the data flash is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DFLCTL register is to enable or disable accessing (reading, programming, and erasing) of the data flash. After setting the DFLCTL.DFLEN bit, Data Flash STOP recovery time (t_{DSTOP}) is nccessary before reading the data flash or entering the data flash P/E mode.

The time setup takes differs for each operating mode.

<Setup time for each operating mode>

- HS (High-speed) mode: 5 µs
- LS (Low-speed) mode: 720 ns
- LP (Low-power) mode: 720 ns
- LV (Low-voltage) mode: 10 µs

43.4 Operation

Use the FCACHEE register to set up and enable flash operation. To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Set the MEMWAIT.MEMWAIT bit as required for the ICLK frequency and power control mode set in the OPCCR and SOPCCR registers.
3. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
4. Check that FCACHEIV.FCACHEIV is 0.
5. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note: Do not change operation mode (read mode, wait mode) when the flash cache is enabled.
Note 1. It is not necessary to disable the flash cache on the first setup after reset.

43.4.1 Notice to use Flash Cache

When using flash cache by access from the CPU, Arm® MPU should also be set to be cacheable.

See the *ARM®v7-M Architecture Reference Manual* and the *ARM® Cortex®-M4 Devices Generic User Guide.*

Bit	Symbol	位名称	Description	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当FCACHEIV.FCACHEIV位写入1时，FCACHE1、FCACHE2和FLPF中的闪存缓存数据无效。

43.3.2.3 数据闪存控制电阻(DFLCTL)

Address(es): FLCN.DFLCTL 407E C090h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DFLEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DFLEN	数据闪存访问使能	0：禁止访问数据闪存1：允许访问数据闪存	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DFLCTL寄存器用于启用或禁用对数据闪存的访问（读取、编程和擦除）。设置DFLCTL.DFLEN位后，在读取数据闪存或进入数据闪存PE模式之前，数据闪存停止恢复时间(tDSTOP)是必需的。

每种操作模式所需的时间设置不同。

<每种操作模式的设置时间>

- HS (High-speed) mode: 5 µs
- LS (Low-speed) mode: 720 ns
- LP (Low-power) mode: 720 ns
- LV (Low-voltage) mode: 10 µs

43.4 Operation

使用FCACHEE寄存器设置和启用闪存操作。设置闪存缓存并准备重写闪存：

1. 通过重置FCACHEE.FCACHEEN禁用闪存缓存。*1
2. 根据OPCCR和SOPCCR寄存器中设置的ICLK频率和功率控制模式的需要设置MEMWAIT.MEMWAIT位。
3. 通过设置FCACHEIV.FCACHEIV使闪存缓存无效。
4. 检查FCACHEIV.FCACHEIV是否为0。
5. 通过设置FCACHEE.FCACHEEN启用闪存缓存。

Note: 启用闪存缓存时，请勿更改操作模式（读取模式、等待模式）。
注1.复位后第一次设置时无需禁用闪存缓存。

43.4.1 使用FlashCache的注意事项

当通过CPU访问使用闪存缓存时，Arm®MPU也应设置为可缓存。

请参阅ARM®v7-M架构参考手册和ARM®Cortex®-M4设备通用用户指南。

43.5 Operating Modes Associated with the Flash Memory

Figure 43.5 shows a diagram of the mode transitions associated with the flash memory. For information on setting up the modes, see section 3, Operating Modes.

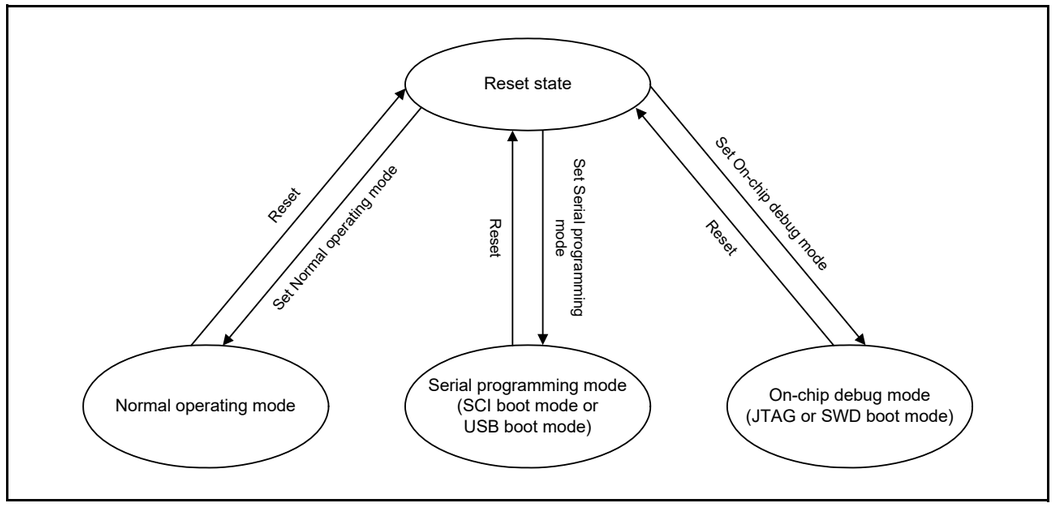


Figure 43.5 Mode transitions associated with flash memory

The flash memory areas where programming and erasure are permitted, and where the boot program executes at a reset, differ with mode. Table 43.5 shows the differences between the modes.

Table 43.5 Difference between modes

Parameter	Normal operating mode	Serial programming mode (SCI or USB boot mode)	On-chip debug mode (JTAG or SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory.	• Code flash memory • Data flash memory.	• Code flash memory • Data flash memory.
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

43.5.1 ID Code Protection

The ID code protection function prohibits programming and on-chip debugging. When ID code protection is enabled, the device validates or invalidates the ID code sent from the host by comparing it with the ID code stored in the flash memory. Programming and on-chip debugging are enabled only when the two match.

The ID code in flash memory consists of four 32-bit words. ID code bits [127] and [126] determine whether ID code protection is enabled and the authentication method to use with the host. Table 43.6 shows how the ID code determines the authentication method.

43.5 与闪存相关的操作模式

图43.5显示了与闪存相关的模式转换图。有关设置模式的信息，请参阅第3节，操作模式。

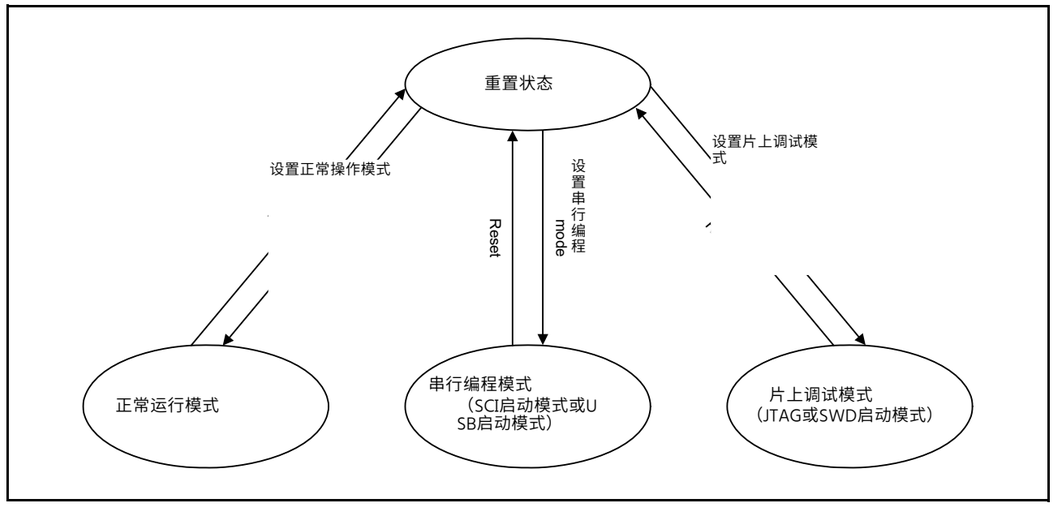


Figure 43.5 与闪存相关的模式转换

允许编程和擦除的闪存区域以及在复位时执行引导程序的区域因模式而异。表43.5显示了这些模式之间的差异。

Table 43.5 模式之间的差异

Parameter	正常运行模式	串行编程模式（SCI或USB启动模式）	片上调试模式（JTAG或SWD引导模式）
可编程和可擦除区域	代码闪存 数据闪存。	代码闪存 数据闪存。	代码闪存 数据闪存。
以块为单位擦除	Possible	Possible	Possible
复位时的引导程序	用户区程序	用于串行编程的嵌入式程序	取决于调试命令

43.5.1 ID码保护

ID码保护功能禁止编程和片上调试。启用ID代码保护时，设备通过将主机发送的ID代码与存储在闪存中的ID代码进行比较来使该ID代码有效或无效。编程和片上调试仅在两者匹配时才启用。

闪存中的ID代码由四个32位字组成。ID代码位[127]和[126]确定是否启用ID代码保护以及与主机一起使用的身份验证方法。表43.6显示了ID代码如何确定身份验证方法。

Table 43.6 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/USB boot mode) On-chip debug mode (JTAG/SWD boot mode)	FFh, …, FFh (all bytes are FFh)	Protection disabled	ID code validation is not performed, the ID code always matches, and connection to the programmer or the on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of all 16 bytes is not FFh	Protection enabled	Matching ID code: Authentication ends and connection with the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents in the user flash (code and data) area, and the configuration area are erased. However, forced erasure is not performed when the FSPR bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection with the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited.

43.6 Overview of Functions

By using a dedicated flash-memory programmer to program the on-chip flash memory through a serial interface (serial programming mode) or through JTAG/SWD interface (on-chip debug mode), the device can be programmed before or after it is mounted on the target system. Additionally, security functions to prohibit overwriting of the user program prevent tampering by third parties.

Programming by the user program (self-programming) is available for applications that might require updating after system manufacturing or shipment. Protection features for safely overwriting the flash memory area are also provided. Additionally, interrupt processing during self-programming is supported so that programming can continue while processing external communications and other functions. Table 43.7 lists the programming methods and the associated operating modes.

Table 43.7 Programming methods (1 of 2)

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer connected through the SCI or USBFS interface can program the on-board flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer connected through the SCI or USBFS interface and a dedicated programming adapter board allow off-board programming of the flash memory, before it is mounted on the target system.	
Self-programming	A user program written to memory in advance of serial programming execution is also capable of programming the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from code flash memory while the data flash memory is programmed. As a result, a program resident in code flash memory is able to program data flash memory.	Normal operating mode

Table 43.6 ID码保护规范

启动时的操作模式	身份证号码	保护状态	与编程器或片上调试器连接的操作
串行编程模式（SCIUSB启动模式） 片上调试模式（JTAGSWD引导模式）	FFh … FFh（所有字节均为FFh）	保护已禁用	不执行ID代码验证，ID代码始终匹配，并且允许连接到编程器或片上调试器。
	位[127]=1，位[126]=1，并且所有16个字节中至少有一个不是FFh	启用保护	匹配ID码：认证结束，允许与编程器或片上调试器连接。不匹配的ID代码：额外转换到ID代码保护等待状态。当编程器或片上调试器发送的ID码为ASCII码（414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh）的ALeRASE时，用户闪存（代码和数据）区和配置区的内容被擦除。但是，当FSPR位为0时，不执行强制擦除。
	位[127]=1和位[126]=0	启用保护	匹配ID码：认证结束，允许与编程器或片上调试器连接。不匹配的ID代码：额外转换到ID代码保护等待状态。
	Bit [127] = 0	启用保护	不执行ID代码验证，ID代码总是不匹配，并且禁止连接到编程器或片上调试器。

43.6 功能概述

通过使用专用闪存编程器通过串行接口（串行编程模式）或通过JTAGSWD接口（片上调试模式）对片上闪存进行编程，可以在器件安装之前或之后对其进行编程目标系统。此外，禁止覆盖用户程序的安全功能可防止第三方篡改。

用户程序编程（自编程）可用于在系统制造或发货后可能需要更新的应用程序。还提供了用于安全覆盖闪存区域的保护功能。此外，支持自编程期间的中断处理，以便在处理外部通信和其他功能的同时继续编程。表43.7列出了编程方法和相关的操作模式。

Table 43.7 编程方法(1of2)

编程方法	功能概览	操作模式
串行编程	通过SCI连接的专用闪存编程器或USBFS接口可以在设备挂载到目标系统后对板载闪存进行编程。	串行编程模式
	通过SCI或USBFS接口连接的专用闪存编程器和专用编程适配器板允许在将闪存安装到目标系统之前对其进行板外编程。	
Self-programming	在串行编程执行之前写入存储器的用户程序也能够对闪存进行编程。后台操作能力使得在对数据闪存进行编程时，可以从代码闪存中获取指令或以其他方式读取数据。因此，驻留在代码闪存中的程序能够对数据闪存进行编程。	正常运行模式

Table 43.7 Programming methods (2 of 2)

Programming method	Functional overview	Operating mode
JTAG or SWD programming	A dedicated flash-memory programmer or an on-chip debugger connected through JTAG/SWD can program the on-board flash memory after the device is mounted on the target system.	On-chip debug mode
	A dedicated flash-memory programmer or an on-chip debugger connected through JTAG/SWD and a dedicated programming adapter board allow off-board programming of the flash memory, before it is mounted on the target system.	

The MCU supports programming commands for self-programming. Table 43.8 lists the functions of the on-chip flash memory. Use serial programmer commands for serial programming. For self-programming, use the programming commands to read the on-chip flash memory or run the user program.

Table 43.8 Basic functions

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing is written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not proceeded after erasure.	Not supported	Supported
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
Read	Reads data programmed in the flash memory	Supported	Not supported (read by user program is possible)
ID code check	Compares the ID code sent by the host with the code stored in the ROM. If the two match, the FCB enters the wait state for programming and erasure commands from the host.	Supported	Not supported (ID authentication is not performed)
Security configuration	Configures the security function for serial programming	Supported with conditions (only allows switching from enabled to disabled)	Supported with conditions (only allows switching from enabled to disabled)
Protection configuration	Configures the access window for flash area protection in the code flash memory	Supported	Supported

The on-chip flash memory supports the ID code security function. Authentication of ID codes is a security function for use with serial programming and with JTAG or SWD programming. Table 43.9 lists the security functions supported by the on-chip flash memory, and Table 43.10 lists the available operations and security settings.

Table 43.9 Security functions

Function	Description
ID authentication	The result of ID authentication can be used to control the connection of a serial programmer for serial programming

Table 43.7 编程方法（2之2）

编程方法	功能概览	操作模式
JTAG或SWD编程	通过JTAGSWD连接的专用闪存编程器或片上调试器可以在器件安装到目标系统后对板载闪存进行编程。	片上调试模式
	通过JTAGSWD和专用编程适配器板连接的专用闪存编程器或片上调试器允许在将闪存安装到目标系统之前对其进行板外编程。	

MCU支持自编程的编程命令。表43.8列出了片上闪存的功能。使用串行编程器命令进行串行编程。对于自编程，使用编程命令读取片上闪存或运行用户程序。

Table 43.8 基本功能

Function	功能概览	Availability	
		串行编程	Self-programming
空白支票	检查指定的块以确保尚未对其进行写入。无法保证从擦除后没有写入任何内容的数据闪存中读取的结果，因此使用空白检查来确认擦除后没有继续写入内存。	不支持	Supported
块擦除	擦除指定块中的内存内容	Supported	Supported
Programming	写入指定地址	Supported	Supported
Read	读取闪存中编程的数据	Supported	不支持（可由用户程序读取）
识别码检查	将主机发送的ID代码与存储在ROM中的代码进行比较。如果两者匹配，则FCB进入等待状态，等待来自主机的编程和擦除命令。	Supported	不支持（不进行身份验证）
安全配置	配置串行编程的安全功能	有条件支持（只允许从启用切换到禁用）	有条件支持（只允许从启用切换到禁用）
保护配置	配置代码闪存中闪存区域保护的访问窗口	Supported	Supported

片上闪存支持ID码安全功能。ID代码验证是一种安全功能，可用于串行编程和JTAG或SWD编程。表43.9列出了片上闪存支持的安全功能，表43.10列出了可用的操作和安全设置。

Table 43.9 安全功能

Function	Description
身份认证	ID认证的结果可以用来控制串口编程器的连接进行串口编程

Table 43.10 Available operations and security settings

Function	All security settings and erasure, programming, and read operations		Constraints on the security setting configuration
	Serial programming and on-chip debug mode	Self-programming mode	Self-programming mode
ID authentication	When ID codes do not match: • Block erasure commands: not supported • Programming commands: not supported • Read commands: not supported • Security configuration commands: not supported • Protection configuration commands: not supported When the ID codes match: • Block erasure commands: supported • Programming commands: supported • Read commands: supported • Security configuration commands: supported • Protection configuration commands: supported	• ID authentication is not performed • Blank check: supported • Block erasure: supported • Programming: supported • Security configuration: supported • Protection configuration: supported.	ID authentication is not performed

43.6.1 Configuration Area Bit Map

The bits used for ID authentication, startup area select, access window protection, and security configuration functions are mapped in Figure 43.6. The boot program must use these bits as hexadecimal data.

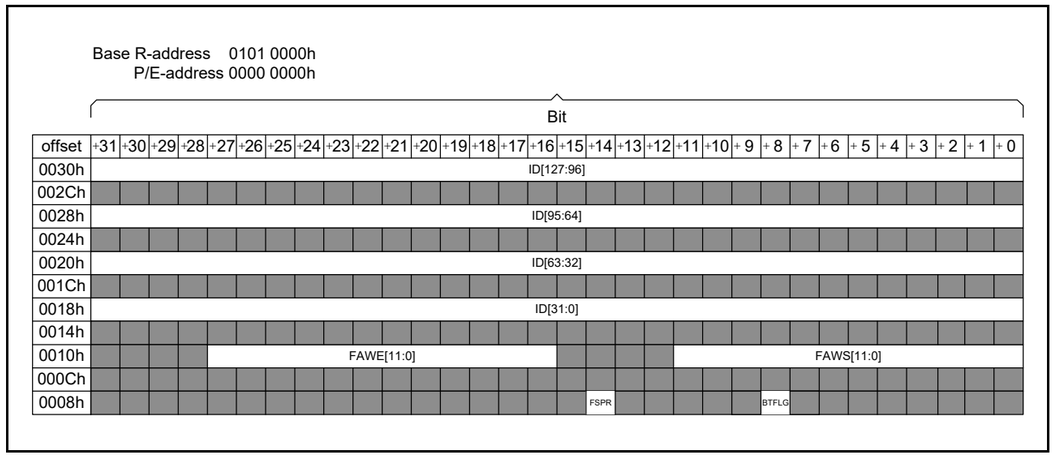


Figure 43.6 Configuration area bit map

43.6.2 Startup Area Select

The startup area select function allows the boot program to be safely updated. The startup area is 8 KB of space located in the user area. The FCB controls the startup area address based on the Startup Area Select Flag (BTFLG) that is located in the AWSC register. The startup area can be locked by the FSPR bit.

Figure 43.7 shows an overview of the startup program protection.

Table 43.10 可用的操作和安全设置

Function	所有安全设置和擦除、编程和读取操作		安全设置配置的约束
	串行编程和片上调试模式	Self-programming mode	Self-programming mode
身份认证	当ID代码不匹配时： 块擦除命令：不支持 编程命令：不支持 读取命令：不支持 安全配置命令：不支持 保护配置命令：不支持ID代码匹配时： 块擦除命令：支持 编程：支持 编程命令：支持 读取命令：支持 安全配置命令：支持 保护配置命令：支持	不执行ID身份验证 空白检查：支持 块擦除：支持 安全配置：支持 保护配置：支持。	不进行身份验证

43.6.1 配置区位图

用于身份验证、启动区域选择、访问窗口保护和安全配置功能的位映射在图43.6中。引导程序必须使用这些位作为十六进制数据。

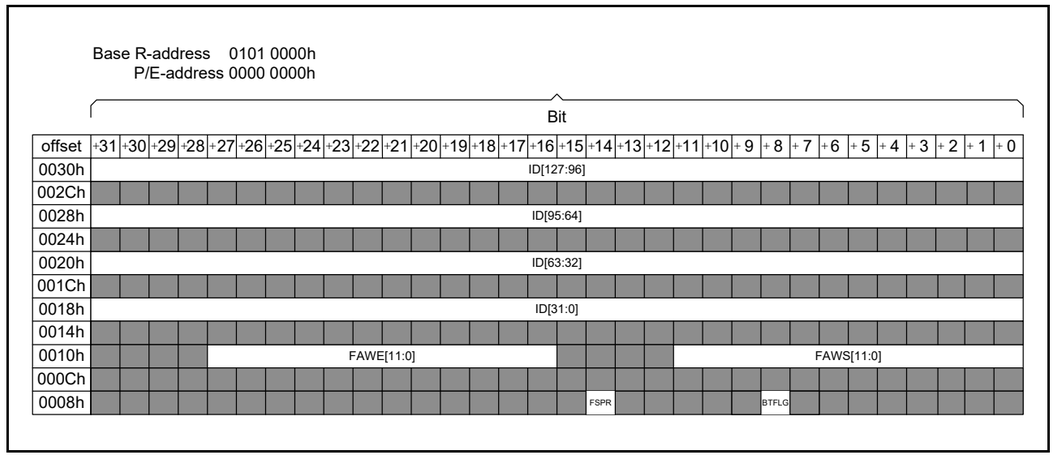
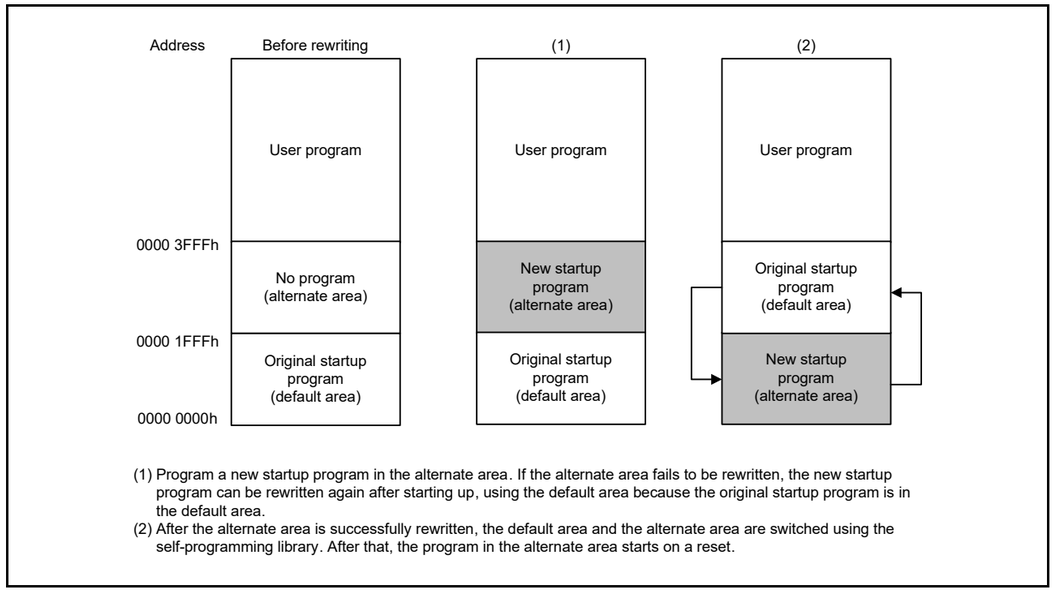


Figure 43.6 配置区位图

43.6.2 启动区域选择

启动区域选择功能允许安全更新引导程序。启动区是位于用户区的8KB空间。FCB根据位于AWSC寄存器中的启动区域选择标志(BTFLG)控制启动区域地址。启动区域可以通过FSPR位锁定。

图43.7显示了启动程序保护的概述。



(1) Program a new startup program in the alternate area. If the alternate area fails to be rewritten, the new startup program can be rewritten again after starting up, using the default area because the original startup program is in the default area.
(2) After the alternate area is successfully rewritten, the default area and the alternate area are switched using the self-programming library. After that, the program in the alternate area starts on a reset.

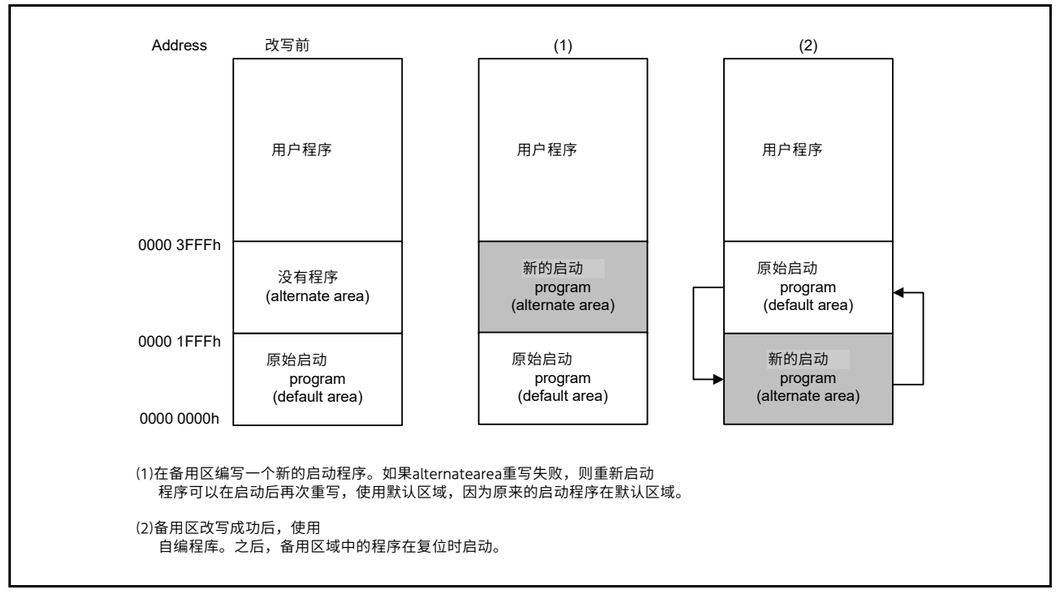
Figure 43.7 Overview of startup program protection

43.6.3 Protection by Access Window

Issuing the program or block erase command to a flash memory area outside of the access window results in the command-locked state. The access window is only valid in the user area of the code flash memory. The access window provides protection in self-programming, serial programming, and on-chip debug modes. Figure 43.8 shows the flash area protection.

The access window is specified in both the FAWS[11:0] and FAWE[11:0] bits. Setting of the FAWE[11:0] and FAWS[11:0] bits in various conditions is described as follows:

- FAWE[11:0] = FAWS[11:0]: The P/E command can execute anywhere in the user area of the code flash memory.
- FAWE[11:0] > FAWS[11:0]: The P/E command can only execute in the window from the block pointed to by the FAWS[11:0] bits to one block lower than the block pointed to by the FAWE[11:0] bits.
- FAWE[11:0] < FAWS[11:0]: The P/E command cannot execute anywhere in the user area of the code flash memory.



(1)在备用区编写一个新的启动程序。如果alternatearea重写失败，则重新启动
程序可以在启动后再次重写，使用默认区域，因为原来的启动程序在默认区域。

(2)备用区改写成功后，使用
自编程库。之后，备用区域中的程序在复位时启动。

Figure 43.7 启动程序保护概述

43.6.3 通过访问窗口保护

向访问窗口之外的闪存区域发出程序或块擦除命令会导致命令锁定状态。访问窗口仅在代码闪存的用户区有效。访问窗口在自编程、串行编程和片上调试模式下提供保护。图43.8显示了闪存区域保护。

访问窗口在FAWS[11:0]和FAWE[11:0]位中指定。FAWE[11:0]的设置和
各种条件下的FAWS[11:0]位描述如下：

- FAWE[11:0]=FAWS[11:0]：PE命令可以在代码闪存用户区的任何地方执行。
- FAWE[11:0]>FAWS[11:0]：PE命令只能在窗口中执行
FAWS[11:0]位比FAWE[11:0]位指向的块低一个块。
- FAWE[11:0]<FAWS[11:0]：PE命令不能在代码闪存用户区的任何地方执行。

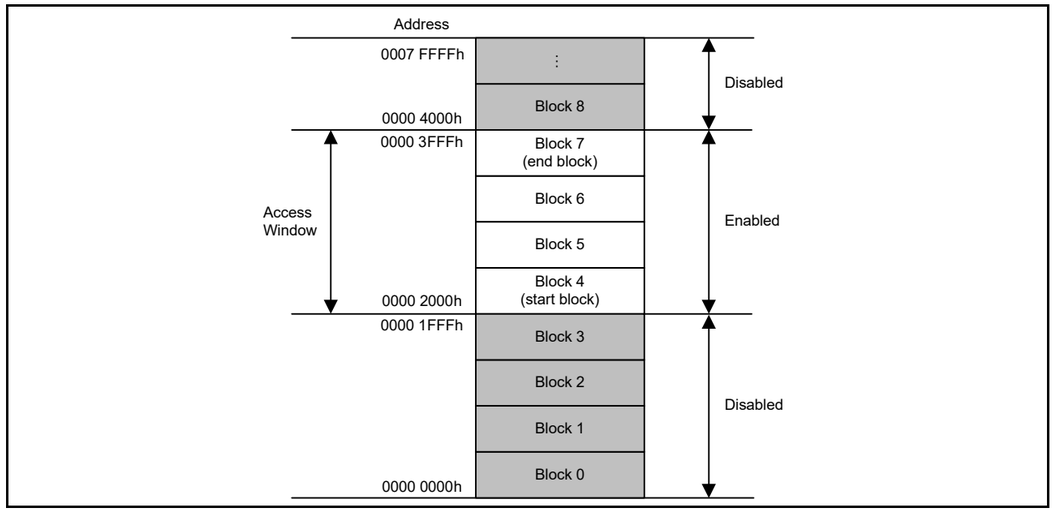


Figure 43.8 Flash area protection overview

43.7 Programming Commands

The FCB controls the programming commands.

43.8 Suspend Operation

The forced stop command forces the blank check command or the block erase command to stop. When a forced stop is executed, the stopped address values are stored in the registers. The command can restart from the stopped address after resetting the registers for command execution by copying the saved addresses.

43.9 Protection

The types of protection provided include:

- Software protection
- Error protection
- Boot program protection.

43.10 Serial Programming Mode

The serial programming modes include:

- Boot mode with SCI9
- USB boot mode with the USBFS.

Table 43.11 lists the I/O pins of the flash memory-related modules.

Table 43.11 I/O pins of flash memory-related modules (1 of 2)

Pin name	I/O	Applicable modes	Function
MD	Input	SCI boot mode USB boot mode (serial programming mode)	Selection of operating mode
P110/RXD9	Input	SCI boot mode	For host communication, to receive data through SCI
P109/TXD9	Output		For host communication, to transmit data through SCI

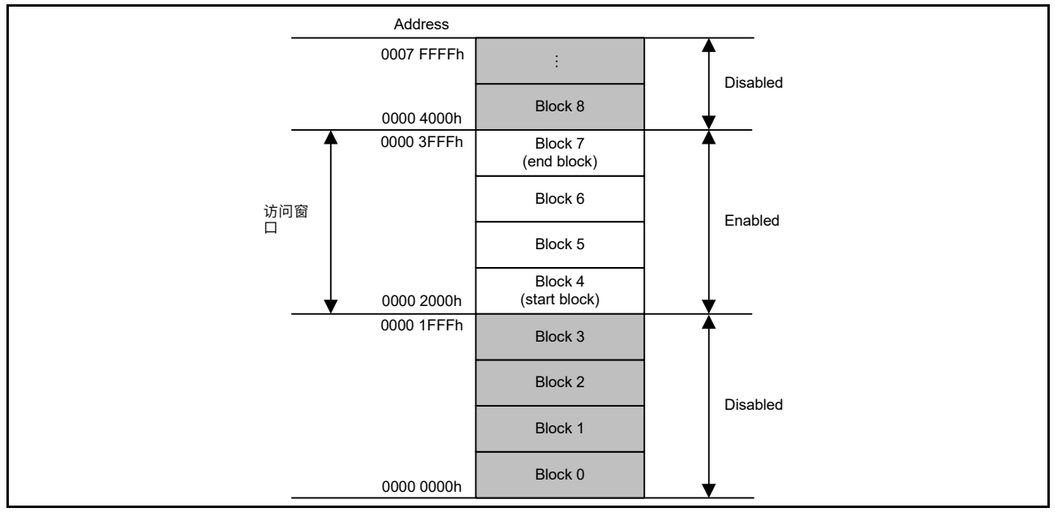


Figure 43.8 闪存区域保护概述

43.7 编程命令

FCB控制编程命令。

43.8 暂停操作

强制停止命令强制空白检查命令或块擦除命令停止。当执行强制停止时，停止的地址值存储在寄存器中。通过复制保存的地址，可以在重置用于命令执行的寄存器后，从停止的地址重新启动命令。

43.9 Protection

提供的保护类型包括：

- 软件保护
- 错误保护
- 引导程序保护。

43.10 串行编程模式

串行编程模式包括：

- 带有SCI9的引导模式
- USB引导模式与USBFS。

表43.11列出了闪存相关模块的IO引脚。

Table 43.11 闪存相关模块的IO管脚(1of2)

引脚名称	I/O	适用模式	Function
MD	Input	SCI启动模式USB启动模式 （串行编程模式）	操作模式的选择
P110/RXD9	Input	SCI开机模式	用于主机通信，通过SCI接收数据
P109/TXD9	Output		用于主机通信，通过SCI传输数据

Table 43.11 I/O pins of flash memory-related modules (2 of 2)

Pin name	I/O	Applicable modes	Function
USB_DP, USB_DM	I/O	USB boot mode	USB data I/O
USB_VBUS	Input		Detection of connection and disconnection of USB cables

Note: Serial programming mode is not executed when security MPU is enabled.

43.10.1 SCI Boot Mode

In boot mode, the host sends control commands and data for programming, and the code flash memory and data flash memory areas are programmed or erased accordingly. An on-chip SCI handles transfers between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When the MCU is activated in boot mode, the embedded program for serial programming is executed. This program automatically adjusts the bit rate of the SCI and controls programming and erasure by receiving control commands from the host. The USB cable must not be connected on reset release.

Figure 43.9 shows the system configuration for operations in boot mode.

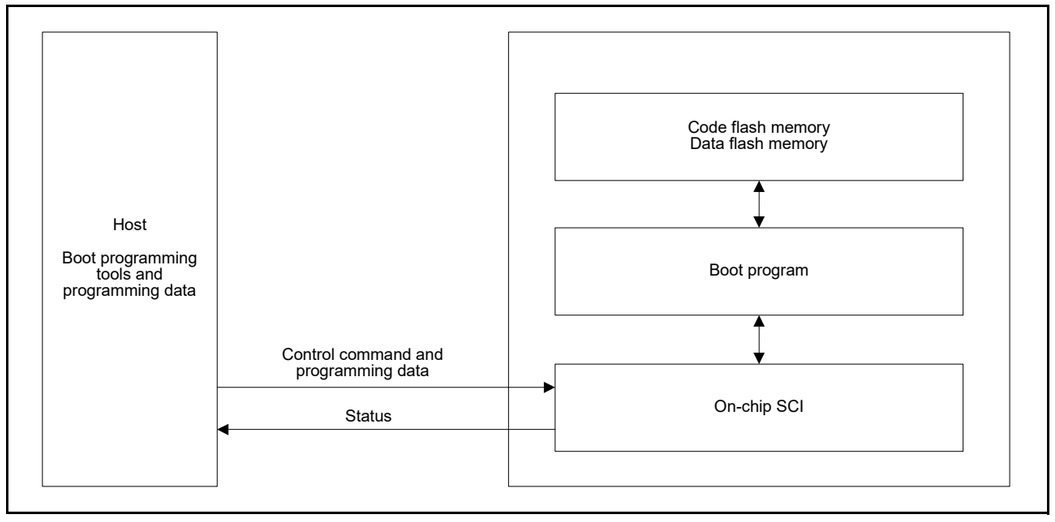


Figure 43.9 System configuration in SCI boot mode

43.10.2 USB Boot Mode

In USB boot mode, the code and data flash memory are programmed or erased by control commands and data for programming transmitted from an externally connected host through the USB interface.

Using USB boot mode requires preparation on the host side of the tools for transmitting control commands and data for programming. Figure 43.10 shows the configuration of a system in USB boot mode. The USB cable must be connected on reset release.

For a USB self-powered system, the total current consumption from VBUS should not exceed 100 mA.

Table 43.11 闪存相关模块的IO管脚(2of2)

引脚名称	I/O	适用模式	Function
USB_DP, USB_DM	I/O	USB启动模式	USB数据输入输出
USB_VBUS	Input		检测USB电缆的连接和断开

Note: 启用安全MPU时不执行串行编程模式。

43.10.1 SCI启动模式

在引导模式下，主机发送控制命令和数据进行编程，代码闪存和数据闪存区域被相应地编程或擦除。片上SCI以异步模式处理主机和MCU之间的传输。主机中必须准备好用于传输控制命令和编程数据的工具。

当MCU在引导模式下激活时，将执行用于串行编程的嵌入式程序。该程序通过接收来自主机的控制命令自动调整SCI的比特率并控制编程和擦除。复位释放时不得连接USB电缆。

图43.9显示了引导模式下操作的系统配置。

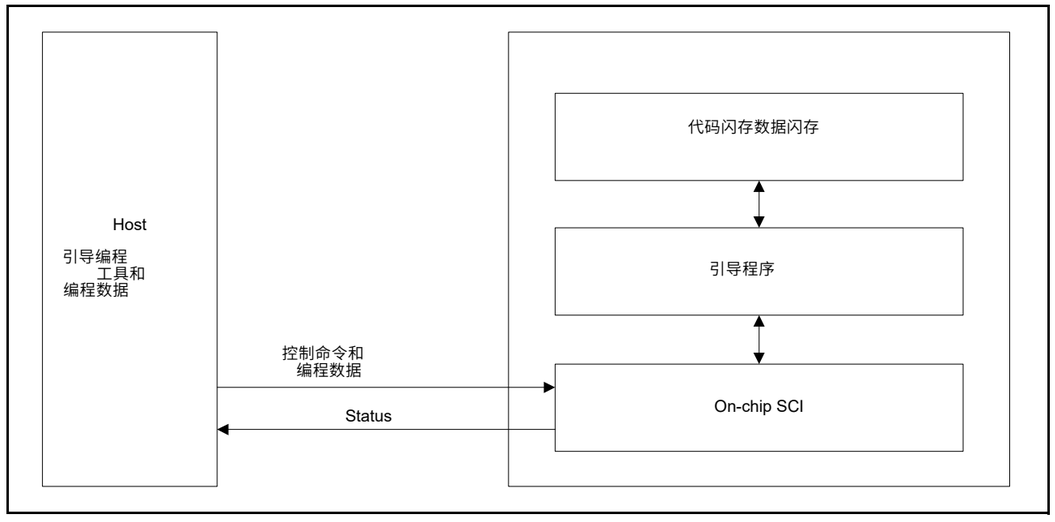


Figure 43.9 SCI引导模式下的系统配置

43.10.2 USB启动模式

在USB引导模式下，代码和数据闪存通过USB接口从外部连接的主机传输的控制命令和用于编程的数据进行编程或擦除。

使用USB启动模式需要在主机端准备用于传输控制命令和数据以进行编程的工具。图43.10显示了USB引导模式下的系统配置。USB电缆必须在复位释放时连接。

对于USB自供电系统，来自VBUS的总电流消耗不应超过100mA。

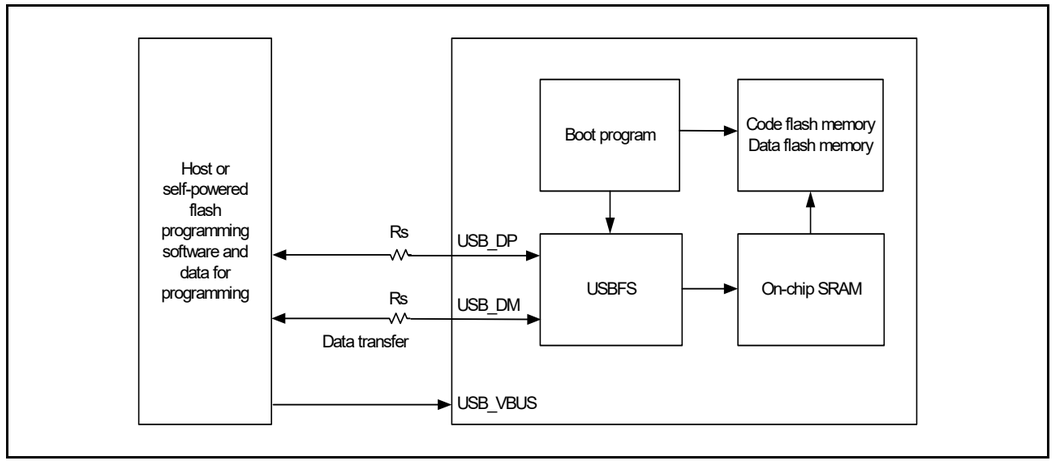


Figure 43.10 System configuration in USB boot mode

43.11 Using a Serial Programmer

A dedicated flash memory programmer can be used to program the flash memory in serial programming mode.

43.11.1 Serial Programming

The MCU is mounted on the system board for serial programming. A connector to the board allows programming by the flash memory programmer.

43.11.2 Programming Environment

Figure 43.11 shows the environment recommended by Renesas for programming the flash memory of the MCU with data.

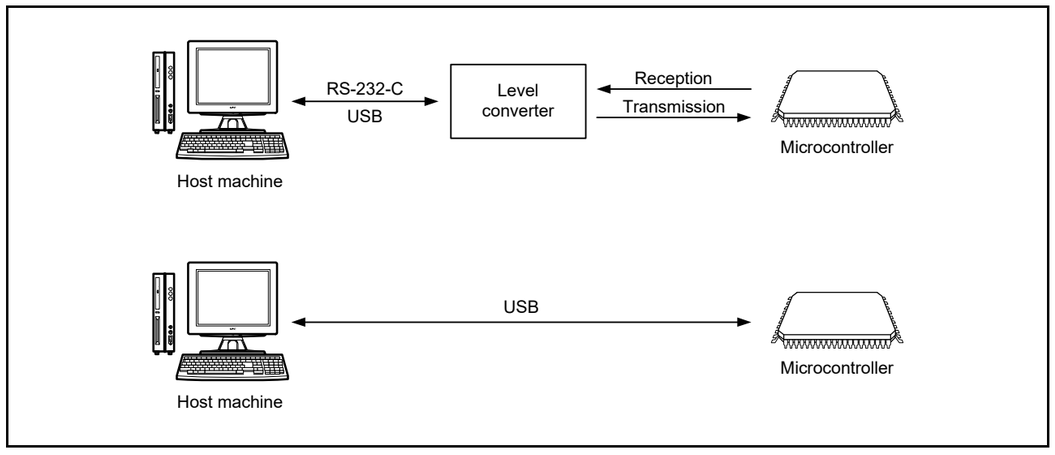


Figure 43.11 Environment for writing programs to the flash memory

43.12 Self-Programming

43.12.1 Overview

The MCU supports programming of the flash memory by the user program. The programming commands can be used

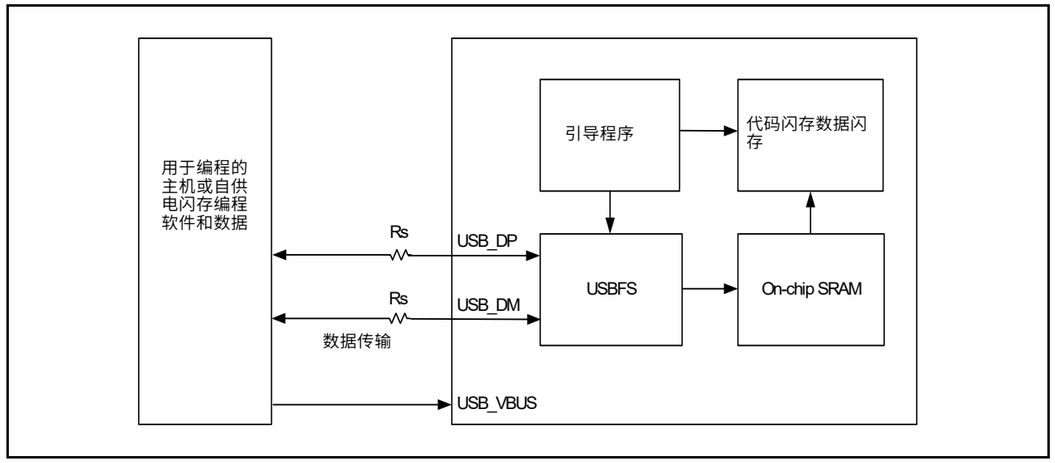


Figure 43.10 USB引导模式下的系统配置

43.11 使用串行编程器

可以使用专用的闪存编程器在串行编程模式下对闪存进行编程。

43.11.1 串行编程

MCU安装在系统板上，用于串行编程。板上的连接器允许闪存编程器进行编程。

43.11.2 编程环境

图43.11显示了瑞萨推荐的使用数据对MCU闪存进行编程的环境。

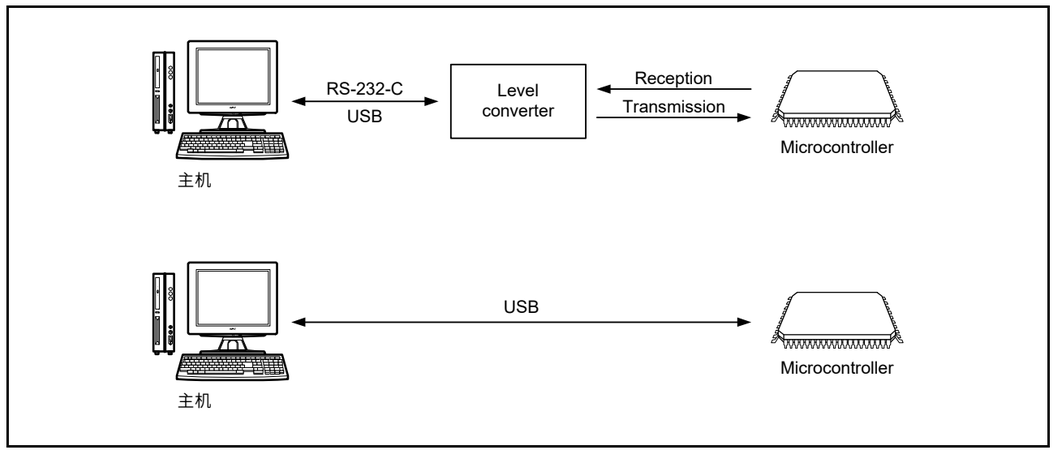


Figure 43.11 将程序写入闪存的环境

43.12 Self-Programming

43.12.1 Overview

MCU支持通过用户程序对闪存进行编程。可以使用编程命令

with user programs for writing to the code and data flash memory. This enables updates to the user programs and overwriting of constant data fields.

The background operation facility makes it possible to execute a program from the code flash memory to program the data flash memory under the conditions shown in Table 43.12. This program can also be copied in advance to and executed from the internal SRAM. When executing from the internal SRAM, this program can also program the code flash memory area.

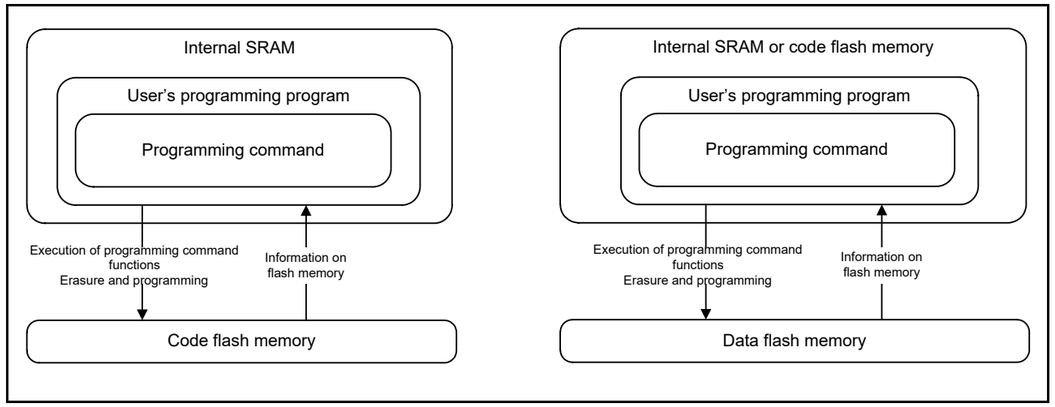


Figure 43.12 Schematic view of self-programming

43.12.2 Background Operation

Background operation can be used when a combination of the flash memory for writing and reading is as listed in Table 43.12.

Table 43.12 Conditions under which background operation is available

Product	Writable range	Readable range
All products	Data flash memory	Code flash memory

43.13 Reading the Flash Memory

43.13.1 Reading the Code Flash Memory

No special settings are required to read the code flash memory in Normal mode. Data can be read by accessing addresses in the code flash memory. When reading code flash memory that is erased but not yet reprogrammed, such as code flash memory in the non-programmed state, all bits are read as 1s.

43.13.2 Reading the Data Flash Memory

No special settings are required to read the data flash memory in Normal mode except when issuing a reset that causes the data flash access disable mode to disable reading. In this case, the application must transfer back to the data flash read mode. When reading data flash memory that is erased but not yet reprogrammed, such as data flash memory in the non-programmed state, all bits are read as 1s.

43.14 Usage Notes

43.14.1 Erase Suspended Area

Data in areas where an erase operation is suspended is undefined. To avoid malfunctions caused by reading undefined data, do not execute commands and read data in the area where erase operation is suspended.

与用于写入代码和数据闪存的用户程序。这可以更新用户程序和覆盖常量数据字段。

后台操作工具可以在表43.12所示的条件下从代码闪存执行程序以对数据闪存进行编程。该程序也可以预先复制到内部SRAM中并从内部SRAM中执行。当从内部SRAM执行时，该程序还可以对代码闪存区域进行编程。

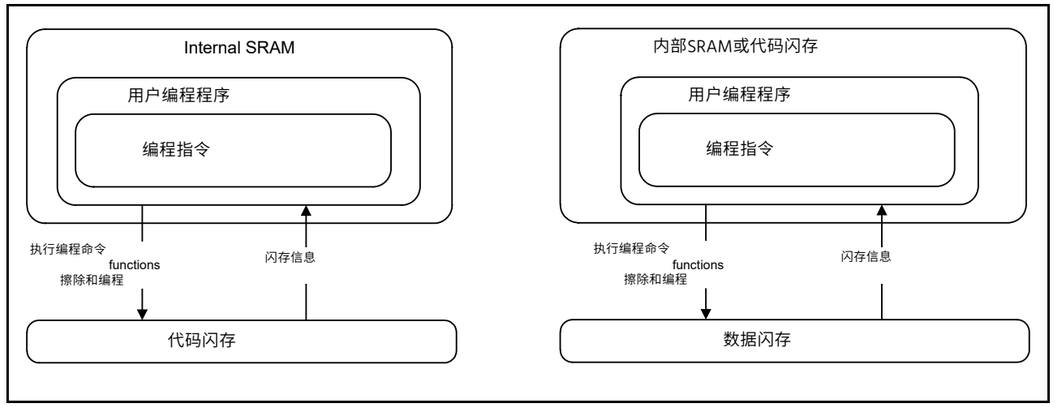


Figure 43.12 自编程示意图

43.12.2 后台操作

当用于写入和读取的闪存组合如表43.12中所列时，可以使用后台操作。

Table 43.12 后台操作可用的条件

Product	Writable range	可读范围
所有产品	数据闪存	代码闪存

43.13 读取闪存

43.13.1 读取代码闪存

在正常模式下读取代码闪存不需要特殊设置。可以通过访问代码闪存中的地址来读取数据。当读取已擦除但尚未重新编程的代码闪存时，例如处于未编程状态的代码闪存，所有位都被读取为1。

43.13.2 读取数据闪存

在正常模式下读取数据闪存不需要特殊设置，除非发出导致数据闪存访问禁用模式禁用读取的复位。在这种情况下，应用程序必须转回数据闪存读取模式。在读取已擦除但尚未重新编程的数据闪存时，例如处于未编程状态的数据闪存，所有位都被读取为1。

43.14 使用说明

43.14.1 擦除暂停区域

擦除操作暂停的区域中的数据未定义。为避免读取未定义数据引起故障，请勿在擦除操作暂停的区域执行命令和读取数据。

43.14.2 Suspension by Erase Suspend Commands

When suspending an erase operation with the erase suspend command, complete the operation with a resume command.

43.14.3 Constraints on Additional Writes

Other than the configuration area, no other area can be written to twice. After a write to a flash memory area is complete, erase the area before attempting to overwrite data in that area. The configuration area can be overwritten.

43.14.4 Reset during Programming and Erasure

If inputting a reset from the RES pin, release the reset after a reset input time of at least tRESW (see section 48, Electrical Characteristics) within the range of the operating voltage defined in the electrical characteristics.

The IWDT reset and software reset do not require a tRESW input time.

43.14.5 Non-Maskable Interrupt Disabled during Programming and Erasure

When a non-maskable interrupt*1 occurs during a programming and erasure operation, the vectors are fetched from the code flash memory, and undefined data is read. Therefore, do not generate a non-maskable interrupt during a programming and erasure operation in the code flash memory. This constraint applies only to the code flash memory.

Note 1. A non-maskable interrupt is an NMI pin interrupt, oscillation stop detection interrupt, WDT underflow/refresh error interrupt, IWDT underflow/refresh error interrupt, voltage monitor 1 interrupt, VBATT monitor interrupt, SRAM parity error interrupt, SRAM ECC error interrupt, MPU bus master error interrupt, MPU bus slave error interrupt, or CPU stack pointer monitor interrupt.

43.14.6 Location of Interrupt Vectors during Programming and Erasure

When an interrupt occurs during a programming and erasure operation, the vector can be fetched from the code flash memory. To avoid fetching the vector from the code flash memory, set the destination for fetching interrupt vectors to an area other than the code flash memory with the interrupt table.

43.14.7 Programming and Erasure in Low-Speed Operating Mode

Do not program or erase the flash memory when low-speed operating mode is selected in the SOPCCR register for low power consumption functions.

43.14.8 Abnormal Termination during Programming and Erasure

When the voltage exceeds the range of the operating voltage during a programming and erasure operation, or when a programming or erasure operation did not complete successfully because of a reset or prohibited actions as described in section 43.14.9, Actions Prohibited during Programming and Erasure, erase the area again.

43.14.9 Actions Prohibited during Programming and Erasure

To prevent damage to the flash memory, comply with the following instructions during programming and erasure:

- Do not use an MCU power supply that is outside the operating voltage range
- Do not update the OPCCR.OPCM[1:0] bit value
- Do not update the SOPCCR.SOPCM bit value
- Do not change the division ratio of the flash interface clock (FCLK)
- Do not place the MCU in Software Standby mode
- Do not access the data flash memory during a programming or erasure operation to the code flash memory
- Do not change the DFLCTL.DFLEN bit value during a programming or erasure operation to the data flash memory.

43.14.2 通过擦除挂起命令挂起

使用erasesuspend命令暂停擦除操作时，请使用resume命令完成操作。

43.14.3 额外写入的限制

除配置区域外，其他区域不能写入两次。对闪存区域的写入完成后，请先擦除该区域，然后再尝试覆盖该区域中的数据。配置区域可以被覆盖。

43.14.4 在编程和擦除期间复位

如果从RES引脚输入复位，请在至少tRESW的复位输入时间后释放复位（参见第48节，电气特性)在电气特性中定义的工作电压范围内。

IWDT复位和软件复位不需要tRESW输入时间。

43.14.5 在编程和擦除期间禁用不可屏蔽中断

在编程和擦除操作期间发生不可屏蔽中断*1时，将从代码闪存中获取向量，并读取未定义的数据。因此，在代码闪存中的编程和擦除操作期间不要产生不可屏蔽的中断。此约束仅适用于代码闪存。

注1.不可屏蔽中断是NMI引脚中断、振荡停止检测中断、WDT下溢刷新错误中断　　、IWDT下溢刷新错误中断　　、电压监控1中断、VBATT监控中断、SRAM奇偶校验错误中断、SRAMECC错误中断、MPU总线主机错误中断、MPU总线从机错误中断或CPU堆栈指针监控中断。

43.14.6 编程和擦除期间中断向量的位置

当在编程和擦除操作期间发生中断时，可以从代码闪存中获取向量。为避免从代码闪存中获取向量，请使用中断表将获取中断向量的目标设置为代码闪存之外的区域。

43.14.7 低速操作模式下的编程和擦除

当在SOPCCR寄存器中选择低速工作模式以实现低功耗功能时，请勿对闪存进行编程或擦除。

43.14.8 编程和擦除过程中的异常终止

当电压在编程和擦除操作期间超过工作电压范围时，或者由于第43.14.9节"编程和擦除期间禁止的操作"中所述的复位或禁止操作而导致编程或擦除操作未成功完成时，再次擦除该区域。

43.14.9 编程和擦除期间禁止的操作

为防止损坏闪存，请在编程和擦除过程中遵守以下说明：

- 请勿使用超出工作电压范围的MCU电源
- 不更新OPCCR.OPCM[1:0]位值
- 不更新SOPCCR.SOPCM位值
- 不要改变闪存接口时钟（FCLK）的分频比
- 不要将MCU置于软件待机模式
- 在对代码闪存进行编程或擦除操作期间不要访问数据闪存
- 在对数据闪存进行编程或擦除操作期间，请勿更改DFLCTL.DFLEN位的值。

44. Segment LCD Controller (SLCDC)

44.1 Overview

The MCU provides a controller for LCD display and display pins. Table 44.1 lists the SLCDC specifications.

Table 44.1 SLCDC specifications

Parameter	Description
Features	• Liquid crystal waveform (waveform A or B) selectable • LCD driver voltage generator can use external resistance division method • Automatic output of segment and shared signals based on automatic display data register read • LCD blinking and display selectable.
Number of pins	For details on the number of pins, see Table 44.2, SLCDC display function pins for 56-pin products
Source clocks	• Main clock oscillator • Sub-clock oscillator • Low-speed on-chip oscillator • High-speed on-chip oscillator.
Module-stop state function	Module-stop state can be set to reduce power consumption

The number of LCD display function pins for the MCU differ depending on the product. Table 44.2 shows the display function pins for products with different pin counts. Table 44.3 shows the maximum number of pixels for products with different pin counts. Figure 44.1 shows the SLDC block diagram.

Table 44.2 SLCDC display function pins for 56-pin products

Parameter	56 Pins															
LCD controller/ driver	Number of segment pins (SEG) : 9 Number of common pins (COM) : 4															
Multiplexed I/O port	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PORT1	-	-	-	-	-	SEG 53	SEG 52	-	COM 3	COM 2	COM 1	COM 0	VL4*1	-	VL2*1	VL1*1
PORT2	-	-	-	-	-	-	-	-	-	SEG 12	SEG 20	SEG 23	-	-	-	-
PORT3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT4	-	-	-	-	-	-	SEG9	-	SEG 11	-	-	-	-	SEG6	-	-
PORT5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SEG 49	-
PORT6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note 1. VL1, VL2, and VL4 are power supply pins for driving the LCD.

Table 44.3 Maximum number of pixels for 56-pin products (1 of 2)

Drive waveform for LCD driver	LCD driver voltage generator	Bias mode	Number of time slices	Maximum number of pixels
Waveform A	External resistance division	-	Static	9 (9 segment signals, 1 common signal)
		1/2	2	18 (9 segment signals, 2 common signals)
			3	27 (9 segment signals, 3 common signals)
		1/3	3	
			4	36 (9 segment signals, 4 common signals)

44. 段式LCD控制器(SLCDC)

44.1 Overview

MCU为LCD显示和显示引脚提供控制器。表44.1列出了SLCDC规格。

Table 44.1 SLCDC specifications

Parameter	Description
Features	液晶波形（波形A或B）可选 LCD驱动电压发生器可以使用外部电阻分压方法 根据自动显示数据寄存器读取自动输出段和共享信号 LCD闪烁和显示可选。
引脚数	管脚数量详见表44.2，56管脚产品的SLCDC显示功能管脚
源时钟	主时钟振荡器 子时钟振荡器 低速内部振荡器 高速内部振荡器。
模块停止状态功能	可设置模块停止状态以降低功耗

MCU的LCD显示功能引脚数因产品而异。表44.2显示了具有不同引脚数的产品的显示功能引脚。表44.3显示了具有不同引脚数的产品的最大像素数。图44.1显示了SLDC框图。

Table 44.2 SLCDC显示功能引脚用于56引脚产品

Parameter	56 Pins															
LCD controller/ driver	段引脚数(SEG):9公共引脚数(COM): 4															
Multiplexed I/O port	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PORT1	-	-	-	-	-	SEG 53	SEG 52	-	COM 3	COM 2	COM 1	COM 0	VL4*1	-	VL2*1	VL1*1
PORT2	-	-	-	-	-	-	-	-	-	SEG 12	SEG 20	SEG 23	-	-	-	-
PORT3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT4	-	-	-	-	-	-	SEG9	-	SEG 11	-	-	-	-	SEG6	-	-
PORT5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SEG 49	-
PORT6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PORT9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note 1. VL1、VL2和VL4是驱动LCD的电源引脚。

Table 44.3 56针产品的最大像素数（2个中的1个）

LCD驱动器的驱动波形	LCD驱动电压发生器	偏置模式	时间片数	最大像素数
Waveform A	外电阻分工	-	Static	9个（9个段信号，1个公共信号）
		1/2	2	18个（9个段信号，2个公共信号）
			3	27（9个段信号，3个公共信号）
		1/3	3	
			4	36（9个段信号，4个公共信号）

Table 44.3 Maximum number of pixels for 56-pin products (2 of 2)

Drive waveform for LCD driver	LCD driver voltage generator	Bias mode	Number of time slices	Maximum number of pixels
Waveform B	External resistance division	1/3	4	36 (9 segment signals, 4 common signals)

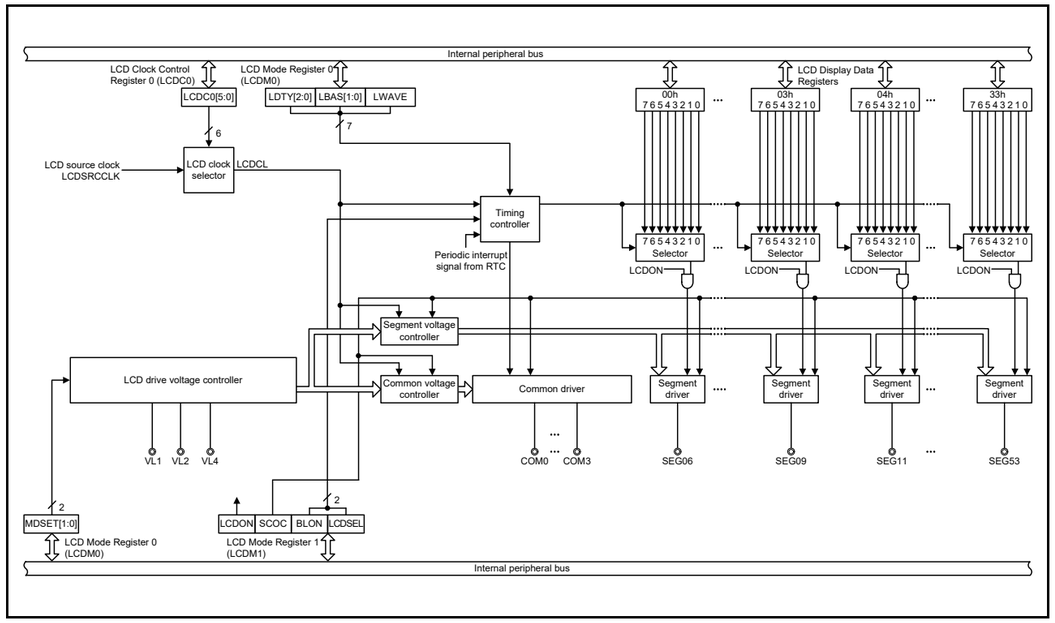


Figure 44.1 SLCDC block diagram

44.2 Register Descriptions

44.2.1 LCD Mode Register 0 (LCDM0)

Address(es): SLCDC.LCDM0 4008 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	MDSET[1:0]		LWAVE	LDTY[2:0]			LBAS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	LBAS[1:0]	LCD Display Bias Method Select	b1 b0 0 0: 1/2 bias method 0 1: 1/3 bias method 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b4 to b2	LDTY[2:0]	Time Slice of LCD Display Select	b4 b2 0 0 0: Static 0 0 1: 2-time slice 0 1 0: 3-time slice 0 1 1: 4-time slice Other settings are prohibited.	R/W
b5	LWAVE	LCD Display Waveform Select	0: Waveform A 1: Waveform B.	R/W

Table 44.3 56针产品的最大像素数（2个中的2个）

LCD驱动器的驱动波形	LCD驱动电压发生器	偏置模式	时间片数	最大像素数
Waveform B	外电阻分工	1/3	4	36（9个段信号，4个公共信号）

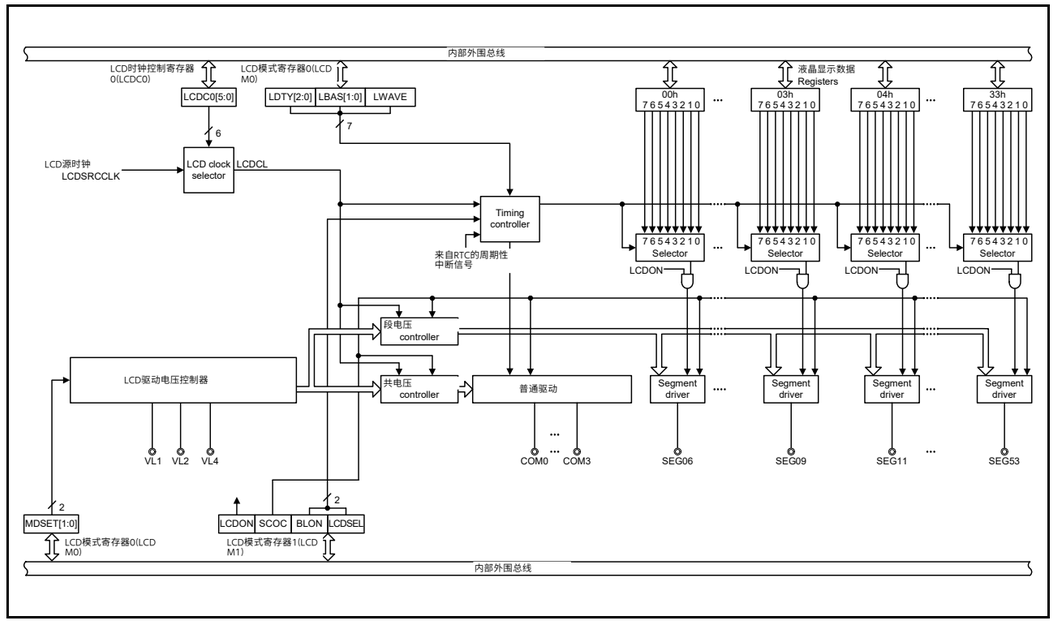


Figure 44.1 SLCDC框图

44.2 注册说明

44.2.1 LCD模式寄存器0(LCDM0)

Address(es): SLCDC.LCDM0 4008 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	MDSET[1:0]		LWAVE	LDTY[2:0]			LBAS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	LBAS[1:0]	LCD显示偏压法 Select	b1b000：12偏置方式0 1：13偏置方式10：禁 止设置11：禁止设置。	R/W
b4 to b2	LDTY[2:0]	液晶时间片 显示选择	b4b2000：静态001：2-tim eslice010：3-timeslice011 ：4-timeslice禁止其他设置 。	R/W
b5	LWAVE	LCD显示波形 Select	0: Waveform A 1: Waveform B.	R/W

Bit	Symbol	Bit name	Description	R/W
b7, b6	MDSET[1:0]	LCD Drive Voltage Generator Select	b7 b6 0 0: External resistance division method Other settings are prohibited.	R/W

Note: Do not rewrite the LCDM0 value when the SCOC bit of the LCDM1 register is 1.
Note: When static is selected (LDTY[2:0] = 000b), you must set the LBAS[1:0] bits to the default value (00b). Otherwise, the operation is not guaranteed.
Note: Only the combinations of display waveform, number of time slices, and bias method shown in Table 44.4 are supported. Combinations of settings not shown in Table 44.4 are prohibited.

Table 44.4 Combinations of display waveform, time slices, bias method, and frame frequency

Display mode			Set value						Driving voltage generation method
Display waveform	Number of time slices	Bias mode	LWAVE	LDTY[2:0]			LBAS[1:0]		External resistance division
Waveform A	4	1/3	0	0	1	1	0	1	A
Waveform A	3	1/3	0	0	1	0	0	1	A
Waveform A	3	1/2	0	0	1	0	0	0	A
Waveform A	2	1/2	0	0	0	1	0	0	A
Waveform A	Static		0	0	0	0	0	0	A
Waveform B	4	1/3	1	0	1	1	0	1	A

A: Available, N/A: Not available

44.2.2 LCD Mode Register 1 (LCDM1)

Address(es): SLCDC.LCDM1 4008 2001h

	b7	b6	b5	b4	b3	b2	b1	b0
	LCDON	SCOC	—	BLON	LCDSEL	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	LCDSEL	Display Data Area Control	b4 b3 0 0: Display an A-pattern area data (lower 4 bits of LCD display data register) 0 1: Display a B-pattern area data (upper 4 bits of LCD display data register) 1 0: Alternately display A-pattern and B-pattern area data (blinking display associated with the periodic interrupt (RTC_PRD) timing of the Realtime Clock (RTC)) 1 1: Alternately display A-pattern and B-pattern area data (blinking display associated with the periodic interrupt (RTC_PRD) timing of the Realtime Clock (RTC)).	R/W
b4	BLON	Display Data Area Control		R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	SCOC	LCD Display Enable/Disable	b7 b6 0 0: Output ground level to segment/common pin 0 1: Display off (all segment outputs are deselected) 1 0: Output ground level to segment/common pin 1 1: Display on.	R/W
b7	LCDON	LCD Display Enable/Disable		R/W

Bit	Symbol	位名称	Description	R/W
b7, b6	MDSET[1:0]	LCD驱动电压发电机选择	b7b600：外部电阻分压方式禁止其他设置。	R/W

Note: LCDM1寄存器的SCOC位为1时，不要改写LCDM0的值。
Note: 选择静态时(LDTY[2:0]=000b)，您必须将LBAS[1:0]位设置为默认值(00b)。否则，无法保证运行。

Note: 仅支持表44.4所示的显示波形、时间片数和偏置方法的组合。
禁止组合未在表44.4中显示的设置。

Table 44.4 显示波形、时间片、偏置方法和帧频的组合

显示模式			设定值						驱动电压产生方法
显示波形	时间片数	偏置模式	LWAVE	LDTY[2:0]			LBAS[1:0]		外电阻分工
Waveform A	4	1/3	0	0	1	1	0	1	A
Waveform A	3	1/3	0	0	1	0	0	1	A
Waveform A	3	1/2	0	0	1	0	0	0	A
Waveform A	2	1/2	0	0	0	1	0	0	A
Waveform A	Static		0	0	0	0	0	0	A
Waveform B	4	1/3	1	0	1	1	0	1	A

A：可用，NA：不可用

44.2.2 LCD模式寄存器1(LCDM1)

Address(es): SLCDC.LCDM1 4008 2001h

	b7	b6	b5	b4	b3	b2	b1	b0
	LCDON	SCOC	—	BLON	LCDSEL	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	LCDSEL	显示数据区控件	b4b300：显示A模式区域数据（LCD显示数据寄存器的低4位）01：显示B模式区域数据（LCD显示数据寄存器的高4位）10：交替显示A模式和B模式区域数据（与实时时钟(RTC)的周期性中断(RTC_PRD)时序相关的闪烁显示）11：交替显示A模式和B模式区域数据（与周期性中断相关的闪烁显示(RTC_PRD))实时时钟(RTC)的时序。	R/W
b4	BLON	显示数据区控件		R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	SCOC	LCD Display Enable/Disable	b7b600：输出地电平到段公共引脚01：显示关闭（取消选择所有段输出）10：输出地电平到段公共引脚11：显示打开。	R/W
b7	LCDON	LCD Display Enable/Disable		R/W

44.2.3 LCD Clock Control Register 0 (LCDC0)

Address(es): SLCDC.LCDC0 4008 2002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LCDC0[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	LCDC0[5:0]	LCD Clock (LCDCL) Setting	b5 b0 0 0 0 0 0 1: (Sub clock)/2^2 or (LOCO clock)/2^2 0 0 0 0 1 0: (Sub clock)/2^3 or (LOCO clock)/2^3 0 0 0 0 1 1: (Sub clock)/2^4 or (LOCO clock)/2^4 0 0 0 1 0 0: (Sub clock)/2^5 or (LOCO clock)/2^5 0 0 0 1 0 1: (Sub clock)/2^6 or (LOCO clock)/2^6 0 0 0 1 1 0: (Sub clock)/2^7 or (LOCO clock)/2^7 0 0 0 1 1 1: (Sub clock)/2^8 or (LOCO clock)/2^8 0 0 1 0 0 0: (Sub clock)/2^9 or (LOCO clock)/2^9 0 0 1 0 0 1: (Sub clock)/2^{10} or (LOCO clock)/2^{10} 0 1 0 0 0 1: (Main clock)/2^8 or (HOCO clock)/2^8 0 1 0 0 1 0: (Main clock)/2^9 or (HOCO clock)/2^9 0 1 0 0 1 1: (Main clock)/2^{10}or (HOCO clock)/2^{10} 0 1 0 1 0 0: (Main clock)/2^{11}or (HOCO clock)/2^{11} 0 1 0 1 0 1: (Main clock)/2^{12} or (HOCO clock)/2^{12} 0 1 0 1 1 0: (Main clock)/2^{13} or (HOCO clock)/2^{13} 0 1 0 1 1 1: (Main clock)/2^{14} or (HOCO clock)/2^{14} 0 1 1 0 0 0: (Main clock)/2^{15} or (HOCO clock)/2^{15} 0 1 1 0 0 1: (Main clock)/2^{16} or (HOCO clock)/2^{16} 0 1 1 0 1 0: (Main clock)/2^{17} or (HOCO clock)/2^{17} 0 1 1 0 1 1: (Main clock)/2^{18} or (HOCO clock)/2^{18} 1 0 1 0 1 1: (Main clock)/2^{19} or (HOCO clock)/2^{19}. Other settings are prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the frame frequency in a range from 32 Hz to 128 Hz.
Note: Do not set LCDC0 when the LCDM1.SCOC bit is 1.

44.3 LCD Display Data Registers

The LCD display data registers are mapped as shown in Table 44.5. The contents displayed on the LCD can be changed by changing the contents of the LCD display data registers.

Table 44.5 Relationship between LCD Display Data Register contents and segment/common outputs

Register name	Address	b7	b6	b5	b4	b3	b2	b1	b0	56-pin
		COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	
SEG06	4008 2106h	SEG06 (B-pattern area)				SEG06 (A-pattern area)				A
SEG09	4008 2109h	SEG09 (B-pattern area)				SEG09 (A-pattern area)				A
SEG11	4008 210Bh	SEG11 (B-pattern area)				SEG11 (A-pattern area)				A
SEG12	4008 210Ch	SEG12 (B-pattern area)				SEG12 (A-pattern area)				A
SEG20	4008 2114h	SEG20 (B-pattern area)				SEG20 (A-pattern area)				A
SEG23	4008 2117h	SEG23 (B-pattern area)				SEG23 (A-pattern area)				A
SEG49	4008 2131h	SEG49 (B-pattern area)				SEG49 (A-pattern area)				A
SEG52	4008 2134h	SEG52 (B-pattern area)				SEG52 (A-pattern area)				A
SEG53	4008 2135h	SEG53 (B-pattern area)				SEG53 (A-pattern area)				A

A: Available, N/A: Not available

Note: All LCD display data registers have an initial value of 0h, and all bits that are read/write.

44.2.3 LCD时钟控制寄存器0(LCDC0)

Address(es): SLCDC.LCDC0 4008 2002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LCDC0[5:0]					
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	LCDC0[5:0]	LCD Clock (LCDCL) Setting	b5b0000001：（副时钟）22或（LOCO时钟）22000010：（副时钟）23或（LOCO时钟）23000011：（副时钟）24或（LOCO时钟）24000100：（副时钟）25或（LOCO时钟）25000101：（副时钟）26或（LOCO时钟）26000110:(副时钟)27或(LOCO时钟)27000111:(副时钟)28或(LOCO时钟)28001000:(副时钟）29或（LOCO时钟）29001001：（副时钟）210或（LOCO时钟）210010001：（主时钟）28或（HOCO时钟）28010010：（主时钟）29或（HOCO时钟）29010011：（主时钟）210或（HOCO时钟）210010100：（主时钟）211或（HOCO时钟）211010101：（主时钟）212或（HOCO时钟）212010110：（主时钟）213或（HOCO时钟）213010111：（主时钟）214或（HOCO时钟）214011000：（主时钟）215或（HOCO时钟）215011001：（主时钟）216或（HOCO时钟）216011010：（主时钟）217或（HOCO时钟）217011011：（主时钟）)218或（HOCO时钟）218101011：（主时钟）219或（HOCO时钟）219。禁止其他设置。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 将帧频率设置在32Hz到128Hz的范围内。
Note: LCDM1.SCOC位为1时不要设置LCDC0。

44.3 LCD显示数据寄存器

LCD显示数据寄存器的映射如表44.5所示。通过改变LCD显示数据寄存器的内容，可以改变LCD上显示的内容。

Table 44.5 LCD显示数据寄存器内容和段公共输出之间的关系

注册名称	Address	b7	b6	b5	b4	b3	b2	b1	b0	56-pin
		COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	
SEG06	4008 2106h	SEG06 (B-pattern area)				SEG06 (A-pattern area)				A
SEG09	4008 2109h	SEG09 (B-pattern area)				SEG09 (A-pattern area)				A
SEG11	4008 210Bh	SEG11 (B-pattern area)				SEG11 (A-pattern area)				A
SEG12	4008 210Ch	SEG12 (B-pattern area)				SEG12 (A-pattern area)				A
SEG20	4008 2114h	SEG20 (B-pattern area)				SEG20 (A-pattern area)				A
SEG23	4008 2117h	SEG23 (B-pattern area)				SEG23 (A-pattern area)				A
SEG49	4008 2131h	SEG49 (B-pattern area)				SEG49 (A-pattern area)				A
SEG52	4008 2134h	SEG52 (B-pattern area)				SEG52 (A-pattern area)				A
SEG53	4008 2135h	SEG53 (B-pattern area)				SEG53 (A-pattern area)				A

A：可用，NA：不可用

Note: 所有LCD显示数据寄存器的初始值为0h，并且所有位都是可读写的。

When the number of time slices is static, two, three, or four, the lower four bits and upper four bits of each address of the LCD display data register become an A-pattern area and a B-pattern area, respectively.

The correspondence between A-pattern area data and COM signals is as follows:
bit [0] ↔ COM0, bit [1] ↔ COM1, bit [2] ↔ COM2, and bit [3] ↔ COM3.

The correspondence between B-pattern area data and COM signals is as follows:
bit [4] ↔ COM0, bit [5] ↔ COM1, bit [6] ↔ COM2, and bit [7] ↔ COM3.

A-pattern area data is displayed on the LCD panel when BLON = LCDSEL = 0 is selected, and B-pattern area data is displayed on the LCD panel when BLON = 0 and LCDSEL = 1 is selected.

44.4 Selection of LCD Display Data Register

When the number of time slices is static, two, three, or four, the LCD display data register can be selected from the following types, based on the BLON and LCDSEL bit settings:

- Displaying an A-pattern area data (lower 4 bits of LCD display data register)
- Displaying a B-pattern area data (upper 4 bits of LCD display data register)
- Alternately displaying an A-pattern and B-pattern area data (blinking display associated with the periodic interrupt timing of the Realtime Clock (RTC)).

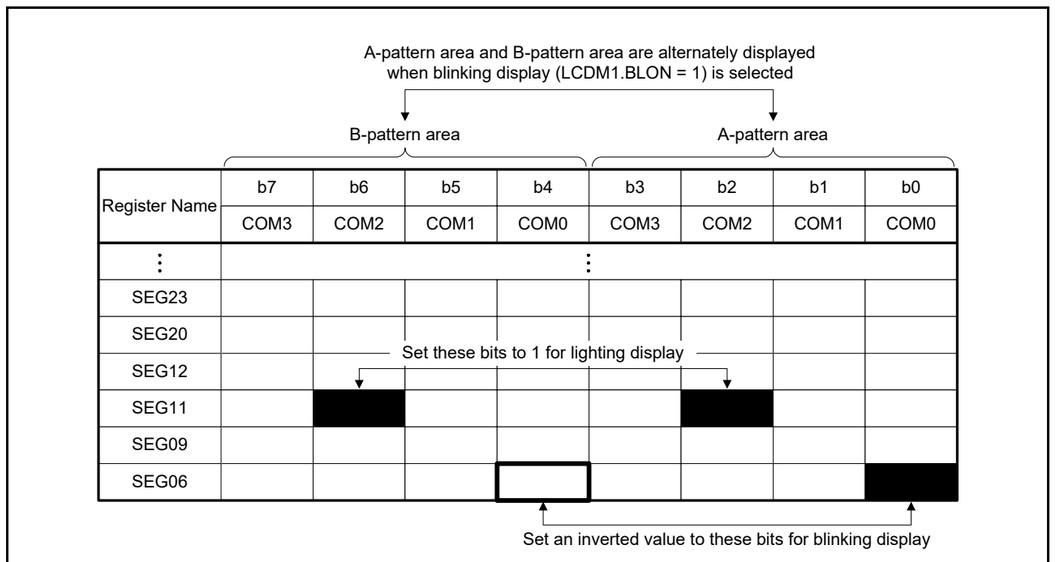


Figure 44.2 Example for setting LCD display data registers when the pattern is changed

44.4.1 A-Pattern Area and B-pattern Area Data Display

When both BLON and LCDSEL are 0, A-pattern area (lower four bits of the LCD display data register) data is output as the LCD display register.

When BLON is 0 and LCDSEL is 1, B-pattern area (upper four bits of the LCD display data register) data is output as the LCD display register.

For details on the display area, see section 44.3, LCD Display Data Registers.

44.4.2 Blinking Display (Alternately Displaying A-Pattern and B-Pattern Area Data)

When BLON is set to 1, A-pattern and B-pattern area data are alternately displayed, according to the constant-period interrupt timing of the Realtime Clock (RTC). See section 25, Realtime Clock (RTC) for information about the setting of

当时间片的个数为静态时，两个、三个或四个时，每个地址的低四位和高四位
LCD显示数据寄存器分别成为A模式区域和B模式区域。

A字区数据与COM信号的对应关系如下：bit[0]↔COM0，bit[1]↔COM1，
bit[2]↔COM2，bit[3]↔COM3。

B-pattern区域数据与COM信号的对应关系如下：bit[4]↔COM0，bit[5]↔
COM1，bit[6]↔COM2，bit[7]↔COM3。

选择BLON=LCDSEL=0时，LCD面板上显示A图案区域数据，选择BLON=0和LCDSEL=1时，LCD面板上显示B图案区域数据。

44.4 LCD显示数据寄存器的选择

当时间片数为静态、二、三或四时，可根据BLON和LCDSEL位设置从以下类型中选择LCD显示数据寄存器：

- 显示A型区域数据（LCD显示数据寄存器的低4位）
- 显示B模式区域数据（LCD显示数据寄存器的高4位）
- 交替显示A模式和B模式区域数据（与实时时钟(RTC)的周期性中断时序相关的闪烁显示）。

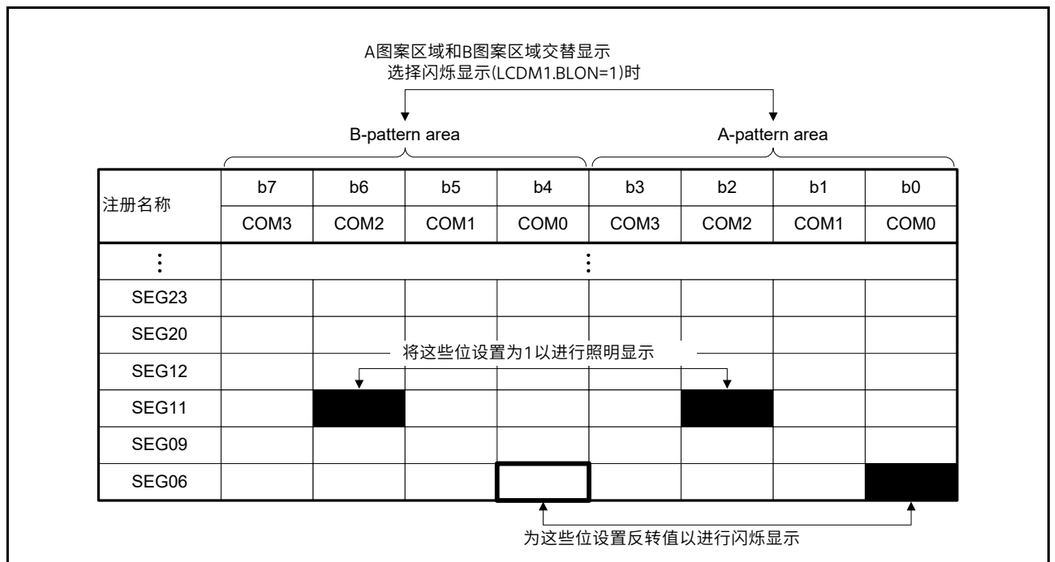


Figure 44.2 模式更改时设置LCD显示数据寄存器的示例

44.4.1 A型区域和B型区域数据显示

当BLON和LCDSEL都为0时，A模式区域（LCD显示数据寄存器的低4位）数据作为LCD显示寄存器输出。

当BLON为0且LCDSEL为1时，B模式区域（LCD显示数据寄存器的高4位）数据作为
LCD显示寄存器。

有关显示区域的详细信息，请参阅第44.3节，LCD显示数据寄存器。

44.4.2 闪烁显示（交替显示A-Pattern和B-Pattern区域数据）

当BLON设置为1时，根据实时时钟(RTC)的恒定周期中断时序交替显示A模式和B模式区域数据。有关设置的信息，请参见第25节，实时时钟(RTC)

the RTC constant-period interrupt (0.5 s setting only) timing.

To use the LCD blinking display feature, set inverted values to the B-pattern area bits associated with the A-pattern area bits. For example, set bit [0] of SEG06 register to 1, and bit [4] of SEG06 register to 0 to use the blinking display. When not using the blinking display feature, set the same values to both the A-pattern and B-pattern area bits. For example, set bit [2] of SEG09 register to 1, and set bit [6] of SEG09 register to 1 for lighting display. For details on the display area, see section 44.3, LCD Display Data Registers.

Figure 44.3 and Figure 44.4 show the timing operation of display switching.

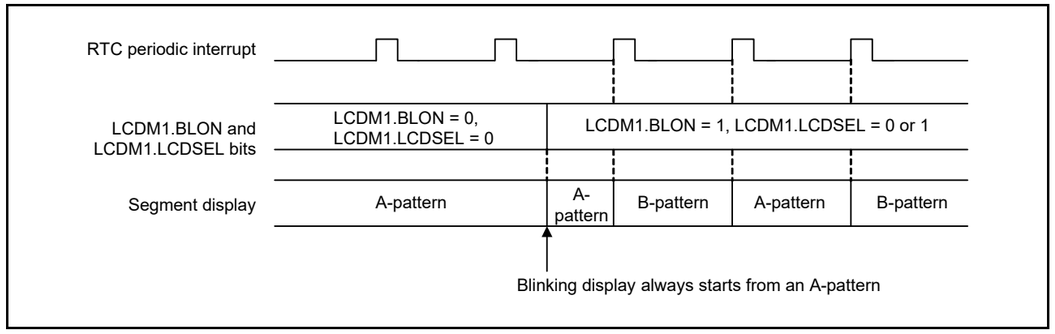


Figure 44.3 Switching operation from A-pattern display to blinking display

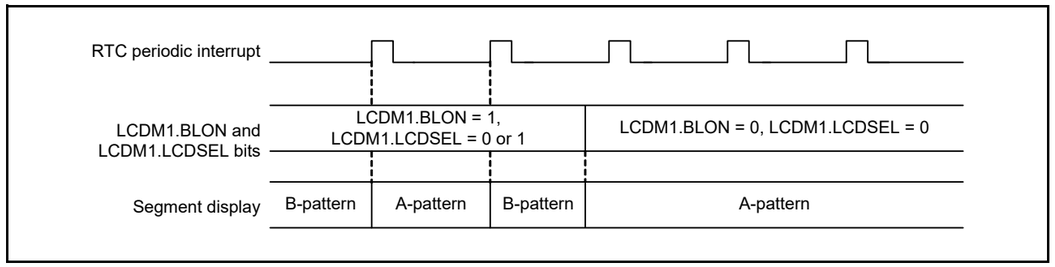


Figure 44.4 Switching operation from blinking display to A-pattern display

44.5 Setting LCD Controller/Driver

To operate the LCD controller/driver, follow procedures in this section. Otherwise, the LCD operation is not guaranteed.

RTC恒定周期中断（仅0.5秒设置）时序。

要使用LCD闪烁显示功能，请将反转值设置为与A模式区域位相关的B模式区域位。例如，将SEG06寄存器的位[0]设置为1，将SEG06寄存器的位[4]设置为0以使用闪烁显示。不使用闪烁显示功能时，将相同的值设置为A模式和B模式区域位。例如，将SEG09寄存器的位[2]设置为1，将SEG09寄存器的位[6]设置为1用于照明显示。有关显示区域的详细信息，请参阅第44.3节，LCD显示数据寄存器。

图44.3和图44.4显示了显示切换的时序操作。

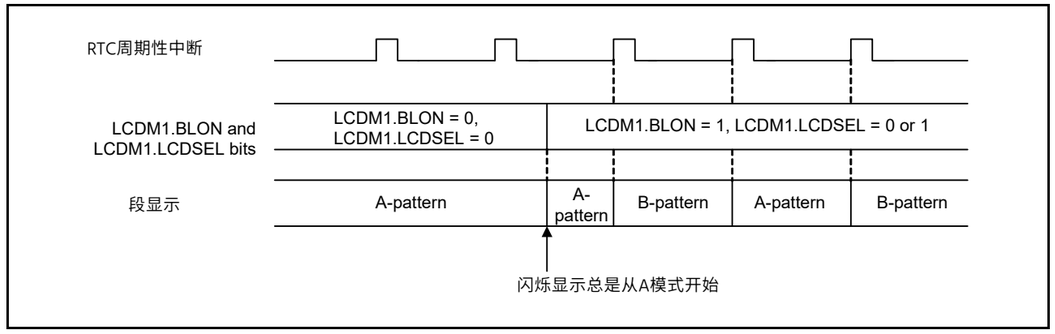


Figure 44.3 从A模式显示切换到闪烁显示

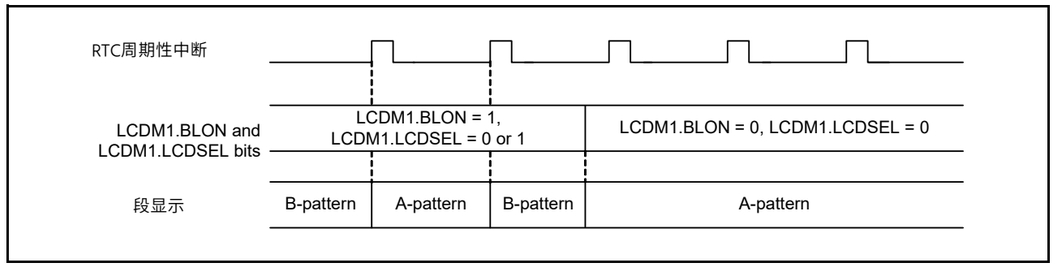


Figure 44.4 从闪烁显示切换到A模式显示

44.5 Setting LCD Controller/Driver

要操作LCD控制器驱动程序，请遵循本节中的步骤。否则，无法保证LCD操作。

(1) External resistance division method during normal liquid crystal waveform display

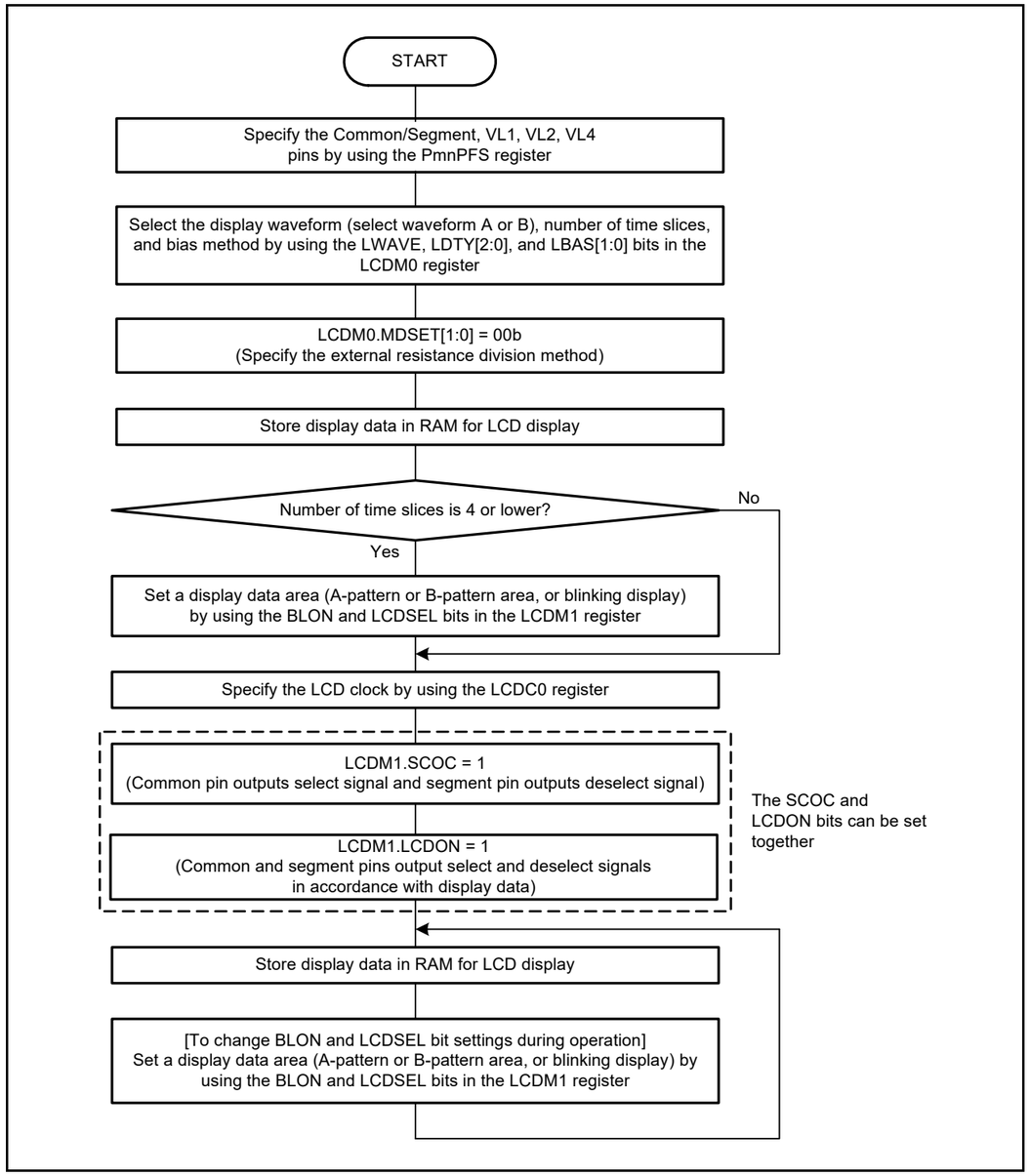


Figure 44.5 Setting procedure for external resistance division method during normal liquid crystal waveform display

44.6 Operation Stop Procedure

To stop the operation of the LCD, follow the steps shown in Figure 44.6.

The LCD stops operating when the LCDM1.LDCON and LCDM1.SCOC bits are set to 0.

(1) 正常液晶波形显示时的外阻划分方法

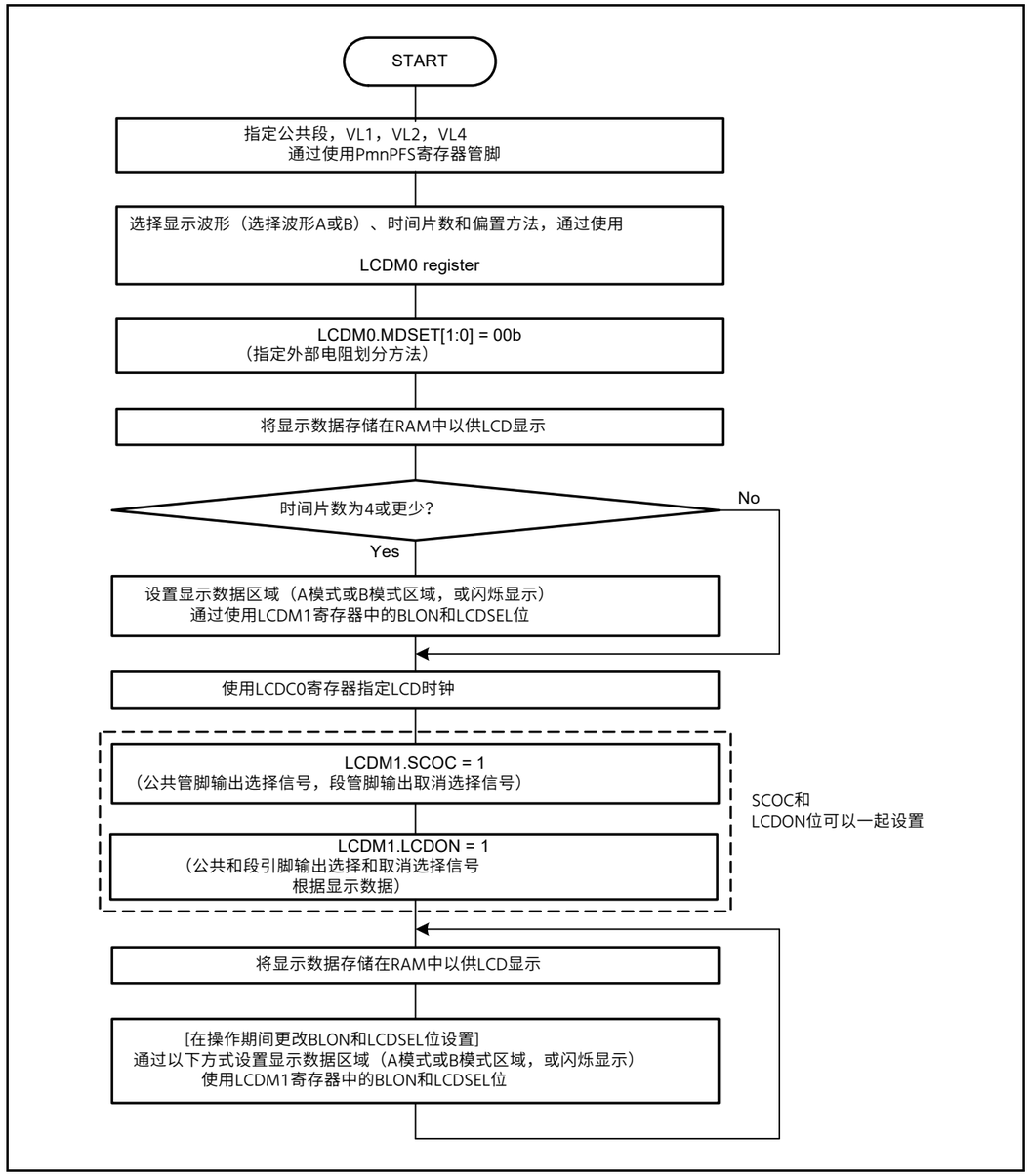


Figure 44.5 正常液晶波形显示时外接电阻分压方法的设置步骤

44.6 运行停止程序

要停止LCD的操作，请按照图44.6中所示的步骤操作。

LCDM1.LDCON和LCDM1.SCOC位设置为0时LCD停止工作。

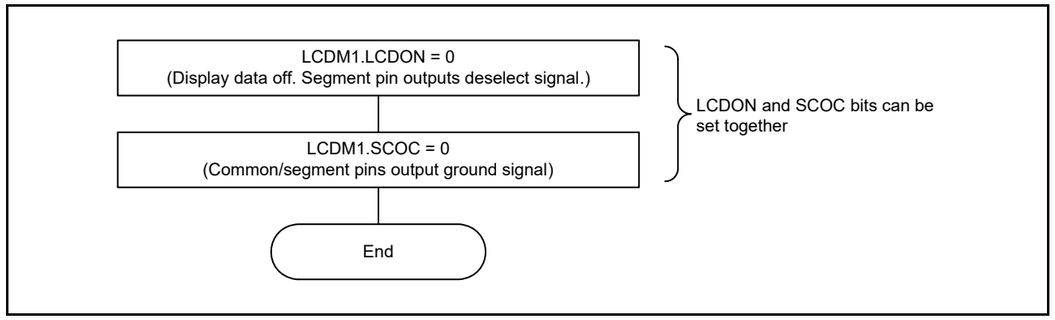


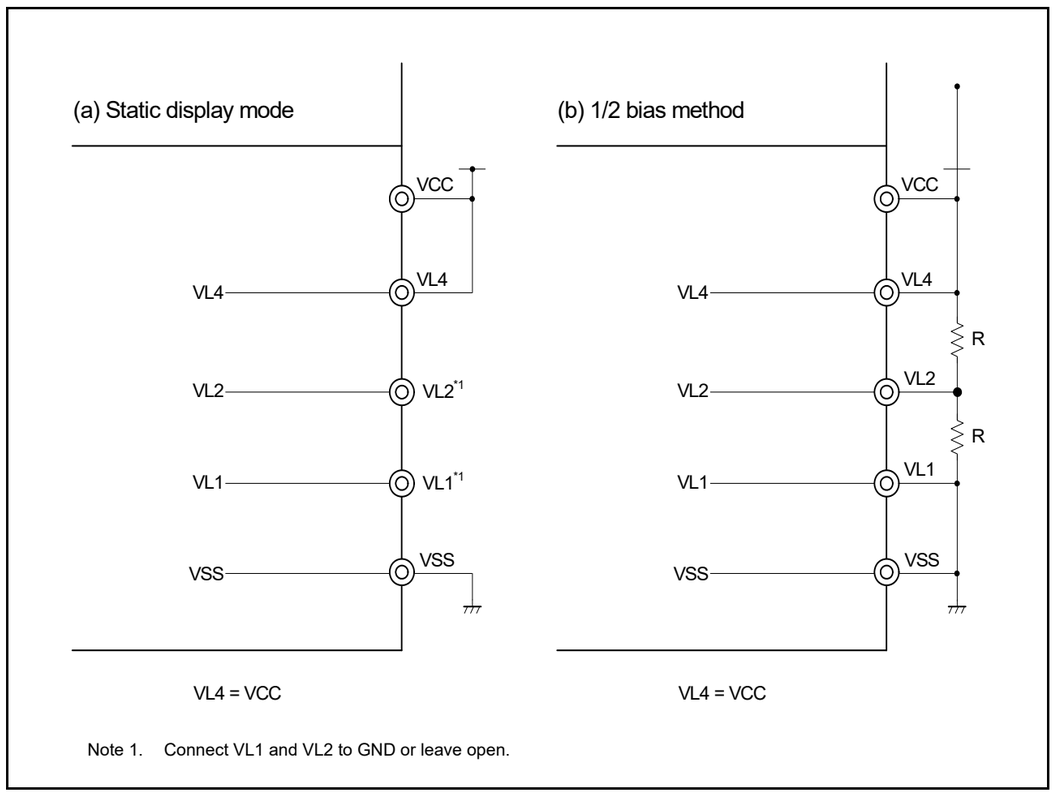
Figure 44.6 Operation stop procedure during normal liquid crystal waveform (A or B) display

44.7 Supplying LCD Drive Voltages VL1, VL2, and VL4

The power supply voltages for the LCD driver can be produced through external resistance division.

44.7.1 External Resistance Division Method

Figure 44.7 and Figure 44.8 show examples of the LCD drive power supply connection, associated with each bias method.



Note 1. Connect VL1 and VL2 to GND or leave open.

Figure 44.7 Examples of LCD drive power connections using the external resistance division method (1 of 2)

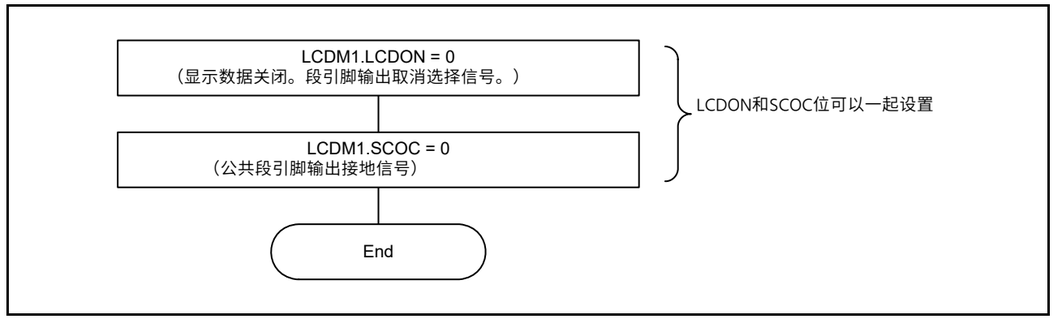


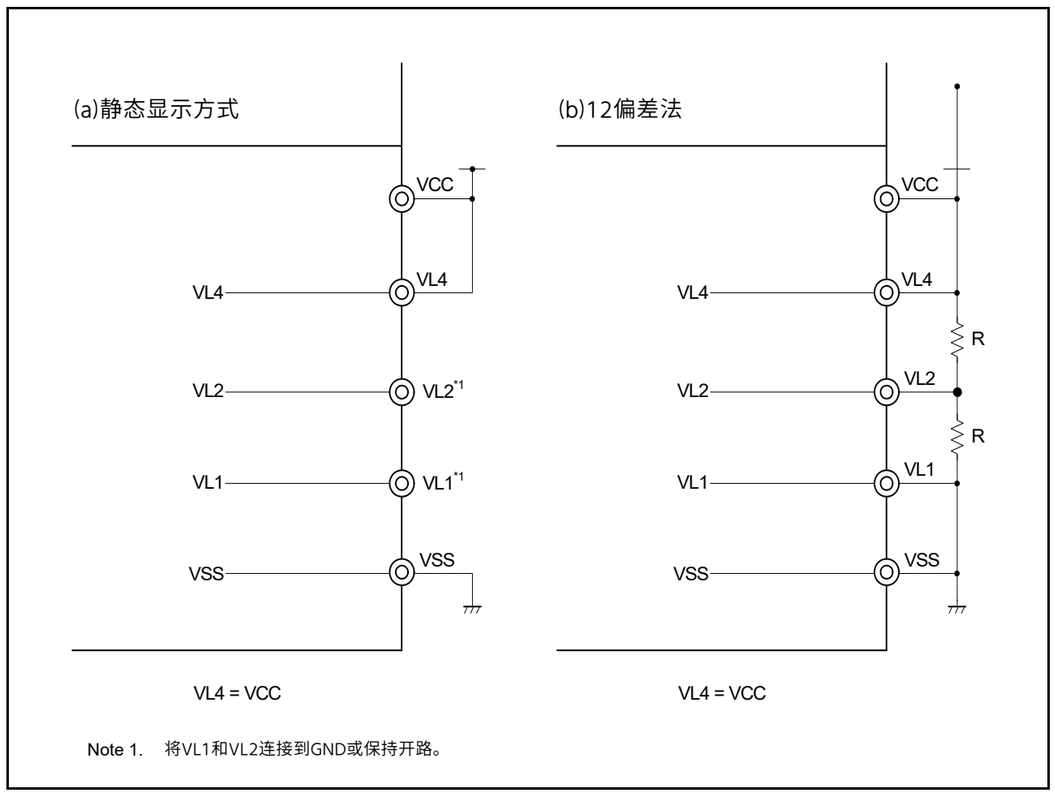
Figure 44.6 正常液晶波形（A或B）显示期间的操作停止程序

44.7 提供LCD驱动电压VL1、VL2和VL4

LCD驱动器的电源电压可以通过外部电阻分压产生。

44.7.1 外电阻分法

图44.7和图44.8显示了与每种偏置方法相关的LCD驱动电源连接示例。



Note 1. 将VL1和VL2连接到GND或保持开路。

Figure 44.7 使用外部电阻分压法的LCD驱动电源连接示例(1of2)

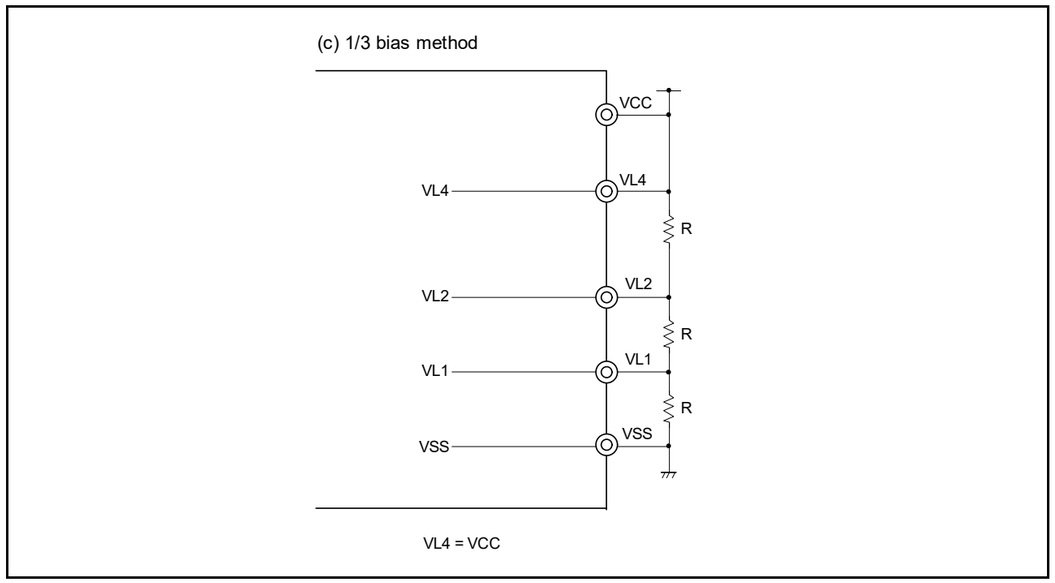


Figure 44.8 Examples of LCD drive power connections using external resistance division method (2 of 2)

Note: The reference resistance R value for external resistance division is 10 kΩ to 1 MΩ. In addition, to stabilize the voltage at the VL1 to VL4 pins, connect a capacitor between each pin VL1 to VL4 and the GND pin as needed. The reference capacitance is about 0.47 μF, but it depends on the LCD panel used, the number of segment pins, the number of common pins, the frame frequency, and the operating environment. Thoroughly evaluate these values in accordance with your system and adjust the capacitance.

44.8 Common and Segment Signals

Each pixel of an LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage, VLCD). The pixels turn off when the potential difference becomes lower than VLCD.

Applying DC voltage to the common and segment signals of an LCD panel causes deterioration. To avoid this problem, the SLCDC is driven by AC voltage.

(1) Common signals

Each common signal is selected sequentially according to a specified number of time slices listed in Table 44.6. In the static display mode, the same signal is output to COM0 to COM3.

In the two-time-slice mode, leave the COM2 and COM3 pins open. In the three-time-slice mode, leave the COM3 pin open.

Table 44.6 COM signal

Number of time slices	COM0	COM1	COM2	COM3
Static display mode				
Two-time-slice mode			Open	Open
Three-time-slice mode				Open
Four-time-slice mode				

Note 1. Use the pins as open or segment pins.

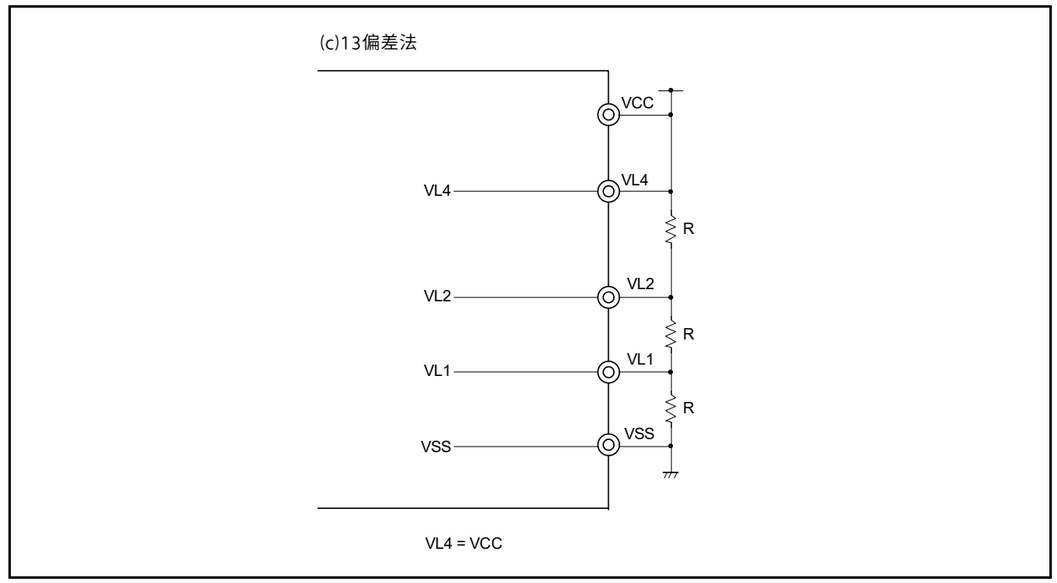


Figure 44.8 使用外部电阻分压法的LCD驱动电源连接示例(2of2)

Note: 外部电阻分压的参考电阻R值为10kΩ至1MΩ。此外，为了稳定VL1至VL4引脚的电压，根据需要在每个引脚VL1至VL4和GND引脚之间连接一个电容器。参考电容约为0.47μF，但取决于所使用的LCD面板、段引脚数、公共引脚数、帧频和操作环境。根据您的系统彻底评估这些值并调整电容。

44.8 通用和分段信号

当相应的公共信号和段信号之间的电位差高于特定电压（LCD驱动电压，VLCD）时，LCD面板的每个像素都会开启。当电位差低于VLCD时，像素关闭。

对LCD面板的公共信号和分段信号施加直流电压会导致劣化。为避免此问题，SLCDC由交流电压驱动。

(1) 常见信号

每个公共信号根据表44.6中列出的指定数量的时间片顺序选择。在静态显示模式下，相同的信号输出到COM0到COM3。

在两次分片模式下，将COM2和COM3引脚保持开路。在三时间片模式下，将COM3引脚保持打开状态。

Table 44.6 通讯信号

时间片数	COM0	COM1	COM2	COM3
静态显示方式				
Two-time-slice mode			Open	Open
Three-time-slice mode				Open
Four-time-slice mode				

Note 1. 将引脚用作开路或分段引脚。

(2) Segment signals

The segment signals correspond to the LCD display data register (see section 44.3, LCD Display Data Registers).

Bit [0] to bit [3] of each byte in A-pattern area are read in synchronization with COM0 to COM3, and bit [4] to bit [7] of each byte in B-pattern area are read in synchronization with COM0 to COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins.

Check what combination of front-surface electrodes (associated with the segment signals) and rear-surface electrodes (associated with the common signals) forms display patterns in the LCD display data register, and write the bit data associated with the desired display pattern on a one-to-one basis.

Note: The mounted segment output pins vary depending on the product.

(3) Output waveforms of common and segment signals

The voltages listed in Table 44.7 are output as common and segment signals.

When both common and segment signals are at the select voltage, display on-voltage is ±VLCD. Other combinations of the signals correspond to display off-voltage.

Table 44.7 LCD drive voltage

Static display mode

	Segment signal	
	Select signal level	**Deselect signal level**
Common signal	**VSS/VL4**	**VL4/VSS**
VL4/VSS	–VLCD/+VLCD	0 V/0 V

1/2 bias method

		Segment signal	
		Select signal level	**Deselect signal level**
Common signal		**VSS/VL4**	**VL4/VSS**
Select Signal Level	VL4/VSS	–VLCD/+VLCD	0 V/0 V
Deselect Signal Level	VL2	$-\frac{1}{2}$VLCD/+$\frac{1}{2}$VLCD	+$\frac{1}{2}$VLCD/–$\frac{1}{2}$VLCD

1/3 bias method (waveform A or B)

		Segment signal	
		Select signal level	**Deselect signal level**
Common signal		**VSS/VL4**	**VL2/VL1**
Select Signal Level	VL4/VSS	–VLCD/+VLCD	$-\frac{1}{3}$VLCD/+$\frac{1}{3}$VLCD
Deselect Signal Level	VL1/VL2	$-\frac{1}{3}$VLCD/+$\frac{1}{3}$VLCD	+$\frac{1}{3}$VLCD/–$\frac{1}{3}$VLCD

Figure 44.9 and Figure 44.10 show the common signal waveforms. Figure 44.11 to Figure 44.16 show the voltages and phases of the common and segment signals.

(2) 分段信号

段信号对应于LCD显示数据寄存器（参见第44.3节，LCD显示数据寄存器）。

A-pattern区每个字节的bit[0]-bit[3]与COM0-COM3同步读取，B-pattern区每个字节的bit[4]-bit[7]与COM0同步读取到COM3，分别。如果某位为1，则转换为选择电压，如果为0，则转换为取消选择电压。转换结果输出到段引脚。

检查LCD显示数据寄存器中的前表面电极（与段信号相关联）和后表面电极（与公共信号相关联）形成显示模式的组合，并将与所需显示模式相关联的位数据写入到一对一的基础。

Note: 安装的段输出引脚因产品而异。

(3) 公共和分段信号的输出波形

表44.7中列出的电压作为公共和分段信号输出。

当公共信号和段信号都处于选择电压时，显示导通电压为±VLCD。信号的其他组合对应于显示关断电压。

Table 44.7 液晶驱动电压

静态显示方式

	段信号	
	选择信号电平	**取消选择信号电平**
常用信号	**VSS/VL4**	**VL4/VSS**
VL4/VSS	–VLCD/+VLCD	0 V/0 V

12偏置法

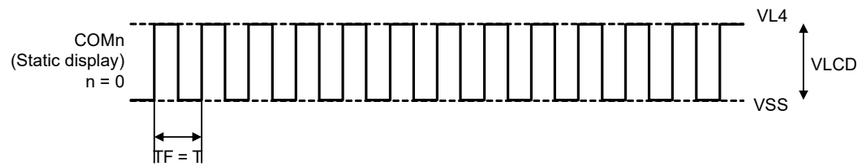
		段信号	
		选择信号电平	**取消选择信号电平**
常用信号		**VSS/VL4**	**VL4/VSS**
选择信号电平	VL4/VSS	–VLCD/+VLCD	0 V/0 V
取消选择信号电平	VL2	$-\frac{1}{2}$VLCD/+$\frac{1}{2}$VLCD	+$\frac{1}{2}$VLCD/–$\frac{1}{2}$VLCD

13偏置法（波形A或B）

		段信号	
		选择信号电平	**取消选择信号电平**
常用信号		**VSS/VL4**	**VL2/VL1**
选择信号电平	VL4/VSS	–VLCD/+VLCD	$-\frac{1}{3}$VLCD/+$\frac{1}{3}$VLCD
取消选择信号电平	VL1/VL2	$-\frac{1}{3}$VLCD/+$\frac{1}{3}$VLCD	+$\frac{1}{3}$VLCD/–$\frac{1}{3}$VLCD

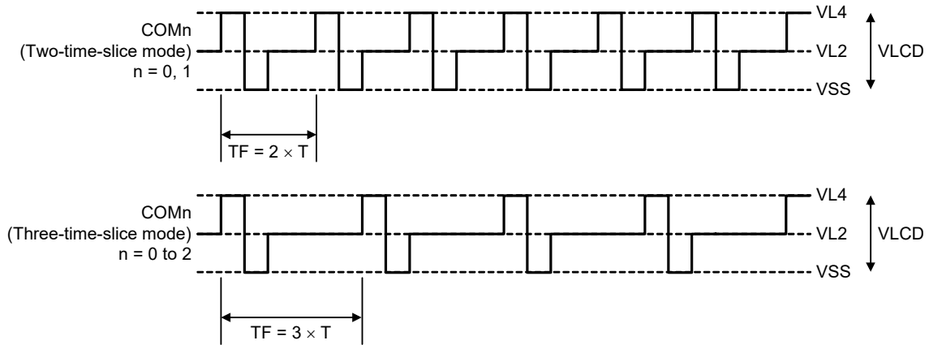
图44.9和图44.10显示了常见的信号波形。图44.11至图44.16显示了公共和分段信号的电压和相位。

(a) Static display mode



T: One LCD clock period TF: Frame period

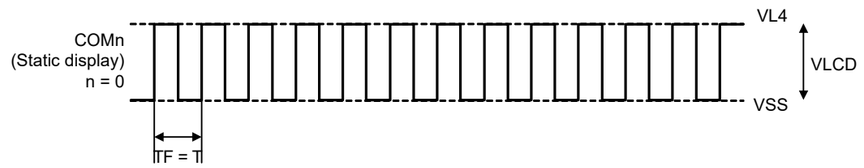
(b) 1/2 bias method



T: One LCD clock period TF: Frame period

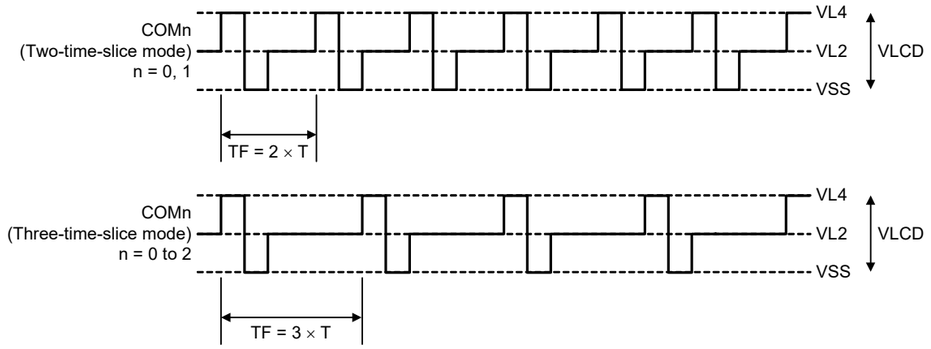
Figure 44.9 Common signal waveforms (1 of 2)

(a)静态显示方式



T：一个LCD时钟周期TF：帧周期

(b)12偏差法



T：一个LCD时钟周期TF：帧周期

Figure 44.9 常见信号波形(1of2)

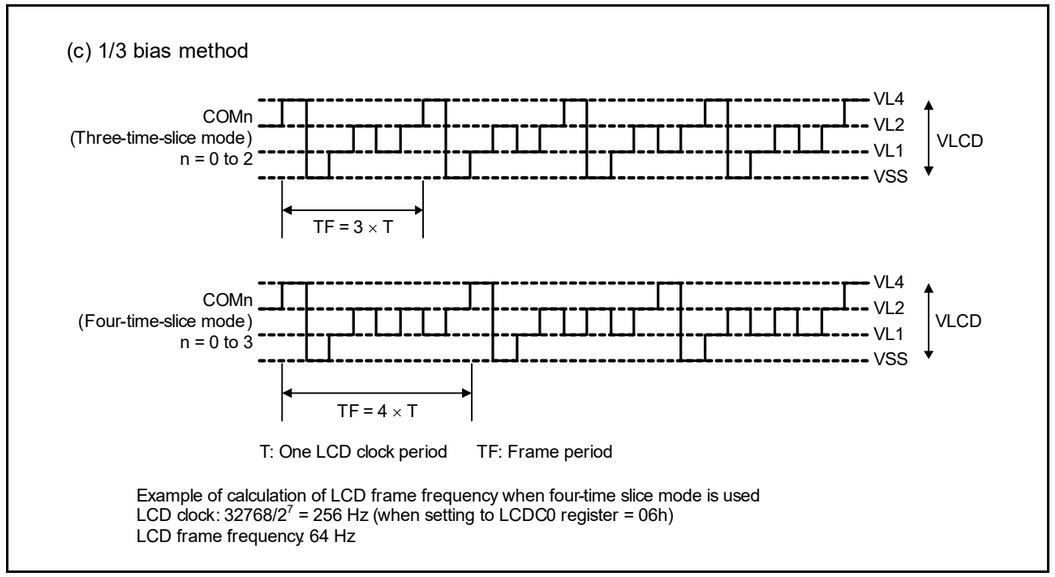


Figure 44.10 Common signal waveforms (2 of 2)

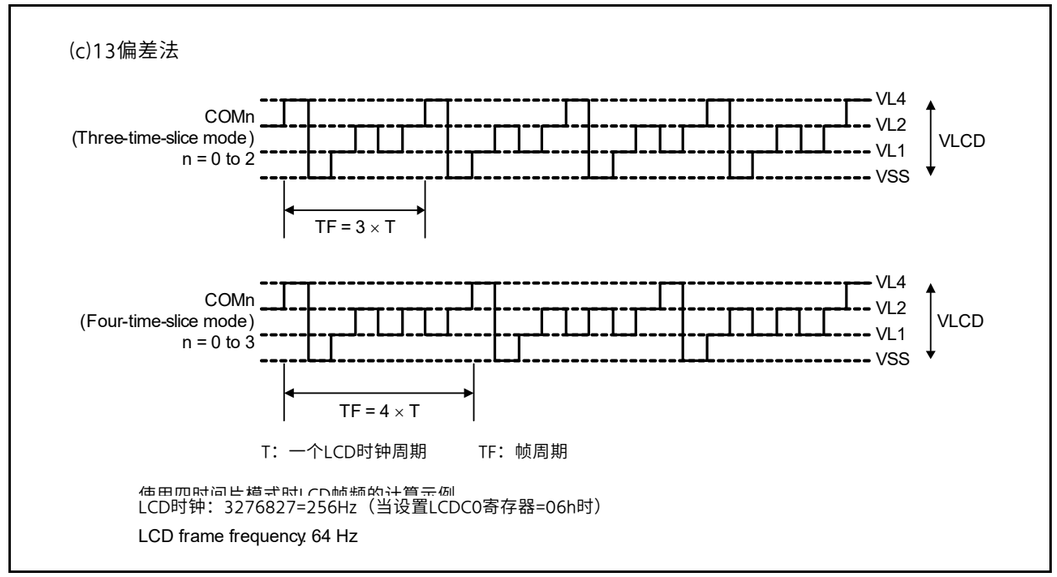
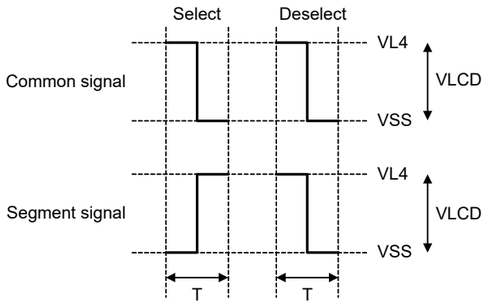


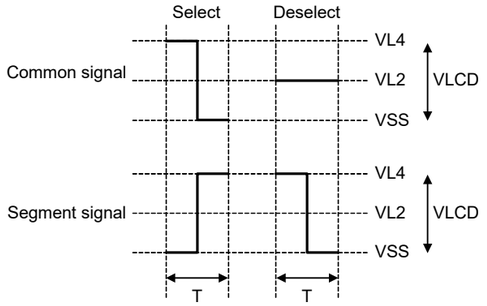
Figure 44.10 常见信号波形(2of2)

(a) Static display mode (waveform A)



T: One LCD clock period

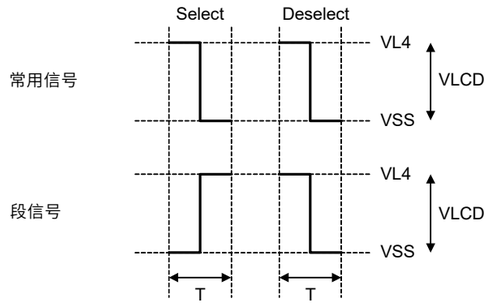
(b) 1/2 bias method (waveform A)



T: One LCD clock period

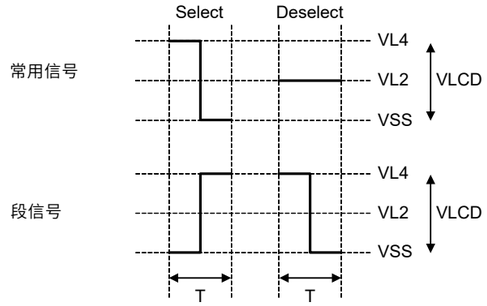
Figure 44.11 Voltages and phases of common and segment signals (1 of 3)

(a)静态显示模式（波形A）



T：一个LCD时钟周期

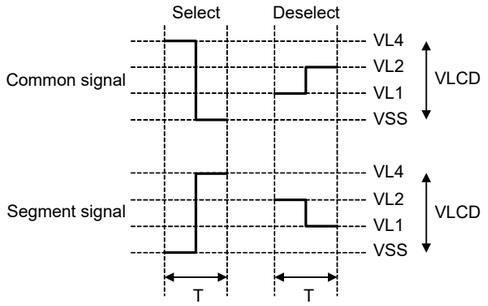
(b)12偏压法（波形A）



T：一个LCD时钟周期

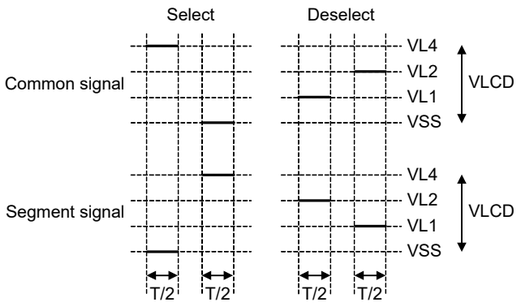
Figure 44.11 公共和分段信号的电压和相位(1of3)

(c) 1/3 bias method (waveform A)



T: One LCD clock period

(d) 1/3 bias method (waveform B)



T: One LCD clock period

Figure 44.12 Voltages and phases of common and segment signals (2 of 3)

44.9 Display Modes

44.9.1 Four-Time-Slice Display Example

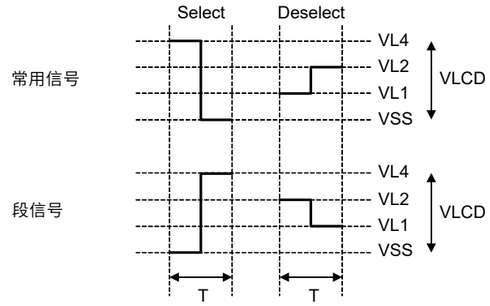
Figure 44.14 shows how a 12-digit LCD panel with the display pattern shown in Figure 44.13 is connected to the segment signals and the common signals (COM0 to COM3). This example displays "56.78" in the LCD panel. The contents of the display data register correspond to this display.

The following description focuses on numeral "6." ( ) displayed in the seventh digit. To display "6." in the LCD panel, the select or deselect voltage must be applied to the SEG20 and SEG23 pins at the select timing of the common signals COM0 to COM3. See Figure 44.13 for the relationship between the segment signals and LCD segments.

Table 44.8 Example of select (1) and deselect (0) data (COM0 to COM3) (1 of 2)

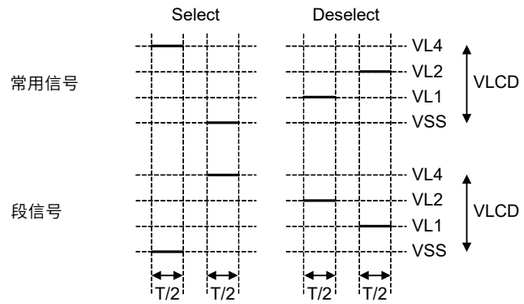
	Segment	
Common	**SEG20**	**SEG23**
COM0	Select	Select

(c)13偏置法（波形A）



T：一个LCD时钟周期

(d)13偏置法（波形B）



T：一个LCD时钟周期

Figure 44.12 公共和分段信号的电压和相位(2of3)

44.9 显示模式

44.9.1 四时间片显示示例

图44.14显示了具有图44.13所示显示模式的12位LCD面板如何连接到段信号和公共信号（COM0到COM3）。此示例在LCD面板中显示"56.78"。显示数据寄存器的内容与该显示相对应。

以下描述集中在数字"6"上。()显示在第七位。显示"6"。在LCD面板中，选择或取消选择电压必须在公共信号COM0到COM3的选择时序上施加到SEG20和SEG23引脚。段信号和LCD段之间的关系见图44.13。

Table 44.8 选择(1)和取消选择(0)数据(COM0到COM3)的示例(1of2)

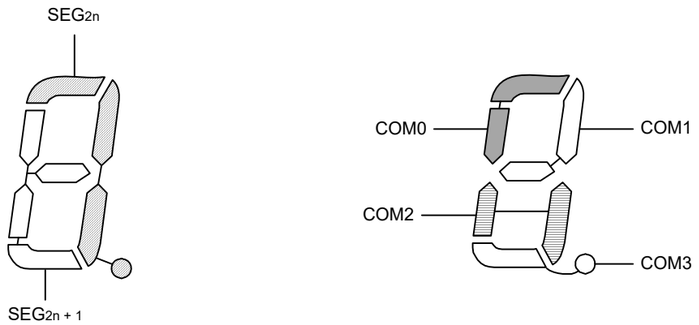
	Segment	
Common	**SEG20**	**SEG23**
COM0	Select	Select

Table 44.8 Example of select (1) and deselect (0) data (COM0 to COM3) (2 of 2)

	Segment	
Common	**SEG20**	**SEG23**
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 44.8, the display data register location that corresponds to SEG20 must contain "1101b".

Figure 44.15 shows examples of LCD drive waveforms between the SEG20 signal and each common signal. When the select voltage is applied to SEG20 at the timing of COM0, an alternating rectangle waveform, +VLCD/–VLCD, is generated to turn on the associated LCD segment.



Note: The mounted segment output pins vary depending on the product.

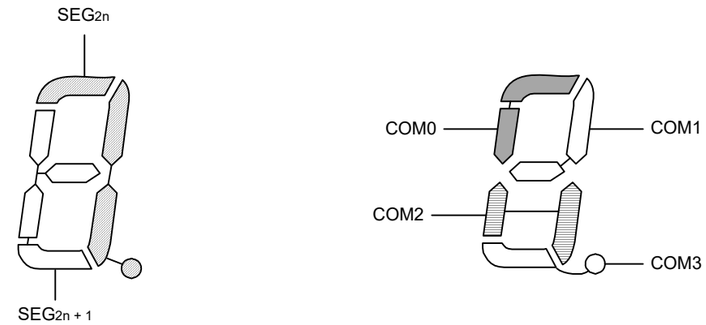
Figure 44.13 Four-time-slice LCD display pattern and electrode connections

Table 44.8 选择(1)和取消选择(0)数据(COM0到COM3)的示例(2of2)

	Segment	
Common	**SEG20**	**SEG23**
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

根据表44.8，SEG20对应的显示数据寄存器位置必须包含"1101b"。

图44.15显示了SEG20信号和每个公共信号之间的LCD驱动波形示例。当在COM0的时间安排将选择电压应用于SEG20时，生成交替的矩形波形+VLCD VLCD，以打开相关的LCD段。



Note: 安装的段输出引脚因产品而异。

Figure 44.13 四时间片LCD显示模式和电极连接

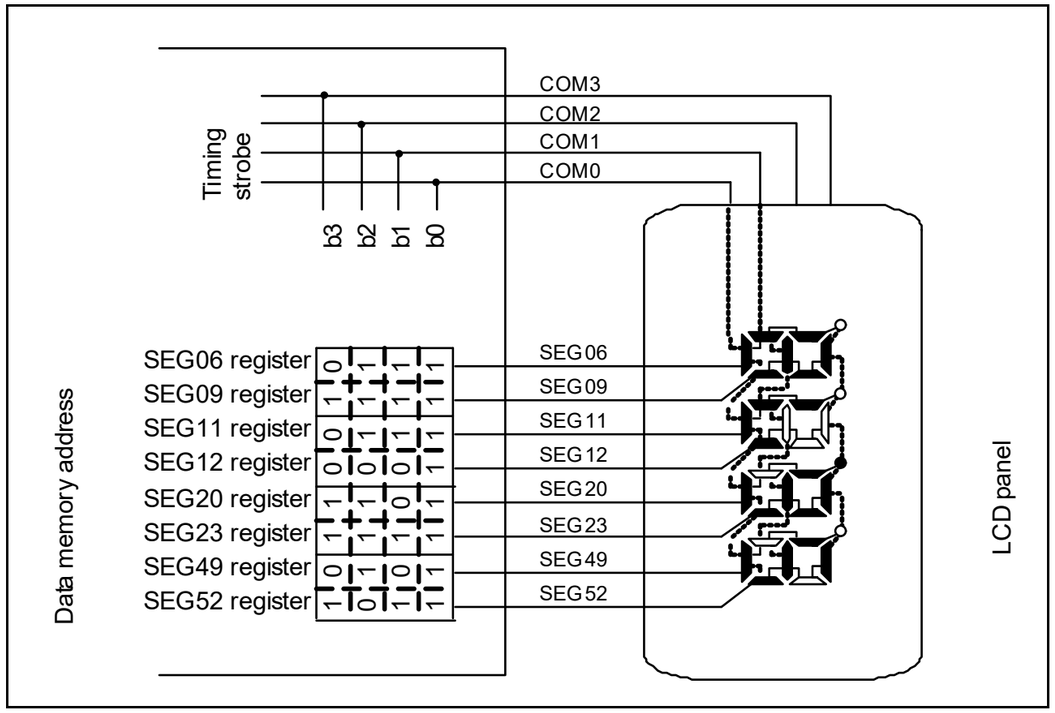


Figure 44.14 Example for connecting four-time-slice LCD panel

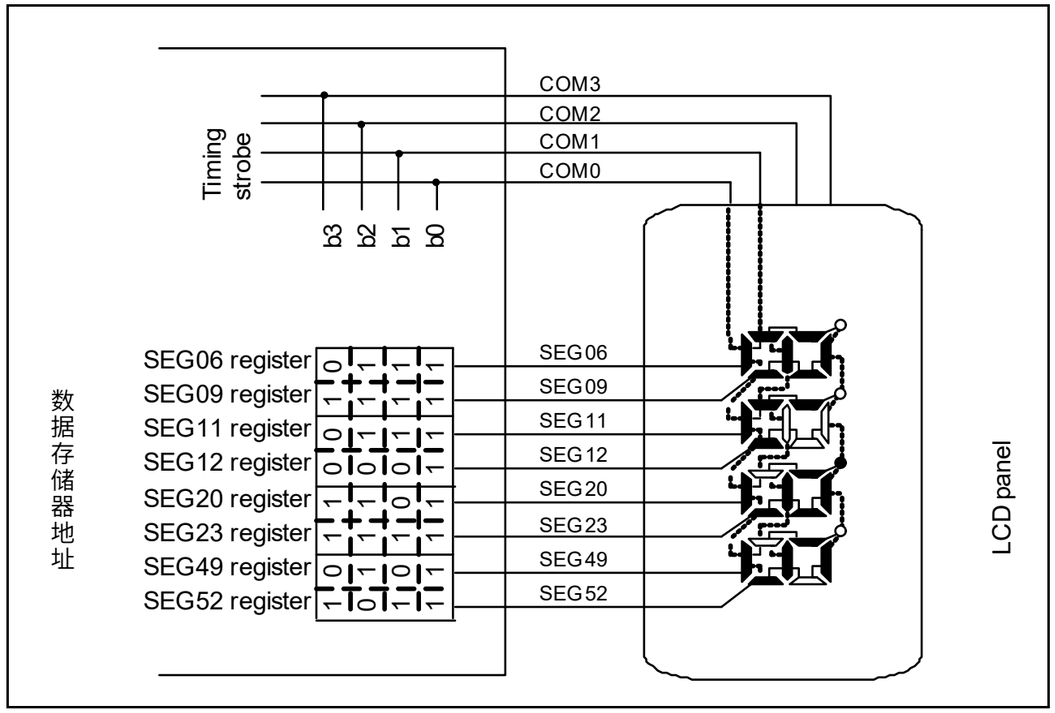


Figure 44.14 四倍片液晶面板连接示例

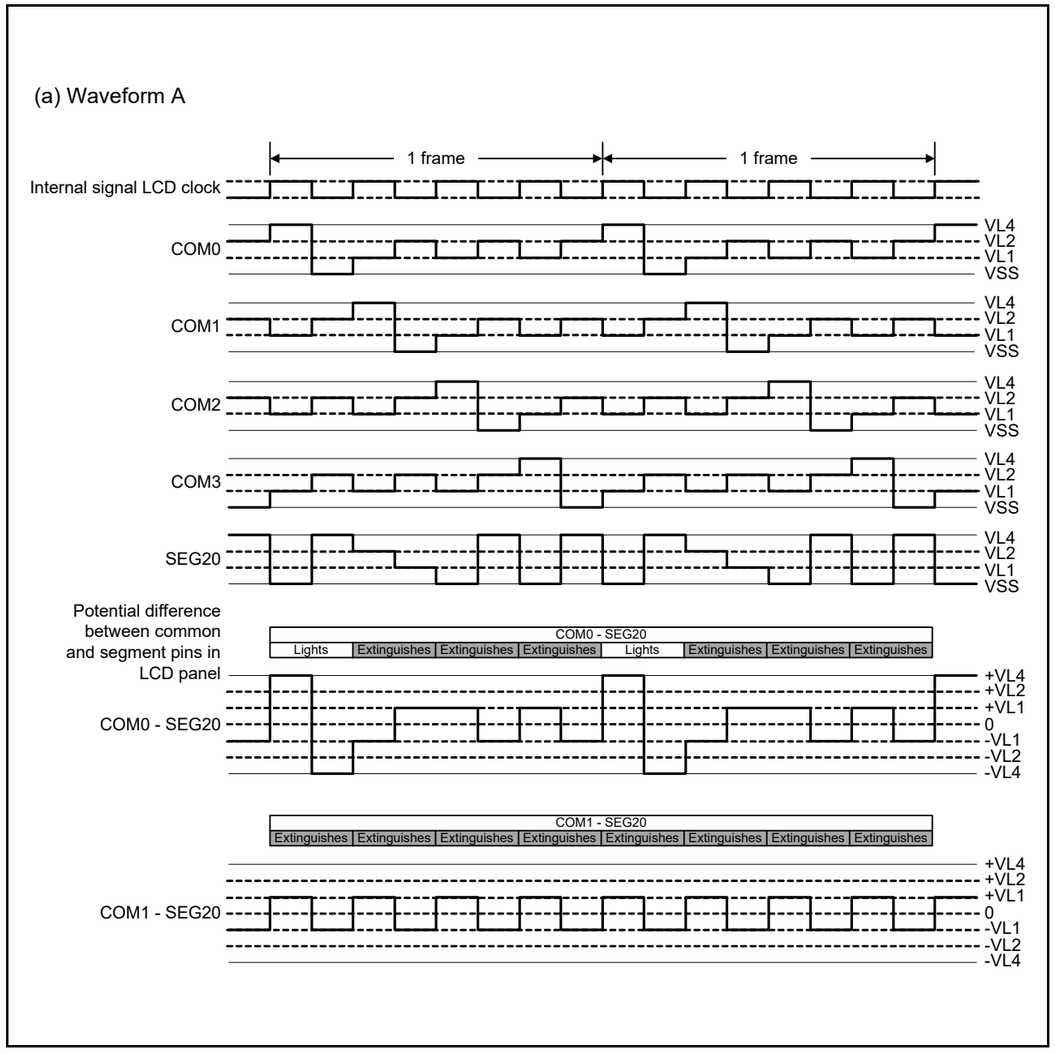


Figure 44.15 Four-time-slice LCD drive waveform examples between SEG20 and each common signal using 1/3 bias method (1 of 2)

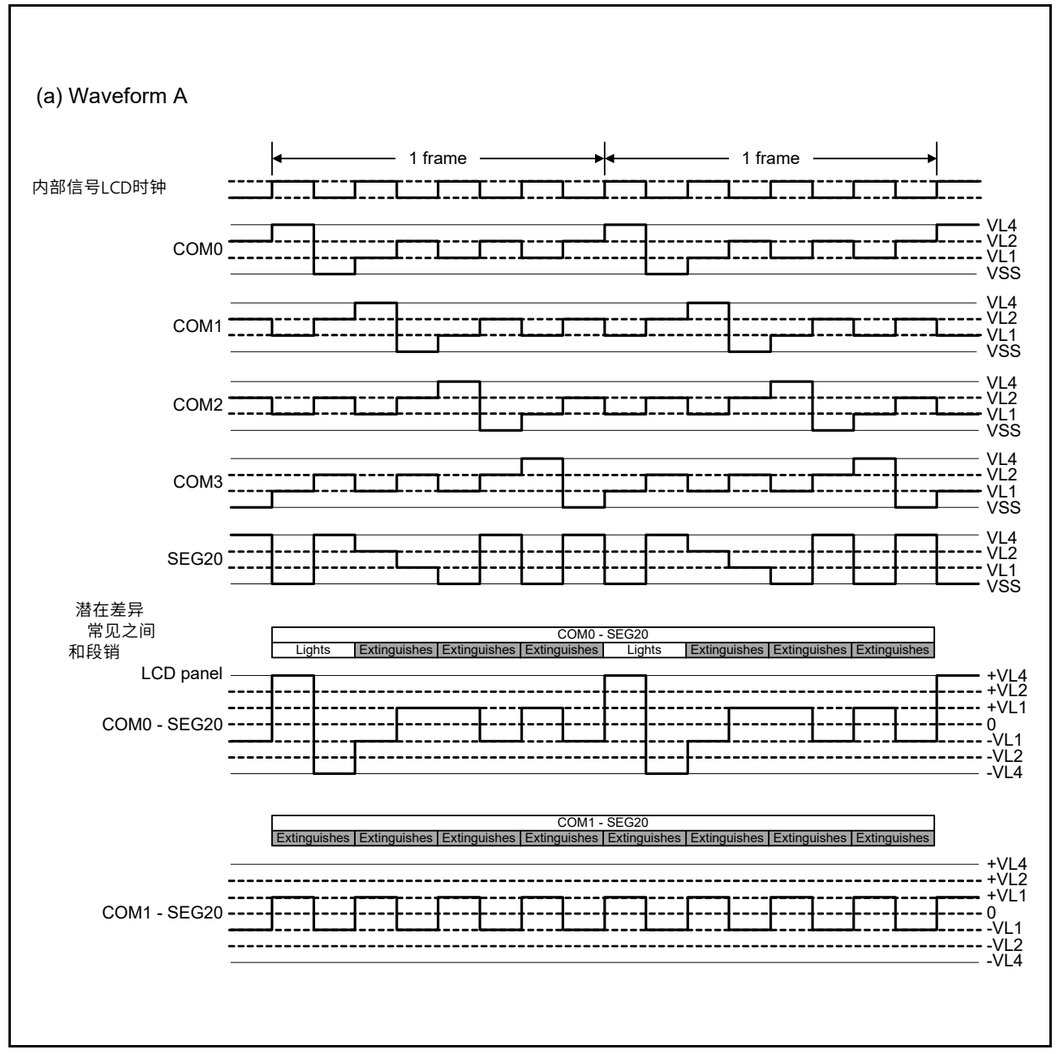


Figure 44.15 SEG20和使用13偏置方法的每个公共信号之间的四时间片LCD驱动波形示例(1of2)

(b) Waveform B

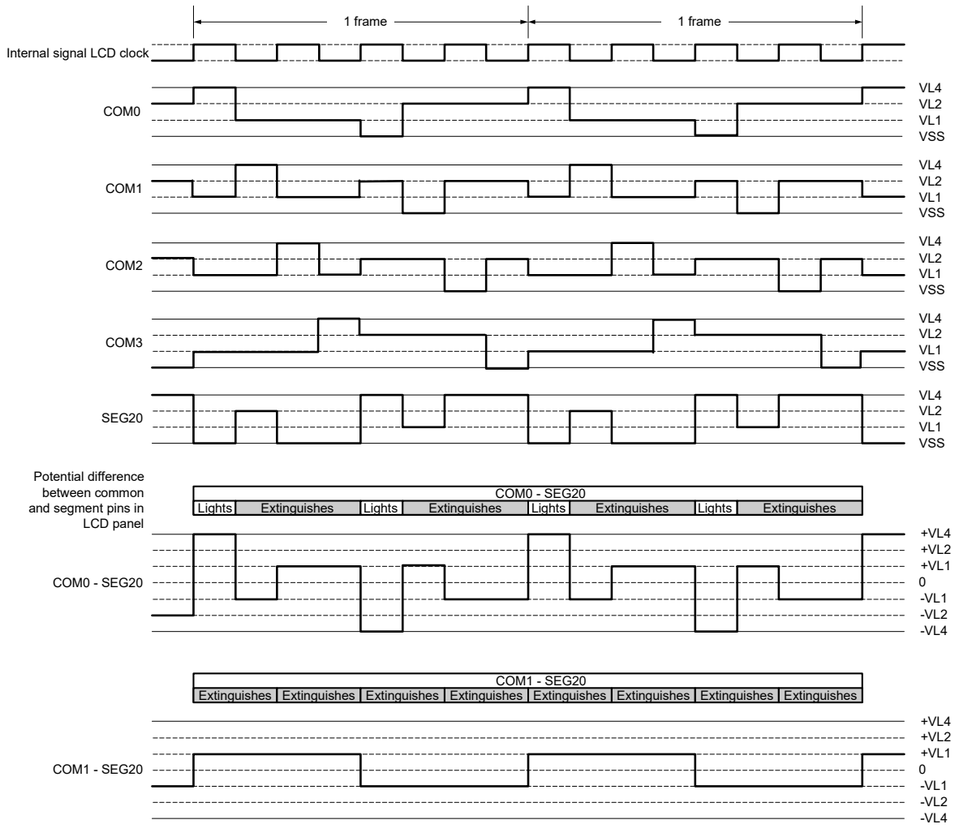


Figure 44.16 Four-time-slice LCD drive waveform examples between SEG12 and each common signal using 1/3 bias method (2 of 2)

(b) Waveform B

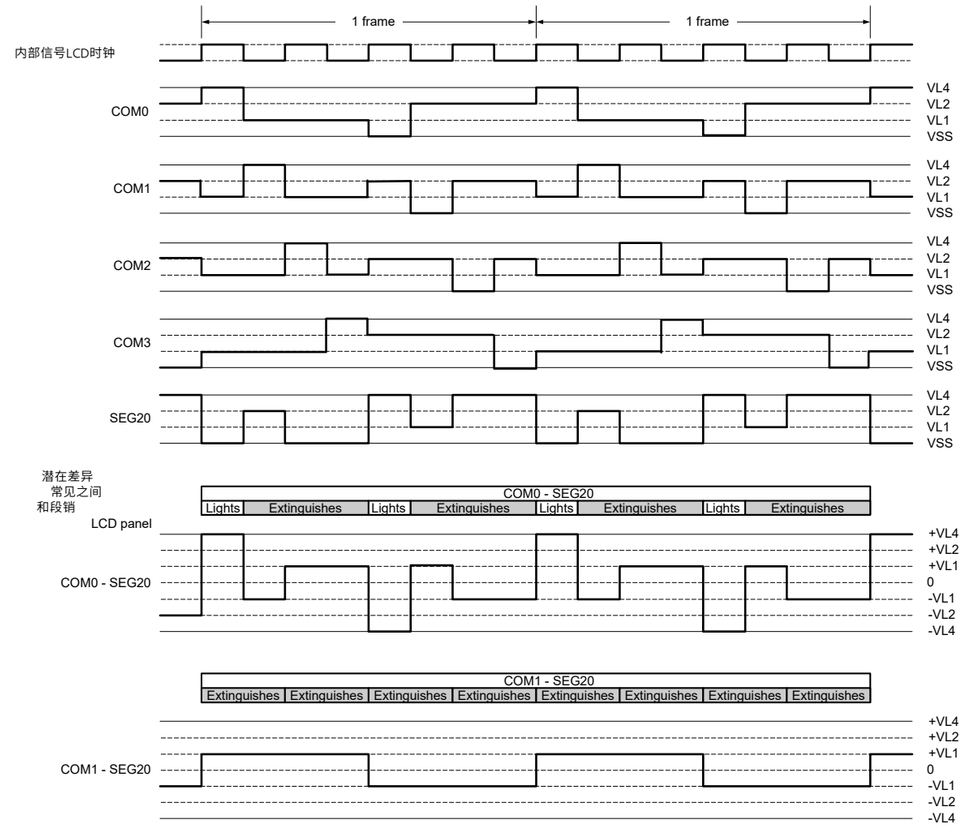


Figure 44.16 SEG12和使用13偏置方法的每个公共信号之间的四时间片LCD驱动波形示例(2of2)

45. Secure Cryptographic Engine (SCE5)

45.1 Overview

The MCU incorporates a Secure Cryptographic Engine (SCE5) module to provide security functions. The module consists of an access management circuit, encryption engine, and random number generator.

Table 45.1 shows the SCE5 specifications and Figure 45.1 shows the SCE5 block diagram.

Table 45.1 SCE5 specifications

Item	Description
Access control	Access management circuit • In case of irregular access to the SCE5 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE5.
Encryption engine	Advanced Encryption Standard (AES): Compliant with NIST FIPS PUB 197 algorithm • Key sizes: 128 or 256 bits • Block size: 128 bits • Chaining modes - ECB, CBC, CTR: Compliant with NIST SP 800-38A - GCM: Compliant with NIST SP 800-38D - XTS: Compliant with NIST SP 800-38E. - GCTR • Throughput for 128-bit data - 44 PCLKA cycles for 128-bit key - 61 PCLKA cycles for 256-bit key. AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Key management • Wrapped keys are only valid within the SCE5.
Generation of random numbers	32-bit true random number generator
Unique ID	• An ID unique to the MCU (unique ID) is accessible from the access management circuit through the dedicated bus • Combining the unique ID with the key generation information prevents illicit copying of data to another MCU.
Privileged mode	• The privileged mode access signal is connected to the access management circuit and is used to limit control of the SCE5 module to privileged mode only.
Low power consumption	Setting of the module-stop state is possible

45. 安全加密引擎(SCE5)

45.1 Overview

MCU包含一个安全加密引擎(SCE5)模块以提供安全功能。该模块由访问管理电路、加密引擎和随机数发生器组成。

表45.1显示了SCE5规范，图45.1显示了SCE5框图。

Table 45.1 SCE5 specifications

Item	Description
访问控制	访问管理电路　如果由于伪造程序或程序执行失控导致对SCE5的非正常访问，该电路将阻止所有后续访问，并停止从SCE5输出数据。
加密引擎	高级加密标准(AES)：符合NISTFIPSPUB197算法　密钥大小：128或256位　块大小：128位　链接模式 ECB、CBC、CTR：符合NISTSP800-38AGCM：符合NISTSP800-38DXTS：符合NISTSP800-38E。GCTR　128位数据的吞吐量 128位密钥44个PCLKA周期256位密钥61个PCLKA周期。 AES-GCM　AES-GCM是通过结合AES-GCTR和GHASH实现的。 密钥管理　封装密钥仅在SCE5内有效。
随机数的产生	32位真随机数发生器
唯一身份	MCU唯一的ID（唯一ID）可通过专用总线从访问管理电路访问　将唯一ID与密钥生成信息相结合可防止将数据非法复制到另一个MCU。
特权模式	特权模式访问信号连接到访问管理电路，用于将SCE5模块的控制仅限于特权模式。
低功耗	可以设置模块停止状态

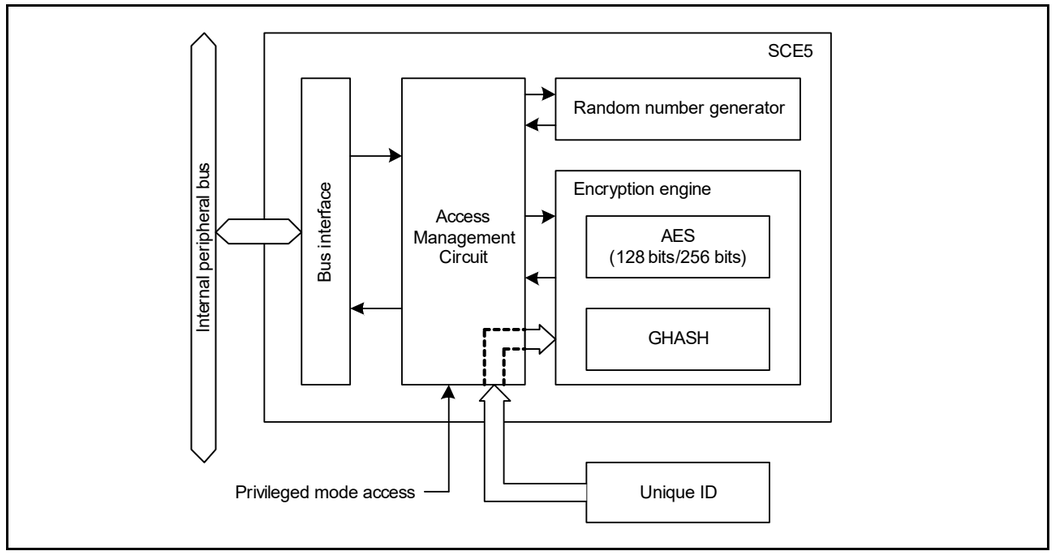


Figure 45.1 SCE5 block diagram

45.2 Operation

45.2.1 Encryption Engine

The encryption engine performs the following operation in hardware, as shown in Figure 45.2:

- Plaintext to ciphertext encryption
- Ciphertext to plaintext decryption.

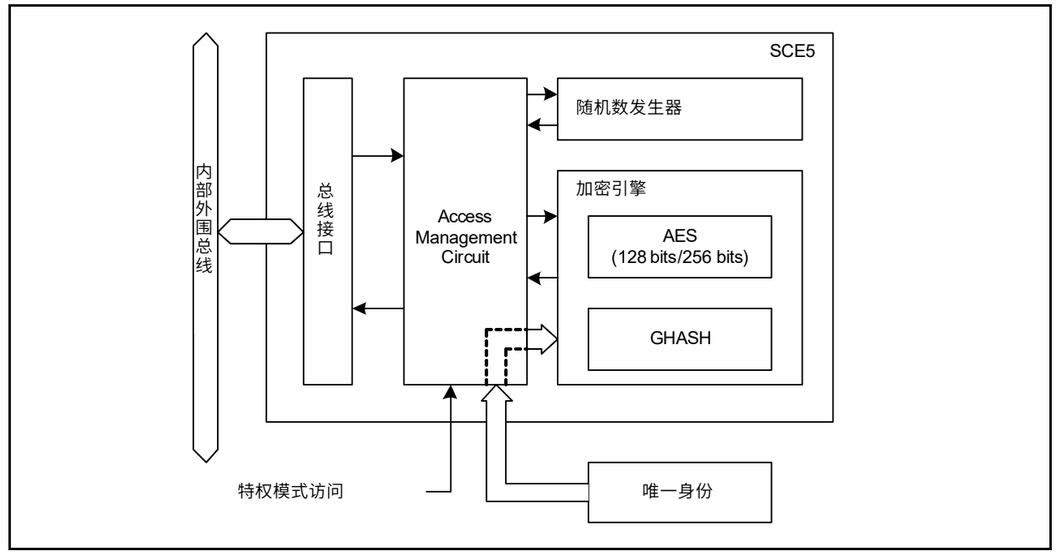


Figure 45.1 SCE5框图

45.2 Operation

45.2.1 加密引擎

加密引擎在硬件上执行以下操作，如图45.2所示：

- 明文到密文加密
- 密文转明文解密。

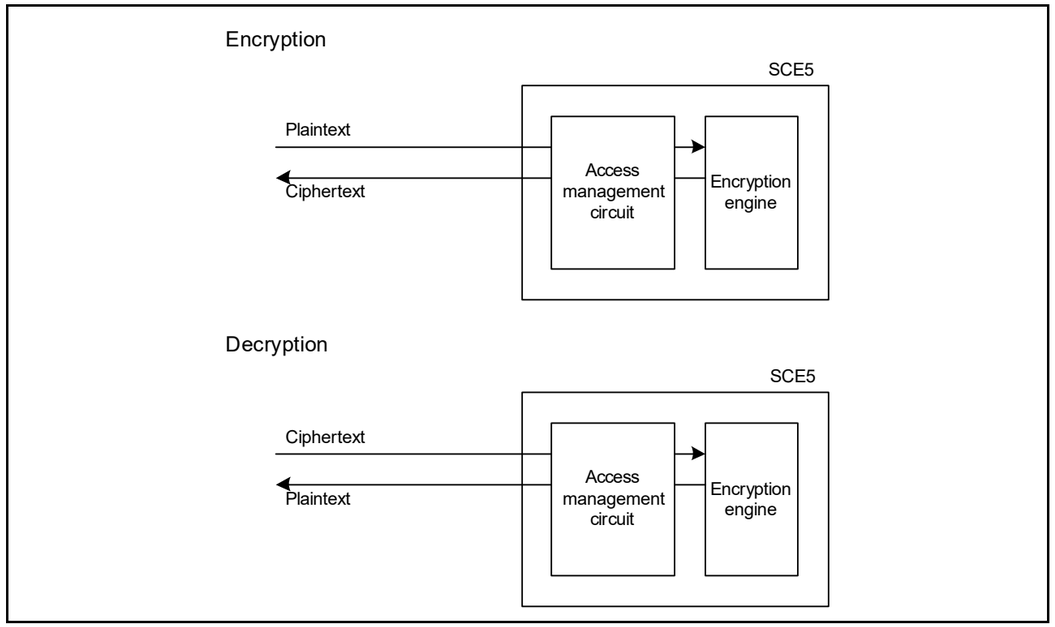


Figure 45.2 Encryption and decryption processes by encryption engine

45.2.2 Encryption and Decryption

To encrypt or decrypt data:

1. Input the data to encrypt or decrypt in the SCE5.
   The SCE5 converts the plaintext data to ciphertext or ciphertext data to plaintext.
2. Read the converted data.

The encryption engine has an input buffer and an output buffer, enabling encryption/decryption to proceed in parallel with data input/output. Figure 45.3 shows the encryption engine timing.

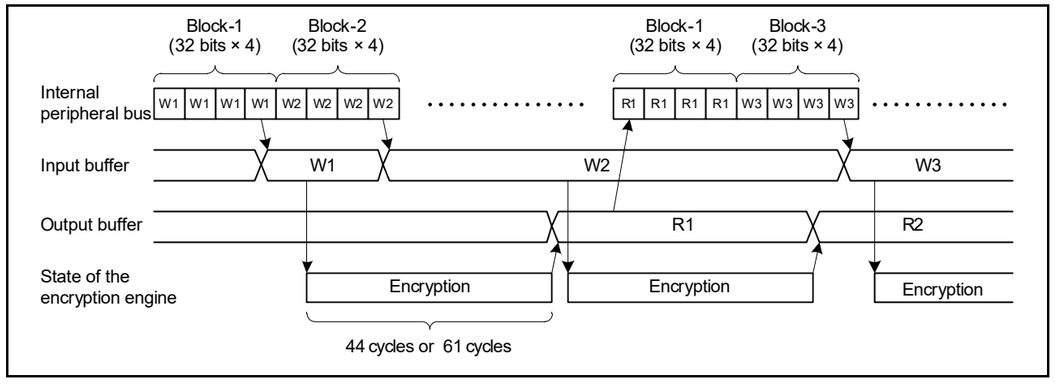


Figure 45.3 Encryption and decryption timing (AES)

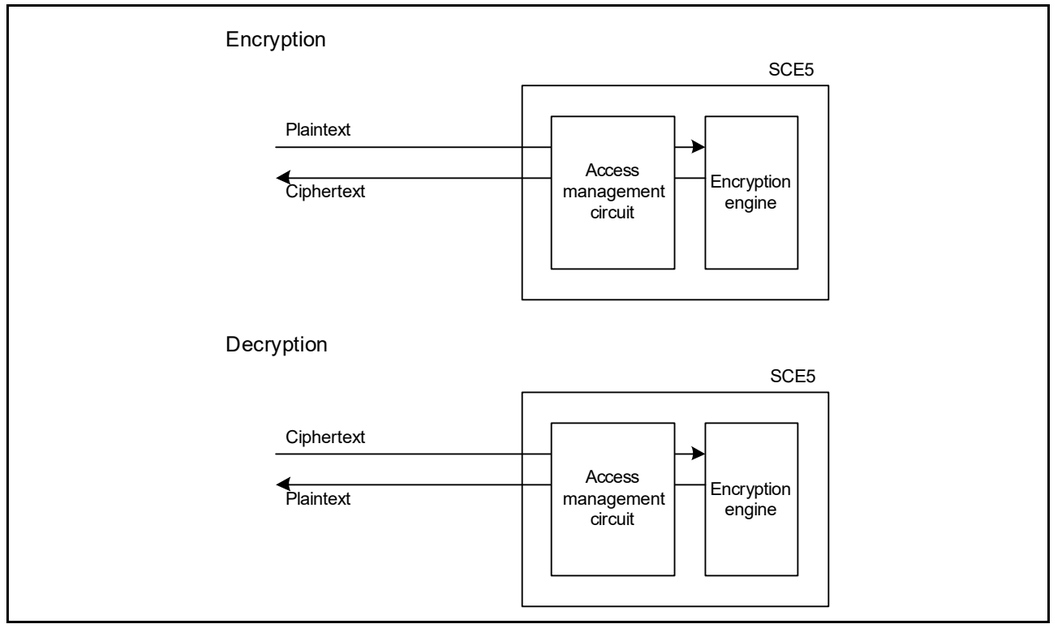


Figure 45.2 加密引擎的加解密过程

45.2.2 加密和解密

要加密或解密数据：

1. 在SCE5中输入要加密或解密的数据。
   SCE5将明文数据转换为密文或将密文数据转换为明文。
2. 读取转换后的数据。

加密引擎有一个输入缓冲区和一个输出缓冲区，使加密解密与数据输入输出并行进行。图45.3显示了加密引擎的时序。

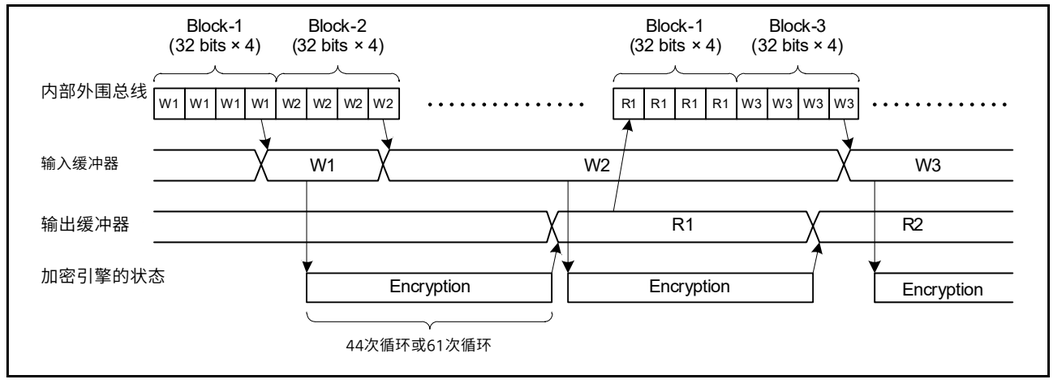


Figure 45.3 加密和解密时序（AES）

45.3 Usage Notes

45.3.1 Software Standby Mode

If the MCU enters Software Standby mode while the encryption engine is processing, proper processing cannot be resumed after exiting Software Standby mode. Therefore, it is necessary to enter Software Standby mode while the encryption engine is not running.

45.3.2 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable SCE5 operation. The SCE5 module is initially stopped after reset. Releasing the module-stop state enables access to the registers.

45.3 使用说明

45.3.1 软件待机模式

如果MCU在加密引擎正在处理时进入软件待机模式，则退出软件待机模式后无法恢复正常处理。因此，必须在加密引擎未运行时进入软件待机模式。

45.3.2 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用SCE5操作。SCE5模块在复位后最初停止。释放模块停止状态可以访问寄存器。

46. Bluetooth Low Energy (BLE)

This MCU has a Bluetooth Low Energy (BLE), which consists of an RF transceiver compliant with Bluetooth 5.0 Low Energy (single mode), a link layer, and an RF transceiver power-supply.

The BLE is controlled by a Bluetooth middlewear available from Renesas Electronics Corporation.

46.1 Overview

Table 46.1 lists the Specifications of the BLE. Figure 46.1 is a BLE Block Diagram.

Table 46.1 Specifications of the BLE

Item	Description		
Features	• RF transceiver compliant with the Bluetooth 5.0 Low Energy specification and a link layer • An on-chip matching circuit allows reducing the number of external parts • On-chip BLE-dedicated high-precision low-speed oscillator (32.768 kHz) • Transmission power is selectable as 0 dBm or +4 dBm. • The minimum receiving sensitivity is selectable from among –105 dBm (125 kbps), –100 dBm (500 kbps), –95 dBm (1 Mbps), or –92 dBm (2 Mbps).		
Bluetooth 5.0 functions	Classification	Function	Remark
	Device Address	Public or random address	The address can be set as a desired address.
	Advertising	Extended or periodic	
		Multiple advertising	Maximum number of sets: 4
		Advertising or Scan Response Data	Maximum data length=1650 bytes
	Scanning	Passive, active, or periodic	Number of units for concurrent synchronization with periodic advertising=2
		Whitelist or periodic advertiser list	Number of units registered in the whitelist: 4 Number of units registered in the periodic advertiser list: 4
	Master or slave	Data transmission or reception	Maximum payload length=251 bytes MoreData function is supported. Master/slave multi-role function is supported.
	Other	Bit rates	125 kbps, 500 kbps, 1 Mbps, 2 Mbps Bit-rate combinations for transmission and reception can be set as desired.
		Frequency hopping	Channel Selection Algorithm #2
		Encryption circuit for Bluetooth	On-chip Bluetooth-dedicated AES-CCM (128 bits) circuit
Other functions	RF transceiver power-supply (DC-to-DC converter, and linear regulator)		

46. 低功耗蓝牙(BLE)

该MCU具有蓝牙低功耗(BLE)，由符合蓝牙5.0Low的RF收发器组成
能量（单模）、链路层和射频收发器电源。

BLE由RenesasElectronicsCorporation提供的蓝牙中间件控制。

46.1 Overview

表46.1列出了BLE的规格。图46.1是一个BLE框图。

Table 46.1 BLE的规格

Item	Description		
Features	符合低功耗蓝牙5.0规范的射频收发器和链路层 片上匹配电路可减少外部部件数量 片上BLE专用高精度低速振荡器（32.768kHz） 传输功率可选择为0dBm或+4dBm。 最小接收灵敏度可从 105dBm(125kbps)、 100dBm(500kbps)、 95dBm(1Mbps)或 92dBm(2Mbps)中选择。		
蓝牙5.0功能	Classification	Function	Remark
	设备地址	公共或随机地址	该地址可以设置为所需的地址。
	Advertising	延长或定期	
		多重广告	最大套数：4
		广告或扫描响应 Data	最大数据长度=1650字节
	Scanning	被动、主动或周期性	周期性广播的并发同步单元数=2
		白名单或定期广告客户名单	白名单注册单位数：4 定期广告客户列表中注册的单位数量：4
	主人或奴隶	数据传输或接收	最大有效载荷长度=251字节 支持更多数据功能。 支持主从多角色功能。
	Other	比特率	125kbps、500kbps、1Mbps、2Mbps可以 根据需要设置发送和接收的比特率组合。
		跳频	频道选择算法#2
		蓝牙加密电路	On-chip Bluetooth-dedicated AES-CCM (128 bits) circuit
其他功能	RF收发器电源（DC-DC转换器和线性稳压器）		

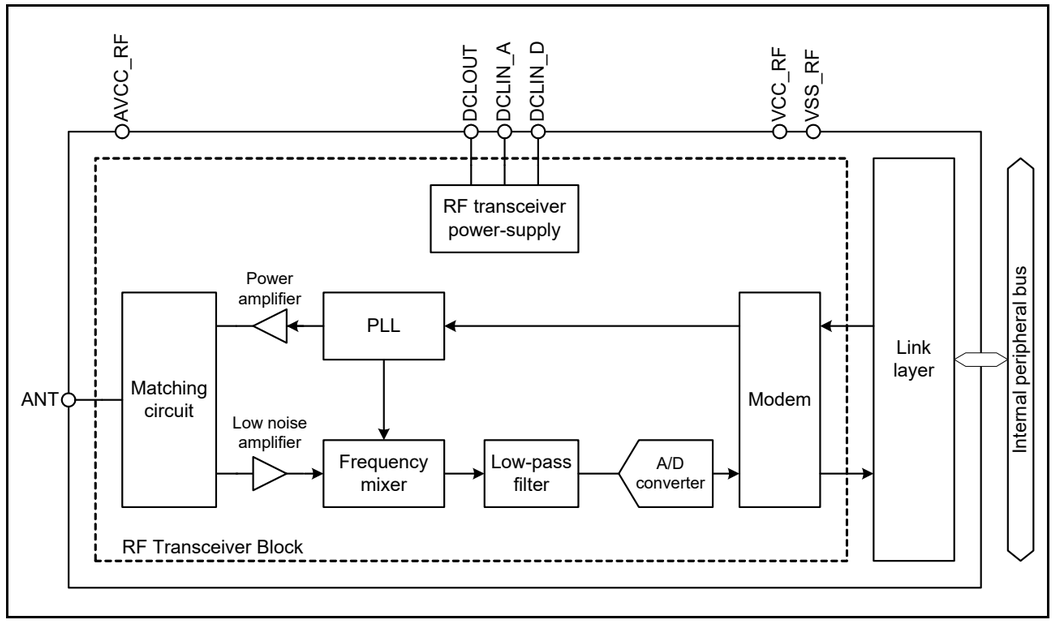


Figure 46.1 BLE Block Diagram

Table 46.2 lists the BLE I/O Pins.

Table 46.2 BLE I/O Pins

Pin name	I/O	Description
ANT	I/O	RF single I/O pin for RF transceiver Set the impedance of the signal line to 50 Ω.
DCLOUT	Output	Output pin for the RF transceiver power-supply
DCLIN_A, DCLIN_D	Input	If the DC-to-DC converter is to be selected as the power supply for the RF transceiver, connect an inductor and capacitor between the DCLOUT pin and the converter. If the linear regulator is to be selected as the power supply for the RF transceiver, connect a capacitor between the DCLOUT pin and the converter.
VCC_RF	Input	RF transceiver power-supply pin
AVCC_RF	Input	RF transceiver power-supply pin
VSS_RF	Input	RF transceiver ground pin

Table 46.3 lists the Bluetooth Low Energy functions that this MCU supports. The use of these functions requires the Bluetooth middleware.

Table 46.3 List of Supported Bluetooth Low Energy Functions (1 of 2)

Function	Bluetooth® core spec
Low Energy Controller (PHY and LL)	v4.0
Low Energy Host (L2CAP and Security Manager)	
Attribute Protocol and Generic Attribute Profile	

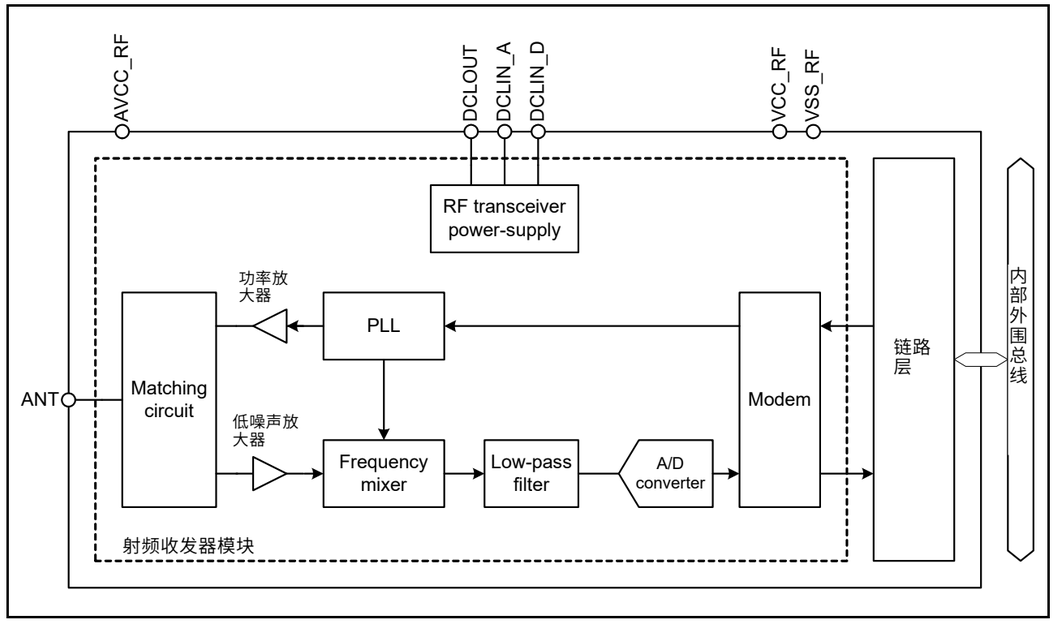


Figure 46.1 BLE框图

表46.2列出了BLEIO引脚。

Table 46.2 BLEIO引脚

引脚名称	I/O	Description
ANT	I/O	RF收发器的RF单IO引脚 将信号线的阻抗设置为50Ω。
DCLOUT	Output	RF收发器电源的输出引脚
DCLIN_A, DCLIN_D	Input	如果要选择DC-DC转换器作为RF收发器的电源，请在DCLOUT引脚和转换器之间连接一个电感器和电容器。如果要选择线性稳压器作为RF收发器的电源，请在DCLOUT引脚和转换器之间连接一个电容器。
VCC_RF	Input	射频收发器电源引脚
AVCC_RF	Input	射频收发器电源引脚
VSS_RF	Input	射频收发器接地引脚

表46.3列出了该MCU支持的蓝牙低功耗功能。使用这些功能需要
Bluetooth middleware.

Table 46.3 支持的蓝牙低功耗功能列表（2个中的1个）

Function	蓝牙®核心规格
低能耗控制器（PHY和LL）	v4.0
低能耗主机（L2CAP和安全管理器）	
属性协议和通用属性配置文件	

Table 46.3 List of Supported Bluetooth Low Energy Functions (2 of 2)

Function	Bluetooth® core spec
Appearance Data Type	v4.1
Low Duty Cycle Directed Advertising	
32-bit UUID Support in LE	
LE L2CAP Connection Oriented Channel Support	
LE Link Layer Topology	
LE Ping	
LE Data Packet Length Extension	v4.2
LE Secure Connections	
Link Layer Privacy	
Link Layer Extended Filter Policies	
LE 2M PHY	v5.0
LE Coded PHY	
High Duty Cycle Non-Connectable Advertising	
LE Advertising Extensions	
LE Channel Selection Algorithm #2	

46.2 Operation

46.2.1 State Transitions

Figure 46.2 is the State Transition Diagram of the BLE.

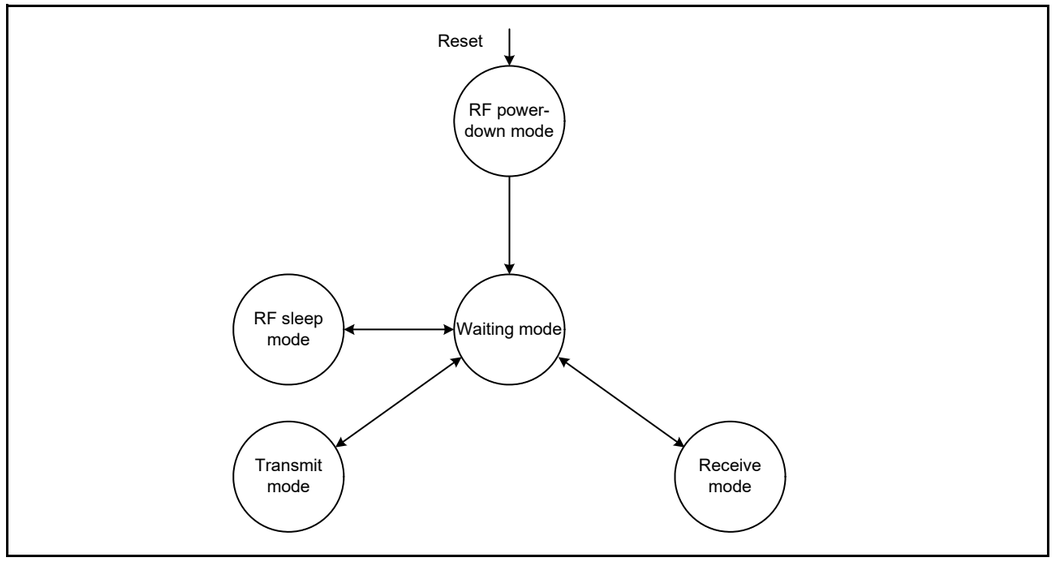


Figure 46.2 State Transition Diagram of the BLE

RF Power-Down Mode

The RF power-down mode is the initial mode of the BLE after release from the reset state.

Power is supplied to the MCU, but not to the RF transceiver.

Table 46.3 支持的蓝牙低功耗功能列表（2个中的2个）

Function	蓝牙®核心规格
外观数据类型	v4.1
低占空比定向广告	
LE中的32位UUID支持	
LEL2CAP面向连接的通道支持	
LE链路层拓扑	
乐平	
LE数据包长度扩展	v4.2
LE安全连接	
链路层隐私	
链路层扩展过滤策略	
LE 2M PHY	v5.0
LE编码PHY	
高占空比不可连接广告	
LE广告扩展	
LE频道选择算法#2	

46.2 Operation

46.2.1 状态转换

图46.2是BLE的状态转换图。

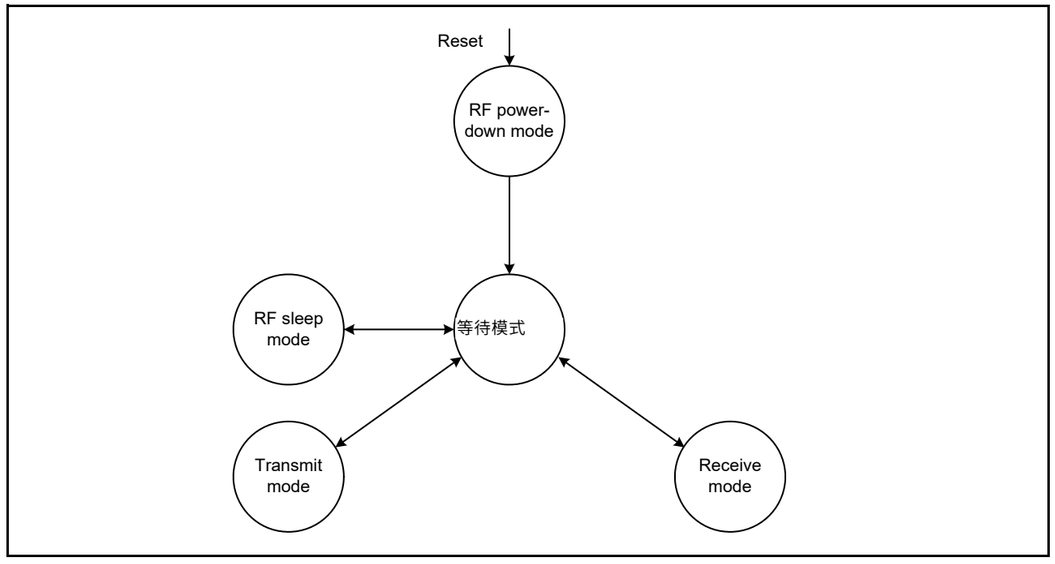


Figure 46.2 BLE的状态转换图

RF Power-Down Mode

RF掉电模式是BLE从复位状态释放后的初始模式。

向MCU供电，但不向RF收发器供电。

Waiting Mode

In waiting mode, the BLE waits until the transmission or reception of data or a transition to sleep mode is requested.

RF Sleep Mode

The RF sleep mode is a low-power operating mode and the power supply, except to part of the link-layer circuit, is stopped.

Transmit Mode

The transmit mode is for the transmission of data.

The mode shifts to waiting mode after the data have been transmitted.

Receive Mode

The receive mode is for the reception of data.

The mode shifts to waiting mode after the data have been received.

46.3 Interrupts

Table 46.4 shows the interrupt sources.

The Bluetooth middleware executes processing in response to this interrupts.

Table 46.4 BLE Interrupt Sources

Name	DTC Activation	DMAC Activation
BLEIRQ	Not possible	Not possible

46.4 Usage Notes

46.4.1 RF Transceiver Power-Supply

The RF transceiver power-supply is selectable as either from the DC-to-DC converter or linear regulator.

Figure 46.3 and Figure 46.4 show an example of the external connection circuit when the DC-to-DC converter or the linear regulator is selected, respectively.

等待模式

在等待模式下，BLE会一直等待，直到请求发送或接收数据或转换到睡眠模式。

射频睡眠模式

RF睡眠模式是一种低功耗操作模式，并且除了对部分链路层电路之外的电源都停止供电。

传输模式

传输模式用于传输数据。

数据传输完毕后，模式切换到等待模式。

接收模式

接收模式用于接收数据。

接收到数据后模式切换到等待模式。

46.3 Interrupts

表46.4显示了中断源。

蓝牙中间件响应该中断执行处理。

Table 46.4 BLE中断源

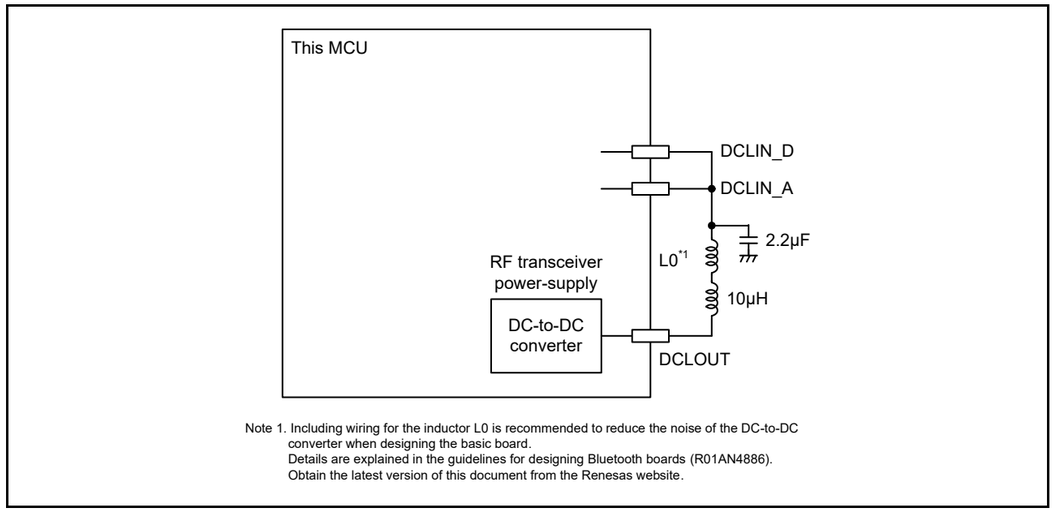
Name	DTC Activation	DMAC Activation
BLEIRQ	不可能	不可能

46.4 使用说明

46.4.1 RF Transceiver Power-Supply

RF收发器电源可选择DC-DC转换器或线性稳压器。

图46.3和图46.4分别显示了选择DC-DC转换器或线性稳压器时的外部连接电路示例。



Note 1. Including wiring for the inductor L0 is recommended to reduce the noise of the DC-to-DC converter when designing the basic board.
Details are explained in the guidelines for designing Bluetooth boards (R01AN4886).
Obtain the latest version of this document from the Renesas website.

Figure 46.3 Example of the BLE Externally Connected Circuit When the DC-to-DC Converter is Selected

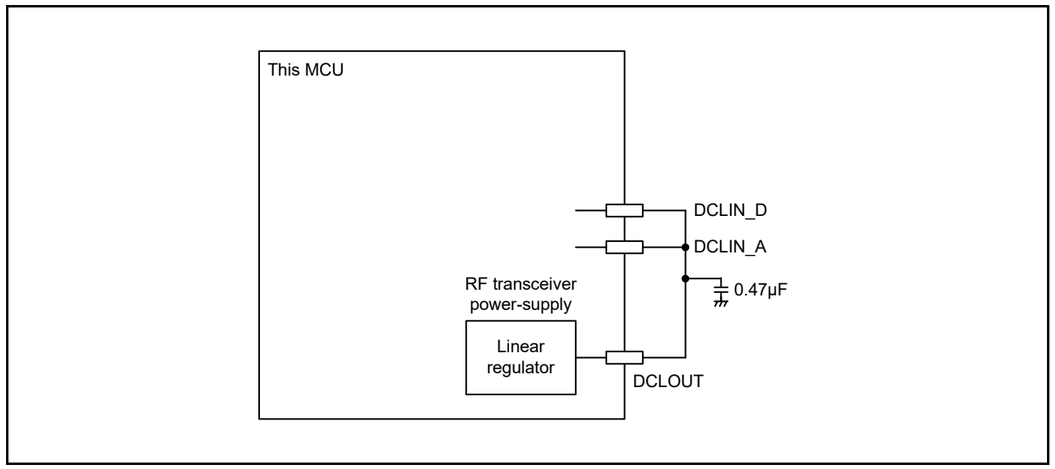


Figure 46.4 Example of the BLE Externally Connected Circuit When the Linear Regulator is Selected

Do not connect other pins or external circuits to the I/O pins (DCLOUT, DCLIN_D, or DCLIN_A) of the RF transceiver power-supply whether the DC to DC converter or linear regulator is selected.

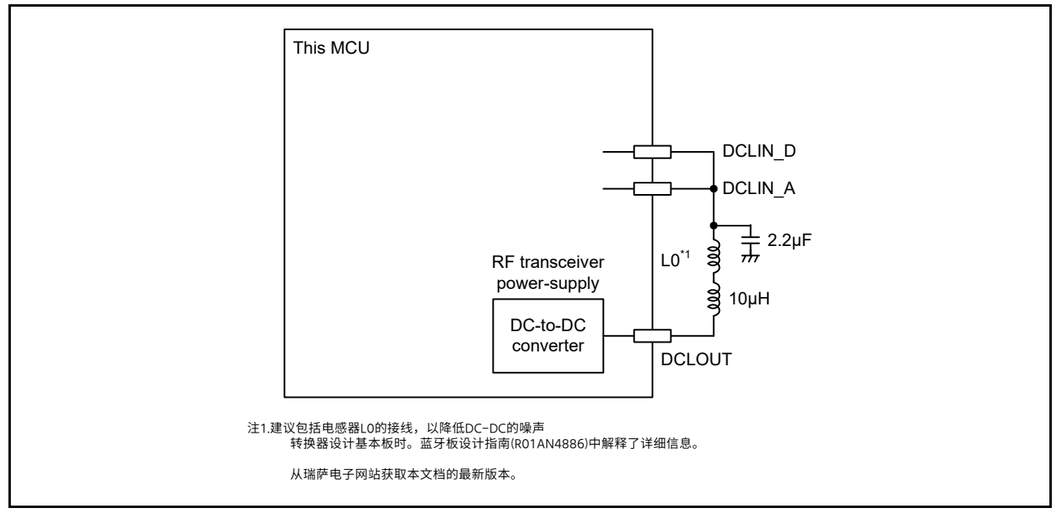
46.4.2 Wireless Standards

International standards and domestic regulations stipulate the use of wireless receivers and transmitters.

Use the device in compliance with the standards or regulations of the country in which the device is being used.

Main standards applicable to the 2.4 GHz band:

- Japan: ARIB STD-T66



注1.建议包括电感器L0的接线，以降低DC-DC的噪声
转换器设计基本板时。蓝牙板设计指南(R01AN4886)中解释了详细信息。

从瑞萨电子网站获取本文档的最新版本。

Figure 46.3 选择DC-DC转换器时的BLE外部连接电路示例

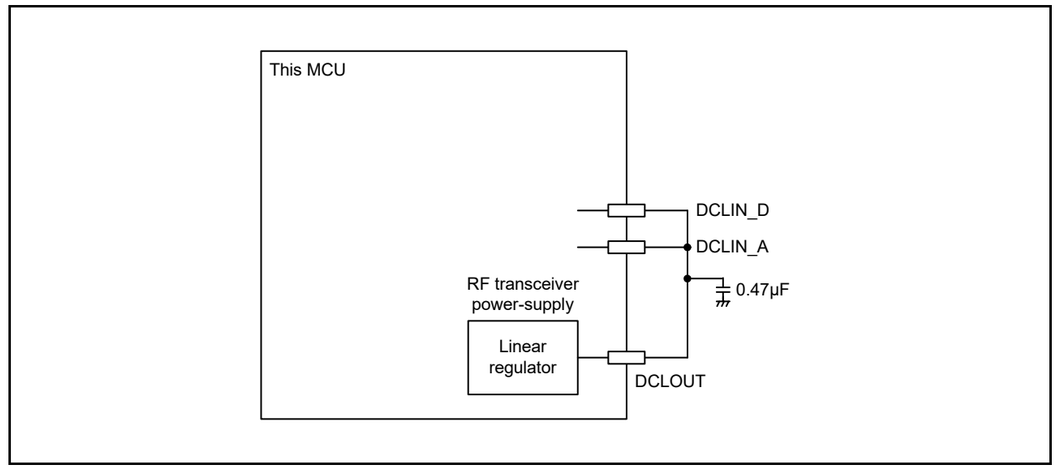


Figure 46.4 选择线性稳压器时的BLE外接电路示例

无论选择DC到DC转换器还是线性稳压器，请勿将其他引脚或外部电路连接到RF收发器电源的IO引脚（DCLOUT、DCLIN_D或DCLIN_A）。

46.4.2 无线标准

国际标准和国内法规规定了无线接收器和发射器的使用。

请按照使用设备所在国家/地区的标准或法规使用设备。

适用于2.4GHz频段的主要标准：

- Japan: ARIB STD-T66

- U.S.A.: FCC CFR Title 47 parts 15.247 and 15.249
- Europe: EN 300 440 and EN 300 328

46.4.3 Notes on Board Design

The applicability of the notes on board design differs with the wireless standard to be employed.

Notes on board design are explained in more detail in the guidelines for designing Bluetooth boards (R01AN4886). Obtain the latest version of this document from the Renesas website.

- 美国：FCCCFRTitle47部分15.247和15.249
- 欧洲：EN300440和EN300328

46.4.3 电路板设计注意事项

板卡设计注释的适用性因所采用的无线标准而异。

蓝牙板设计指南(R01AN4886)中更详细地解释了板设计注意事项。
从瑞萨电子网站获取本文档的最新版本。

47. Internal Voltage Regulator

47.1 Overview

The MCU includes a linear regulator (LDO) that supplies voltage to the internal circuits and memory, except for I/O and the analog domain.

47.2 Operation

Table 47.1 lists the LDO mode pin settings, and Figure 47.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 47.1 LDO mode pin settings

Pin	Settings
All VCC pins	• Connect each pin to the system power supply • Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL pin	Connect each pin to VSS through a 4.7-µF multilayer ceramic capacitor. Place the capacitor close to the pin.

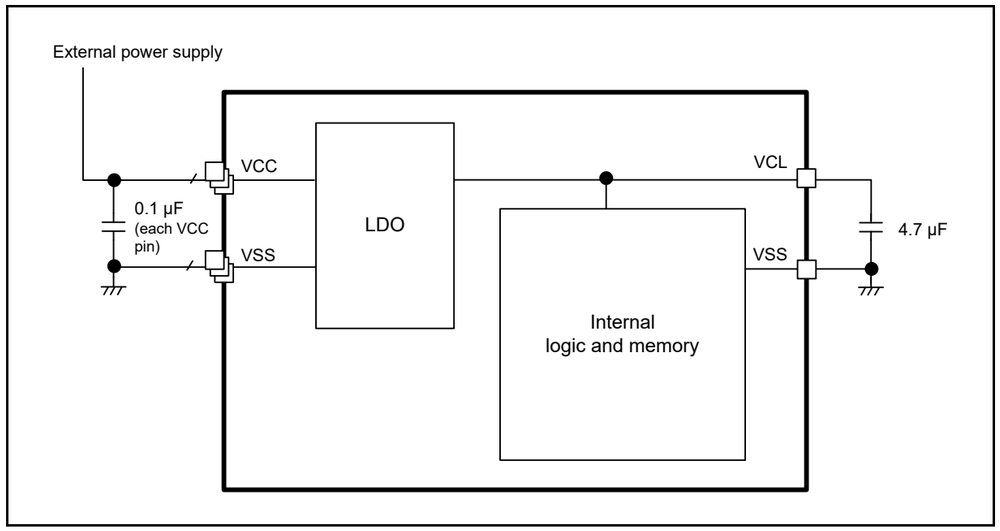


Figure 47.1 LDO mode settings

47. 内部稳压器

47.1 Overview

MCU包含一个线性稳压器(LDO)，可为内部电路和存储器（IO和模拟域除外）提供电压。

47.2 Operation

表47.1列出了LDO模式引脚设置，图47.1显示了LDO模式设置。在LDO模式下，内部电压由VCC产生。

Table 47.1 LDO模式引脚设置

Pin	Settings
所有VCC引脚	将每个引脚连接到系统电源 通过一个0.1µF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
VCL pin	通过一个4.7µF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。

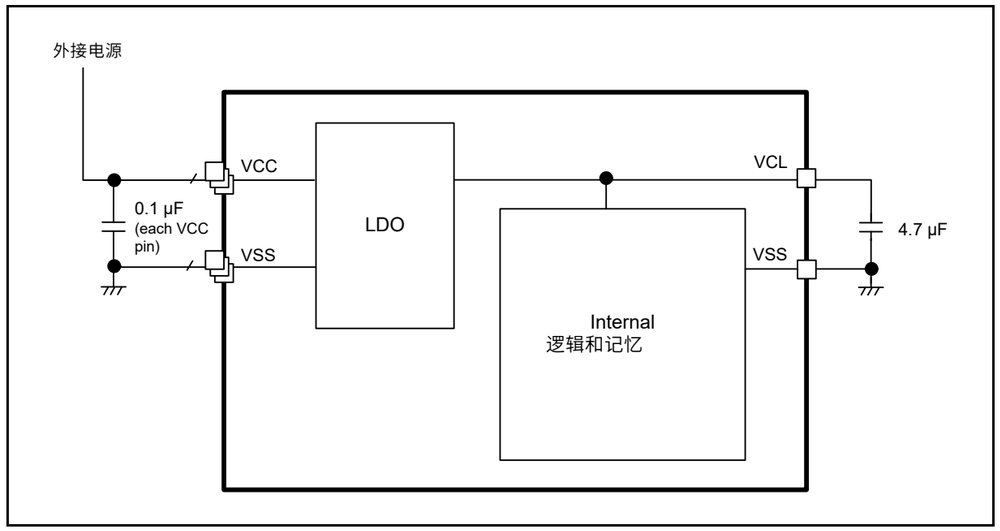


Figure 47.1 LDO模式设置

48. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = VCC_RF = AVCC_RF = 1.8 to 3.6V, VREFH0 = 1.8 to AVCC0, VBATT = 1.8 to 3.6V, VSS = AVSS0 = VREFL0 = VSS_RF = VSS_USB = 0V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 48.1 shows the timing conditions.

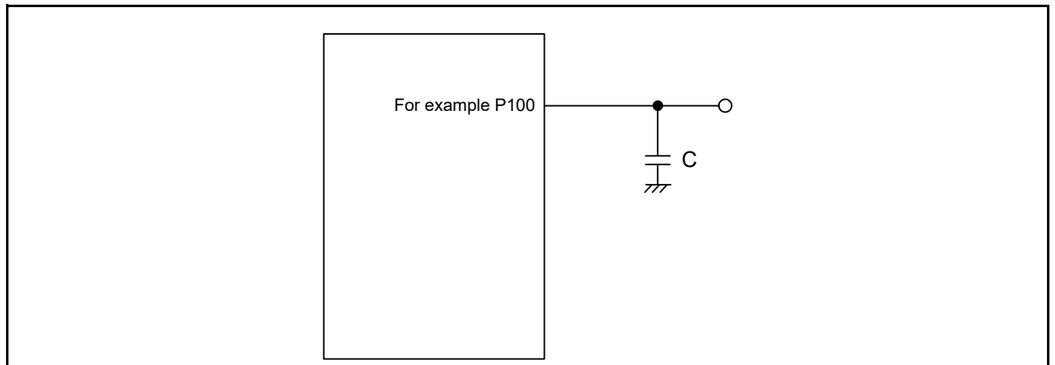


Figure 48.1 Input or output timing measurement conditions

The measurement conditions of timing specifications in each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pin to meet your conditions.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC specification of each function is not guaranteed.

48. 电气特性

除非另有规定，MCU的电气特性在以下条件下定义：

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = VCC_RF = AVCC_RF = 1.8 to 3.6V, VREFH0 = 1.8 to AVCC0，VBATT=1.8至3.6V，VSS=AVSS0=VREFL0=VSS_RF=VSS_USB=0V，Ta=Topr。

注1.典型条件设置为VCC=3.3V。
注2.不使用USBFS时。

图48.1显示了时序条件。

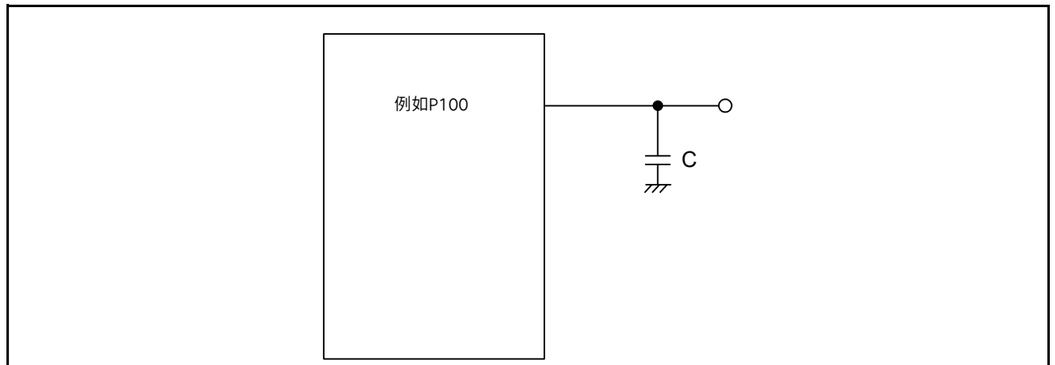


Figure 48.1 输入或输出定时测量条件

推荐每个外设中时序规格的测量条件，以实现最佳外设操作。但是，请确保调整每个引脚的驱动能力以满足您的条件。

用于相同功能的每个功能引脚必须选择相同的驱动能力。如果各功能管脚的IO驱动能力混用，则无法保证各功能的AC规格。

48.1 Absolute Maximum Ratings

Table 48.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	–0.5 to +4.0	V
Input voltage	5V-tolerant ports*1	V_{in}	–0.3 to +6.5	V
	P004, P010, P011, P014, P015	V_{in}	–0.3 to AVCC0 + 0.3	V
	ANT	V_{in}	–1.0 to +1.4	V
	XTAL1_RF, XTAL2_RF	V_{in}	–0.3 to +1.4	V
	DCLIN_A, DCLIN_D	V_{in}	–0.3 to +2.2	V
	Others	V_{in}	–0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	–0.3 to +4.0	V
VBATT power supply voltage		VBATT	–0.5 to +4.0	V
Analog power supply voltage		AVCC0	–0.5 to +4.0	V
		VCC_RF	–0.3 to +4.0	V
		AVCC_RF	–0.3 to +4.0	V
USB power supply voltage		VCC_USB	–0.5 to +4.0	V
		VCC_USB_LDO	–0.5 to +4.0	V
Analog input voltage	When AN004 to AN006, AN009, AN010 are used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN017, AN019, AN020 are used		–0.3 to VCC + 0.3	V
LCD voltage	VL1 voltage	V_{L1}	–0.3 to +2.8	V
	VL2 voltage	V_{L2}	–0.3 to +4.0	V
	VL4 voltage	V_{L4}	–0.3 to +4.0	V
Operating temperature*2		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Note 1. Ports P205, P206, P402, P407 are 5V-tolerant.
Note 2. See section 48.2.1, Tj/Ta Definition.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between VCC_RF and VSS_RF pins, between the AVDD_RF and VSS_RF pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins. Place capacitors with values of about 2.2 µF in the case of the VCC_RF pin and about 0.1 µF otherwise as close as possible to every power supply pin, and use the shortest and thickest possible traces for the connections. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

48.1 绝对最大额定值

Table 48.1 绝对最大额定值

Parameter		Symbol	Value	Unit
电源电压		VCC	–0.5 to +4.0	V
输入电压	5V-tolerant ports*1	V_{in}	–0.3 to +6.5	V
	P004, P010, P011, P014, P015	V_{in}	–0.3 to AVCC0 + 0.3	V
	ANT	V_{in}	–1.0 to +1.4	V
	XTAL1_RF, XTAL2_RF	V_{in}	–0.3 to +1.4	V
	DCLIN_A, DCLIN_D	V_{in}	–0.3 to +2.2	V
	Others	V_{in}	–0.3 to VCC + 0.3	V
参考电源电压		VREFH0	–0.3 to +4.0	V
VBATT电源电压		VBATT	–0.5 to +4.0	V
模拟电源电压		AVCC0	–0.5 to +4.0	V
		VCC_RF	–0.3 to +4.0	V
		AVCC_RF	–0.3 to +4.0	V
USB电源电压		VCC_USB	–0.5 to +4.0	V
		VCC_USB_LDO	–0.5 to +4.0	V
模拟输入电压	使用AN004至AN006、AN009、AN010时	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN017, AN019, 使用AN020		–0.3 to VCC + 0.3	V
LCD voltage	VL1 voltage	V_{L1}	–0.3 to +2.8	V
	VL2 voltage	V_{L2}	–0.3 to +4.0	V
	VL4 voltage	V_{L4}	–0.3 to +4.0	V
Operating temperature*2		T_{opr}	–40 to +85	°C
贮存温度		T_{stg}	–55 to +125	°C

Note 1. 端口P205、P206、P402、P407可承受5V。
Note 2. 请参见第48.2.1节，TjTa定义。

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。
为避免因噪声干扰而导致的任何故障，请在VCC和VSS引脚之间、AVCC0和AVSS0引脚之间、VCC_RF和VSS_RF引脚之间、AVDD_RF和VSS_RF引脚之间、VCC_USB和VSS_USB引脚之间、之间插入具有高频特性的电容器。VREFH0和VREFL0引脚。在VCC_RF引脚的情况下放置值约为2.2µF的电容器，在其他情况下放置大约0.1µF的电容器，尽可能靠近每个电源引脚，并使用最短和最厚的走线进行连接。此外，连接电容器作为稳定电容。通过一个4.7µF电容将VCL引脚连接到VSS引脚。电容必须靠近引脚放置。

请勿在设备未通电时输入信号或IO上拉电源。输入此类信号或IO上拉导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件劣化。

Table 48.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.8	-	3.6	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used	-	VCC	-	V
	VSS_USB		-	0	-	V
VBATT power supply voltage	VBATT	When the battery backup function is not used	-	VCC	-	V
		When the battery backup function is used	1.8	-	3.6	V
Analog power supply voltages	AVCC0*1, *2		1.8	-	3.6	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.8	-	AVCC0	V
	VREFL0		-	0	-	V
BLE power supply voltages	VCC_RF*3		1.8	-	3.6	V
	AVCC_RF*3		1.8	-	3.6	
	VSS_RF		-	0	-	

Note: Bluetooth power supply voltage
VCC_RF *3 1.8 - 3.6 V
Note: AVCC_RF *3 1.8 - 3.6 V
Note: VCC_RF - 0 - V
Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V
AVCC0 = VCC when VCC < 2.2 V or AVCC0 < 2.2 V
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.
Note 3. Use VCC = VCC_RF = AVCC_RF

Table 48.2 推荐工作条件

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC*1, *2	不使用USBFS时	1.8	-	3.6	V
		使用USBFS时 USB稳压器 Disable	VCC_USB	-	3.6	V
	VSS		-	0	-	V
USB电源电压	VCC_USB	不使用USBFS时	-	VCC	-	V
		使用USBFS时 USB稳压器 Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	不使用USBFS时	-	VCC	-	V
		使用USBFS时	-	VCC	-	V
	VSS_USB		-	0	-	V
VBATT电源电压	VBATT	不使用电池备份功能时	-	VCC	-	V
		使用电池备份功能时	1.8	-	3.6	V
模拟电源电压	AVCC0*1, *2		1.8	-	3.6	V
	AVSS0		-	0	-	V
	VREFH0	当用作 ADC14 Reference	1.8	-	AVCC0	V
	VREFL0		-	0	-	V
BLE电源电压	VCC_RF*3		1.8	-	3.6	V
	AVCC_RF*3		1.8	-	3.6	
	VSS_RF		-	0	-	

Note: 蓝牙电源电压
VCC_RF *3 1.8 - 3.6 V
Note: AVCC_RF *3 1.8 - 3.6 V
Note: VCC_RF - 0 - V
Note 1. 在以下条件下使用AVCC0和VCC：当VCC≥2.2V和AVCC0≥2.2V时，AVCC0和VCC可以在工作范围内单独设置
当VCC<2.2V或AVCC0<2.2V时，AVCC0=VCC
Note 2. 给VCC和AVCC0上电时，要同时上电或者先上VCC再上AVCC0。
Note 3. Use VCC = VCC_RF = AVCC_RF

48.2 DC Characteristics

48.2.1 Tj/Ta Definition

Table 48.3 DC characteristics
Conditions: Products with operating temperature (T_a) –40 to +85°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	105*1	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC – V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is 85°C. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C.

48.2.2 I/O V_{IH}, V_{IL}

Table 48.4 I/O V_{IH}, V_{IL} (1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 3.6V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	IIC*1	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*2	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P004, P010	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P004, P010, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.05	-	-		

Note 1. P205, P206, P407 (total 3 pins).
Note 2. P205, P206, P402, P407 (total 4 pins).

48.2 DC Characteristics

48.2.1 Tj/Ta Definition

Table 48.3 DC characteristics
条件：工作温度(Ta) 40至+85°C的产品

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	Tj	-	105*1	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCC VOH)×ΣIOH+VOL×ΣIOL+ICCmax×VCC。

Note 1. 工作温度上限为85°C。有关详细信息，请参阅第1.3节，部件编号。如果零件编号显示工作温度为85°C，则Tj的最大值为105°C。

48.2.2 IOVIH

Table 48.4 IOVIH VIL(1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 3.6V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
施密特触发器输入电压	IIC*1	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI 除IIC外的其他外设输入引脚	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
输入电压（施密特触发器输入引脚除外）	5V-tolerant ports*2	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P004, P010	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL 输入端口引脚除了 P004, P010, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
选择VBATT电源时	P402	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.05	-	-		

Note 1. P205, P206, P407 (total 3 pins).
Note 2. P205, P206, P402, P407 (total 4 pins).

Table 48.5 I/O V_{IH}, V_{IL} (2)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.8 to 2.7 V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	-	V	-
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P004, P010	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P004, P010	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.01	-	-		

Note 1. P205, P206, P402, P407 (total 4 pins).

Table 48.5 IOVIH VIL(2)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.8 to 2.7 V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
施密特触发器输入电压	RES, NMI 外设输入引脚	V_{IH}	VCC × 0.8	-	-	V	-
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
输入电压（施密特触发器输入引脚除外）	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P004, P010	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL 输入端口引脚除了 P004, P010	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
选择VBATT电源时	P402, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.01	-	-		

Note 1. P205, P206, P402, P407 (total 4 pins).

48.2.3 I/O I_{OH}, I_{OL}

Table 48.6 I/O I_{OH}, I_{OL}
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P409	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 3.6 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P111, P201, P204, P300, P501 (total 16 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pin*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (Max value per pin)	Ports P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P409	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 3.6 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P111, P201, P204, P300, P501 (total 16 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pin*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value total pins)	Total of ports P004, P010		ΣI_{OH} (max)	-	-	–30	mA
			ΣI_{OL} (max)	-	-	30	mA
	Ports P914, P915		ΣI_{OH} (max)	-	-	–4.0	mA
			ΣI_{OL} (min)	-	-	4.0	mA
	Total of all output pin*5		ΣI_{OH} (max)	-	-	–60	mA
			ΣI_{OL} (max)	-	-	60	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

48.2.3 我爱我哦

Table 48.6 我爱我哦
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit
允许输出电流（每个引脚的平均值）	Ports P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P409	低驱*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		中驱*2 VCC = 3.0 to 3.6 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	端口P100至P111，P201, P204, P300, P501 (total 16 pins)	低驱*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	其他输出引脚*3	低驱*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
允许输出电流（每个引脚的最大值）	Ports P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P409	低驱*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		中驱*2 VCC = 3.0 to 3.6 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	端口P100至P111，P201, P204, P300, P501 (total 16 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	其他输出引脚*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
允许输出电流（最大总引脚数）	P004、P010端口总数		ΣI_{OH} (max)	-	-	–30	mA
			ΣI_{OL} (max)	-	-	30	mA
	Ports P914, P915		ΣI_{OH} (max)	-	-	–4.0	mA
			ΣI_{OL} (min)	-	-	4.0	mA
	所有输出引脚的总数*5		ΣI_{OH} (max)	-	-	–60	mA
			ΣI_{OL} (max)	-	-	60	mA

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流是指在100µs内测得的电流平均值。

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 3. Except for ports P200, P214, P215, which are input ports.
Note 4. This is the value when middle driving ability for IIC Fast-mode is selected with the Port Drive Capability bit in PmnPFS register.
Note 5. For details on the permissible output current used with CTSU, see section 48.11, CTSU Characteristics.

48.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 48.7 I/O V_{OH}, V_{OL} (1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}*2,*5	-	-	0.6		I_{OL} = 6.0 mA
	Ports P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Ports P004, P010	Low drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Ports P914, P915		V_{OH}	VCC_USB – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
	Other output pins *4, *6	Low drive	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive*5	V_{OH}	VCC – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA

Note 1. P100, P101, P204, P205, P206, P407 (total 6 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for ports P200, P214, P215, which are input ports.
Note 5. Except for P212, P213.
Note 6. This excludes the CLKOUT_RF pin.

Table 48.8 I/O V_{OH}, V_{OL} (2)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.8 to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P004, P010	Low drive	V_{OH}	AVCC0 – 0.3	-	-	V	I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive	V_{OH}	AVCC0 – 0.3	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Ports P914, P915		V_{OH}	VCC_USB – 0.3	-	-		I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
	Other output pins *1, *3	Low drive	V_{OH}	VCC – 0.3	-	-		I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive*2	V_{OH}	VCC – 0.3	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA

Note 1. Except for ports P200, P214, P215, which are input ports.
Note 2. Except for P212, P213.
Note 3. This excludes the CLKOUT_RF pin.

Note 1. 这是使用PmnPFS寄存器中的端口驱动能力位选择低驱动能力时的值。
Note 2. 这是使用PmnPFS寄存器中的端口驱动能力位选择中等驱动能力时的值。
Note 3. 端口P200、P214、P215除外，它们是输入端口。
Note 4. 这是使用PmnPFS寄存器中的端口驱动能力位选择IIC快速模式的中等驱动能力时的值。
Note 5. 有关与CTSU一起使用的允许输出电流的详细信息，请参阅第48.11节，CTSU特性。

48.2.4 IOVOH VOL和其他特性

Table 48.7 IOVOH VOL(1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
输出电压	IIC*1		V_{OL}	-	-	0.4	V	我OL=3.0毫安
			V_{OL}*2,*5	-	-	0.6		我OL=6.0毫安
	Ports P409*2, *3		V_{OH}	VCC – 1.0	-	-		IOH= 20mAV CC=3.3V
			V_{OL}	-	-	1.0		我OL=20毫安VCC=3.3V
	Ports P004, P010	低驱动	V_{OH}	AVCC0 – 0.5	-	-		IOH= 1.0毫安
			V_{OL}	-	-	0.5		我OL=1.0毫安
		中间驱动器	V_{OH}	AVCC0 – 0.5	-	-		IOH= 2.0毫安
			V_{OL}	-	-	0.5		我OL=2.0毫安
	Ports P914, P915		V_{OH}	VCC_USB – 0.5	-	-		IOH= 1.0毫安
			V_{OL}	-	-	0.5		我OL=1.0毫安
	其他输出引脚*4、*6	低驱动	V_{OH}	VCC – 0.5	-	-		IOH= 1.0毫安
			V_{OL}	-	-	0.5		我OL=1.0毫安
		Middle drive*5	V_{OH}	VCC – 0.5	-	-		IOH= 2.0毫安
			V_{OL}	-	-	0.5		我OL=2.0毫安

Note 1. P100, P101, P204, P205, P206, P407 (total 6 pins).
Note 2. 这是使用PmnPFS寄存器中的端口驱动能力位选择中等驱动能力时的值。
Note 3. 基于特性数据，未经生产测试。
Note 4. 端口P200、P214、P215除外，它们是输入端口。
Note 5. P212、P213除外。
Note 6. 这不包括CLKOUT_RF引脚。

Table 48.8 IOVOH VOL(2)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.8 to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
输出电压	Ports P004, P010	低驱动	V_{OH}	AVCC0 – 0.3	-	-	V	IOH= 0.5毫安
			V_{OL}	-	-	0.3		我OL=0.5毫安
		中间驱动器	V_{OH}	AVCC0 – 0.3	-	-		IOH= 1.0毫安
			V_{OL}	-	-	0.3		我OL=1.0毫安
	Ports P914, P915		V_{OH}	VCC_USB – 0.3	-	-		IOH= 0.5毫安
			V_{OL}	-	-	0.3		我OL=0.5毫安
	其他输出引脚*1、*3	低驱动	V_{OH}	VCC – 0.3	-	-		IOH= 0.5毫安
			V_{OL}	-	-	0.3		我OL=0.5毫安
		Middle drive*2	V_{OH}	VCC – 0.3	-	-		IOH= 1.0毫安
			V_{OL}	-	-	0.3		我OL=1.0毫安

Note 1. 端口P200、P214、P215除外，它们是输入端口。
Note 2. P212、P213除外。
Note 3. 这不包括CLKOUT_RF引脚。

Table 48.9 I/O V_{OH}, V_{OL} (3)
Conditions: 3.0V ≤ VCC = AVCC0 = VCC_USB = VCC_USB_LDO = VCC_RF = AVCC_RF ≤ 3.6 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Output low	CLKOUT_RF	V_{OL}	-	0.3	V	I_{OL} = 0.5 mA
Output high	CLKOUT_RF	V_{OH}	VCC_RF – 0.3	-	V	I_{OH} = –0.5 mA

Table 48.10 I/O other characteristics
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, P200, P214, P215	$\lvert I_{in} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports	$\lvert I_{TSI} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for ports P200, P214, P215 and 5 V tolerant)		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for ports P200, P214, P215, P914, P915)	R_U	10	20	50	kΩ	V_{in} = 0 V
Input capacitance	P914, P915, P100 to P103, P111, P200	C_{in}	-	-	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		-	-	15		

48.2.5 I/O Pin Output Characteristics of Low Drive Capacity

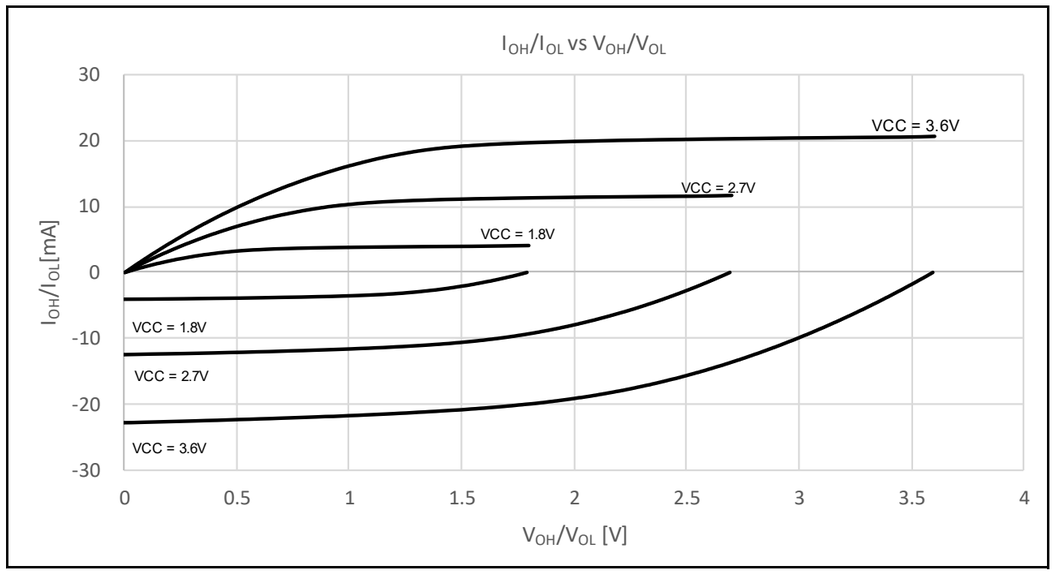


Figure 48.2 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when low drive output is selected (reference data)

Table 48.9 IOVOH VOL(3)
Conditions: 3.0V ≤ VCC = AVCC0 = VCC_USB = VCC_USB_LDO = VCC_RF = AVCC_RF ≤ 3.6 V

Parameter		Symbol	Min	Max	Unit	测试条件
输出低	CLKOUT_RF	V_{OL}	-	0.3	V	我OL=0.5毫安
输出高	CLKOUT_RF	V_{OH}	VCC_RF – 0.3	-	V	IOH= 0.5毫安

Table 48.10 IO其他特征
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入漏电流	RES, P200, P214, P215	$\lvert I_{in} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5V-tolerant ports	$\lvert I_{TSI} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	其他端口（端口P200、P214、P215和5V容限除外）		-	-	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉电阻	所有端口（端口P200、P214、P215、P914、P915除外）	R_U	10	20	50	kΩ	V_{in} = 0 V
输入电容	P914, P915, P100 to P103, P111, P200	C_{in}	-	-	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	其他输入引脚		-	-	15		

48.2.5 低驱动能力的IO引脚输出特性

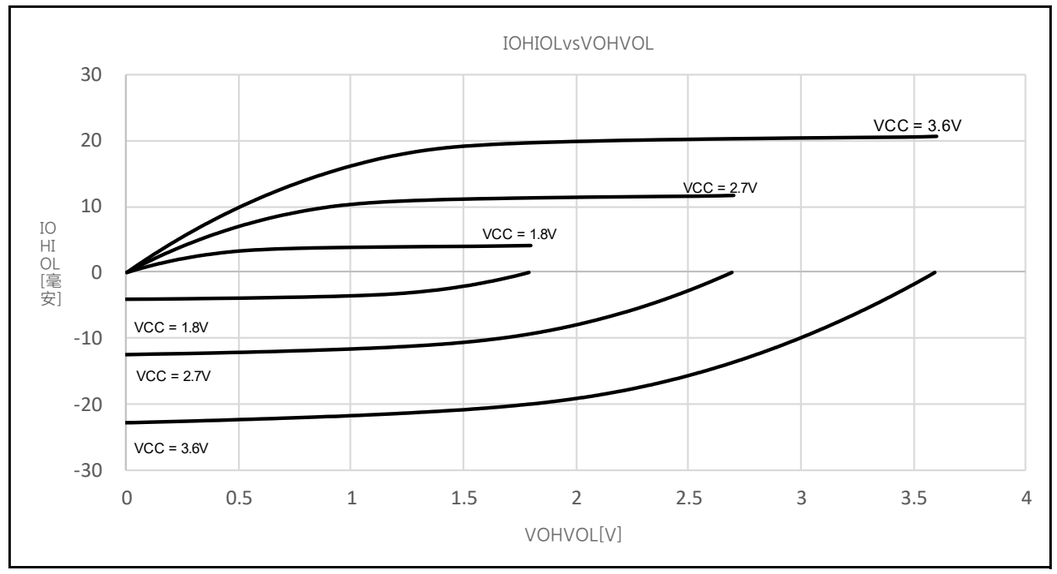


Figure 48.2 选择低驱动输出时，Ta=25°C时的VOHVOL和IOHIOL电压特性（参考数据）

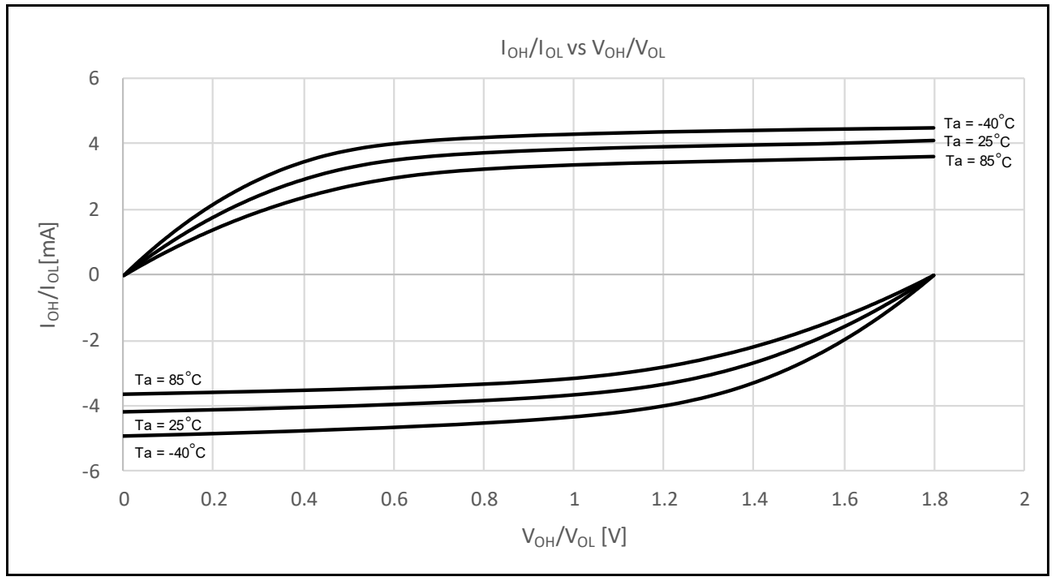


Figure 48.3 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.8 V when low drive output is selected (reference data)

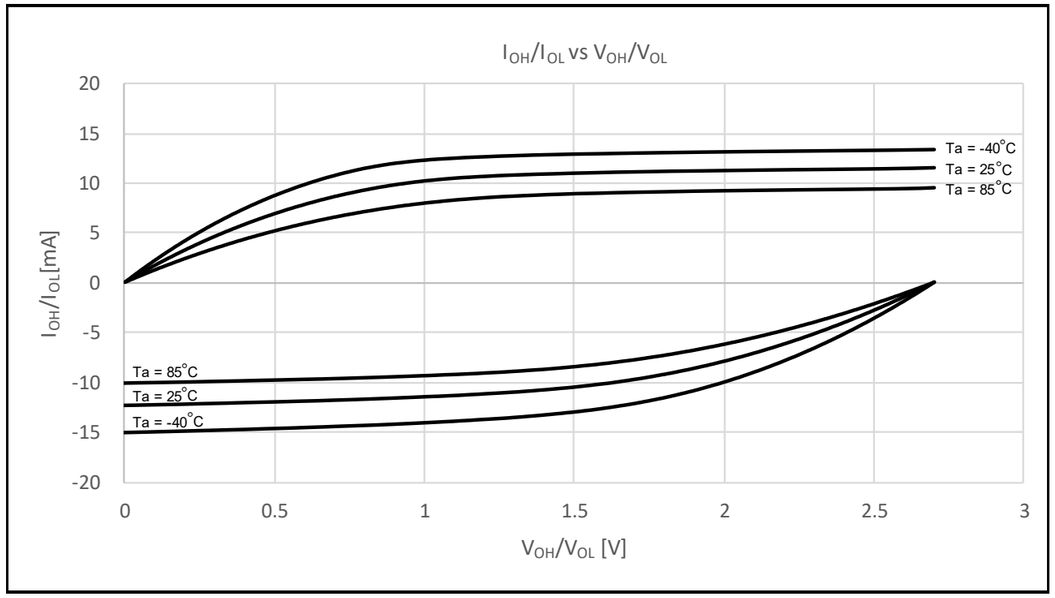


Figure 48.4 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when low drive output is selected (reference data)

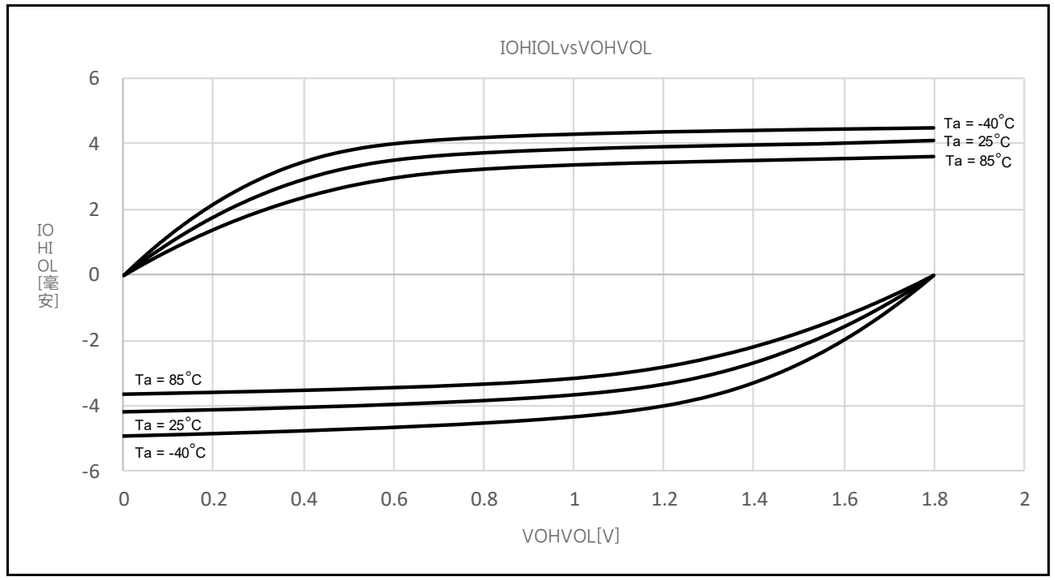


Figure 48.3 选择低驱动输出时，VCC=1.8V时的VOHVOL和IOHIOL温度特性（参考数据）

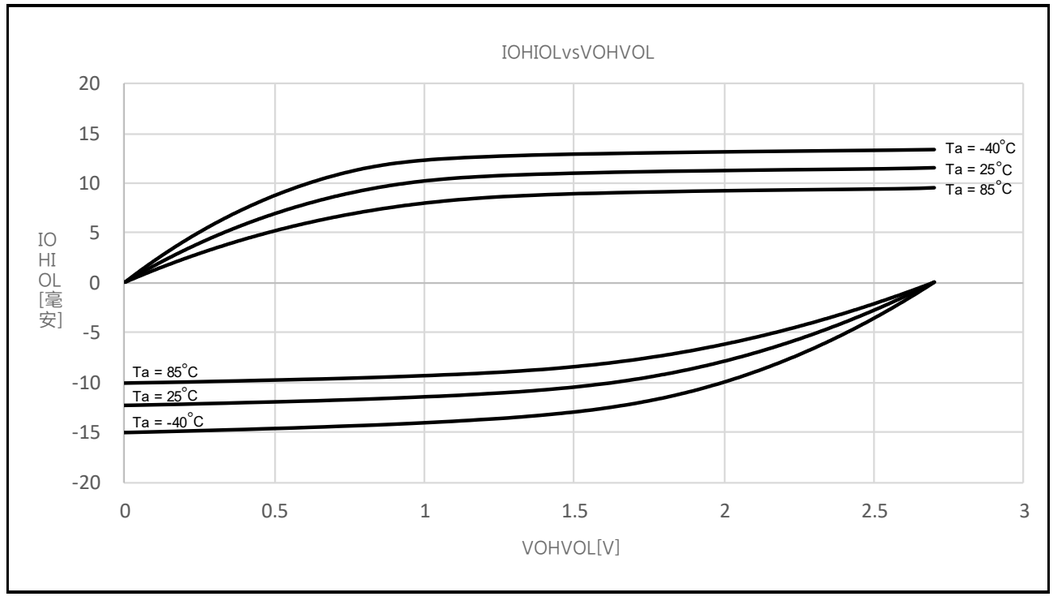


Figure 48.4 选择低驱动输出时，VCC=2.7V时的VOHVOL和IOHIOL温度特性（参考数据）

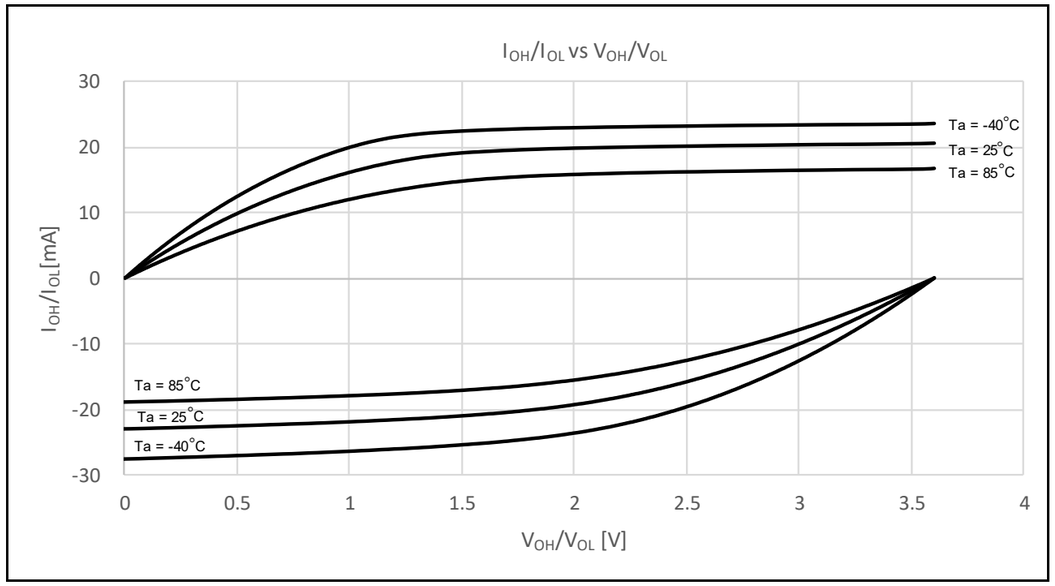


Figure 48.5 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.6 V when low drive output is selected (reference data)

48.2.6 I/O Pin Output Characteristics of Middle Drive Capacity

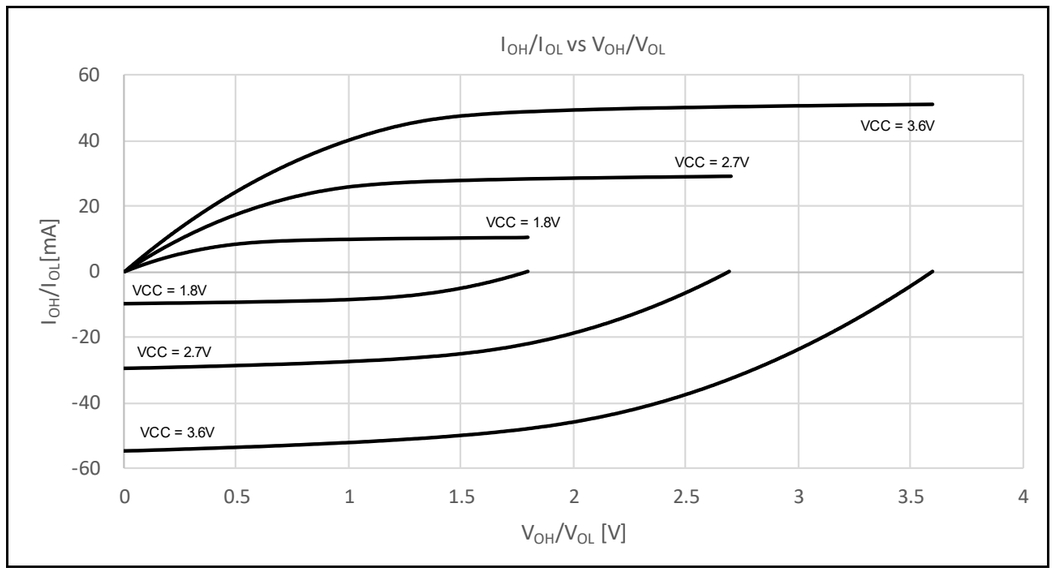


Figure 48.6 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)

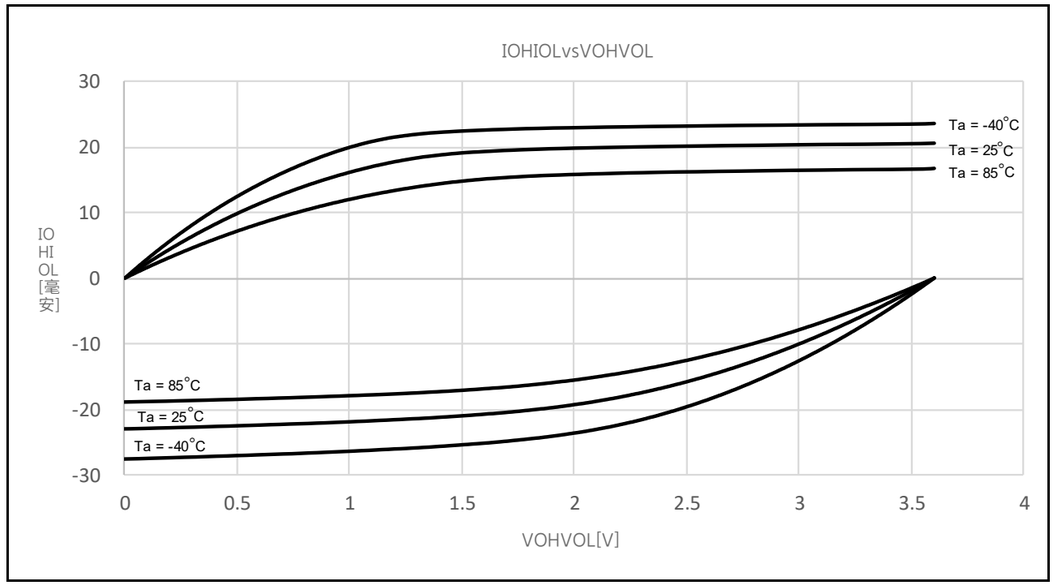


Figure 48.5 选择低驱动输出时，VCC=3.6V时的VOHVOL和IOHIOL温度特性（参考数据）

48.2.6 中等驱动容量的IOPin输出特性

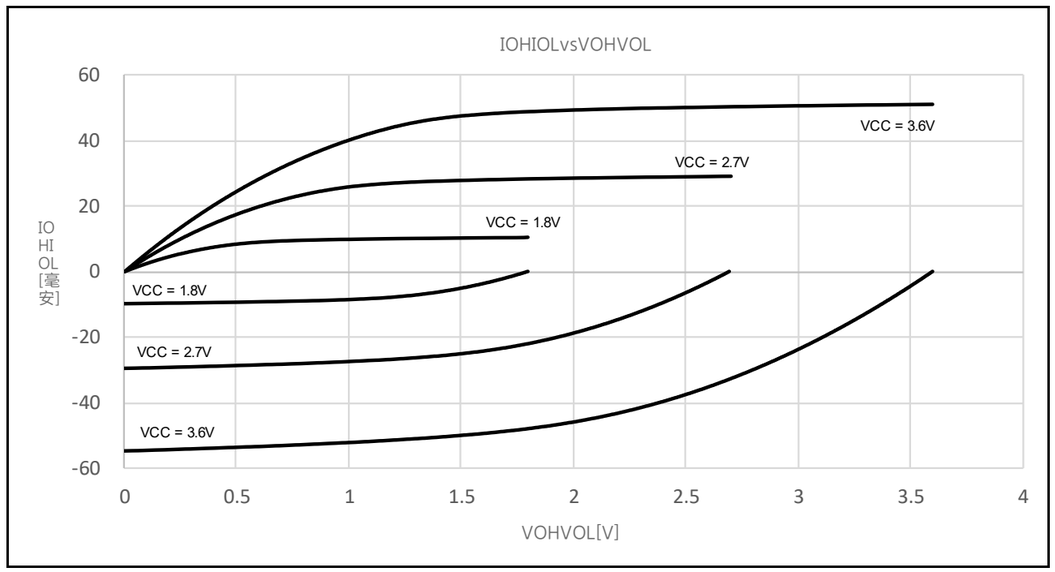


Figure 48.6 选择中间驱动输出时Ta=25°C时的VOHVOL和IOHIOL电压特性（参考数据）

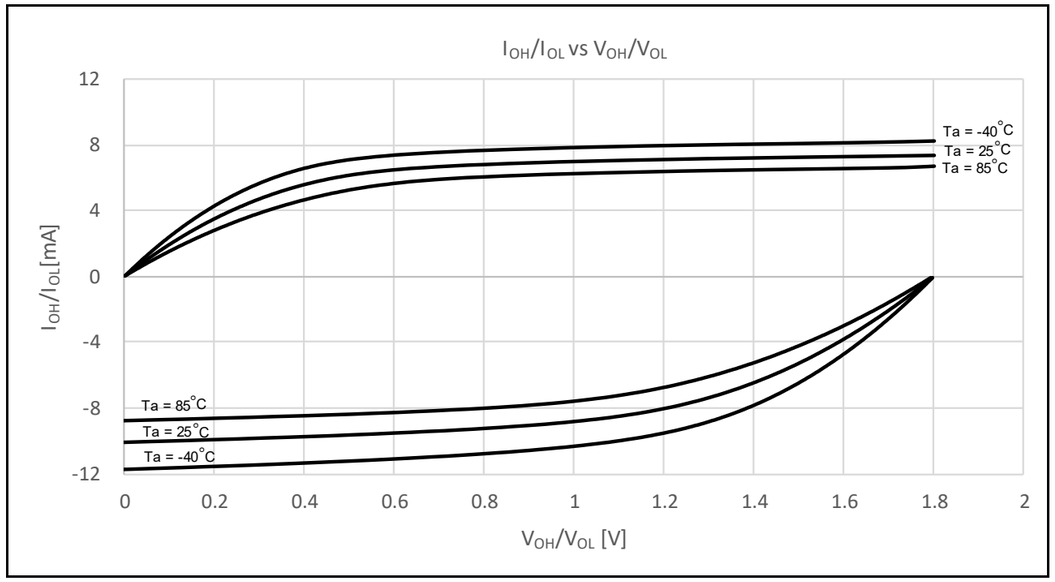


Figure 48.7 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.8 V when middle drive output is selected (reference data)

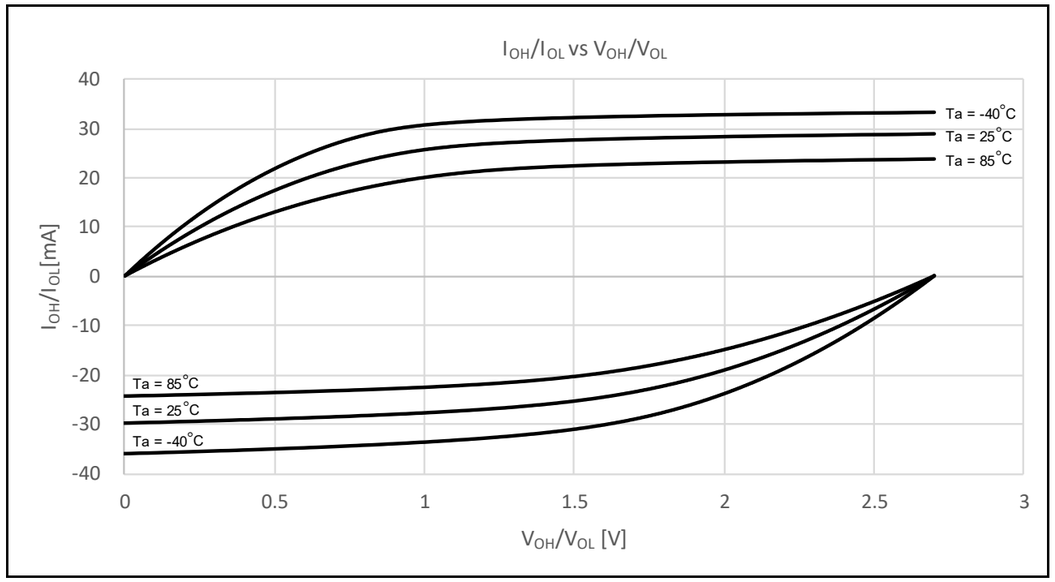


Figure 48.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)

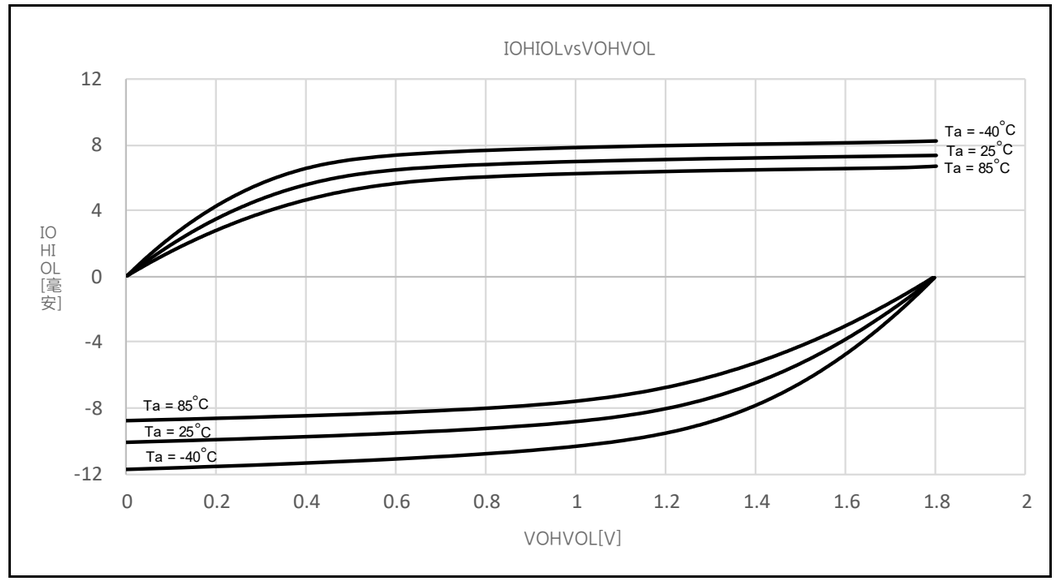


Figure 48.7 选择中间驱动输出时，VCC=1.8V时的VOHVOL和IOHIOL温度特性（参考数据）

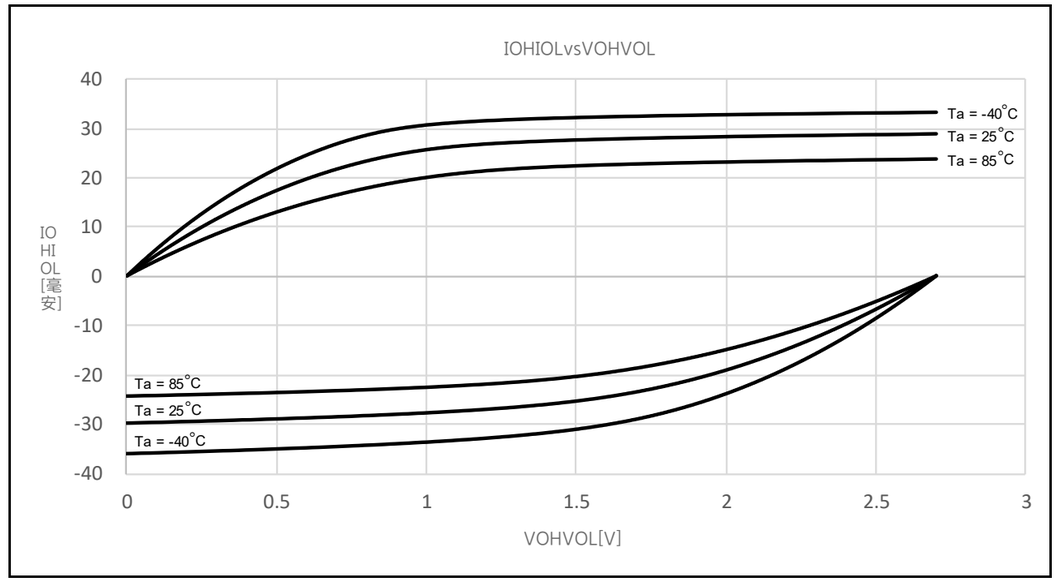


Figure 48.8 选择中间驱动输出时，VCC=2.7V时的VOHVOL和IOHIOL温度特性（参考数据）

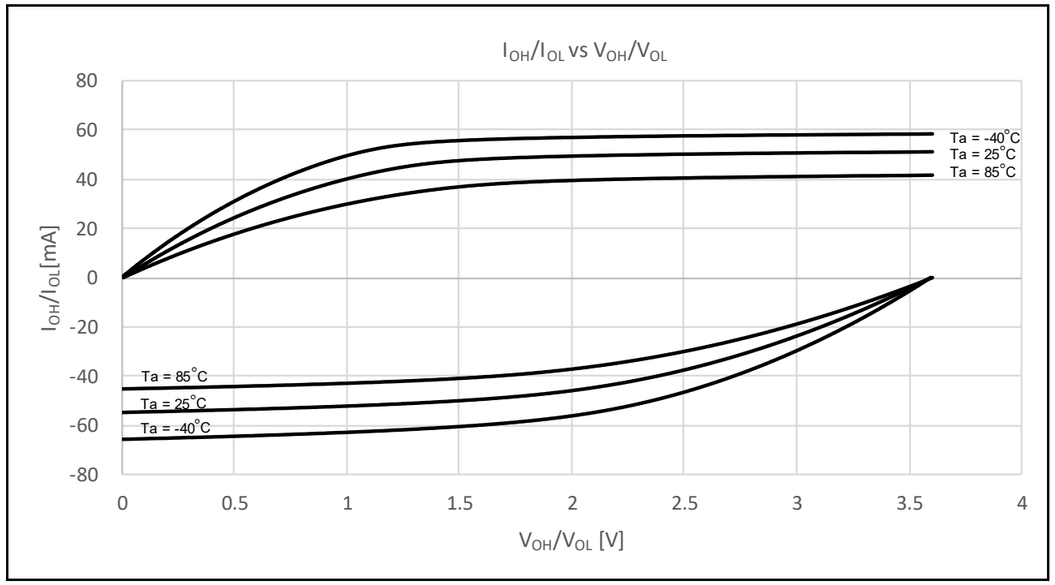


Figure 48.9 V_{OH}/V_{OL} **and** I_{OH}/I_{OL} **temperature characteristics at VCC = 3.6 V when middle drive output is selected (reference data)**

48.2.7 P409 I/O Pin Output Characteristics of Middle Drive Capacity

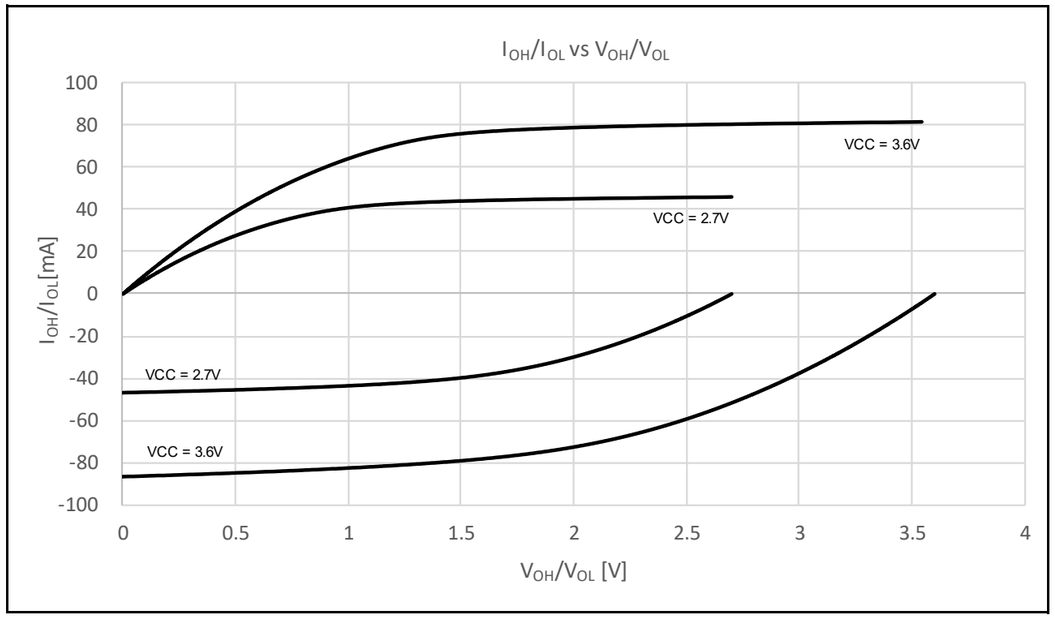


Figure 48.10 V_{OH}/V_{OL} **and** I_{OH}/I_{OL} **voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

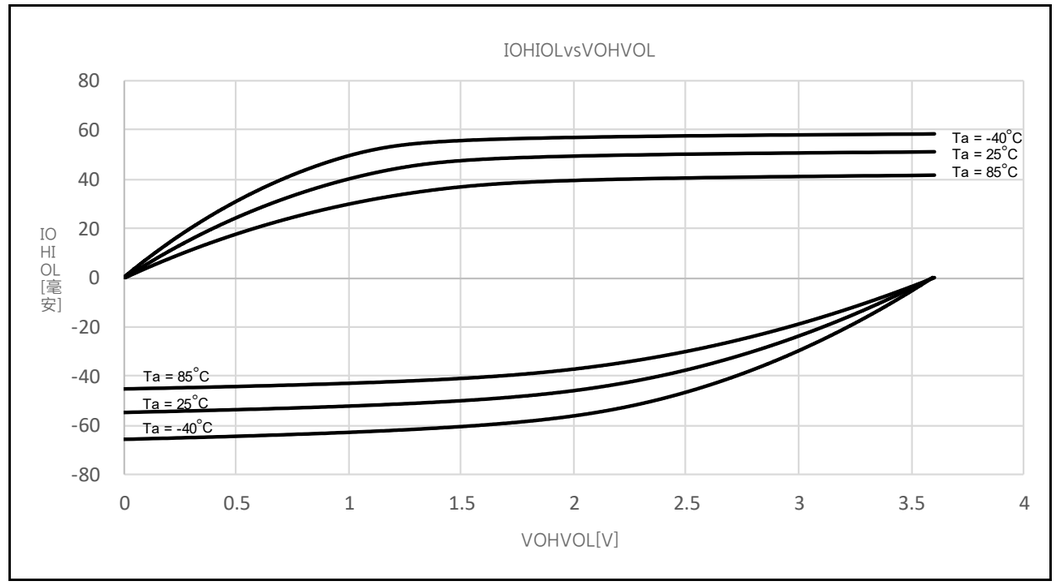


Figure 48.9 **选择中间驱动输出时，VCC=3.6V时的VOHVOL和IOHIOL温度特性（参考数据）**

48.2.7 P409中间驱动容量的IO管脚输出特性

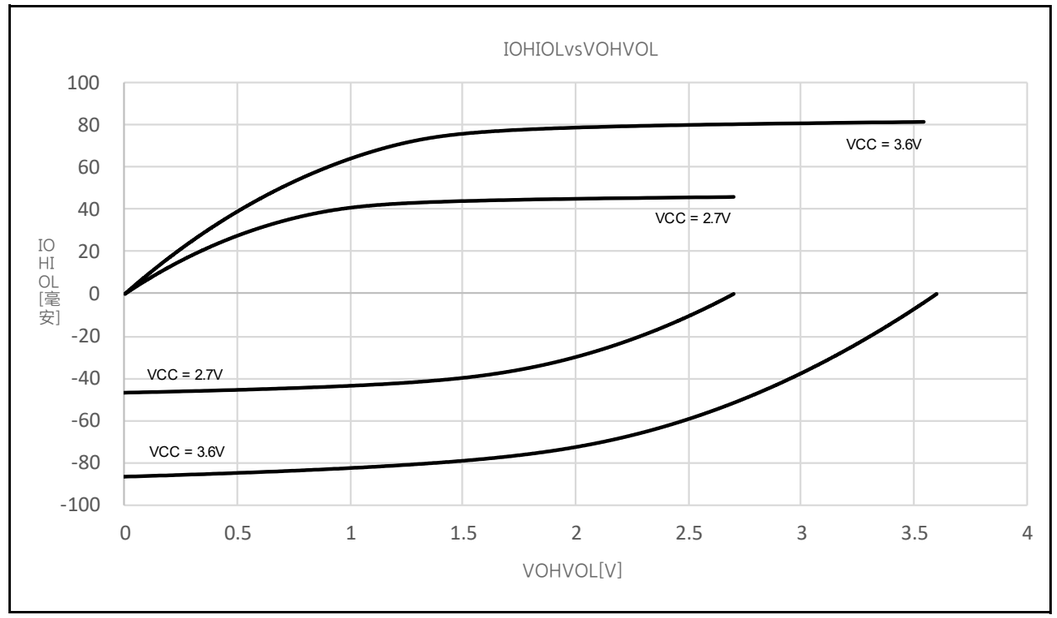


Figure 48.10 **选择中间驱动输出时Ta=25°C时的VOHVOL和IOHIOL电压特性（参考数据）**

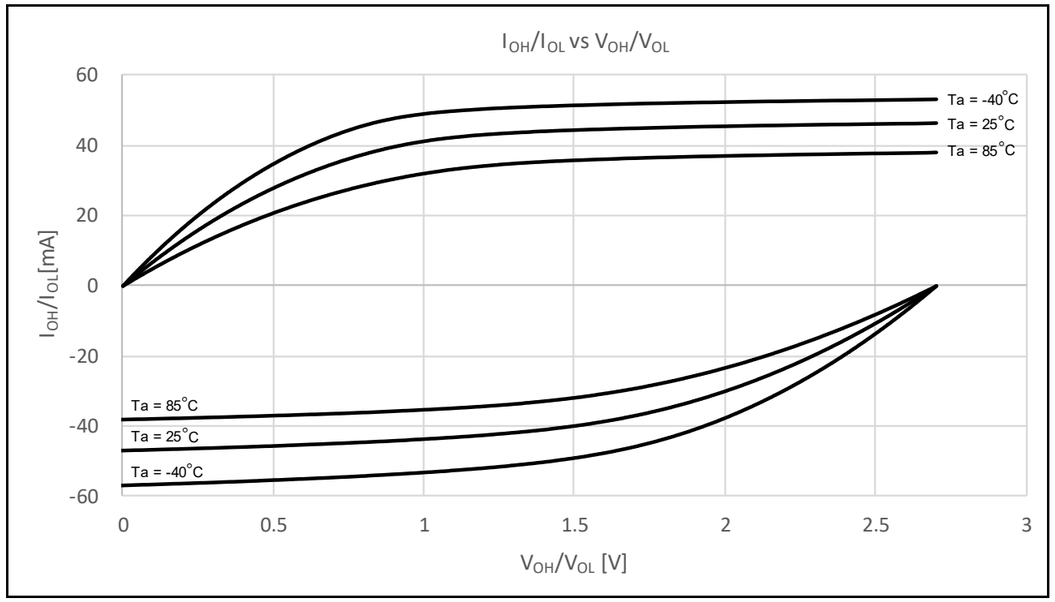


Figure 48.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)

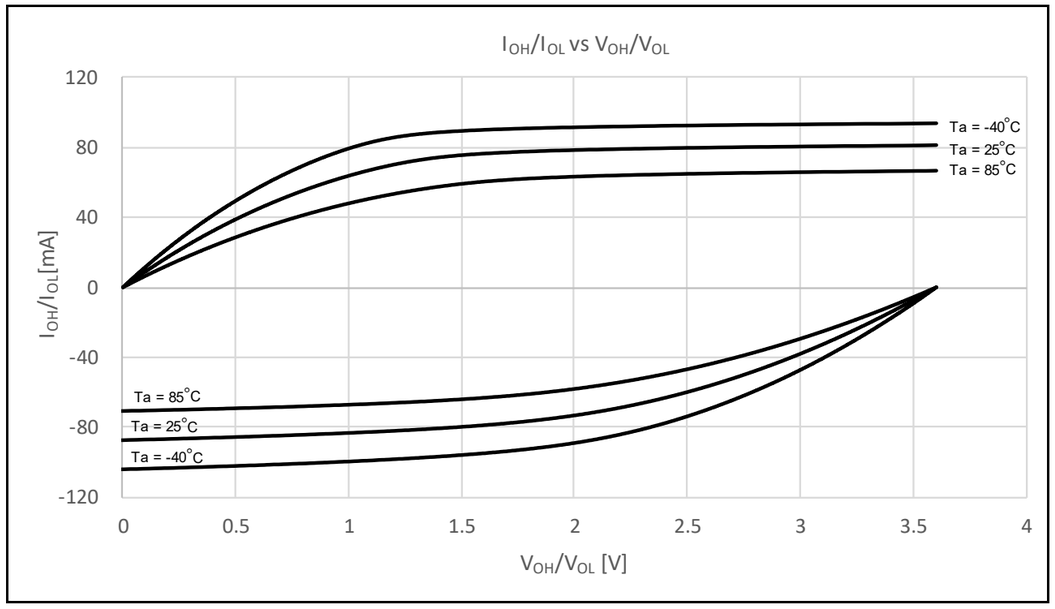


Figure 48.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.6 V when middle drive output is selected (reference data)

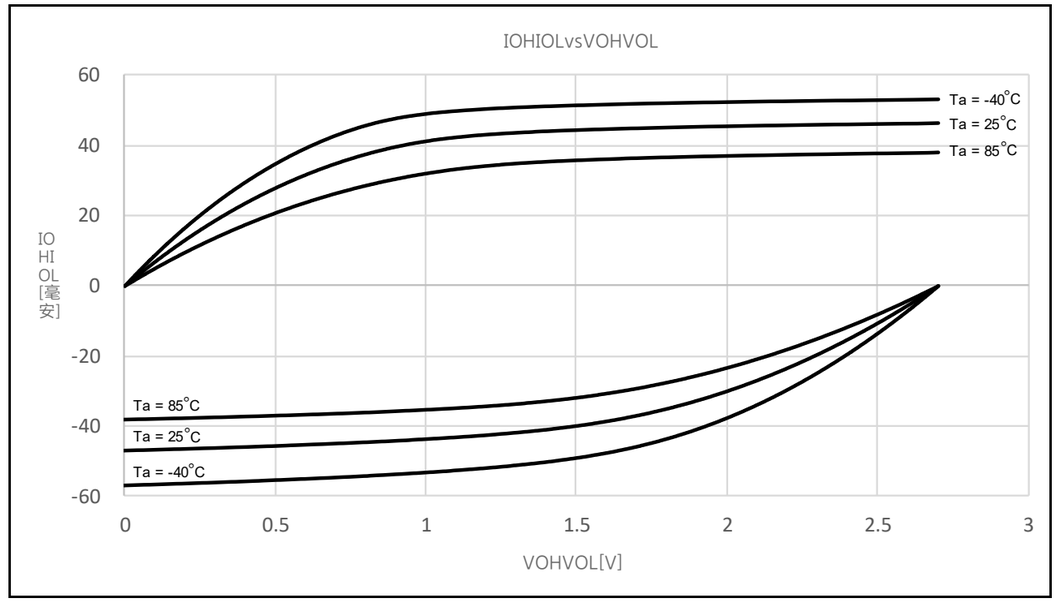


Figure 48.11 选择中间驱动输出时，VCC=2.7V时的VOHVOL和IOHIOL温度特性（参考数据）

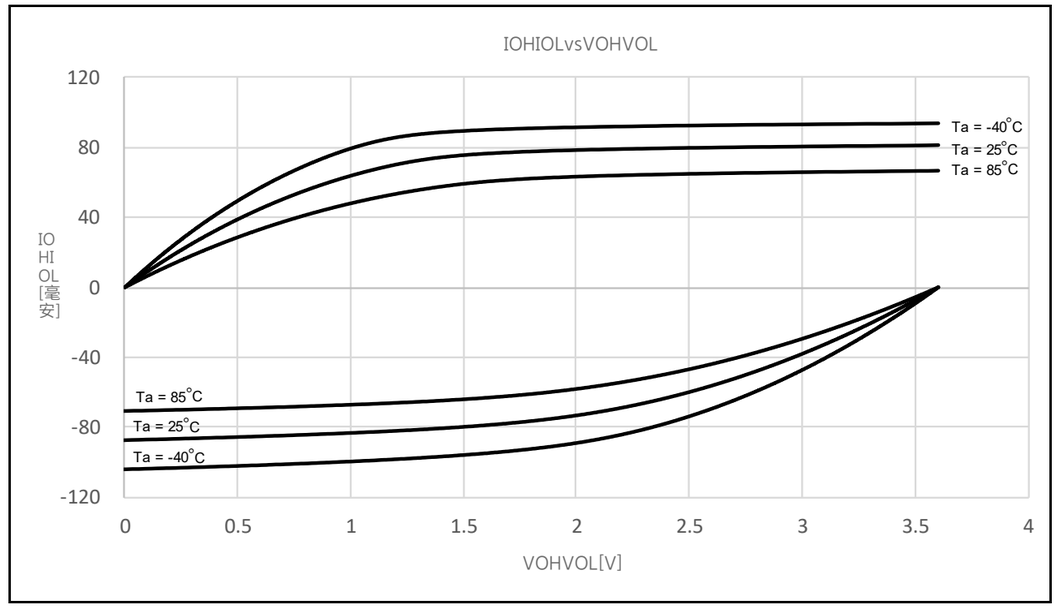


Figure 48.12 选择中间驱动输出时，VCC=3.6V时的VOHVOL和IOHIOL温度特性（参考数据）

48.2.8 IIC I/O Pin Output Characteristics

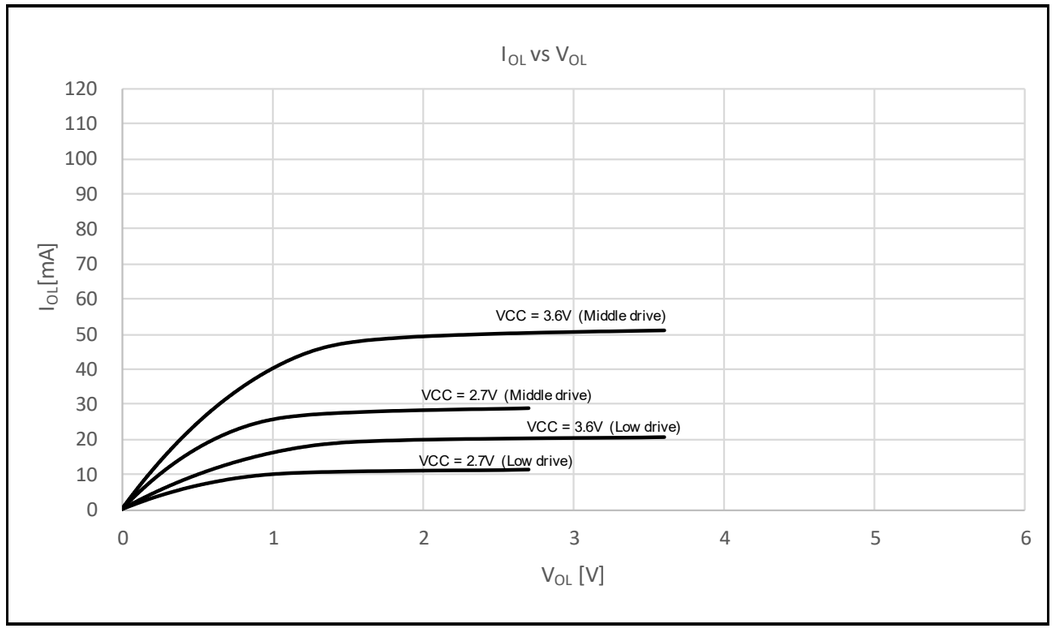


Figure 48.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C

48.2.8 IICIO引脚输出特性

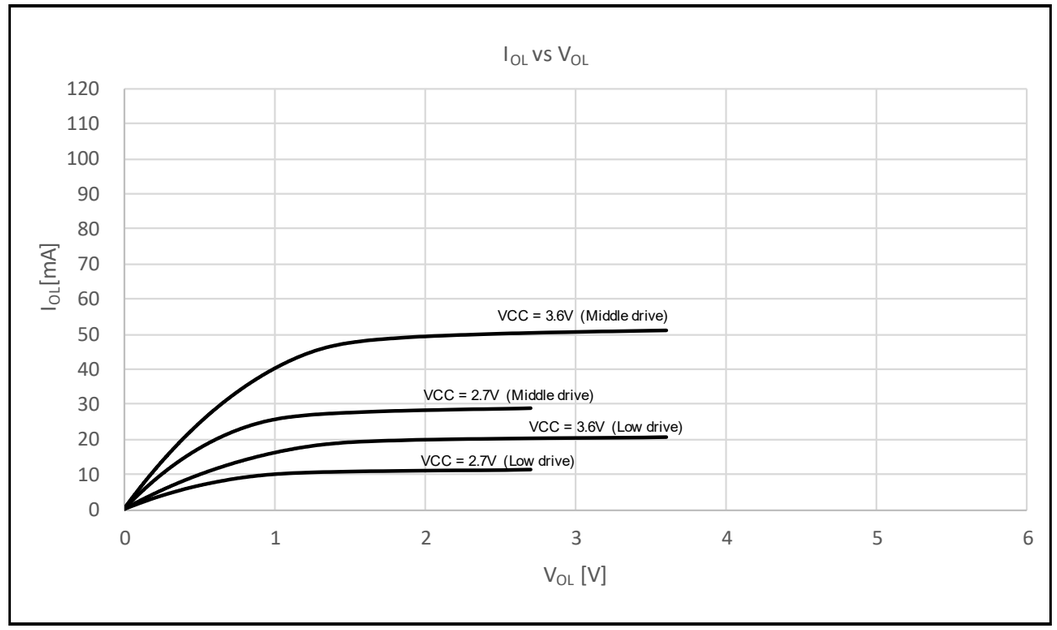


Figure 48.13 Ta=25°C时的VOHVOL和IOHIOL电压特性

48.2.9 Operating and Standby Current

Table 48.11 Operating and standby current (1) (1 of 2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 48 MHz	I_{CC}	8.4	-	mA	*7
				ICLK = 32 MHz		5.9	-		
				ICLK = 16 MHz		3.5	-		
				ICLK = 8 MHz		2.3	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 48 MHz		17.9	-		
				ICLK = 32 MHz		12.4	-		
				ICLK = 16 MHz		7.0	-		
				ICLK = 8 MHz		4.3	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 48 MHz		21.2	-		*9
				ICLK = 32 MHz		16.0	-		*8
				ICLK = 16 MHz		8.8	-		
				ICLK = 8 MHz		5.1	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 48 MHz		-	56.0		*9
		Sleep mode	All peripheral clock disabled*5	ICLK = 48 MHz		3.7	-		*7
				ICLK = 32 MHz		2.7	-		
				ICLK = 16 MHz		2.0	-		
				ICLK = 8 MHz		1.5	-		
			All peripheral clock enabled*5	ICLK = 48 MHz		16.4	-		*9
				ICLK = 32 MHz		12.7	-		*8
				ICLK = 16 MHz		7.2	-		
				ICLK = 8 MHz		4.3	-		
		Increase during BGO operation*6				2.5	-		-
	Middle-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I_{CC}	2.5	-	mA	*7
				ICLK = 8 MHz		2.1	-		
				ICLK = 1 MHz		1.0	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 12 MHz		5.2	-		
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.3	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 12 MHz		6.5	-		*8
				ICLK = 8 MHz		4.8	-		
				ICLK = 1 MHz		1.6	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 12 MHz		-	23.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 12 MHz		1.4	-		*7
				ICLK = 8 MHz		1.3	-		
				ICLK = 1 MHz		0.9	-		
			All peripheral clock enabled*5	ICLK = 12 MHz		5.3	-		*8
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.5	-		
		Increase during BGO operation*6				2.5	-		-

48.2.9 工作和待机电流

Table 48.11 工作和待机电流(1)(1of2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter					Symbol	Typ*10	Max	Unit	测试条件
供电电流*1	High-speed mode*2	正常模式	禁用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 48 MHz	I_{CC}	8.4	-	mA	*7
				ICLK = 32 MHz		5.9	-		
				ICLK = 16 MHz		3.5	-		
				ICLK = 8 MHz		2.3	-		
			所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 48 MHz		17.9	-		
				ICLK = 32 MHz		12.4	-		
				ICLK = 16 MHz		7.0	-		
				ICLK = 8 MHz		4.3	-		
			启用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 48 MHz		21.2	-		*9
				ICLK = 32 MHz		16.0	-		*8
				ICLK = 16 MHz		8.8	-		
				ICLK = 8 MHz		5.1	-		
			启用所有外设时钟，从SRAM执行代码*5	ICLK = 48 MHz		-	56.0		*9
		睡眠模式	所有外设时钟禁用*5	ICLK = 48 MHz		3.7	-		*7
				ICLK = 32 MHz		2.7	-		
				ICLK = 16 MHz		2.0	-		
				ICLK = 8 MHz		1.5	-		
			启用所有外设时钟*5	ICLK = 48 MHz		16.4	-		*9
				ICLK = 32 MHz		12.7	-		*8
				ICLK = 16 MHz		7.2	-		
				ICLK = 8 MHz		4.3	-		
		BGO运行时增加*6				2.5	-		-
	Middle-speed mode*2	正常模式	禁用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 12 MHz	I_{CC}	2.5	-	mA	*7
				ICLK = 8 MHz		2.1	-		
				ICLK = 1 MHz		1.0	-		
			所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 12 MHz		5.2	-		
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.3	-		
			启用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 12 MHz		6.5	-		*8
				ICLK = 8 MHz		4.8	-		
				ICLK = 1 MHz		1.6	-		
			启用所有外设时钟，从SRAM执行代码*5	ICLK = 12 MHz		-	23.0		
		睡眠模式	所有外设时钟禁用*5	ICLK = 12 MHz		1.4	-		*7
				ICLK = 8 MHz		1.3	-		
				ICLK = 1 MHz		0.9	-		
			启用所有外设时钟*5	ICLK = 12 MHz		5.3	-		*8
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.5	-		
		BGO运行时增加*6				2.5	-		-

Table 48.11 Operating and standby current (1) (2 of 2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

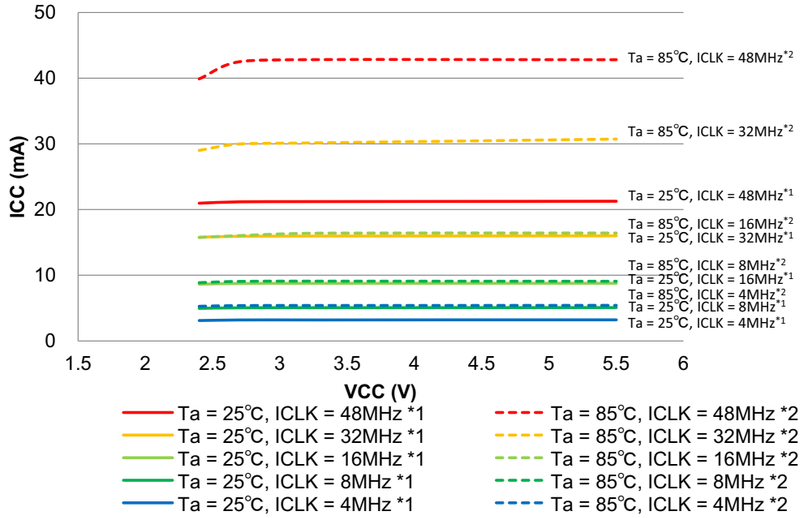
Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.4	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.6	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 1 MHz		1.1	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	2.5		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.3	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		1.0	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I_{CC}	1.8	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		3.0	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz		3.3	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz		-	9.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		1.4	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		2.9	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	9.3	-	µA	*8
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		17.2	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	106.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		6.0	-		
			All peripheral clock enabled*5	ICLK = 32.768 kHz		14.0	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. FCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.
Note 8. FCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.

Table 48.11 工作和待机电流(1)(2of2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter					Symbol	Typ*10	Max	Unit	测试条件
供电电流*1	Low-speed mode*3	正常模式	禁用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 1 MHz	I_{CC}	0.4	-	mA	*7
			所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 1 MHz		0.6	-		
			启用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 1 MHz		1.1	-		*8
			启用所有外设时钟，从SRAM执行代码*5	ICLK = 1 MHz		-	2.5		
		睡眠模式	所有外设时钟禁用*5	ICLK = 1 MHz		0.3	-		*7
			启用所有外设时钟*5	ICLK = 1 MHz		1.0	-		*8
	Low-voltage mode*3	正常模式	禁用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 4 MHz	I_{CC}	1.8	-	mA	*7
			所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 4 MHz		3.0	-		
			启用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 4 MHz		3.3	-		*8
			启用所有外设时钟，从SRAM执行代码*5	ICLK = 4 MHz		-	9.0		
		睡眠模式	所有外设时钟禁用*5	ICLK = 4 MHz		1.4	-		*7
			启用所有外设时钟*5	ICLK = 4 MHz		2.9	-		*8
	Subosc-speed mode*4	正常模式	禁用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 32.768 kHz	I_{CC}	9.3	-	µA	*8
			启用所有外设时钟，同时(1)代码从闪存执行*5	ICLK = 32.768 kHz		17.2	-		
			启用所有外设时钟，从SRAM执行代码*5	ICLK = 32.768 kHz		-	106.0		
		睡眠模式	所有外设时钟禁用*5	ICLK = 32.768 kHz		6.0	-		
			启用所有外设时钟*5	ICLK = 32.768 kHz		14.0	-		

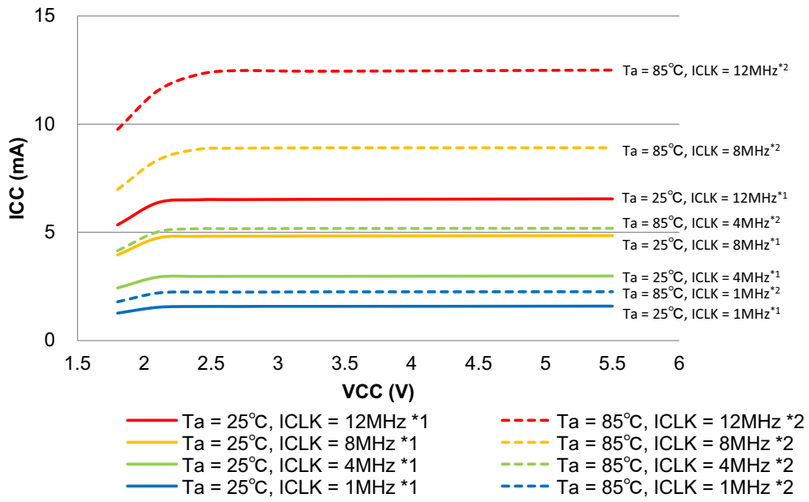
Note 1. 电源电流值不包括所有引脚的输出充电放电电流。这些值适用于内部上拉时MOS处于关闭状态。
Note 2. 时钟源是HOCO。
Note 3. 时钟源为MOCO。
Note 4. 时钟源是子时钟振荡器。
Note 5. 这不包括BGO操作。
Note 6. 这是在程序执行期间用于数据存储的闪存的编程或擦除的增加。
Note 7. FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频。
Note 8. FCLK、PCLKA、PCLKB、PCLKC和PCLKD与ICLK的频率相同。
Note 9. FCLK和PCLKB设置为2分频，P CLKA、PCLKC和PCLKD的频率与ICLK的频率相同。
Note 10. VCC = 3.3 V.



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

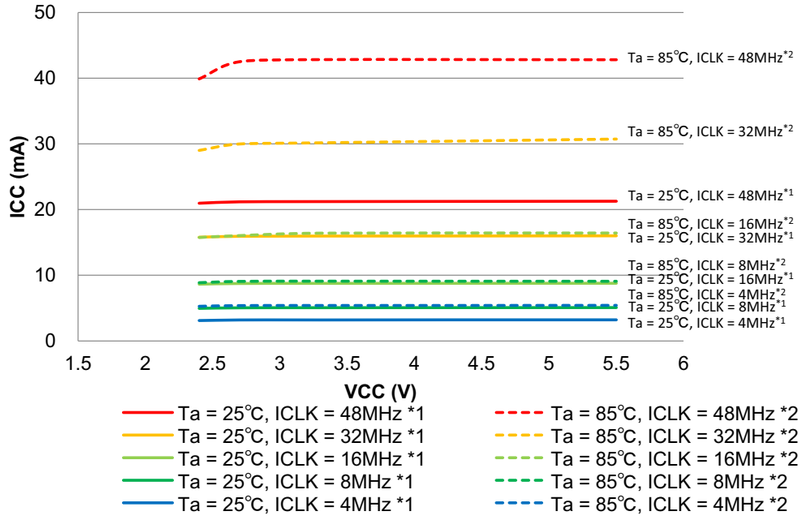
Figure 48.14 Voltage dependency in high-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

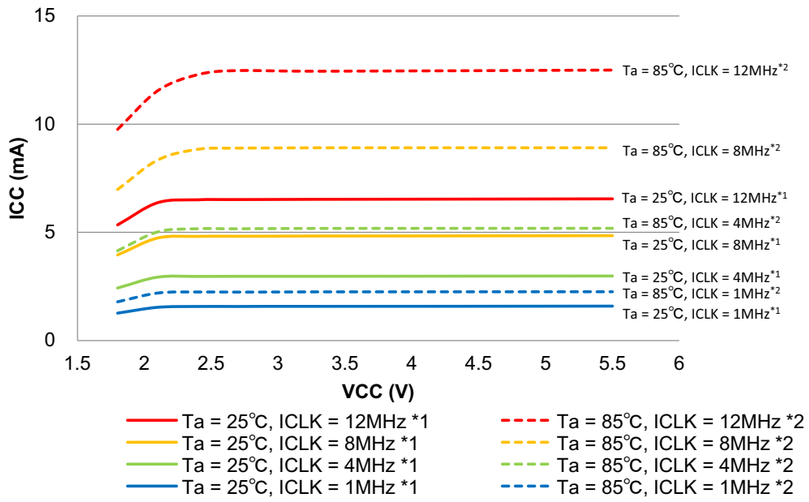
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 48.15 Voltage dependency in middle-speed mode (reference data)



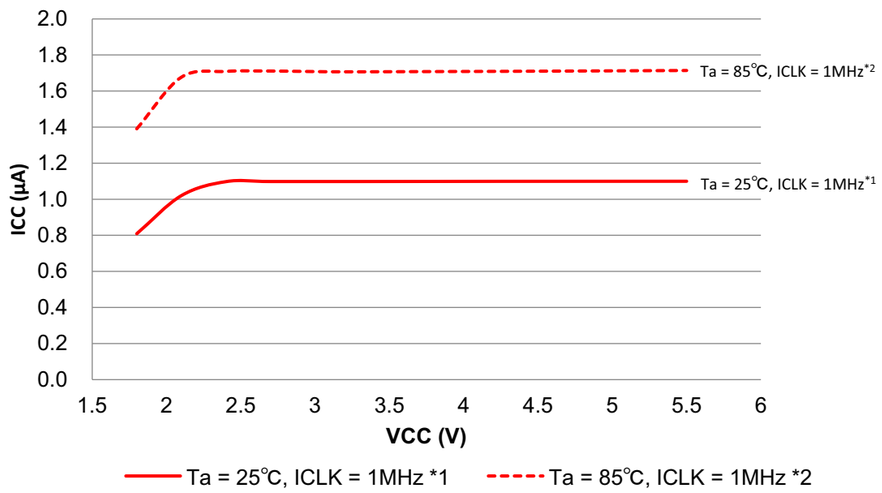
注1.除任何BGO操作外，所有外设操作均正常运行。这是产品评估期间样品芯的实际测量值的平均值。注2.除任何BGO操作外，所有外设操作都在最大运行。这是产品评估期间上限样品的实际测量值的平均值。

Figure 48.14 高速模式下的电压依赖性（参考数据）



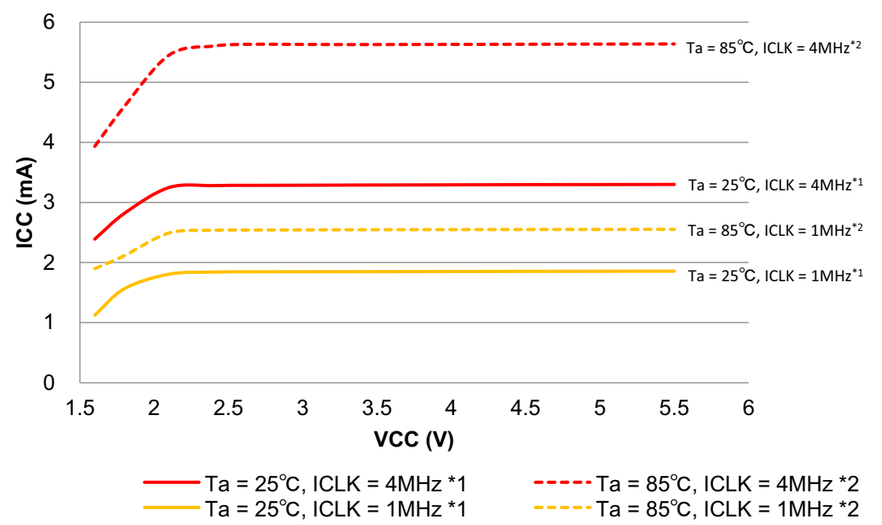
注1.除任何BGO操作外，所有外设操作均正常运行。这是产品评估期间样品芯的实际测量值的平均值。注2.除任何BGO操作外，所有外设操作都在最大运行。这是产品评估期间上限样品的实际测量值的平均值。

Figure 48.15 中速模式下的电压依赖性（参考数据）



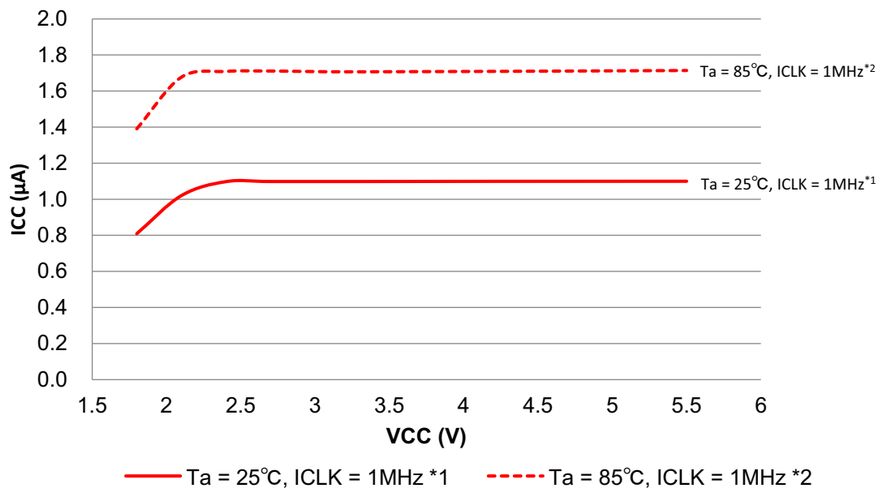
Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 48.16 Voltage dependency in low-speed mode (reference data)



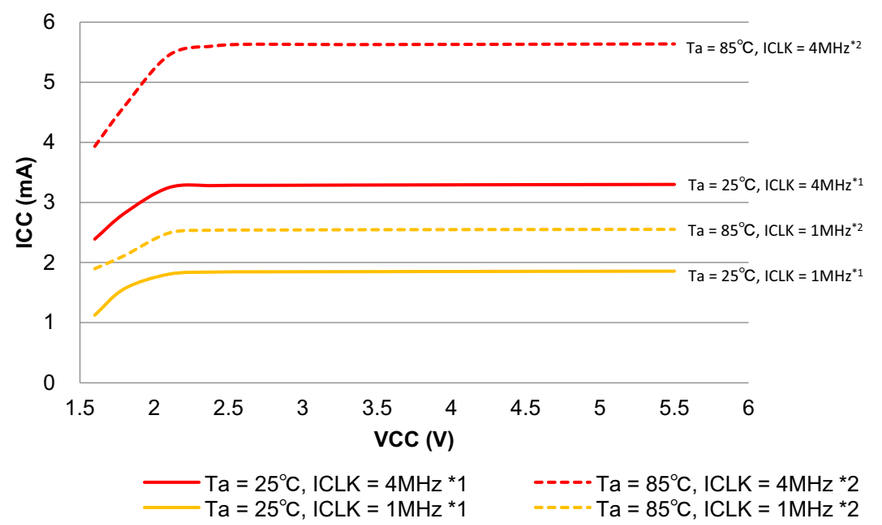
Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 48.17 Voltage dependency in low-voltage mode (reference data)



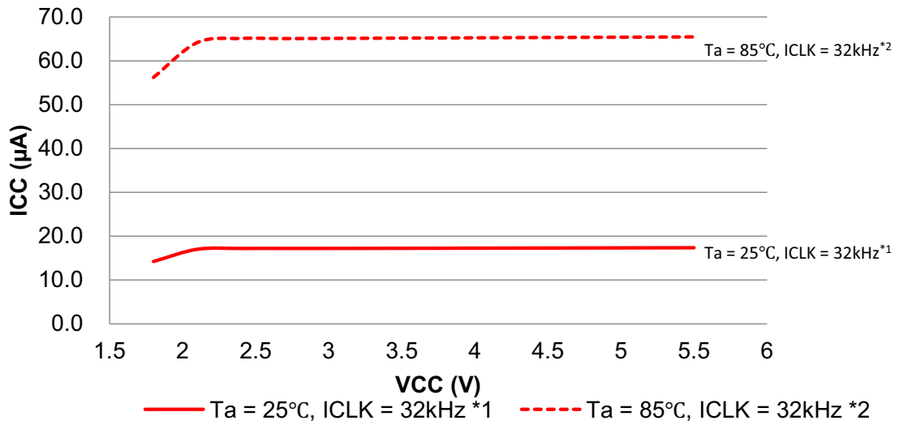
注1.除任何BGO操作外，所有外设操作均正常运行。这是产品评估期间样品芯的实际测量值的平均值。注2.除任何BGO操作外，所有外设操作都在最大运行。这是产品评估期间上限样品的实际测量值的平均值。

Figure 48.16 低速模式下的电压依赖性（参考数据）



注1.除任何BGO操作外，所有外设操作均正常运行。这是产品评估期间样品芯的实际测量值的平均值。注2.除任何BGO操作外，所有外设操作都在最大运行。这是产品评估期间上限样品的实际测量值的平均值。

Figure 48.17 低压模式下的电压依赖性（参考数据）



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

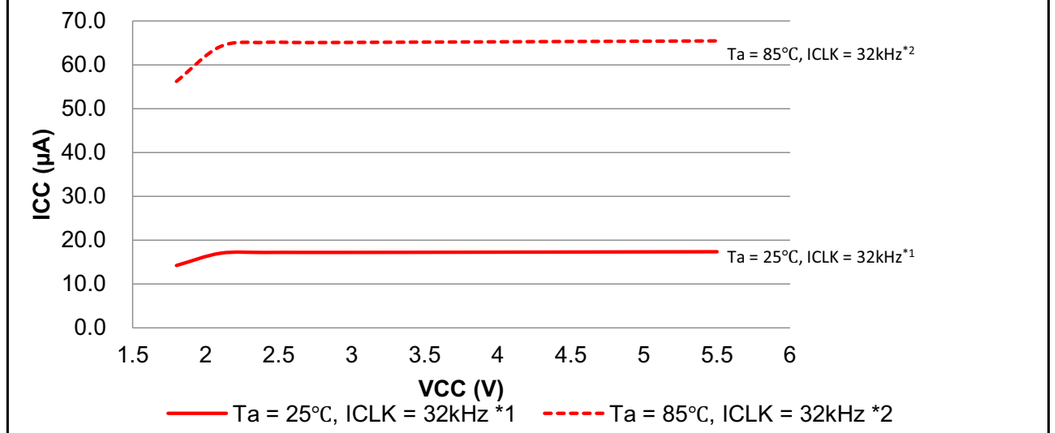
Figure 48.18 Voltage dependency in subosc-speed mode (reference data)

Table 48.12 Operating and standby current (2)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Typ*4	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.9	5.0	µA	PSMCR.PSMC[1:0] = 01b (48-KB SRAM on)
		T_a = 55°C		1.5	8.1		
		T_a = 85°C		3.6	22.1		
		T_a = 25°C		1.0	5.6		PSMCR.PSMC[1:0] = 00b (All SRAM on)
		T_a = 55°C		1.6	8.4		
		T_a = 85°C		4.3	26.7		
	Increment for RTC operation with low-speed on-chip oscillator*3			0.5	-		-
	Increment for RTC operation with sub-clock oscillator*3			0.4	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.2	-		SOMCR.SODRV[1:0] are 00b (Normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.
Note 4. VCC = 3.3 V.



注1.除任何BGO操作外，所有外设操作均正常运行。这是产品评估期间样品芯的实际测量值的平均值。注2.除任何BGO操作外，所有外设操作都在最大运行。这是产品评估期间上限样品的实际测量值的平均值。

Figure 48.18 subosc速度模式下的电压依赖性（参考数据）

Table 48.12 工作和待机电流(2)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Typ*4	Max	Unit	测试条件
Supply current*1	软件待机模式*2	T_a = 25°C	I_{CC}	0.9	5.0	µA	PSMCR.PSMC[1:0] = 01b (48-KB SRAM on)
		T_a = 55°C		1.5	8.1		
		T_a = 85°C		3.6	22.1		
		T_a = 25°C		1.0	5.6		PSMCR.PSMC[1:0] = 00b (All SRAM on)
		T_a = 55°C		1.6	8.4		
		T_a = 85°C		4.3	26.7		
	使用低速片上振荡器*3的RTC操作增量			0.5	-		-
	使用副时钟振荡器的RTC操作增量*3			0.4	-		SOMCR.SODRV[1:0]为11b（低功耗模式3）
				1.2	-		SOMCR.SODRV[1:0] are 00b (Normal mode)

Note 1. 电源电流值不包括所有引脚的输出充电放电电流。这些值适用于内部上拉时MOS处于关闭状态。
Note 2. IWDT和LVD未运行。
Note 3. 包括子振荡电路或低速片上振荡器的电流。
Note 4. VCC = 3.3 V.

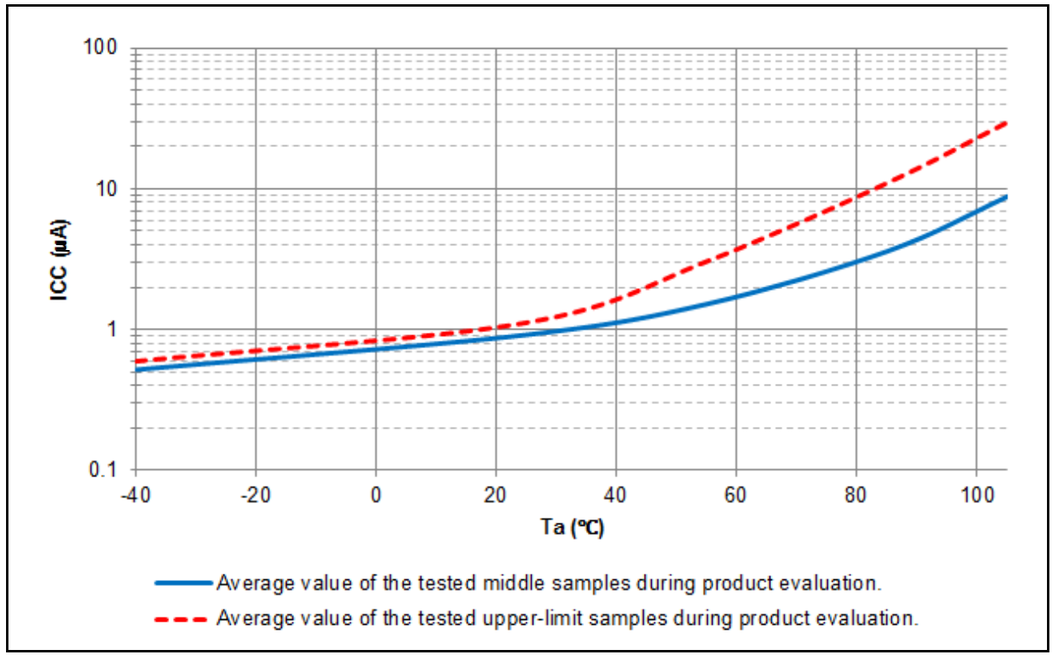


Figure 48.19 Temperature dependency in Software Standby mode 48-KB SRAM on (reference data)

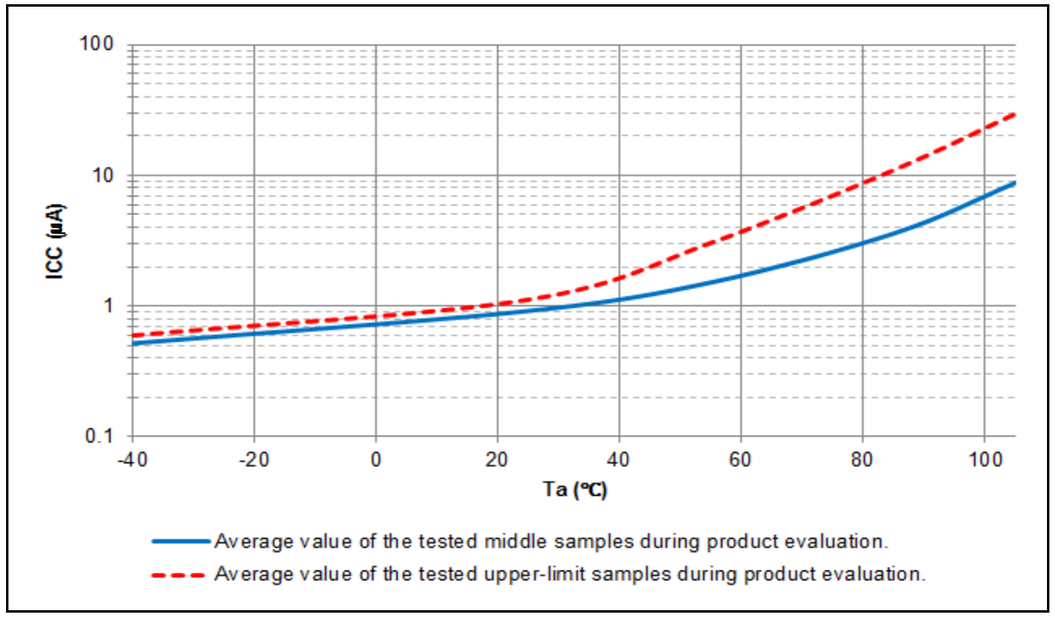


Figure 48.20 Temperature dependency in Software Standby mode all SRAM on (reference data)

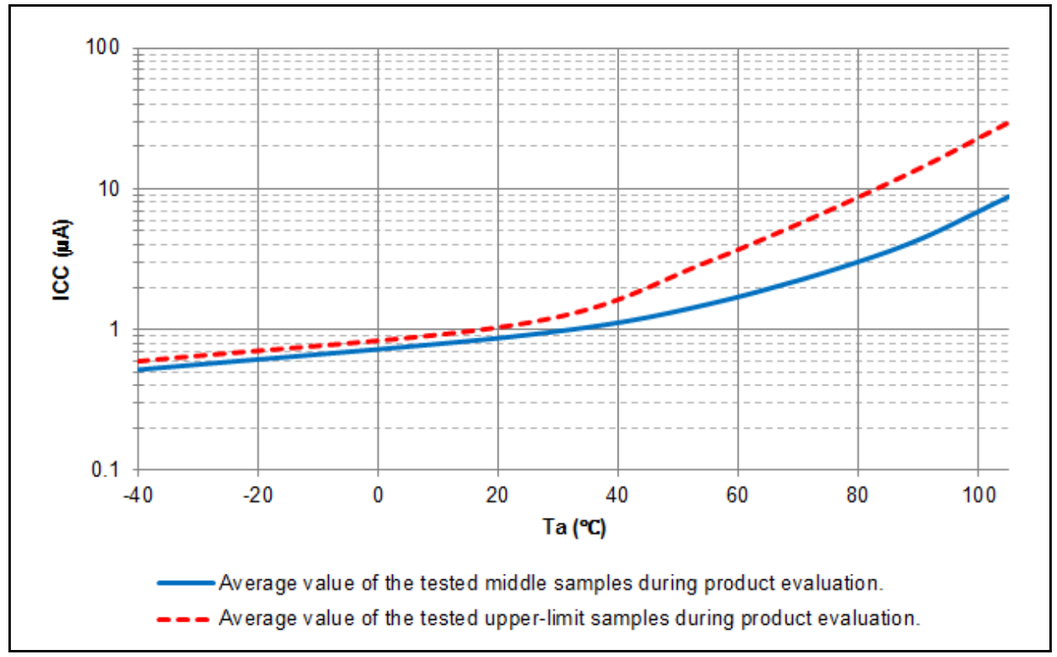


Figure 48.19 软件待机模式下的温度依赖性48-KBSRAM开启（参考数据）

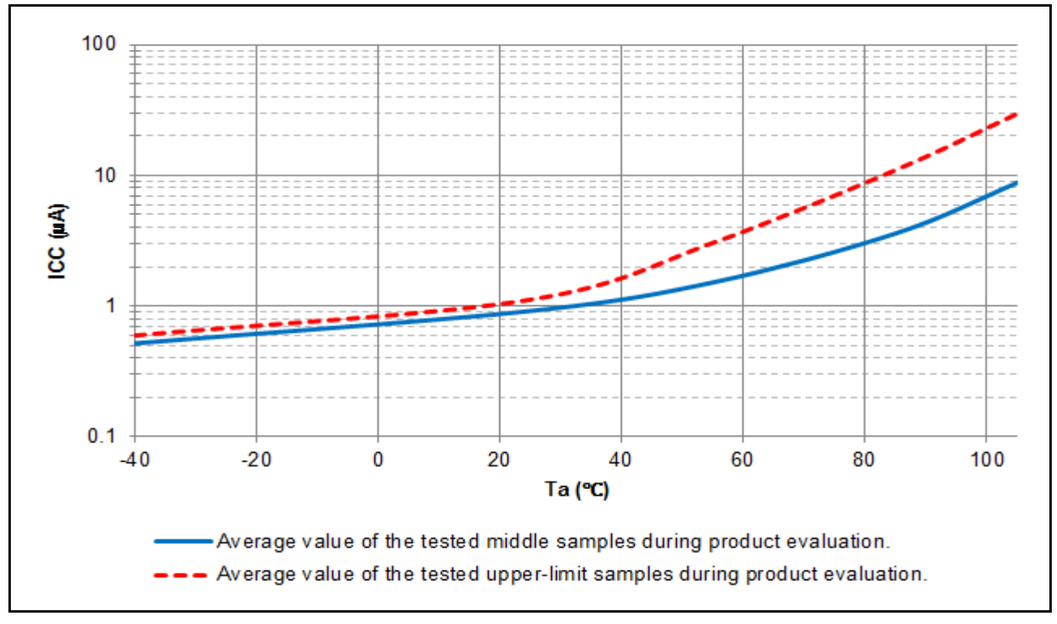


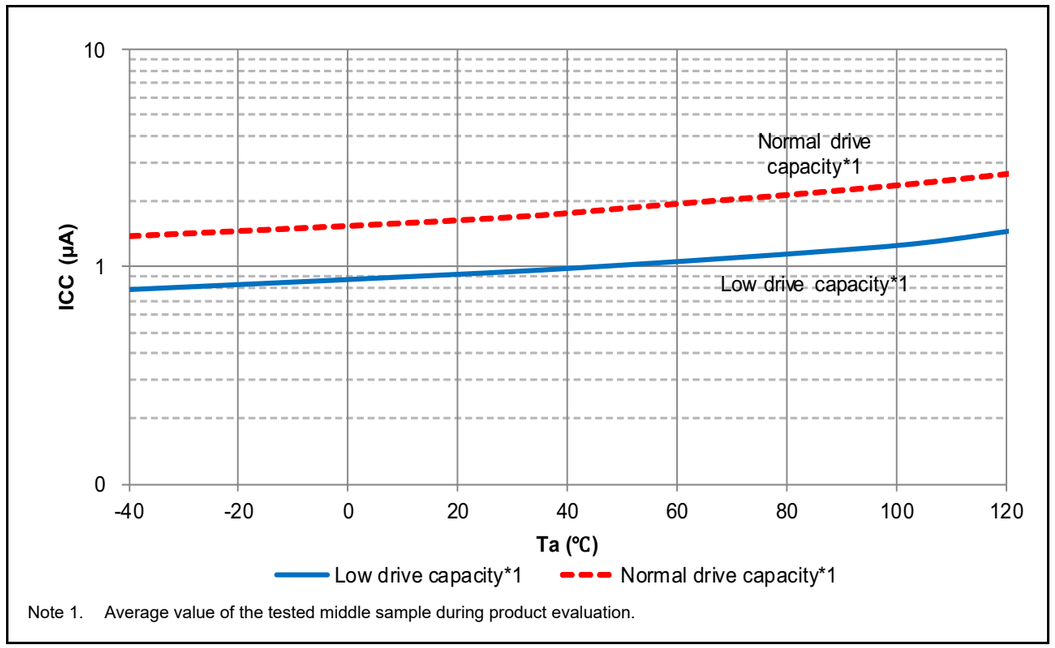
Figure 48.20 软件待机模式下所有SRAM开启时的温度依赖性（参考数据）

Table 48.13 Operating and standby current (3)

Conditions: VCC = AVCC0 = 0V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0V

Parameter			Symbol	Typ	Max	Unit	Test conditions
Supply current*1	RTC operation when VCC is off	T_a = 25°C	I_{CC}	0.8	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)
		T_a = 55°C		0.9	-		
		T_a = 85°C		1.1	-		
		T_a = 25°C		0.9	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)
		T_a = 55°C		1.0	-		
		T_a = 85°C		1.2	-		
		T_a = 25°C		1.6	-		VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.8	-		
		T_a = 85°C		2.1	-		
		T_a = 25°C		1.7	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.9	-		
		T_a = 85°C		2.2	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.



Note 1. Average value of the tested middle sample during product evaluation.

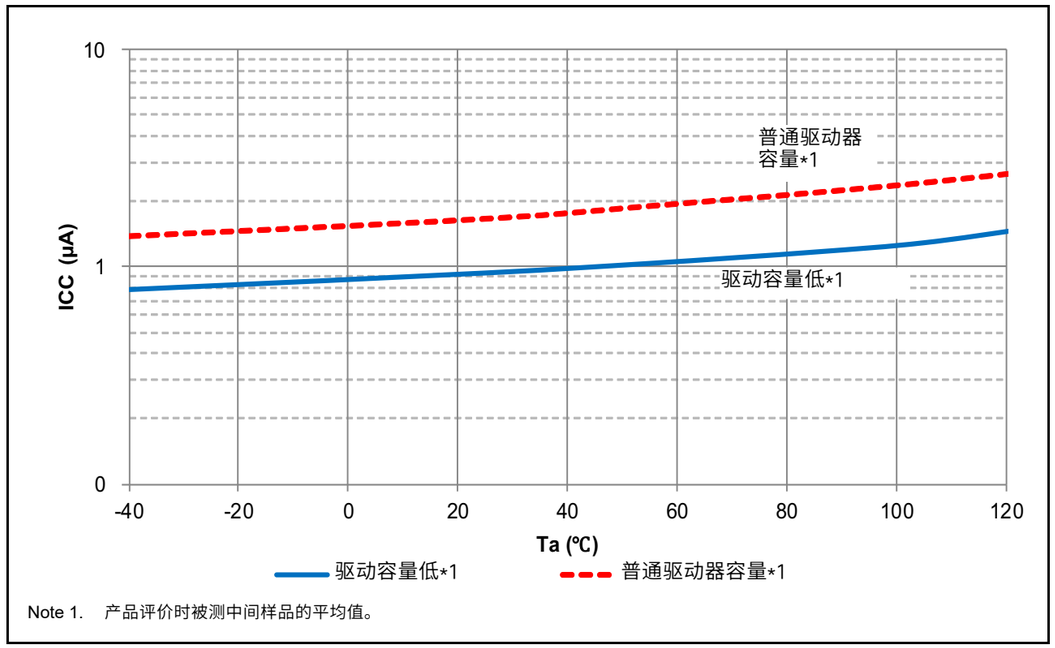
Figure 48.21 Temperature dependency of RTC operation with VCC off (reference data)

Table 48.13 工作和待机电流(3)

Conditions: VCC = AVCC0 = 0V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0V

Parameter			Symbol	Typ	Max	Unit	测试条件
Supply current*1	VCC关闭时的RTC操作	T_a = 25°C	I_{CC}	0.8	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0]=11b（低功耗模式3）
		T_a = 55°C		0.9	-		
		T_a = 85°C		1.1	-		
		T_a = 25°C		0.9	-		VBATT = 3.3 V SOMCR.SORDRV[1:0]=11b（低功耗模式3）
		T_a = 55°C		1.0	-		
		T_a = 85°C		1.2	-		
		T_a = 25°C		1.6	-		VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.8	-		
		T_a = 85°C		2.1	-		
		T_a = 25°C		1.7	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.9	-		
		T_a = 85°C		2.2	-		

Note 1. 电源电流值不包括所有引脚的输出充电放电电流。这些值适用于内部上拉时MOS处于关闭状态。



Note 1. 产品评价时被测中间样品的平均值。

Figure 48.21 VCC关闭时RTC操作的温度依赖性（参考数据）

Table 48.14 Operating and standby current (4)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V, VREFH0 = 2.7 V to AVCC0

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During A/D conversion (at high-speed conversion)		I_{AVCC}	-	-	3.0	mA	-
	During A/D conversion (at low power conversion)			-	-	1.0	mA	-
	During D/A conversion (per channel)*1			-	0.4	0.8	mA	-
	Waiting for A/D and D/A conversion (all units)*6			-	-	1.0	µA	-
Reference power supply current	During A/D conversion		I_{REFH0}	-	-	150	µA	-
	Waiting for A/D conversion (all units)			-	-	60	nA	-
	During D/A conversion		I_{REFH}	-	50	100	µA	-
	Waiting for D/A conversion (all units)			-	-	100	µA	-
Temperature sensor			I_{TNS}	-	75	-	µA	-
Low-Power Analog Comparator operating current	Window mode		I_{CMPLP}	-	15	-	µA	-
	Comparator High-speed mode			-	10	-	µA	-
	Comparator Low-speed mode			-	2	-	µA	-
	Comparator Low-speed mode using DAC8			-	820	-	µA	-
Operational Amplifier operating current	Low power mode	1 unit operating	I_{AMP}	-	2.5	4.0	µA	-
	High speed mode	1 unit operating		-	140	220	µA	-
LCD operating current	External resistance division method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD1}*5	-	0.34	-	µA	-
USB operating current	During USB communication operation under the following settings and conditions: • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.		I_{USBH}*2	-	4.3 (VCC) 0.9 (VCC_USB)*4	-	mA	-
	During USB communication operation under the following settings and conditions: • Device controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Device controller operation is set to full-speed mode (pull up the USB_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU during the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. Current flowing only to the LCD controller. Not including the current that flows through the LCD panel.
Note 6. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 Module Stop bit) is in the module-stop state.

Table 48.14 工作和待机电流(4)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V, VREFH0 = 2.7 V to AVCC0

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
模拟电源电流	AD转换期间（高速转换时）		I_{AVCC}	-	-	3.0	mA	-
	AD转换期间（低功率转换时）			-	-	1.0	mA	-
	DA转换期间（每个通道）*1			-	0.4	0.8	mA	-
	等待AD和DA转换（所有单位）*6			-	-	1.0	µA	-
参考电源电流	在AD转换期间		I_{REFH0}	-	-	150	µA	-
	等待AD转换（所有单位）			-	-	60	nA	-
	DA转换期间		I_{REFH}	-	50	100	µA	-
	等待DA转换（所有单位）			-	-	100	µA	-
温度感应器			I_{TNS}	-	75	-	µA	-
Low-Power Analog 比较器工作电流	窗口模式		I_{CMPLP}	-	15	-	µA	-
	比较器高速模式			-	10	-	µA	-
	比较器低速模式			-	2	-	µA	-
	使用DAC8的比较器低速模式			-	820	-	µA	-
Operational 放大器工作电流	低功耗模式	1个单位运营	I_{AMP}	-	2.5	4.0	µA	-
	高速模式	1个单位运营		-	140	220	µA	-
液晶工作电流	外部电阻分压方法fLCD=fSUB=128Hz 13偏置 4-timeslice		I_{LCD1}*5	-	0.34	-	µA	-
USB工作电流	在以下设置和条件下进行USB通信操作期间： 主机控制器操作设置为全速模式BulkOUT传输（64字节）×1，批量IN传输（64字节）×1 通过1米连接外围设备来自USB端口的USB电缆。		I_{USBH}*2	-	4.3 (VCC) 0.9 (VCC_USB)*4	-	mA	-
	在以下设置和条件下进行USB通信操作期间： 设备控制器操作设置为全速模式BulkOUT传输（64字节）×1，批量IN传输（64字节）×1 通过1-连接主机设备米USB电缆从USB端口。		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	在以下设置和条件下处于挂起状态： 设备控制器操作设置为全速模式（拉起USB_DP引脚） 软件待机模式 通过USB端口通过1米长的USB电缆连接主机设备。		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-

Note 1. 基准电源电流包含在DA转换的电源电流值中。
Note 2. 仅由USBFS消耗的电流。
Note 3. 包括从USB_DP引脚的上拉电阻提供给主机设备下拉电阻的电流，以及MCU在挂起状态期间消耗的电流。
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. 电流仅流向LCD控制器。不包括流过LCD面板的电流。
Note 6. 当MCU处于软件待机模式或MSTPCRD.MSTPD16（ADC140模块停止位）处于模块停止状态时。

Table 48.15 Operating and standby current (5)

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, Ta = +25°C

Parameter		Symbol	Min	Typ		Max	Unit	Test conditions
				Transmit output power				
				0 dBm	4 dBm			
BLE operating current (When DC-DC converter is selected)	Transmit mode, 2 Mbps	Idd_tx	-	4.5	8.7	-	mA	-
	Transmit mode, 1 Mbps		-			-	mA	-
	Transmit mode, 500 kbps		-			-	mA	-
	Transmit mode, 125 kbps		-			-	mA	-
	Receive mode, 2 Mbps Prf = -67 dBm	Idd_rx	-	3.3	3.5	-	mA	-
	Receive mode, 1 Mbps Prf = -67 dBm		-			-	mA	-
	Receive mode, 500 kbps Prf = -72 dBm		-			-	mA	-
	Receive mode, 125 kbps Prf = -79 dBm		-			-	mA	-
	Idle mode	Idd_idle	-	0.5		-	mA	-
	Deep sleep mode	Idd_slp	-	1.5		-	µA	-
	Power down mode	Idd_down	-	0.1		-	µA	-
BLE operating current (When linear regulator is selected)	Transmit mode, 2 Mbps	Idd_tx	-	10.2	18.1	-	mA	-
	Transmit mode, 1 Mbps		-			-	mA	-
	Transmit mode, 500 kbps		-			-	mA	-
	Transmit mode, 125 kbps		-			-	mA	-
	Receive mode, 2M bps Prf = -67 dBm	Idd_rx	-	6.9		-	mA	-
	Receive mode, 1 Mbps Prf = -67 dBm		-	6.9		-	mA	-
	Receive mode, 500 kbps Prf = -72 dBm		-	6.9		-	mA	-
	Receive mode, 125 kbps Prf = -79 dBm		-	7.1		-	mA	-
	Idd_idle	Idd_idle	-	0.7		-	mA	-
	Idd_slp	Idd_slp	-	1.5		-	µA	-
	Idd_down	Idd_down	-	0.1		-	µA	-

Table 48.15 工作和待机电流(5)

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, Ta = +25°C

Parameter		Symbol	Min	Typ		Max	Unit	测试条件
				发射输出功率				
				0 dBm	4 dBm			
BLE工作电流（选择DC-DC转换器时）	传输模式，2Mbps	Idd_tx	-	4.5	8.7	-	mA	-
	传输模式，1Mbps		-			-	mA	-
	传输模式，500kbps		-			-	mA	-
	传输模式，125kbps		-			-	mA	-
	接收模式，2Mbps Prf = -67 dBm	Idd_rx	-	3.3	3.5	-	mA	-
	接收模式，1Mbps Prf = -67 dBm		-			-	mA	-
	接收模式，500kbps Prf = -72 dBm		-			-	mA	-
	接收模式，125kbps Prf = -79 dBm		-			-	mA	-
	空闲模式	Idd_idle	-	0.5		-	mA	-
	深度睡眠模式	Idd_slp	-	1.5		-	µA	-
	掉电模式	Idd_down	-	0.1		-	µA	-
BLE工作电流（选择线性稳压器时）	传输模式，2Mbps	Idd_tx	-	10.2	18.1	-	mA	-
	传输模式，1Mbps		-			-	mA	-
	传输模式，500kbps		-			-	mA	-
	传输模式，125kbps		-			-	mA	-
	接收模式，2Mbps Prf = -67 dBm	Idd_rx	-	6.9		-	mA	-
	接收模式，1Mbps Prf = -67 dBm		-	6.9		-	mA	-
	接收模式，500kbps Prf = -72 dBm		-	6.9		-	mA	-
	接收模式，125kbps Prf = -79 dBm		-	7.1		-	mA	-
	Idd_idle	Idd_idle	-	0.7		-	mA	-
	Idd_slp	Idd_slp	-	1.5		-	µA	-
	Idd_down	Idd_down	-	0.1		-	µA	-

48.2.10 VCC Rise and Fall Gradient and Ripple Frequency

Table 48.16 Rise and fall gradient characteristics
Conditions: VCC = AVCC0 = 0 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup (normal startup)	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1		0.02	-	-		
	SCI/USB Boot mode*2		0.02	-	2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 48.17 Rising and falling gradient and ripple frequency characteristics
Conditions: VCC = AVCC0 = VCC_USB = 1.8 to 3.6 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).
When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r (VCC)}$	-	-	10	kHz	Figure 48.22 $V_{r (VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 48.22 $V_{r (VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 48.22 $V_{r (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

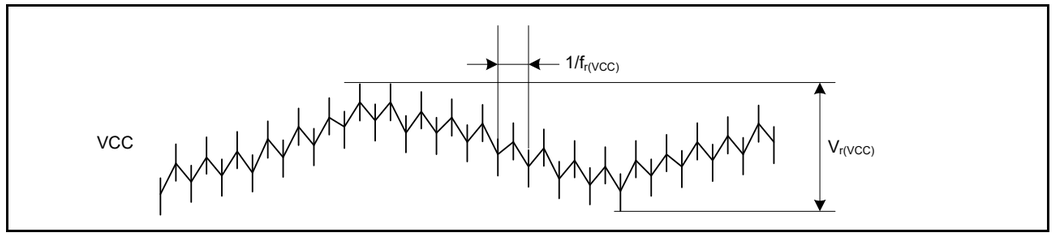


Figure 48.22 Ripple waveform

48.2.10 VCC上升和下降梯度和纹波频率

Table 48.16 上升和下降梯度特性
Conditions: VCC = AVCC0 = 0 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电VCC上升梯度	启动时禁用电压监视器0复位（正常启动）	SrVCC	0.02	-	2	ms/V	-
	电压监视器0启动时启用复位*1		0.02	-	-		
	SCI/USB Boot mode*2		0.02	-	2		

Note 1. When OFS1.LVDAS = 0.
Note 2. 在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

Table 48.17 上升下降梯度和纹波频率特性
Conditions: VCC = AVCC0 = VCC_USB = 1.8 to 3.6 V
纹波电压必须在VCC上限(3.6V)和下限(1.8V)之间的范围内满足允许的纹波频率fr(VCC)。当VCC变化超过VCC±10%时，必须满足允许的电压变化上升下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r (VCC)}$	-	-	10	kHz	Figure 48.22 $V_{r (VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 48.22 $V_{r (VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 48.22 $V_{r (VCC)} \leq VCC \times 0.06$
允许电压变化上升下降梯度	dt/dVCC	1.0	-	-	ms/V	当VCC变化超过VCC±10%

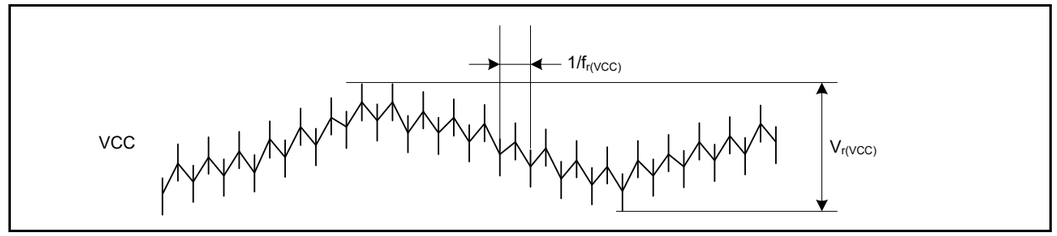


Figure 48.22 纹波波形

48.3 AC Characteristics

48.3.1 Frequency

Table 48.18 Operation frequency value in high-speed operating mode

Conditions: VCC = AVCC0 = 2.4 to 3.6 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 3.6 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 3.6 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKA)*4	2.7 to 3.6 V		-	-	48	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKB)*4	2.7 to 3.6 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 3.6 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*4	2.7 to 3.6 V		-	-	64	
		2.4 to 2.7 V		-	-	16	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 9, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.

Note 5. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 48.23, Clock timing.

Table 48.19 Operation frequency value in Middle-speed mode

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 3.6 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 3.6 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKA)*4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKB)*4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	

48.3 交流特性

48.3.1 Frequency

Table 48.18 高速运行模式下的运行频率值

Conditions: VCC = AVCC0 = 2.4 to 3.6 V

Parameter			Symbol	Min	Typ	Max*5	Unit
运行频率	系统时钟(ICLK)*4	2.7 to 3.6 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 3.6 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
	外设模块时钟(PCLKA)*4	2.7 to 3.6 V		-	-	48	
		2.4 to 2.7 V		-	-	16	
	外设模块时钟(PCLKB)*4	2.7 to 3.6 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	外设模块时钟（PCLKC）*3 *4	2.7 to 3.6 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	外设模块时钟(PCLKD)*4	2.7 to 3.6 V		-	-	64	
		2.4 to 2.7 V		-	-	16	

Note 1. 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用FCLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1 MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

Note 2. 在对闪存进行编程或擦除时，FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

Note 3. 使用14位AD转换器时，PCLKC的下限频率为2.4V或以上时为4MHz，低于2.4V时为1MHz。

Note 4. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD和FCLK之间的频率关系，请参见第9节，时钟生成电路。

Note 5. 工作频率的最大值不包括内部振荡器误差。内部振荡器的误差可以保证操作。有关保证操作范围的详细信息，请参见表48.23，时钟时序。

Table 48.19 中速模式运行频率值

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max*5	Unit
运行频率	系统时钟(ICLK)*4	2.7 to 3.6 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 3.6 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	外设模块时钟(PCLKA)*4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	外设模块时钟(PCLKB)*4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	外设模块时钟（PCLKC）*3 *4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	外设模块时钟(PCLKD)*4	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 9, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 48.23, Clock timing.

Table 48.20 Operation frequency value in Low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 3.6 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK)*1, *3	1.8 to 3.6 V		0.032768	-	1	
	Peripheral module clock (PCLKA)*3	1.8 to 3.6 V		-	-	1	
	Peripheral module clock (PCLKB)*3	1.8 to 3.6 V		-	-	1	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 3.6 V		-	-	1	
	Peripheral module clock (PCLKD)*3	1.8 to 3.6 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.
Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.
Note 3. See section 9, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
Note 4. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 48.23, Clock timing.

Table 48.21 Operation frequency value in low-voltage mode

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	1.8 to 3.6 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1, *2, *4	1.8 to 3.6 V		0.032768	-	4	
	Peripheral module clock (PCLKA)*4	1.8 to 3.6 V		-	-	4	
	Peripheral module clock (PCLKB)*4	1.8 to 3.6 V		-	-	4	
	Peripheral module clock (PCLKC)*3, *4	1.8 to 3.6 V		-	-	4	
	Peripheral module clock (PCLKD)*4	1.8 to 3.6 V		-	-	4	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 9, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 48.23, Clock timing.

Note 1. 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用FCLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note 2. 在对闪存进行编程或擦除时，FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。
Note 3. 使用14位AD转换器时，PCLKC的下限频率为2.4V或以上时为4MHz，低于2.4V时为1MHz。
Note 4. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD和FCLK之间的频率关系，请参见第9节，时钟生成电路。
Note 5. 工作频率的最大值不包括内部振荡器的误差。内部振荡器的误差可以保证操作。有关保证操作范围的详细信息，请参见表48.23，时钟时序。

Table 48.20 低速模式下的运行频率值

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max*4	Unit
运行频率	系统时钟(ICLK)*3	1.8 to 3.6 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK)*1, *3	1.8 to 3.6 V		0.032768	-	1	
	外设模块时钟(PCLKA)*3	1.8 to 3.6 V		-	-	1	
	外设模块时钟(PCLKB)*3	1.8 to 3.6 V		-	-	1	
	外设模块时钟（PCLKC）*2 *3	1.8 to 3.6 V		-	-	1	
	外设模块时钟(PCLKD)*3	1.8 to 3.6 V		-	-	1	

Note 1. 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。
Note 2. 使用AD转换器时，PCLKC的下限频率为1MHz。
Note 3. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD和FCLK之间的频率关系，请参见第9节，时钟生成电路。
Note 4. 工作频率的最大值不包括内部振荡器误差。内部振荡器的误差可以保证操作。有关保证操作范围的详细信息，请参见表48.23，时钟时序。

Table 48.21 低压模式下的工作频率值

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max*5	Unit
运行频率	系统时钟(ICLK)*4	1.8 to 3.6 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1, *2, *4	1.8 to 3.6 V		0.032768	-	4	
	外设模块时钟(PCLKA)*4	1.8 to 3.6 V		-	-	4	
	外设模块时钟(PCLKB)*4	1.8 to 3.6 V		-	-	4	
	外设模块时钟（PCLKC）*3 *4	1.8 to 3.6 V		-	-	4	
	外设模块时钟(PCLKD)*4	1.8 to 3.6 V		-	-	4	

Note 1. 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用FCLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note 2. 在对闪存进行编程或擦除时，FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。
Note 3. 使用14位AD转换器时，PCLKC的下限频率为2.4V或以上时为4MHz，低于2.4V时为1MHz。
Note 4. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD和FCLK之间的频率关系，请参见第9节，时钟生成电路。
Note 5. 工作频率的最大值不包括内部振荡器的误差。内部振荡器的误差可以保证操作。有关保证操作范围的详细信息，请参见表48.23，时钟时序。

Table 48.22 Operation frequency value in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 3.6 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1, *3	1.8 to 3.6 V		27.8528	32.768	37.6832	
	Peripheral module clock (PCLKA)*3	1.8 to 3.6 V		-	-	37.6832	
	Peripheral module clock (PCLKB)*3	1.8 to 3.6 V		-	-	37.6832	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 3.6 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*3	1.8 to 3.6 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 9, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

48.3.2 Clock Timing

Table 48.23 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	-	-	ns	Figure 48.23
EXTAL external clock input high pulse width	t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width	t_{XL}	20	-	-	ns	
EXTAL external clock rising time	t_{Xr}	-	-	5	ns	
EXTAL external clock falling time	t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	-	-	µs	-
EXTAL external clock input frequency	f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 3.6
		-	-	8		1.8 ≤ VCC < 2.4
Main clock oscillator oscillation frequency	f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 3.6
		1	-	8		1.8 ≤ VCC < 2.4
Main clock oscillation stabilization wait time (crystal)*9	$t_{MAINOSCWT}$	-	-	-*9	ms	
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time	t_{LOCO}	-	-	100	µs	Figure 48.24
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	-
Bluetooth-dedicated clock oscillation frequency	f_{BLECK}	-	32	-	MHz	
Bluetooth-dedicated low-speed on-chip oscillator oscillation frequency	$f_{BLELOCO}$	-	32.768	-	kHz	
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time	t_{MOCO}	-	-	1	µs	-
HOCO clock oscillation frequency	f_{HOCO24}	23.64	24	24.36	MHz	Ta = –40 to –20°C 1.8 ≤ VCC ≤ 3.6
		23.76	24	24.24		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 3.6
	f_{HOCO32}	31.52	32	32.48		Ta = –40 to -20°C 1.8 ≤ VCC ≤ 3.6
		31.68	32	32.32		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 3.6
	f_{HOCO48}*4	47.28	48	48.72		Ta = –40 to –20°C 1.8 ≤ VCC ≤ 3.6
		47.52	48	48.48		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 3.6
	f_{HOCO64}*5	63.04	64	64.96		Ta = –40 to –20°C 2.4 ≤ VCC ≤ 3.6
		63.36	64	64.64		Ta = –20 to 85°C 2.4 ≤ VCC ≤ 3.6

Table 48.22 Subosc-speed模式下的运行频率值

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*3	1.8 to 3.6 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1, *3	1.8 to 3.6 V		27.8528	32.768	37.6832	
	外设模块时钟(PCLKA)*3	1.8 to 3.6 V		-	-	37.6832	
	外设模块时钟(PCLKB)*3	1.8 to 3.6 V		-	-	37.6832	
	外设模块时钟（PCLKC）*2 *3	1.8 to 3.6 V		-	-	37.6832	
	外设模块时钟(PCLKD)*3	1.8 to 3.6 V		-	-	37.6832	

Note 1. 无法对闪存进行编程和擦除。
Note 2. 不能使用14位AD转换器。
Note 3. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK, and BCLK.

48.3.2 时钟时序

Table 48.23 时钟计时(1of2)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间	t_{Xcyc}	50	-	-	ns	Figure 48.23
EXTAL外部时钟输入高脉冲宽度	t_{XH}	20	-	-	ns	
EXTAL外部时钟输入低脉冲宽度	t_{XL}	20	-	-	ns	
EXTAL外部时钟上升时间	t_{Xr}	-	-	5	ns	
EXTAL外部时钟下降时间	t_{Xf}	-	-	5	ns	
EXTAL外部时钟输入等待时间*1	t_{EXWT}	0.3	-	-	µs	-
EXTAL外部时钟输入频率	f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 3.6
		-	-	8		1.8 ≤ VCC < 2.4
主时钟振荡器振荡频率	f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 3.6
		1	-	8		1.8 ≤ VCC < 2.4
主时钟振荡稳定等待时间（晶体）*9	$t_{MAINOSCWT}$	-	-	-*9	ms	
LOCO时钟振荡频率	f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO时钟振荡稳定时间	t_{LOCO}	-	-	100	µs	Figure 48.24
IWDT专用时钟振荡频率	f_{ILOCO}	12.75	15	17.25	kHz	-
蓝牙专用时钟振荡频率	f_{BLECK}	-	32	-	MHz	
蓝牙专用低速片上振荡器振荡频率	$f_{BLELOCO}$	-	32.768	-	kHz	
MOCO时钟振荡频率	f_{MOCO}	6.8	8	9.2	MHz	-
MOCO时钟振荡稳定时间	t_{MOCO}	-	-	1	µs	-
HOCO时钟振荡频率	f_{HOCO24}	23.64	24	24.36	MHz	Ta= 40至 20°C1.8≤VCC≤3.6
		23.76	24	24.24		Ta= 20至85°C1.8≤VCC≤3.6
	f_{HOCO32}	31.52	32	32.48		Ta= 40至-20°C1.8≤VCC≤3.6
		31.68	32	32.32		Ta= 20至85°C1.8≤VCC≤3.6
	f_{HOCO48}*4	47.28	48	48.72		Ta= 40至 20°C1.8≤VCC≤3.6
		47.52	48	48.48		Ta= 20至85°C1.8≤VCC≤3.6
	f_{HOCO64}*5	63.04	64	64.96		Ta= 40至 20°C2.4≤VCC≤3.6
		63.36	64	64.64		Ta= 20至85°C2.4≤VCC≤3.6

Table 48.23 Clock timing (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillation stabilization time*6, *7	Except low-voltage mode	t_{HOCO24} t_{HOCO32}	-	-	37.1	µs	Figure 48.25
		t_{HOCO48}	-	-	43.3		
		t_{HOCO64}	-	-	80.6		
	Low-Voltage mode	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	-	-	100.9		
PLL input frequency*2		f_{PLLIN}	4	-	12.5	MHz	-
PLL circuit oscillation frequency*2		f_{PLL}	24	-	64	MHz	-
PLL clock oscillation stabilization time*8		t_{PLL}	-	-	55.5	µs	Figure 48.27
PLL free-running oscillation frequency		f_{PLLFR}	-	8	-	MHz	-
Sub-clock oscillator oscillation frequency		f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization time*3		t_{SUBOSC}	-	-	-*3	s	Figure 48.28

Note 1. Time until the clock can be used after the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. The VCC range that the PLL can be used is 2.4 to 3.6 V.
Note 3. After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapses, that is greater than or equal to the value recommended by the oscillator manufacturer.
Note 4. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 3.6 V.
Note 5. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 3.6 V.
Note 6. This is a characteristic when HOCOCR.HCSTP bit is set to 0 (oscillation) in MOCO stop state.
When HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 7. Whether stabilization time has elapsed can be confirmed by OSCSF.HOCOSF.
Note 8. This is a characteristic when PLLCR.PLLSTP bit is set to 0 (operation) in MOCO stop state.
When PLLCR.PLLSTP bit is set to 0 (operation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 9. When setting up the main clock, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended stabilization time. After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCSF.MOSCSF flag to confirm that it is 1, then start using the main clock.

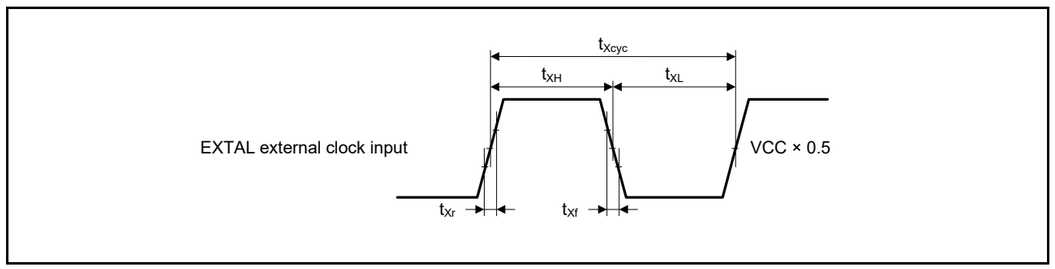


Figure 48.23 EXTAL external clock input timing

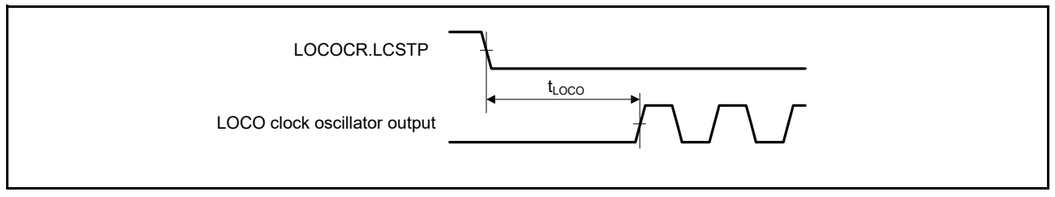


Figure 48.24 LOCO clock oscillation start timing

Table 48.23 时钟计时（2个中的2个）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
HOCO时钟振荡稳定时间*6、*7	低压模式除外	t_{HOCO24} t_{HOCO32}	-	-	37.1	µs	Figure 48.25
		t_{HOCO48}	-	-	43.3		
		t_{HOCO64}	-	-	80.6		
	Low-Voltage mode	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	-	-	100.9		
PLL input frequency*2		f_{PLLIN}	4	-	12.5	MHz	-
PLL电路振荡频率*2		f_{PLL}	24	-	64	MHz	-
PLL时钟振荡稳定时间*8		t_{PLL}	-	-	55.5	µs	Figure 48.27
PLL自由振荡频率		f_{PLLFR}	-	8	-	MHz	-
副时钟振荡器振荡频率		f_{SUB}	-	32.768	-	kHz	-
副时钟振荡稳定时间*3		t_{SUBOSC}	-	-	-*3	s	Figure 48.28

Note 1. 当外部时钟稳定时，主时钟振荡器停止位(MOSCCR.MOSTP)设置为0（运行）后，时钟可以使用的时间。
Note 2. PLL可以使用的VCC范围是2.4到3.6V。
Note 3. 更改SOSCCR.SOSTP位的设置使副时钟振荡器工作后，只有在副时钟振荡稳定等待时间过去后才开始使用副时钟振荡器，即大于或等于推荐值振荡器制造商。
Note 4. 48-MHzHOCO可在1.8V至3.6V的VCC范围内使用。
Note 5. 64MHzHOCO可在2.4V至3.6V的VCC范围内使用。
Note 6. 这是在MOCO停止状态下将HOCOCR.HCSTP位设置为0（振荡）时的特性。
在MOCO振荡期间，当HOCOCR.HCSTP位设置为0（振荡）时，该规范将缩短1µs。
Note 7. OSCSF.HOCOSF可以确认稳定时间是否已过。
Note 8. 这是在MOCO停止状态下将PLLCR.PLLSTP位设置为0（操作）时的特性。
当在MOCO振荡期间将PLLCR.PLLSTP位设置为0（操作）时，该规范将缩短1µs。
Note 9. 设置主时钟时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于建议的稳定时间的值。更改MOSCCR.MOSTP位的设置以使主时钟振荡器工作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟。

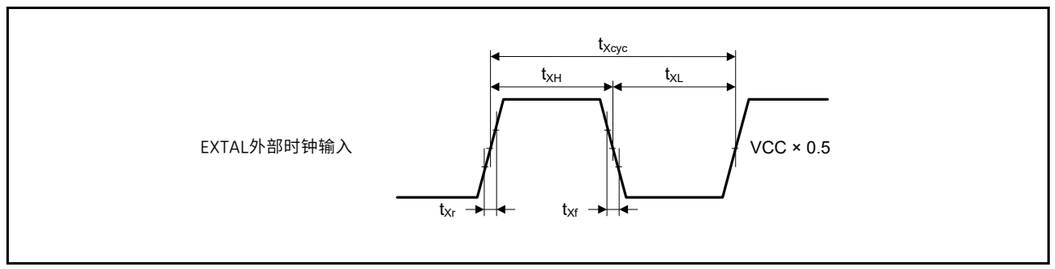


Figure 48.23 EXTAL外部时钟输入时序

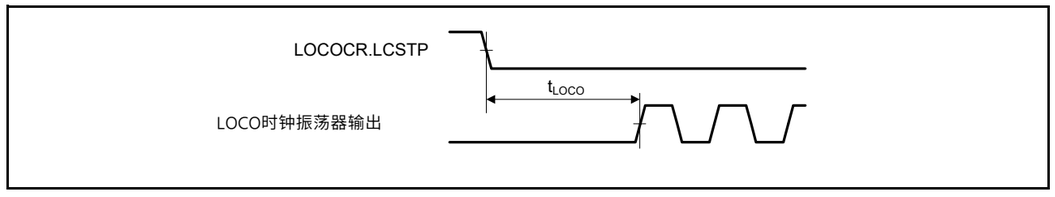


Figure 48.24 LOCO时钟振荡开始时序

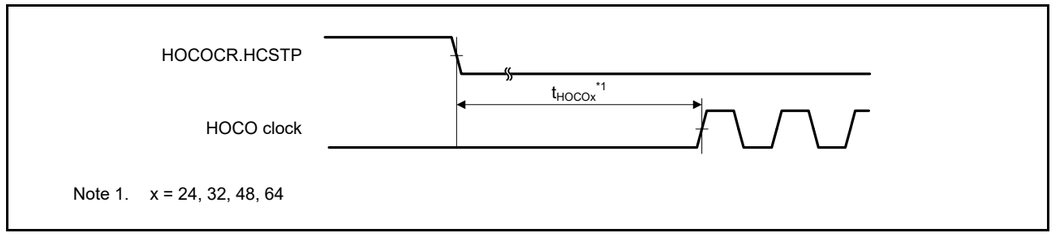


Figure 48.25 HOCO clock oscillation start timing (started by setting HOCOCR.HCSTP bit)

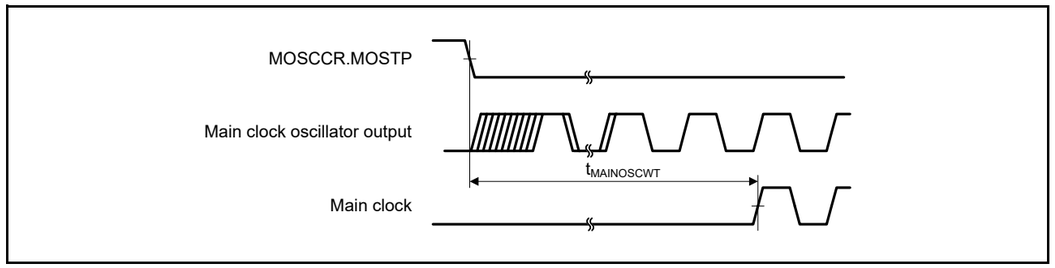


Figure 48.26 Main clock oscillation start timing

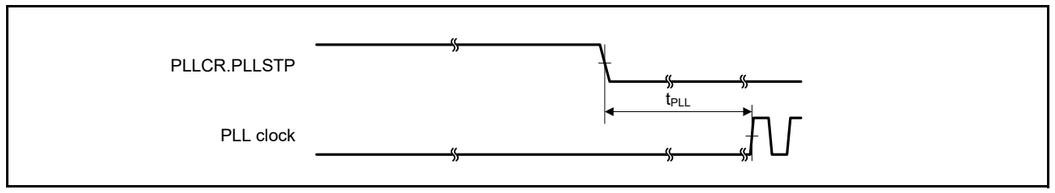


Figure 48.27 PLL clock oscillation start timing (PLL is operated after main clock oscillation has settled)

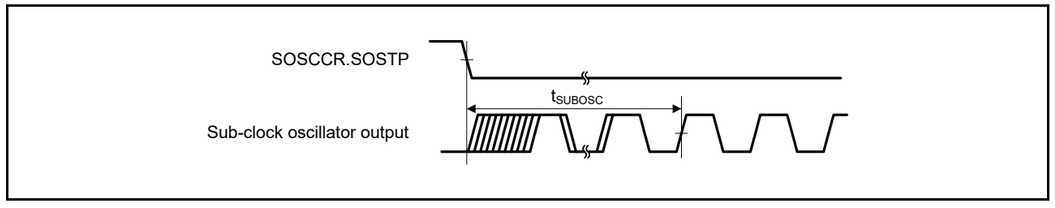


Figure 48.28 Sub-clock oscillation start timing

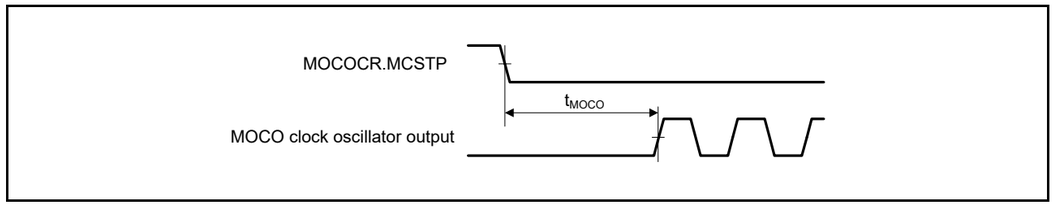


Figure 48.29 MOCO clock oscillation start timing

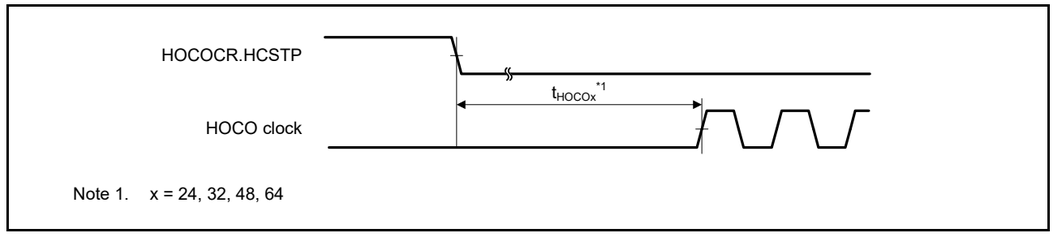


Figure 48.25 HOCO时钟振荡开始时序（通过设置HOCOCR.HCSTP位开始）

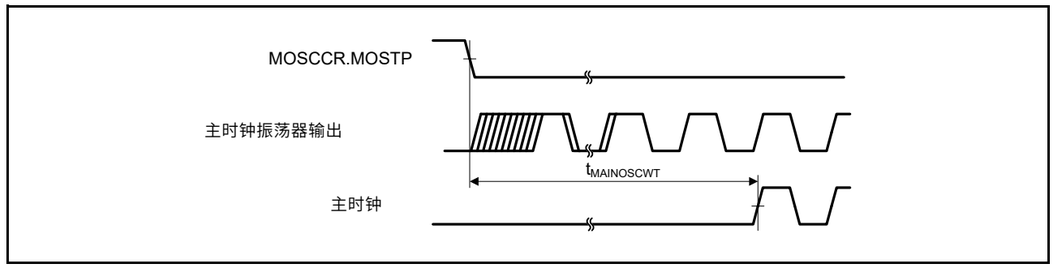


Figure 48.26 主时钟振荡开始时序

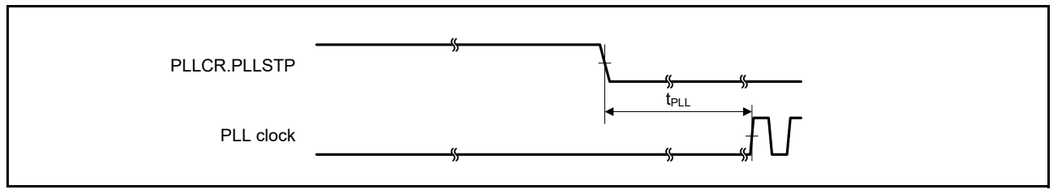


Figure 48.27 PLL时钟振荡开始时序（PLL在主时钟振荡稳定后运行）

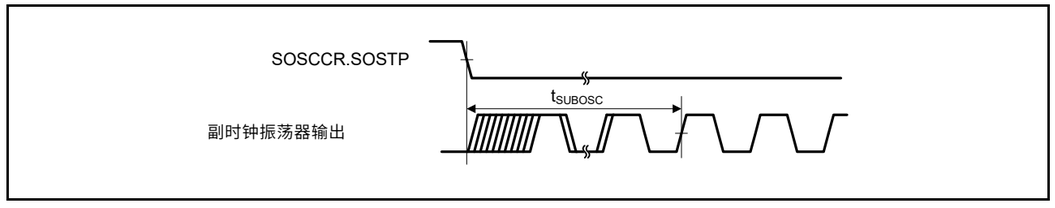


Figure 48.28 副时钟振荡开始时序

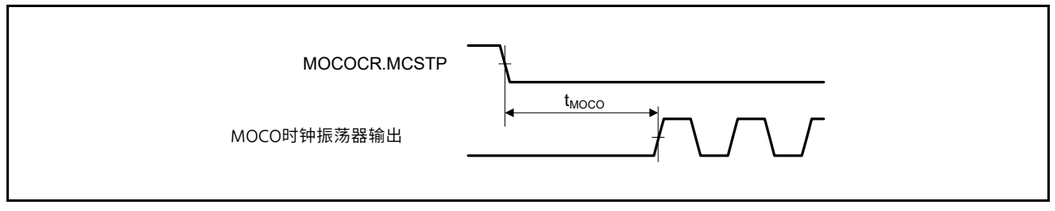


Figure 48.29 MOCO时钟振荡开始时序

48.3.3 Reset Timing

Table 48.24 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 48.30
	Other than above	t_{RESW}	30	-	-	µs	Figure 48.31
Wait time after RES cancellation (at power-on)	LVD0: enable*1	t_{RESWT}	-	0.7	-	ms	Figure 48.30
	LVD0: disable*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0: enable*1	t_{RESWT2}	-	0.5	-	ms	Figure 48.31
	LVD0: disable*2		-	0.05	-		
Internal reset cancellation time (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, Bus master MPU error reset, Bus slave MPU error reset, Stack pointer error reset, Software reset)	LVD0: enable*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0: disable*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

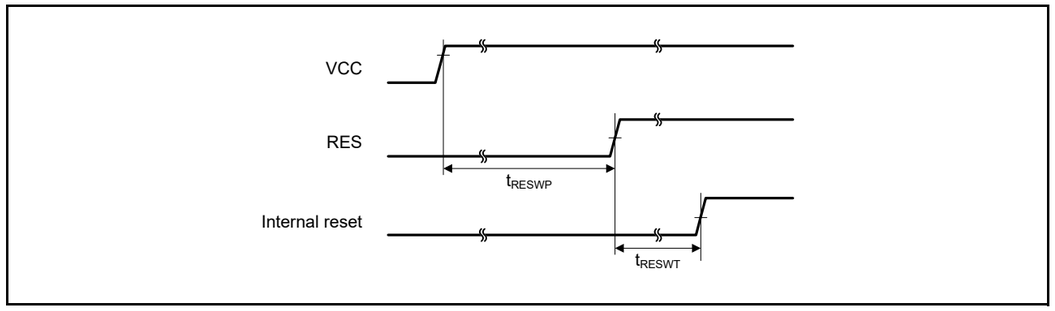


Figure 48.30 Reset input timing at power-on

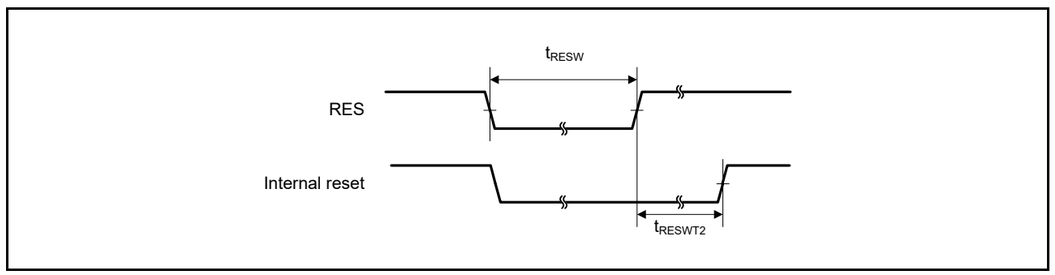


Figure 48.31 Reset input timing (1)

48.3.3 重置时间

Table 48.24 重置时间

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	At power-on	t_{RESWP}	3	-	-	ms	Figure 48.30
	上述以外	t_{RESW}	30	-	-	µs	Figure 48.31
RES取消后的等待时间（上电时）	LVD0: enable*1	t_{RESWT}	-	0.7	-	ms	Figure 48.30
	LVD0: disable*2		-	0.3	-		
RES取消后的等待时间（开机状态下）	LVD0: enable*1	t_{RESWT2}	-	0.5	-	ms	Figure 48.31
	LVD0: disable*2		-	0.05	-		
内部复位取消时间（看门狗定时器复位、SRAM奇偶校验错误复位、SRAMECC错误复位、总线主控MPU错误复位、总线从属MPU错误复位、堆栈指针错误复位、软件复位）	LVD0: enable*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0: disable*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

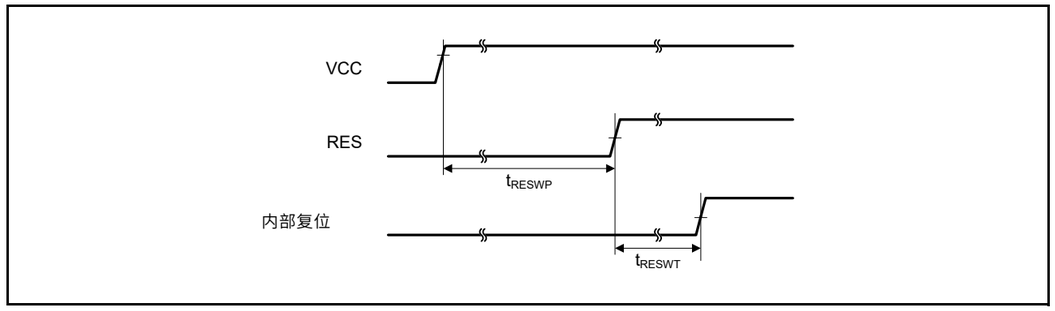


Figure 48.30 上电时复位输入时序

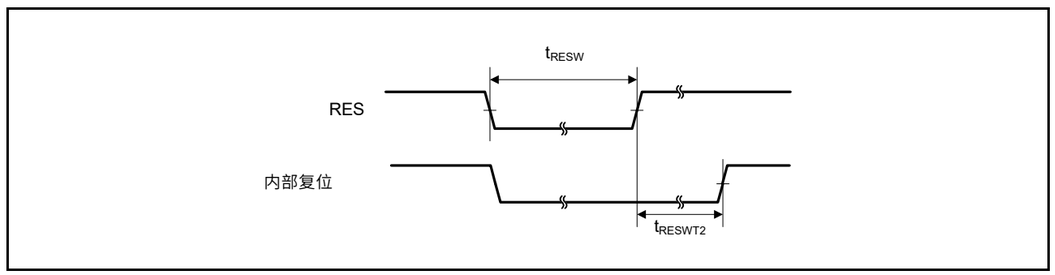


Figure 48.31 复位输入时序(1)

48.3.4 Wakeup Time

Table 48.25 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
			System clock source is PLL (48 MHz) with Main clock oscillator*2	t_{SBYPC}	-	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	-	14	25	µs	
			System clock source is PLL (48 MHz) with Main clock oscillator*3	t_{SBYPE}	-	53	76	µs	
		System clock source is HOCO*4 (HOCO clock is 32 MHz)		t_{SBYHO}	-	43	52	µs	
		System clock source is HOCO*4 (HOCO clock is 48 MHz)		t_{SBYHO}	-	44	52	µs	
		System clock source is HOCO*5 (HOCO clock is 64 MHz)		t_{SBYHO}	-	82	110	µs	
		System clock source is MOCO		t_{SBYMO}	-	16	25	µs	

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.
Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

Table 48.26 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
			System clock source is PLL (24 MHz) with main clock oscillator*2	t_{SBYPC}	-	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t_{SBYEX}	-	2.9	10	µs	
			System clock source is PLL (24 MHz) with main clock oscillator*3	t_{SBYPE}	-	49	76	µs	
		System clock source is HOCO (24 MHz)		t_{SBYHO}	-	38	50	µs	
		System clock source is MOCO		t_{SBYMO}	-	3.5	5.5	µs	

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

48.3.4 唤醒时间

Table 48.25 从低功耗模式恢复的时间(1)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	High-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器（20MHz）*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
			系统时钟源是带有主时钟振荡器的PLL(48MHz)*2	t_{SBYPC}	-	2	3	ms	
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器（20MHz）*3	t_{SBYEX}	-	14	25	µs	
			系统时钟源是带有主时钟振荡器的PLL(48MHz)*3	t_{SBYPE}	-	53	76	µs	
		系统时钟源为HOCO*4（HOCO时钟为32MHz）		t_{SBYHO}	-	43	52	µs	
		系统时钟源为HOCO*4（HOCO时钟为48MHz）		t_{SBYHO}	-	44	52	µs	
		系统时钟源为HOCO*5（HOCO时钟为64MHz）		t_{SBYHO}	-	82	110	µs	
		系统时钟源为MOCO		t_{SBYMO}	-	16	25	µs	

Note 1. ICK、BCK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。
Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。
Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。
Note 4. HOCO时钟等待控制寄存器(HOCOWTCR)设置为05h。
Note 5. HOCO时钟等待控制寄存器(HOCOWTCR)设置为06h。

Table 48.26 从低功耗模式恢复的时间(2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Middle-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器(12MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
			系统时钟源是PLL(24MHz)，带有主时钟振荡器*2	t_{SBYPC}	-	2	3	ms	
		主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器(12MHz)*3	t_{SBYEX}	-	2.9	10	µs	
			系统时钟源是PLL(24MHz)，带有主时钟振荡器*3	t_{SBYPE}	-	49	76	µs	
		系统时钟源是HOCO(24MHz)		t_{SBYHO}	-	38	50	µs	
		系统时钟源为MOCO		t_{SBYMO}	-	3.5	5.5	µs	

Note 1. ICK、BCK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。
Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。
Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。

Table 48.27 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t_{SBYEX}	-	28	50	µs	
		System clock source is MOCO		t_{SBYMO}	-	25	35	µs	

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 48.28 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t_{SBYEX}	-	108	130	µs	
		System clock source is HOCO		t_{SBYHO}	-	108	130	µs	

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined by the following expression.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 48.29 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	-	0.85	1	ms	Figure 48.32
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues to oscillate in Software Standby mode during Subosc-speed mode.

Table 48.27 从低功耗模式恢复的时间(3)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Low-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器(1MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
		主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器(1MHz)*3	t_{SBYEX}	-	28	50	µs	
		系统时钟源为MOCO		t_{SBYMO}	-	25	35	µs	

Note 1. ICK、BCK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。
Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。

Table 48.28 从低功耗模式恢复的时间(4)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Low-voltage mode	连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器（4MHz）*2	t_{SBYMC}	-	2	3	ms	Figure 48.32
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器（4MHz）*3	t_{SBYEX}	-	108	130	µs	
		系统时钟源为HOCO		t_{SBYHO}	-	108	130	µs	

Note 1. ICK、BCK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下表达式确定。

Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。
Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。

Table 48.29 从低功耗模式恢复的时间(5)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Subosc-speed mode	系统时钟源为副时钟振荡器（32.768kHz）	t_{SBYSC}	-	0.85	1	ms	Figure 48.32
		系统时钟源为LOCO(32.768kHz)	t_{SBYLO}	-	0.85	1.2	ms	

Note 1. 在Subosc速度模式期间，副时钟振荡器或LOCO本身在软件待机模式下继续振荡。

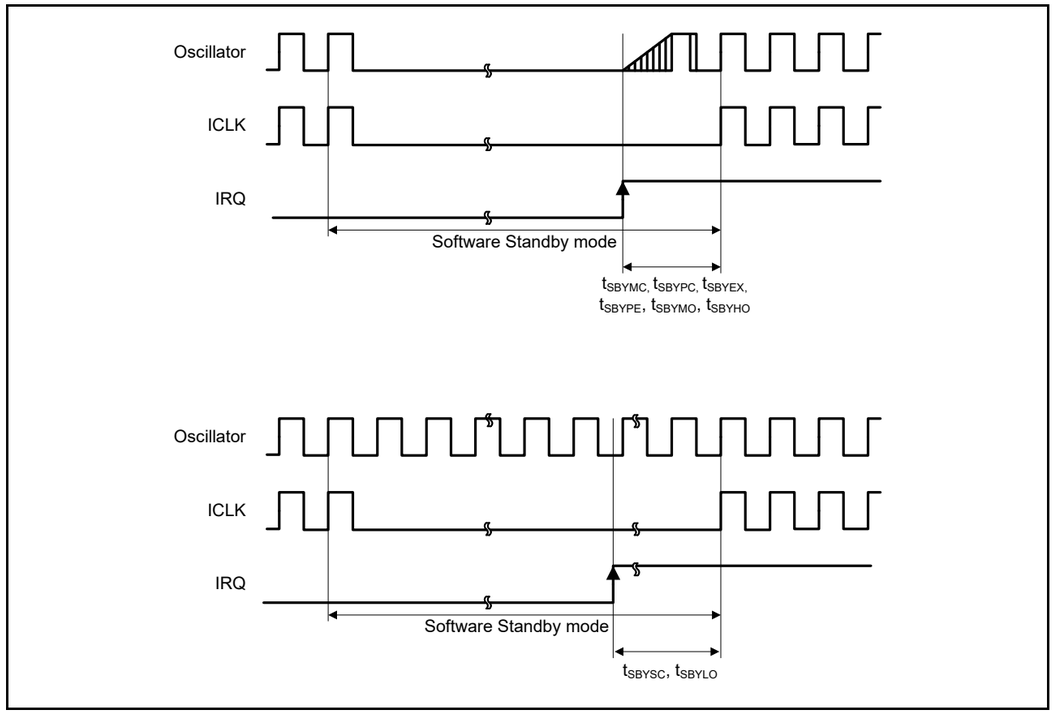


Figure 48.32 Software Standby mode cancellation timing

Table 48.30 Timing of recovery from low power modes (6)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	µs	Figure 48.33
	Middle-speed mode System clock source is MOCO	t_{SNZ}	-	1.3	3.6	µs	
	Low-speed mode System clock source is MOCO	t_{SNZ}	-	10	13	µs	
	Low-voltage mode System clock source is HOCO	t_{SNZ}	-	87	110	µs	

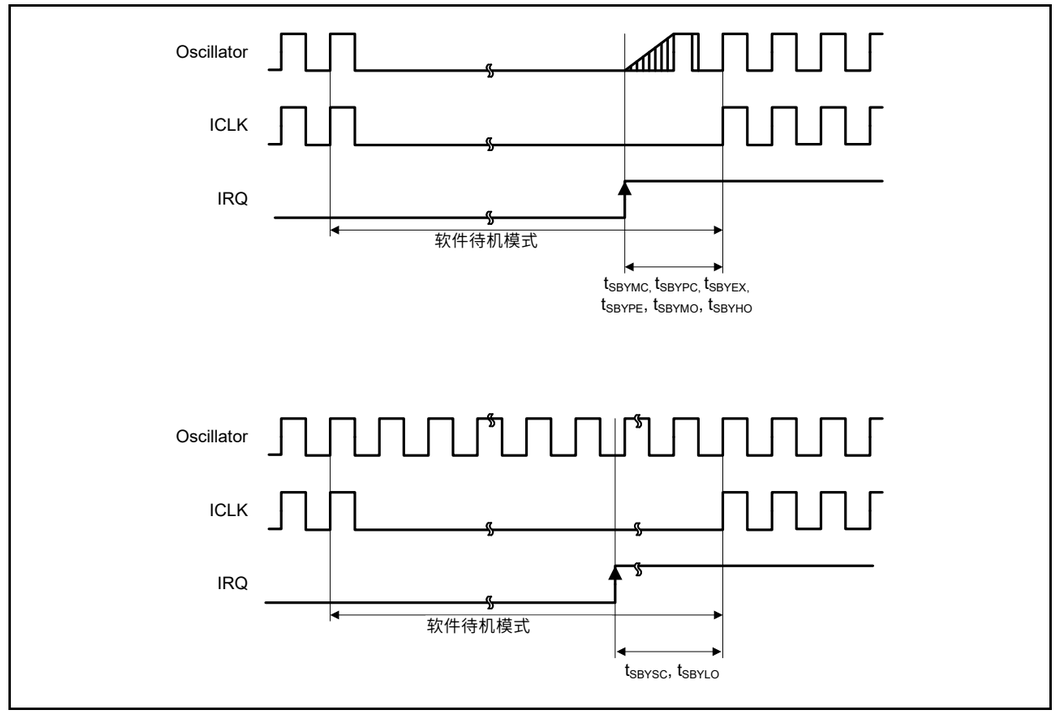
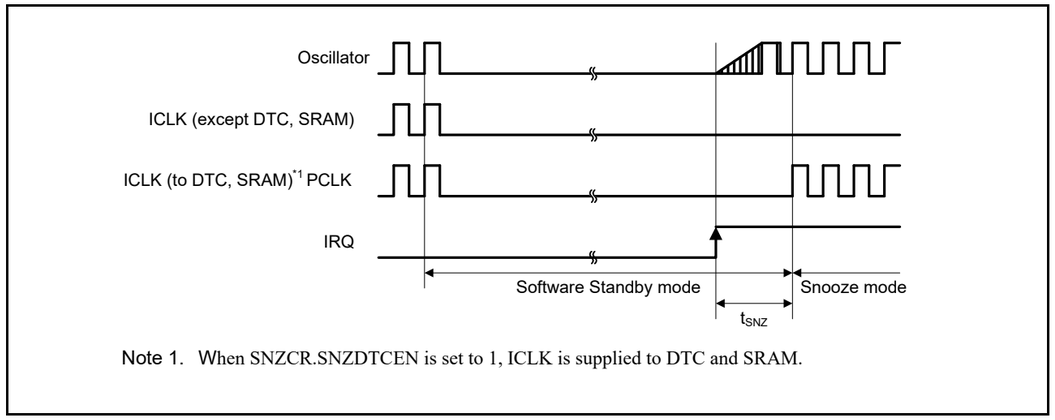


Figure 48.32 软件待机模式取消时序

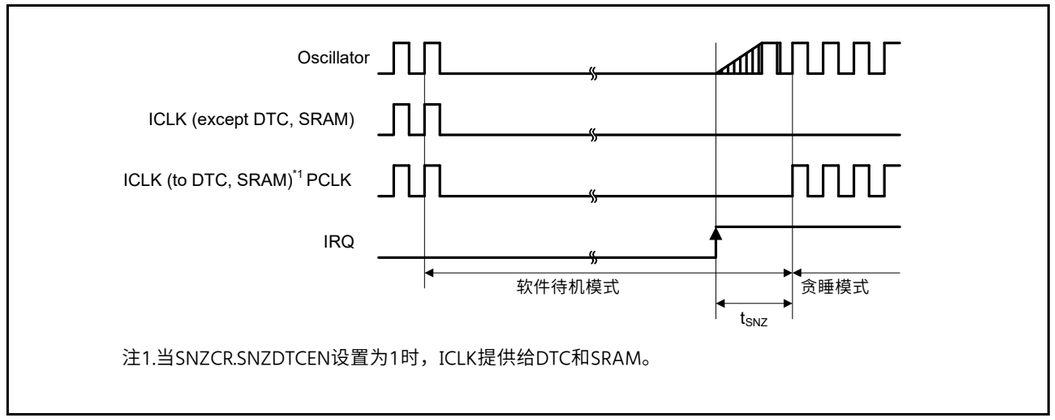
Table 48.30 从低功耗模式恢复的时间(6)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
恢复时间从软件待机模式到贪睡模式	High-speed mode 系统时钟源为HOCO	t_{SNZ}	-	36	45	µs	Figure 48.33
	Middle-speed mode 系统时钟源为MOCO	t_{SNZ}	-	1.3	3.6	µs	
	Low-speed mode 系统时钟源为MOCO	t_{SNZ}	-	10	13	µs	
	Low-voltage mode 系统时钟源为HOCO	t_{SNZ}	-	87	110	µs	



Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

Figure 48.33 Recovery timing from Software Standby mode to Snooze mode



注1.当SNZCR.SNZDTCEN设置为1时，ICLK提供给DTC和SRAM。

Figure 48.33 从软件待机模式到贪睡模式的恢复时间

48.3.5 NMI and IRQ Noise Filter

Table 48.31 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 15).

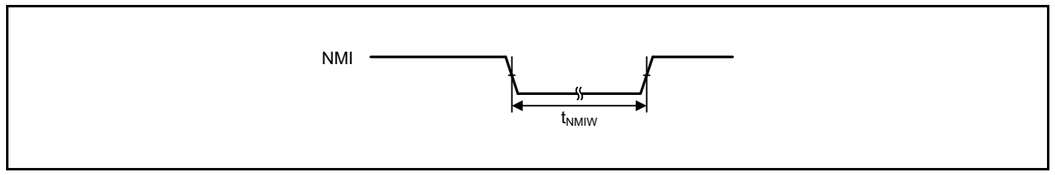


Figure 48.34 NMI interrupt input timing

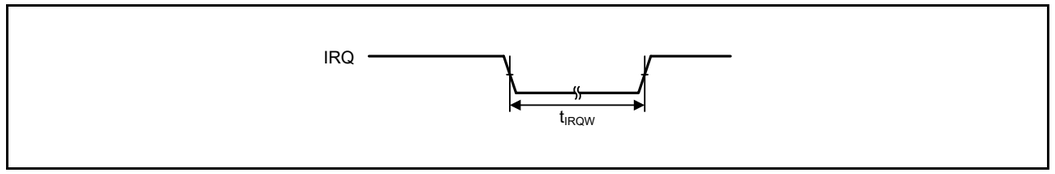


Figure 48.35 IRQ interrupt input timing

48.3.5 NMI和IRQ噪声滤波器

Table 48.31 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	-	-	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	-	-	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。
Note: 如果时钟源切换，则增加切换源的4个时钟周期。
Note 1. tPcyc表示PCLKB的周期。
Note 2. tNMICK表示NMI数字滤波器采样时钟的周期。
Note 3. tIRQCK表示IRQi数字滤波器采样时钟的周期（i=0到15）。

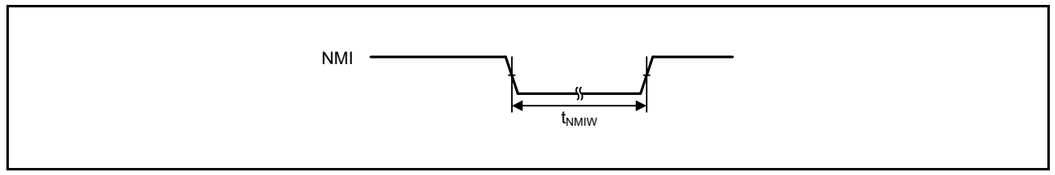


Figure 48.34 NMI中断输入时序

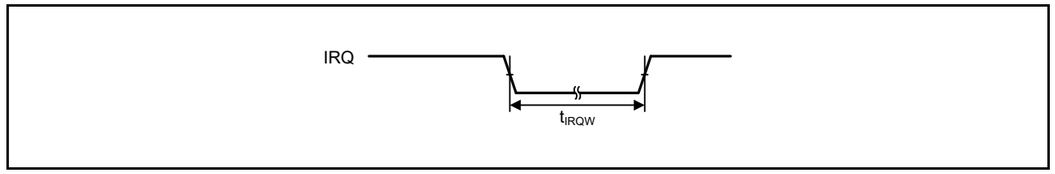


Figure 48.35 IRQ中断输入时序

48.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 48.32 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 48.36
	Input/output data cycle (P004)		t_{POcyc}	10	-	us	
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 48.37
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 48.38
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	2.7 V ≤ VCC ≤ 3.6 V	t_{ACYC}*1	250	-	ns	Figure 48.39
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
	AGTIO, AGTEE input high level width, low-level width	2.7 V ≤ VCC ≤ 3.6 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
	AGTIO, AGTO, AGTOB output cycle	2.7 V ≤ VCC ≤ 3.6 V	t_{ACYC2}	62.5	-	ns	Figure 48.39
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
ADC14	14-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 48.40
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 48.41

Note 1. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.
Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle

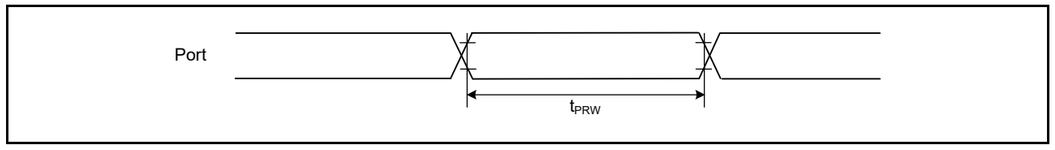


Figure 48.36 I/O ports input timing

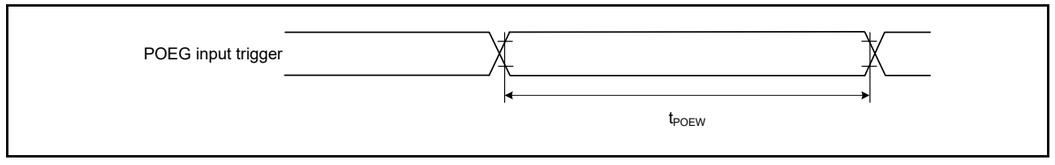


Figure 48.37 POEG input trigger timing

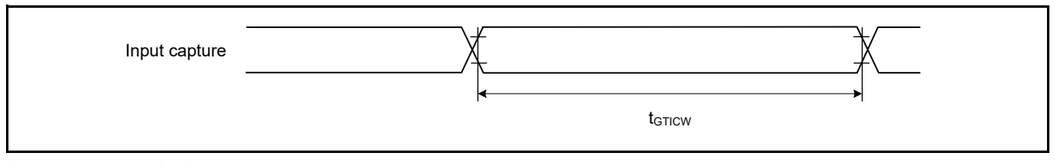


Figure 48.38 GPT input capture timing

48.3.6 IO端口、POEG、GPT、AGT、KINT和ADC14触发时序

Table 48.32 IO端口、POEG、GPT、AGT、KINT和ADC14触发时序

Parameter			Symbol	Min	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度		t_{PRW}	1.5	-	t_{Pcyc}	Figure 48.36
	输入输出数据周期(P004)		t_{POcyc}	10	-	us	
POEG	POEG输入触发脉冲宽度		t_{POEW}	3	-	t_{Pcyc}	Figure 48.37
GPT	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 48.38
		双刃		2.5	-		
AGT	AGTIO、AGTEE输入周期	2.7 V ≤ VCC ≤ 3.6 V	t_{ACYC}*1	250	-	ns	Figure 48.39
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
	AGTIO、AGTEE输入高电平宽度、低电平宽度	2.7 V ≤ VCC ≤ 3.6 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
	AGTIO、AGTO、AGTOB输出周期	2.7 V ≤ VCC ≤ 3.6 V	t_{ACYC2}	62.5	-	ns	Figure 48.39
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
ADC14	14位模数转换器触发输入脉冲宽度		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 48.40
KINT	KRn(n=00to07)脉冲宽度		t_{KR}	250	-	ns	Figure 48.41

Note 1. 输入周期的约束：
不切换源时钟时：tPcyc×2<tACYC应满足。
切换源时钟时：tPcyc×6<tACYC应满足。
Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle

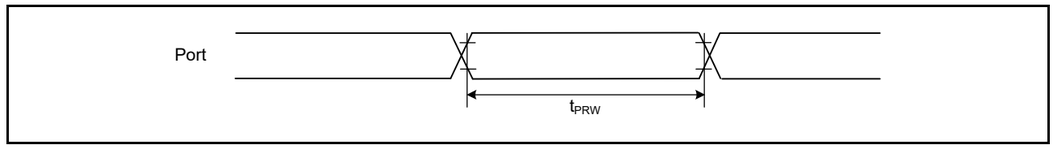


Figure 48.36 IO端口输入时序

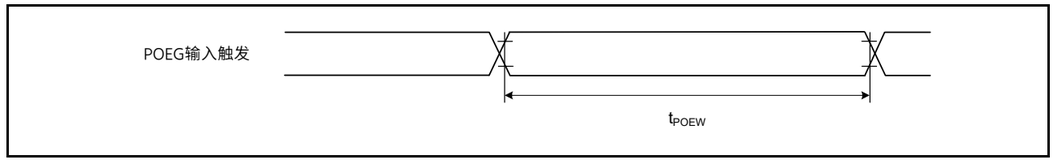


Figure 48.37 POEG输入触发时序

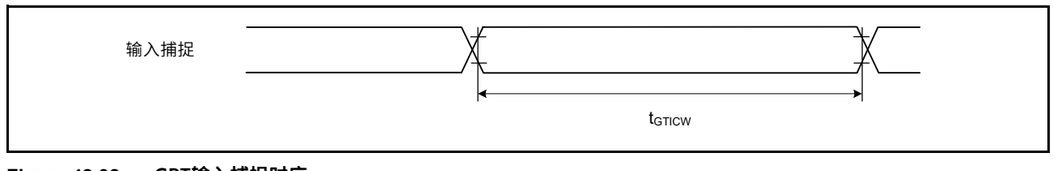


Figure 48.38 GPT输入捕捉时序

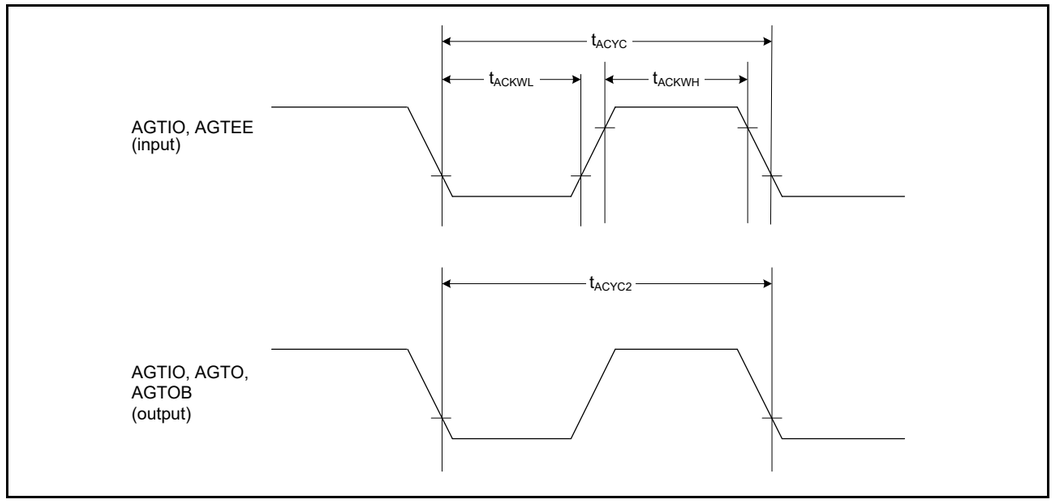


Figure 48.39 AGT I/O timing

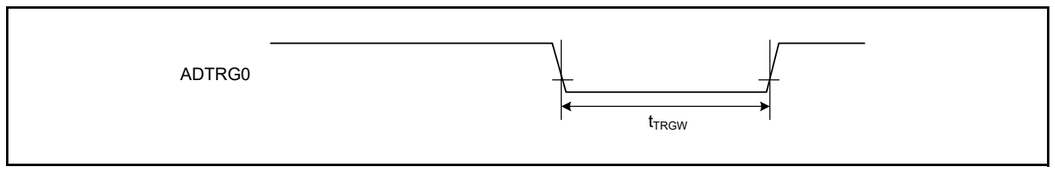


Figure 48.40 ADC14 trigger input timing

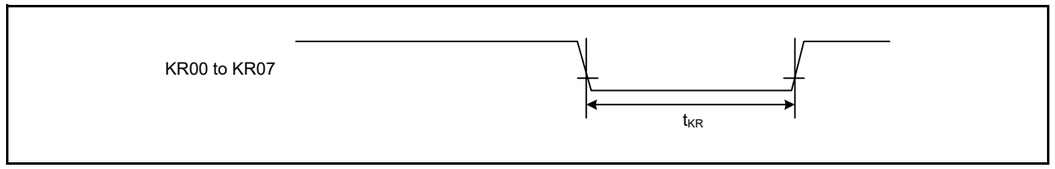


Figure 48.41 Key interrupt input timing

48.3.7 CAC Timing

Table 48.33 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{PBcyc}*1 ≤ t_{cac}*2	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}*1	-	-	ns	-
		t_{PBcyc}*1 > t_{cac}*2		5 × t_{cac} + 6.5 × t_{PBcyc}*1	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

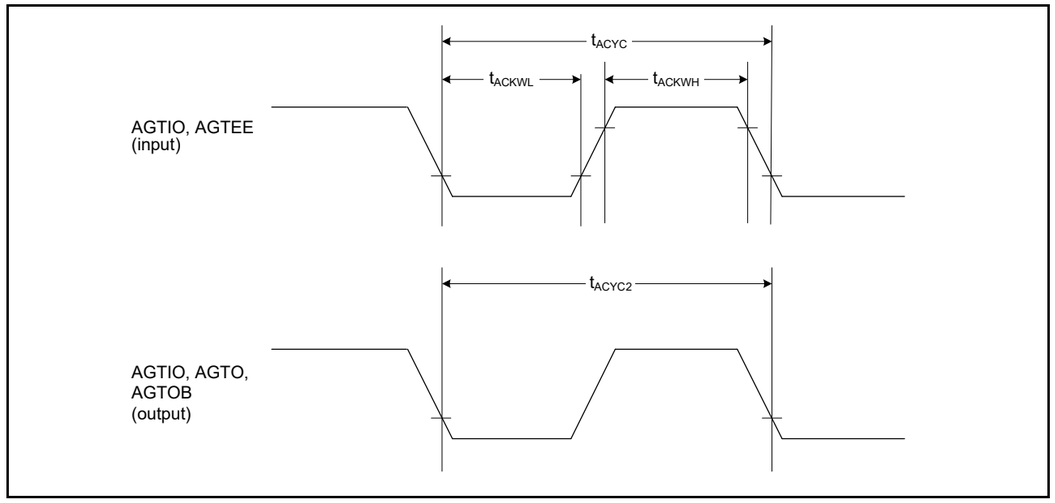


Figure 48.39 AGT I/O timing

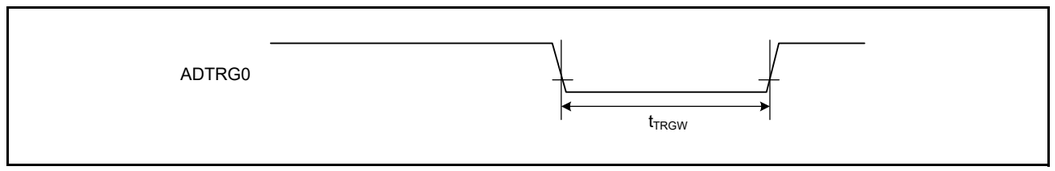


Figure 48.40 ADC14触发输入时序

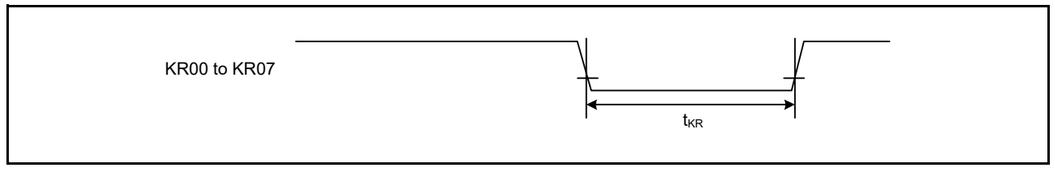


Figure 48.41 按键中断输入时序

48.3.7 CAC时序

Table 48.33 CAC计时

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	t_{PBcyc}*1 ≤ t_{cac}*2	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}*1	-	-	ns	-
		t_{PBcyc}*1 > t_{cac}*2		5 × t_{cac} + 6.5 × t_{PBcyc}*1	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. tcac:CAC计数时钟源周期。

48.3.8 SCI Timing

Table 48.34 SCI timing (1)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous		t_{Scyc}	4	-	t_{Pcyc}	Figure 48.42
		Clock synchronous			6	-		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	-	20	ns	
	Input clock fall time			t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous		t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous			4	-		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V or above	t_{SCKr}	-	20	ns	
	Output clock fall time		1.8 V or above	t_{SCKf}	-	20	ns	
	Transmit data delay (master)	Clock synchronous	1.8 V or above	t_{TXD}	-	40	ns	Figure 48.43
	Transmit data delay (slave)	Clock synchronous	2.7 V or above		-	55	ns	
			2.4 V or above		-	60		
			1.8 V or above		-	100		
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t_{RXS}	45	-	ns	
			2.4 V or above		55	-		
			1.8 V or above		90	-		
	Receive data setup time (slave)	Clock synchronous	2.7 V or above		40	-	ns	
			1.8 V or above		45	-		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	-	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

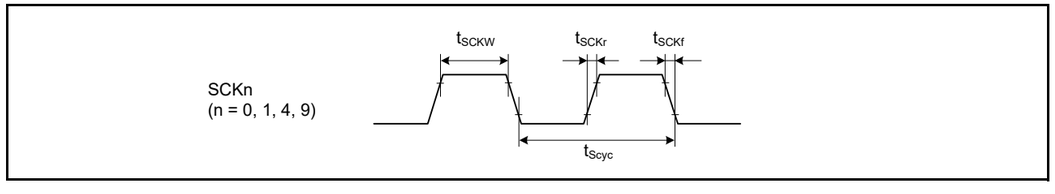


Figure 48.42 SCK clock input timing

48.3.8 SCI时序

Table 48.34 SCI时序（1）

Parameter				Symbol	Min	Max	Unit*1	测试条件
SCI	输入时钟周期	Asynchronous		t_{Scyc}	4	-	t_{Pcyc}	Figure 48.42
		时钟同步			6	-		
	输入时钟脉冲宽度			t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间			t_{SCKr}	-	20	ns	
	输入时钟下降时间			t_{SCKf}	-	20	ns	
	输出时钟周期	Asynchronous		t_{Scyc}	6	-	t_{Pcyc}	
		时钟同步			4	-		
	输出时钟脉冲宽度			t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		1.8V或以上	t_{SCKr}	-	20	ns	
	输出时钟下降时间		1.8V或以上	t_{SCKf}	-	20	ns	
	传输数据延迟（主）	时钟同步	1.8V或以上	t_{TXD}	-	40	ns	Figure 48.43
	传输数据延迟（从）	时钟同步	2.7V或以上		-	55	ns	
			2.4V或以上		-	60		
			1.8V或以上		-	100		
	接收数据建立时间（主）	时钟同步	2.7V或以上	t_{RXS}	45	-	ns	
			2.4V或以上		55	-		
			1.8V或以上		90	-		
	接收数据建立时间（从机）	时钟同步	2.7V或以上		40	-	ns	
			1.8V或以上		45	-		
	接收数据保持时间（主机）	时钟同步		t_{RXH}	5	-	ns	
	接收数据保持时间（从机）	时钟同步		t_{RXH}	40	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

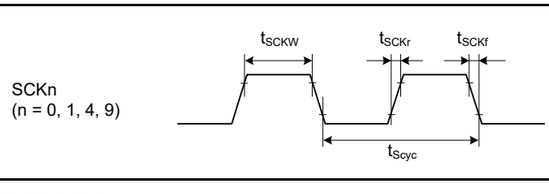


Figure 48.42 SCK时钟输入时序

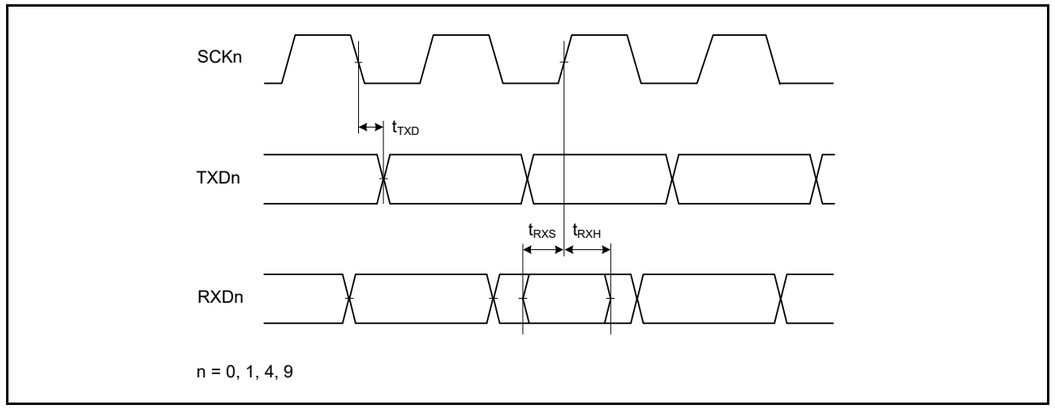


Figure 48.43 SCI input/output timing in clock synchronous mode

Table 48.35 SCI timing (2)

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 48.44
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	1.8 V or above	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	Data input setup time	Master 2.7 V or above	t_{SU}	45	-	ns	Figure 48.45 to Figure 48.48
		Master 2.4 V or above		55	-		
		Master 1.8 V or above		80	-		
		Slave 2.7 V or above		40	-		
		Slave 1.8 V or above		45	-		
	Data input hold time	Master	t_H	33.3	-	ns	
		Slave		40	-		
	SS input setup time		t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	Master 1.8 V or above	t_{OD}	-	40	ns	
		Slave 2.4 V or above		-	65		
		Slave 1.8 V or above		-	100		
	Data output hold time	Master 2.7 V or above	t_{OH}	–10	-	ns	
		Master 2.4 V or above		–20	-		
		Master 1.8 V or above		–30	-		
		Slave		–10	-		
	Data rise and fall time	Master 1.8 V or above	t_{Dr}, t_{Df}	-	20	ns	
		Slave 1.8 V or above		-	20		
	Slave access time		t_{SA}	-	10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz)	t_{Pcyc}	Figure 48.47 and Figure 48.48
	Slave output release time		t_{REL}	-	10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz)	t_{Pcyc}	

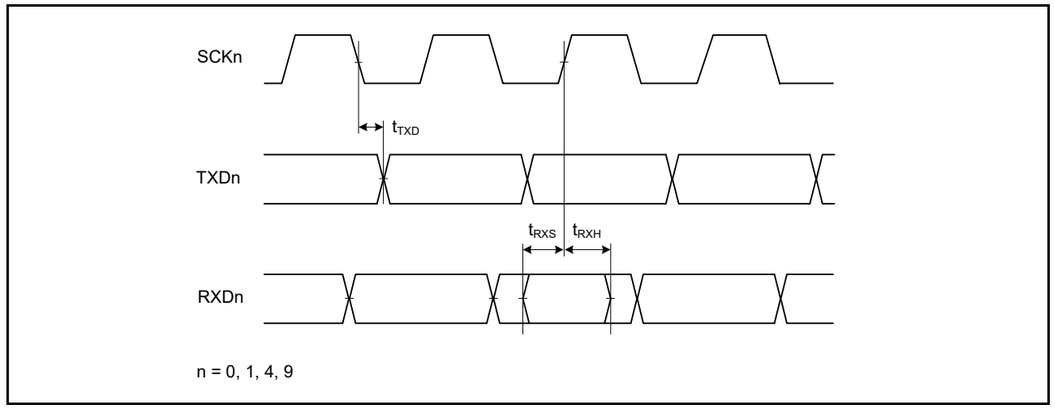


Figure 48.43 时钟同步模式下的SCI输入输出时序

Table 48.35 SCI时序（2）

Parameter			Symbol	Min	Max	Unit	测试条件
Simple SPI	SCK时钟周期输出（主机）		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 48.44
	SCK时钟周期输入（从机）			6	65536		
	SCK时钟高脉冲宽度		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间	1.8V或以上	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	数据输入建立时间	Master 2.7V或以上	t_{SU}	45	-	ns	图48.45至 Figure 48.48
		Master 2.4V或以上		55	-		
		Master 1.8V或以上		80	-		
		Slave 2.7V或以上		40	-		
		Slave 1.8V或以上		45	-		
	数据输入保持时间	Master	t_H	33.3	-	ns	
		Slave		40	-		
	SS输入建立时间		t_{LEAD}	1	-	t_{SPcyc}	
	SS输入保持时间		t_{LAG}	1	-	t_{SPcyc}	
	数据输出延迟	Master 1.8V或以上	t_{OD}	-	40	ns	
		Slave 2.4V或以上		-	65		
		Slave 1.8V或以上		-	100		
	数据输出保持时间	Master 2.7V或以上	t_{OH}	–10	-	ns	
		Master 2.4V或以上		–20	-		
		Master 1.8V或以上		–30	-		
		Slave		–10	-		
	数据上升和下降时间	Master 1.8V或以上	t_{Dr}, t_{Df}	-	20	ns	
		Slave 1.8V或以上		-	20		
	从站访问时间		t_{SA}	-	10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz)	t_{Pcyc}	图48.47和 Figure 48.48
	从机输出释放时间		t_{REL}	-	10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz)	t_{Pcyc}	

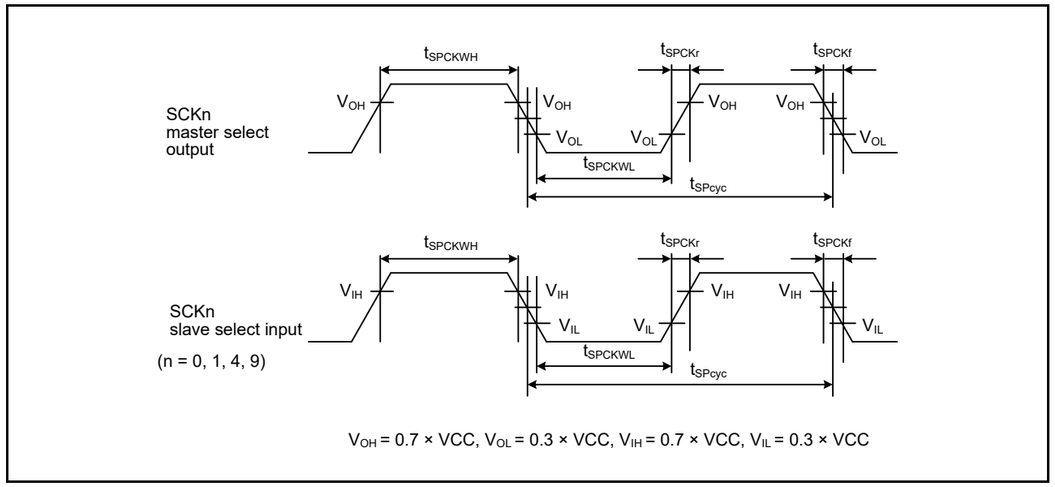


Figure 48.44 SCI simple SPI mode clock timing

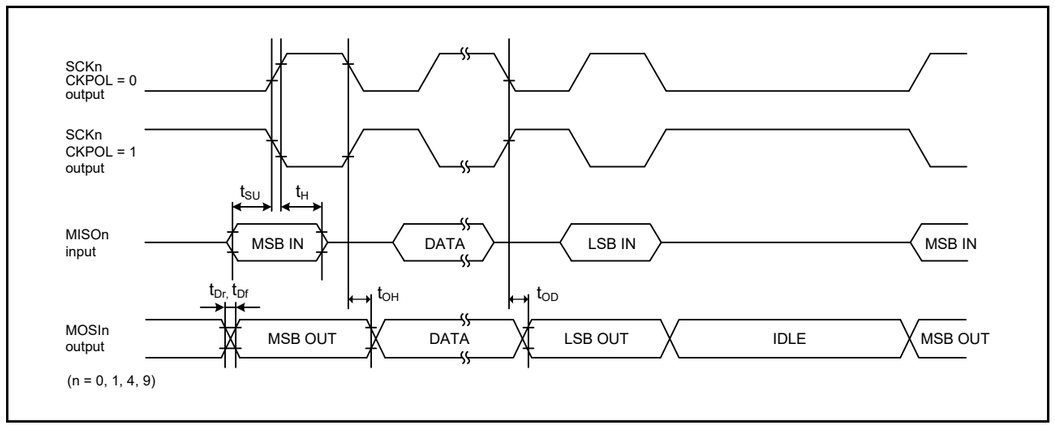


Figure 48.45 SCI simple SPI mode timing (master, CKPH = 1)

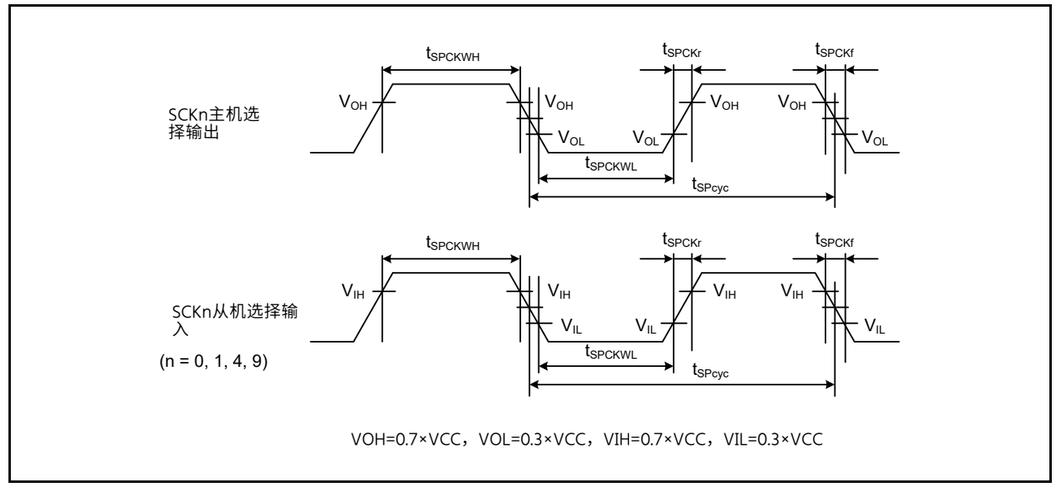


Figure 48.44 SCI简单SPI模式时钟时序

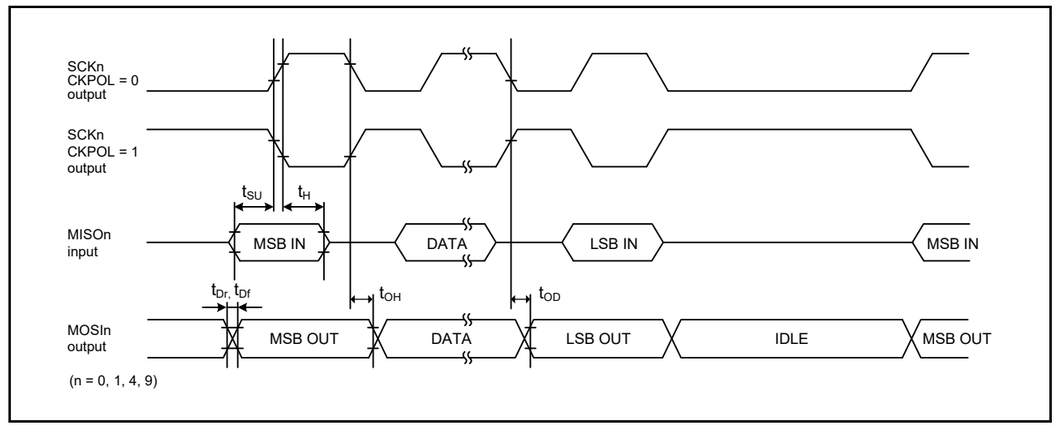


Figure 48.45 SCI简单SPI模式时序（主机，CKPH=1）

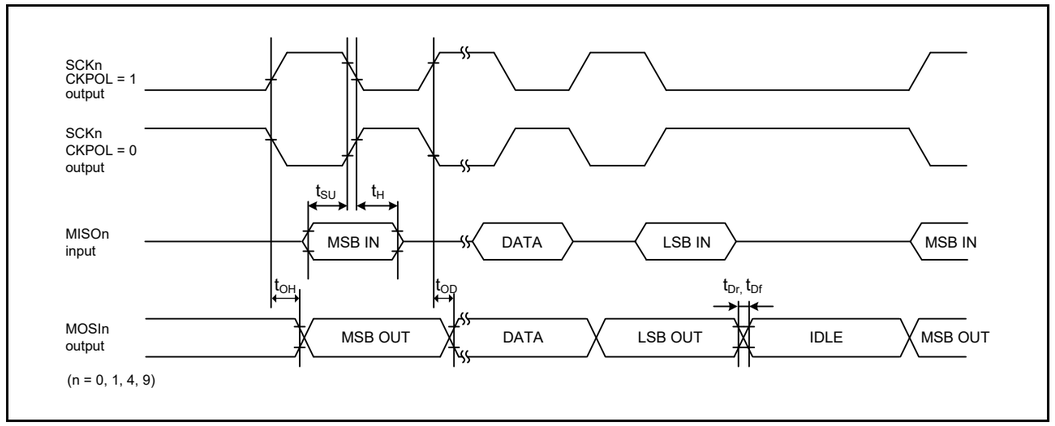


Figure 48.46 SCI simple SPI mode timing (master, CKPH = 0)

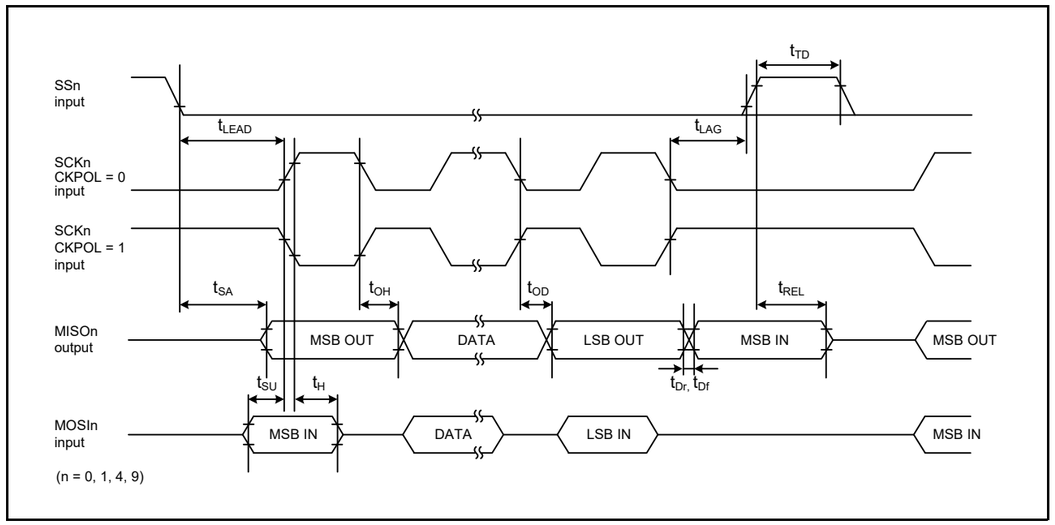


Figure 48.47 SCI simple SPI mode timing (slave, CKPH = 1)

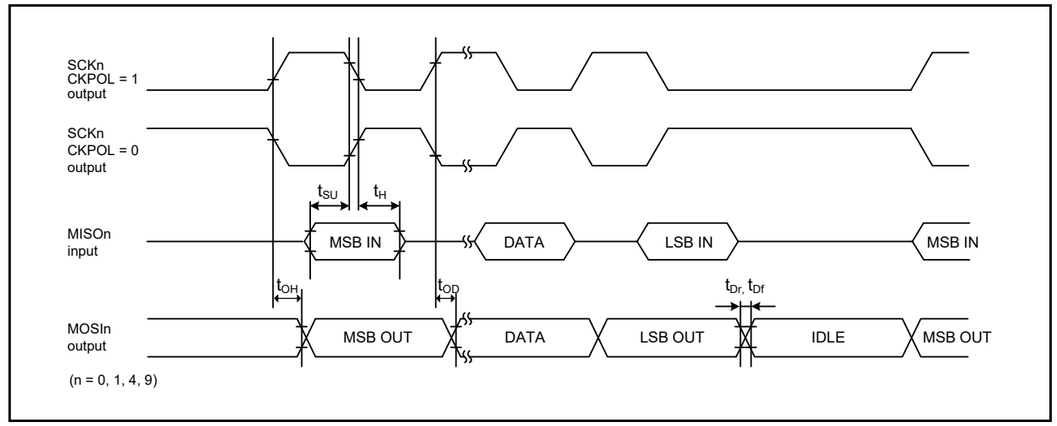


Figure 48.46 SCI简单SPI模式时序（主机，CKPH=0）

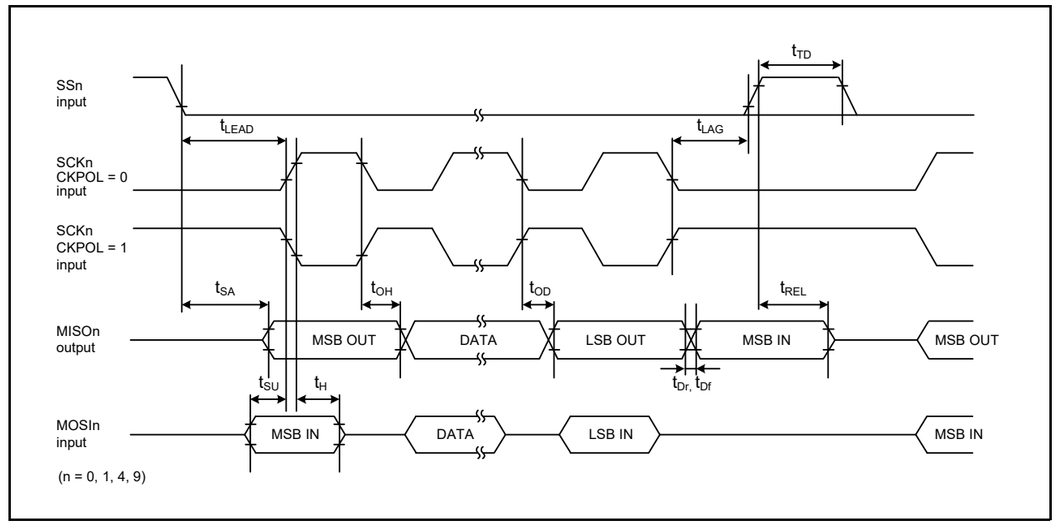


Figure 48.47 SCI简单SPI模式时序（从机，CKPH=1）

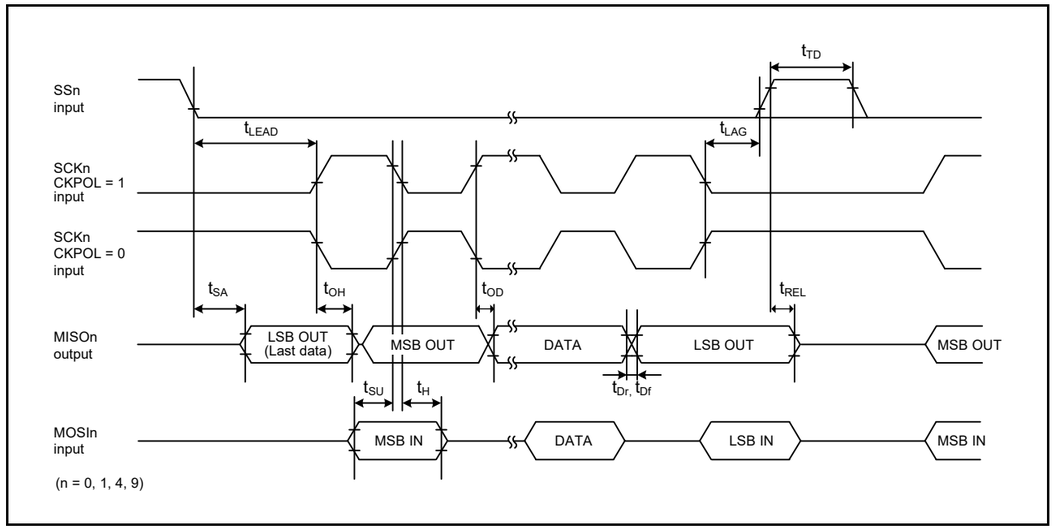


Figure 48.48 SCI simple SPI mode timing (slave, CKPH = 0)

Table 48.36 SCI timing (3)
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 48.49
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}*1	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 48.49 For all ports use PmnPFS.DSCR of middle drive.
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}*1	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. Cb indicates the total capacity of the bus line.

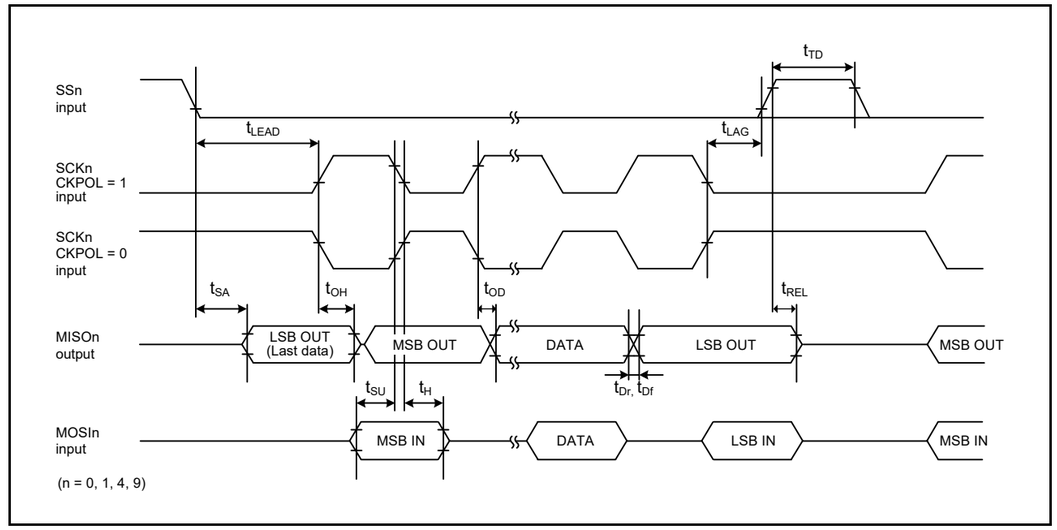
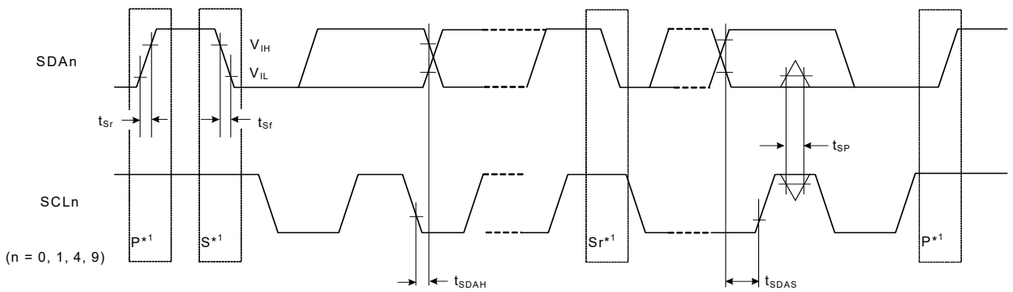


Figure 48.48 SCI简单SPI模式时序（从机，CKPH=0）

Table 48.36 SCI时序（3）
Conditions: VCC = 2.7 to 3.6 V

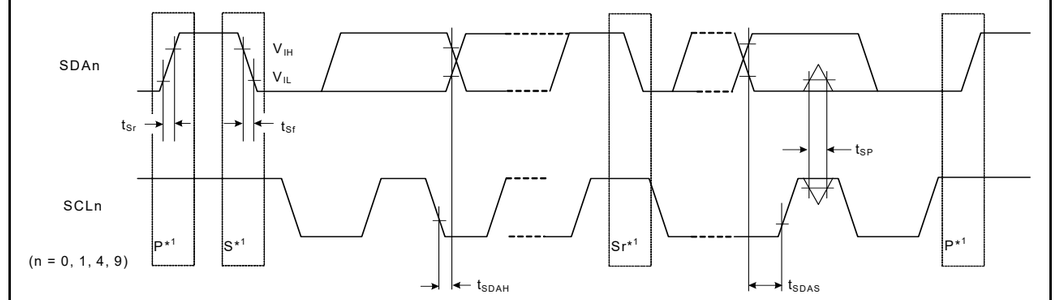
Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	-	1000	ns	Figure 48.49
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}*1	ns	
	数据输入建立时间	t_{SDAS}	250	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	-	300	ns	Figure 48.49 对于所有端口，使用中间驱动器的PmnPFS.DSCR。
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}*1	ns	
	数据输入建立时间	t_{SDAS}	100	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	

Note 1. tIICcyc：由SMR.CKS[1:0]位选择的时钟周期。
Note 2. Cb表示公交线路的总容量。



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition.

Figure 48.49 SCI simple IIC mode timing



Note 1. S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件。

Figure 48.49 SCI简单IIC模式时序

48.3.9 SPI Timing

Table 48.37 SPI timing (1 of 2)
Conditions: Middle drive output is selected in the Port Drive Capability in PmnPFS register

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master		t_{SPcyc}	2*4	4096	t_{Pcyc}	Figure 48.50
		Slave			6	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	-	10	ns	
			2.4 V or above		-	15		
			1.8 V or above		-	20		
		Input			-	1	µs	
	Data input setup time	Master		t_{SU}	10	-	ns	Figure 48.51 to Figure 48.56
		Slave	2.4 V or above		10	-		
			1.8 V or above		15	-		
	Data input hold time	Master (RSPCK is PCLKA/2)		t_{HF}	0	-	ns	
		Master (RSPCK is other than above.)		t_H	t_{Pcyc}	-		
		Slave		t_H	20	-		
	SSL setup time	Master	1.8 V or above	t_{LEAD}	$-30 + N \times t_{Spcyc}$*2	-	ns	
		Slave			$6 \times t_{Pcyc}$	-		
	SSL hold time	Master		t_{LAG}	$-30 + N \times t_{Spcyc}$*3	-		
		Slave			$6 \times t_{Pcyc}$	-		
	Data output delay	Master	2.7 V or above	t_{OD}	-	14	ns	Figure 48.51 to Figure 48.56
			2.4 V or above		-	20		
			1.8 V or above		-	25		
		Slave	2.7 V or above		-	50		
			2.4 V or above		-	60		
			1.8 V or above		-	85		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	-		
	MOSI and MISO rise and fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	-	10	ns	
			2.4 V or above		-	15		
			1.8 V or above		-	20		
		Input			-	1	µs	

48.3.9 SPI时序

Table 48.37 SPI时序（1of2）
条件：在PmnPFS寄存器的PortDriveCapability中选择中间驱动输出

Parameter				Symbol	Min	Max	Unit*1	测试条件
SPI	RSPCK时钟周期	Master		t_{SPcyc}	2*4	4096	t_{Pcyc}	Figure 48.50
		Slave			6	4096		
	RSPCK时钟高脉冲宽度	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK时钟低脉冲宽度	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK时钟上升和下降时间	Output	2.7V或以上	t_{SPCKr}, t_{SPCKf}	-	10	ns	
			2.4V或以上		-	15		
			1.8V或以上		-	20		
		Input			-	1	µs	
	数据输入建立时间	Master		t_{SU}	10	-	ns	图48.51至 Figure 48.56
		Slave	2.4V或以上		10	-		
			1.8V或以上		15	-		
	数据输入保持时间	主机（RSPCK为PCLKA2）		t_{HF}	0	-	ns	
		主控（RSPCK不在上述范围内。）		t_H	t_{Pcyc}	-		
		Slave		t_H	20	-		
	SSL设置时间	Master	1.8V或以上	t_{LEAD}	$-30 + N \times t_{Spcyc}$*2	-	ns	
		Slave			$6 \times t_{Pcyc}$	-		
	SSL保持时间	Master		t_{LAG}	$-30 + N \times t_{Spcyc}$*3	-		
		Slave			$6 \times t_{Pcyc}$	-		
	数据输出延迟	Master	2.7V或以上	t_{OD}	-	14	ns	图48.51至 Figure 48.56
			2.4V或以上		-	20		
			1.8V或以上		-	25		
		Slave	2.7V或以上		-	50		
			2.4V或以上		-	60		
			1.8V或以上		-	85		
	数据输出保持时间	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	连续传输延迟	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	-		
	MOSI和MISO上升和下降时间	Output	2.7V或以上	t_{Dr}, t_{Df}	-	10	ns	
			2.4V或以上		-	15		
			1.8V或以上		-	20		
		Input			-	1	µs	

Table 48.37 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability in PmnPFS register

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	SSL rise and fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	-	10	ns	Figure 48.51 to Figure 48.56
			2.4 V or above		-	15		
			1.8 V or above		-	20		
		Input			-	1	µs	
	Slave access time		2.4 V or above	t_{SA}	-	2 × t_{Pcyc} + 100	ns	Figure 48.55 and Figure 48.56
			1.8 V or above		-	2 × t_{Pcyc} + 140		
	Slave output release time		2.4 V or above	t_{REL}	-	2 × t_{Pcyc} + 100	ns	
			1.8 V or above		-	2 × t_{Pcyc} + 140		

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.
Note 4. The upper limit of RSPCK is 16 MHz.

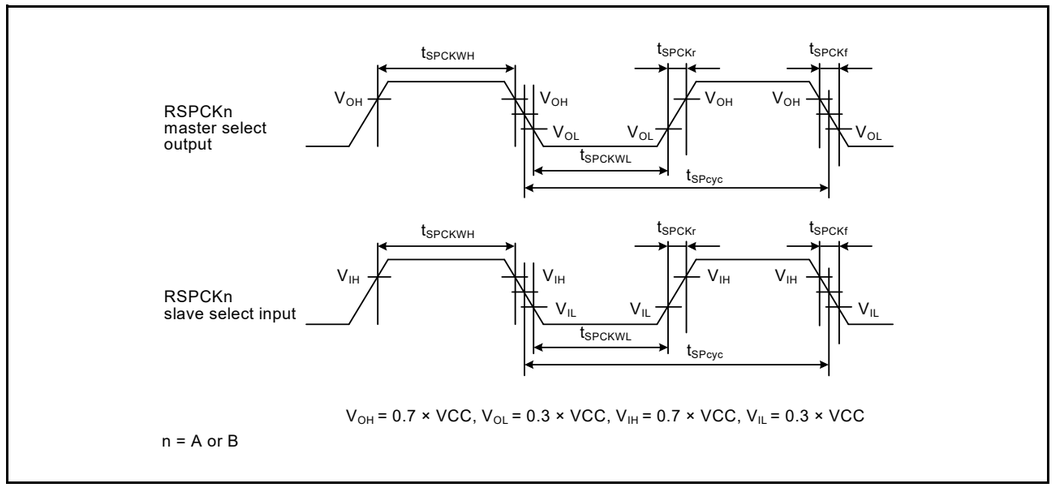


Figure 48.50 SPI clock timing

Table 48.37 SPI时序（2之2）

条件：在PmnPFS寄存器的PortDriveCapability中选择中间驱动输出

Parameter				Symbol	Min	Max	Unit*1	测试条件
SPI	SSL上升和下降时间	Output	2.7V或以上	t_{SSLr}, t_{SSLf}	-	10	ns	图48.51至 Figure 48.56
			2.4V或以上		-	15		
			1.8V或以上		-	20		
		Input			-	1	µs	
	从站访问时间		2.4V或以上	t_{SA}	-	2 × t_{Pcyc} + 100	ns	图48.55和 Figure 48.56
			1.8V或以上		-	2 × t_{Pcyc} + 140		
	从机输出释放时间		2.4V或以上	t_{REL}	-	2 × t_{Pcyc} + 100	ns	
			1.8V或以上		-	2 × t_{Pcyc} + 140		

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N由SPCKD寄存器设置为从1到8的整数。
Note 3. N由SSLND寄存器设置为1到8的整数。
Note 4. RSPCK的上限为16MHz。

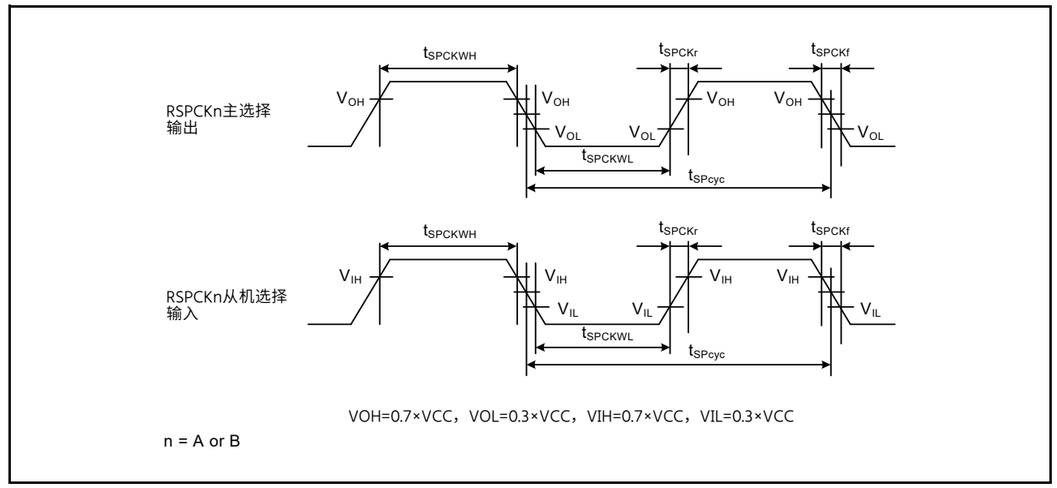


Figure 48.50 SPI时钟时序

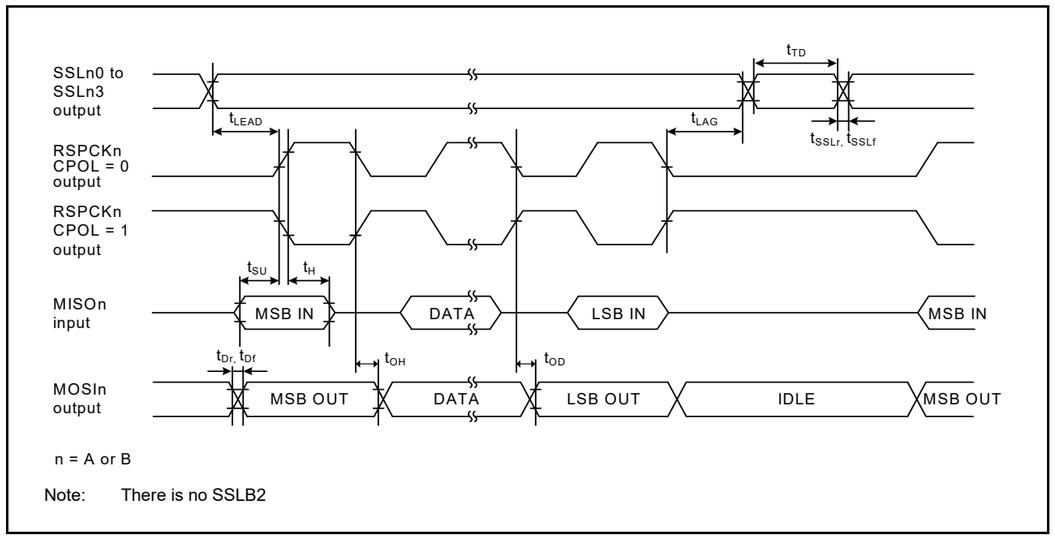


Figure 48.51 SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to any value other than 1/2)

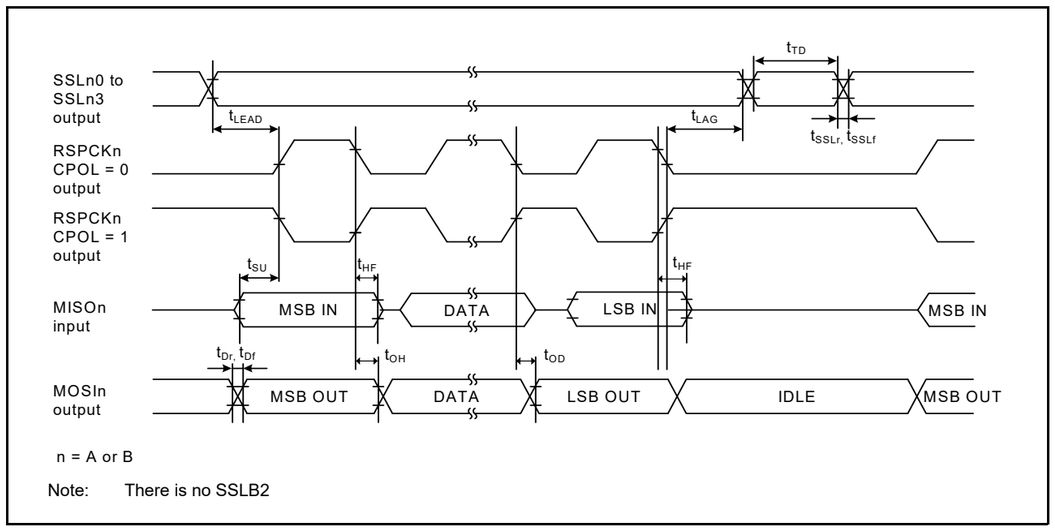


Figure 48.52 SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)

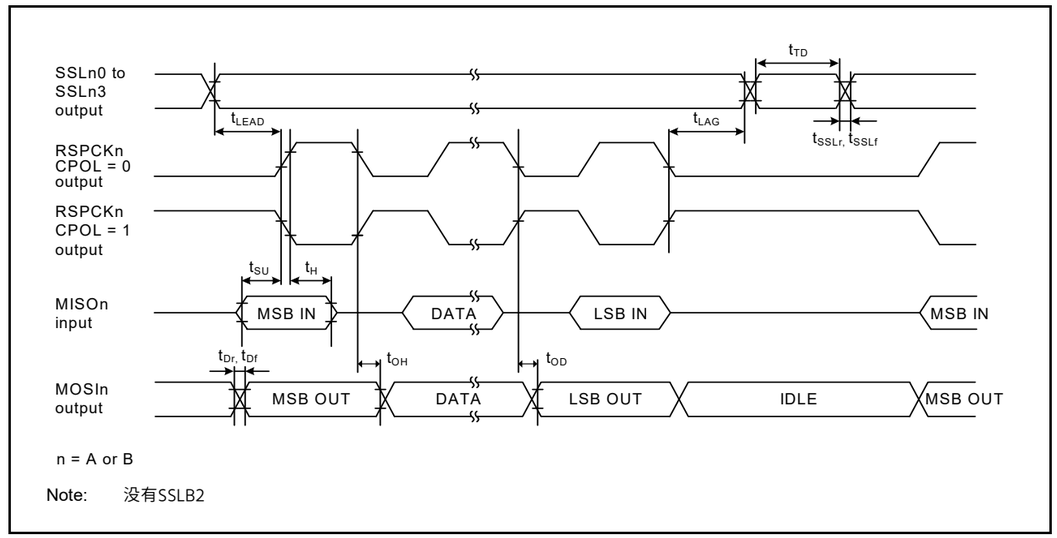


Figure 48.51 SPI时序（主机，CPHA=0）（比特率：PCLKA分频比设置为12以外的任何值）

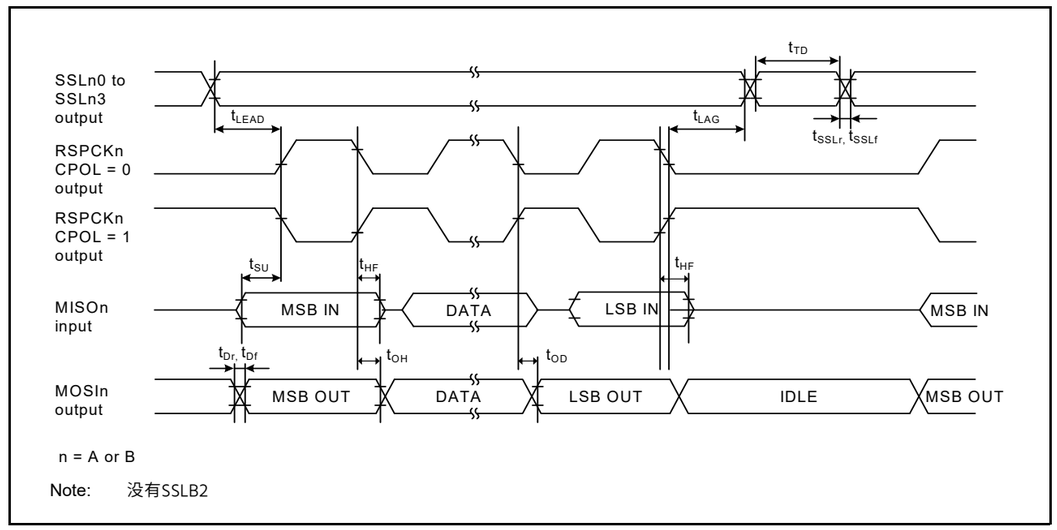


Figure 48.52 SPI时序（主控，CPHA=0）（比特率：PCLKA分频比设置为12）

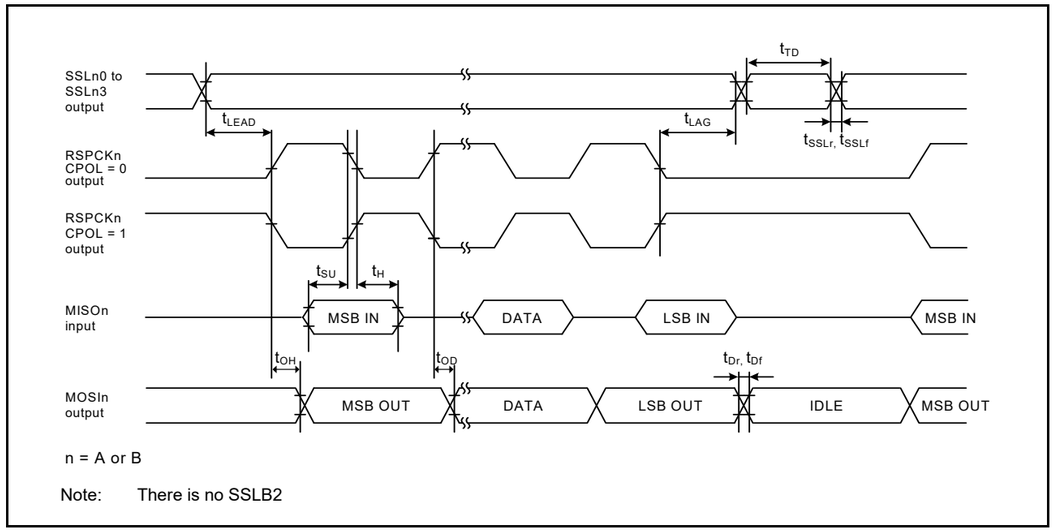


Figure 48.53 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to any value other than 1/2)

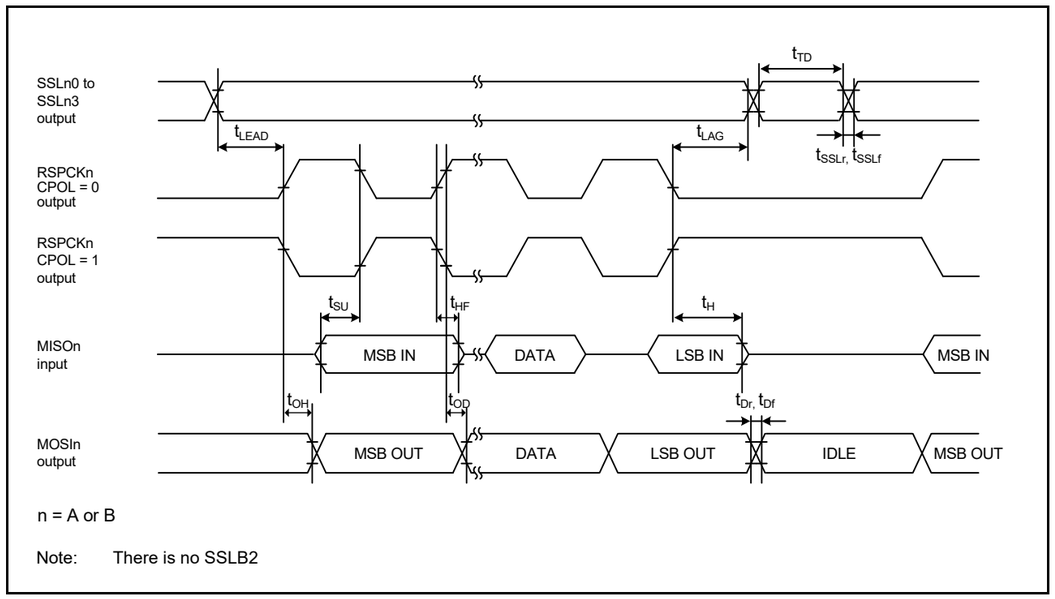


Figure 48.54 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to 1/2)

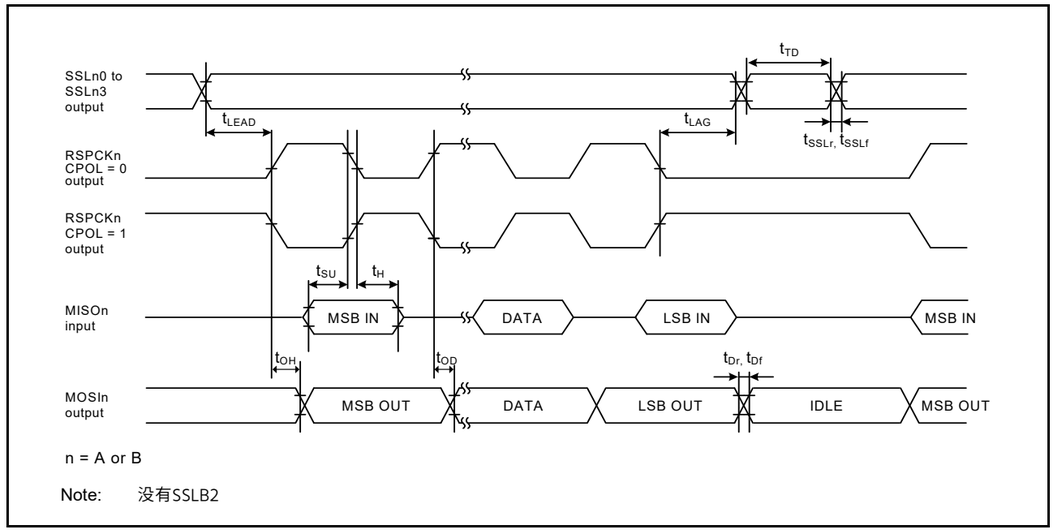


Figure 48.53 SPI时序（主机，CPHA=1）（比特率：PCLKA分频比设置为12以外的任何值）

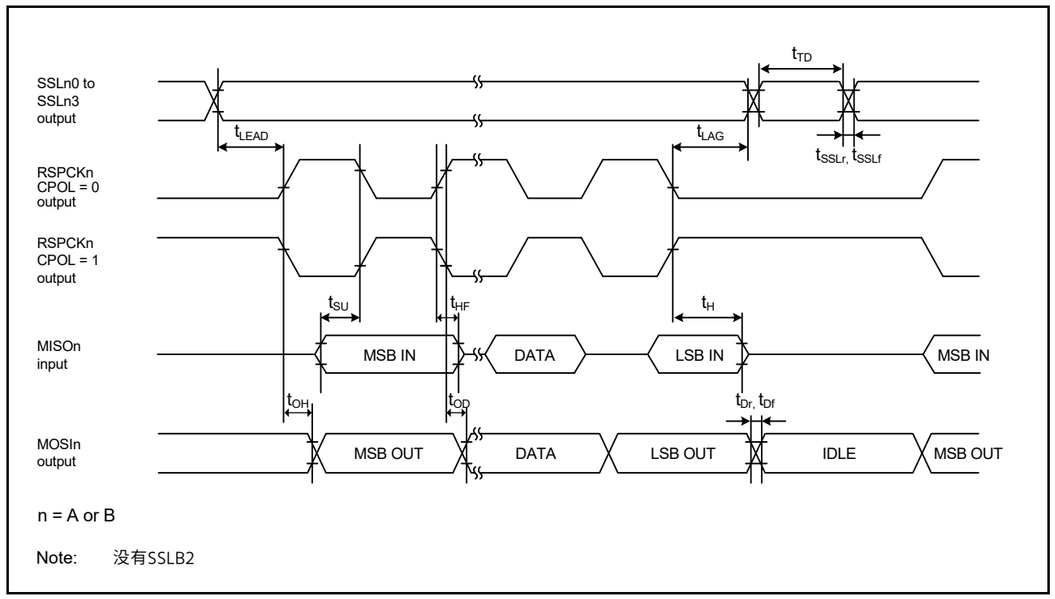


Figure 48.54 SPI时序（主控，CPHA=1）（比特率：PCLKA分频比设置为12）

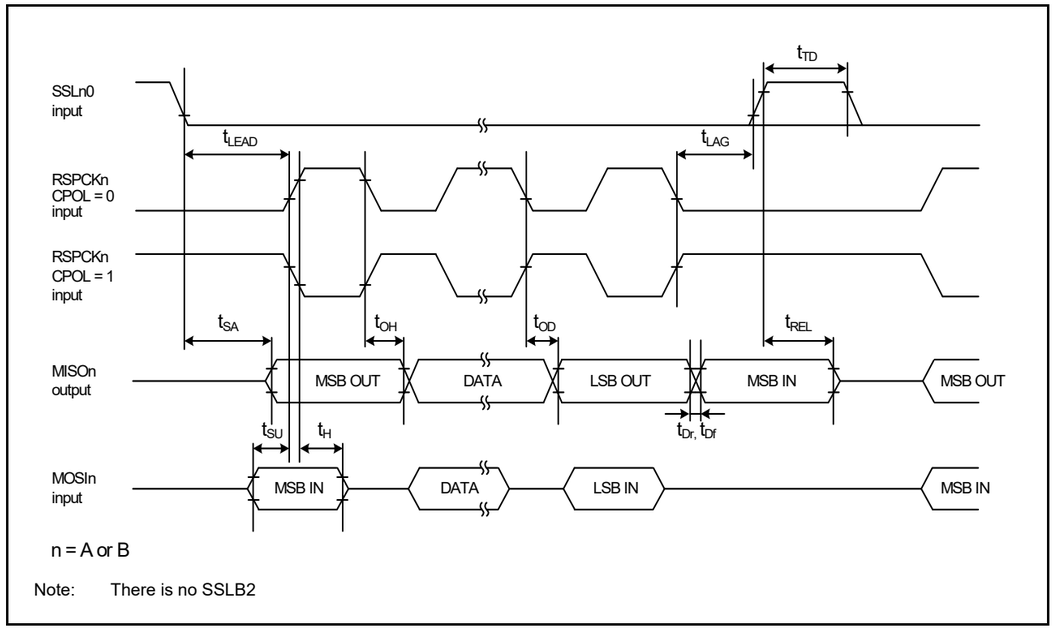


Figure 48.55 SPI timing (slave, CPHA = 0)

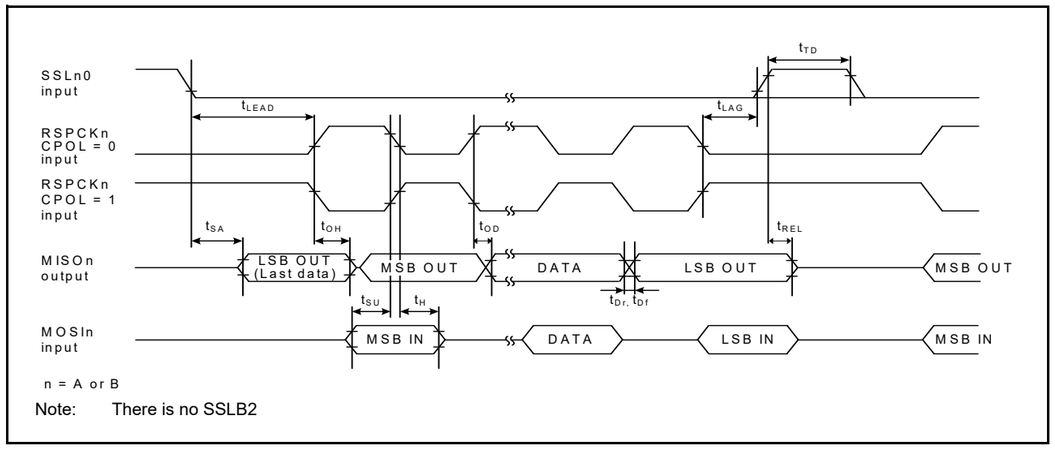


Figure 48.56 SPI timing (slave, CPHA = 1)

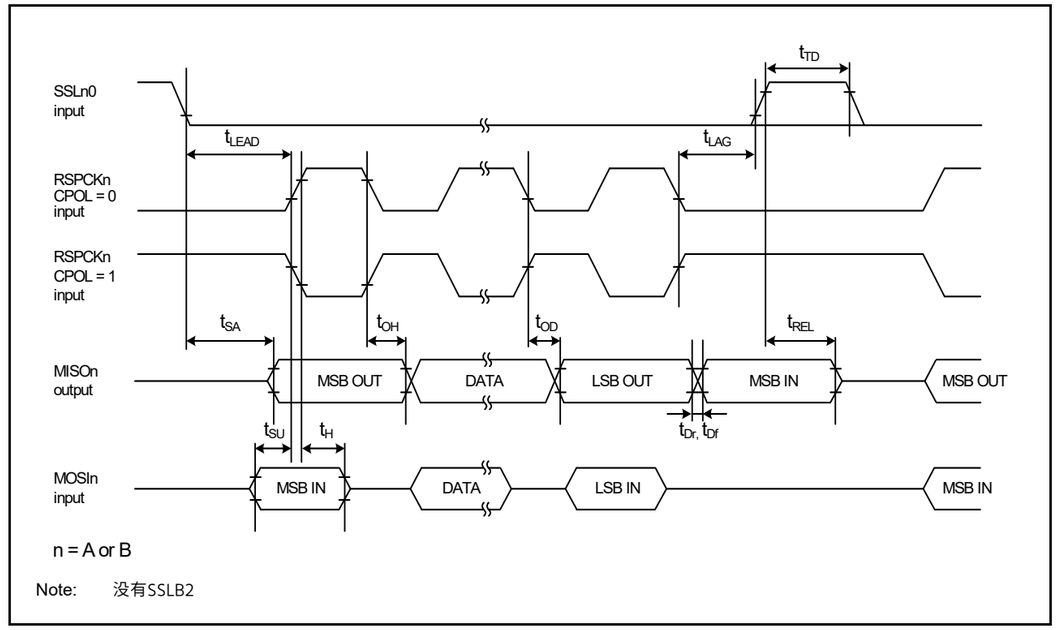


Figure 48.55 SPI时序（从机，CPHA=0）

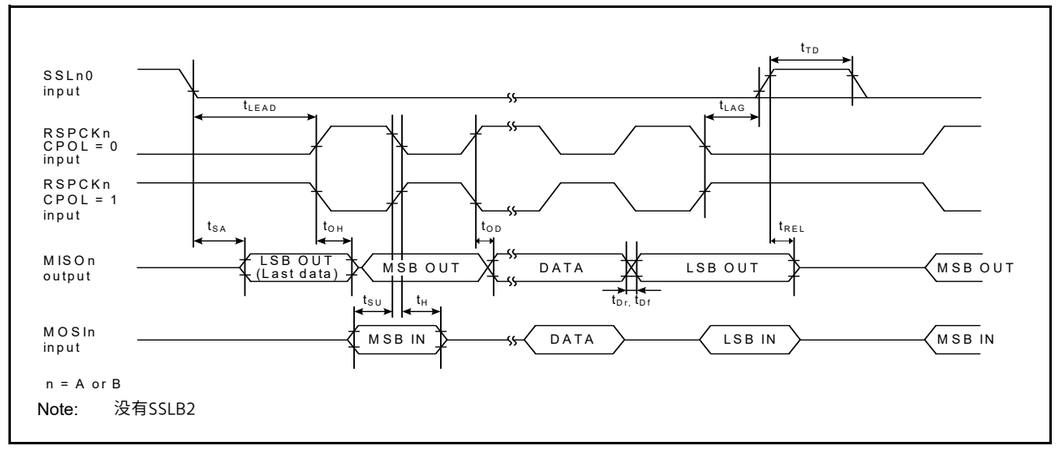


Figure 48.56 SPI时序（从机，CPHA=1）

48.3.10 IIC Timing

Table 48.38 IIC timing
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 48.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 48.57 For all ports, use PmnPFS.DSCR of middle drive.
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

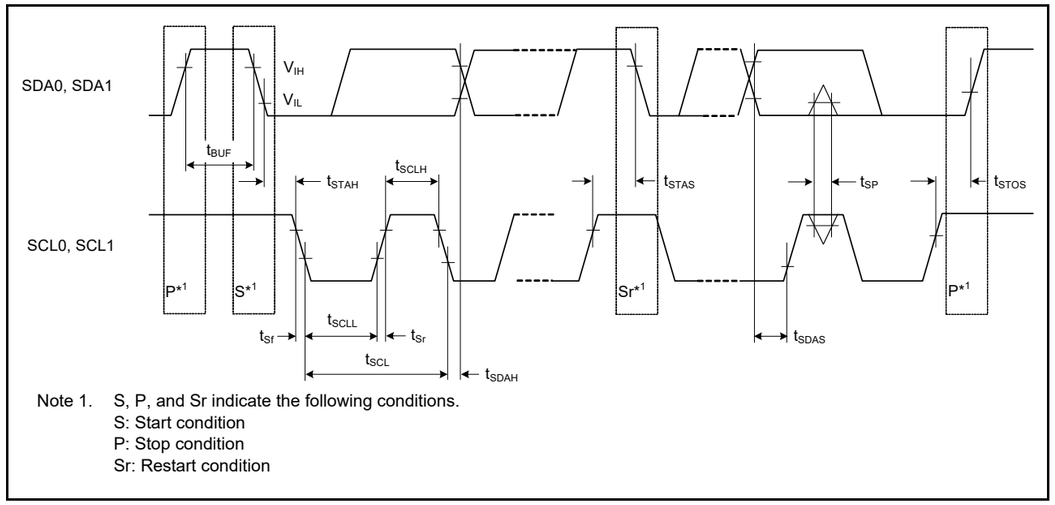
Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle
Note 1. The value in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

48.3.10 IIC Timing

Table 48.38 IIC timing
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	Min*1	Max	Unit	测试条件
IIC (standard mode, SMBus)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 48.57
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	1000	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间（禁用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA输入总线空闲时间（启用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START条件输入保持时间（禁用唤醒功能时）	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START条件输入保持时间（启用唤醒功能时）	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	-	ns	
	STOP条件输入建立时间	t_{STOS}	1000	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC (Fast mode)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	图48.57对于所有端口，使用中间驱动器的PmnPFS.DSCR。
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	300	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间（禁用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA输入总线空闲时间（启用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START条件输入保持时间（禁用唤醒功能时）	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START条件输入保持时间（启用唤醒功能时）	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	300	-	ns	
	STOP条件输入建立时间	t_{STOS}	300	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期，tPcyc:PCLKB周期
Note 1. 括号中的值适用于ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时。



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

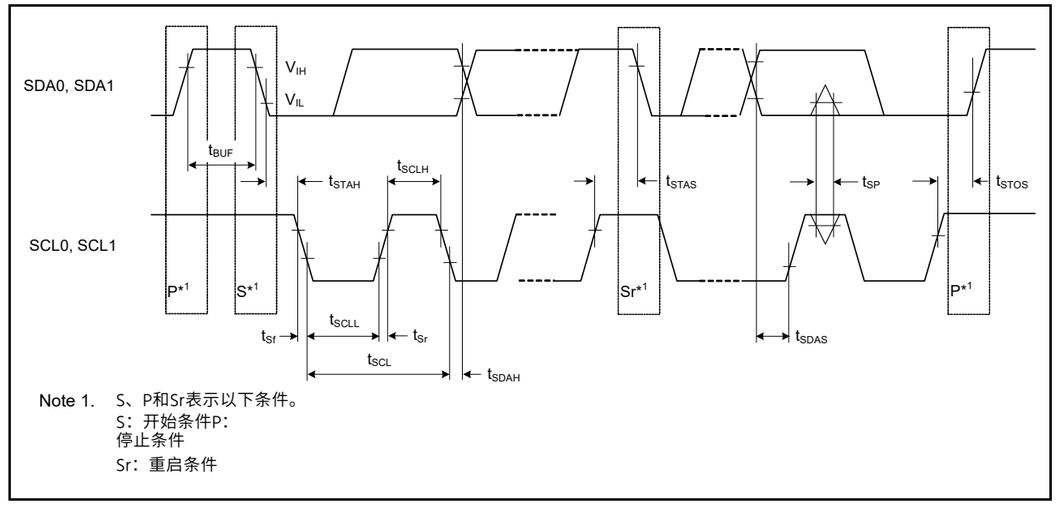
Figure 48.57 I²C bus interface input/output timing

48.3.11 CLKOUT Timing

Table 48.39 CLKOUT timing

Parameter			Symbol	Min	Max	Unit*1	Test conditions
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t_{Ccyc}	62.5	-	ns	Figure 48.58
		VCC = 1.8 V or above		125	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t_{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t_{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
CLKOUT_RF*3	CLKOUT_RF pin output cycle		t_{CRFcyc}	250	-	ns	Figure 48.59
	CLKOUT_RF pin high pulse width		t_{CRFH}	100	-	ns	
	CLKOUT_RF pin low pulse width		t_{CRFL}	100	-	ns	
	CLKOUT_RF pin output rise time		t_{CRFr}	-	5	ns	
	CLKOUT_RF pin output fall time		t_{CRFf}	-	5	ns	

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.
Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).
Note 3. The voltage for VCC_RF when CLKOUT_RF pin is to be used is between 3.0 V and 3.6 V.



Note 1. S、P和Sr表示以下条件。
S：开始条件P：
停止条件
Sr：重启条件

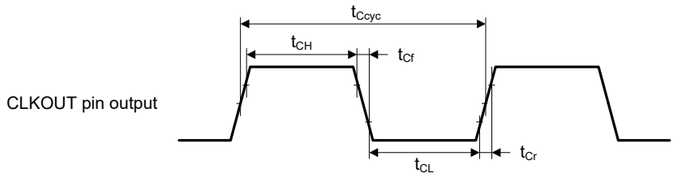
Figure 48.57 I2C总线接口输入输出时序

48.3.11 CLKOUT Timing

Table 48.39 CLKOUT timing

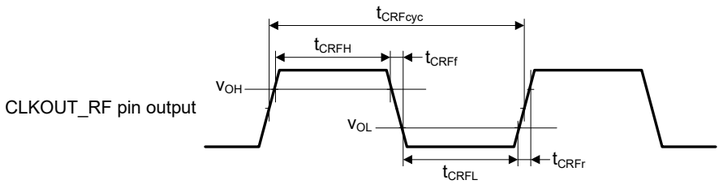
Parameter			Symbol	Min	Max	Unit*1	测试条件
CLKOUT	CLKOUT引脚输出周期*1	VCC=2.7V或以上	t_{Ccyc}	62.5	-	ns	Figure 48.58
		VCC=1.8V或以上		125	-		
	CLKOUT引脚高脉冲宽度*2	VCC=2.7V或以上	t_{CH}	15	-	ns	
		VCC=1.8V或以上		30	-		
	CLKOUT引脚低脉冲宽度*2	VCC=2.7V或以上	t_{CL}	15	-	ns	
		VCC=1.8V或以上		30	-		
	CLKOUT引脚输出上升时间	VCC=2.7V或以上	t_{Cr}	-	12	ns	
		VCC=1.8V或以上		-	25		
	CLKOUT引脚输出下降时间	VCC=2.7V或以上	t_{Cf}	-	12	ns	
		VCC=1.8V或以上		-	25		
CLKOUT_RF*3	CLKOUT_RF引脚输出周期		t_{CRFcyc}	250	-	ns	Figure 48.59
	CLKOUT_RF引脚高脉冲宽度		t_{CRFH}	100	-	ns	
	CLKOUT_RF引脚低脉冲宽度		t_{CRFL}	100	-	ns	
	CLKOUT_RF引脚输出上升时间		t_{CRFr}	-	5	ns	
	CLKOUT_RF引脚输出下降时间		t_{CRFf}	-	5	ns	

Note 1. 当使用EXTAL外部时钟输入或振荡器以1分频（CKOCR.CKOSEL[2:0]位为011b，CKOCR.CKODIV[2:0]位为000b）从CLKOUT输出时，上述应满足45至55%的输入占空比。
Note 2. WhentheMOCOisselectedastheclockoutputsource(theCKOCR.CKOSEL[2:0]bitsare001b) settheclockoutputdivisionratioselectiontobedividedby2(theCKOCR.CKODIV[2:0]bitsare001b）。
Note 3. 使用CLKOUT_RF引脚时，VCC_RF的电压在3.0V和3.6V之间。



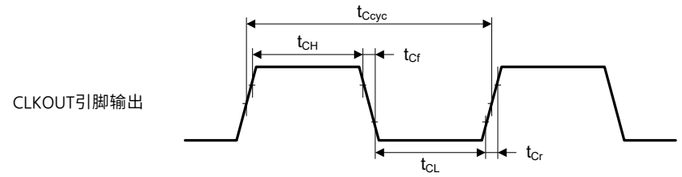
Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 48.58 CLKOUT output timing



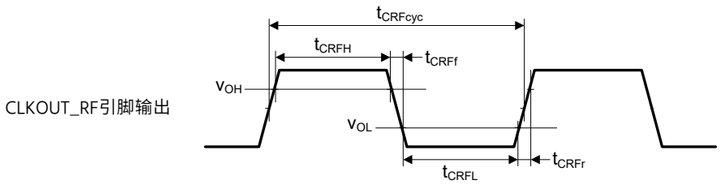
Test conditions: V_{OH} = VCC_RF × 0.8 , V_{OL} = VCC_RF × 0.2
Note. The voltage for VCC_RF pin when CLKOUT_RF is to be used is between 3.0 V and 3.6 V.

Figure 48.59 CLKOUT_RF Output Timing



测试条件：VOH=VCC×0.7，VOL=VCC×0.3，IOH=−1.0mA，IOL=1.0mA，C=30pF

Figure 48.58 CLKOUT输出时序



测试条件：VOH=VCC_RF×0.8 VOL=VCC_RF×0.2
笔记。使用CLKOUT_RF时VCC_RF管脚的电压在3.0V和3.6V之间。

Figure 48.59 CLKOUT_RF输出时序

48.4 USB Characteristics

48.4.1 USBFS Timing

Table 48.40 USB characteristics

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85°C (USBCLKSEL = 1)

Parameter			Symbol	Min	Max	Unit	Test conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	-	V	-
	Input low level voltage		V_{IL}	-	0.8	V	-
	Differential input sensitivity		V_{DI}	0.2	-	V	| USB_DP - USB_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	-
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 48.60, Figure 48.61, Figure 48.62
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not required.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D + sink current		I_{DP_SINK}	25	175	µA	-
	D – sink current		I_{DM_SINK}	25	175	µA	-
	DCD source current		I_{DP_SRC}	7	13	µA	-
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	-
	D + source voltage		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D – source voltage		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

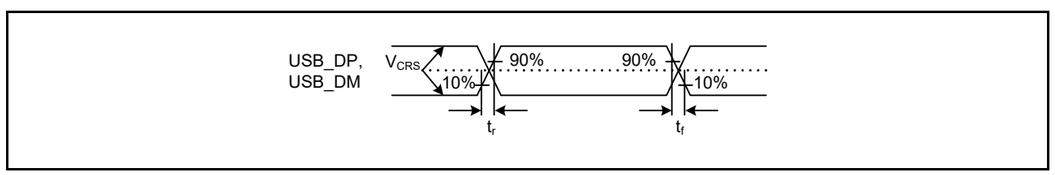


Figure 48.60 USB_DP and USB_DM output timing

48.4 USB特性

48.4.1 USBFS Timing

Table 48.40 USB特性

条件：VCC=VCC_USB=3.0至3.6V，Ta=−20至+85°C(USBCLKSEL=1)

Parameter			Symbol	Min	Max	Unit	测试条件
输入特性	输入高电平电压		V_{IH}	2.0	-	V	-
	输入低电平电压		V_{IL}	-	0.8	V	-
	差分输入灵敏度		V_{DI}	0.2	-	V	| USB_DP - USB_DM |
	差分共模范围		V_{CM}	0.8	2.5	V	-
输出特性	输出高电平电压		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	输出低电平电压		V_{OL}	0.0	0.3	V	我OL=2毫安
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 48.60, Figure 48.61, Figure 48.62
	上升时间	FS	t_r	4	20	ns	
		LS		75	300		
	秋季时间	FS	t_f	4	20	ns	
		LS		75	300		
	上升下降时间比	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	输出电阻		Z_{DRV}	28	44	Ω	（不需要调整外部元件的电阻。）
VBUS characteristics	VBUS输入电压		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	空闲状态期间
			R_{PUA}	1.425	3.09	kΩ	接待期间
电池充电 Specification Ver 1.2	D+灌电流		I_{DP_SINK}	25	175	µA	-
	D 灌电流		I_{DM_SINK}	25	175	µA	-
	DCD源电流		I_{DP_SRC}	7	13	µA	-
	数据检测电压		V_{DAT_REF}	0.25	0.4	V	-
	D+源电压		V_{DP_SRC}	0.5	0.7	V	输出电流=250µA
	D——源电压		V_{DM_SRC}	0.5	0.7	V	输出电流=250µA

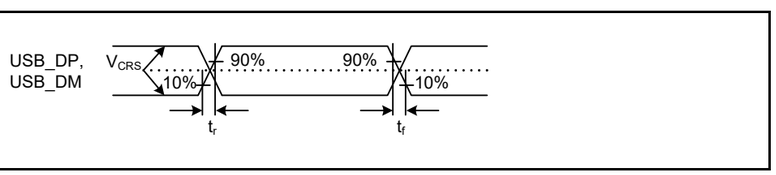


Figure 48.60 USB_DP和USB_DM输出时序

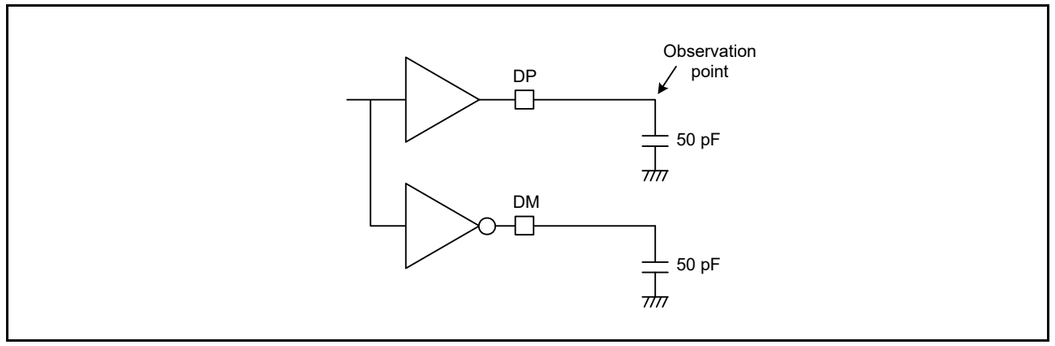


Figure 48.61 Test circuit for Full-Speed (FS) connection

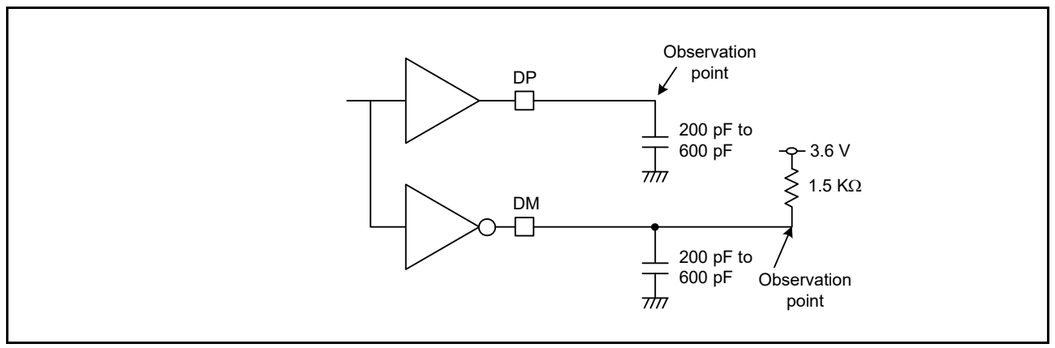


Figure 48.62 Test circuit for Low-Speed (LS) connection

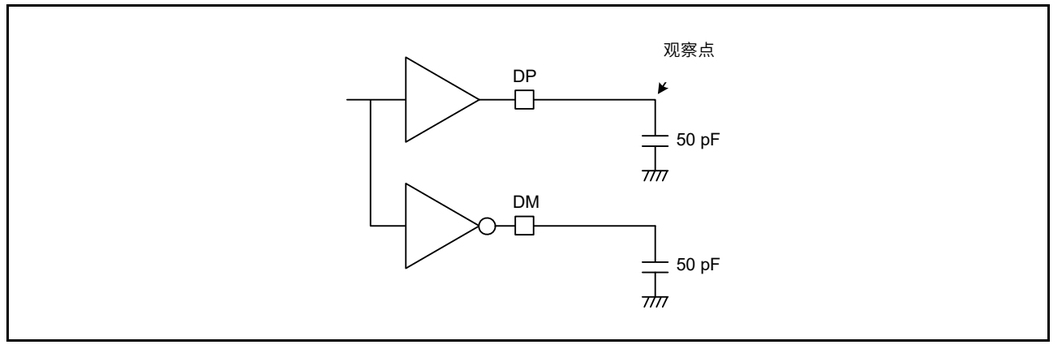


Figure 48.61 全速(FS)连接测试电路

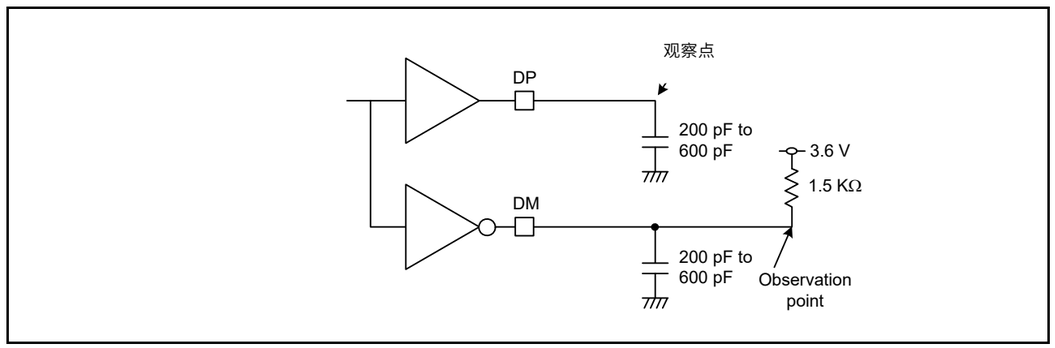


Figure 48.62 低速(LS)连接测试电路

48.5 ADC14 Characteristics

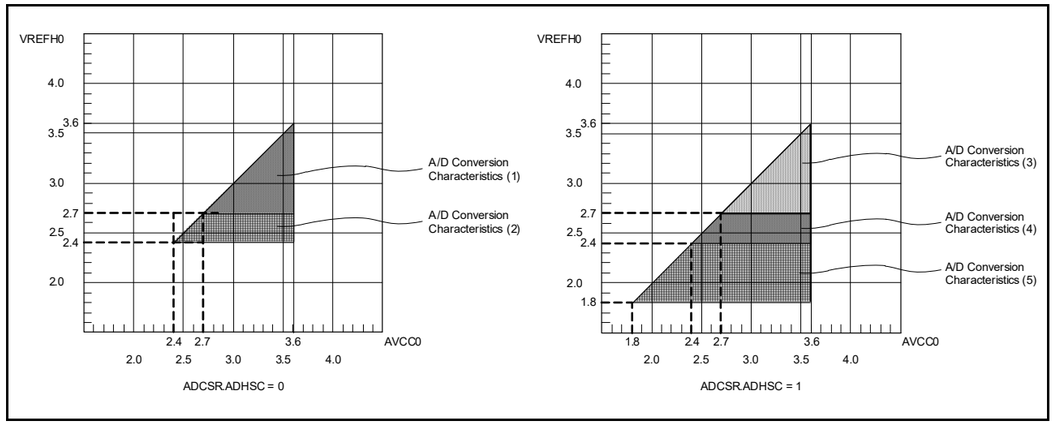


Figure 48.63 AVCC0 to VREFH0 voltage range

Table 48.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	48	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.94	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

48.5 ADC14 Characteristics

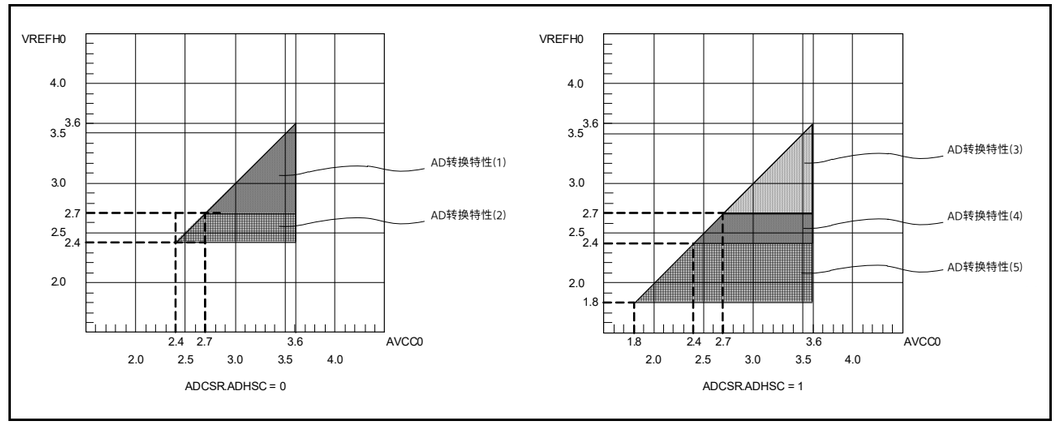


Figure 48.63 AVCC0至VREFH0电压范围

Table 48.41 高速AD转换模式下的AD转换特性(1)(1of2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Frequency		1	-	48	MHz	-
模拟输入电容*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
模拟输入电阻	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 48 MHz)	允许的信号源阻抗 Max.=0.3kΩ	0.94	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	上述以外
DNL微分非线性误差		-	±1.0	-	LSB	-
INL积分非线性误差		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

Table 48.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 48.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 48.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	32	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.41	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						

Table 48.41 高速AD转换模式下的AD转换特性(1)(2of2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Conversion time*1 (Operation at PCLKC = 48 MHz)	允许的信号源阻抗 Max.=0.3kΩ	1.06	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	上述以外
DNL微分非线性误差		-	±4.0	-	LSB	-
INL积分非线性误差		-	±4.0	±12.0	LSB	-

Note: 该特性适用于不使用除14位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。
Note 1. 转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。
Note 2. 除IO输入电容(Cin)外，请参阅第48.2.4节，IOVOH、VOL和其他特性。

Table 48.42 高速AD转换模式下的AD转换特性(2)(1of2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Frequency		1	-	32	MHz	-
模拟输入电容*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
模拟输入电阻	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	允许的信号源阻抗 Max.=1.3kΩ	1.41	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	上述以外
DNL微分非线性误差		-	±1.0	-	LSB	-
INL积分非线性误差		-	±1.0	±3.0	LSB	-
14-bit mode						

Table 48.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 48.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 48.43 A/D conversion characteristics (3) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	24	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-

Table 48.42 高速AD转换模式下的AD转换特性(2)(2of2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	允许的信号源阻抗 Max.=1.3kΩ	1.59	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	上述以外
DNL微分非线性误差		-	±4.0	-	LSB	-
INL积分非线性误差		-	±4.0	±12.0	LSB	-

Note: 该特性适用于不使用除14位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。
Note 1. 转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。
Note 2. 除IO输入电容(Cin)外，请参阅第48.2.4节，IOVOH、VOL和其他特性。

Table 48.43 低功耗AD转换模式下的AD转换特性(3)(1of2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Frequency		1	-	24	MHz	-
模拟输入电容*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
模拟输入电阻	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	允许的信号源阻抗 Max.=1.1kΩ	2.25	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	上述以外
DNL微分非线性误差		-	±1.0	-	LSB	-
INL积分非线性误差		-	±1.0	±3.0	LSB	-

Table 48.43 A/D conversion characteristics (3) in low power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 48.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 48.44 A/D conversion characteristics (4) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	16	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.38	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-

Table 48.43 低功耗AD转换模式下的AD转换特性(3)(2of2)
Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	允许的信号源阻抗 Max.=1.1kΩ	2.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	上述以外
DNL微分非线性误差		-	±4.0	-	LSB	-
INL积分非线性误差		-	±4.0	±12.0	LSB	-

Note: 该特性适用于不使用除14位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

Note 1. 转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

Note 2. 除IO输入电容(Cin)外，请参阅第48.2.4节，IOVOH、VOL和其他特性。

Table 48.44 低功耗AD转换模式下的AD转换特性(4)(1of2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Frequency		1	-	16	MHz	-
模拟输入电容*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
模拟输入电阻	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	允许的信号源阻抗 Max.=2.2kΩ	3.38	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	上述以外
DNL微分非线性误差		-	±1.0	-	LSB	-

Table 48.44 A/D conversion characteristics (4) in low power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 48.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 48.45 A/D conversion characteristics (5) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	8	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above

Table 48.44 低功耗AD转换模式下的AD转换特性(4)(2of2)
Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
INL积分非线性误差		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	允许的信号源阻抗 Max.=2.2kΩ	3.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	上述以外
DNL微分非线性误差		-	±4.0	-	LSB	-
INL积分非线性误差		-	±4.0	±12.0	LSB	-

Note: 该特性适用于不使用除14位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

Note 1. 转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

Note 2. 除IO输入电容(Cin)外，请参阅第48.2.4节，IOVOH、VOL和其他特性。

Table 48.45 低功耗AD转换模式下的AD转换特性(5)(1of2)
条件：VCC=AVCC0=1.8至3.6V（当VCC<2.0V时AVCC0=VCC），VREFH0=1.8至3.6V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
Frequency		1	-	8	MHz	-
模拟输入电容*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
模拟输入电阻	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	允许的信号源阻抗 Max.=5kΩ	6.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	上述以外
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	上述以外

Table 48.45 A/D conversion characteristics (5) in low power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 3.6 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	7.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.88	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±12.0	±32.0	LSB	High-precision channel
				±48.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 48.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

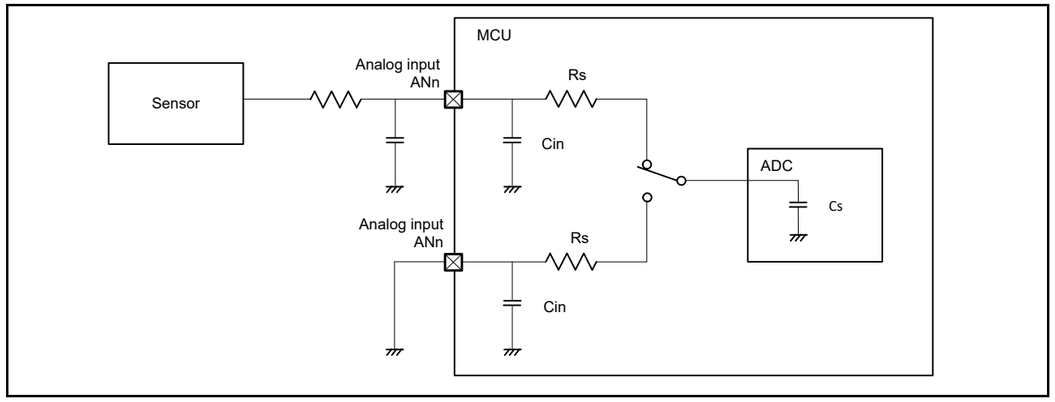


Figure 48.64 Equivalent circuit for analog input

Table 48.46 14-bit A/D converter channel classification (1 of 2)

Classification	Channel	Conditions	Remarks
High-precision channel	AN004 to AN006, AN009, AN010	AVCC0 = 1.8 to 3.6 V	Pins AN004 to AN006, AN009 and AN010 cannot be used as general I/O, IRQ3 inputs, and TS transmission, when the A/D converter is in use
Normal-precision channel	AN017, AN019, AN020		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	-

Table 48.45 低功耗AD转换模式下的AD转换特性(5)(2of2)
条件：VCC=AVCC0=1.8至3.6V（当VCC<2.0V时AVCC0=VCC），VREFH0=1.8至3.6V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
DNL微分非线性误差		-	±1.0	-	LSB	-
INL积分非线性误差		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	允许的信号源阻抗 Max.=5kΩ	7.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.88	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
偏移误差		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	上述以外
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	上述以外
量化误差		-	±0.5	-	LSB	-
绝对精度		-	±12.0	±32.0	LSB	High-precision channel
				±48.0	LSB	上述以外
DNL微分非线性误差		-	±4.0	-	LSB	-
INL积分非线性误差		-	±4.0	±12.0	LSB	-

Note: 该特性适用于不使用除14位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

Note 1. 转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

Note 2. 除IO输入电容(Cin)外，请参阅第48.2.4节，IOVOH、VOL和其他特性。

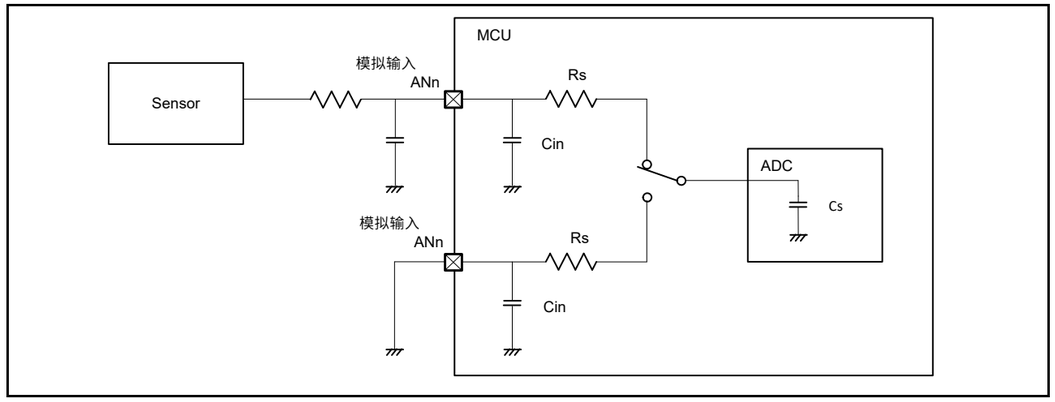


Figure 48.64 模拟输入等效电路

Table 48.46 14位AD转换器通道分类(1of2)

Classification	Channel	Conditions	Remarks
High-precision channel	AN004 to AN006, AN009, AN010	AVCC0 = 1.8 to 3.6 V	AN004至AN006、AN009和AN010引脚不能用作通用I O、IRQ3输入和TS传输，当使用AD转换器时
Normal-precision channel	AN017, AN019, AN020		
内部参考电压输入通道	内部参考电压	AVCC0 = 2.0 to 3.6 V	-

Table 48.46 14-bit A/D converter channel classification (2 of 2)

Classification	Channel	Conditions	Remarks
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	-

Table 48.47 A/D internal reference voltage characteristics
Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 3.6 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Frequency*3	1	-	2	MHz	-
Sampling time*4	5.0	-	-	µs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.
Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.
Note 3. This is a parameter for ADC14 when the internal reference voltage is used as a high-potential reference voltage.
Note 4. This is a parameter for ADC14 when the internal reference voltage is selected for an analog input channel in ADC14.

Table 48.46 14位AD转换器通道分类(2of2)

Classification	Channel	Conditions	Remarks
温度传感器输入通道	温度传感器输出	AVCC0 = 2.0 to 3.6 V	-

Table 48.47 AD内部参考电压特性
Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 3.6 V*1

Parameter	Min	Typ	Max	Unit	测试条件
内部参考电压输入通道*2	1.36	1.43	1.50	V	-
Frequency*3	1	-	2	MHz	-
Sampling time*4	5.0	-	-	µs	-

Note 1. 当AVCC0<2.0V时，不能为输入通道选择内部参考电压。
Note 2. 14位AD内部参考电压是指内部参考电压输入到14位AD转换器时的电压。
Note 3. 这是内部参考电压用作高电位参考电压时ADC14的参数。
Note 4. 当为ADC14中的模拟输入通道选择内部参考电压时，这是ADC14的参数。

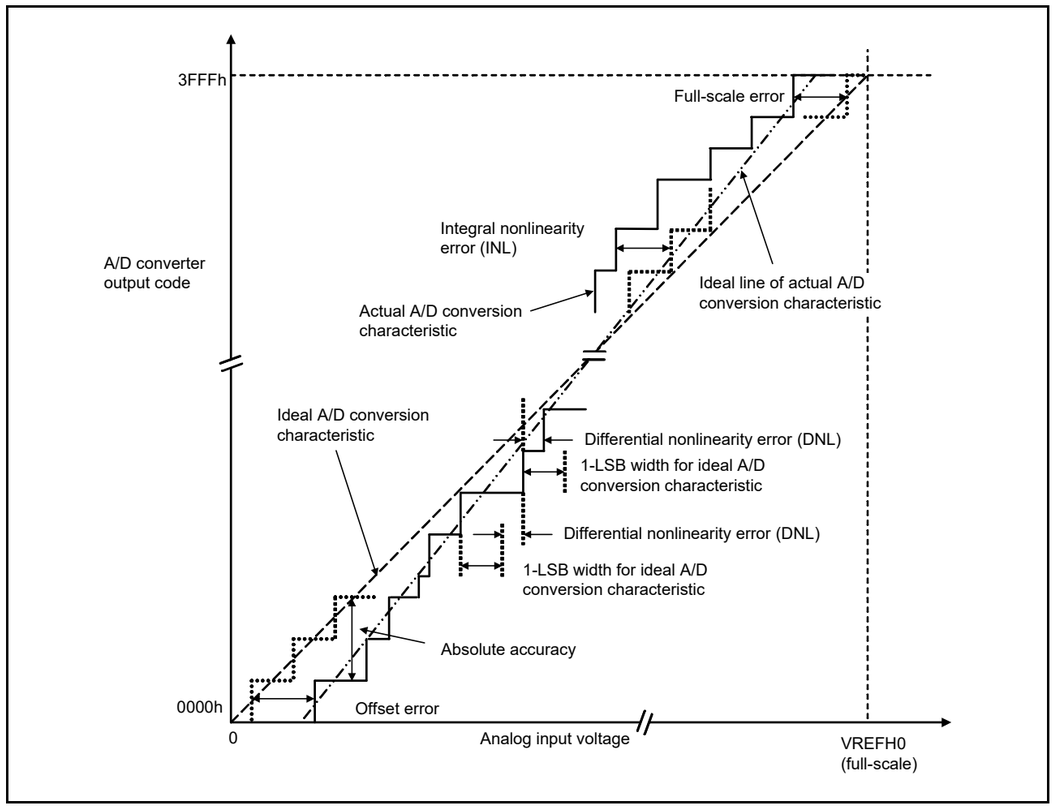


Figure 48.65 Illustration of 14-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

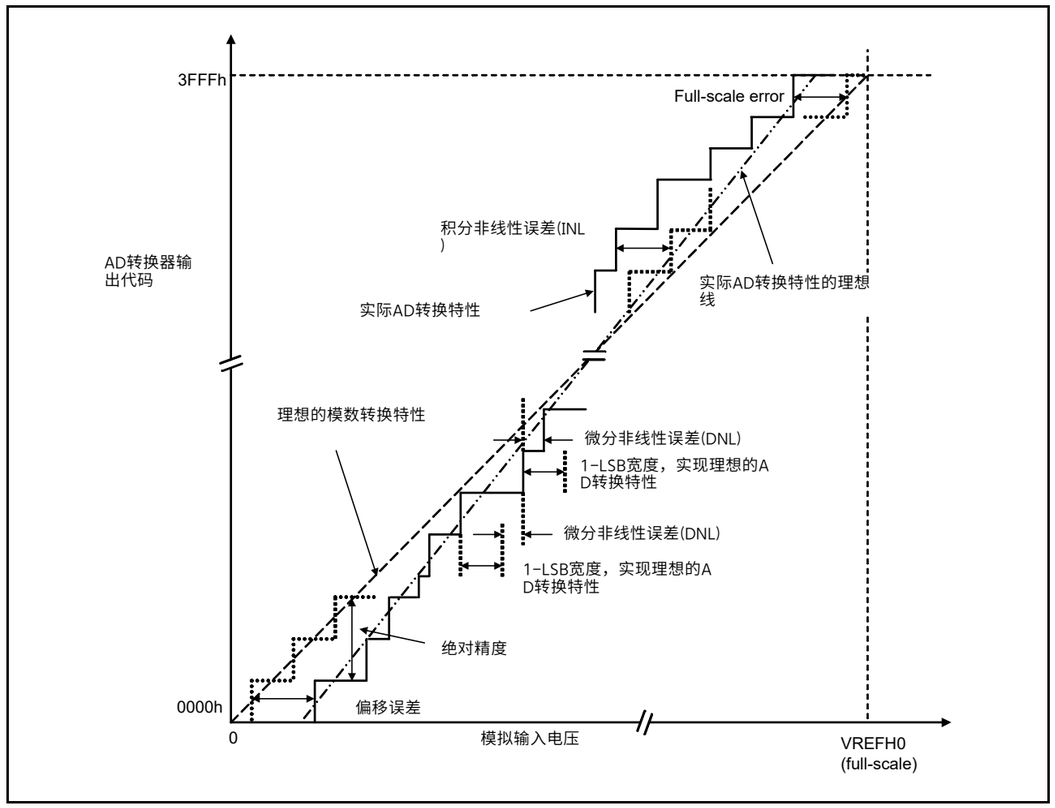


Figure 48.65 14位AD转换器特性项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。在测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压可以满足基于理论模数转换特性输出等码的预期。例如，如果使用12位分辨率并且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在003h到00Dh的范围内，尽管从理论上的AD转换特性可以预期输出代码为008h。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

48.6 DAC12 Characteristics

Table 48.48 D/A conversion characteristics (1)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V
Reference voltage = AVCC0 or AVSS0 selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	AVCC0 – 0.47	V	-
DNL differential nonlinearity error	-	±0.5	±2.0	LSB	-
INL integral nonlinearity error	-	±2.0	±8.0	LSB	-
Offset error	-	-	±30	mV	-
Full-scale error	-	-	±30	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

Table 48.49 D/A conversion characteristics (2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V
Reference voltage = internal reference voltage selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	Vbgr	V	-
DNL differential nonlinearity error	-	±2.0	±16.0	LSB	-
INL integral nonlinearity error	-	±8.0	±16.0	LSB	-
Offset error	-	-	±30	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

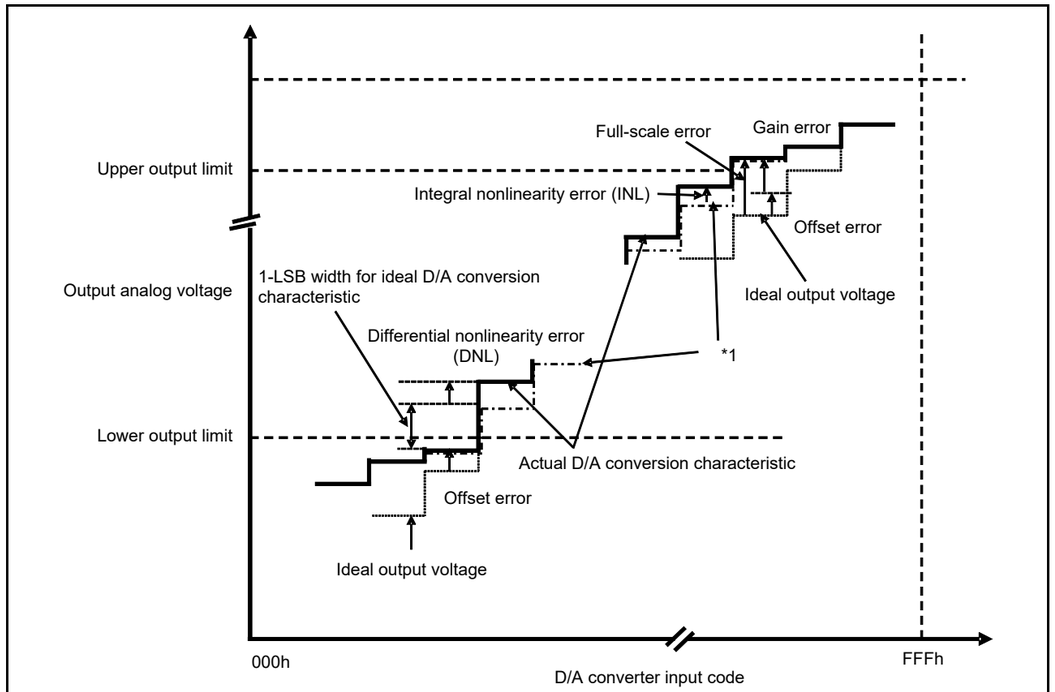
48.6 DAC12 Characteristics

Table 48.48 DA转换特性(1)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V
参考电压=选择AVCC0或AVSS0

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	-	-	12	bit	-
阻性负载	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
输出电压范围	0.35	-	AVCC0 – 0.47	V	-
DNL微分非线性误差	-	±0.5	±2.0	LSB	-
INL积分非线性误差	-	±2.0	±8.0	LSB	-
偏移误差	-	-	±30	mV	-
Full-scale error	-	-	±30	mV	-
输出阻抗	-	5	-	Ω	-
转换时间	-	-	30	μs	-

Table 48.49 DA转换特性(2)
Conditions: VCC = AVCC0 = 1.8 to 3.6 V
参考电压=选择的内部参考电压

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	-	-	12	bit	-
内部参考电压(Vbgr)	1.36	1.43	1.50	V	-
阻性负载	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
输出电压范围	0.35	-	Vbgr	V	-
DNL微分非线性误差	-	±2.0	±16.0	LSB	-
INL积分非线性误差	-	±8.0	±16.0	LSB	-
偏移误差	-	-	±30	mV	-
输出阻抗	-	5	-	Ω	-
转换时间	-	-	30	μs	-



Note 1. Ideal D/A conversion output voltage that is adjusted so that offset and full scale errors are zeroed.

Figure 48.66 Illustration of D/A converter characteristic terms

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

Differential nonlinearity error (DNL)

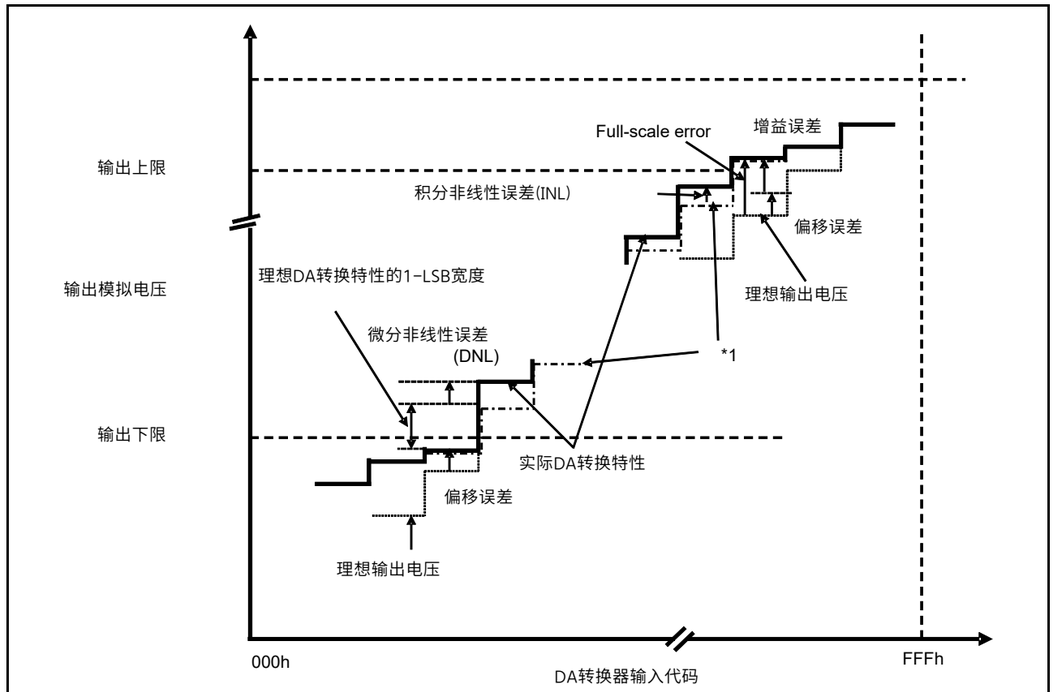
Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.



Note 1. 理想DA转换输出电压经过调整，使偏移和满量程误差为零。

Figure 48.66 数模转换器特性项说明

积分非线性误差(INL)

积分非线性误差是在测量的失调和满量程误差为零时基于理想转换特性的理想输出电压与实际输出电压之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想DA转换特性的1-LSB电压宽度与实际输出电压的宽度之差。

偏移误差

失调误差是低于输出下限的最高实际输出电压与基于输入代码的理想输出电压之间的差值。

Full-scale error

满量程误差是超出输出上限的最低实际输出电压与基于输入代码的理想输出电压之间的差值。

48.7 TSN Characteristics

Table 48.50 TSN characteristics
Conditions: VCC = AVCC0 = 2.0 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.5	-	°C	2.4 V or above
	-	-	±2.0	-	°C	Below 2.4 V
Temperature slope	-	-	–3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	-	-	5	µs	-
Sampling time	-	5	-	-	µs	-

48.8 OSC Stop Detect Characteristics

Table 48.51 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 48.67

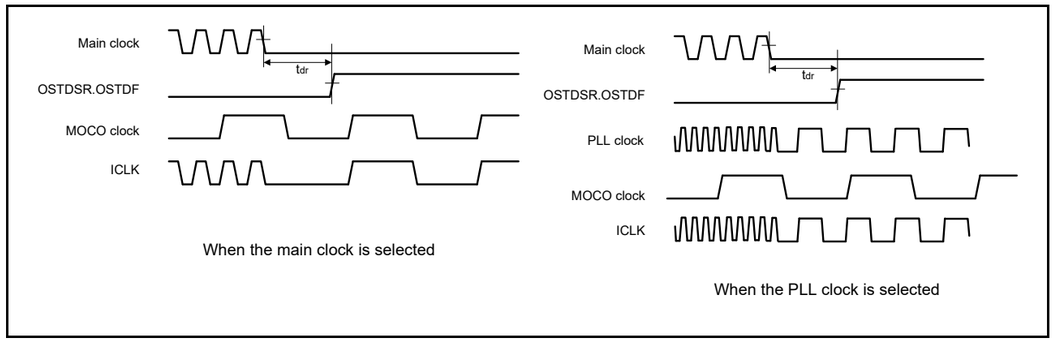


Figure 48.67 Oscillation stop detection timing

48.7 TSN Characteristics

Table 48.50 TSN characteristics
Conditions: VCC = AVCC0 = 2.0 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	-	-	±1.5	-	°C	2.4V或以上
	-	-	±2.0	-	°C	Below 2.4 V
温度斜率	-	-	–3.65	-	mV/°C	-
输出电压（25°C时）	-	-	1.05	-	V	VCC = 3.3 V
温度传感器启动时间	t_{START}	-	-	5	µs	-
采样时间	-	5	-	-	µs	-

48.8 OSC停止检测特性

Table 48.51 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	-	-	1	ms	Figure 48.67

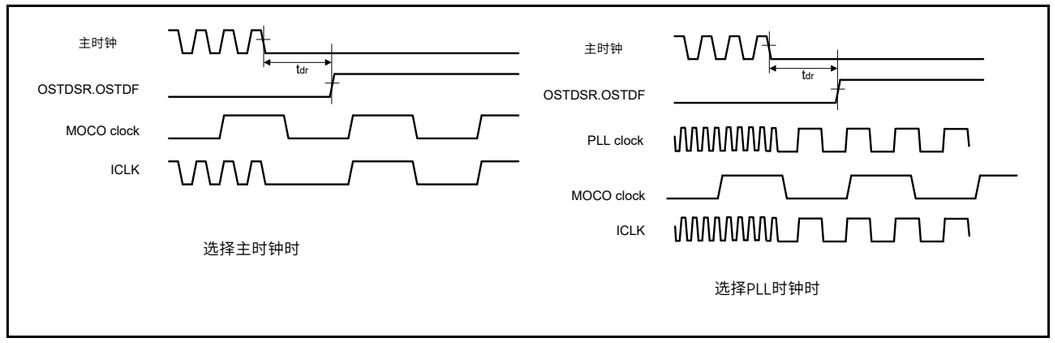


Figure 48.67 振荡停止检测时机

48.9 POR and LVD Characteristics

Table 48.52 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 48.68, Figure 48.69
	Voltage detection circuit (LVD0)*2	V_{det0_1}	2.68	2.85	2.96	V	Figure 48.70 At falling edge VCC
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
	Voltage detection circuit (LVD1)*3	V_{det1_4}	2.98	3.10	3.22	V	Figure 48.71 At falling edge VCC
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		

Note 1. These characteristics apply when noise is not superimposed on the power supply.
Note 2. # in the symbol Vdet0_# denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.

48.9 POR和LVD特性

Table 48.52 上电复位电路及电压检测电路特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 48.68, Figure 48.69
	电压检测电路（LVD0）*2	V_{det0_1}	2.68	2.85	2.96	V	Figure 48.70 在下降沿 VCC
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
	电压检测电路（LVD1）*3	V_{det1_4}	2.98	3.10	3.22	V	Figure 48.71 在下降沿 VCC
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		

Note 1. 这些特性适用于电源上没有叠加噪声的情况。
Note 2. 符号Vdet0_#中的#表示OFS1.VDSEL1[2:0]位的值。
Note 3. 符号Vdet1_#中的#表示LVDLVLR.LVD1LVL[4:0]位的值。

Table 48.53 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after power-on reset cancellation	LVD0:enable	t_{POR}	-	1.7	-	ms	-
	LVD0:disable	t_{POR}	-	1.3	-	ms	-
Wait time after voltage monitor 0,1 reset cancellation	LVD0:enable*1	$t_{LVD0,1}$	-	0.6	-	ms	-
	LVD0:disable*2	t_{LVD1}	-	0.2	-	ms	-
Response delay*3		t_{det}	-	-	350	µs	Figure 48.68, Figure 48.69
Minimum VCC down time		t_{VOFF}	450	-	-	µs	Figure 48.68, VCC = 1.0 V or above
Power-on reset enable time		$t_{W (POR)}$	1	-	-	ms	Figure 48.69, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$t_{d (E-A)}$	-	-	300	µs	Figure 48.71
Hysteresis width (POR)		V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0 and LVD1)		V_{LVH}	-	60	-	mV	LVD0 selected
			-	60	-		V_{det1_4} to V_{det1_9} selected
			-	50	-		V_{det1_A} or V_{det1_B} selected
			-	40	-		V_{det1_C} or V_{det1_F} selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0} and V_{det1} for the POR/LVD.

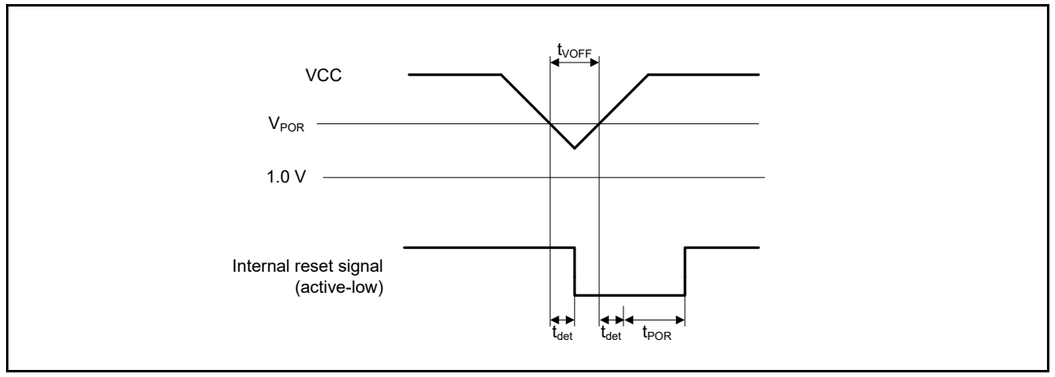


Figure 48.68 Voltage detection reset timing

Table 48.53 上电复位电路及电压检测电路特性（二）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电复位取消后的等待时间	LVD0:enable	t_{POR}	-	1.7	-	ms	-
	LVD0:disable	t_{POR}	-	1.3	-	ms	-
电压监视器0、1复位取消后的等待时间	LVD0:enable*1	$t_{LVD0,1}$	-	0.6	-	ms	-
	LVD0:disable*2	t_{LVD1}	-	0.2	-	ms	-
Response delay*3		t_{det}	-	-	350	µs	Figure 48.68, Figure 48.69
最小VCC停机时间		t_{VOFF}	450	-	-	µs	Figure 48.68, VCC=1.0V或以上
上电复位使能时间		$t_{W (POR)}$	1	-	-	ms	Figure 48.69, VCC = below 1.0 V
LVD操作稳定时间（启用LVD后）		$t_{d (E-A)}$	-	-	300	µs	Figure 48.71
迟滞宽度(POR)		V_{PORH}	-	110	-	mV	-
迟滞宽度（LVD0和LVD1）		V_{LVH}	-	60	-	mV	LVD0 selected
			-	60	-		已选择Vdet1_4至Vdet1_9
			-	50	-		选择Vdet1_A或Vdet1_B
			-	40	-		选择Vdet1_C或Vdet1_F

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. 最小VCC下降时间表示VCC低于PORLVD的电压检测电平VPOR、Vdet0和Vdet1的最小值的时间。

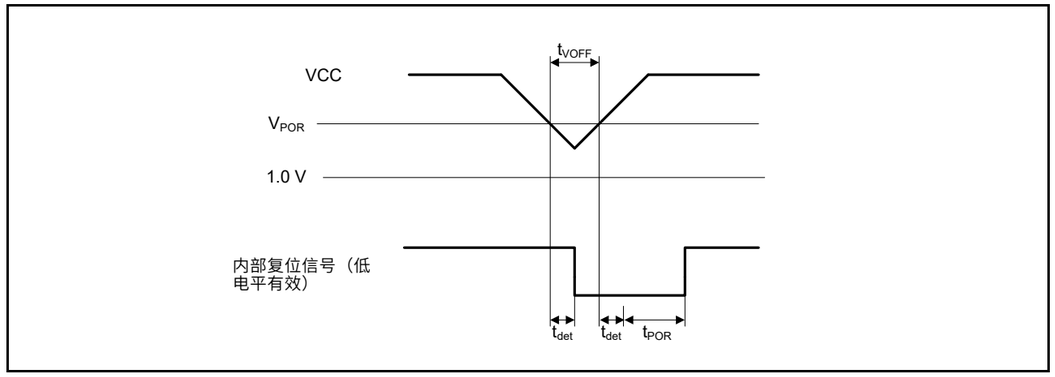
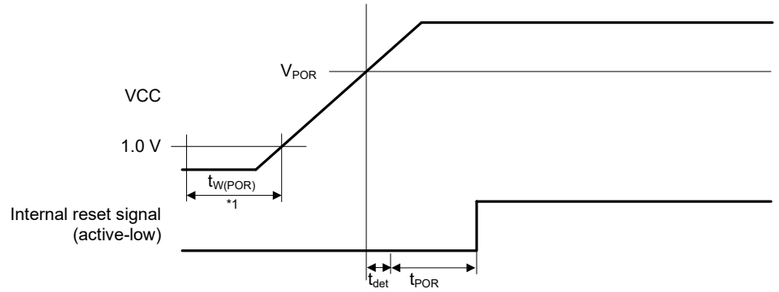


Figure 48.68 电压检测复位时序



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 48.69 Power-on reset timing

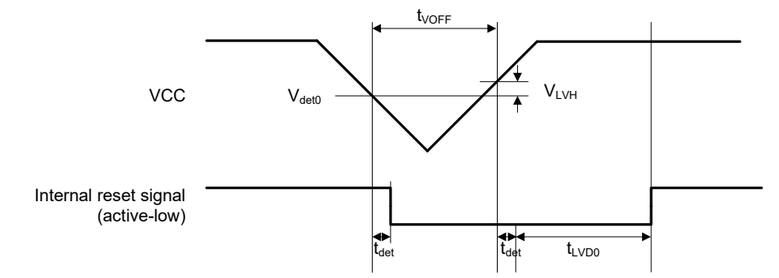
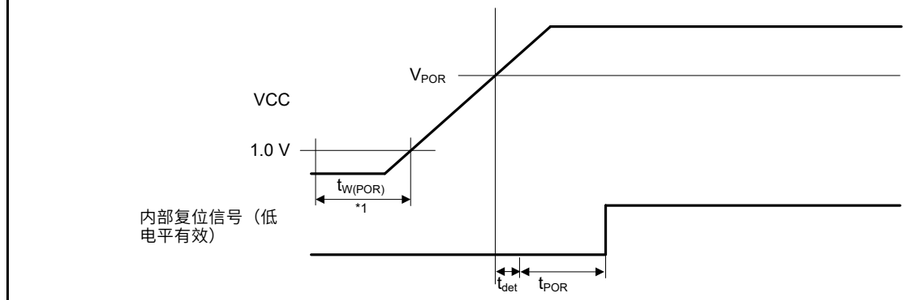


Figure 48.70 Voltage detection circuit timing (V_{det0})



Note: tW(POR)是在外部电源VCC保持在有效电压(1.0V)以下时上电复位启用所需的时间。当VCC打开时，保持tW(POR)1.0ms或更长。

Figure 48.69 上电复位时序

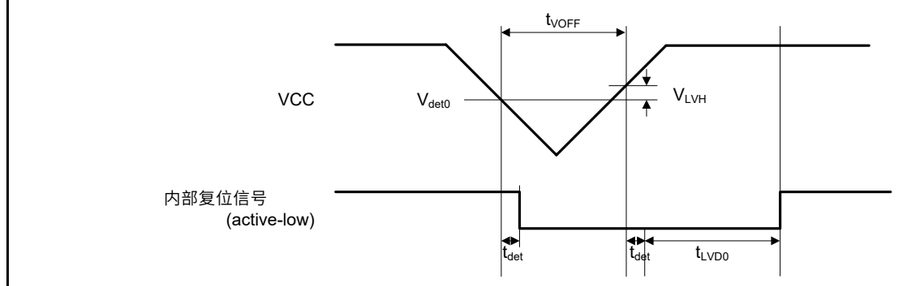


Figure 48.70 电压检测电路时序（Vdet0）

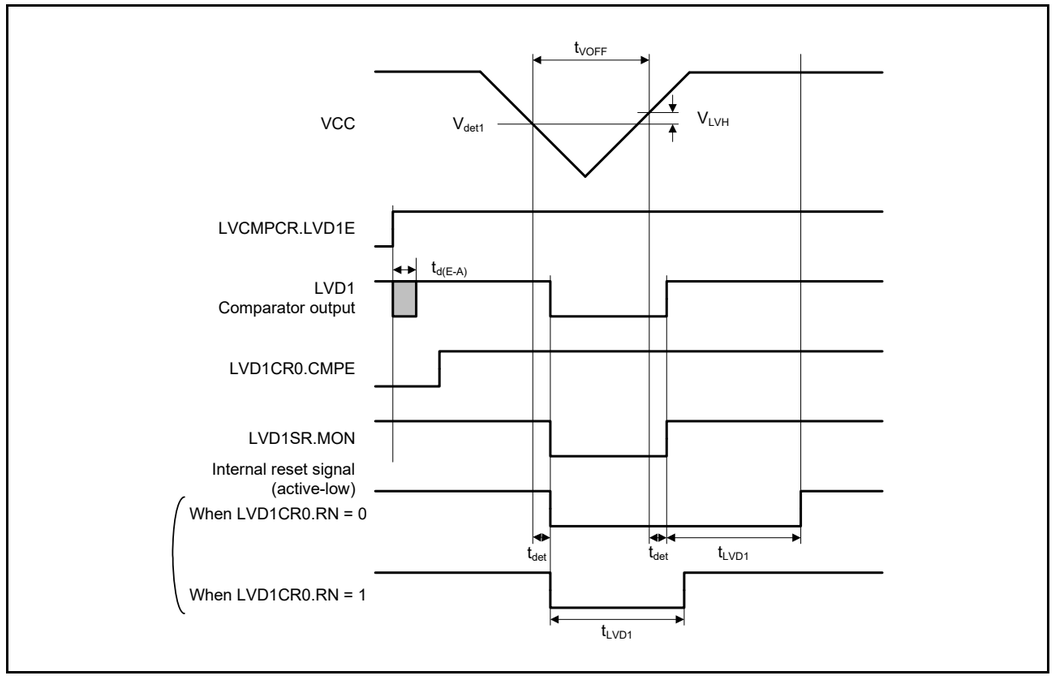


Figure 48.71 Voltage detection circuit timing (V_{det1})

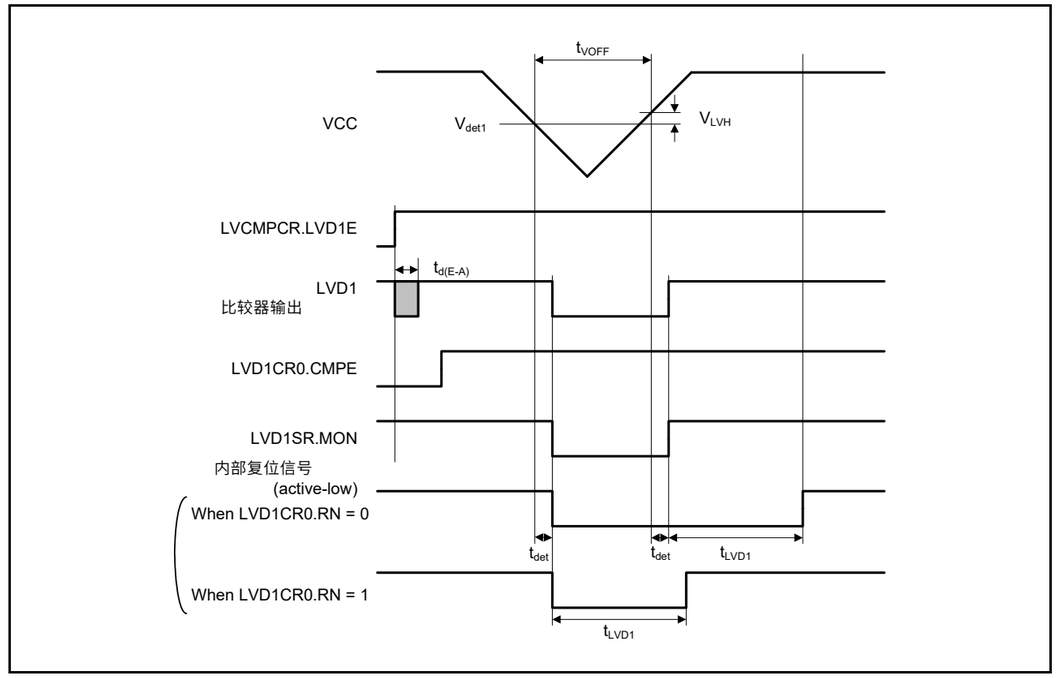


Figure 48.71 电压检测电路时序（Vdet1）

48.10 VBATT Characteristics

Table 48.54 Battery backup function characteristics
Conditions: VCC = AVCC0 = 1.8V to 3.6V, VBATT = 1.6 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup (falling)		$V_{DETBATT}$	1.99	2.09	2.19	V	Figure 48.72, Figure 48.73
Hysteresis width for switching to battery back up		V_{VBATTH}	-	100	-	mV	
VCC-off period for starting power supply switching		$t_{VOFFBATT}$	300	-	-	µs	-
Voltage detection level VBATT_Power-on reset (VBATT_POR)		$V_{VBATPOR}$	1.30	1.40	1.50	V	Figure 48.72, Figure 48.73
Wait time after VBATT_POR reset time cancellation		$t_{VBATPOR}$	-	-	3	mS	-
Level for detection of voltage drop on the VBATT pin (falling)	VBTLVDLVL[1:0] = 10b	$V_{DETBATLVD}$	2.11	2.2	2.29	V	Figure 48.74
	VBTLVDLVL[1:0] = 11b		1.92	2	2.08	V	
Hysteresis width for VBATT pin LVD		$V_{VBATLVDTH}$	-	50	-	mV	
VBATT pin LVD operation stabilization time		t_{d_vbat}	-	-	300	µs	Figure 48.74
VBATT pin LVD response delay time		t_{det_vbat}	-	-	350	µs	
Allowable voltage change rising/falling gradient		dt/dVCC	1.0	-	-	ms/V	-
VCC voltage level for access to the VBATT backup registers		$V_{\_BKBATT}$	1.8	-	-	V	-

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

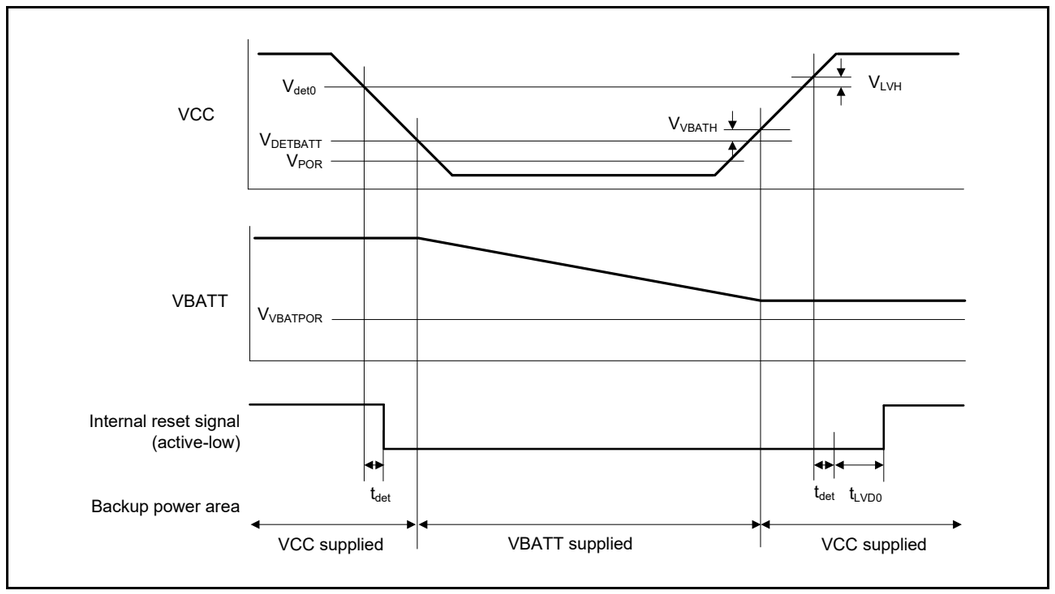


Figure 48.72 Power supply switching and LVD0 reset timing

48.10 VBATT Characteristics

Table 48.54 电池备份功能特点
Conditions: VCC = AVCC0 = 1.8V to 3.6V, VBATT = 1.6 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
切换到备用电池的电压电平（下降）		$V_{DETBATT}$	1.99	2.09	2.19	V	Figure 48.72, Figure 48.73
切换到备用电池的滞后宽度		V_{VBATTH}	-	100	-	mV	
启动电源切换的VCC-off周期		$t_{VOFFBATT}$	300	-	-	µs	-
电压检测电平 VBATT_Power-on reset (VBATT_POR)		$V_{VBATPOR}$	1.30	1.40	1.50	V	Figure 48.72, Figure 48.73
VBATT_POR复位时间取消后的等待时间		$t_{VBATPOR}$	-	-	3	mS	-
VBATT引脚电压降检测电平（下降）	VBTLVDLVL[1:0] = 10b	$V_{DETBATLVD}$	2.11	2.2	2.29	V	Figure 48.74
	VBTLVDLVL[1:0] = 11b		1.92	2	2.08	V	
VBATT引脚LVD的迟滞宽度		$V_{VBATLVDTH}$	-	50	-	mV	
VBATT引脚LVD操作稳定时间		t_{d_vbat}	-	-	300	µs	Figure 48.74
VBATT引脚LVD响应延迟时间		t_{det_vbat}	-	-	350	µs	
允许电压变化上升下降梯度		dt/dVCC	1.0	-	-	ms/V	-
用于访问VBATT备份寄存器的VCC电压电平		$V_{\_BKBATT}$	1.8	-	-	V	-

Note: 开始电源切换的VCC-off周期表示VCC低于切换到备用电池的电压电平最小值(VDETBATT)的周期。

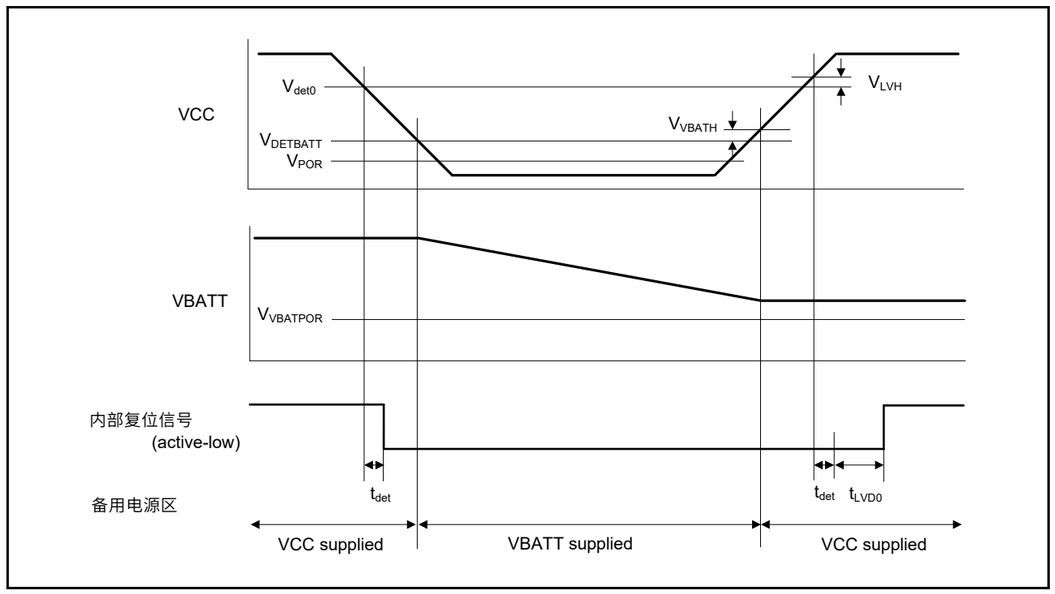


Figure 48.72 电源切换和LVD0复位时序

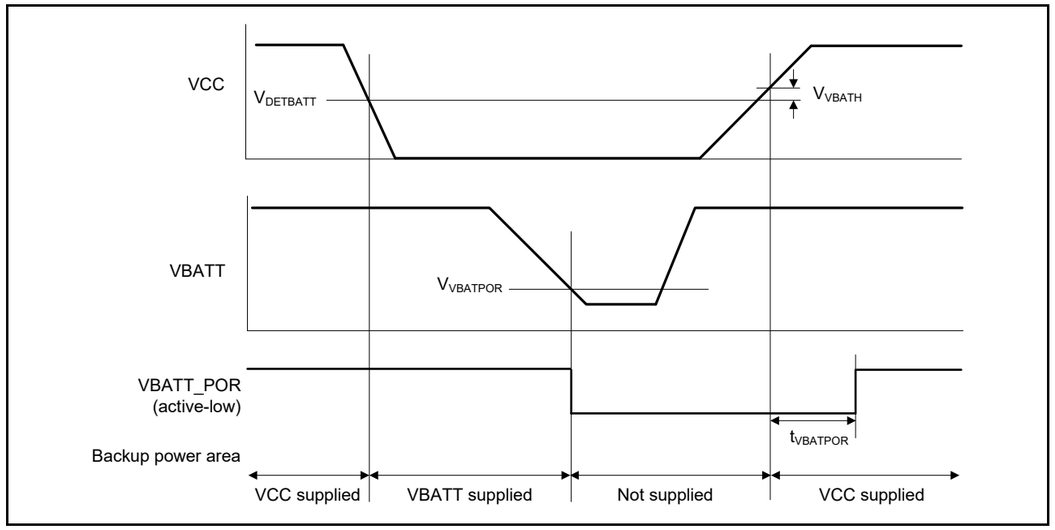


Figure 48.73 VBATT_POR reset timing

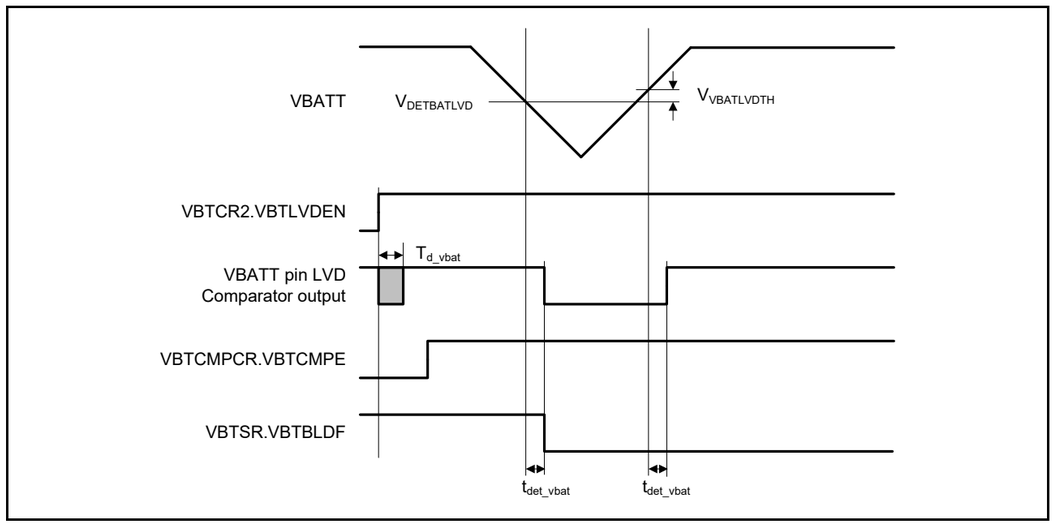


Figure 48.74 VBATT pin voltage detection circuit timing

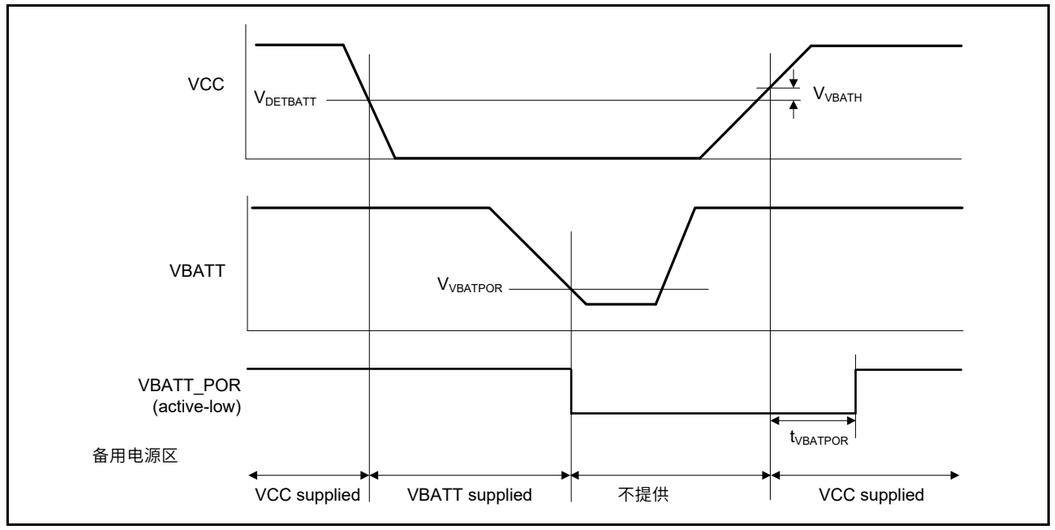


Figure 48.73 VBATT_POR复位时序

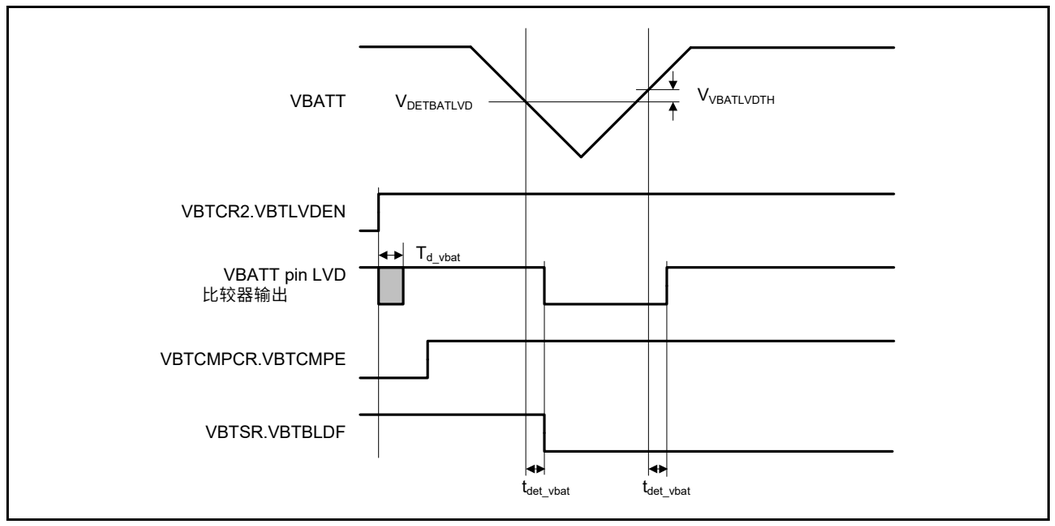


Figure 48.74 VBATT引脚电压检测电路时序

Table 48.55 VBATT-I/O characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
VBATWIOn I/O output characteristics (n = 0)	VCC > $V_{DETBATT}$	VCC = 2.7 to 3.6 V	V_{OH}	VCC - 0.5	-	-		I_{OH} = -100 µA
			V_{OL}	-	-	0.5		I_{OL} = 100 µA
		VCC = $V_{DETBATT}$ to 2.7 V	V_{OH}	VCC - 0.3	-	-		I_{OH} = -50 µA
			V_{OL}	-	-	0.3		I_{OL} = 50 µA
	VCC < $V_{DETBATT}$	VBATT = 2.7 to 3.6 V	V_{OH}	V_{BATT} - 0.5	-	-		I_{OH} = -100 µA
			V_{OL}	-	-	0.5		I_{OL} = 100 µA
		VBATT = 1.8 to 2.7 V	V_{OH}	V_{BATT} - 0.3	-	-		I_{OH} = -50 µA
			V_{OL}	-	-	0.3		I_{OL} = 50 µA

48.11 CTSU Characteristics

Table 48.56 CTSU characteristics
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

Table 48.55 VBATT-I/O characteristics

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
VBATWIOnIO 输出特性(n=0)	VCC > $V_{DETBATT}$	VCC = 2.7 to 3.6 V	V_{OH}	VCC - 0.5	-	-		I_{OH} = -100 µA
			V_{OL}	-	-	0.5		I_{OL} = 100 µA
		VCC = $V_{DETBATT}$ to 2.7 V	V_{OH}	VCC - 0.3	-	-		I_{OH} = -50 µA
			V_{OL}	-	-	0.3		I_{OL} = 50 µA
	VCC < $V_{DETBATT}$	VBATT = 2.7 to 3.6 V	V_{OH}	V_{BATT} - 0.5	-	-		I_{OH} = -100 µA
			V_{OL}	-	-	0.5		I_{OL} = 100 µA
		VBATT = 1.8 to 2.7 V	V_{OH}	V_{BATT} - 0.3	-	-		I_{OH} = -50 µA
			V_{OL}	-	-	0.3		I_{OL} = 50 µA

48.11 CTSU Characteristics

Table 48.56 CTSU characteristics
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C_{tscap}	9	10	11	nF	-
TS引脚容性负载	C_{base}	-	-	50	pF	-
允许输出大电流	ΣIoH	-	-	-24	mA	应用互电容法时

48.12 Segment LCD Controller Characteristics

48.12.1 Resistance Division Method

[Static Display Mode]

Table 48.57 Resistance division method LCD characteristics (1)
Conditions: VL4 ≤ VCC ≤ 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	-	VCC	V	-

[1/2 Bias Method, 1/4 Bias Method]

Table 48.58 Resistance division method LCD characteristics (2)
Conditions: VL4 ≤ VCC ≤ 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 48.59 Resistance division method LCD characteristics (3)
Conditions: VL4 ≤ VCC ≤ 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	-	VCC	V	-

48.13 Comparator Characteristics

Table 48.60 ACMPLP characteristics
Conditions: VCC = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	Standard mode	IVREFn (n=0,1)	VREF	0	-	VCC–1.4	V	-
	Window mode*2	IVREF1	VREFH	1.4	-	VCC	V	-
		IVREF0	VREFL	0	-	VCC–1.4	V	-
Input voltage range			VI	0	-	VCC	V	-
Internal reference voltage			-	1.36	1.44	1.50	V	-
Output delay	High-speed mode		Td	-	-	1.2	µs	VCC = 3.0 Slew rate of input signal > 50 mV/µs
	Low-speed mode			-	-	5	µs	
	Window mode			-	-	2	µs	
Offset voltage*1	High-speed mode		-	-	-	50	mV	-
	Low-speed mode		-	-	-	40	mV	-
	Window mode		-	-	-	60	mV	-
Operation stabilization wait time			T_{cmp}	100	-	-	µs	-

Note 1. When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.
Note 2. In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

48.12 段式LCD控制器特性

48.12.1 电阻分割法

[Static Display Mode]

Table 48.57 电阻分法LCD特性（一）
Conditions: VL4 ≤ VCC ≤ 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
液晶驱动电压	V_{L4}	2.0	-	VCC	V	-

[12偏置法，14偏置法]

Table 48.58 电阻分法LCD特性（二）
Conditions: VL4 ≤ VCC ≤ 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
液晶驱动电压	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 48.59 电阻分法LCD特性（三）
Conditions: VL4 ≤ VCC ≤ 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
液晶驱动电压	V_{L4}	2.5	-	VCC	V	-

48.13 比较器特性

Table 48.60 ACMPLP characteristics
Conditions: VCC = 1.8 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
参考电压范围	标准模式	IVREFn (n=0,1)	VREF	0	-	VCC–1.4	V	-
	Window mode*2	IVREF1	VREFH	1.4	-	VCC	V	-
		IVREF0	VREFL	0	-	VCC–1.4	V	-
输入电压范围			VI	0	-	VCC	V	-
内部参考电压			-	1.36	1.44	1.50	V	-
输出延迟	High-speed mode		Td	-	-	1.2	µs	VCC = 3.0 输入信号的压摆率>50mVµs
	Low-speed mode			-	-	5	µs	
	窗口模式			-	-	2	µs	
Offset voltage*1	High-speed mode		-	-	-	50	mV	-
	Low-speed mode		-	-	-	40	mV	-
	窗口模式		-	-	-	60	mV	-
运行稳定等待时间			T_{cmp}	100	-	-	µs	-

注1.当8位DAC输出用作参考电压时，失调电压会增加到2.5xVCC256。
注2.在窗口模式下，请务必满足以下条件：IVREF1IVREF0>0.2V。

48.14 OPAMP Characteristics

Table 48.61 OPAMP characteristics
Conditions: VCC = AVCC0 = 1.8 to 3.6 V (AVCC0 = VCC when VCC < 2.0 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Common mode input range	Vicm1	Low-power mode		0.2	-	AVCC0 – 0.5	V
	Vicm2	High-speed mode		0.3	-	AVCC0 – 0.6	V
Output voltage range	Vo1	Low-power mode		0.1	-	AVCC0 – 0.1	V
	Vo2	High-speed mode		0.1	-	AVCC0 – 0.1	V
Input offset voltage	Vioff	3σ		–10	-	10	mV
Open gain	Av			60	120	-	dB
Gain-bandwidth (GB) product	GBW1	Low-power mode		-	0.04	-	MHz
	GBW2	High-speed mode		-	1.7	-	MHz
Phase margin	PM	CL = 20 pF		50	-	-	deg
Gain margin	GM	CL = 20 pF		10	-	-	dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power mode	-	230	-	nV/√Hz
	Vnoise2	f = 10 kHz		-	200	-	nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode	-	90	-	nV/√Hz
	Vnoise4	f = 2 kHz		-	70	-	nV/√Hz
Power supply reduction ratio	PSRR			-	90	-	dB
Common mode signal reduction ratio	CMRR			-	90	-	dB
Stabilization wait time	Tstd1	CL = 20 pF Only operational amplifier is activated *1	Low-power mode	650	-	-	µs
	Tstd2		High-speed mode	13	-	-	µs
	Tstd3	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously	Low-power mode	650	-	-	µs
	Tstd4		High-speed mode	13	-	-	µs
Settling time	Tset1	CL = 20 pF	Low-power mode	-	-	750	µs
	Tset2		High-speed mode	-	-	13	µs
Slew rate	Tslew1	CL = 20 pF	Low-power mode	-	0.02	-	V/µs
	Tslew2		High-speed mode	-	1.1	-	V/µs
Load current	Iload1	Low power mode		–100	-	100	µA
	Iload2	High-speed mode		–100	-	100	µA
Load capacitance	CL			-	-	20	pF

Note 1. When the operational amplifier reference current circuit is activated in advance.

48.14 OPAMP Characteristics

Table 48.61 OPAMP characteristics
条件：VCC=AVCC0=1.8至3.6V（当VCC<2.0V时，AVCC0=VCC）

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
共模输入范围	Vicm1	Low-power mode		0.2	-	AVCC0 – 0.5	V
	Vicm2	High-speed mode		0.3	-	AVCC0 – 0.6	V
输出电压范围	Vo1	Low-power mode		0.1	-	AVCC0 – 0.1	V
	Vo2	High-speed mode		0.1	-	AVCC0 – 0.1	V
输入失调电压	Vioff	3σ		–10	-	10	mV
打开增益	Av			60	120	-	dB
Gain-bandwidth (GB) product	GBW1	Low-power mode		-	0.04	-	MHz
	GBW2	High-speed mode		-	1.7	-	MHz
相位裕度	PM	CL = 20 pF		50	-	-	deg
获得利润	GM	CL = 20 pF		10	-	-	dB
等效输入噪声	Vnoise1	f = 1 kHz	Low-power mode	-	230	-	nV/√Hz
	Vnoise2	f = 10 kHz		-	200	-	nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode	-	90	-	nV/√Hz
	Vnoise4	f = 2 kHz		-	70	-	nV/√Hz
电源减速比	PSRR			-	90	-	dB
共模信号衰减比	CMRR			-	90	-	dB
稳定等待时间	Tstd1	CL=20pF仅激活运算放大器*1	Low-power mode	650	-	-	µs
	Tstd2		High-speed mode	13	-	-	µs
	Tstd3	CL = 20 pF 运算放大器和参考电流电路同时启动	Low-power mode	650	-	-	µs
	Tstd4		High-speed mode	13	-	-	µs
稳定时间	Tset1	CL = 20 pF	Low-power mode	-	-	750	µs
	Tset2		High-speed mode	-	-	13	µs
转换率	Tslew1	CL = 20 pF	Low-power mode	-	0.02	-	V/µs
	Tslew2		High-speed mode	-	1.1	-	V/µs
负载电流	Iload1	低功耗模式		–100	-	100	µA
	Iload2	High-speed mode		–100	-	100	µA
负载电容	CL			-	-	20	pF

Note 1. 当运算放大器参考电流电路被预先激活时。

48.15 Flash Memory Characteristics

48.15.1 Code Flash Memory Characteristics

Table 48.62 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be done n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 48.63 Code flash characteristics (2)
High-speed operating mode
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	-	116	998	-	54	506	µs
Erasure time	2-KB	t_{E2K}	-	9.03	287	-	5.67	222	ms
Blank check time	8-byte	t_{BC8}	-	-	56.8	-	-	16.6	µs
	2-KB	t_{BC2K}	-	-	1899	-	-	140	µs
Erase suspended time		t_{SED}	-	-	22.5	-	-	10.7	µs
Startup area switching setting time		t_{SAS}	-	21.7	585	-	12.1	447	ms
Access window time		t_{AWS}	-	21.7	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	21.7	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	5	-	-	5	-	-	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

48.15 闪存特性

48.15.1 代码闪存特性

Table 48.62 码闪特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
数据保持时间	NPEC1000次后	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=1 000）时，可以对每个块进行n次擦除。例如，当对2KB块中的不同地址执行256次8字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除（禁止覆盖）。

Note 2. 使用瑞萨电子提供的闪存编程器和自编程库时的特性。
Note 3. 这个结果是从可靠性测试中获得的。

Table 48.63 码闪特性（二）
高速运行模式
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	8-byte	t_{P8}	-	116	998	-	54	506	µs
擦除时间	2-KB	t_{E2K}	-	9.03	287	-	5.67	222	ms
空白检查时间	8-byte	t_{BC8}	-	-	56.8	-	-	16.6	µs
	2-KB	t_{BC2K}	-	-	1899	-	-	140	µs
擦除暂停时间		t_{SED}	-	-	22.5	-	-	10.7	µs
启动区切换设置时间		t_{SAS}	-	21.7	585	-	12.1	447	ms
访问窗口时间		t_{AWS}	-	21.7	585	-	12.1	447	ms
OCD串口编程器ID设置时间		t_{OSIS}	-	21.7	585	-	12.1	447	ms
闪存模式转换等待时间1		t_{DIS}	2	-	-	2	-	-	µs
闪存模式转换等待时间2		t_{MS}	5	-	-	5	-	-	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

Table 48.64 Code flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = 1.8 to 3.6 V, Ta = –40 to +85°C

Parameter		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	-	157	1411	-	101	966	µs
Erasure time	2-KB	t_{E2K}	-	9.10	289	-	6.10	228	ms
Blank check time	8-byte	t_{BC8}	-	-	87.7	-	-	52.5	µs
	2-KB	t_{BC2K}	-	-	1930	-	-	414	µs
Erase suspended time		t_{SED}	-	-	32.7	-	-	21.6	µs
Startup area switching setting time		t_{SAS}	-	22.5	592	-	14.0	464	ms
Access window time		t_{AWS}	-	22.5	592	-	14.0	464	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	22.5	592	-	14.0	464	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

48.15.2 Data Flash Memory Characteristics

Table 48.65 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	-	Times	-
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	-	-	Year	
	After 1000000 times of N_{DPEC}		-	1*2, *3	-	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited).
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 48.66 Data flash characteristics (2)
High-speed operating mode
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	52.4	463	-	42.1	387	µs
Erasure time	1-KB	t_{DE1K}	-	8.98	286	-	6.42	237	ms
Blank check time	1-byte	t_{DBC1}	-	-	24.3	-	-	16.6	µs
	1-KB	t_{DBC1K}	-	-	1872	-	-	512	µs
Suspended time during erasing		t_{DSED}	-	-	13.0	-	-	10.7	µs
Data flash STOP recovery time		t_{DSTOP}	5	-	-	5	-	-	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

Table 48.64 码闪特性（三）
中速运行模式
条件：VCC=1.8至3.6V，Ta= 40至+85°C

Parameter		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	8-byte	t_{P8}	-	157	1411	-	101	966	µs
擦除时间	2-KB	t_{E2K}	-	9.10	289	-	6.10	228	ms
空白检查时间	8-byte	t_{BC8}	-	-	87.7	-	-	52.5	µs
	2-KB	t_{BC2K}	-	-	1930	-	-	414	µs
擦除暂停时间		t_{SED}	-	-	32.7	-	-	21.6	µs
启动区切换设置时间		t_{SAS}	-	22.5	592	-	14.0	464	ms
访问窗口时间		t_{AWS}	-	22.5	592	-	14.0	464	ms
OCD串口编程器ID设置时间		t_{OSIS}	-	22.5	592	-	14.0	464	ms
闪存模式转换等待时间1		t_{DIS}	2	-	-	2	-	-	µs
闪存模式转换等待时间2		t_{MS}	720	-	-	720	-	-	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

48.15.2 数据闪存特性

Table 48.65 数据闪存特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	-	Times	-
数据保持时间	NDPEC10000次后	t_{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	NDPEC100000次后		5*2, *3	-	-	Year	
	NDPEC1000000次后		-	1*2, *3	-	Year	Ta = +25°C

Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=100 000）时，可以对每个块执行n次擦除。例如，当对1字节块中的不同地址执行1 000次1字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止覆盖）。
Note 2. 使用瑞萨电子提供的闪存编程器和自编程库时的特性。
Note 3. 这些结果来自可靠性测试。

Table 48.66 数据闪存特性（2）
高速运行模式
Conditions: VCC = 2.7 to 3.6 V

Parameter		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	-	52.4	463	-	42.1	387	µs
擦除时间	1-KB	t_{DE1K}	-	8.98	286	-	6.42	237	ms
空白检查时间	1-byte	t_{DBC1}	-	-	24.3	-	-	16.6	µs
	1-KB	t_{DBC1K}	-	-	1872	-	-	512	µs
擦除期间的暂停时间		t_{DSED}	-	-	13.0	-	-	10.7	µs
数据闪停恢复时间		t_{DSTOP}	5	-	-	5	-	-	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

Table 48.67 Data flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = 1.8 to 3.6 V, Ta = –40 to +85°C

Parameter		Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	94.7	886	-	89.3	849	µs
Erasure time	1-KB	t_{DE1K}	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t_{DBC1}	-	-	56.2	-	-	52.5	µs
	1-KB	t_{DBC1K}	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t_{DSED}	-	-	23.0	-	-	21.7	µs
Data flash STOP recovery time		t_{DSTOP}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

48.16 Joint Test Action Group (JTAG)

Table 48.68 JTAG (debug) characteristics (1)
Conditions: VCC = 2.4 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	80	-	-	ns	Figure 48.75
TCK clock high pulse width	t_{TCKH}	35	-	-	ns	
TCK clock low pulse width	t_{TCKL}	35	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	16	-	-	ns	Figure 48.76
TMS hold time	t_{TMSH}	16	-	-	ns	
TDI setup time	t_{TDIS}	16	-	-	ns	
TDI hold time	t_{TDIH}	16	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	70	ns	

Table 48.69 JTAG (debug) characteristics (2)
Conditions: VCC = 1.8 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	250	-	-	ns	Figure 48.75
TCK clock high pulse width	t_{TCKH}	120	-	-	ns	
TCK clock low pulse width	t_{TCKL}	120	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	50	-	-	ns	Figure 48.76
TMS hold time	t_{TMSH}	50	-	-	ns	
TDI setup time	t_{TDIS}	50	-	-	ns	
TDI hold time	t_{TDIH}	50	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	150	ns	

Table 48.67 数据闪存特性（3）
中速运行模式
条件：VCC=1.8至3.6V，Ta= 40至+85°C

Parameter		Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	-	94.7	886	-	89.3	849	µs
擦除时间	1-KB	t_{DE1K}	-	9.59	299	-	8.29	273	ms
空白检查时间	1-byte	t_{DBC1}	-	-	56.2	-	-	52.5	µs
	1-KB	t_{DBC1K}	-	-	2.17	-	-	1.51	ms
擦除期间的暂停时间		t_{DSED}	-	-	23.0	-	-	21.7	µs
数据闪停恢复时间		t_{DSTOP}	720	-	-	720	-	-	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

48.16 联合测试行动组(JTAG)

Table 48.68 JTAG (debug) characteristics (1)
Conditions: VCC = 2.4 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	80	-	-	ns	Figure 48.75
TCK时钟高脉冲宽度	t_{TCKH}	35	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	35	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	
TMS设置时间	t_{TMSS}	16	-	-	ns	Figure 48.76
TMS保持时间	t_{TMSH}	16	-	-	ns	
TDI建立时间	t_{TDIS}	16	-	-	ns	
TDI保持时间	t_{TDIH}	16	-	-	ns	
TDO数据延迟时间	t_{TDOD}	-	-	70	ns	

Table 48.69 JTAG (debug) characteristics (2)
Conditions: VCC = 1.8 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	250	-	-	ns	Figure 48.75
TCK时钟高脉冲宽度	t_{TCKH}	120	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	120	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	
TMS设置时间	t_{TMSS}	50	-	-	ns	Figure 48.76
TMS保持时间	t_{TMSH}	50	-	-	ns	
TDI建立时间	t_{TDIS}	50	-	-	ns	
TDI保持时间	t_{TDIH}	50	-	-	ns	
TDO数据延迟时间	t_{TDOD}	-	-	150	ns	

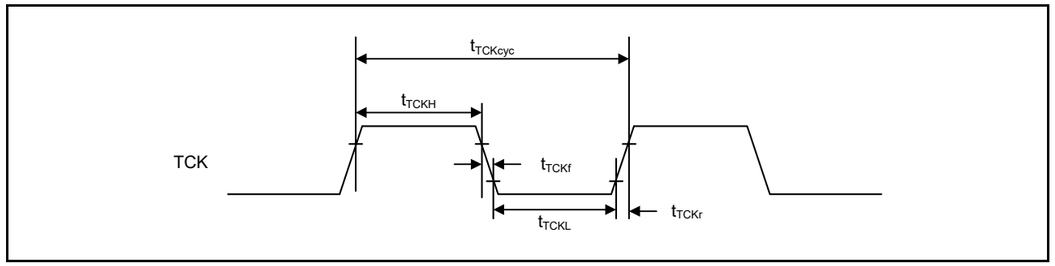


Figure 48.75 JTAG TCK timing

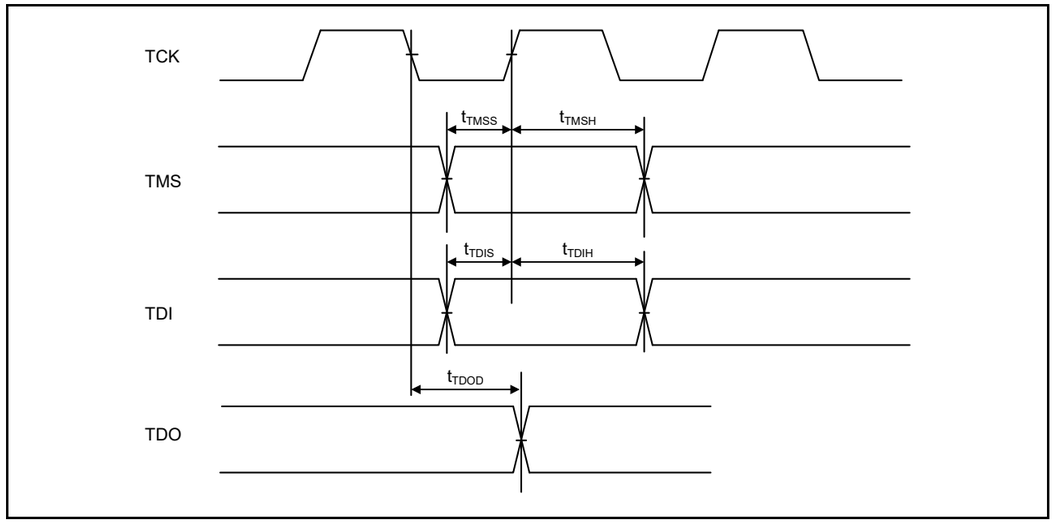


Figure 48.76 JTAG input/output timing

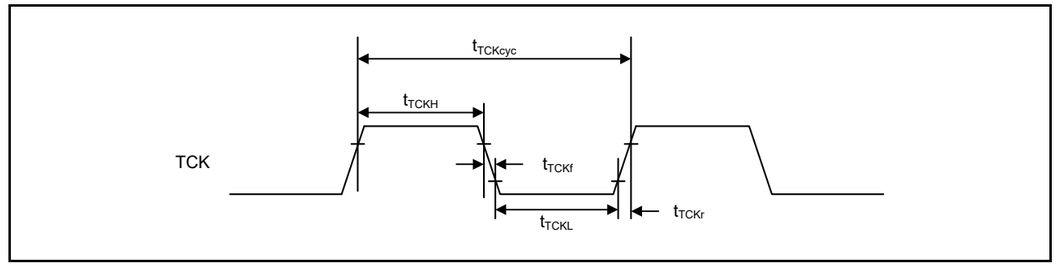


Figure 48.75 JTAG TCK timing

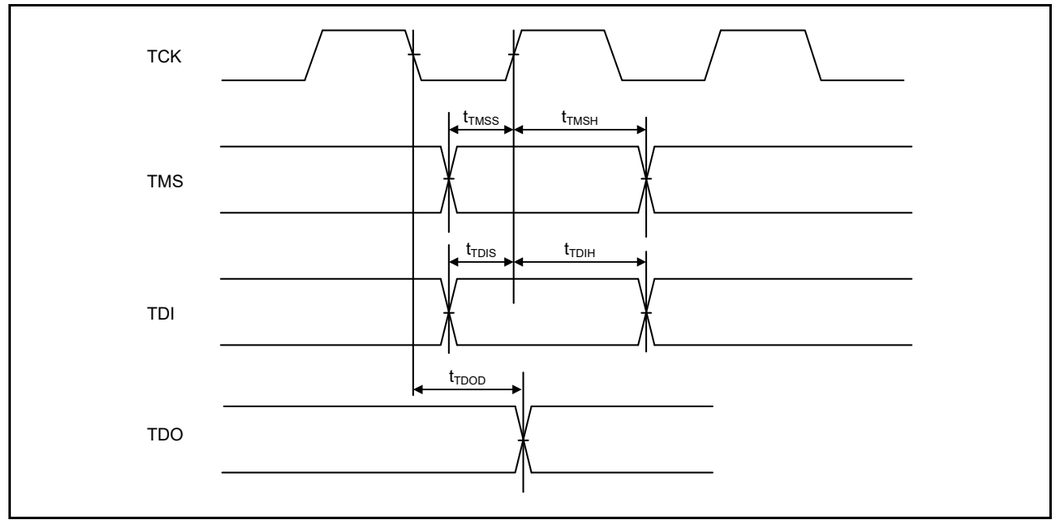


Figure 48.76 JTAG input/output timing

48.16.1 Serial Wire Debug (SWD)

Table 48.70 SWD characteristics (1)
Conditions: VCC = 2.4 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	-	-	ns	Figure 48.77
SWCLK clock high pulse width	t_{SWCKH}	35	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	16	-	-	ns	Figure 48.78
SWDIO hold time	t_{SWDH}	16	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	70	ns	

Table 48.71 SWD characteristics (2)
Conditions: VCC = 1.8 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	-	-	ns	Figure 48.77
SWCLK clock high pulse width	t_{SWCKH}	120	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	50	-	-	ns	Figure 48.78
SWDIO hold time	t_{SWDH}	50	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	150	ns	

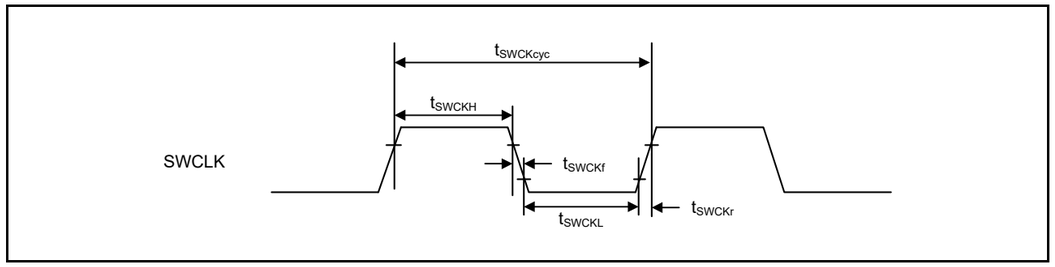


Figure 48.77 SWD SWCLK timing

48.16.1 串行线调试(SWD)

Table 48.70 SWD characteristics (1)
Conditions: VCC = 2.4 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	80	-	-	ns	Figure 48.77
SWCLK时钟高脉冲宽度	t_{SWCKH}	35	-	-	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	35	-	-	ns	
SWCLK时钟上升时间	t_{SWCKr}	-	-	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	-	-	5	ns	
SWDIO设置时间	t_{SWDS}	16	-	-	ns	Figure 48.78
SWDIO保持时间	t_{SWDH}	16	-	-	ns	
SWDIO数据延迟时间	t_{SWDD}	2	-	70	ns	

Table 48.71 SWD characteristics (2)
Conditions: VCC = 1.8 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	250	-	-	ns	Figure 48.77
SWCLK时钟高脉冲宽度	t_{SWCKH}	120	-	-	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	120	-	-	ns	
SWCLK时钟上升时间	t_{SWCKr}	-	-	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	-	-	5	ns	
SWDIO设置时间	t_{SWDS}	50	-	-	ns	Figure 48.78
SWDIO保持时间	t_{SWDH}	50	-	-	ns	
SWDIO数据延迟时间	t_{SWDD}	2	-	150	ns	

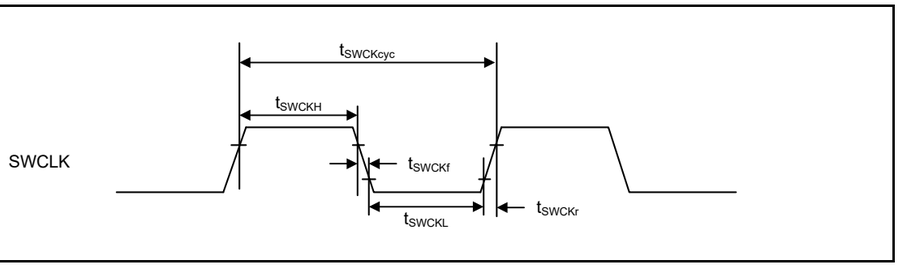


Figure 48.77 SWD SWCLK timing

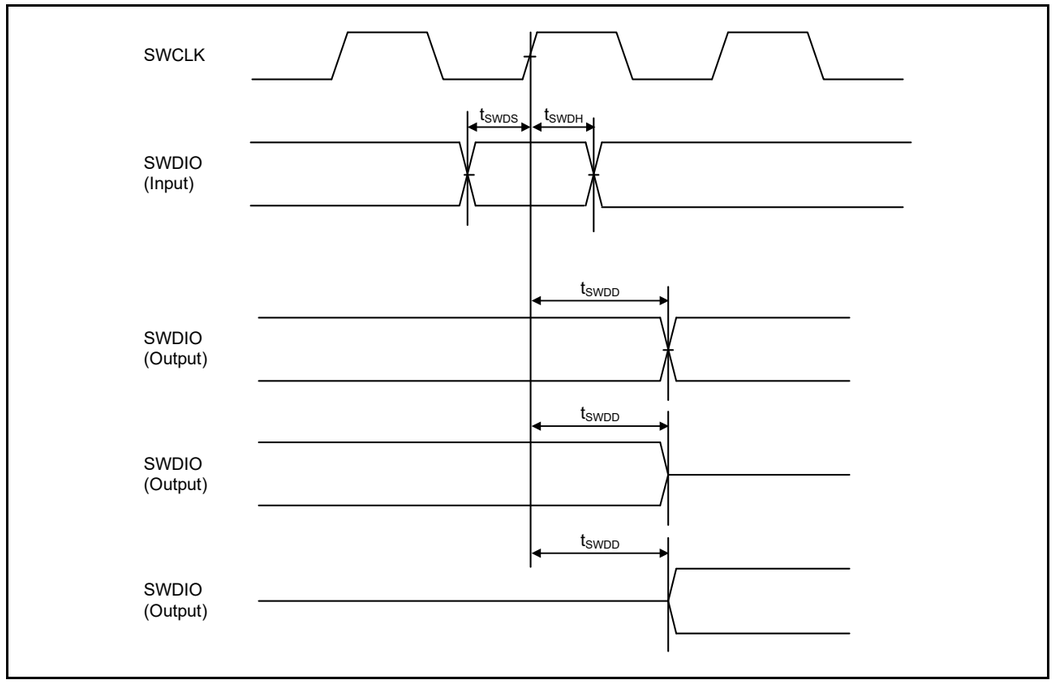


Figure 48.78 SWD input/output timing

48.17 BLE Characteristics

48.17.1 Transmission Characteristics

Table 48.72 Transmission Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Range of frequency	RF_{CF}	2402	-	2480	MHz	
Data rate	RF_{DATA_2M}	-	2	-	Mbps	
	RF_{DATA_1M}	-	1	-	Mbps	
	RF_{DATA_500k}	-	500	-	kbps	
	RF_{DATA_125k}	-	125	-	kbps	
Maximum transmitted output power	RF_{POWER}	-	0	2	dBm	0 dBm output mode
		-	4	6	dBm	4 dBm output mode
Output frequency error	RF_{TXFERR}	–10	-	10	ppm	*1

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. This does not take frequency errors due to manufacturing irregularities, drift with temperature, or deterioration of the crystal over time into account.

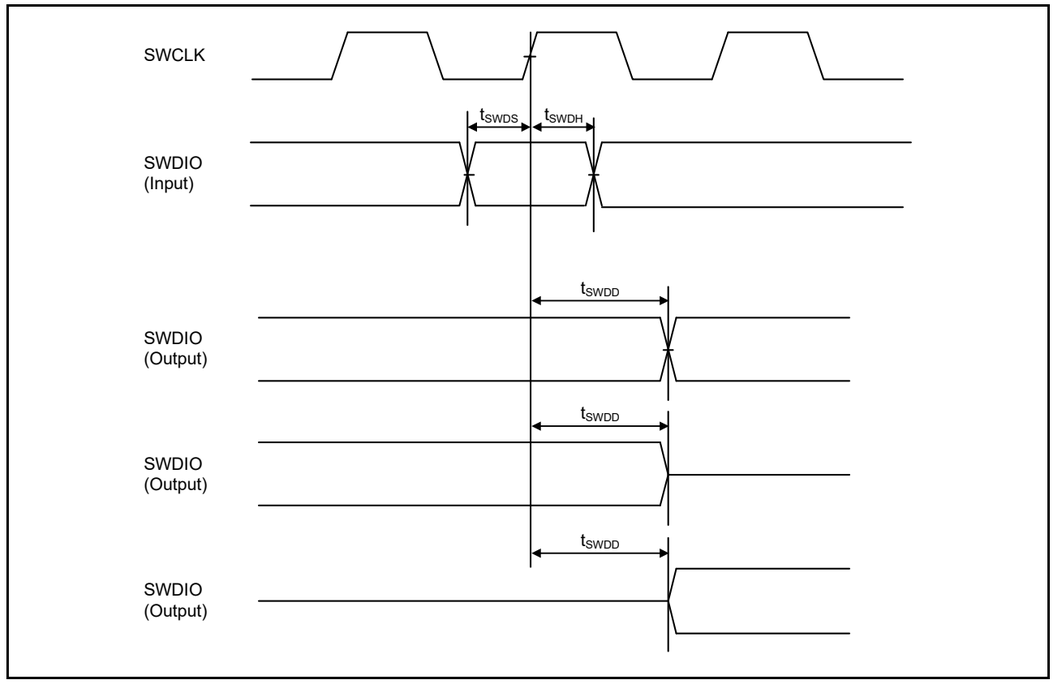


Figure 48.78 SWD input/output timing

48.17 低功耗蓝牙特性

48.17.1 传输特性

Table 48.72 传输特性

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
频率范围	RF_{CF}	2402	-	2480	MHz	
数据速率	RF_{DATA_2M}	-	2	-	Mbps	
	RF_{DATA_1M}	-	1	-	Mbps	
	RF_{DATA_500k}	-	500	-	kbps	
	RF_{DATA_125k}	-	125	-	kbps	
最大发射输出功率	RF_{POWER}	-	0	2	dBm	0dBm输出模式
		-	4	6	dBm	4dBm输出模式
输出频率误差	RF_{TXFERR}	–10	-	10	ppm	*1

Note: 这些特性基于未使用的BLE接口以外的引脚和功能。
Note 1. 这没有考虑由于制造不规则性、温度漂移或晶体随时间劣化引起的频率误差。

48.17.2 Reception Characteristics (2 Mbps)

Table 48.73 Reception Characteristics
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_2M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_2M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_2M}	—	–92	—	dBm	*1	
Secondary emission strength	RF_{RXSP_2M}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_2M}	—	–8	—	dB	Prf = –67 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_2M}	—	2	—	dB	Prf = –67 dBm*1	±2 MHz
		—	35	—	dB		±4 MHz
		—	39	—	dB		±6 MHz
Blocking	RF_{BLK_2M}	—	–1	—	dBm	Prf = –67 dBm*1	30 MHz to 2000 MHz
		—	–25	—	dBm		2000 MHz to 2399 MHz
		—	–21	—	dBm		2484 MHz to 3000 MHz
		—	–10	—	dBm		> 3000 MHz
Allowable frequency deviation*2	RF_{RXFER_2M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_2M}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

48.17.3 Reception Characteristics (1 Mbps)

Table 48.74 Reception Characteristics
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_1M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_1M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_1M}	—	–95	—	dBm	*1	
Secondary emission strength	RF_{RXSP_1M}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF_{CCR_1M}	—	–7	—	dB	Prf = –67dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_1M}	—	–1	—	dB	Prf = –67dBm*1	±1MHz
		—	34	—	dB		±2MHz
		—	35	—	dB		±3MHz
Blocking	RF_{BLK_1M}	—	0	—	dBm	Prf = –67dBm*1	30MHz to 2000MHz
		—	–24	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–4	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_1M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_1M}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

48.17.2 接收特性(2Mbps)

Table 48.73 接收特性
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	测试条件	
输入频率	RF_{RXFIN_2M}	2402	—	2480	MHz		
最大输入电平	RF_{LEVL_2M}	–10	4	—	dBm	*1	
接收灵敏度	RF_{STY_2M}	—	–92	—	dBm	*1	
二次发射强度RFRXSP_2M		—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
同频抑制比	RF_{CCR_2M}	—	–8	—	dB	Prf = –67 dBm*1	
邻道抑制比	RF_{ADCR_2M}	—	2	—	dB	Prf = –67 dBm*1	±2 MHz
		—	35	—	dB		±4 MHz
		—	39	—	dB		±6 MHz
Blocking	RF_{BLK_2M}	—	–1	—	dBm	Prf = –67 dBm*1	30 MHz to 2000 MHz
		—	–25	—	dBm		2000 MHz to 2399 MHz
		—	–21	—	dBm		2484 MHz to 3000 MHz
		—	–10	—	dBm		> 3000 MHz
允许频率偏差*2	RF_{RXFER_2M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_2M}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: 这些特性基于未使用的BLE接口以外的引脚和功能。
Note 1. PER≤30.8%，有效载荷为37字节
Note 2. RF输入信号的中心频率与芯片内部产生的载波频率之间的允许差值范围

48.17.3 接收特性(1Mbps)

Table 48.74 接收特性
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	测试条件	
输入频率	RF_{RXFIN_1M}	2402	—	2480	MHz		
最大输入电平	RF_{LEVL_1M}	–10	4	—	dBm	*1	
接收灵敏度	RF_{STY_1M}	—	–95	—	dBm	*1	
二次发射强度	RF_{RXSP_1M}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
同频抑制比	RF_{CCR_1M}	—	–7	—	dB	Prf = –67dBm*1	
邻道抑制比	RF_{ADCR_1M}	—	–1	—	dB	Prf = –67dBm*1	±1MHz
		—	34	—	dB		±2MHz
		—	35	—	dB		±3MHz
Blocking	RF_{BLK_1M}	—	0	—	dBm	Prf = –67dBm*1	30MHz to 2000MHz
		—	–24	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–4	—	dBm		> 3000MHz
允许频率偏差*2	RF_{RXFER_1M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_1M}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: 这些特性基于未使用的BLE接口以外的引脚和功能。
Note 1. PER≤30.8%，有效载荷为37字节
Note 2. RF输入信号的中心频率与芯片内部产生的载波频率之间的允许差值范围

48.17.4 Reception Characteristics (500 kbps)

Table 48.75 Reception Characteristics
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_500k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_500k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_500k}	—	–100	—	dBm	*1	
Secondary emission strength	RF_{RXSP_500k}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF_{CCR_500k}	—	–4	—	dB	Prf = –72dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_500k}	—	6	—	dB	Prf = –72dBm*1	±1MHz
		—	36	—	dB		±2MHz
		—	42	—	dB		±3MHz
Blocking	RF_{BLK_500k}	—	0	—	dBm	Prf = –72dBm*1	30MHz to 2000MHz
		—	–23	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–7	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_500k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_500k}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

48.17.5 Reception Characteristics (125 kbps)

Table 48.76 Reception Characteristics
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_125k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_125k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_125k}	—	–105	—	dBm	*1	
Secondary emission strength	RF_{RXSP_125k}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_125k}	—	–2	—	dB	Prf = –79 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_125k}	—	12	—	dB	Prf = –79 dBm*1	±1 MHz
		—	39	—	dB		±2 MHz
		—	45	—	dB		±3 MHz
Blocking	RF_{BLK_125k}	—	0	—	dBm	Prf = –79 dBm*1	30 MHz to 2000 MHz
		—	–23	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–1	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_125k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_125k}	—	±4	—	dB	T_a = +25°C, –70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

48.17.4 接收特性(500kbps)

Table 48.75 接收特性
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	测试条件	
输入频率	RF_{RXFIN_500k}	2402	—	2480	MHz		
最大输入电平	RF_{LEVL_500k}	–10	4	—	dBm	*1	
接收灵敏度	RF_{STY_500k}	—	–100	—	dBm	*1	
二次发射强度	RF_{RXSP_500k}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
同频抑制比	RF_{CCR_500k}	—	–4	—	dB	Prf = –72dBm*1	
邻道抑制比	RF_{ADCR_500k}	—	6	—	dB	Prf = –72dBm*1	±1MHz
		—	36	—	dB		±2MHz
		—	42	—	dB		±3MHz
Blocking	RF_{BLK_500k}	—	0	—	dBm	Prf = –72dBm*1	30MHz to 2000MHz
		—	–23	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–7	—	dBm		> 3000MHz
允许频率偏差*2	RF_{RXFER_500k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_500k}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: 这些特性基于未使用的BLE接口以外的引脚和功能。
Note 1. PER≤30.8%，有效载荷为37字节
Note 2. RF输入信号的中心频率与芯片内部产生的载波频率之间的允许差值范围

48.17.5 接收特性(125kbps)

Table 48.76 接收特性
Conditions:VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	测试条件	
输入频率	RF_{RXFIN_125k}	2402	—	2480	MHz		
最大输入电平	RF_{LEVL_125k}	–10	4	—	dBm	*1	
接收灵敏度	RF_{STY_125k}	—	–105	—	dBm	*1	
二次发射强度	RF_{RXSP_125k}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
同频抑制比	RF_{CCR_125k}	—	–2	—	dB	Prf = –79 dBm*1	
邻道抑制比	RF_{ADCR_125k}	—	12	—	dB	Prf = –79 dBm*1	±1 MHz
		—	39	—	dB		±2 MHz
		—	45	—	dB		±3 MHz
Blocking	RF_{BLK_125k}	—	0	—	dBm	Prf = –79 dBm*1	30 MHz to 2000 MHz
		—	–23	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–1	—	dBm		> 3000MHz
允许频率偏差*2	RF_{RXFER_125k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_125k}	—	±4	—	dB	T_a = +25°C, –70 dBm ≤ Prf ≤ –10 dBm	

Note: 这些特性基于未使用的BLE接口以外的引脚和功能。
Note 1. PER≤30.8%，有效载荷为37字节
Note 2. RF输入信号的中心频率与芯片内部产生的载波频率之间的允许差值范围

Appendix 1. Port States in each Processing Mode

Table 1.1 Port states in each processing mode (1 of 2)

Port name	Reset	Software Standby Mode	
		OPE = 0	OPE = 1
P004/IRQ3	Hi-Z	Keep-O*1	
P010/IRQ14	Hi-Z	Keep-O*1	
P011/IRQ15	Hi-Z	Keep-O*1	
P014/DA0	Hi-Z	[DA0 output (DAOE0 = 1)] DA output retained [All other (DAOE0 = 0)] Keep-O	
P015/IRQ7	Hi-Z	Keep-O*1	
P100/RXD0/CMPIN0/KR00/IRQ2/AGTIO0	Hi-Z	[AGTIO0 selected] AGTIO0 output*2 [All other] Keep-O*1	
P101/CMPREF0/KR01/IRQ1	Hi-Z	[All other] Keep-O*1	
P102/CMPIN1/KR02/AGTO0	Hi-Z	[AGTO0 selected] AGTO0 output*2 [All other] Keep-O*1	
P103/CMPREF1/KR03	Hi-Z	[All other] Keep-O*1	
P104/RXD0/KR04/IRQ1	Hi-Z	[All other] Keep-O*1	
P105/KR05/IRQ0	Hi-Z	[All other] Keep-O*1	
P106/KR06	Hi-Z	[All other] Keep-O*1	
P107/KR07	Hi-Z	[All other] Keep-O*1	
P108/TMS	Pull-up	Keep-O	
P109/TDO/CLKOUT	TDO output	[CLKOUT selected] CLKOUT output [All other] Keep-O	
P110/IRQ3/TDI/VCOUT	Pull-up	[ACMPLP selected] VCOUT output [All other] Keep-O*1	
P200/NMI	Hi-Z	Hi-Z	
P201	Pull-up	Keep-O	
P204/SCL0/USB_OVRCURB/AGTIO1	Hi-Z	[AGTIO1 selected] AGTIO1 output*2 [All other] Keep-O*1	
P205/USB_OVRCURA/IRQ1/CLKOUT/ AGTO1	Hi-Z	[CLKOUT selected] CLKOUT output [AGTO1 selected] AGTO1 output*2 [All other] Keep-O*1	
P206/WAIT/IRQ0	Hi-Z	Keep-O*1	
P212/IRQ3/EXTAL	Hi-Z	Keep-O*1	
P213/IRQ2/XTAL	Hi-Z	Keep-O*1	
P214/XCOUT	Hi-Z	[Sub-clock oscillator selected] Sub-clock oscillator is operating [All other] Hi-Z	
P215/XCIN	Hi-Z	[Sub-clock oscillator selected] Sub-clock oscillator is operating [All other] Hi-Z	

附录1.每种处理模式下的端口状态

Table 1.1 每种处理模式中的端口状态（2个中的1个）

端口名称	Reset	软件待机模式	
		OPE = 0	OPE = 1
P004/IRQ3	Hi-Z	Keep-O*1	
P010/IRQ14	Hi-Z	Keep-O*1	
P011/IRQ15	Hi-Z	Keep-O*1	
P014/DA0	Hi-Z	[DA0输出(DAOE0=1)]DA 输出保留[所有其他(DAOE 0=0)]保持-O	
P015/IRQ7	Hi-Z	Keep-O*1	
P100/RXD0/CMPIN0/KR00/IRQ2/AGTIO0	Hi-Z	[AGTIO0 selected] AGTIO0 output*2 [All other] Keep-O*1	
P101/CMPREF0/KR01/IRQ1	Hi-Z	[All other] Keep-O*1	
P102/CMPIN1/KR02/AGTO0	Hi-Z	[AGTO0 selected] AGTO0 output*2 [All other] Keep-O*1	
P103/CMPREF1/KR03	Hi-Z	[All other] Keep-O*1	
P104/RXD0/KR04/IRQ1	Hi-Z	[All other] Keep-O*1	
P105/KR05/IRQ0	Hi-Z	[All other] Keep-O*1	
P106/KR06	Hi-Z	[All other] Keep-O*1	
P107/KR07	Hi-Z	[All other] Keep-O*1	
P108/TMS	Pull-up	Keep-O	
P109/TDO/CLKOUT	TDO输出	[CLKOUT selected] CLKOUT output [All other] Keep-O	
P110/IRQ3/TDI/VCOUT	Pull-up	[ACMPLP selected] VCOUT output [All other] Keep-O*1	
P200/NMI	Hi-Z	Hi-Z	
P201	Pull-up	Keep-O	
P204/SCL0/USB_OVRCURB/AGTIO1	Hi-Z	[AGTIO1 selected] AGTIO1 output*2 [All other] Keep-O*1	
P205/USB_OVRCURA/IRQ1/CLKOUT/ AGTO1	Hi-Z	[CLKOUT selected] CLKOUT output [AGTO1 selected] AGTO1 output*2 [All other] Keep-O*1	
P206/WAIT/IRQ0	Hi-Z	Keep-O*1	
P212/IRQ3/EXTAL	Hi-Z	Keep-O*1	
P213/IRQ2/XTAL	Hi-Z	Keep-O*1	
P214/XCOUT	Hi-Z	[选择子时钟振荡器]子时钟振荡 器正在运行[所有其他]Hi-Z	
P215/XCIN	Hi-Z	[选择子时钟振荡器]子时钟振荡 器正在运行[所有其他]Hi-Z	

Table 1.1 Port states in each processing mode (2 of 2)

Port name	Reset	Software Standby Mode	
		OPE = 0	OPE = 1
P300/TCK	Pull-up	Keep-O	
P402/RTCIC0/IRQ4	Hi-Z	[All other] Keep-O*1	
P404	Hi-Z	Keep-O*1	
P407/SDA0/USB_VBUS/RTCOUT/AGTIO0	Hi-Z	[RTCOUT selected] RTCOUT output [AGTIO0 selected] AGTIO0 output*2 [All other] Keep-O*1	
P409/IRQ6	Hi-Z	Keep-O*1	
P414/IRQ9	Hi-Z	Keep-O*1	
P501/CMPIN1/USB_OVRCURA/IRQ11/ AGTOB0	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [All other] Keep-O*1	
P914/USB_DP	Hi-Z	Keep-O	
P915/USB_DM	Hi-Z	Keep-O	

H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.

Note: Retains LCD output when the LCD controller/driver pin functions (COM0 to COM3 and SEG6, SEG9, SEG11, SEG12, SEG20, SEG23, SEG49, SEG52, SEG51) are set and LOCO or SOSC is selected in the SLCDSCKCR.LCDSCKSEL[2:0] bit.
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.
Note 2. AGTIO output is enabled while LOCO or SOSC is selected as a count source.

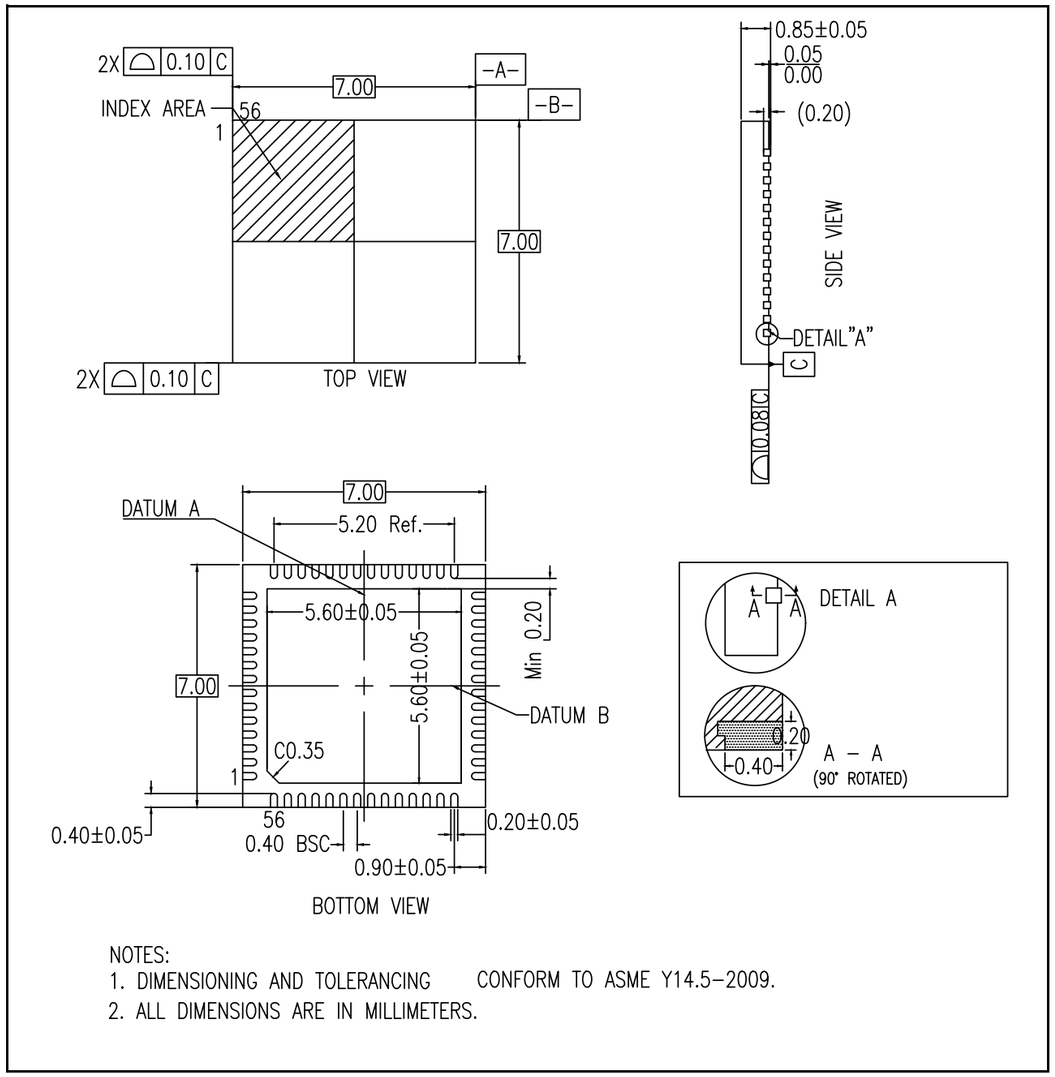
Table 1.1 每种处理模式中的端口状态（2个中的2个）

端口名称	Reset	软件待机模式	
		OPE = 0	OPE = 1
P300/TCK	Pull-up	Keep-O	
P402/RTCIC0/IRQ4	Hi-Z	[All other] Keep-O*1	
P404	Hi-Z	Keep-O*1	
P407/SDA0/USB_VBUS/RTCOUT/AGTIO0	Hi-Z	[RTCOUT selected] RTCOUT output [AGTIO0 selected] AGTIO0 output*2 [All other] Keep-O*1	
P409/IRQ6	Hi-Z	Keep-O*1	
P414/IRQ9	Hi-Z	Keep-O*1	
P501/CMPIN1/USB_OVRCURA/IRQ11/ AGTOB0	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [All other] Keep-O*1	
P914/USB_DP	Hi-Z	Keep-O	
P915/USB_DM	Hi-Z	Keep-O	

H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O：输出引脚保留其先前的值。输入引脚变为高阻抗。

Note: 当LCD控制器驱动器引脚功能（COM0至COM3和SEG6、SEG9、SEG11、SEG12、SEG20、SEG23、SEG49、SEG52、SEG51)置位，并在SLCDSCKCR.LCDSCKSEL[2:0]位中选择LOCO或SOSC。
Note 1. 如果该引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
Note 2. 在选择LoCO或SOSC作为计数源时，启用了AGTIO输出。

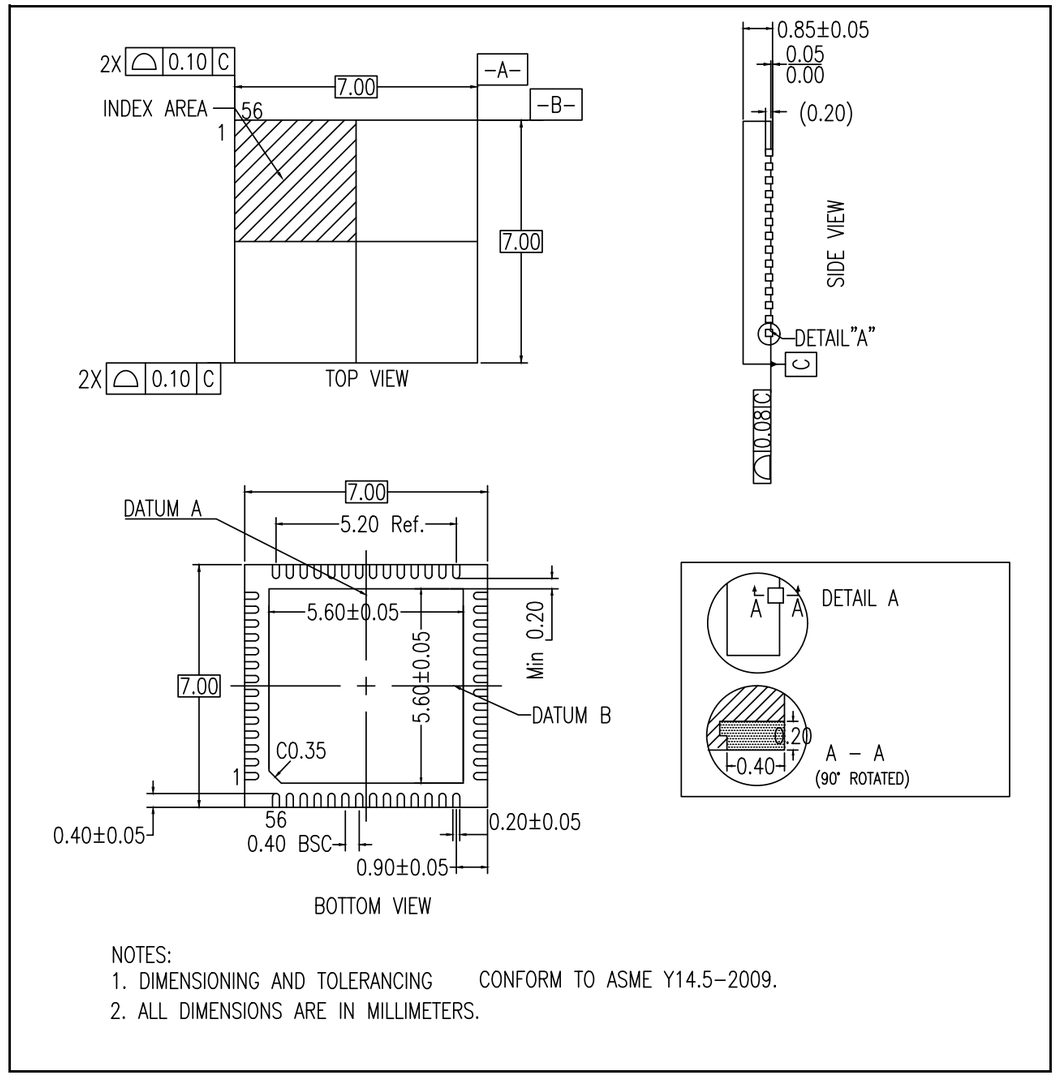
Appendix 2. Package Dimensions



NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

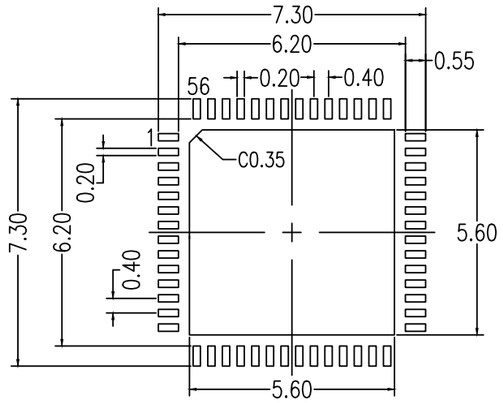
Figure 2.1 QFN 56-pin

附录2.封装尺寸



NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

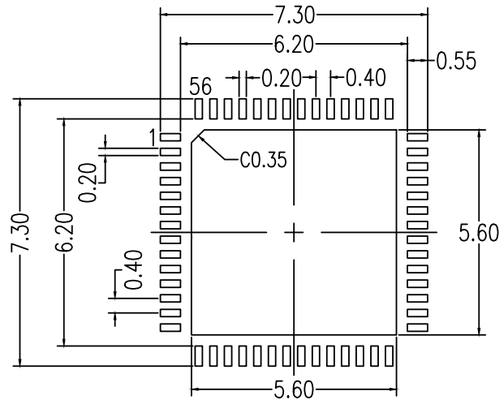
Figure 2.1 QFN 56-pin



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.

Figure 2.2 Land Pattern



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.

Figure 2.2 土地格局

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MMPU	Bus Master MPU	0x40000000
SMPU	Bus Slave MPU	0x40000C00
SPMON	CPU Stack Pointer Monitor	0x40000D00
MMF	Memory Mirror Function	0x40001000
SRAM	SRAM Control	0x40002000
BUS	BUS Control	0x40003000
DMAC0	Direct Memory Access Controller 0	0x40005000
DMAC1	Direct Memory Access Controller 1	0x40005040
DMAC2	Direct Memory Access Controller 2	0x40005080
DMAC3	Direct Memory Access Controller 3	0x400050C0
DMA	DMAC Module Activation	0x40005200
DTC	Data Transfer Controller	0x40005400
ICU	Interrupt Controller	0x40006000
DBG	Debug Function	0x4001B000
FCACHE	Flash Cache	0x4001C000
SYSTEM	System Control	0x4001E000
PORT0	Port 0 Control Registers	0x40040000
PORT1	Port 1 Control Registers	0x40040020
PORT2	Port 2 Control Registers	0x40040040
PORT3	Port 3 Control Registers	0x40040060
PORT4	Port 4 Control Registers	0x40040080
PORT5	Port 5 Control Registers	0x400400A0
PORT9	Port 9 Control Registers	0x40040120
PFS	Pmn Pin Function Control Register	0x40040800
PMISC	Miscellaneous Port Control Register	0x40040D00
ELC	Event Link Controller	0x40041000
POEG	Port Output Enable Module for GPT	0x40042000
RTC	Realtime Clock	0x40044000
WDT	Watchdog Timer	0x40044200
IWDT	Independent Watchdog Timer	0x40044400
CAC	Clock Frequency Accuracy Measurement Circuit	0x40044600
MSTP	Module Stop Control B,C,D	0x40047000
CAN0	CAN0 Module	0x40050000
IIC0	Inter-Integrated Circuit 0	0x40053000
IIC1	Inter-Integrated Circuit 1	0x40053100
DOC	Data Operation Circuit	0x40054100
ADC140	14-bit A/D Converter	0x4005C000
DAC12	12-bit D/A Converter	0x4005E000

附录3.IO寄存器

本附录按功能描述了IO寄存器地址、访问周期和复位值。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。

表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of2)

Name	Description	基址
MMPU	总线主控MPU	0x40000000
SMPU	总线从MPU	0x40000C00
SPMON	CPU堆栈指针监视器	0x40000D00
MMF	内存镜像功能	0x40001000
SRAM	SRAM Control	0x40002000
BUS	总线控制	0x40003000
DMAC0	直接内存访问控制器0	0x40005000
DMAC1	直接内存访问控制器1	0x40005040
DMAC2	直接内存访问控制器2	0x40005080
DMAC3	直接内存访问控制器3	0x400050C0
DMA	DMAC模块激活	0x40005200
DTC	数据传输控制器	0x40005400
ICU	中断控制器	0x40006000
DBG	调试功能	0x4001B000
FCACHE	闪存缓存	0x4001C000
SYSTEM	系统控制	0x4001E000
PORT0	端口0控制寄存器	0x40040000
PORT1	端口1控制寄存器	0x40040020
PORT2	端口2控制寄存器	0x40040040
PORT3	端口3控制寄存器	0x40040060
PORT4	端口4控制寄存器	0x40040080
PORT5	端口5控制寄存器	0x400400A0
PORT9	端口9控制寄存器	0x40040120
PFS	Pmn引脚功能控制寄存器	0x40040800
PMISC	杂项端口控制寄存器	0x40040D00
ELC	事件链接控制器	0x40041000
POEG	GPT端口输出使能模块	0x40042000
RTC	实时时钟	0x40044000
WDT	看门狗定时器	0x40044200
IWDT	独立看门狗定时器	0x40044400
CAC	时钟频率精度测量电路	0x40044600
MSTP	模块停止控制B C D	0x40047000
CAN0	CAN0 Module	0x40050000
IIC0	Inter-Integrated Circuit 0	0x40053000
IIC1	Inter-Integrated Circuit 1	0x40053100
DOC	数据运算电路	0x40054100
ADC140	14-bit A/D Converter	0x4005C000
DAC12	12-bit D/A Converter	0x4005E000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
SCI0	Serial Communication Interface 0	0x40070000
SCI1	Serial Communication Interface 1	0x40070020
SCI4	Serial Communication Interface 4	0x40070080
SCI9	Serial Communication Interface 9	0x40070120
SPI0	Serial Peripheral Interface 0	0x40072000
SPI1	Serial Peripheral Interface 1	0x40072100
CRC	CRC Calculator	0x40074000
GPT320	General PWM Timer 0 (32-bit)	0x40078000
GPT321	General PWM Timer 1 (32-bit)	0x40078100
GPT322	General PWM Timer 2 (32-bit)	0x40078200
GPT323	General PWM Timer 3 (32-bit)	0x40078300
GPT164	General PWM Timer 4 (16-bit)	0x40078400
GPT165	General PWM Timer 5 (16-bit)	0x40078500
GPT168	General PWM Timer 8 (16-bit)	0x40078800
GPT_OPS	Output Phase Switching Controller	0x40078FF0
KINT	Key Interrupt Function	0x40080000
CTSU	Capacitive Touch Sensing Unit	0x40081000
SLCDC	Segment LCD Controller/Driver	0x40082000
AGT0	Asynchronous General Purpose Timer 0	0x40084000
AGT1	Asynchronous General Purpose Timer 1	0x40084100
ACMPLP	Low-Power Analog Comparator	0x40085E00
OPAMP	Operational Amplifier	0x40086000
USBFS	USB 2.0 Full-Speed Module	0x40090000
DAC8	8-bit D/A converter	0x4009E000
FLCN	Flash I/O Register	0x407EC000
TSN	Temperature Sensor	0x407EC000

Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2 and Table 3.3:

- Registers are grouped by associated module
- The number of access cycles indicates the number of cycles based on the specified reference clock
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.1 外设基地址（2个中的2个）

Name	Description	基址
SCI0	串行通讯接口0	0x40070000
SCI1	串行通讯接口1	0x40070020
SCI4	串行通讯接口4	0x40070080
SCI9	串行通讯接口9	0x40070120
SPI0	串行外设接口0	0x40072000
SPI1	串行外设接口1	0x40072100
CRC	CRC Calculator	0x40074000
GPT320	通用PWM定时器0（32位）	0x40078000
GPT321	通用PWM定时器1（32位）	0x40078100
GPT322	通用PWM定时器2（32位）	0x40078200
GPT323	通用PWM定时器3（32位）	0x40078300
GPT164	通用PWM定时器4（16位）	0x40078400
GPT165	通用PWM定时器5（16位）	0x40078500
GPT168	通用PWM定时器8（16位）	0x40078800
GPT_OPS	输出相位切换控制器	0x40078FF0
KINT	按键中断功能	0x40080000
CTSU	电容式触控感应单元	0x40081000
SLCDC	Segment LCD Controller/Driver	0x40082000
AGT0	异步通用定时器0	0x40084000
AGT1	异步通用定时器1	0x40084100
ACMPLP	低功耗模拟比较器	0x40085E00
OPAMP	运算放大器	0x40086000
USBFS	USB2.0全速模块	0x40090000
DAC8	8-bit D/A converter	0x4009E000
FLCN	闪存IO寄存器	0x407EC000
TSN	温度感应器	0x407EC000

名称=外设名称
描述=外围功能
基地址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

以下信息适用于表3.2和表3.3：

- 寄存器按相关模块分组
- 访问周期数表示基于指定参考时钟的周期数
- 在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作
- IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。
- 当ICLK的频率等于PCLK的频率时，分频时钟同步周期的数量始终是恒定的。
- 当ICLK的频率大于PCLK的频率时，分频时钟同步周期数至少增加1个PCLK周期。

Note: 这适用于当来自CPU的访问与从外部存储器获取指令或来自其他总线主控器（例如DTC或DMAC）的总线访问不冲突时的周期数。

Table 3.2 shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	4000 0000h	4001 CFFFh	2				ICLK	Memory Protection Unit, Memory Mirror Function, SRAM, Buses, DMA Controller, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSTEM	4001 E000h	4001 E3FFh	3				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
SYSTEM	4001 E400h	4001 E6FFh	7		5 ~ 7		PCLKB	Low Power Modes, Resets, Low Voltage Detection, Battery Backup Function
PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	4004 0000h	4004 7FFFh	3		2 ~ 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
CAN0, IICn, DOC, ADC140, DAC12	4004 E000h	4005 EFFFh	3		2 ~ 3		PCLKB	Controller Area Network Module, I²C Bus Interface, Data Operation Circuit, 14-Bit A/D Converter, 12-Bit D/A Converter
SCIn	4007 0000h	4007 0EFFh	5*2		2 ~ 3*2		PCLKA	Serial Communications Interface
SPIn	4007 2000h	4007 2FFFh	5*3		2 ~ 3*3		PCLKA	Serial Peripheral Interface
CRC	4007 4000h	4007 4FFFh	3		2 ~ 3		PCLKA	CRC Calculator
GPT32n, GPT_OPS	4007 8000h	4007 8FFFh	See Table 3.3*4				PCLKA	General PWM Timer
FLCN	407E C000h	407E CFFFh	7		7		ICLK	Flash I/O Register
TSN	407E C000h	407E CFFFh	7		7		ICLK	Temperature Sensor
KINT, CTSU, SLCDC	4008 0000h	4008 1FFFh	2		1 ~ 2		PCLKB	Key Interrupt Function, Capacitive Touch Sensing Unit, Segment LCD Controller
AGTn	4008 4000h	4008 4FFFh	3		2 ~ 3		PCLKB	Asynchronous General Purpose Timer
ACMPLP, OPAMP	4008 5000h	4008 6FFFh	2		1 ~ 2		PCLKB	Low-Power Analog Comparator, Operational Amplifier
USBFS	4009 0000h	4009 03FFh	4		3 ~ 4		PCLKB	USB 2.0 Full-Speed Module
USBFS	4009 0400h	4009 04FFh	3		2 ~ 3		PCLKB	USB 2.0 Full-Speed Module

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 ~ 2. 5 is 1 ~ 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Note 4. The access cycles differ depending on the frequency ratio between ICLK, PCLKA, and PCLKD, as shown in Table 3.3.

表3.2显示了非GPT模块的寄存器访问周期。

Table 3.2 非GPT模块的访问周期

Peripherals	Address		访问周期数				循环单元	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	4000 0000h	4001 CFFFh	2				ICLK	内存保护单元，内存镜像功能、SRAM、总线、DMA控制器、数据传输控制器、中断控制器、CPU、闪存
SYSTEM	4001 E000h	4001 E3FFh	3				ICLK	低功耗模式、复位、低电压检测、时钟生成电路，寄存器写入Protection
SYSTEM	4001 E400h	4001 E6FFh	7		5 ~ 7		PCLKB	低功耗模式，复位，低电压检测，电池备份功能
PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	4004 0000h	4004 7FFFh	3		2 ~ 3		PCLKB	IO端口，事件链接控制器，GPT的端口输出使能，实时时钟，看门狗定时器，独立看门狗定时器，时钟频率精度测量电路，模块停止控制
CAN0, IICn, DOC, ADC140, DAC12	4004 E000h	4005 EFFFh	3		2 ~ 3		PCLKB	控制器局域网模块，I2C总线接口，数据运算电路，14位AD转换器，12位数模转换器
SCIn	4007 0000h	4007 0EFFh	5*2		2 ~ 3*2		PCLKA	串行通信接口
SPIn	4007 2000h	4007 2FFFh	5*3		2 ~ 3*3		PCLKA	串行外设接口
CRC	4007 4000h	4007 4FFFh	3		2 ~ 3		PCLKA	CRC Calculator
GPT32n, GPT_OPS	4007 8000h	4007 8FFFh	见表3.3*4				PCLKA	通用PWM定时器
FLCN	407E C000h	407E CFFFh	7		7		ICLK	闪存IO寄存器
TSN	407E C000h	407E CFFFh	7		7		ICLK	温度感应器
KINT, CTSU, SLCDC	4008 0000h	4008 1FFFh	2		1 ~ 2		PCLKB	按键中断功能，电容式触摸传感单元，分段LCD Controller
AGTn	4008 4000h	4008 4FFFh	3		2 ~ 3		PCLKB	异步通用Timer
ACMPLP, OPAMP	4008 5000h	4008 6FFFh	2		1 ~ 2		PCLKB	低功耗模拟比较器，运算放大器
USBFS	4009 0000h	4009 03FFh	4		3 ~ 4		PCLKB	USB2.0全速模块
USBFS	4009 0400h	4009 04FFh	3		2 ~ 3		PCLKB	USB2.0全速模块

注1.如果PCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5~2.5为1~3。注2.访问16位寄存器（FTDRHL、FRDRHL、FCR、FDR、LSR和CDR）时，访问比表3.2中所示的值多2个周期.访问8位寄存器（FTDRH、FTDRL、FRRDH和FRDRL）时，访问周期如表3.2所示。注3.访问32位寄存器(SPDR)时，访问比表3.2中的值多2个周期。访问8位或16位寄存器（SPDR_HA）时，访问周期如表3.2所示。注4.访问周期因ICLK、PCLKA和PCLKD之间的频率比而异，如图所示

Table 3.3.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKA	5 ~ 6	3 ~ 4	PCLKA
ICLK > PCLKD > PCLKA	3 ~ 4	2 ~ 3	PCLKA
PCLKD = ICLK = PCLKA	6	4	PCLKA
PCLKD = ICLK > PCLKA	2 ~ 3	1 ~ 2	PCLKA
PCLKD > ICLK = PCLKA	4	3	PCLKA
PCLKD > ICLK > PCLKA	2 ~ 3	1 ~ 2	PCLKA

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.4 Register description (1 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MMPU	-	-	-	MMPUCTLA	Bus Master MPU Control Register A	0x000	16	read/ write	0x0000	0xFFFF
				MMPUPTA	Group A Protection of Register	0x102	16	read/ write	0x0000	0xFFFF
	16	0x010	0-15	MMPUACA%s	Group A Region %s Access Control Register	0x200	16	read/ write	0x0000	0xFFFF
	16	0x010	0-15	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	read/ write	0x00000000	0x00000003
	16	0x010	0-15	MMPUEA%s	Group A Region %s End Address Register	0x208	32	read/ write	0x00000003	0x00000003
SMPU	-	-	-	SMPUCTL	Slave MPU Control Register	0x00	16	read/ write	0x0000	0xFFFF
				SMPUMBIU	Access Control Register for MBIU	0x10	16	read/ write	0x0000	0xFFFF
				SMPUFBIU	Access Control Register for FBIU	0x14	16	read/ write	0x0000	0xFFFF
				SMPUSRAM0	Access Control Register for SRAM0	0x18	16	read/ write	0x0000	0xFFFF
	3	0x4	0, 2, 6	SMPUP%sBIU	Access Control Register for P%sBIU	0x20	16	read/ write	0x0000	0xFFFF
	-	-	-	SMPUEXBIU	Access Control Register for EXBIU	0x30	16	read/ write	0x0000	0xFFFF
				SMPUEXBIU2	Access Control Register for EXBIU2	0x34	16	read/ write	0x0000	0xFFFF

表3.3显示了GPT模块的寄存器访问周期。

Table 3.3 GPT模块的访问周期

ICLK和PCLK之间的频率比	访问周期数		循环单元
	Read	Write	
ICLK > PCLKD = PCLKA	5 ~ 6	3 ~ 4	PCLKA
ICLK > PCLKD > PCLKA	3 ~ 4	2 ~ 3	PCLKA
PCLKD = ICLK = PCLKA	6	4	PCLKA
PCLKD = ICLK > PCLKA	2 ~ 3	1 ~ 2	PCLKA
PCLKD > ICLK = PCLKA	4	3	PCLKA
PCLKD > ICLK > PCLKA	2 ~ 3	1 ~ 2	PCLKA

3.3 注册说明

本节提供与本手册中描述的寄存器相关的信息。

表3.4显示了寄存器列表，包括地址偏移、地址大小、访问权限和复位值。

Table 3.4 寄存器描述（25个中的1个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
MMPU	-	-	-	MMPUCTLA	总线主控MPU控制 Register A	0x000	16	read/ write	0x0000	0xFFFF
				MMPUPTA	A组保护 Register	0x102	16	read/ write	0x0000	0xFFFF
	16	0x010	0-15	MMPUACA%s	A组区域%s访问权限 控制寄存器	0x200	16	read/ write	0x0000	0xFFFF
	16	0x010	0-15	MMPUSA%s	A组地区%s开始 地址寄存器	0x204	32	read/ write	0x00000000	0x00000003
	16	0x010	0-15	MMPUEA%s	A组地区%s结束 地址寄存器	0x208	32	read/ write	0x00000003	0x00000003
SMPU	-	-	-	SMPUCTL	从机MPU控制寄存器	0x00	16	read/ write	0x0000	0xFFFF
				SMPUMBIU	访问控制寄存器 MBIU	0x10	16	read/ write	0x0000	0xFFFF
				SMPUFBIU	访问控制寄存器 FBIU	0x14	16	read/ write	0x0000	0xFFFF
				SMPUSRAM0	访问控制寄存器 SRAM0	0x18	16	read/ write	0x0000	0xFFFF
	3	0x4	0, 2, 6	SMPUP%sBIU	访问控制寄存器 P%sBIU	0x20	16	read/ write	0x0000	0xFFFF
	-	-	-	SMPUEXBIU	访问控制寄存器 EXBIU	0x30	16	read/ write	0x0000	0xFFFF
				SMPUEXBIU2	访问控制寄存器 EXBIU2	0x34	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (2 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SPMON	-	-	-	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x00	16	read/ write	0x0000	0xFFFF
				MSPMPUCTL	Stack Pointer Monitor Access Control Register	0x04	16	read/ write	0x0000	0xFEFF
				MSPMPUPT	Stack Pointer Monitor Protection Register	0x06	16	read/ write	0x0000	0xFFFF
				MSPMPUSA	Main Stack Pointer (MSP) Monitor Start Address Register	0x08	32	read/ write	0x00000000	0x00000003
				MSPMPUEA	Main Stack Pointer (MSP) Monitor End Address Register	0x0C	32	read/ write	0x00000003	0x00000003
				PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x10	16	read/ write	0x0000	0xFFFF
				PSPMPUCTL	Stack Pointer Monitor Access Control Register	0x14	16	read/ write	0x0000	0xFEFF
				PSPMPUPT	Stack Pointer Monitor Protection Register	0x16	16	read/ write	0x0000	0xFFFF
				PSPMPUSA	Process Stack Pointer (PSP) Monitor Start Address Register	0x18	32	read/ write	0x00000000	0x00000003
				PSPMPUEA	Process Stack Pointer (PSP) Monitor End Address Register	0x1C	32	read/ write	0x00000003	0x00000003
MMF	-	-	-	MMSFR	MemMirror Special Function Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				MMEN	MemMirror Enable Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	read/ write	0x00	0xFF
				SRAMPRCR	SRAM Protection Register	0x04	8	read/ write	0x00	0xFF
				ECCMODE	ECC Operating Mode Control Register	0xC0	8	read/ write	0x00	0xFF
				ECC2STS	ECC 2-Bit Error Status Register	0xC1	8	read/ write	0x00	0xFF
				ECC1STSEN	ECC 1-Bit Error Information Update Enable Register	0xC2	8	read/ write	0x00	0xFF
				ECC1STS	ECC 1-Bit Error Status Register	0xC3	8	read/ write	0x00	0xFF
				ECCPRCR	ECC Protection Register	0xC4	8	read/ write	0x00	0xFF
				ECCPRCR2	ECC Protection Register 2	0xD0	8	read/ write	0x00	0xFF
				ECCETST	ECC Test Control Register	0xD4	8	read/ write	0x00	0xFF
				ECCOAD	SRAM ECC Error Operation After Detection Register	0xD8	8	read/ write	0x00	0xFF

Table 3.4 寄存器说明（25个中的2个）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
SPMON	-	-	-	MSPMPUOAD	堆栈指针监视器检测后的操作Register	0x00	16	read/ write	0x0000	0xFFFF
				MSPMPUCTL	堆栈指针监视器访问控制寄存器	0x04	16	read/ write	0x0000	0xFEFF
				MSPMPUPT	堆栈指针监视器保护登记册	0x06	16	read/ write	0x0000	0xFFFF
				MSPMPUSA	主堆栈指针(MSP)监控起始地址Register	0x08	32	read/ write	0x00000000	0x00000003
				MSPMPUEA	主堆栈指针(MSP)监控结束地址Register	0x0C	32	read/ write	0x00000003	0x00000003
				PSPMPUOAD	堆栈指针监视器检测后的操作Register	0x10	16	read/ write	0x0000	0xFFFF
				PSPMPUCTL	堆栈指针监视器访问控制寄存器	0x14	16	read/ write	0x0000	0xFEFF
				PSPMPUPT	堆栈指针监视器保护登记册	0x16	16	read/ write	0x0000	0xFFFF
				PSPMPUSA	进程堆栈指针(PSP)监控起始地址Register	0x18	32	read/ write	0x00000000	0x00000003
				PSPMPUEA	进程堆栈指针(PSP)监控结束地址Register	0x1C	32	read/ write	0x00000003	0x00000003
MMF	-	-	-	MMSFR	MemMirror特殊功能Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				MMEN	MemMirror启用寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
SRAM	-	-	-	PARIOAD	SRAM奇偶校验错误操作检测后寄存器	0x00	8	read/ write	0x00	0xFF
				SRAMPRCR	SRAM保护寄存器	0x04	8	read/ write	0x00	0xFF
				ECCMODE	ECC操作模式控制寄存器	0xC0	8	read/ write	0x00	0xFF
				ECC2STS	ECC2位错误状态Register	0xC1	8	read/ write	0x00	0xFF
				ECC1STSEN	ECC1位错误信息更新启用寄存器	0xC2	8	read/ write	0x00	0xFF
				ECC1STS	ECC1位错误状态Register	0xC3	8	read/ write	0x00	0xFF
				ECCPRCR	ECC保护寄存器	0xC4	8	read/ write	0x00	0xFF
				ECCPRCR2	ECC保护寄存器2	0xD0	8	read/ write	0x00	0xFF
				ECCETST	ECC测试控制寄存器	0xD4	8	read/ write	0x00	0xFF
				ECCOAD	SRAMECC错误操作检测后寄存器	0xD8	8	read/ write	0x00	0xFF

Table 3.4 Register description (3 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DMAC0-3	-	-	-	DMSAR	DMA Source Address Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				DMDAR	DMA Destination Address Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				DMCRA	DMA Transfer Count Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
				DMCRB	DMA Block Transfer Count Register	0x0C	16	read/ write	0x0000	0xFFFF
				DMTMD	DMA Transfer Mode Register	0x10	16	read/ write	0x0000	0xFFFF
				DMINT	DMA Interrupt Setting Register	0x13	8	read/ write	0x00	0xFF
				DMAMD	DMA Address Mode Register	0x14	16	read/ write	0x0000	0xFFFF
				DMOFR	DMA Offset Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
				DMCNT	DMA Transfer Enable Register	0x1C	8	read/ write	0x00	0xFF
				DMREQ	DMA Software Start Register	0x1D	8	read/ write	0x00	0xFF
				DMSTS	DMA Status Register	0x1E	8	read/ write	0x00	0xFF
DMA	-	-	-	DMAST	DMAC Module Activation Register	0x00	8	read/ write	0x00	0xFF
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	read/ write	0x08	0xFF
				DTCVBR	DTC Vector Base Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				DTCST	DTC Module Start Register	0x0C	8	read/ write	0x00	0xFF
				DTCSTS	DTC Status Register	0x0E	16	read-only	0x0000	0xFFFF
ICU	16	0x1	0-15	IRQCR%s	IRQ Control Register %s	0x000	8	read/ write	0x00	0xFF
	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	read/ write	0x00	0xFF
				NMIER	Non-Maskable Interrupt Enable Register	0x120	16	read/ write	0x0000	0xFFFF
				NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	read/ write	0x0000	0xFFFF
				NMISR	Non-Maskable Interrupt Status Register	0x140	16	read-only	0x0000	0xFFFF
				WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	read/ write	0x00000000	0xFFFFFFFF
				SELSR0	Snooze Event Link Setting Register	0x200	16	read/ write	0x0000	0xFFFF
	4	0x4	0-3	DELSR%s	DMAC Event Link Setting Register %s	0x280	16	read/ write	0x0000	0xFFFF
	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	read/ write	0x00000000	0xFFFFFFFF
DBG	-	-	-	DBGSTR	Debug Status Register	0x000	32	read-only	0x00000000	0xFFFFFFFF
				DBGSTOPCR	Debug Stop Control Register	0x010	32	read/ write	0x00000003	0xFFFFFFFF
				TRACECTR	Trace Control Register	0x020	32	read/ write	0x00000000	0xFFFFFFFF
FCACHE	-	-	-	FCACHEE	Flash Cache Enable Register	0x100	16	read/ write	0x0000	0xFFFF
				FCACHEIV	Flash Cache Invalidate Register	0x104	16	read/ write	0x0000	0xFFFF

Table 3.4 注册描述（3/25）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
DMAC0-3	-	-	-	DMSAR	DMA源地址 Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				DMDAR	DMA目标地址 Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				DMCRA	DMA传输计数 Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
				DMCRB	DMA块传输计数 Register	0x0C	16	read/ write	0x0000	0xFFFF
				DMTMD	DMA传输模式 Register	0x10	16	read/ write	0x0000	0xFFFF
				DMINT	DMA中断设置 Register	0x13	8	read/ write	0x00	0xFF
				DMAMD	DMA地址模式寄存器0x14		16	read/ write	0x0000	0xFFFF
				DMOFR	DMA偏移寄存器	0x18	32	read/ write	0x00000000	0xFFFFFFFF
				DMCNT	DMA传输使能 Register	0x1C	8	read/ write	0x00	0xFF
				DMREQ	DMA软件启动寄存器0x 1D		8	read/ write	0x00	0xFF
				DMSTS	DMA状态寄存器	0x1E	8	read/ write	0x00	0xFF
DMA	-	-	-	DMAST	DMAC模块激活 Register	0x00	8	read/ write	0x00	0xFF
DTC	-	-	-	DTCCR	DTC控制寄存器	0x00	8	read/ write	0x08	0xFF
				DTCVBR	DTC向量基址寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				DTCST	DTC模块启动寄存器	0x0C	8	read/ write	0x00	0xFF
				DTCSTS	DTC状态寄存器	0x0E	16	只读	0x0000	0xFFFF
ICU	16	0x1	0-15	IRQCR%s	IRQ控制寄存器%s	0x000	8	read/ write	0x00	0xFF
	-	-	-	NMICR	NMI引脚中断控制 Register	0x100	8	read/ write	0x00	0xFF
				NMIER	Non-Maskable Interrupt 启用注册	0x120	16	read/ write	0x0000	0xFFFF
				NMICLR	Non-Maskable Interrupt 状态清除寄存器	0x130	16	read/ write	0x0000	0xFFFF
				NMISR	Non-Maskable Interrupt 状态寄存器	0x140	16	只读	0x0000	0xFFFF
				WUPEN	唤醒中断使能 Register	0x1A0	32	read/ write	0x00000000	0xFFFFFFFF
				SELSR0	贪睡事件链接设置 Register	0x200	16	read/ write	0x0000	0xFFFF
	4	0x4	0-3	DELSR%s	DMAC事件链接设置 Register %s	0x280	16	read/ write	0x0000	0xFFFF
	32	0x4	0-31	IELSR%s	ICU事件链接设置 Register %s	0x300	32	read/ write	0x00000000	0xFFFFFFFF
DBG	-	-	-	DBGSTR	调试状态寄存器	0x000	32	只读	0x00000000	0xFFFFFFFF
				DBGSTOPCR	调试停止控制寄存器0x 010		32	read/ write	0x00000003	0xFFFFFFFF
				TRACECTR	跟踪控制寄存器	0x020	32	read/ write	0x00000000	0xFFFFFFFF
FCACHE	-	-	-	FCACHEE	闪存缓存启用 Register	0x100	16	read/ write	0x0000	0xFFFF
				FCACHEIV	闪存缓存失效 Register	0x104	16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (4 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	SBYCR	Standby Control Register	0x00C	16	read/ write	0x4000	0xFFFF
				MSTPCRA	Module Stop Control Register A	0x01C	32	read/ write	0xFFBFFFBE	0xFFFFFFFF
				SCKDIVCR	System Clock Division Control Register	0x020	32	read/ write	0x44044444	0xFFFFFFFF
				SCKSCR	System Clock Source Control Register	0x026	8	read/ write	0x01	0xFF
				PLLCR	PLL Control Register	0x02A	8	read/ write	0x01	0xFF
				PLLCCR2	PLL Clock Control Register2	0x02B	8	read/ write	0x07	0xFF
				MEMWAIT	Memory Wait Cycle Control Register	0x031	8	read/ write	0x00	0xFF
				MOSCCR	Main Clock Oscillator Control Register	0x032	8	read/ write	0x01	0xFF
				HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	read/ write	0x00	0xFE
				MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	read/ write	0x00	0xFF
				OSCSF	Oscillation Stabilization Flag Register	0x03C	8	read-only	0x00	0xFE
				CKOCR	Clock Out Control Register	0x03E	8	read/ write	0x00	0xFF
				TRCKCR	Trace Clock Control Register	0x03F	8	read/ write	0x01	0xFF
				OSTDCR	Oscillation Stop Detection Control Register	0x040	8	read/ write	0x00	0xFF
				OSTDSR	Oscillation Stop Detection Status Register	0x041	8	read/ write	0x00	0xFF
				SLCDSCKCR	Segment LCD Source Clock Control Register	0x050	8	read/ write	0x00	0xFF
				MOCOUTCR	MOCO User Trimming Control Register	0x061	8	read/ write	0x00	0xFF
				HOCOUTCR	HOCO User Trimming Control Register	0x062	8	read/ write	0x00	0xFF
				SNZCR	Snooze Control Register	0x092	8	read/ write	0x00	0xFF
				SNZEDCR	Snooze End Control Register	0x094	8	read/ write	0x00	0xFF
				SNZREQCR	Snooze Request Control Register	0x098	32	read/ write	0x00000000	0xFFFFFFFF
				FLSTOP	Flash Operation Control Register	0x09E	8	read/ write	0x00	0xFF

Table 3.4 寄存器说明（25个中的4个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
SYSTEM	-	-	-	SBYCR	待机控制寄存器	0x00C	16	read/ write	0x4000	0xFFFF
				MSTPCRA	模块停止控制 Register A	0x01C	32	read/ write	0xFFBFFFBE	0xFFFFFFFF
				SCKDIVCR	系统时钟划分 控制寄存器	0x020	32	read/ write	0x44044444	0xFFFFFFFF
				SCKSCR	系统时钟源 控制寄存器	0x026	8	read/ write	0x01	0xFF
				PLLCR	锁相环控制寄存器	0x02A	8	read/ write	0x01	0xFF
				PLLCCR2	PLL时钟控制寄存器20x02B		8	read/ write	0x07	0xFF
				MEMWAIT	内存等待周期控制 Register	0x031	8	read/ write	0x00	0xFF
				MOSCCR	主时钟振荡器控制 Register	0x032	8	read/ write	0x01	0xFF
				HOCOCR	High-Speed On-Chip 振荡器控制寄存器	0x036	8	read/ write	0x00	0xFE
				MOCOCR	Middle-Speed On-Chip 振荡器控制寄存器	0x038	8	read/ write	0x00	0xFF
				OSCSF	振荡稳定标志 Register	0x03C	8	只读	0x00	0xFE
				CKOCR	时钟输出控制寄存器	0x03E	8	read/ write	0x00	0xFF
				TRCKCR	跟踪时钟控制寄存器0x 03F		8	read/ write	0x01	0xFF
				OSTDCR	振荡停止检测 控制寄存器	0x040	8	read/ write	0x00	0xFF
				OSTDSR	振荡停止检测 状态寄存器	0x041	8	read/ write	0x00	0xFF
				SLCDSCKCR	段式LCD源时钟 控制寄存器	0x050	8	read/ write	0x00	0xFF
				MOCOUTCR	MOCO用户修整 控制寄存器	0x061	8	read/ write	0x00	0xFF
				HOCOUTCR	HOCO用户修整 控制寄存器	0x062	8	read/ write	0x00	0xFF
				SNZCR	贪睡控制寄存器	0x092	8	read/ write	0x00	0xFF
				SNZEDCR	贪睡结束控制寄存器0x 094		8	read/ write	0x00	0xFF
				SNZREQCR	贪睡请求控制 Register	0x098	32	read/ write	0x00000000	0xFFFFFFFF
				FLSTOP	闪光操作控制 Register	0x09E	8	read/ write	0x00	0xFF

Table 3.4 Register description (5 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	PSMCR	Power Save Memory Control Register	0x09F	8	read/ write	0x00	0xFF
				OPCCR	Operating Power Control Register	0x0A0	8	read/ write	0x02	0xFF
				MOSCWTCR	Main Clock Oscillator Wait Control Register	0x0A2	8	read/ write	0x05	0xFF
				HOCOWTCR	High-Speed On-Chip Oscillator Wait Control Register	0x0A5	8	read/ write	0x05	0xFF
				SOPCCR	Sub Operating Power Control Register	0x0AA	8	read/ write	0x00	0xFF
				RSTSR1	Reset Status Register 1	0x0C0	16	read/ write	0x0000	0xE0F8
				BKRACR	Backup Register Access Control Register	0x0C6	8	read/ write	0x06	0xFF
				USBCKCR	USB Clock Control register	0x0D0	8	read/ write	0x00	0xFF
	2	0x2	1,2	LVD%sCR1	Voltage Monitor %s Circuit Control Register 1	0x0E0	8	read/ write	0x01	0xFF
	2	0x2	1,2	LVD%sSR	Voltage Monitor %s Circuit Status Register	0x0E1	8	read/ write	0x02	0xFF
	-	-	-	PRCR	Protect Register	0x3FE	16	read/ write	0x0000	0xFFFF
				SYOCDCR	System Control OCD Control Register	0x40E	8	read/ write	0x00	0xFF
				RSTSR0	Reset Status Register 0	0x410	8	read/ write	0x00	0xF0
				RSTSR2	Reset Status Register 2	0x411	8	read/ write	0x00	0xFE
				MOMCR	Main Clock Oscillator Mode Oscillation Control Register	0x413	8	read/ write	0x00	0xFF
				LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	read/ write	0x00	0xFF
				LVDLVLR	Voltage Detection Level Select Register	0x418	8	read/ write	0x07	0xFF
	2	0x1	1,2	LVD%sCR0	Voltage Monitor %s Circuit Control Register 0	0x41A	8	read/ write	0x80	0xF7
	-	-	-	VBTCR1	VBATT Control Register1	0x41F	8	read/ write	0x00	0xFF
				SOSCCR	Sub-Clock Oscillator Control Register	0x480	8	read/ write	0x01	0xFF
				SOMCR	Sub Clock Oscillator Mode Control Register	0x481	8	read/ write	0x00	0xFF
				LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	read/ write	0x00	0xFF
				LOCOUTCR	LOCO User Trimming Control Register	0x492	8	read/ write	0x00	0xFF
				VBTCR2	VBATT Control Register2	0x4B0	8	read/ write	0x00	0xFF
				VBTSR	VBATT Status Register	0x4B1	8	read/ write	0x01	0xEC
				VBTCMPCR	VBATT Comparator Control Register	0x4B2	8	read/ write	0x00	0xFF

Table 3.4 注册描述（5/25）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
SYSTEM	-	-	-	PSMCR	省电记忆控制 Register	0x09F	8	read/ write	0x00	0xFF
				OPCCR	工作功率控制 Register	0x0A0	8	read/ write	0x02	0xFF
				MOSCWTCR	主时钟振荡器等待控制寄存器	0x0A2	8	read/ write	0x05	0xFF
				HOCOWTCR	High-Speed On-Chip 振荡器等待控制 Register	0x0A5	8	read/ write	0x05	0xFF
				SOPCCR	副作业功率控制寄存器	0x0AA	8	read/ write	0x00	0xFF
				RSTSR1	复位状态寄存器1	0x0C0	16	read/ write	0x0000	0xE0F8
				BKRACR	备份寄存器访问控制寄存器	0x0C6	8	read/ write	0x06	0xFF
				USBCKCR	USB时钟控制寄存器	0x0D0	8	read/ write	0x00	0xFF
	2	0x2	1,2	LVD%sCR1	电压监视器%s电路控制寄存器1	0x0E0	8	read/ write	0x01	0xFF
	2	0x2	1,2	LVD%sSR	电压监视器%s电路状态寄存器	0x0E1	8	read/ write	0x02	0xFF
	-	-	-	PRCR	保护寄存器	0x3FE	16	read/ write	0x0000	0xFFFF
				SYOCDCR	系统控制OCD控制 Register	0x40E	8	read/ write	0x00	0xFF
				RSTSR0	复位状态寄存器0	0x410	8	read/ write	0x00	0xF0
				RSTSR2	复位状态寄存器2	0x411	8	read/ write	0x00	0xFE
				MOMCR	主时钟振荡器模式振荡控制寄存器	0x413	8	read/ write	0x00	0xFF
				LVCMPCR	电压监控电路控制寄存器	0x417	8	read/ write	0x00	0xFF
				LVDLVLR	电压检测电平选择注册	0x418	8	read/ write	0x07	0xFF
	2	0x1	1,2	LVD%sCR0	电压监视器%s电路控制寄存器0	0x41A	8	read/ write	0x80	0xF7
	-	-	-	VBTCR1	VBATT Control Register1	0x41F	8	read/ write	0x00	0xFF
				SOSCCR	副时钟振荡器控制 Register	0x480	8	read/ write	0x01	0xFF
				SOMCR	副时钟振荡器模式控制寄存器	0x481	8	read/ write	0x00	0xFF
				LOCOCR	Low-Speed On-Chip 振荡器控制寄存器	0x490	8	read/ write	0x00	0xFF
				LOCOUTCR	LOCO用户修整控制寄存器	0x492	8	read/ write	0x00	0xFF
				VBTCR2	VBATT Control Register2	0x4B0	8	read/ write	0x00	0xFF
				VBTSR	VBATT状态寄存器	0x4B1	8	read/ write	0x01	0xEC
				VBTCMPCR	VBATT比较器控制 Register	0x4B2	8	read/ write	0x00	0xFF

Table 3.4 Register description (6 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	VBTLVDICR	VBATT Pin Low Voltage Detect Interrupt Control Register	0x4B4	8	read/ write	0x00	0xFF
				VBTWCTLR	VBATT Wakeup function Control Register	0x4B6	8	read/ write	0x00	0xFF
				VBTWCH0OTSR	VBATT Wakeup I/O 0 Output Trigger Select Register	0x4B8	8	read/ write	0x00	0xFF
				VBTICTLR	VBATT Input Control Register	0x4BB	8	read/ write	0x00	0xFF
				VBTOCTLR	VBATT Output Control Register	0x4BC	8	read/ write	0x00	0xFF
				VBTWTER	VBATT Wakeup Trigger source Enable Register	0x4BD	8	read/ write	0x00	0xFF
				VBTWEGR	VBATT Wakeup Trigger source Edge Register	0x4BE	8	read/ write	0x00	0xFF
				VBTWFR	VBATT Wakeup trigger source Flag Register	0x4BF	8	read/ write	0x00	0xFF
	512	0x1	0-511	VBTBKR[%s]	VBATT Backup Register [%s]	0x500	8	read/ write	0x00	0x00
PORT0, 5, 9	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				PODR	Output Data Register	0x00	16	read/ write	0x0000	0xFFFF
				PDR	Data Direction Register	0x02	16	read/ write	0x0000	0xFFFF
				PCNTR2	Port Control Register 2	0x04	32	read-only	0x00000000	0xFFFF0000
				PIDR	Input Data Register	0x06	16	read-only	0x0000	0x0000
				PCNTR3	Port Control Register 3	0x08	32	write-only	0x00000000	0xFFFFFFFF
				PORR	Output Reset Register	0x08	16	write-only	0x0000	0xFFFF
				POSR	Output Set Register	0x0A	16	write-only	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				PODR	Output Data Register	0x00	16	read/ write	0x0000	0xFFFF
				PDR	Data Direction Register	0x02	16	read/ write	0x0000	0xFFFF
				PCNTR2	Port Control Register 2	0x04	32	read-only	0x00000000	0xFFFF0000
				EIDR	Event Input Data Register	0x04	16	read-only	0x0000	0x0000
				PIDR	Input Data Register	0x06	16	read-only	0x0000	0x0000
				PCNTR3	Port Control Register 3	0x08	32	write-only	0x00000000	0xFFFFFFFF
				PORR	Output Set Register	0x08	16	write-only	0x0000	0xFFFF
				POSR	Output Reset Register	0x0A	16	write-only	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR4	Port Control Register 4	0x0C	32	read/ write	0x00000000	0xFFFFFFFF
				EORR	Event Output Set Register	0x0C	16	read/ write	0x0000	0xFFFF
				EOSR	Event Output Reset Register	0x0E	16	read/ write	0x0000	0xFFFF

Table 3.4 寄存器说明（25个中的6个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
SYSTEM	-	-	-	VBTLVDICR	VBATT引脚低电压检测中断控制 Register	0x4B4	8	read/ write	0x00	0xFF
				VBTWCTLR	VBATT唤醒功能控制寄存器	0x4B6	8	read/ write	0x00	0xFF
				VBTWCH0OTSR	VBATT唤醒IO0输出触发选择寄存器	0x4B8	8	read/ write	0x00	0xFF
				VBTICTLR	VBATT输入控制 Register	0x4BB	8	read/ write	0x00	0xFF
				VBTOCTLR	VBATT输出控制 Register	0x4BC	8	read/ write	0x00	0xFF
				VBTWTER	VBATT唤醒触发源使能寄存器	0x4BD	8	read/ write	0x00	0xFF
				VBTWEGR	VBATT唤醒触发源边沿寄存器	0x4BE	8	read/ write	0x00	0xFF
				VBTWFR	VBATT唤醒触发源标志寄存器	0x4BF	8	read/ write	0x00	0xFF
	512	0x1	0-511	VBTBKR[%s]	VBATT备份寄存器[%s]	0x500	8	read/ write	0x00	0x00
PORT0, 5, 9	-	-	-	PCNTR1	端口控制寄存器1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				PODR	输出数据寄存器	0x00	16	read/ write	0x0000	0xFFFF
				PDR	数据方向寄存器	0x02	16	read/ write	0x0000	0xFFFF
				PCNTR2	端口控制寄存器2	0x04	32	只读	0x00000000	0xFFFF0000
				PIDR	输入数据寄存器	0x06	16	只读	0x0000	0x0000
				PCNTR3	端口控制寄存器3	0x08	32	只写	0x00000000	0xFFFFFFFF
				PORR	输出复位寄存器	0x08	16	只写	0x0000	0xFFFF
				POSR	输出设置寄存器	0x0A	16	只写	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR1	端口控制寄存器1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				PODR	输出数据寄存器	0x00	16	read/ write	0x0000	0xFFFF
				PDR	数据方向寄存器	0x02	16	read/ write	0x0000	0xFFFF
				PCNTR2	端口控制寄存器2	0x04	32	只读	0x00000000	0xFFFF0000
				EIDR	事件输入数据寄存器	0x04	16	只读	0x0000	0x0000
				PIDR	输入数据寄存器	0x06	16	只读	0x0000	0x0000
				PCNTR3	端口控制寄存器3	0x08	32	只写	0x00000000	0xFFFFFFFF
				PORR	输出设置寄存器	0x08	16	只写	0x0000	0xFFFF
				POSR	输出复位寄存器	0x0A	16	只写	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR4	端口控制寄存器4	0x0C	32	read/ write	0x00000000	0xFFFFFFFF
				EORR	事件输出设置寄存器	0x0C	16	read/ write	0x0000	0xFFFF
				EOSR	事件输出复位寄存器0x 0E		16	read/ write	0x0000	0xFFFF

Table 3.4 Register description (7 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	-	-	-	P004PFS	P00%s Pin Function Control Register	0x004	32	read/ write	0x00000000	0xFFFFFFFD
	-	-	-	P004PFS_HA	P00%s Pin Function Control Register	0x006	16	read/ write	0x0000	0xFFFD
	-	-	-	P004PFS_BY	P00%s Pin Function Control Register	0x007	8	read/ write	0x00	0xFD
	4	0x4	10, 11, 14, 15	P0%sPFS	P0%s Pin Function Control Register	0x028	32	read/ write	0x00000000	0xFFFFFFFD
	4	0x4	10, 11, 14, 15	P0%sPFS_HA	P0%s Pin Function Control Register	0x02A	16	read/ write	0x0000	0xFFFD
	4	0x4	10, 11, 14, 15	P0%sPFS_BY	P0%s Pin Function Control Register	0x02B	8	read/ write	0x00	0xFD
	8	0x4	0-7	P10%sPFS	P10%s Pin Function Control Register	0x040	32	read/ write	0x00000000	0xFFFFFFFD
	8	0x4	0-7	P10%sPFS_HA	P10%s Pin Function Control Register	0x042	16	read/ write	0x0000	0xFFFD
	8	0x4	0-7	P10%sPFS_BY	P10%s Pin Function Control Register	0x043	8	read/ write	0x00	0xFD
	-	-	-	P108PFS	P108 Pin Function Control Register	0x060	32	read/ write	0x00010010	0xFFFFFFFD
				P108PFS_HA	P108 Pin Function Control Register	0x062	16	read/ write	0x0010	0xFFFD
				P108PFS_BY	P108 Pin Function Control Register	0x063	8	read/ write	0x10	0xFD
				P109PFS	P109 Pin Function Control Register	0x064	32	read/ write	0x00010000	0xFFFFFFFD
				P109PFS_HA	P109 Pin Function Control Register	0x066	16	read/ write	0x0000	0xFFFD
				P109PFS_BY	P109 Pin Function Control Register	0x067	8	read/ write	0x00	0xFD
				P110PFS	P110 Pin Function Control Register	0x068	32	read/ write	0x00010010	0xFFFFFFFD
				P110PFS_HA	P110 Pin Function Control Register	0x06A	16	read/ write	0x0010	0xFFFD
				P110PFS_BY	P110 Pin Function Control Register	0x06B	8	read/ write	0x10	0xFD
				P111PFS	P1%s Pin Function Control Register	0x06C	32	read/ write	0x00000000	0xFFFFFFFD
				P111PFS_HA	P1%s Pin Function Control Register	0x06E	16	read/ write	0x0000	0xFFFD
				P111PFS_BY	P1%s Pin Function Control Register	0x06F	8	read/ write	0x00	0xFD
				P200PFS	P200 Pin Function Control Register	0x080	32	read/ write	0x00000000	0xFFFFFFFD
				P200PFS_HA	P200 Pin Function Control Register	0x082	16	read/ write	0x0000	0xFFFD
				P200PFS_BY	P200 Pin Function Control Register	0x083	8	read/ write	0x00	0xFD

Table 3.4 寄存器说明（25个中的7个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
PFS	-	-	-	P004PFS	P00%s引脚功能控制 Register	0x004	32	read/ write	0x00000000	0xFFFFFFFD
	-	-	-	P004PFS_HA	P00%s引脚功能控制 Register	0x006	16	read/ write	0x0000	0xFFFD
	-	-	-	P004PFS_BY	P00%s引脚功能控制 Register	0x007	8	read/ write	0x00	0xFD
	4	0x4	10, 11, 14, 15	P0%sPFS	P0%s引脚功能控制 Register	0x028	32	read/ write	0x00000000	0xFFFFFFFD
	4	0x4	10, 11, 14, 15	P0%sPFS_HA	P0%s引脚功能控制 Register	0x02A	16	read/ write	0x0000	0xFFFD
	4	0x4	10, 11, 14, 15	P0%sPFS_BY	P0%s引脚功能控制 Register	0x02B	8	read/ write	0x00	0xFD
	8	0x4	0-7	P10%sPFS	P10%s引脚功能控制 Register	0x040	32	read/ write	0x00000000	0xFFFFFFFD
	8	0x4	0-7	P10%sPFS_HA	P10%s引脚功能控制 Register	0x042	16	read/ write	0x0000	0xFFFD
	8	0x4	0-7	P10%sPFS_BY	P10%s引脚功能控制 Register	0x043	8	read/ write	0x00	0xFD
	-	-	-	P108PFS	P108引脚功能控制 Register	0x060	32	read/ write	0x00010010	0xFFFFFFFD
				P108PFS_HA	P108引脚功能控制 Register	0x062	16	read/ write	0x0010	0xFFFD
				P108PFS_BY	P108引脚功能控制 Register	0x063	8	read/ write	0x10	0xFD
				P109PFS	P109引脚功能控制 Register	0x064	32	read/ write	0x00010000	0xFFFFFFFD
				P109PFS_HA	P109引脚功能控制 Register	0x066	16	read/ write	0x0000	0xFFFD
				P109PFS_BY	P109引脚功能控制 Register	0x067	8	read/ write	0x00	0xFD
				P110PFS	P110引脚功能控制 Register	0x068	32	read/ write	0x00010010	0xFFFFFFFD
				P110PFS_HA	P110引脚功能控制 Register	0x06A	16	read/ write	0x0010	0xFFFD
				P110PFS_BY	P110引脚功能控制 Register	0x06B	8	read/ write	0x10	0xFD
				P111PFS	P1%s引脚功能控制 Register	0x06C	32	read/ write	0x00000000	0xFFFFFFFD
				P111PFS_HA	P1%s引脚功能控制 Register	0x06E	16	read/ write	0x0000	0xFFFD
				P111PFS_BY	P1%s引脚功能控制 Register	0x06F	8	read/ write	0x00	0xFD
				P200PFS	P200引脚功能控制 Register	0x080	32	read/ write	0x00000000	0xFFFFFFFD
				P200PFS_HA	P200引脚功能控制 Register	0x082	16	read/ write	0x0000	0xFFFD
				P200PFS_BY	P200引脚功能控制 Register	0x083	8	read/ write	0x00	0xFD

Table 3.4 Register description (8 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	-	-	-	P201PFS	P201 Pin Function Control Register	0x084	32	read/ write	0x00000010	0xFFFFFFFD
				P201PFS_HA	P201 Pin Function Control Register	0x086	16	read/ write	0x0010	0xFFFD
				P201PFS_BY	P201 Pin Function Control Register	0x087	8	read/ write	0x10	0xFD
	3	0x4	4-6	P20%sPFS	P20%s Pin Function Control Register	0x088	32	read/ write	0x00000000	0xFFFFFFFD
	3	0x4	4-6	P20%sPFS_HA	P20%s Pin Function Control Register	0x08A	16	read/ write	0x0000	0xFFFD
	3	0x4	4-6	P20%sPFS_BY	P20%s Pin Function Control Register	0x08B	8	read/ write	0x00	0xFD
	4	0x4	12-15	P2%sPFS	P2%s Pin Function Control Register	0x0B0	32	read/ write	0x00000000	0xFFFFFFFD
	4	0x4	12-15	P2%sPFS_HA	P2%s Pin Function Control Register	0x0B2	16	read/ write	0x0000	0xFFFD
	4	0x4	12-15	P2%sPFS_BY	P2%s Pin Function Control Register	0x0B3	8	read/ write	0x00	0xFD
	-	-	-	P300PFS	P300 Pin Function Control Register	0x0C0	32	read/ write	0x00010010	0xFFFFFFFD
				P300PFS_HA	P300 Pin Function Control Register	0x0C2	16	read/ write	0x0010	0xFFFD
				P300PFS_BY	P300 Pin Function Control Register	0x0C3	8	read/ write	0x10	0xFD
	4	0x4	2, 4, 7	P40%sPFS	P40%s Pin Function Control Register	0x100	32	read/ write	0x00000000	0xFFFFFFFD
	4	0x4	2, 4, 7	P40%sPFS_HA	P40%s Pin Function Control Register	0x102	16	read/ write	0x0000	0xFFFD
	4	0x4	2, 4, 7	P40%sPFS_BY	P40%s Pin Function Control Register	0x103	8	read/ write	0x00	0xFD
	-	-	-	P409PFS	P409 Pin Function Control Register	0x124	32	read/ write	0x00000000	0xFFFFFFFD
				P409PFS_HA	P409 Pin Function Control Register	0x126	16	read/ write	0x0000	0xFFFD
				P409PFS_BY	P409 Pin Function Control Register	0x127	8	read/ write	0x00	0xFD
	-	-	-	P414PFS	P4%s Pin Function Control Register	0x128	32	read/ write	0x00000000	0xFFFFFFFD
				P414PFS_HA	P4%s Pin Function Control Register	0x12A	16	read/ write	0x0000	0xFFFD
				P414PFS_BY	P4%s Pin Function Control Register	0x12B	8	read/ write	0x00	0xFD
PFS	-	-	-	P501PFS	P50%s Pin Function Control Register	0x140	32	read/ write	0x00000000	0xFFFFFFFD
				P501PFS_HA	P50%s Pin Function Control Register	0x142	16	read/ write	0x0000	0xFFFD
				P501PFS_BY	P50%s Pin Function Control Register	0x143	8	read/ write	0x00	0xFD
PFS	2	0x4	14,15	P9%sPFS	P9%s Pin Function Control Register	0x278	32	read/ write	0x00010000	0xFFFFFFFD
	2	0x4	14,15	P9%sPFS_HA	P9%s Pin Function Control Register	0x27A	16	read/ write	0x0000	0xFFFD
	2	0x4	14,15	P9%sPFS_BY	P9%s Pin Function Control Register	0x27B	8	read/ write	0x00	0xFD
PMISC	-	-	-	PWPR	Write-Protect Register	0x03	8	read/ write	0x80	0xFF

Table 3.4 寄存器说明（25个中的8个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
PFS	-	-	-	P201PFS	P201引脚功能控制 Register	0x084	32	read/ write	0x00000010	0xFFFFFFFD
				P201PFS_HA	P201引脚功能控制 Register	0x086	16	read/ write	0x0010	0xFFFD
				P201PFS_BY	P201引脚功能控制 Register	0x087	8	read/ write	0x10	0xFD
	3	0x4	4-6	P20%sPFS	P20%s引脚功能控制 Register	0x088	32	read/ write	0x00000000	0xFFFFFFFD
	3	0x4	4-6	P20%sPFS_HA	P20%s引脚功能控制 Register	0x08A	16	read/ write	0x0000	0xFFFD
	3	0x4	4-6	P20%sPFS_BY	P20%s引脚功能控制 Register	0x08B	8	read/ write	0x00	0xFD
	4	0x4	12-15	P2%sPFS	P2%s引脚功能控制 Register	0x0B0	32	read/ write	0x00000000	0xFFFFFFFD
	4	0x4	12-15	P2%sPFS_HA	P2%s引脚功能控制 Register	0x0B2	16	read/ write	0x0000	0xFFFD
	4	0x4	12-15	P2%sPFS_BY	P2%s引脚功能控制 Register	0x0B3	8	read/ write	0x00	0xFD
	-	-	-	P300PFS	P300引脚功能控制 Register	0x0C0	32	read/ write	0x00010010	0xFFFFFFFD
				P300PFS_HA	P300引脚功能控制 Register	0x0C2	16	read/ write	0x0010	0xFFFD
				P300PFS_BY	P300引脚功能控制 Register	0x0C3	8	read/ write	0x10	0xFD
	4	0x4	2, 4, 7	P40%sPFS	P40%s引脚功能控制 Register	0x100	32	read/ write	0x00000000	0xFFFFFFFD
	4	0x4	2, 4, 7	P40%sPFS_HA	P40%s引脚功能控制 Register	0x102	16	read/ write	0x0000	0xFFFD
	4	0x4	2, 4, 7	P40%sPFS_BY	P40%s引脚功能控制 Register	0x103	8	read/ write	0x00	0xFD
	-	-	-	P409PFS	P409引脚功能控制 Register	0x124	32	read/ write	0x00000000	0xFFFFFFFD
				P409PFS_HA	P409引脚功能控制 Register	0x126	16	read/ write	0x0000	0xFFFD
				P409PFS_BY	P409引脚功能控制 Register	0x127	8	read/ write	0x00	0xFD
	-	-	-	P414PFS	P4%s引脚功能控制 Register	0x128	32	read/ write	0x00000000	0xFFFFFFFD
				P414PFS_HA	P4%s引脚功能控制 Register	0x12A	16	read/ write	0x0000	0xFFFD
				P414PFS_BY	P4%s引脚功能控制 Register	0x12B	8	read/ write	0x00	0xFD
PFS	-	-	-	P501PFS	P50%s引脚功能控制 Register	0x140	32	read/ write	0x00000000	0xFFFFFFFD
				P501PFS_HA	P50%s引脚功能控制 Register	0x142	16	read/ write	0x0000	0xFFFD
				P501PFS_BY	P50%s引脚功能控制 Register	0x143	8	read/ write	0x00	0xFD
PFS	2	0x4	14,15	P9%sPFS	P9%s引脚功能控制 Register	0x278	32	read/ write	0x00010000	0xFFFFFFFD
	2	0x4	14,15	P9%sPFS_HA	P9%s引脚功能控制 Register	0x27A	16	read/ write	0x0000	0xFFFD
	2	0x4	14,15	P9%sPFS_BY	P9%s引脚功能控制 Register	0x27B	8	read/ write	0x00	0xFD
PMISC	-	-	-	PWPR	Write-Protect Register	0x03	8	read/ write	0x80	0xFF

Table 3.4 Register description (9 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ELC	-	-	-	ELCR	Event Link Controller Register	0x00	8	read/ write	0x00	0xFF
	2	0x2	0,1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	read/ write	0x80	0xFF
	10	0x4	0-9	ELSR%s	Event Link Setting Register %s	0x10	16	read/ write	0x0000	0xFFFF
	-	-	-	ELSR12	Event Link Setting Register 12	0x40	16	read/ write	0x0000	0xFFFF
	5	0x4	14-18	ELSR%s	Event Link Setting Register %s	0x48	16	read/ write	0x0000	0xFFFF
POEG	2	0x100	A,B	POEGG%s	POEG Group %s Setting Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	read-only	0x00	0x80
				RSECCNT	Second Counter	0x02	8	read/ write	0x00	0x00
				BCNT0	Binary Counter 0	0x02	8	read/ write	0x00	0x00
				RMINCNT	Minute Counter	0x04	8	read/ write	0x00	0x00
				BCNT1	Binary Counter 1	0x04	8	read/ write	0x00	0x00
				RHRCNT	Hour Counter	0x06	8	read/ write	0x00	0x00
				BCNT2	Binary Counter 2	0x06	8	read/ write	0x00	0x00
				RWKCNT	Day-of-Week Counter	0x08	8	read/ write	0x00	0x00
				BCNT3	Binary Counter 3	0x08	8	read/ write	0x00	0x00
				RDAYCNT	Day Counter	0x0A	8	read/ write	0x00	0xC0
				RMONCNT	Month Counter	0x0C	8	read/ write	0x00	0xE0
				RYRCNT	Year Counter	0x0E	16	read/ write	0x0000	0xFF00
				RSECAR	Second Alarm Register	0x10	8	read/ write	0x00	0x00
				BCNT0AR	Binary Counter 0 Alarm Register	0x10	8	read/ write	0x00	0x00
				RMINAR	Minute Alarm Register	0x12	8	read/ write	0x00	0x00
				BCNT1AR	Binary Counter 1 Alarm Register	0x12	8	read/ write	0x00	0x00
				RHRAR	Hour Alarm Register	0x14	8	read/ write	0x00	0x00
				BCNT2AR	Binary Counter 2 Alarm Register	0x14	8	read/ write	0x00	0x00
				RWKAR	Day-of-Week Alarm Register	0x16	8	read/ write	0x00	0x00
				BCNT3AR	Binary Counter 3 Alarm Register	0x16	8	read/ write	0x00	0x00

Table 3.4 寄存器说明（25个中的9个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
ELC	-	-	-	ELCR	事件链接控制器 Register	0x00	8	read/ write	0x00	0xFF
	2	0x2	0,1	ELSEGR%s	活动链接软件活动 代寄存器%s	0x02	8	read/ write	0x80	0xFF
	10	0x4	0-9	ELSR%s	事件链接设置寄存器%s	0x10	16	read/ write	0x0000	0xFFFF
	-	-	-	ELSR12	事件链接设置寄存器12	0x40	16	read/ write	0x0000	0xFFFF
	5	0x4	14-18	ELSR%s	事件链接设置寄存器%s	0x48	16	read/ write	0x0000	0xFFFF
POEG	2	0x100	A,B	POEGG%s	POEG组%s设置 Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	只读	0x00	0x80
				RSECCNT	第二个柜台	0x02	8	read/ write	0x00	0x00
				BCNT0	二进制计数器0	0x02	8	read/ write	0x00	0x00
				RMINCNT	分钟计数器	0x04	8	read/ write	0x00	0x00
				BCNT1	二进制计数器1	0x04	8	read/ write	0x00	0x00
				RHRCNT	小时计数器	0x06	8	read/ write	0x00	0x00
				BCNT2	二进制计数器2	0x06	8	read/ write	0x00	0x00
				RWKCNT	Day-of-Week Counter	0x08	8	read/ write	0x00	0x00
				BCNT3	二进制计数器3	0x08	8	read/ write	0x00	0x00
				RDAYCNT	日计数器	0x0A	8	read/ write	0x00	0xC0
				RMONCNT	月计数器	0x0C	8	read/ write	0x00	0xE0
				RYRCNT	年计数器	0x0E	16	read/ write	0x0000	0xFF00
				RSECAR	第二报警寄存器	0x10	8	read/ write	0x00	0x00
				BCNT0AR	二进制计数器0报警 Register	0x10	8	read/ write	0x00	0x00
				RMINAR	分钟报警寄存器	0x12	8	read/ write	0x00	0x00
				BCNT1AR	二进制计数器1警报 Register	0x12	8	read/ write	0x00	0x00
				RHRAR	小时报警寄存器	0x14	8	read/ write	0x00	0x00
				BCNT2AR	二进制计数器2报警 Register	0x14	8	read/ write	0x00	0x00
				RWKAR	星期报警寄存器0x 16		8	read/ write	0x00	0x00
				BCNT3AR	二进制计数器3报警 Register	0x16	8	read/ write	0x00	0x00

Table 3.4 Register description (10 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
RTC	-	-	-	RDAYAR	Date Alarm Register	0x18	8	read/ write	0x00	0x00
				BCNT0AER	Binary Counter 0 Alarm Enable Register	0x18	8	read/ write	0x00	0x00
				RMONAR	Month Alarm Register	0x1A	8	read/ write	0x00	0x00
				BCNT1AER	Binary Counter 1 Alarm Enable Register	0x1A	8	read/ write	0x00	0x00
				RYRAR	Year Alarm Register	0x1C	16	read/ write	0x0000	0xFF00
				BCNT2AER	Binary Counter 2 Alarm Enable Register	0x1C	16	read/ write	0x0000	0xFF00
				RYRAREN	Year Alarm Enable Register	0x1E	8	read/ write	0x00	0x00
				BCNT3AER	Binary Counter 3 Alarm Enable Register	0x1E	8	read/ write	0x00	0x00
				RCR1	RTC Control Register 1	0x22	8	read/ write	0x00	0x0A
				RCR2	RTC Control Register 2	0x24	8	read/ write	0x00	0x0E
				RCR4	RTC Control Register 4	0x28	8	read/ write	0x00	0xFE
				RFRH	Frequency Register H	0x2A	16	read/ write	0x0000	0xFFFE
				RFRL	Frequency Register L	0x2C	16	read/ write	0x0000	0x0000
				RADJ	Time Error Adjustment Register	0x2E	8	read/ write	0x00	0x00
	3	0x2	0-2	RTCCR%s	Time Capture Control Register %s	0x40	8	read/ write	0x00	0x00
	3	0x10	0-2	RSECCP%s	Second Capture Register %s	0x52	8	read-only	0x00	0x00
	3	0x10	0-2	BCNT0CP%s	BCNT0 Capture Register %s	0x52	8	read-only	0x00	0x00
	3	0x10	0-2	RMINCP%s	Minute Capture Register %s	0x54	8	read-only	0x00	0x00
	3	0x10	0-2	BCNT1CP%s	BCNT1 Capture Register %s	0x54	8	read-only	0x00	0x00
	3	0x10	0-2	RHRCP%s	Hour Capture Register %s	0x56	8	read-only	0x00	0x00
	3	0x10	0-2	BCNT2CP%s	BCNT2 Capture Register %s	0x56	8	read-only	0x00	0x00
	3	0x10	0-2	RDAYCP%s	Date Capture Register %s	0x5A	8	read-only	0x00	0x00
	3	0x10	0-2	BCNT3CP%s	BCNT3 Capture Register %s	0x5A	8	read-only	0x00	0x00
	3	0x10	0-2	RMONCP%s	Month Capture Register %s	0x5C	8	read-only	0x00	0x00
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	read/ write	0xFF	0xFF
				WDTCR	WDT Control Register	0x02	16	read/ write	0x33F3	0xFFFF
				WDTSR	WDT Status Register	0x04	16	read/ write	0x0000	0xFFFF
				WDTRCR	WDT Reset Control Register	0x06	8	read/ write	0x80	0xFF
				WDTCSTPR	WDT Count Stop Control Register	0x08	8	read/ write	0x80	0xFF
				IWDTRR	IWDT Refresh Register	0x00	8	read/ write	0xFF	0xFF

Table 3.4 寄存器说明（25个中的10个）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
RTC	-	-	-	RDAYAR	日期报警寄存器	0x18	8	read/ write	0x00	0x00
				BCNT0AER	二进制计数器0报警启用注册	0x18	8	read/ write	0x00	0x00
				RMONAR	月报警寄存器	0x1A	8	read/ write	0x00	0x00
				BCNT1AER	二进制计数器1警报启用注册	0x1A	8	read/ write	0x00	0x00
				RYRAR	年报警寄存器	0x1C	16	read/ write	0x0000	0xFF00
				BCNT2AER	二进制计数器2报警启用注册	0x1C	16	read/ write	0x0000	0xFF00
				RYRAREN	年警报启用寄存器	0x1E	8	read/ write	0x00	0x00
				BCNT3AER	二进制计数器3报警启用注册	0x1E	8	read/ write	0x00	0x00
				RCR1	RTC控制寄存器1	0x22	8	read/ write	0x00	0x0A
				RCR2	RTC控制寄存器2	0x24	8	read/ write	0x00	0x0E
				RCR4	RTC控制寄存器4	0x28	8	read/ write	0x00	0xFE
				RFRH	频率寄存器H	0x2A	16	read/ write	0x0000	0xFFFE
				RFRL	频率寄存器L	0x2C	16	read/ write	0x0000	0x0000
				RADJ	时间误差调整 Register	0x2E	8	read/ write	0x00	0x00
	3	0x2	0-2	RTCCR%s	时间捕捉控制 Register %s	0x40	8	read/ write	0x00	0x00
	3	0x10	0-2	RSECCP%s	第二个捕获寄存器%s0x52		8	只读	0x00	0x00
	3	0x10	0-2	BCNT0CP%s	BCNT0捕捉寄存器%s0x52		8	只读	0x00	0x00
	3	0x10	0-2	RMINCP%s	分钟捕获寄存器%s	0x54	8	只读	0x00	0x00
	3	0x10	0-2	BCNT1CP%s	BCNT1捕获寄存器%s0x54		8	只读	0x00	0x00
	3	0x10	0-2	RHRCP%s	小时记录寄存器%s	0x56	8	只读	0x00	0x00
	3	0x10	0-2	BCNT2CP%s	BCNT2捕捉寄存器%s0x56		8	只读	0x00	0x00
	3	0x10	0-2	RDAYCP%s	日期捕获寄存器%s	0x5A	8	只读	0x00	0x00
	3	0x10	0-2	BCNT3CP%s	BCNT3捕捉寄存器%s0x5A		8	只读	0x00	0x00
	3	0x10	0-2	RMONCP%s	月份捕获寄存器%s	0x5C	8	只读	0x00	0x00
WDT	-	-	-	WDTRR	WDT刷新寄存器	0x00	8	read/ write	0xFF	0xFF
				WDTCR	WDT控制寄存器	0x02	16	read/ write	0x33F3	0xFFFF
				WDTSR	WDT状态寄存器	0x04	16	read/ write	0x0000	0xFFFF
				WDTRCR	WDT复位控制寄存器0x 06		8	read/ write	0x80	0xFF
				WDTCSTPR	WDT计数停止控制 Register	0x08	8	read/ write	0x80	0xFF
				IWDTRR	IWDT刷新寄存器	0x00	8	read/ write	0xFF	0xFF

Table 3.4 Register description (11 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
WDT	-	-	-	IWDTSR	IWDT Status Register	0x04	16	read/ write	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	read/ write	0x00	0xFF
				CACR1	CAC Control Register 1	0x01	8	read/ write	0x00	0xFF
				CACR2	CAC Control Register 2	0x02	8	read/ write	0x00	0xFF
				CAICR	CAC Interrupt Control Register	0x03	8	read/ write	0x00	0xFF
				CASTR	CAC Status Register	0x04	8	read-only	0x00	0xFF
				CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	read/ write	0x0000	0xFFFF
				CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	read/ write	0x0000	0xFFFF
				CACNTBR	CAC Counter Buffer Register	0x0A	16	read-only	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x00	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				MSTPCRC	Module Stop Control Register C	0x04	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				MSTPCRD	Module Stop Control Register D	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
CAN0	32	0x10	0-31	MB%s_ID	Mailbox Register	0x200	32	read/ write	0x00000000	0x00000000
	32	0x10	0-31	MB%s_DL	Mailbox Register	0x204	16	read/ write	0x0000	0x0000
	32	0x10	0-31	MB%s_D0	Mailbox Register	0x206	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D1	Mailbox Register	0x207	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D2	Mailbox Register	0x208	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D3	Mailbox Register	0x209	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D4	Mailbox Register	0x20A	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D5	Mailbox Register	0x20B	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D6	Mailbox Register	0x20C	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D7	Mailbox Register	0x20D	8	read/ write	0x00	0x00

Table 3.4 寄存器说明（25个中的11个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
WDT	-	-	-	IWDTSR	IWDT状态寄存器	0x04	16	read/ write	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC控制寄存器0	0x00	8	read/ write	0x00	0xFF
				CACR1	CAC控制寄存器1	0x01	8	read/ write	0x00	0xFF
				CACR2	CAC控制寄存器2	0x02	8	read/ write	0x00	0xFF
				CAICR	CAC中断控制 Register	0x03	8	read/ write	0x00	0xFF
				CASTR	CAC状态寄存器	0x04	8	只读	0x00	0xFF
				CAULVR	CAC上限值 设置寄存器	0x06	16	read/ write	0x0000	0xFFFF
				CALLVR	CAC下限值 设置寄存器	0x08	16	read/ write	0x0000	0xFFFF
				CACNTBR	CAC计数器缓冲寄存器0x	0A	16	只读	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	模块停止控制 Register B	0x00	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				MSTPCRC	模块停止控制 Register C	0x04	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				MSTPCRD	模块停止控制 Register D	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
CAN0	32	0x10	0-31	MB%s_ID	邮箱注册	0x200	32	read/ write	0x00000000	0x00000000
	32	0x10	0-31	MB%s_DL	邮箱注册	0x204	16	read/ write	0x0000	0x0000
	32	0x10	0-31	MB%s_D0	邮箱注册	0x206	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D1	邮箱注册	0x207	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D2	邮箱注册	0x208	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D3	邮箱注册	0x209	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D4	邮箱注册	0x20A	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D5	邮箱注册	0x20B	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D6	邮箱注册	0x20C	8	read/ write	0x00	0x00
	32	0x10	0-31	MB%s_D7	邮箱注册	0x20D	8	read/ write	0x00	0x00

Table 3.4 Register description (12 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CAN0	32	0x10	0-31	MB%s_TS	Mailbox Register	0x20E	16	read/ write	0x0000	0x0000
	8	0x4	0-7	MKR[%s]	Mask Register	0x400	32	read/ write	0x00000000	0x00000000
	2	0x4	0,1	FIDCR%s	FIFO Received ID Compare Registers	0x420	32	read/ write	0x00000000	0x00000000
	-	-	-	MKIVLR	Mask Invalid Register	0x428	32	read/ write	0x00000000	0x00000000
				MIER	Mailbox Interrupt Enable Register	0x42C	32	read/ write	0x00000000	0x00000000
				MIER_FIFO	Mailbox Interrupt Enable Register for FIFO Mailbox Mode	0x42C	32	read/ write	0x00000000	0x00000000
	32	0x1	0-31	MCTL_TX[%s]	Message Control Register for Transmit	0x820	8	read/ write	0x00	0xFF
	32	0x1	0-31	MCTL_RX[%s]	Message Control Register for Receive	0x820	8	read/ write	0x00	0xFF
	-	-	-	CTLR	Control Register	0x840	16	read/ write	0x0500	0xFFFF
				STR	Status Register	0x842	16	read-only	0x0500	0xFFFF
				BCR	Bit Configuration Register	0x844	32	read/ write	0x00000000	0xFFFFFFFF
				RFCR	Receive FIFO Control Register	0x848	8	read/ write	0x80	0xFF
				RFPCR	Receive FIFO Pointer Control Register	0x849	8	write-only	0x00	0x00
				TFCR	Transmit FIFO Control Register	0x84A	8	read/ write	0x80	0xFF
				TFPCR	Transmit FIFO Pointer Control Register	0x84B	8	write-only	0x00	0x00
				EIER	Error Interrupt Enable Register	0x84C	8	read/ write	0x00	0xFF
				EIFR	Error Interrupt Factor Judge Register	0x84D	8	read/ write	0x00	0xFF
				RECR	Receive Error Count Register	0x84E	8	read-only	0x00	0xFF
				TECR	Transmit Error Count Register	0x84F	8	read-only	0x00	0xFF
				ECSR	Error Code Store Register	0x850	8	read/ write	0x00	0xFF
				CSSR	Channel Search Support Register	0x851	8	read/ write	0x00	0x00
				MSSR	Mailbox Search Status Register	0x852	8	read-only	0x80	0xFF
				MSMR	Mailbox Search Mode Register	0x853	8	read/ write	0x00	0xFF
				TSR	Time Stamp Register	0x854	16	read-only	0x0000	0xFFFF
				AFSR	Acceptance Filter Support Register	0x856	16	read/ write	0x0000	0x0000
				TCR	Test Control Register	0x858	8	read/ write	0x00	0xFF
IIC0	-	-	-	ICCR1	I^2C Bus Control Register 1	0x00	8	read/ write	0x1F	0xFF
				ICCR2	I^2C Bus Control Register 2	0x01	8	read/ write	0x00	0xFF
				ICMR1	I^2C Bus Mode Register 1	0x02	8	read/ write	0x08	0xFF

Table 3.4 寄存器说明（25个中的12个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
CAN0	32	0x10	0-31	MB%s_TS	邮箱注册	0x20E	16	read/ write	0x0000	0x0000
	8	0x4	0-7	MKR[%s]	掩码寄存器	0x400	32	read/ write	0x00000000	0x00000000
	2	0x4	0,1	FIDCR%s	FIFO接收ID比较 Registers	0x420	32	read/ write	0x00000000	0x00000000
	-	-	-	MKIVLR	屏蔽无效寄存器	0x428	32	read/ write	0x00000000	0x00000000
				MIER	邮箱中断启用 Register	0x42C	32	read/ write	0x00000000	0x00000000
				MIER_FIFO	FIFO邮箱的邮箱中断使能寄存器 Mode	0x42C	32	read/ write	0x00000000	0x00000000
	32	0x1	0-31	MCTL_TX[%s]	用于发送的消息控制寄存器	0x820	8	read/ write	0x00	0xFF
	32	0x1	0-31	MCTL_RX[%s]	接收消息控制寄存器	0x820	8	read/ write	0x00	0xFF
	-	-	-	CTLR	控制寄存器	0x840	16	read/ write	0x0500	0xFFFF
				STR	状态寄存器	0x842	16	只读	0x0500	0xFFFF
				BCR	位配置寄存器	0x844	32	read/ write	0x00000000	0xFFFFFFFF
				RFCR	接收FIFO控制 Register	0x848	8	read/ write	0x80	0xFF
				RFPCR	接收FIFO指针 控制寄存器	0x849	8	只写	0x00	0x00
				TFCR	发送FIFO控制 Register	0x84A	8	read/ write	0x80	0xFF
				TFPCR	发送FIFO指针 控制寄存器	0x84B	8	只写	0x00	0x00
				EIER	错误中断使能 Register	0x84C	8	read/ write	0x00	0xFF
				EIFR	错误中断因素判断 Register	0x84D	8	read/ write	0x00	0xFF
				RECR	接收错误计数 Register	0x84E	8	只读	0x00	0xFF
				TECR	传输错误计数 Register	0x84F	8	只读	0x00	0xFF
				ECSR	错误代码存储寄存器	0x850	8	read/ write	0x00	0xFF
				CSSR	频道搜索支持 Register	0x851	8	read/ write	0x00	0x00
				MSSR	邮箱搜索状态 Register	0x852	8	只读	0x80	0xFF
				MSMR	邮箱搜索模式 Register	0x853	8	read/ write	0x00	0xFF
				TSR	时间戳寄存器	0x854	16	只读	0x0000	0xFFFF
				AFSR	接受过滤器支持 Register	0x856	16	read/ write	0x0000	0x0000
				TCR	测试控制寄存器	0x858	8	read/ write	0x00	0xFF
IIC0	-	-	-	ICCR1	I2C总线控制寄存器1	0x00	8	read/ write	0x1F	0xFF
				ICCR2	I2C总线控制寄存器2	0x01	8	read/ write	0x00	0xFF
				ICMR1	I2C总线模式寄存器1	0x02	8	read/ write	0x08	0xFF

Table 3.4 Register description (13 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
IIC0	-	-	-	ICMR2	I²C Bus Mode Register 2	0x03	8	read/ write	0x06	0xFF
				ICMR3	I²C Bus Mode Register 3	0x04	8	read/ write	0x00	0xFF
				ICFER	I²C Bus Function Enable Register	0x05	8	read/ write	0x72	0xFF
				ICSER	I²C Bus Status Enable Register	0x06	8	read/ write	0x09	0xFF
				ICIER	I²C Bus Interrupt Enable Register	0x07	8	read/ write	0x00	0xFF
				ICSR1	I²C Bus Status Register 1	0x08	8	read/ write	0x00	0xFF
				ICSR2	I²C Bus Status Register 2	0x09	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read/ write	0x00	0xFF
	-	-	-	ICBRL	I²C Bus Bit Rate Low-Level Register	0x10	8	read/ write	0xFF	0xFF
				ICBRH	I²C Bus Bit Rate High-Level Register	0x11	8	read/ write	0xFF	0xFF
				ICDRT	I²C Bus Transmit Data Register	0x12	8	read/ write	0xFF	0xFF
				ICDRR	I²C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF
				ICWUR	I²C Bus Wake Up Unit Register	0x16	8	read/ write	0x10	0xFF
				ICWUR2	I²C Bus Wake up Unit Register 2	0x17	8	read/ write	0xFD	0xFF
IIC1	-	-	-	ICCR1	I²C Bus Control Register 1	0x00	8	read/ write	0x1F	0xFF
				ICCR2	I²C Bus Control Register 2	0x01	8	read/ write	0x00	0xFF
				ICMR1	I²C Bus Mode Register 1	0x02	8	read/ write	0x08	0xFF
				ICMR2	I²C Bus Mode Register 2	0x03	8	read/ write	0x06	0xFF
				ICMR3	I²C Bus Mode Register 3	0x04	8	read/ write	0x00	0xFF
				ICFER	I²C Bus Function Enable Register	0x05	8	read/ write	0x72	0xFF
				ICSER	I²C Bus Status Enable Register	0x06	8	read/ write	0x09	0xFF
				ICIER	I²C Bus Interrupt Enable Register	0x07	8	read/ write	0x00	0xFF
				ICSR1	I²C Bus Status Register 1	0x08	8	read/ write	0x00	0xFF
				ICSR2	I²C Bus Status Register 2	0x09	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read/ write	0x00	0xFF
	-	-	-	ICBRL	I²C Bus Bit Rate Low-Level Register	0x10	8	read/ write	0xFF	0xFF
				ICBRH	I²C Bus Bit Rate High-Level Register	0x11	8	read/ write	0xFF	0xFF
				ICDRT	I²C Bus Transmit Data Register	0x12	8	read/ write	0xFF	0xFF

Table 3.4 寄存器说明（25个中的13个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
IIC0	-	-	-	ICMR2	I2C总线模式寄存器2	0x03	8	read/ write	0x06	0xFF
				ICMR3	I2C总线模式寄存器3	0x04	8	read/ write	0x00	0xFF
				ICFER	I2C总线功能使能 Register	0x05	8	read/ write	0x72	0xFF
				ICSER	I2C总线状态启用 Register	0x06	8	read/ write	0x09	0xFF
				ICIER	I2C总线中断使能 Register	0x07	8	read/ write	0x00	0xFF
				ICSR1	I2C总线状态寄存器1	0x08	8	read/ write	0x00	0xFF
				ICSR2	I2C总线状态寄存器2	0x09	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARL%s	从地址寄存器L%s0x0A		8	read/ write	0x00	0xFF
	3	0x2	0-2	SARU%s	从机地址寄存器U%s0x0B		8	read/ write	0x00	0xFF
	-	-	-	ICBRL	I2C总线比特率低电平 Register	0x10	8	read/ write	0xFF	0xFF
				ICBRH	I2C总线比特率高电平 Register	0x11	8	read/ write	0xFF	0xFF
				ICDRT	I2C总线传输数据 Register	0x12	8	read/ write	0xFF	0xFF
				ICDRR	I2C总线接收数据 Register	0x13	8	只读	0x00	0xFF
				ICWUR	I2C总线唤醒单元 Register	0x16	8	read/ write	0x10	0xFF
				ICWUR2	I2C总线唤醒单元 Register 2	0x17	8	read/ write	0xFD	0xFF
IIC1	-	-	-	ICCR1	I2C总线控制寄存器1	0x00	8	read/ write	0x1F	0xFF
				ICCR2	I2C总线控制寄存器2	0x01	8	read/ write	0x00	0xFF
				ICMR1	I2C总线模式寄存器1	0x02	8	read/ write	0x08	0xFF
				ICMR2	I2C总线模式寄存器2	0x03	8	read/ write	0x06	0xFF
				ICMR3	I2C总线模式寄存器3	0x04	8	read/ write	0x00	0xFF
				ICFER	I2C总线功能使能 Register	0x05	8	read/ write	0x72	0xFF
				ICSER	I2C总线状态启用 Register	0x06	8	read/ write	0x09	0xFF
				ICIER	I2C总线中断使能 Register	0x07	8	read/ write	0x00	0xFF
				ICSR1	I2C总线状态寄存器1	0x08	8	read/ write	0x00	0xFF
				ICSR2	I2C总线状态寄存器2	0x09	8	read/ write	0x00	0xFF
	3	0x2	0-2	SARL%s	从地址寄存器L%s0x0A		8	read/ write	0x00	0xFF
	3	0x2	0-2	SARU%s	从机地址寄存器U%s0x0B		8	read/ write	0x00	0xFF
	-	-	-	ICBRL	I2C总线比特率低电平 Register	0x10	8	read/ write	0xFF	0xFF
				ICBRH	I2C总线比特率高电平 Register	0x11	8	read/ write	0xFF	0xFF
				ICDRT	I2C总线传输数据 Register	0x12	8	read/ write	0xFF	0xFF

Table 3.4 Register description (14 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
IIC1	-	-	-	ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	read/write	0x00	0xFF
				DODIR	DOC Data Input Register	0x02	16	read/write	0x0000	0xFFFF
				DODSR	DOC Data Setting Register	0x04	16	read/write	0x0000	0xFFFF
ADC140	-	-	-	ADCSR	A/D Control Register	0x000	16	read/write	0x0000	0xFFFF
				ADANSA0	A/D Channel Select Register A0	0x004	16	read/write	0x0000	0xFFFF
				ADANSA1	A/D Channel Select Register A1	0x006	16	read/write	0x0000	0xFFFF
				ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	read/write	0x0000	0xFFFF
				ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	read/write	0x0000	0xFFFF
				ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	read/write	0x00	0xFF
				ADCER	A/D Control Extended Register	0x00E	16	read/write	0x0000	0xFFFF
				ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	read/write	0x0000	0xFFFF
				ADEXICR	A/D Conversion Extended Input Control Register	0x012	16	read/write	0x0000	0xFFFF
				ADANSB0	A/D Channel Select Register B0	0x014	16	read/write	0x0000	0xFFFF
				ADANSB1	A/D Channel Select Register B1	0x016	16	read/write	0x0000	0xFFFF
				ADDBLDR	A/D Data Duplication Register	0x018	16	read-only	0x0000	0xFFFF
				ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	read-only	0x0000	0xFFFF
				ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	read-only	0x0000	0xFFFF
				ADRD	A/D Self-Diagnosis Data Register	0x01E	16	read-only	0x0000	0xFFFF
	28	0x2	0-27	ADDR%s	A/D Data Register %s	0x020	16	read-only	0x0000	0xFFFF
	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	read/write	0x00	0xFF
				ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	read/write	0x0000	0xFFFF
				ADDBLDRA	A/D Data Duplexing Register A	0x084	16	read-only	0x0000	0xFFFF
				ADDBLDRB	A/D Data Duplexing Register B	0x086	16	read-only	0x0000	0xFFFF
				ADHVREFCNT	A/D High-Potential/Low-Potential Reference Voltage Control Register	0x08A	8	read/write	0x00	0xFF
				ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	read-only	0x00	0xFF
				ADCMPCR	A/D Compare Function Control Register	0x090	16	read/write	0x0000	0xFFFF

Table 3.4 寄存器说明（25中的14）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
IIC1	-	-	-	ICDRR	I2C总线接收数据 Register	0x13	8	只读	0x00	0xFF
DOC	-	-	-	DOCR	DOC控制寄存器	0x00	8	read/write	0x00	0xFF
				DODIR	DOC数据输入寄存器	0x02	16	read/write	0x0000	0xFFFF
				DODSR	DOC数据设置寄存器	0x04	16	read/write	0x0000	0xFFFF
ADC140	-	-	-	ADCSR	AD控制寄存器	0x000	16	read/write	0x0000	0xFFFF
				ADANSA0	AD通道选择寄存器 A0	0x004	16	read/write	0x0000	0xFFFF
				ADANSA1	AD通道选择寄存器 A1	0x006	16	read/write	0x0000	0xFFFF
				ADADS0	A/D-Converted Value Addition/Average Channel 选择寄存器0	0x008	16	read/write	0x0000	0xFFFF
				ADADS1	A/D-Converted Value Addition/Average Channel 选择寄存器1	0x00A	16	read/write	0x0000	0xFFFF
				ADADC	A/D-Converted Value Addition/Average Count 选择注册	0x00C	8	read/write	0x00	0xFF
				ADCER	AD控制扩展 Register	0x00E	16	read/write	0x0000	0xFFFF
				ADSTRGR	AD转换开始触发 选择注册	0x010	16	read/write	0x0000	0xFFFF
				ADEXICR	AD转换扩展 输入控制寄存器	0x012	16	read/write	0x0000	0xFFFF
				ADANSB0	AD通道选择寄存器 B0	0x014	16	read/write	0x0000	0xFFFF
				ADANSB1	AD通道选择寄存器 B1	0x016	16	read/write	0x0000	0xFFFF
				ADDBLDR	AD数据复制 Register	0x018	16	只读	0x0000	0xFFFF
				ADTSDR	AD温度传感器 数据寄存器	0x01A	16	只读	0x0000	0xFFFF
				ADOCDR	AD内部参考 电压数据寄存器	0x01C	16	只读	0x0000	0xFFFF
				ADRD	A/D Self-Diagnosis Data Register	0x01E	16	只读	0x0000	0xFFFF
	28	0x2	0-27	ADDR%s	AD数据寄存器%s	0x020	16	只读	0x0000	0xFFFF
	-	-	-	ADDISCR	AD断线检测 控制寄存器	0x07A	8	read/write	0x00	0xFF
				ADGSPCR	AD组扫描优先级 控制寄存器	0x080	16	read/write	0x0000	0xFFFF
				ADDBLDRA	AD数据双工寄存器 A	0x084	16	只读	0x0000	0xFFFF
				ADDBLDRB	AD数据双工寄存器 B	0x086	16	只读	0x0000	0xFFFF
				ADHVREFCNT	A/D High-Potential/Low-潜在参考电压 控制寄存器	0x08A	8	read/write	0x00	0xFF
				ADWINMON	AD比较功能 窗口AB状态监视器 Register	0x08C	8	只读	0x00	0xFF
				ADCMPCR	AD比较功能 控制寄存器	0x090	16	read/write	0x0000	0xFFFF

Table 3.4 Register description (15 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC140	-	-	-	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	read/ write	0x00	0xFF
				ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	read/ write	0x00	0xFF
				ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	read/ write	0x0000	0xFFFF
				ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	read/ write	0x0000	0xFFFF
				ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	read/ write	0x0000	0xFFFF
				ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	read/ write	0x0000	0xFFFF
				ADCMPDR0	A/D Compare Function Window A Lower-Side Level Setting Register	0x09C	16	read/ write	0x0000	0xFFFF
				ADCMPDR1	A/D Compare Function Window A Upper-Side Level Setting Register	0x09E	16	read/ write	0x0000	0xFFFF
				ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	read/ write	0x0000	0xFFFF
				ADCMPSR1	A/D Compare Function Window A Channel Status Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
				ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	read/ write	0x00	0xFF
				ADCMPBNSR	A/D Compare Function Window B Channel Selection Register	0x0A6	8	read/ write	0x00	0xFF
				ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	read/ write	0x0000	0xFFFF
				ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	read/ write	0x0000	0xFFFF
				ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	read/ write	0x00	0xFF
				ADSSTRL	A/D Sampling State Register L	0x0DD	8	read/ write	0x0D	0xFF
				ADSSTRT	A/D Sampling State Register T	0x0DE	8	read/ write	0x0D	0xFF
				ADSSTRO	A/D Sampling State Register O	0x0DF	8	read/ write	0x0D	0xFF
	5	0x1	4-6, 9, 10	ADSSTR%s	A/D Sampling State Register %s	0x0E0	8	read/ write	0x0D	0xFF
DAC12	-	-	-	DADR0	D/A Data Register 0	0x00	16	read/ write	0x0000	0xFFFF
				DACR	D/A Control Register	0x04	8	read/ write	0x1F	0xFF
				DADPR	DADR0 Format Select Register	0x05	8	read/ write	0x00	0xFF
				DAADSCR	D/A-A/D Synchronous Start Control Register	0x06	8	read/ write	0x00	0xFF

Table 3.4 寄存器说明（25个中的15个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
ADC140	-	-	-	ADCMPANSER	AD比较功能 窗口A扩展输入 选择注册	0x092	8	read/ write	0x00	0xFF
				ADCMPLER	AD比较功能窗口A扩展输入 比较条件 设置寄存器	0x093	8	read/ write	0x00	0xFF
				ADCMPANSR0	AD比较功能 窗口A通道选择 Register 0	0x094	16	read/ write	0x0000	0xFFFF
				ADCMPANSR1	AD比较功能 窗口A通道选择 Register 1	0x096	16	read/ write	0x0000	0xFFFF
				ADCMPLR0	AD比较功能窗口A比较 条件设置寄存器0	0x098	16	read/ write	0x0000	0xFFFF
				ADCMPLR1	AD比较功能窗口A比较 条件设置寄存器1	0x09A	16	read/ write	0x0000	0xFFFF
				ADCMPDR0	AD比较功能 窗口A下层 设置寄存器	0x09C	16	read/ write	0x0000	0xFFFF
				ADCMPDR1	AD比较功能 窗口A上层 设置寄存器	0x09E	16	read/ write	0x0000	0xFFFF
				ADCMPSR0	AD比较功能 窗口A通道状态 Register 0	0x0A0	16	read/ write	0x0000	0xFFFF
				ADCMPSR1	AD比较功能 窗口A通道状态 Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
				ADCMPSER	AD比较功能窗口A扩展输入 通道状态寄存器	0x0A4	8	read/ write	0x00	0xFF
				ADCMPBNSR	AD比较功能 窗口B通道选择 Register	0x0A6	8	read/ write	0x00	0xFF
				ADWINLLB	AD比较功能 窗口B下层 设置寄存器	0x0A8	16	read/ write	0x0000	0xFFFF
				ADWINULB	AD比较功能 窗口B上层 设置寄存器	0x0AA	16	read/ write	0x0000	0xFFFF
				ADCMPBSR	AD比较功能 窗口B状态寄存器	0x0AC	8	read/ write	0x00	0xFF
				ADSSTRL	AD采样状态寄存器 L	0x0DD	8	read/ write	0x0D	0xFF
				ADSSTRT	AD采样状态寄存器 T	0x0DE	8	read/ write	0x0D	0xFF
				ADSSTRO	AD采样状态寄存器 O	0x0DF	8	read/ write	0x0D	0xFF
	5	0x1	4-6, 9, 10	ADSSTR%s	AD采样状态寄存器%s	0x0E0	8	read/ write	0x0D	0xFF
DAC12	-	-	-	DADR0	DA数据寄存器0	0x00	16	read/ write	0x0000	0xFFFF
				DACR	DA控制寄存器	0x04	8	read/ write	0x1F	0xFF
				DADPR	DADR0格式选择 Register	0x05	8	read/ write	0x00	0xFF
				DAADSCR	DA-AD同步启动 控制寄存器	0x06	8	read/ write	0x00	0xFF

Table 3.4 Register description (16 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DAC12	-	-	-	DAVREFCR	D/A VREF Control Register	0x07	8	read/ write	0x00	0xFF
SCI0,1	-	-	-	SMR	Serial Mode Register (SCMR.SMIF = 0)	0x00	8	read/ write	0x00	0xFF
				SMR_SMCI	Serial mode register (SCMR.SMIF = 1)	0x00	8	read/ write	0x00	0xFF
				BRR	Bit Rate Register	0x01	8	read/ write	0xFF	0xFF
				SCR	Serial Control Register (SCMR.SMIF = 0)	0x02	8	read/ write	0x00	0xFF
				SCR_SMCI	Serial Control Register (SCMR.SMIF =1)	0x02	8	read/ write	0x00	0xFF
				TDR	Transmit Data Register	0x03	8	read/ write	0xFF	0xFF
				SSR	Serial Status Register(SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
				SSR_FIFO	Serial Status Register(SCMR.SMIF = 0 and FCR.FM=1)	0x04	8	read/ write	0x80	0xFD
				SSR_SMCI	Serial Status Register(SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
				RDR	Receive Data Register	0x05	8	read-only	0x00	0xFF
				SCMR	Smart Card Mode Register	0x06	8	read/ write	0xF2	0xFF
				SEMR	Serial Extended Mode Register	0x07	8	read/ write	0x00	0xFF
				SNFR	Noise Filter Setting Register	0x08	8	read/ write	0x00	0xFF
				SIMR1	I^2C Mode Register 1	0x09	8	read/ write	0x00	0xFF
				SIMR2	I^2C Mode Register 2	0x0A	8	read/ write	0x00	0xFF
				SIMR3	I^2C Mode Register 3	0x0B	8	read/ write	0x00	0xFF
				SISR	I^2C Status Register	0x0C	8	read-only	0x00	0xCB
				SPMR	SPI Mode Register	0x0D	8	read/ write	0x00	0xFF
				TDRHL	Transmit 9-bit Data Register	0x0E	16	read/ write	0xFFFF	0xFFFF
				FTDRHL	Transmit FIFO Data Register HL	0x0E	16	write-only	0xFFFF	0xFFFF
				FTDRH	Transmit FIFO Data Register H	0x0E	8	write-only	0xFF	0xFF
				FTDRL	Transmit FIFO Data Register L	0x0F	8	write-only	0xFF	0xFF
				RDRHL	Receive 9-bit Data Register	0x10	16	read-only	0x0000	0xFFFF
				FRDRHL	Receive FIFO Data Register HL	0x10	16	read-only	0x0000	0xFFFF
				FRDRH	Receive FIFO Data Register H	0x10	8	read-only	0x00	0xFF
				FRDRL	Receive FIFO Data Register L	0x11	8	read-only	0x00	0xFF
				MDDR	Modulation Duty Register	0x12	8	read/ write	0xFF	0xFF
				DCCR	Data Compare Match Control Register	0x13	8	read/ write	0x40	0xFF

Table 3.4 寄存器说明（25个中的16个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
DAC12	-	-	-	DAVREFCR	DAVREF控制寄存器	0x07	8	read/ write	0x00	0xFF
SCI0,1	-	-	-	SMR	串行模式寄存器(SCMR.SMIF=0)	0x00	8	read/ write	0x00	0xFF
				SMR_SMCI	串行模式寄存器(SCMR.SMIF=1)	0x00	8	read/ write	0x00	0xFF
				BRR	比特率寄存器	0x01	8	read/ write	0xFF	0xFF
				SCR	串行控制寄存器(SCMR.SMIF=0)	0x02	8	read/ write	0x00	0xFF
				SCR_SMCI	串行控制寄存器(SCMR.SMIF=1)	0x02	8	read/ write	0x00	0xFF
				TDR	发送数据寄存器	0x03	8	read/ write	0xFF	0xFF
				SSR	序列状态 Register(SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
				SSR_FIFO	序列状态 Register(SCMR.SMIF = 0 and FCR.FM=1)	0x04	8	read/ write	0x80	0xFD
				SSR_SMCI	序列状态 Register(SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
				RDR	接收数据寄存器	0x05	8	只读	0x00	0xFF
				SCMR	智能卡模式寄存器	0x06	8	read/ write	0xF2	0xFF
				SEMR	串行扩展模式 Register	0x07	8	read/ write	0x00	0xFF
				SNFR	噪声滤波器设置寄存器	0x08	8	read/ write	0x00	0xFF
				SIMR1	I2C模式寄存器1	0x09	8	read/ write	0x00	0xFF
				SIMR2	I2C模式寄存器2	0x0A	8	read/ write	0x00	0xFF
				SIMR3	I2C模式寄存器3	0x0B	8	read/ write	0x00	0xFF
				SISR	我2C状态寄存器	0x0C	8	只读	0x00	0xCB
				SPMR	SPI模式寄存器	0x0D	8	read/ write	0x00	0xFF
				TDRHL	发送9位数据寄存器	0x0E	16	read/ write	0xFFFF	0xFFFF
				FTDRHL	发送FIFO数据寄存器 HL	0x0E	16	只写	0xFFFF	0xFFFF
				FTDRH	发送FIFO数据寄存器 H	0x0E	8	只写	0xFF	0xFF
				FTDRL	发送FIFO数据寄存器 L	0x0F	8	只写	0xFF	0xFF
				RDRHL	接收9位数据寄存器	0x10	16	只读	0x0000	0xFFFF
				FRDRHL	接收FIFO数据寄存器 HL	0x10	16	只读	0x0000	0xFFFF
				FRDRH	接收FIFO数据寄存器 H	0x10	8	只读	0x00	0xFF
				FRDRL	接收FIFO数据寄存器 L	0x11	8	只读	0x00	0xFF
				MDDR	调制占空比寄存器	0x12	8	read/ write	0xFF	0xFF
				DCCR	数据比较匹配 控制寄存器	0x13	8	read/ write	0x40	0xFF

Table 3.4 Register description (17 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SCI0,1	-	-	-	FCR	FIFO Control Register	0x14	16	read/ write	0xF800	0xFFFF
				FDR	FIFO Data Count Register	0x16	16	read-only	0x0000	0xFFFF
				LSR	Line Status Register	0x18	16	read-only	0x0000	0xFFFF
				CDR	Compare Match Data Register	0x1A	16	read/ write	0x0000	0xFFFF
				SPTR	Serial Port Register	0x1C	8	read/ write	0x03	0xFF
SCI4,9	-	-	-	SMR	Serial Mode Register (SCMR.SMIF = 0)	0x00	8	read/ write	0x00	0xFF
				SMR_SMCI	Serial mode register (SCMR.SMIF = 1)	0x00	8	read/ write	0x00	0xFF
				BRR	Bit Rate Register	0x01	8	read/ write	0xFF	0xFF
				SCR	Serial Control Register (SCMR.SMIF = 0)	0x02	8	read/ write	0x00	0xFF
				SCR_SMCI	Serial Control Register (SCMR.SMIF =1)	0x02	8	read/ write	0x00	0xFF
				TDR	Transmit Data Register	0x03	8	read/ write	0xFF	0xFF
				SSR	Serial Status Register(SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
				SSR_SMCI	Serial Status Register(SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
				RDR	Receive Data Register	0x05	8	read-only	0x00	0xFF
				SCMR	Smart Card Mode Register	0x06	8	read/ write	0xF2	0xFF
				SEMR	Serial Extended Mode Register	0x07	8	read/ write	0x00	0xFF
				SNFR	Noise Filter Setting Register	0x08	8	read/ write	0x00	0xFF
				SIMR1	I^2C Mode Register 1	0x09	8	read/ write	0x00	0xFF
				SIMR2	I^2C Mode Register 2	0x0A	8	read/ write	0x00	0xFF
				SIMR3	I^2C Mode Register 3	0x0B	8	read/ write	0x00	0xFF
				SISR	I^2C Status Register	0x0C	8	read-only	0x00	0xCB
				SPMR	SPI Mode Register	0x0D	8	read/ write	0x00	0xFF
				TDRHL	Transmit 9-bit Data Register	0x0E	16	read/ write	0xFFFF	0xFFFF
				RDRHL	Receive 9-bit Data Register	0x10	16	read-only	0x0000	0xFFFF
				MDDR	Modulation Duty Register	0x12	8	read/ write	0xFF	0xFF
				DCCR	Data Compare Match Control Register	0x13	8	read/ write	0x40	0xFF
				CDR	Compare Match Data Register	0x1A	16	read/ write	0x0000	0xFFFF
				SPTR	Serial Port Register	0x1C	8	read/ write	0x03	0xFF
SPI0	-	-	-	SPCR	SPI Control Register	0x00	8	read/ write	0x00	0xFF

Table 3.4 寄存器说明（25个中的17个）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
SCI0,1	-	-	-	FCR	先进先出控制寄存器	0x14	16	read/ write	0xF800	0xFFFF
				FDR	FIFO数据计数寄存器	0x16	16	只读	0x0000	0xFFFF
				LSR	线路状态寄存器	0x18	16	只读	0x0000	0xFFFF
				CDR	比较匹配数据 Register	0x1A	16	read/ write	0x0000	0xFFFF
				SPTR	串口寄存器	0x1C	8	read/ write	0x03	0xFF
SCI4,9	-	-	-	SMR	串行模式寄存器(SCMR.SMIF=0)	0x00	8	read/ write	0x00	0xFF
				SMR_SMCI	串行模式寄存器(SCMR.SMIF=1)	0x00	8	read/ write	0x00	0xFF
				BRR	比特率寄存器	0x01	8	read/ write	0xFF	0xFF
				SCR	串行控制寄存器(SCMR.SMIF=0)	0x02	8	read/ write	0x00	0xFF
				SCR_SMCI	串行控制寄存器(SCMR.SMIF=1)	0x02	8	read/ write	0x00	0xFF
				TDR	发送数据寄存器	0x03	8	read/ write	0xFF	0xFF
				SSR	序列状态 Register(SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
				SSR_SMCI	序列状态 Register(SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
				RDR	接收数据寄存器	0x05	8	只读	0x00	0xFF
				SCMR	智能卡模式寄存器	0x06	8	read/ write	0xF2	0xFF
				SEMR	串行扩展模式 Register	0x07	8	read/ write	0x00	0xFF
				SNFR	噪声滤波器设置寄存器	0x08	8	read/ write	0x00	0xFF
				SIMR1	I2C模式寄存器1	0x09	8	read/ write	0x00	0xFF
				SIMR2	I2C模式寄存器2	0x0A	8	read/ write	0x00	0xFF
				SIMR3	I2C模式寄存器3	0x0B	8	read/ write	0x00	0xFF
				SISR	我2C状态寄存器	0x0C	8	只读	0x00	0xCB
				SPMR	SPI模式寄存器	0x0D	8	read/ write	0x00	0xFF
				TDRHL	发送9位数据寄存器	0x0E	16	read/ write	0xFFFF	0xFFFF
				RDRHL	接收9位数据寄存器	0x10	16	只读	0x0000	0xFFFF
				MDDR	调制占空比寄存器	0x12	8	read/ write	0xFF	0xFF
				DCCR	数据比较匹配 控制寄存器	0x13	8	read/ write	0x40	0xFF
				CDR	比较匹配数据 Register	0x1A	16	read/ write	0x0000	0xFFFF
				SPTR	串口寄存器	0x1C	8	read/ write	0x03	0xFF
SPI0	-	-	-	SPCR	SPI控制寄存器	0x00	8	read/ write	0x00	0xFF

Table 3.4 Register description (18 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SPI0	-	-	-	SSLP	SPI Slave Select Polarity Register	0x01	8	read/ write	0x00	0xFF
				SPPCR	SPI Pin Control Register	0x02	8	read/ write	0x00	0xFF
				SPSR	SPI Status Register	0x03	8	read/ write	0x20	0xFF
				SPDR	SPI Data Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				SPDR_HA	SPI Data Register (halfword access)	0x04	16	read/ write	0x0000	0xFFFF
				SPSCR	SPI Sequence Control Register	0x08	8	read/ write	0x00	0xFF
				SPSSR	SPI Sequence Status Register	0x09	8	read-only	0x00	0xFF
				SPBR	SPI Bit Rate Register	0x0A	8	read/ write	0xFF	0xFF
				SPDCR	SPI Data Control Register	0x0B	8	read/ write	0x00	0xFF
				SPCKD	SPI Clock Delay Register	0x0C	8	read/ write	0x00	0xFF
				SSLND	SPI Slave Select Negation Delay Register	0x0D	8	read/ write	0x00	0xFF
				SPND	SPI Next-Access Delay Register	0x0E	8	read/ write	0x00	0xFF
				SPCR2	SPI Control Register 2	0x0F	8	read/ write	0x00	0xFF
	8	0x2	0-7	SPCMD%s	SPI Command Register %s	0x10	16	read/ write	0x070D	0xFFFF
SPI1	-	-	-	SPCR	SPI Control Register	0x00	8	read/ write	0x00	0xFF
				SSLP	SPI Slave Select Polarity Register	0x01	8	read/ write	0x00	0xFF
				SPPCR	SPI Pin Control Register	0x02	8	read/ write	0x00	0xFF
				SPSR	SPI Status Register	0x03	8	read/ write	0x20	0xFF
				SPDR	SPI Data Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				SPDR_HA	SPI Data Register (halfword access)	0x04	16	read/ write	0x0000	0xFFFF
				SPBR	SPI Bit Rate Register	0x0A	8	read/ write	0xFF	0xFF
				SPDCR	SPI Data Control Register	0x0B	8	read/ write	0x00	0xFF
				SPCKD	SPI Clock Delay Register	0x0C	8	read/ write	0x00	0xFF
				SSLND	SPI Slave Select Negation Delay Register	0x0D	8	read/ write	0x00	0xFF
				SPND	SPI Next-Access Delay Register	0x0E	8	read/ write	0x00	0xFF
				SPCR2	SPI Control Register 2	0x0F	8	read/ write	0x00	0xFF
				SPCMD0	SPI Command Register 0	0x10	16	read/ write	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC Control Register0	0x00	8	read/ write	0x00	0xFF
				CRCCR1	CRC Control Register1	0x01	8	read/ write	0x00	0xFF
				CRCDIR	CRC Data Input Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.4 寄存器说明（25中的18）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
SPI0	-	-	-	SSLP	SPI从机选择极性 Register	0x01	8	read/ write	0x00	0xFF
				SPPCR	SPI引脚控制寄存器	0x02	8	read/ write	0x00	0xFF
				SPSR	SPI状态寄存器	0x03	8	read/ write	0x20	0xFF
				SPDR	SPI数据寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				SPDR_HA	SPI数据寄存器（半字访问）	0x04	16	read/ write	0x0000	0xFFFF
				SPSCR	SPI序列控制 Register	0x08	8	read/ write	0x00	0xFF
				SPSSR	SPI序列状态 Register	0x09	8	只读	0x00	0xFF
				SPBR	SPI比特率寄存器	0x0A	8	read/ write	0xFF	0xFF
				SPDCR	SPI数据控制寄存器	0x0B	8	read/ write	0x00	0xFF
				SPCKD	SPI时钟延迟寄存器	0x0C	8	read/ write	0x00	0xFF
				SSLND	SPI从机选择否定 延迟寄存器	0x0D	8	read/ write	0x00	0xFF
				SPND	SPI下一次访问延迟 Register	0x0E	8	read/ write	0x00	0xFF
				SPCR2	SPI控制寄存器2	0x0F	8	read/ write	0x00	0xFF
	8	0x2	0-7	SPCMD%s	SPI命令寄存器%s	0x10	16	read/ write	0x070D	0xFFFF
SPI1	-	-	-	SPCR	SPI控制寄存器	0x00	8	read/ write	0x00	0xFF
				SSLP	SPI从机选择极性 Register	0x01	8	read/ write	0x00	0xFF
				SPPCR	SPI引脚控制寄存器	0x02	8	read/ write	0x00	0xFF
				SPSR	SPI状态寄存器	0x03	8	read/ write	0x20	0xFF
				SPDR	SPI数据寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				SPDR_HA	SPI数据寄存器（半字访问）	0x04	16	read/ write	0x0000	0xFFFF
				SPBR	SPI比特率寄存器	0x0A	8	read/ write	0xFF	0xFF
				SPDCR	SPI数据控制寄存器	0x0B	8	read/ write	0x00	0xFF
				SPCKD	SPI时钟延迟寄存器	0x0C	8	read/ write	0x00	0xFF
				SSLND	SPI从机选择否定 延迟寄存器	0x0D	8	read/ write	0x00	0xFF
				SPND	SPI下一次访问延迟 Register	0x0E	8	read/ write	0x00	0xFF
				SPCR2	SPI控制寄存器2	0x0F	8	read/ write	0x00	0xFF
				SPCMD0	SPI命令寄存器0	0x10	16	read/ write	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC Control Register0	0x00	8	read/ write	0x00	0xFF
				CRCCR1	CRC Control Register1	0x01	8	read/ write	0x00	0xFF
				CRCDIR	CRC数据输入寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.4 Register description (19 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CRC	-	-	-	CRCDIR_BY	CRC Data Input Register (byte access)	0x04	8	read/ write	0x00	0xFF
				CRCDOR	CRC Data Output Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
				CRCDOR_HA	CRC Data Output Register (halfword access)	0x08	16	read/ write	0x0000	0xFFFF
				CRCDOR_BY	CRC Data Output Register (byte access)	0x08	8	read/ write	0x00	0xFF
				CRCSAR	Snoop Address Register	0x0C	16	read/ write	0x0000	0xFFFF
GPT320-3	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				GTSTR	General PWM Timer Software Start Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				GTSTP	General PWM Timer Software Stop Register	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x00000000	0xFFFFFFFF
				GTSSR	General PWM Timer Start Source Select Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
				GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read/ write	0x00000000	0xFFFFFFFF
				GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
				GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read/ write	0x00000000	0xFFFFFFFF
				GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
				GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read/ write	0x00000000	0xFFFFFFFF
				GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read/ write	0x00000000	0xFFFFFFFF
				GTCR	General PWM Timer Control Register	0x2C	32	read/ write	0x00000000	0xFFFFFFFF
				GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read/ write	0x00000001	0xFFFFFFFF
				GTIOR	General PWM Timer I/O Control Register	0x34	32	read/ write	0x00000000	0xFFFFFFFF
				GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
				GTST	General PWM Timer Status Register	0x3C	32	read/ write	0x00008000	0xFFFFFFFF
				GTBER	General PWM Timer Buffer Enable Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
				GTCNT	General PWM Timer Counter	0x48	32	read/ write	0x00000000	0xFFFFFFFF
				GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read/ write	0xFFFFFFFF	0xFFFFFFFF

Table 3.4 寄存器说明（25中的19）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
CRC	-	-	-	CRCDIR_BY	CRC数据输入寄存器（字节访问）	0x04	8	read/ write	0x00	0xFF
				CRCDOR	CRC数据输出寄存器	0x08	32	read/ write	0x00000000	0xFFFFFFFF
				CRCDOR_HA	CRC数据输出寄存器（半字访问）	0x08	16	read/ write	0x0000	0xFFFF
				CRCDOR_BY	CRC数据输出寄存器（字节访问）	0x08	8	read/ write	0x00	0xFF
				CRCSAR	窥探地址寄存器	0x0C	16	read/ write	0x0000	0xFFFF
GPT320-3	-	-	-	GTWP	通用PWM定时器写保护登记册	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				GTSTR	通用PWM定时器软件启动寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				GTSTP	通用PWM定时器软件停止寄存器	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCLR	通用PWM定时器软件清除寄存器	0x0C	32	只写	0x00000000	0xFFFFFFFF
				GTSSR	通用PWM定时器启动源选择寄存器	0x10	32	read/ write	0x00000000	0xFFFFFFFF
				GTPSR	通用PWM定时器停止源选择寄存器	0x14	32	read/ write	0x00000000	0xFFFFFFFF
				GTCSR	通用PWM定时器清零源选择寄存器	0x18	32	read/ write	0x00000000	0xFFFFFFFF
				GTUPSR	通用PWM定时器启动计数源选择Register	0x1C	32	read/ write	0x00000000	0xFFFFFFFF
				GTDNSR	通用PWM定时器停机计数源选择Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
				GTICASR	通用PWM定时器输入捕获源选择Register A	0x24	32	read/ write	0x00000000	0xFFFFFFFF
				GTICBSR	通用PWM定时器输入捕获源选择Register B	0x28	32	read/ write	0x00000000	0xFFFFFFFF
				GTCR	通用PWM定时器控制Register	0x2C	32	read/ write	0x00000000	0xFFFFFFFF
				GTUDDTYC	通用PWM定时器计数方向和占空比设置Register	0x30	32	read/ write	0x00000001	0xFFFFFFFF
				GTIOR	通用PWM定时器IO控制寄存器	0x34	32	read/ write	0x00000000	0xFFFFFFFF
				GTINTAD	通用PWM定时器中断输出设置Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
				GTST	通用PWM定时器状态Register	0x3C	32	read/ write	0x00008000	0xFFFFFFFF
				GTBER	通用PWM定时器缓冲器启用注册	0x40	32	read/ write	0x00000000	0xFFFFFFFF
				GTCNT	通用PWM定时器计数器0x48		32	read/ write	0x00000000	0xFFFFFFFF
				GTCCRA	通用PWM定时器比较捕获寄存器A	0x4C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRB	通用PWM定时器比较捕捉寄存器B	0x50	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRC	通用PWM定时器比较捕捉寄存器C	0x54	32	read/ write	0xFFFFFFFF	0xFFFFFFFF

Table 3.4 Register description (20 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT320-3	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTPR	General PWM Timer Cycle Setting Register	0x64	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read/ write	0x00000000	0xFFFFFFFF
				GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT164, 5, 8	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
				GTSTR	General PWM Timer Software Start Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
				GTSTP	General PWM Timer Software Stop Register	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
				GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x00000000	0xFFFFFFFF
				GTSSR	General PWM Timer Start Source Select Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
				GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read/ write	0x00000000	0xFFFFFFFF
				GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
				GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read/ write	0x00000000	0xFFFFFFFF
				GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
				GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read/ write	0x00000000	0xFFFFFFFF
				GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read/ write	0x00000000	0xFFFFFFFF
				GTCR	General PWM Timer Control Register	0x2C	32	read/ write	0x00000000	0xFFFFFFFF
				GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read/ write	0x00000001	0xFFFFFFFF
				GTIOR	General PWM Timer I/O Control Register	0x34	32	read/ write	0x00000000	0xFFFFFFFF
				GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
				GTST	General PWM Timer Status Register	0x3C	32	read/ write	0x00008000	0xFFFFFFFF
				GTBER	General PWM Timer Buffer Enable Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
				GTCNT	General PWM Timer Counter	0x48	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.4 寄存器说明（25之20）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GPT320-3	-	-	GTCCRE	通用PWM定时器比较捕捉寄存器E	0x58	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
			GTCCRD	通用PWM定时器比较捕捉寄存器D	0x5C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
			GTCCRF	通用PWM定时器比较捕捉寄存器F	0x60	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
			GTPR	通用PWM定时器周期设置寄存器	0x64	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
			GTPBR	通用PWM定时器周期设置缓冲寄存器	0x68	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
			GTDTCR	通用PWM定时器死机时间控制寄存器	0x88	32	read/ write	0x00000000	0xFFFFFFFF
			GTDVU	通用PWM定时器死机时间值寄存器U	0x8C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT164, 5, 8	-	-	GTWP	通用PWM定时器写保护登记册	0x00	32	read/ write	0x00000000	0xFFFFFFFF
			GTSTR	通用PWM定时器软件启动寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
			GTSTP	通用PWM定时器软件停止寄存器	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
			GTCLR	通用PWM定时器软件清除寄存器	0x0C	32	只写	0x00000000	0xFFFFFFFF
			GTSSR	通用PWM定时器启动源选择寄存器	0x10	32	read/ write	0x00000000	0xFFFFFFFF
			GTPSR	通用PWM定时器停止源选择寄存器	0x14	32	read/ write	0x00000000	0xFFFFFFFF
			GTCSR	通用PWM定时器清零源选择寄存器	0x18	32	read/ write	0x00000000	0xFFFFFFFF
			GTUPSR	通用PWM定时器启动计数源选择Register	0x1C	32	read/ write	0x00000000	0xFFFFFFFF
			GTDNSR	通用PWM定时器停机计数源选择Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
			GTICASR	通用PWM定时器输入捕获源选择Register A	0x24	32	read/ write	0x00000000	0xFFFFFFFF
			GTICBSR	通用PWM定时器输入捕获源选择Register B	0x28	32	read/ write	0x00000000	0xFFFFFFFF
			GTCR	通用PWM定时器控制Register	0x2C	32	read/ write	0x00000000	0xFFFFFFFF
			GTUDDTYC	通用PWM定时器计数方向和占空比设置Register	0x30	32	read/ write	0x00000001	0xFFFFFFFF
			GTIOR	通用PWM定时器IO控制寄存器	0x34	32	read/ write	0x00000000	0xFFFFFFFF
			GTINTAD	通用PWM定时器中断输出设置Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
			GTST	通用PWM定时器状态Register	0x3C	32	read/ write	0x00008000	0xFFFFFFFF
			GTBER	通用PWM定时器缓冲器启用注册	0x40	32	read/ write	0x00000000	0xFFFFFFFF
			GTCNT	通用PWM定时器计数器0x48		32	read/ write	0x00000000	0xFFFFFFFF

Table 3.4 Register description (21 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT164, 5, 8	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTPR	General PWM Timer Cycle Setting Register	0x64	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read/ write	0x00000000	0xFFFFFFFF
				GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read/ write	0x0000FFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	Output Phase Switching Control Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
KINT	-	-	-	KRCTL	Key Return Control Register	0x00	8	read/ write	0x00	0xFF
				KRF	Key Return Flag Register	0x04	8	read/ write	0x00	0xFF
				KRM	Key Return Mode Register	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR0	CTSU Control Register 0	0x00	8	read/ write	0x00	0xFF
				CTSUCR1	CTSU Control Register 1	0x01	8	read/ write	0x00	0xFF
				CTSUSDPRS	CTSU Synchronous Noise Reduction Setting Register	0x02	8	read/ write	0x00	0xFF
				CTSUSST	CTSU Sensor Stabilization Wait Control Register	0x03	8	read/ write	0x00	0xFF
				CTSUMCH0	CTSU Measurement Channel Register 0	0x04	8	read/ write	0x3F	0xFF
				CTSUMCH1	CTSU Measurement Channel Register 1	0x05	8	read/ write	0x3F	0xFF
				CTSUCHAC0	CTSU Channel Enable Control Register 0	0x06	8	read/ write	0x00	0xFF
				CTSUCHAC1	CTSU Channel Enable Control Register 1	0x07	8	read/ write	0x00	0xFF
				CTSUCHAC2	CTSU Channel Enable Control Register 2	0x08	8	read/ write	0x00	0xFF
				CTSUCHAC3	CTSU Channel Enable Control Register 3	0x09	8	read/ write	0x00	0xFF
				CTSUCHAC4	CTSU Channel Enable Control Register 4	0x0A	8	read/ write	0x00	0xFF
				CTSUCHTRC0	CTSU Channel Transmit/ Receive Control Register 0	0x0B	8	read/ write	0x00	0xFF
				CTSUCHTRC1	CTSU Channel Transmit/ Receive Control Register 1	0x0C	8	read/ write	0x00	0xFF

Table 3.4 寄存器描述（21的25）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GPT164, 5, 8	-	-	-	GTCCRA	通用PWM定时器比较捕获寄存器A	0x4C	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRB	通用PWM定时器比较捕捉寄存器B	0x50	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRC	通用PWM定时器比较捕捉寄存器C	0x54	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRE	通用PWM定时器比较捕捉寄存器E	0x58	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRD	通用PWM定时器比较捕捉寄存器D	0x5C	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTCCRF	通用PWM定时器比较捕捉寄存器F	0x60	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTPR	通用PWM定时器周期设置寄存器	0x64	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTPBR	通用PWM定时器周期设置缓冲寄存器	0x68	32	read/ write	0x0000FFFF	0xFFFFFFFF
				GTDTCR	通用PWM定时器死机时间控制寄存器	0x88	32	read/ write	0x00000000	0xFFFFFFFF
				GTDVU	通用PWM定时器死机时间值寄存器U	0x8C	32	read/ write	0x0000FFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	输出相位切换控制寄存器	0x00	32	read/ write	0x00000000	0xFFFFFFFF
KINT	-	-	-	KRCTL	密钥返回控制寄存器	0x00	8	read/ write	0x00	0xFF
				KRF	键返回标志寄存器	0x04	8	read/ write	0x00	0xFF
				KRM	键返回模式寄存器	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR0	CTSU控制寄存器0	0x00	8	read/ write	0x00	0xFF
				CTSUCR1	CTSU控制寄存器1	0x01	8	read/ write	0x00	0xFF
				CTSUSDPRS	CTSU同步降噪设置寄存器	0x02	8	read/ write	0x00	0xFF
				CTSUSST	CTSU传感器稳定等待控制寄存器	0x03	8	read/ write	0x00	0xFF
				CTSUMCH0	CTSU Measurement 通道寄存器0	0x04	8	read/ write	0x3F	0xFF
				CTSUMCH1	CTSU Measurement 通道寄存器1	0x05	8	read/ write	0x3F	0xFF
				CTSUCHAC0	CTSU通道启用控制寄存器0	0x06	8	read/ write	0x00	0xFF
				CTSUCHAC1	CTSU通道启用控制寄存器1	0x07	8	read/ write	0x00	0xFF
				CTSUCHAC2	CTSU通道启用控制寄存器2	0x08	8	read/ write	0x00	0xFF
				CTSUCHAC3	CTSU通道启用控制寄存器3	0x09	8	read/ write	0x00	0xFF
				CTSUCHAC4	CTSU通道启用控制寄存器4	0x0A	8	read/ write	0x00	0xFF
				CTSUCHTRC0	CTSU Channel Transmit/ 接收控制寄存器0	0x0B	8	read/ write	0x00	0xFF
				CTSUCHTRC1	CTSU Channel Transmit/ 接收控制寄存器1	0x0C	8	read/ write	0x00	0xFF

Table 3.4 Register description (22 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CTSU	-	-	-	CTSUCHTRC2	CTSU Channel Transmit/ Receive Control Register 3	0x0D	8	read/ write	0x00	0xFF
				CTSUCHTRC3	CTSU Channel Transmit/ Receive Control Register 3	0x0E	8	read/ write	0x00	0xFF
				CTSUCHTRC4	CTSU Channel Transmit/ Receive Control Register 4	0x0F	8	read/ write	0x00	0xFF
				CTSUDCLKC	CTSU High-Pass Noise Reduction Control Register	0x10	8	read/ write	0x00	0xFF
				CTSUST	CTSU Status Register	0x11	8	read/ write	0x00	0xFF
				CTSUSSC	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	0x12	16	read/ write	0x0000	0xFFFF
				CTSUSO0	CTSU Sensor Offset Register 0	0x14	16	read/ write	0x0000	0xFFFF
				CTSUSO1	CTSU Sensor Offset Register 1	0x16	16	read/ write	0x0000	0xFFFF
				CTSUSC	CTSU Sensor Counter	0x18	16	read-only	0x0000	0xFFFF
				CTSURC	CTSU Reference Counter	0x1A	16	read-only	0x0000	0xFFFF
				CTSUERRS	CTSU Error Status Register	0x1C	16	read-only	0x0000	0xFFFF
SLCDC	-	-	-	LCDM0	LCD Mode Register 0	0x000	8	read/ write	0x00	0xFF
				LCDM1	LCD Mode Register 1	0x001	8	read/ write	0x00	0xFF
				LCDC0	LCD Clock Control Register 0	0x002	8	read/ write	0x00	0xFF
	9	0x1	6, 9, 11, 12, 20, 23, 49, 52, 53	SEG%s	LCD Display Data Register %s	0x100	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGT	AGT Counter Register	0x00	16	read/ write	0xFFFF	0xFFFF
				AGTCMA	AGT Compare Match A Register	0x02	16	read/ write	0xFFFF	0xFFFF
				AGTCMB	AGT Compare Match B Register	0x04	16	read/ write	0xFFFF	0xFFFF
				AGTCR	AGT Control Register	0x08	8	read/ write	0x00	0xFF
				AGTMR1	AGT Mode Register 1	0x09	8	read/ write	0x00	0xFF
				AGTMR2	AGT Mode Register 2	0x0A	8	read/ write	0x00	0xFF
				AGTIOC	AGT I/O Control Register	0x0C	8	read/ write	0x00	0xFF
				AGTISR	AGT Event Pin Select Register	0x0D	8	read/ write	0x00	0xFF
				AGTCMSR	AGT Compare Match Function Select Register	0x0E	8	read/ write	0x00	0xFF
				AGTIOSEL	AGT Pin Select Register	0x0F	8	read/ write	0x00	0xFF

Table 3.4 寄存器说明（22之25）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
CTSU	-	-	-	CTSUCHTRC2	CTSU Channel Transmit/ 接收控制寄存器3	0x0D	8	read/ write	0x00	0xFF
				CTSUCHTRC3	CTSU Channel Transmit/ 接收控制寄存器3	0x0E	8	read/ write	0x00	0xFF
				CTSUCHTRC4	CTSU Channel Transmit/ 接收控制寄存器4	0x0F	8	read/ write	0x00	0xFF
				CTSUDCLKC	CTSU High-Pass Noise 减少控制寄存器	0x10	8	read/ write	0x00	0xFF
				CTSUST	CTSU状态寄存器	0x11	8	read/ write	0x00	0xFF
				CTSUSSC	CTSU High-Pass Noise 还原光谱 扩散控制寄存器	0x12	16	read/ write	0x0000	0xFFFF
				CTSUSO0	CTSU传感器偏移 Register 0	0x14	16	read/ write	0x0000	0xFFFF
				CTSUSO1	CTSU传感器偏移 Register 1	0x16	16	read/ write	0x0000	0xFFFF
				CTSUSC	CTSU传感器计数器	0x18	16	只读	0x0000	0xFFFF
				CTSURC	CTSU参考计数器	0x1A	16	只读	0x0000	0xFFFF
				CTSUERRS	CTSU错误状态寄存器	0x1C	16	只读	0x0000	0xFFFF
SLCDC	-	-	-	LCDM0	LCD模式寄存器0	0x000	8	read/ write	0x00	0xFF
				LCDM1	LCD模式寄存器1	0x001	8	read/ write	0x00	0xFF
				LCDC0	LCD时钟控制寄存器0	0x002	8	read/ write	0x00	0xFF
	9	0x1	6, 9, 11, 12, 20, 23, 49, 52, 53	SEG%s	LCD显示数据寄存器%s	0x100	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGT	AGT计数器寄存器	0x00	16	read/ write	0xFFFF	0xFFFF
				AGTCMA	AGT比较匹配A Register	0x02	16	read/ write	0xFFFF	0xFFFF
				AGTCMB	AGT比较匹配B Register	0x04	16	read/ write	0xFFFF	0xFFFF
				AGTCR	AGT控制寄存器	0x08	8	read/ write	0x00	0xFF
				AGTMR1	AGT模式寄存器1	0x09	8	read/ write	0x00	0xFF
				AGTMR2	AGT模式寄存器2	0x0A	8	read/ write	0x00	0xFF
				AGTIOC	AGTIO控制寄存器	0x0C	8	read/ write	0x00	0xFF
				AGTISR	AGT事件引脚选择 Register	0x0D	8	read/ write	0x00	0xFF
				AGTCMSR	AGT比较匹配 功能选择寄存器	0x0E	8	read/ write	0x00	0xFF
				AGTIOSEL	AGT引脚选择寄存器	0x0F	8	read/ write	0x00	0xFF

Table 3.4 Register description (23 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ACMPLP	-	-	-	COMPMDR	ACMPLP Mode Setting Register	0x00	8	read/ write	0x00	0xFF
				COMPFIR	ACMPLP Filter Control Register	0x01	8	read/ write	0x00	0xFF
				COMPOCR	ACMPLP Output Control Register	0x02	8	read/ write	0x00	0xFF
ACMPLP	-	-	-	COMPSEL0	Comparator Input Select Register	0x04	8	read/ write	0x11	0xFF
				COMPSEL1	Comparator Reference Voltage Select Register	0x05	8	read/ write	0x91	0xFF
OPAMP	-	-	-	AMPMC	Operational Amplifier Mode Control Register	0x08	8	read/ write	0x00	0xFF
				AMPTRM	Operational Amplifier Trigger Mode Control Register	0x09	8	read/ write	0x00	0xFF
				AMPTRS	Operational Amplifier Activation Trigger Select Register	0x0A	8	read/ write	0x00	0xFF
				AMPC	Operational Amplifier Control Register	0x0B	8	read/ write	0x00	0xFF
				AMPMON	Operational Amplifier Monitor Register	0x0C	8	read-only	0x00	0xFF

Table 3.4 寄存器描述（23的25）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
ACMPLP	-	-	-	COMPMDR	ACMPLP模式设置 Register	0x00	8	read/ write	0x00	0xFF
				COMPFIR	ACMPLP滤波器控制 Register	0x01	8	read/ write	0x00	0xFF
				COMPOCR	ACMPLP输出控制 Register	0x02	8	read/ write	0x00	0xFF
ACMPLP	-	-	-	COMPSEL0	比较器输入选择 Register	0x04	8	read/ write	0x11	0xFF
				COMPSEL1	比较器参考电压选择寄存器	0x05	8	read/ write	0x91	0xFF
OPAMP	-	-	-	AMPMC	运算放大器模式 控制寄存器	0x08	8	read/ write	0x00	0xFF
				AMPTRM	运算放大器触发器 模式控制寄存器	0x09	8	read/ write	0x00	0xFF
				AMPTRS	运算放大器 激活触发器选择 Register	0x0A	8	read/ write	0x00	0xFF
				AMPC	运算放大器控制 Register	0x0B	8	read/ write	0x00	0xFF
				AMPMON	运算放大器 监控寄存器	0x0C	8	只读	0x00	0xFF

Table 3.4 Register description (24 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBFS	-	-	-	SYSCFG	System Configuration Control Register	0x000	16	read/ write	0x0000	0xFFFF
				SYSSTS0	System Configuration Status Register 0	0x004	16	read-only	0x0000	0x0000
				DVSTCTR0	Device State Control Register 0	0x008	16	read/ write	0x0000	0xFFFF
				CFIFO	CFIFO Port Register	0x014	16	read/ write	0x0000	0xFFFF
				CFIFOL	CFIFO Port Register L	0x014	8	read/ write	0x00	0xFF
				D0FIFO	D0FIFO Port Register	0x018	16	read/ write	0x0000	0xFFFF
				D0FIFOL	D0FIFO Port Register L	0x018	8	read/ write	0x00	0xFF
				D1FIFO	D1FIFO Port Register	0x01C	16	read/ write	0x0000	0xFFFF
				D1FIFOL	D1FIFO Port Register L	0x01C	8	read/ write	0x00	0xFF
				CFIFOSEL	CFIFO Port Select Register	0x020	16	read/ write	0x0000	0xFFFF
				CFIFOCTR	CFIFO Port Control Register	0x022	16	read/ write	0x0000	0xFFFF
				D0FIFOSEL	D0FIFO Port Select Register	0x028	16	read/ write	0x0000	0xFFFF
				D0FIFOCTR	D0FIFO Port Control Register	0x02A	16	read/ write	0x0000	0xFFFF
				D1FIFOSEL	D1FIFO Port Select Register	0x02C	16	read/ write	0x0000	0xFFFF
				D1FIFOCTR	D1FIFO Port Control Register	0x02E	16	read/ write	0x0000	0xFFFF
				INTENB0	Interrupt Enable Register 0	0x030	16	read/ write	0x0000	0xFFFF
				INTENB1	Interrupt Enable Register 1	0x032	16	read/ write	0x0000	0xFFFF
				BRDYENB	BRDY Interrupt Enable Register	0x036	16	read/ write	0x0000	0xFFFF
				NRDYENB	NRDY Interrupt Enable Register	0x038	16	read/ write	0x0000	0xFFFF
				BEMPENB	BEMP Interrupt Enable Register	0x03A	16	read/ write	0x0000	0xFFFF
				SOFCFG	SOF Output Configuration Register	0x03C	16	read/ write	0x0000	0xFFFF
				INTSTS0	Interrupt Status Register 0	0x040	16	read/ write	0x0000	0xFF7F

Table 3.4 注册说明（24篇，共25篇）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
USBFS	-	-	-	SYSCFG	系统配置控制寄存器	0x000	16	read/ write	0x0000	0xFFFF
				SYSSTS0	系统配置状态Register 0	0x004	16	只读	0x0000	0x0000
				DVSTCTR0	设备状态控制Register 0	0x008	16	read/ write	0x0000	0xFFFF
				CFIFO	CFIFO端口寄存器	0x014	16	read/ write	0x0000	0xFFFF
				CFIFOL	CFIFO端口寄存器L	0x014	8	read/ write	0x00	0xFF
				D0FIFO	D0FIFO端口寄存器	0x018	16	read/ write	0x0000	0xFFFF
				D0FIFOL	D0FIFO端口寄存器L	0x018	8	read/ write	0x00	0xFF
				D1FIFO	D1FIFO端口寄存器	0x01C	16	read/ write	0x0000	0xFFFF
				D1FIFOL	D1FIFO端口寄存器L	0x01C	8	read/ write	0x00	0xFF
				CFIFOSEL	CFIFO端口选择寄存器	0x020	16	read/ write	0x0000	0xFFFF
				CFIFOCTR	CFIFO端口控制寄存器0x	022	16	read/ write	0x0000	0xFFFF
				D0FIFOSEL	D0FIFO端口选择寄存器0x	028	16	read/ write	0x0000	0xFFFF
				D0FIFOCTR	D0FIFO端口控制Register	0x02A	16	read/ write	0x0000	0xFFFF
				D1FIFOSEL	D1FIFO端口选择寄存器0x	02C	16	read/ write	0x0000	0xFFFF
				D1FIFOCTR	D1FIFO端口控制Register	0x02E	16	read/ write	0x0000	0xFFFF
				INTENB0	中断使能寄存器0	0x030	16	read/ write	0x0000	0xFFFF
				INTENB1	中断使能寄存器1	0x032	16	read/ write	0x0000	0xFFFF
				BRDYENB	BRDY中断使能Register	0x036	16	read/ write	0x0000	0xFFFF
				NRDYENB	NRDY中断使能Register	0x038	16	read/ write	0x0000	0xFFFF
				BEMPENB	BEMP中断使能Register	0x03A	16	read/ write	0x0000	0xFFFF
				SOFCFG	SOF输出配置Register	0x03C	16	read/ write	0x0000	0xFFFF
				INTSTS0	中断状态寄存器0	0x040	16	read/ write	0x0000	0xFF7F

Table 3.4 Register description (25 of 25)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBFS	-	-	-	INTSTS1	Interrupt Status Register 1	0x042	16	read/ write	0x0000	0xFFFF
				BRDYSTS	BRDY Interrupt Status Register	0x046	16	read/ write	0x0000	0xFFFF
				NRDYSTS	NRDY Interrupt Status Register	0x048	16	read/ write	0x0000	0xFFFF
				BEMPSTS	BEMP Interrupt Status Register	0x04A	16	read/ write	0x0000	0xFFFF
				FRMNUM	Frame Number Register	0x04C	16	read/ write	0x0000	0xFFFF
				USBREQ	USB Request Type Register	0x054	16	read/ write	0x0000	0xFFFF
				USBVAL	USB Request Value Register	0x056	16	read/ write	0x0000	0xFFFF
				USBINDX	USB Request Index Register	0x058	16	read/ write	0x0000	0xFFFF
				USBLENG	USB Request Length Register	0x05A	16	read/ write	0x0000	0xFFFF
				DCPCFG	DCP Configuration Register	0x05C	16	read/ write	0x0000	0xFFFF
				DCPMAXP	DCP Maximum Packet Size Register	0x05E	16	read/ write	0x0040	0xFFFF
				DCPCTR	DCP Control Register	0x060	16	read/ write	0x0040	0xFFFF
				PIPESEL	Pipe Window Select Register	0x064	16	read/ write	0x0000	0xFFFF
				PIPECFG	Pipe Configuration Register	0x068	16	read/ write	0x0000	0xFFFF
				PIPEMAXP	Pipe Maximum Packet Size Register	0x06C	16	read/ write	0x0000	0xFFBF
				PIPEPERI	Pipe Cycle Control Register	0x06E	16	read/ write	0x0000	0xFFFF
	5	0x002	1-5	PIPE%sCTR	Pipe %s Control Register	0x070	16	read/ write	0x0000	0xFFFF
	4	0x002	6-9	PIPE%sCTR	Pipe %s Control Register	0x07A	16	read/ write	0x0000	0xFFFF
	5	0x004	1-5	PIPE%sTRE	Pipe %s Transaction Counter Enable Register	0x090	16	read/ write	0x0000	0xFFFF
	5	0x004	1-5	PIPE%sTRN	Pipe %s Transaction Counter Register	0x092	16	read/ write	0x0000	0xFFFF
	-	-	-	USBBCCTRL0	BC Control Register 0	0x0B0	16	read/ write	0x0000	0xFFFF
				USBMC	USB Module Control Register	0x0CC	16	read/ write	0x0002	0xFFFF
	6	0x002	0-5	DEVADD%s	Device Address %s Configuration Register	0x0D0	16	read/ write	0x0000	0xFFFF
DAC8	2	0x01	0,1	DACS%s	D/A Conversion Value Setting Register %s	0x00	8	read/ write	0x00	0xFF
	-	-	-	DAM	D/A Converter Mode Register	0x03	8	read/ write	0x00	0xFF
FLCN	-	-	-	DFLCTL	Data flash Control Register	0x90	8	read/ write	0x00	0xFF
TSN	-	-	-	TSCDRH	Temperature Sensor Calibration Data Register H	0x229	8	read-only	0x00	0x00
				TSCDRL	Temperature Sensor Calibration Data Register L	0x228	8	read-only	0x00	0x00

Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc = Address increment between two simultaneous registers of a register array in the address map

Table 3.4 寄存器说明（25个中的25个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
USBFS	-	-	-	INTSTS1	中断状态寄存器1	0x042	16	read/ write	0x0000	0xFFFF
				BRDYSTS	BRDY中断状态 Register	0x046	16	read/ write	0x0000	0xFFFF
				NRDYSTS	NRDY中断状态 Register	0x048	16	read/ write	0x0000	0xFFFF
				BEMPSTS	BEMP中断状态 Register	0x04A	16	read/ write	0x0000	0xFFFF
				FRMNUM	帧号寄存器	0x04C	16	read/ write	0x0000	0xFFFF
				USBREQ	USB请求类型寄存器	0x054	16	read/ write	0x0000	0xFFFF
				USBVAL	USB请求值寄存器0x 056		16	read/ write	0x0000	0xFFFF
				USBINDX	USB请求索引寄存器0x 058		16	read/ write	0x0000	0xFFFF
				USBLENG	USB请求长度 Register	0x05A	16	read/ write	0x0000	0xFFFF
				DCPCFG	DCP配置寄存器	0x05C	16	read/ write	0x0000	0xFFFF
				DCPMAXP	DCP最大数据包大小 Register	0x05E	16	read/ write	0x0040	0xFFFF
				DCPCTR	DCP控制寄存器	0x060	16	read/ write	0x0040	0xFFFF
				PIPESEL	管道窗口选择寄存器0x 064		16	read/ write	0x0000	0xFFFF
				PIPECFG	管道配置寄存器	0x068	16	read/ write	0x0000	0xFFFF
				PIPEMAXP	管道最大数据包大小 Register	0x06C	16	read/ write	0x0000	0xFFBF
				PIPEPERI	管道循环控制寄存器	0x06E	16	read/ write	0x0000	0xFFFF
	5	0x002	1-5	PIPE%sCTR	管道%s控制寄存器	0x070	16	read/ write	0x0000	0xFFFF
	4	0x002	6-9	PIPE%sCTR	管道%s控制寄存器	0x07A	16	read/ write	0x0000	0xFFFF
	5	0x004	1-5	PIPE%sTRE	管道%s事务 计数器使能寄存器	0x090	16	read/ write	0x0000	0xFFFF
	5	0x004	1-5	PIPE%sTRN	管道%s事务 计数器寄存器	0x092	16	read/ write	0x0000	0xFFFF
	-	-	-	USBBCCTRL0	BC控制寄存器0	0x0B0	16	read/ write	0x0000	0xFFFF
				USBMC	USB模块控制 Register	0x0CC	16	read/ write	0x0002	0xFFFF
	6	0x002	0-5	DEVADD%s	设备地址%s 配置寄存器	0x0D0	16	read/ write	0x0000	0xFFFF
DAC8	2	0x01	0,1	DACS%s	DA转化价值 设置寄存器%s	0x00	8	read/ write	0x00	0xFF
	-	-	-	DAM	DA转换器模式 Register	0x03	8	read/ write	0x00	0xFF
FLCN	-	-	-	DFLCTL	数据闪存控制寄存器	0x90	8	read/ write	0x00	0xFF
TSN	-	-	-	TSCDRH	温度感应器 校准数据寄存器H	0x229	8	只读	0x00	0x00
				TSCDRL	温度感应器 校准数据寄存器L	0x228	8	只读	0x00	0x00

外设名称=外设名称
Dim=寄存器数组中的元素数
Diminc=地址映射中寄存器阵列的两个同时寄存器之间的地址增量

Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Access = Register access rights:
Read-only: Read access is permitted. Write operations have undefined results.
Write-only: Write access is permitted. Read operations have undefined results.
Read/write: Both read and write accesses are permitted. Writes affect the state of the register and reads return a value related to the register.
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

暗淡索引=替换寄存器名称中的%s占位符的子字符串
寄存器名称=寄存器名称描述=寄
存器描述
地址偏移量=相对于寄存器外设定义的基地址的寄存器地址
大小=寄存器的位宽
访问=注册访问权限：
只读：允许读访问。写操作有未定义的结果。只写：允许写访问。读取操作具
有未定义的结果。
读写：允许读写访问。写入会影响寄存器的状态，读取会返回与寄存器相关的值。复位值=寄存器的默认复位值

复位掩码=标识哪些寄存器位具有定义的复位值

修订记录

Revision History	RA4W1 Group User's Manual

Rev.	Date	Chapter	Description
1.00	Mar 31, 2020	-	First release

修订记录	RA4W1组用户手册

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