Datasheet

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Renesas RA6M3 Group

Datasheet

32-Bit MCU
Renesas Advanced (RA) Family
Renesas RA6 Series

Datasheet

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Datasheet

瑞萨电子高级(RA)系列32位MCU
Renesas RA6 Series

RA6M3 Group

Datasheet

Leading performance 120-MHz Arm® Cortex®-M4 core, up to 2-MB code flash memory, 640-KB SRAM, Graphics LCD Controller, 2D Drawing Engine, Capacitive Touch Sensing Unit, Ethernet MAC Controller with IEEE 1588 PTP, USB 2.0 High-Speed, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

■ Memory
- Up to 2-MB code flash memory (40 MHz zero wait states)
- 64-KB data flash memory (125,000 erase/write cycles)
- Up to 640-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity
- Ethernet MAC Controller (ETHERC)
- Ethernet DMA Controller (EDMAC)
- Ethernet PTP Controller (EPTPC)
- USB 2.0 High-Speed (USBHS) module
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver with voltage regulator
- Serial Communications Interface (SCI) with FIFO × 10
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 3
- Controller Area Network (CAN) × 2
- Serial Sound Interface Enhanced (SSIE) × 2
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External address space
  - 8-bit or 16-bit bus space is selectable per area
  - SDRAM support

■ Analog
- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Graphics LCD Controller (GLCDC)
- JPEG codec
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Parallel Data Capture Unit (PDC)

■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General-Purpose I/O Ports
- Up to 133 input/output pins
  - Up to 9 CMOS input
  - Up to 124 CMOS input/output
    - Up to 21 input/output 5 V tolerant
    - Up to 18 high current (20 mA)

■ Operating Voltage
- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 176-pin BGA (13 mm × 13 mm, 0.8 mm pitch)
  - 145-pin LGA (7 mm × 7 mm, 0.5 mm pitch)
- Ta = -40°C to +105°C
  - 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

RA6M3 Group

Datasheet

领先的性能120-MHzArm®Cortex®-M4内核、高达2-MB代码闪存、640-KBSRAM、图形LCD控制器、2D绘图引擎、电容式触摸传感单元、具有IEEE1588PTP、USB2.0的以太网MAC控制器

高速、USB2.0全速、SDHI、QuadSPI、安全和安全功能以及高级模拟。

Features

■带浮点单元(FPU)的ArmCortex-M4内核带DSP指令集的Armv7E-M架构最大工作频率：120MHz支持4GB地址空间片上调试系统：JTAG、SWD和ETM　边界扫描和Arm内存保护单元(ArmMPU)

■系统和电源管理　低功耗模式　支持日历和VBATT的实时时钟(RTC)　事件链接控制器(ELC)　DMA控制器(DMAC)×8　数据传输控制器(DTC)　按键中断功能(KINT)　上电复位　具有电压设置的低电压检测(LVD)

■ Memory
高达2MB代码闪存（40MHz零等待状态）　64KB数据闪存（125 000个擦除写入周期）　高达640KBSRAM　闪存高速缓存(FCACHE)　内存保护单元(MPU)　内存镜像功能(MMF)　128位唯一ID

■安全和加密　AES128192256　3DESARC4　SHA1SHA224SHA256MD5　GHASH　RSADSAECC　真随机数生成器(TRNG)

■ Connectivity
以太网MAC控制器(ETHERC)　以太网DMA控制器(EDMAC)　以太网PTP控制器(EPTPC)　USB2.0高速(USBHS)模块

带有稳压器的片上收发器符合USB电池充电规范1.2　USB2.0全速(USBFS)模块

带稳压器的片上收发器带FIFO的串行通信接口(SCI)×10串行外设接口(SPI)×2I2C总线接口(IIC)×3控制器局域网(CAN)×2串行声音增强型接口(SSIE)×2　SDMMC主机接口(SDHI)×2　四路串行外设接口(QSPI)　IrDA接口　采样率转换器(SRC)　外部地址空间

■人机界面(HMI)　图形LCD控制器(GLCDC)　JPEG编解码器　2D绘图引擎(DRW)　电容式触摸传感单元(CTSU)　并行数据采集单元(PDC)

■多个时钟源

主时钟振荡器(MOSC)(8至24MHz)　副时钟振荡器(SOSC)(32.768kHz)　高速片上振荡器(HOCO)(161820MHz)　中速片上振荡器(MOCO)(8MHz)　低速片上振荡器(LOCO)(32.768kHz)　IWDT专用片上振荡器(15kHz)　HOCOMOCOLOCO的时钟微调功能　时钟输出支持

每个区域可选择8位或16位总线空间SDRAM支持

■通用IO端口　多达133个输入输出引脚
多达9个CMOS输入多达124个CMOS输入输出多达21个输入输出5V耐受多达18个高电流(20mA)

■ Analog
12位模数转换器(ADC12)，每个具有3个采样和保持电路×2　12位模数转换器(DAC12)×2　高速模拟比较器(ACMPHS)×6　可编程增益放大器(PGA)×6　温度传感器(TSN)

■工作电压　VCC：2.7至3.6V

■工作温度和封装　Ta=−40°C至+85°C

■ Timers
通用PWM定时器32位增强型高分辨率(GPT32EH)×4　通用PWM定时器32位(GPT32E)×4　通用PWM定时器32位(GPT32)×6　异步通用定时器(AGT)×2　看门狗定时器(WDT)

176引脚BGA（13毫米×13毫米，0.8毫米间距）145引脚LGA（7毫米×7毫米，0.5毫米间距）　Ta=−40°C至+105°C
- 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
- 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
- 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

■ Safety
SRAM中的纠错码(ECC)　SRAM奇偶校验错误检查　闪存区域保护　ADC自诊断功能　时钟频率精度测量电路(CAC)　循环冗余校验(CRC)计算器　数据操作电路(DOC)　端口GPT(POEG)的输出使能　独立看门狗定时器(IWDT)　GPIO回读电平检测　寄存器写保护　主振荡器停止检测　非法内存访问

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz, with the following features:

- Up to 2-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	• Maximum operating frequency: up to 120 MHz • Arm Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions. • SysTick timer: - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 2-MB code flash memory. See section 55, Flash Memory in User's Manual.
Data flash memory	64-KB data flash memory. See section 55, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). The first 32 KB in SRAM0 provides error correction capability using ECC. Parity check is performed for other areas. See section 53, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 54, Standby SRAM in User's Manual.

1. Overview

MCU集成了多个系列的软件和基于Arm®引脚兼容的32位内核，它们共享同一组瑞萨外围设备可促进设计可扩展性和高效的基于平台的产品开发。

该系列中的MCU包含一个运行频率高达120MHz的高性能ArmCortex®-M4内核，具有以下特性：

- 高达2MB的代码闪存
- 640-KB SRAM
- 图形LCD控制器(GLCDC)
- 2D绘图引擎(DRW)
- 电容式触控感应单元(CTSU)
- 具有IEEE1588PTP、USBFS、USBHS、SDMMC主机接口的以太网MAC控制器(ETHERC)
- 四路串行外设接口(QSPI)
- 安全和安全功能
- 模拟外设。

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M4内核	最大工作频率：高达120MHz ArmCortex-M4内核：修订版：r0p1-01rel0ARMv7E-M架构配置文件符合ANSIIEEEStd754-2008的单精度浮点单元。 Arm内存保护单元（ArmMPU）： ARMv7ProtectedMemorySystemArchitecture8保护区域。 SysTick计时器： 由SYSTICCLK(LOCO)或ICLK驱动。

Table 1.2 Memory

Feature	功能说明
代码闪存	最大2MB代码闪存。请参阅用户手册中的第55节，闪存。
数据闪存	64KB数据闪存。请参阅用户手册中的第55节，闪存。
内存镜像功能(MMF)	内存镜像功能(MMF)可配置为将代码闪存中的目标应用程序映像加载地址镜像到23位未使用的内存空间（内存镜像空间地址）中的应用程序映像链接地址。您的应用程序代码已开发并链接到从该MMF目标地址运行。应用程序代码不需要知道它存储在代码闪存中的加载位置。请参阅用户手册中的第5节，内存镜像功能(MMF)。
Option-setting memory	选项设置存储器确定复位后MCU的状态。见第7节，用户手册中的选项设置内存。
SRAM	具有奇偶校验位或纠错码(ECC)的片上高速SRAM。SRAM0中的前32KB使用ECC提供纠错能力。对其他区域执行奇偶校验。请参阅用户手册中的第53节，SRAM。
Standby SRAM	可以在深度软件待机模式下保留数据的片上SRAM。见第54节，备用用户手册中的SRAM。

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • Independent watchdog timer reset • Watchdog timer reset • Deep software standby reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种工作模式：单片机模式SCI或USB启动模式。请参阅用户手册中的第3节操作模式。
Resets	14次复位： RES引脚复位 上电复位 电压监控器0复位 电压监控器1复位 电压监控器2复位 独立看门狗定时器复位 看门狗定时器复位 深度软件待机复位 SRAM奇偶校验错误复位 SRAMECC错误复位 总线主MPU错误复位 总线从属MPU错误复位 堆栈指针错误复位 软件复位。请参阅用户手册中的第6节，重置。
低电压检测(LVD)	低电压检测(LVD)功能监控输入到VCC引脚的电压电平，并且可以使用软件程序选择检测电平。请参阅用户手册中的第8节，低电压检测(LVD)。
Clocks	主时钟振荡器(MOSC) 子时钟振荡器(SOSC) 高速片上振荡器(HOCO) 中速片上振荡器(MOCO) 低速片上振荡器(LOCO) PLL频率合成器 IWDT专用片上振荡器 时钟输出支持。请参阅用户手册中的第9节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在用作测量基准的时钟（测量基准时钟）生成的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据是否脉冲数在允许范围内。当测量完成或测量参考时钟在时间内产生的脉冲数不在允许范围内时，将产生中断请求。请参阅用户手册中的第10节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到NVICDTC模块和DMAC模块。ICU还控制NMI中断。请参阅用户手册中的第14节，中断控制器单元(ICU)。
按键中断功能(KINT)	通过设置按键返回模式寄存器(KRM)并向按键中断输入引脚输入上升沿或下降沿，可以生成按键中断。请参阅用户手册中的第21节，按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗，例如设置时钟分频器、控制EBCLK输出、控制SDCLK 输出、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参阅用户手册中的第11节，低功耗模式。
电池备份功能	提供电池备份功能，由电池部分供电。电池供电区域包括RTC、SOSC、备份存储器以及VCC和VBATT之间的切换。请参阅用户手册中的第12节"电池备份功能"。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。请参见用户手册中的第13节，寄存器写保护。
内存保护单元(MPU)	提供四个内存保护单元(MPU)和一个CPU堆栈指针监控功能用于内存保护。请参阅用户手册中的第16节，内存保护单元(MPU)。

Table 1.3 System (2 of 2)

Feature	Functional description
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.6 External bus interface

Feature	Functional description
External buses	• CS area (EXBIU): Connected to the external devices (external memory interface) • SDRAM area (EXBIU): Connected to the SDRAM (external memory interface) • QSPI area (EXBIUT2): Connected to the QSPI (external device interface).

Table 1.7 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General-Purpose Timer (AGT)	The Asynchronous General-Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT). in User's Manual.

Table 1.3 系统(2之2)

Feature	功能说明
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，下溢可能会产生不可屏蔽的中断或中断。可以设置一个允许刷新周期来刷新计数器，作为检测系统何时失控的条件。请参阅用户手册中的第27节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。它可用于复位MCU或为定时器下溢生成不可屏蔽中断或中断。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。这 IWDT可以在复位、下溢、刷新错误或寄存器中的计数值刷新时自动触发。请参阅用户手册中的第28节，独立看门狗定时器(IWDT)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的中断请求作为事件信号，将它们连接到不同的模块，实现模块之间的直接交互，无需CPU干预。请参阅用户手册中的第19节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅用户手册中的第18节，数据传输控制器(DTC)。
DMA Controller (DMAC)	提供了一个8通道DMA控制器(DMAC)模块，用于在没有CPU的情况下传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。请参阅用户手册中的第17节，DMA控制器(DMAC)。

Table 1.6 外部总线接口

Feature	功能说明
外部总线	CS区（EXBIU）：连接到外部设备（外部存储器接口） SDRAM区（EXBIU）：连接到SDRAM（外部存储器接口） QSPI区（EXBIUT2）：连接到QSPI（外部设备接口）。

Table 1.7 计时器(1of2)

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有14个通道的32位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参阅用户手册中的第23节，通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	使用PortOutputEnableforGPT(POEG)功能将通用PWM定时器(GPT)输出引脚置于输出禁用状态。请参阅用户手册中的第22节，GPT(POEG)的端口输出启用。
Asynchronous General-Purpose Timer (AGT)	异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参见第25节，异步通用定时器(AGT)。在用户手册中。

Table 1.7 Timers (2 of 2)

Feature	Functional description
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI) in User's Manual.
IrDA interface	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface in User's Manual.
I^2C bus interface (IIC)	The 3-channel I^2C bus interface (IIC) conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 36, I2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I^2S 2ch, 4ch, 6ch, 8ch, WS Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface Enhanced (SSIE) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI) in User's Manual.
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.7 计时器（2个中的2个）

Feature	功能说明
实时时钟(RTC)	实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，由寄存器设置控制。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。 二进制计数模式可用于公历（西方）以外的日历。 请参阅用户手册中的第26节，实时时钟(RTC)。

Table 1.8 通信接口（2个中的1个）

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)可配置为五个异步和同步串行接口： 异步接口（UART和异步通信接口适配器(ACIA)） 8位时钟同步接口 简单IIC（仅限主机） 简单SPI 智能卡接口。智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。每个SCI都有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。请参阅用户手册中的第34节，串行通信接口(SCI)。
IrDA interface	IrDA接口与基于IrDA（InfraredDataAssociation）标准1.0的SCI1协同发送和接收IrDA数据通信波形。请参阅用户手册中的第35节，IrDA接口。
I2C总线接口(IIC)	3通道I2C总线接口(IIC)符合并提供NXPI2C（内部集成电路）总线接口功能的子集。请参阅用户手册中的第36节，I2C总线接口(IIC)。
串行外设接口(SPI)	两个独立的串行外围接口(SPI)通道能够与多个处理器和外围设备进行高速、全双工同步串行通信。请参阅用户手册中的第38节，串行外设接口(SPI)。
串行声音接口增强(SSIE)	串行声音接口增强(SSIE)外设提供与数字音频设备接口的功能，用于通过串行总线传输I2S2ch、4ch、6ch、8ch、WSContinue单声道TDM音频数据。SSIE支持高达50MHz的音频时钟频率，并可作为从属或主接收器、发送器或收发器运行，以适应各种应用。SSIE在接收器和发送器中包含32级FIFO缓冲区，并支持中断和DMA驱动的数据接收和发送。请参阅用户手册中的第41节，增强的串行声音接口(SSIE)。
四路串行外设接口(QSPI)	QuadSerialPeripheralInterface(QSPI)是一种存储器控制器，用于连接串行具有SPI兼容接口的ROM（非易失性存储器，例如串行闪存、串行EEPROM或串行FeRAM）。请参阅用户手册中的第39节，四通道串行外设接口(QSPI)。
控制器局域网(CAN)模块	控制器局域网(CAN)模块提供了在电磁噪声应用中使用基于消息的协议在多个从机和主机之间接收和传输数据的功能。CAN模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。请参阅用户手册中的第37节，控制器局域网(CAN)模块。
USB2.0全速(USBFS)模块	USB2.0全速(USBFS)模块可以作为主机控制器或设备控制器运行。 该模块支持全速和低速（仅限主机控制器）传输，如通用串行总线规范2.0。该模块有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，最多可提供10个管道。可以根据用于通信的外围设备或根据您的系统为管道1到9分配任何端点编号。请参阅用户手册中的第32节，USB 2.0全速模块(USBFS)。

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
USB 2.0 High-Speed (USBHS) module	The USB 2.0 High-Speed (USBHS) module can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in the Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS) in User's Manual.
Ethernet MAC with IEEE 1588 PTP (ETHERC)	One-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard. The EPTPC is composed of: • Synchronization Frame Processing unit (SYNFP0) • A Statistical Time Correction Algorithm unit (STCA). Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC) in User's Manual.
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	Up to two successive approximation 12-bit A/D Converters (ADC12) are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 11 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 47, 12-Bit A/D Converter (ADC12) in User's Manual.
12-bit D/A Converter (DAC12)	The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 48, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 49, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 50, High-Speed Analog Comparator (ACMPHS) in User's Manual.

Table 1.8 通信接口（2个中的2个）

Feature	功能说明
USB2.0高速(USBHS)模块	USB2.0高速(USBHS)模块可用作主机控制器或设备控制器。作为主机控制器，USBHS支持通用串行总线规范2.0中定义的高速传输、全速传输和低速传输。作为设备控制器，USBHS支持通用串行总线规范2.0中定义的高速传输和全速传输。USBHS有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USBHS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或您的通信系统，可以将任何端点编号分配给管道1到9。请参阅用户手册中的第33节，USB2.0高速模块(USBHS)。
具有IEEE1588PTP(ETHERC)的以太网MAC	符合以太网IEEE802.3媒体访问控制(MAC)层协议的单通道以太网MAC控制器(ETHERC)。一个ETHERC通道提供一个通道 MAC层接口，将MCU连接到物理层LSI(PHY-LSI)，允许发送和接收符合以太网和IEEE802.3标准的帧。ETHERC连接到以太网DMA控制器(EDMAC)，因此可以在不使用CPU的情况下传输数据。为了处理设备之间的定时和同步，以太网PTP控制器(EPTPC)的片上精确时间协议(PTP)模块应用了IEEE1588-20082.0版标准中定义的PTP。EPTPC由以下部分组成：•同步帧处理单元(SYNFP0)•统计时间校正算法单元(STCA)。将EPTPC与片上以太网MAC控制器(ETHERC)和用于PTP以太网控制器(PTPEDMAC)的DMA控制器结合使用。参见第29节，以太网MAC 用户手册中的控制器(ETHERC)。
SDMMC主机接口(SDHI)	SDHI和多媒体卡(MMC)接口模块提供将各种外部存储卡连接到MCU所需的功能。SDHI支持1位和4位总线，用于连接支持SD、SDHC和SDXC格式的存储卡。在开发符合SD规范的主机设备时，您必须遵守SD主机辅助产品许可协议(SDHALA)。MMC接口支持提供eMMC4.51（JEDEC标准JESD84-B451）器件访问的1位、4位和8位MMC总线。该接口还提供向后兼容性并支持高速SDR传输模式。请参阅用户手册中的第43节，SDMMC主机接口(SDHI)。

Table 1.9 Analog

Feature	功能说明
12-bit A/D Converter (ADC12)	最多提供两个逐次逼近型12位模数转换器(ADC12)。在单元0中，最多可选择13个模拟输入通道。在单元1中，可以选择多达11个模拟输入通道、温度传感器输出和内部参考电压进行转换。AD转换精度可从12位、10位和8位转换中选择，从而可以在生成数字值时优化速度和分辨率之间的折衷。请参阅用户手册中的第47节，12位模数转换器(ADC12)。
12-bit D/A Converter (DAC12)	12位DA转换器(DAC12)转换数据并包括一个输出放大器。请参阅用户手册中的第48节，12位DA转换器(DAC12)。
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压呈线性关系。输出电压提供给ADC12进行转换，也可供最终应用使用。请参阅用户手册中的第49节，温度传感器(TSN)。
高速模拟比较器(ACMPHS)	高速模拟比较器(ACMPHS)将测试电压与参考电压进行比较，并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（例如DAC12输出和内部参考电压）以及带有或不带有内部PGA的外部源提供给比较器。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。请参阅用户手册中的第50节，高速模拟比较器(ACMPHS)。

Table 1.10 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 51, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

Table 1.11 Graphics

Feature	Functional description
Graphics LCD Controller (GLCDC)	The Graphics LCD Controller (GLCDC) provides multiple functions and supports various data formats and panels. Key GLCDC features include: • GPX bus master function for accessing graphics data • Superimposition of three planes (single-color background plane, graphic 1-plane, and graphic 2-plane) • Support for many types of 32-bit or 16-bit per pixel graphics data and 8-bit, 4-bit, or 1-bit LUT data format • Digital interface signal output supporting a video image size of WVGA or greater. See section 58, Graphics LCD Controller (GLCDC) in User's Manual.
2D Drawing Engine (DRW)	The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write. See section 56, 2D Drawing Engine (DRW) in User's Manual.
JPEG codec	The JPEG incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 57, JPEG Codec (JPEG) in User's Manual.
Parallel Data Capture (PDC) unit	One Parallel Data Capture (PDC) unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data, such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC) in User's Manual.

Table 1.12 Data processing (1 of 2)

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator in User's Manual.

Table 1.10 人机界面

Feature	功能说明
电容式触控感应单元(CTSU)	电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围，因此手指不会直接接触电极。请参阅用户手册中的第51节，电容式触摸感应单元(CTSU)。

Table 1.11 Graphics

Feature	功能说明
图形LCD控制器(GLCDC)	图形LCD控制器(GLCDC)提供多种功能并支持各种数据格式和面板。主要GLCDC功能包括： 用于访问图形数据的GPX总线主控功能 三个平面的叠加（单色背景平面、图形1平面和图形2平面）支持多种32位或16位每像素图形数据和8位、4位或1位LUT数据格式 支持WVGA或更大视频图像大小的数字接口信号输出。请参阅用户手册中的第58节，图形LCD控制器(GLCDC)。
2D绘图引擎(DRW)	2D绘图引擎(DRW)提供了灵活的功能，可以支持几乎任何对象几何形状，而不是仅绑定到一些特定的几何形状，例如线条、三角形或圆形。每个对象的边缘都可以独立模糊或抗锯齿。在对象的边界框上从左到右和从上到下以每个时钟一个像素执行光栅化。在某些情况下，DRW还可以从下到上进行光栅化以优化性能。此外，还可以使用优化方法来避免边界框的许多空像素的光栅化。到对象边缘的距离由边界框的每个像素的一组边缘方程计算。这些边缘方程可以组合起来描述整个物体。如果像素在对象内部，则选择它进行渲染。如果它在外面，它就会被丢弃。如果它在边缘，则可以选择与像素到最近边缘的距离成比例的alpha值以进行抗锯齿。每个被选择用于渲染的像素都可以被纹理化。可以通过通用光栅操作方法对四个通道中的每一个独立地修改得到的aRGB四元组。然后可以将aRGB四元组与DRW的多种混合模式之一混合。DRW提供两个输入（纹理读取和帧缓冲区读取）和一个输出（帧缓冲区写入）。内部颜色格式始终为aRGB(8888)。来自输入的颜色格式在读取时转换为内部格式，并在写入时进行转换。请参阅用户手册中的第56节，2D绘图引擎(DRW)。
JPEG编解码器	JPEG包含符合JPEG基线压缩和解压缩标准的JPEG编解码器。这提供了图像数据的高速压缩和JPEG数据的高速解码。请参阅用户手册中的第57节，JPEG编解码器(JPEG)。
并行数据采集(PDC)单元	提供一个并行数据采集(PDC)单元，用于与外部IO设备（包括图像传感器）通信，以及传输并行数据，例如通过DTC或DMAC从外部IO设备输出的图像到片上SRAM和外部地址空间（CS和SDRAM区域）。请参阅用户手册中的第44节，并行数据采集单元(PDC)。

Table 1.12 数据处理(1of2)

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种生成CRC的多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅用户手册中的第40节，循环冗余校验(CRC)计算器。

Table 1.12 Data processing (2 of 2)

Feature	Functional description
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 52, Data Operation Circuit (DOC) in User's Manual.
Sampling Rate Converter (SRC)	The Sampling Rate Converter (SRC) converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 42, Sampling Rate Converter (SRC) in User's Manual.

Table 1.13 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and ECC. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5 - 128-bit unique ID. See section 46, Secure Cryptographic Engine (SCE7) in User's Manual.

Table 1.12 数据处理（2之2）

Feature	功能说明
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。见第52节， 用户手册中的数据操作电路(DOC)。
采样率转换器(SRC)	采样率转换器(SRC)转换各种音频解码器（如WMA、MP3和AAC）产生的数据的采样率。支持16位立体声和单声道数据。请参阅用户手册中的第42节，采样率转换器(SRC)。

Table 1.13 Security

Feature	功能说明
安全加密引擎7(SCE7)	• Security algorithms: 对称算法：AES、3DES和ARC4非对称算法：RSA 、DSA和ECC。 其他支持功能： TRNG（真随机数生成器）哈希值生成：SHA1、SHA224、SHA256、GHASH和MD5128位唯一ID。请参阅用户手册中的第46节，安全加密引擎(SCE7)。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

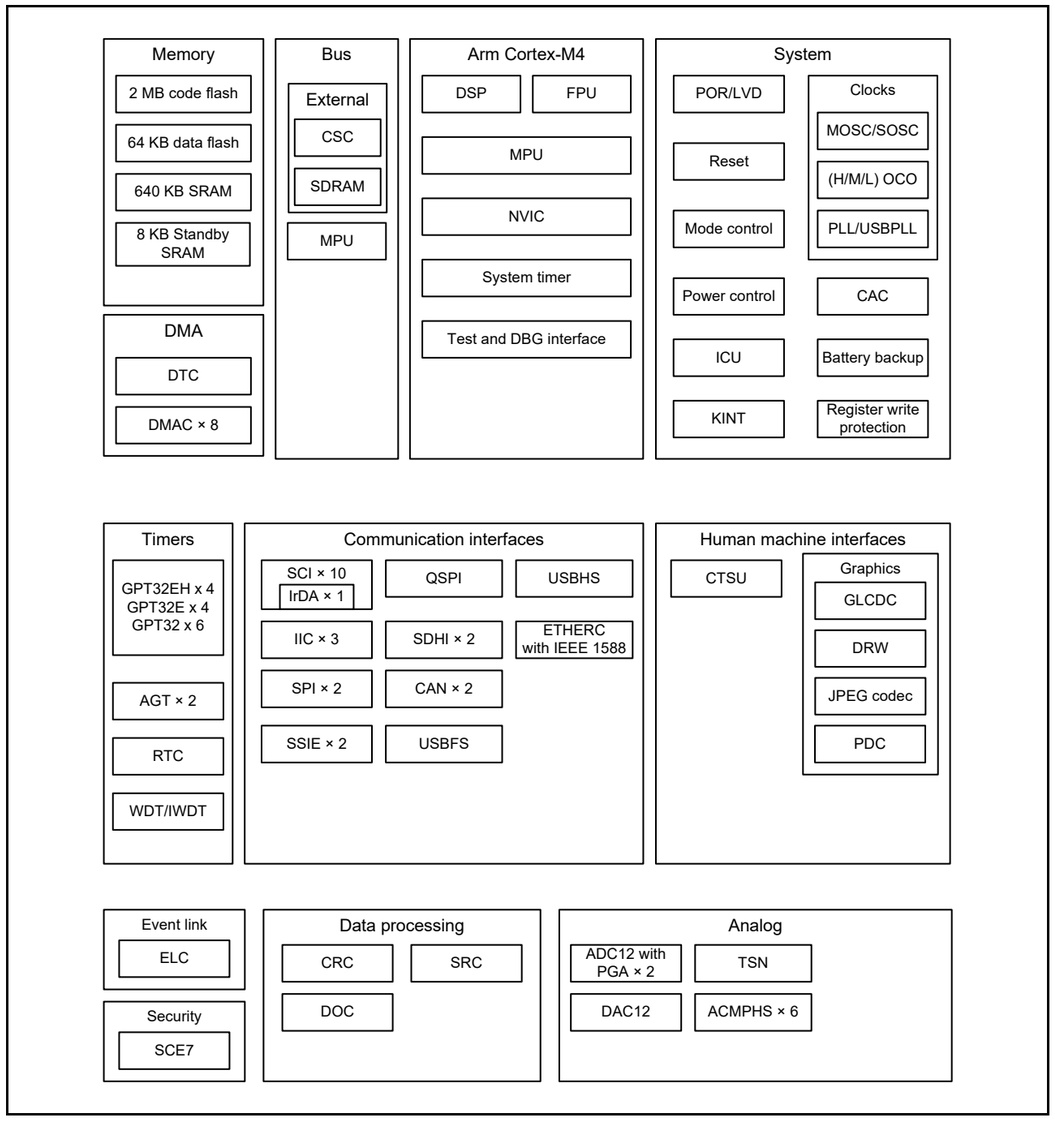


Figure 1.1 Block diagram

1.2 框图

图1.1显示了MCU超集的框图，该组中的一些单独的设备具有功能的子集。

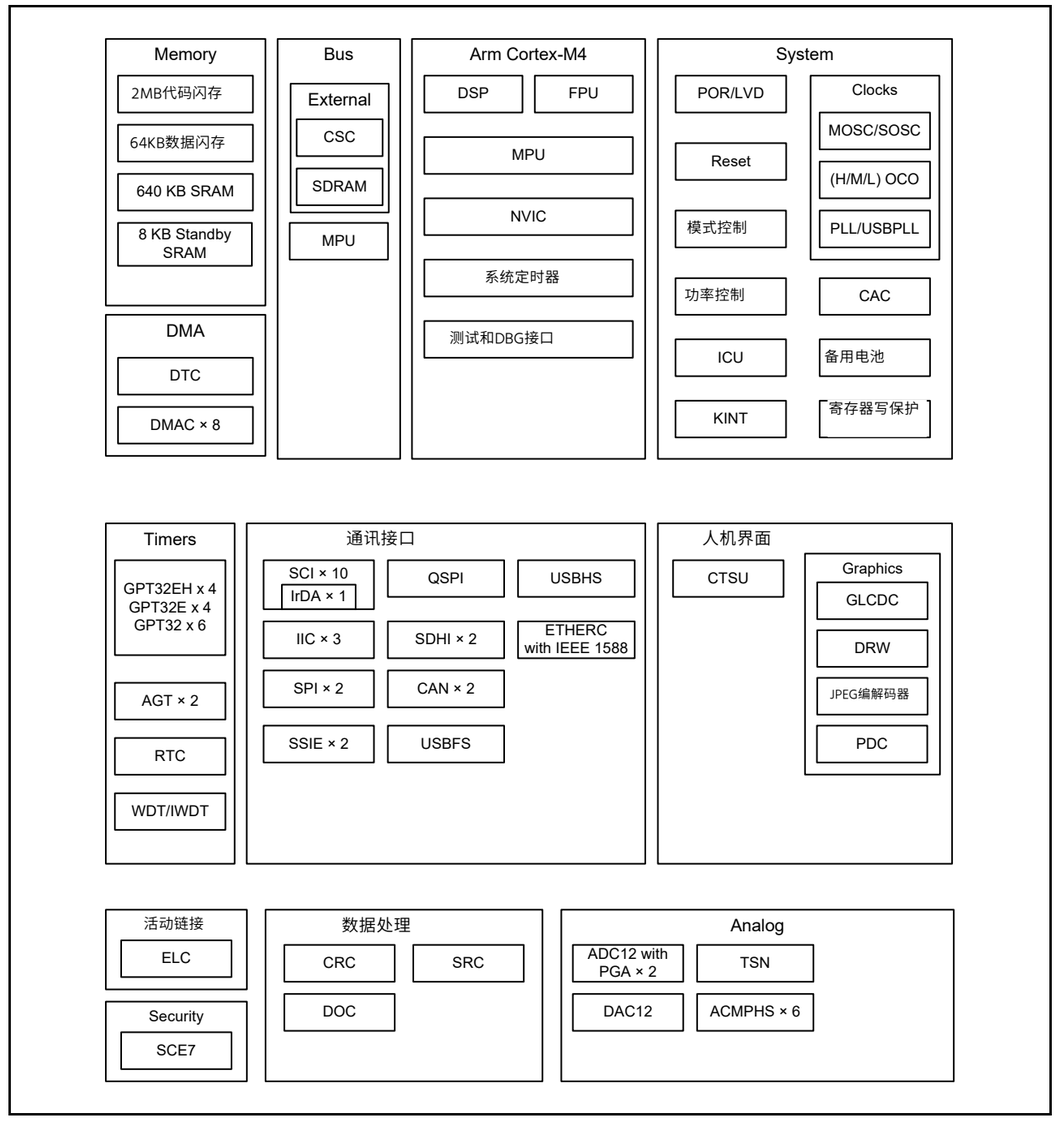


Figure 1.1 框图

1.3 Part Numbering

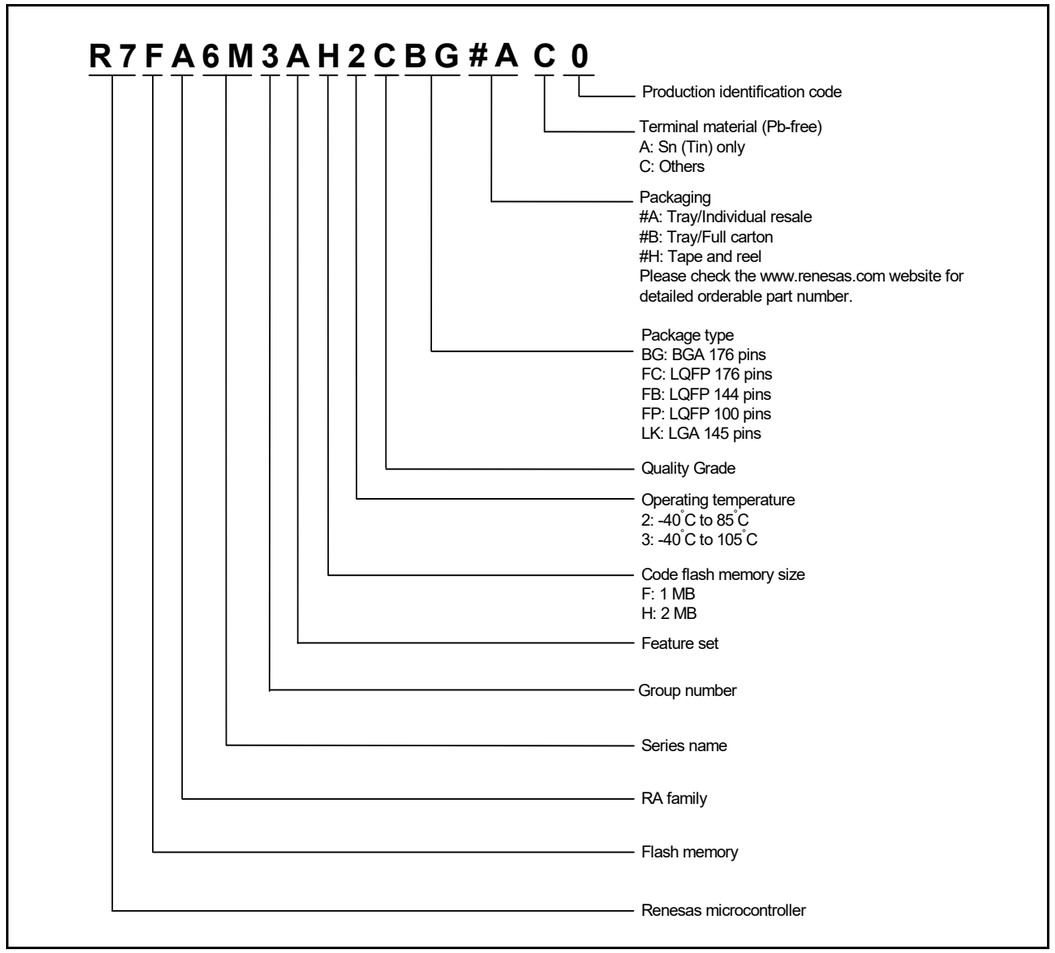


Figure 1.2 Part numbering scheme

Table 1.14 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6M3AH2CBG	PLBG0176GE-A	2 MB	64 KB	640 KB	-40 to +85°C
R7FA6M3AH3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AH2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AH3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AH3CFP	PLQP0100KB-B				-40 to +105°C
R7FA6M3AF2CBG	PLBG0176GE-A	1 MB			-40 to +85°C
R7FA6M3AF3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AF2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AF3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AF3CFP	PLQP0100KB-B				-40 to +105°C

1.3 零件编号

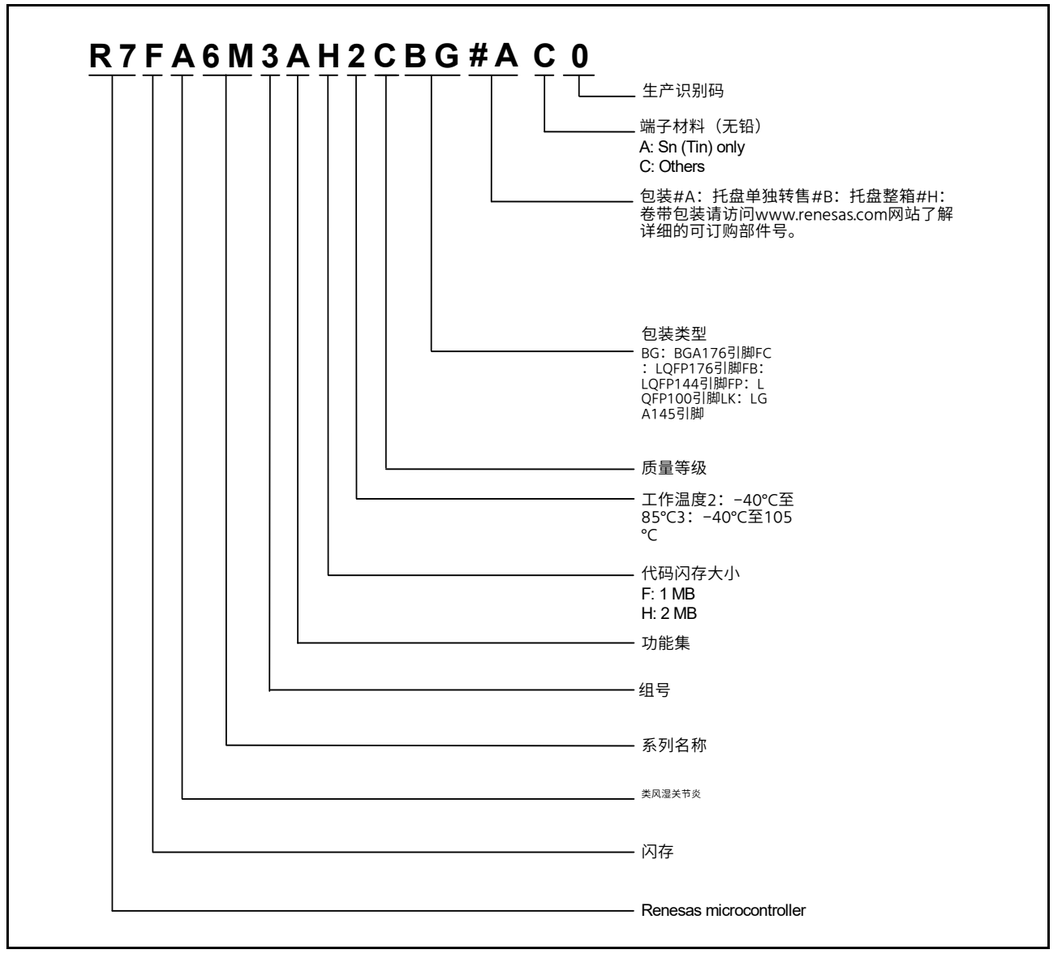


Figure 1.2 零件编号方案

Table 1.14 产品列表

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA6M3AH2CBG	PLBG0176GE-A	2 MB	64 KB	640 KB	-40 to +85°C
R7FA6M3AH3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AH2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AH3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AH3CFP	PLQP0100KB-B				-40 to +105°C
R7FA6M3AF2CBG	PLBG0176GE-A	1 MB			-40 to +85°C
R7FA6M3AF3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AF2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AF3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AF3CFP	PLQP0100KB-B				-40 to +105°C

1.4 Function Comparison

Table 1.15 Functional comparison

Function		Part numbers				
		R7FA6M3AH2CBG/ R7FA6M3AF2CBG	R7FA6M3AH3CFC/ R7FA6M3AF3CFC	R7FA6M3AH2CLK/ R7FA6M3AF2CLK	R7FA6M3AH3CFB/ R7FA6M3AF3CFB	R7FA6M3AH3CFP/ R7FA6M3AF3CFP
Pin count		176	176	145	144	100
Package		BGA	LQFP	LGA	LQFP	LQFP
Code flash memory		2/1 MB				
Data flash memory		64 KB				
SRAM		640 KB				
	Parity	608 KB				
	ECC	32 KB				
Standby SRAM		8 KB				
System	CPU clock	120 MHz				
	Backup registers	512 B				
	ICU	Yes				
	KINT	8				
Event link	ELC	Yes				
DMA	DTC	Yes				
	DMAC	8				
BUS	External bus	16-bit bus				8-bit bus
	SDRAM	Yes				No
Timers	GPT32EH	4	4	4	4	4
	GPT32E	4	4	4	4	4
	GPT32	6	6	6	6	5
	AGT	2	2	2	2	2
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	10				
	IIC	3				2
	SPI	2				
	SSIE	2				1
	QSPI	1				
	SDHI	2				
	CAN	2				
	USBFS	Yes				
	USBHS	Yes		No		
	ETHERC	1				
Analog	ADC12	24		22		19
	DAC12	2				
	ACMPHS	6				
	TSN	Yes				
HMI	CTSU	13		18		12
Graphics	GLCDC	RGB888				
	DRW	Yes				
	JPEG	Yes				
	PDC	Yes				
Data processing	CRC	Yes				
	DOC	Yes				
	SRC	Yes				
Security		SCE7				

1.4 功能比较

Table 1.15 功能比较

Function		零件号				
		R7FA6M3AH2CBG/ R7FA6M3AF2CBG	R7FA6M3AH3CFC/ R7FA6M3AF3CFC	R7FA6M3AH2CLK/ R7FA6M3AF2CLK	R7FA6M3AH3CFB/ R7FA6M3AF3CFB	R7FA6M3AH3CFP/ R7FA6M3AF3CFP
针数		176	176	145	144	100
Package		BGA	LQFP	LGA	LQFP	LQFP
代码闪存		2/1 MB				
数据闪存		64 KB				
SRAM		640 KB				
	Parity	608 KB				
	ECC	32 KB				
Standby SRAM		8 KB				
System	中央处理器时钟	120 MHz				
	备份寄存器	512 B				
	ICU	Yes				
	KINT	8				
活动链接	ELC	Yes				
DMA	DTC	Yes				
	DMAC	8				
BUS	外部总线	16-bit bus				8-bit bus
	SDRAM	Yes				No
Timers	GPT32EH	4	4	4	4	4
	GPT32E	4	4	4	4	4
	GPT32	6	6	6	6	5
	AGT	2	2	2	2	2
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	10				
	IIC	3				2
	SPI	2				
	SSIE	2				1
	QSPI	1				
	SDHI	2				
	CAN	2				
	USBFS	Yes				
	USBHS	Yes		No		
	ETHERC	1				
Analog	ADC12	24		22		19
	DAC12	2				
	ACMPHS	6				
	TSN	Yes				
HMI	CTSU	13		18		12
Graphics	GLCDC	RGB888				
	DRW	Yes				
	JPEG	Yes				
	PDC	Yes				
数据处理	CRC	Yes				
	DOC	Yes				
	SRC	Yes				
Security		SCE7				

1.5 Pin Functions

Table 1.16 Pin functions (1 of 5)

Function	Signal	I/O	Description
Power supply	VCC	Input	Digital voltage supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect to the system power supply. Connect to VSS through a 0.1-μF smoothing capacitor close to each VCC pin.
	VCL0	-	Connect to VSS through a 0.1-μF smoothing capacitor close to each VCL pin. Stabilize the internal power supply.
	VCL	-	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices
	SDCLK	Output	Outputs the SDRAM-dedicated clock
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
	SWO	Output	Serial wire trace output pin
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active low
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active low
	WR0 to WR1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active low
	BC0 to BC1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active low
	CS0 to CS7	Output	Select signals for CS areas, active low
	A00 to A23	Output	Address bus
	D00 to D15	I/O	Data bus
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus

1.5 引脚功能

Table 1.16 引脚功能(1of5)

Function	Signal	I/O	Description
电源	VCC	Input	数字电压电源引脚。这用作各个模块和内部稳压器的数字电源，并用于监控PORLVD的电压。连接到系统电源。通过靠近每个VCC引脚的0.1μF平滑电容器连接到VSS。
	VCL0	-	通过靠近每个VCL引脚的0.1μF平滑电容器连接到VSS。稳定内部电源。
	VCL	-	
	VSS	Input	接地引脚。连接到系统电源(0V)。
	VBATT	Input	备用电源引脚
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过输入 EXTAL pin.
	EXTAL	Input	
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	EBCLK	Output	为外部设备输出外部总线时钟
	SDCLK	Output	输出SDRAM专用时钟
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQ0 to IRQ15	Input	可屏蔽中断请求引脚
KINT	KR00 to KR07	Input	通过向按键中断输入引脚输入下降沿可以产生按键中断
On-chip emulator	TMS	I/O	片上仿真器或边界扫描引脚
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	该引脚输出与跟踪数据同步的时钟
	TDATA0 to TDATA3	Output	跟踪数据输出
	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
	SWO	Output	串行线迹输出引脚
外部总线接口	RD	Output	指示正在从外部总线接口空间读取的选通信号，低电平有效
	WR	Output	Strobe信号指示正在写入外部总线接口空间，在1-writestrobe模式下，低电平有效
	WR0 to WR1	Output	选通信号指示任一组数据总线引脚（D07到D00或D15到D08）在写入外部总线接口空间时有效，在字节选通模式下，低电平有效
	BC0 to BC1	Output	选通信号指示任一组数据总线引脚（D07至D00或 D15到D08）在访问外部总线接口空间时有效，在1-write选通模式下，低电平有效
	ALE	Output	选择地址数据复用总线时的地址锁存信号
	WAIT	Input	用于访问外部空间的等待请求信号的输入引脚，低电平有效
	CS0 to CS7	Output	CS区域的选择信号，低电平有效
	A00 to A23	Output	地址总线
	D00 to D15	I/O	数据总线
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus

Table 1.16 Pin functions (2 of 5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active low
	RAS	Output	SDRAM low address strobe signal, active low
	CAS	Output	SDRAM column address strobe signal, active low
	WE	Output	SDRAM write enable signal, active low
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08
	A00 to A15	Output	Address bus
	DQ00 to DQ15	I/O	Data bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active low
	SCL0 to SCL9	I/O	Input/output pins for the I^2C clock (simple IIC mode)
	SDA0 to SDA9	I/O	Input/output pins for the I^2C data (simple IIC mode)
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0 to SS9	Input	Chip-select input pins (simple SPI mode), active low
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock
	SDA0 to SDA2	I/O	Input/output pins for data
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSIBCK1		
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSILRCK1/SSIFS1		
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	SSIDATA1	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)

Table 1.16 引脚功能（2个，共5个）

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM时钟使能信号
	SDCS	Output	SDRAM片选信号，低电平有效
	RAS	Output	SDRAM低地址选通信号，低电平有效
	CAS	Output	SDRAM列地址选通信号，低电平有效
	WE	Output	SDRAM写使能信号，低电平有效
	DQM0	Output	DQ07到DQ00的SDRAMIO数据屏蔽使能信号
	DQM1	Output	DQ15至DQ08的SDRAMIO数据屏蔽使能信号
	A00 to A15	Output	地址总线
	DQ00 to DQ15	I/O	数据总线
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	外部触发输入引脚
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	输入捕捉、输出比较或PWM输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEE0, AGTEE1	Input	外部事件输入使能信号
	AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出引脚
	AGTO0, AGTO1	Output	脉冲输出引脚
	AGTOA0, AGTOA1	Output	输出比较匹配A输出引脚
	AGTOB0, AGTOB1	Output	输出比较匹配B输出引脚
RTC	RTCOUT	Output	用于1Hz或64Hz时钟的输出引脚
	RTCIC0 to RTCIC2	Input	时间捕捉事件输入引脚
SCI	SCK0 to SCK9	I/O	时钟输入输出引脚（时钟同步模式）
	RXD0 to RXD9	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXD0 to TXD9	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTS0_RTS0 to CTS9_RTS9	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效
	SCL0 to SCL9	I/O	I2C时钟的输入输出引脚（简单IIC模式）
	SDA0 to SDA9	I/O	I2C数据的输入输出引脚（简单IIC模式）
	SCK0 to SCK9	I/O	时钟输入输出引脚（简单SPI模式）
	MISO0 to MISO9	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSI0 to MOSI9	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	SS0 to SS9	Input	片选输入引脚（简单SPI模式），低电平有效
IIC	SCL0 to SCL2	I/O	时钟的输入输出引脚
	SDA0 to SDA2	I/O	数据输入输出引脚
SSIE	SSIBCK0	I/O	SSIE串行位时钟引脚
	SSIBCK1		
	SSILRCK0/SSIFS0	I/O	LR时钟帧同步管脚
	SSILRCK1/SSIFS1		
	SSITXD0	Output	串行数据输出引脚
	SSIRXD0	Input	串行数据输入引脚
	SSIDATA1	I/O	串行数据输入输出引脚
	AUDIO_CLK	Input	音频外部时钟引脚（输入过采样时钟）

Table 1.16 Pin functions (3 of 5)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	Receive data
	CTX0, CTX1	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
USBHS	VCC_USBHS	Input	Power supply pin
	VSS1_USBHS	Input	Ground pin
	VSS2_USBHS	Input	Ground pin
	AVCC_USBHS	Input	Analog power supply pin for the USBHS
	AVSS_USBHS	Input	Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin
	PVSS_USBHS	Input	PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin
	USBHS_RREF	I/O	USBHS reference current source pin. Connect this pin to the AVSS_USBHS pin through a 2.2-kΩ resistor (±1%)
	USBHS_DP	I/O	USB bus D+ data pin
	USBHS_DM	I/O	USB bus D- data pin
	USBHS_EXICEN	Output	Connect this pin to the OTG power supply IC
	USBHS_ID	Input	Connect this pin to the OTG power supply IC
	USBHS_VBUSEN	Output	VBUS power enable signal for USB
	USBHS_OVRCURA, USBHS_OVRCURB	Input	Overcurrent pin for USB
	USBHS_VBUS	Input	USB cable connection monitor input pin

Table 1.16 引脚功能(3of5)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	用于从主机输出数据的输入或输出引脚
	MISOA, MISOB	I/O	从机数据输出的输入或输出引脚
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	从机选择的输出引脚
QSPI	QSPCLK	Output	QSPI时钟输出引脚
	QSSL	Output	QSPI从机输出引脚
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	接收数据
	CTX0, CTX1	Output	传输数据
USBFS	VCC_USB	Input	电源引脚
	VSS_USB	Input	接地引脚
	USB_DP	I/O	USB片上收发器的D+IO引脚。将此引脚连接到USB总线的D+引脚
	USB_DM	I/O	USB片上收发器的DIO引脚。将此引脚连接到USB总线的Dpin
	USB_VBUS	Input	USB电缆连接监视器引脚。将此引脚连接到USB总线的VBUS。当USB模块作为功能控制器运行时，可以检测VBUS引脚状态（连接或断开）。
	USB_EXICEN	Output	用于外部电源(OTG)芯片的低功耗控制信号
	USB_VBUSEN	Output	VBUS(5V)为外部供电芯片供电使能信号
	USB_OVRCURA, USB_OVRCURB	Input	将外部过电流检测信号连接到这些引脚。连接OTG电源芯片时，将VBUS比较器信号连接到这些引脚。
	USB_ID	Input	在操作期间将MicroAB连接器ID输入信号连接到此引脚 OTG mode
USBHS	VCC_USBHS	Input	电源引脚
	VSS1_USBHS	Input	接地引脚
	VSS2_USBHS	Input	接地引脚
	AVCC_USBHS	Input	USBHS的模拟电源引脚
	AVSS_USBHS	Input	USBHS的模拟接地引脚。必须短接到PVSS_USBHS引脚
	PVSS_USBHS	Input	USBHS的PLL电路接地引脚。必须短接到AVSS_USBHS引脚
	USBHS_RREF	I/O	USBHS参考电流源引脚。通过一个2.2-kΩ电阻(　1%)将此引脚连接到AVSS_USBHS引脚
	USBHS_DP	I/O	USB总线D+数据引脚
	USBHS_DM	I/O	USB总线Ddata引脚
	USBHS_EXICEN	Output	将此引脚连接到OTG电源IC
	USBHS_ID	Input	将此引脚连接到OTG电源IC
	USBHS_VBUSEN	Output	USB的VBUS电源使能信号
	USBHS_OVRCURA, USBHS_OVRCURB	Input	USB过流引脚
	USBHS_VBUS	Input	USB线连接显示器输入引脚

Table 1.16 Pin functions (4 of 5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode
	ET0_CRS	Input	Carrier detection/data reception enable signal
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0
	ET0_EXOUT	Output	General-purpose external output pin
	ET0_LINKSTA	Input	Input link status from the PHY-LSI
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission
	ET0_RX_ER	Input	Receive error pin. Functions as signal to recognize an error during reception
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER
	ET0_COL	Input	Input collision detection signal
	ET0_WOL	Output	Receive Magic packets
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO.
	ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI
SDHI	SD0CLK, SD1CLK	Output	SD clock output pins
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pins
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins
	SD0CD, SD1CD	Input	SD card detection pins
	SD0WP, SD1WP	Input	SD write-protect signals
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.

Table 1.16 引脚功能(4of5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50MHz参考时钟。该引脚输入RMII模式下发送接收时序的参考信号。
	RMII0_CRS_DV	Input	在RMII模式下指示RMII0_RXD1和RMII0_RXD0上的载波检测信号和有效接收数据
	RMII0_TXD0, RMII0_TXD1	Output	RMII模式下的2位发送数据
	RMII0_RXD0, RMII0_RXD1	Input	RMII模式下的2位接收数据
	RMII0_TXD_EN	Output	RMII模式下数据发送使能信号的输出引脚
	RMII0_RX_ER	Input	表示在RMII模式下接收数据时发生错误
	ET0_CRS	Input	载波检测数据接收使能信号
	ET0_RX_DV	Input	指示ET0_ERXD3到ET0_ERXD0上的有效接收数据
	ET0_EXOUT	Output	通用外部输出引脚
	ET0_LINKSTA	Input	从PHY-LSI输入链路状态
	ET0_ETXD0 to ET0_ETXD3	Output	4位MII传输数据
	ET0_ERXD0 to ET0_ERXD3	Input	4位MII接收数据
	ET0_TX_EN	Output	发送使能信号。用作指示在ET0_ETXD3到ET0_ETXD0上传输数据已准备好的信号
	ET0_TX_ER	Output	发送错误引脚。作为信号通知PHY_LSI传输过程中的错误
	ET0_RX_ER	Input	接收错误引脚。在接收过程中用作识别错误的信号
	ET0_TX_CLK	Input	发送时钟引脚。该引脚输入参考信号用于从ET0_TX_EN、ET0_ETXD3到ET0_ETXD0和ET0_TX_ER
	ET0_RX_CLK	Input	接收时钟引脚。该引脚输入用于输入时序的参考信号ET0_RX_DV、ET0_ERXD3到ET0_ERXD0和ET0_RX_ER
	ET0_COL	Input	输入碰撞检测信号
	ET0_WOL	Output	接收魔术包
	ET0_MDC	Output	通过ET0_MDIO输出用于信息传输的参考时钟信号。
	ET0_MDIO	I/O	用于交换管理数据的输入或输出双向信号PHY-LSI
SDHI	SD0CLK, SD1CLK	Output	SD时钟输出引脚
	SD0CMD, SD1CMD	I/O	命令输出引脚和响应输入信号引脚
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD和MMC数据总线引脚
	SD0CD, SD1CD	Input	SD卡检测引脚
	SD0WP, SD1WP	Input	SD write-protect signals
模拟电源	AVCC0	Input	模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。
	AVSS0	Input	模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。
	VREFH0	Input	ADC12（单元0）的模拟参考电压电源引脚。当不使用ADC12（单元0）和AN000到AN002的采样保持电路时，将此引脚连接到VCC。
	VREFL0	Input	ADC12的模拟参考接地引脚。不使用ADC12（单元0）和AN000至AN002的采样保持电路时，将此引脚连接到VSS
	VREFH	Input	ADC12（单元1）和DA的模拟参考电压电源引脚转换器。不使用ADC12（单元1）、AN100至AN102的采样保持电路和DA转换器时，将此引脚连接到VCC。
	VREFL	Input	ADC12和DA转换器的模拟参考接地引脚。不使用ADC12（单元1）、AN100至AN102的采样保持电路和DA转换器时，将此引脚连接到VSS。

Table 1.16 Pin functions (5 of 5)

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	Input pins for the analog signals to be processed by the ADC12
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion
	ADTRG1	Input	
	PGAVSS000/PGAVSS100	Input	Differential input pins
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter
ACMPHS	VCOUT	Output	Comparator output pin
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator
	IVCMP0 to IVCMP2	Input	Analog voltage input pins for comparator
CTSU	TS00 to TS17	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
I/O ports	P000 to P007	Input	General-purpose input pins
	P008 to P010, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P214	I/O	General-purpose input/output pins
	P300 to P315	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P508, P511 to P513	I/O	General-purpose input/output pins
	P600 to P615	I/O	General-purpose input/output pins
	P700 to P713	I/O	General-purpose input/output pins
	P800 to P806	I/O	General-purpose input/output pins
	P900, P901, P905 to P908	I/O	General-purpose input/output pins
	PA00, PA01, PA08 to PA10	I/O	General-purpose input/output pins
	PB00, PB01	I/O	General-purpose input/output pins
GLCDC	LCD_DATA23 to LCD_DATA00	Output	Data output pins for panel
	LCD_TCON3 to LCD_TCON0	Output	Output pins for panel timing adjustment
	LCD_CLK	Output	Panel clock output pin
	LCD_EXTCLK	Input	Panel clock source input pin
PDC	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock

Table 1.16 引脚功能（5个中的5个）

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	ADC12处理的模拟信号的输入引脚
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚
	ADTRG1	Input	
	PGAVSS000/PGAVSS100	Input	差分输入引脚
DAC12	DA0, DA1	Output	DA转换器处理的模拟信号的输出引脚
ACMPHS	VCOUT	Output	比较器输出引脚
	IVREF0 to IVREF3	Input	比较器的参考电压输入引脚
	IVCMP0 to IVCMP2	Input	比较器的模拟电压输入引脚
CTSU	TS00 to TS17	Input	电容式触摸检测引脚（触摸引脚）
	TSCAP	-	触摸驱动器的辅助电源引脚
I/O ports	P000 to P007	Input	通用输入引脚
	P008 to P010, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201 to P214	I/O	General-purpose input/output pins
	P300 to P315	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P508, P511 to P513	I/O	General-purpose input/output pins
	P600 to P615	I/O	General-purpose input/output pins
	P700 to P713	I/O	General-purpose input/output pins
	P800 to P806	I/O	General-purpose input/output pins
	P900, P901, P905 to P908	I/O	General-purpose input/output pins
	PA00, PA01, PA08 to PA10	I/O	General-purpose input/output pins
	PB00, PB01	I/O	General-purpose input/output pins
GLCDC	LCD_DATA23 to LCD_DATA00	Output	面板数据输出引脚
	LCD_TCON3 to LCD_TCON0	Output	用于面板时序调整的输出引脚
	LCD_CLK	Output	面板时钟输出引脚
	LCD_EXTCLK	Input	面板时钟源输入引脚
PDC	PIXCLK	Input	图像传输时钟引脚
	VSYNC	Input	垂直同步信号引脚
	HSYNC	Input	水平同步信号引脚
	PIXD0 to PIXD7	Input	8位图像数据引脚
	PCKO	Output	点时钟的输出引脚

1.6 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments.

R7FA6M3XX2CBG

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212/EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213/XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK/SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1

Figure 1.3 Pin assignment for 176-pin BGA (top view)

1.6 引脚分配

图1.3至图1.7显示了引脚分配。

R7FA6M3XX2CBG

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212/EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213/XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK/SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1

Figure 1.3 176引脚BGA的引脚分配（顶视图）

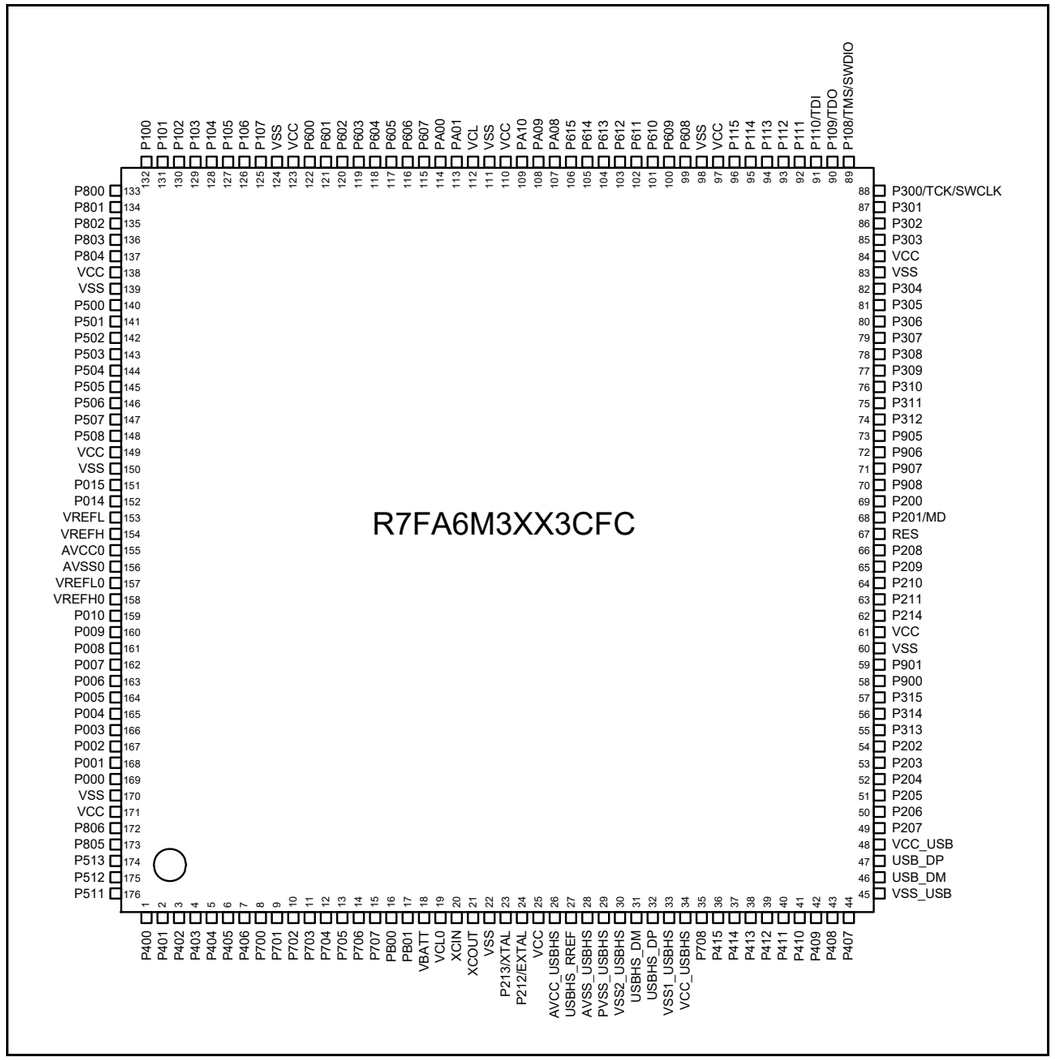


Figure 1.4 Pin assignment for 176-pin LQFP (top view)

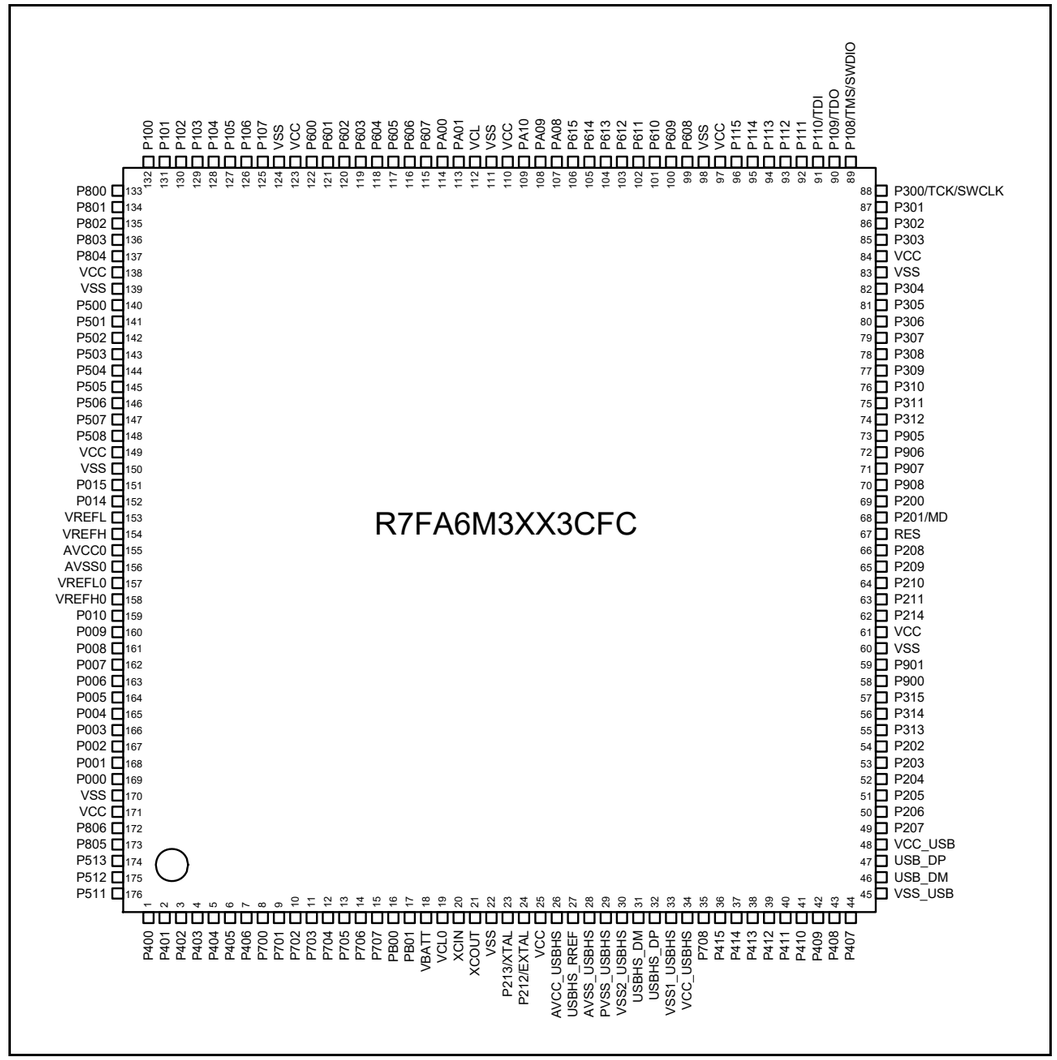


Figure 1.4 176引脚LQFP的引脚分配（俯视图）

R7FA6M3XX2CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	P214	P211	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	P210	P209	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	P208	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	P508	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.5 Pin assignment for 145-pin LGA (top view)

R7FA6M3XX2CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	P214	P211	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	P210	P209	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	P208	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	P508	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.5 145引脚LGA的引脚分配（俯视图）

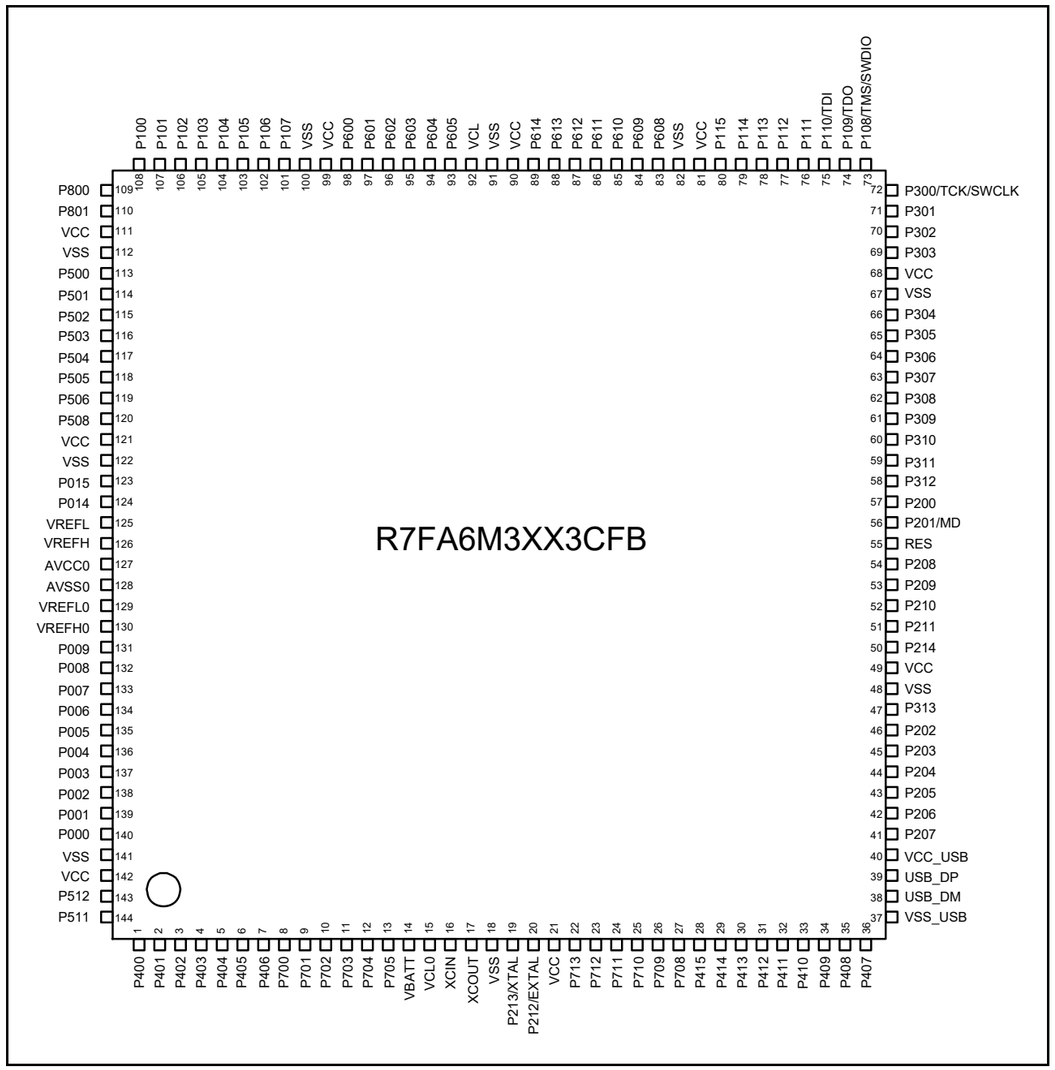


Figure 1.6 Pin assignment for 144-pin LQFP (top view)

RA6M3 Group 1. Overview

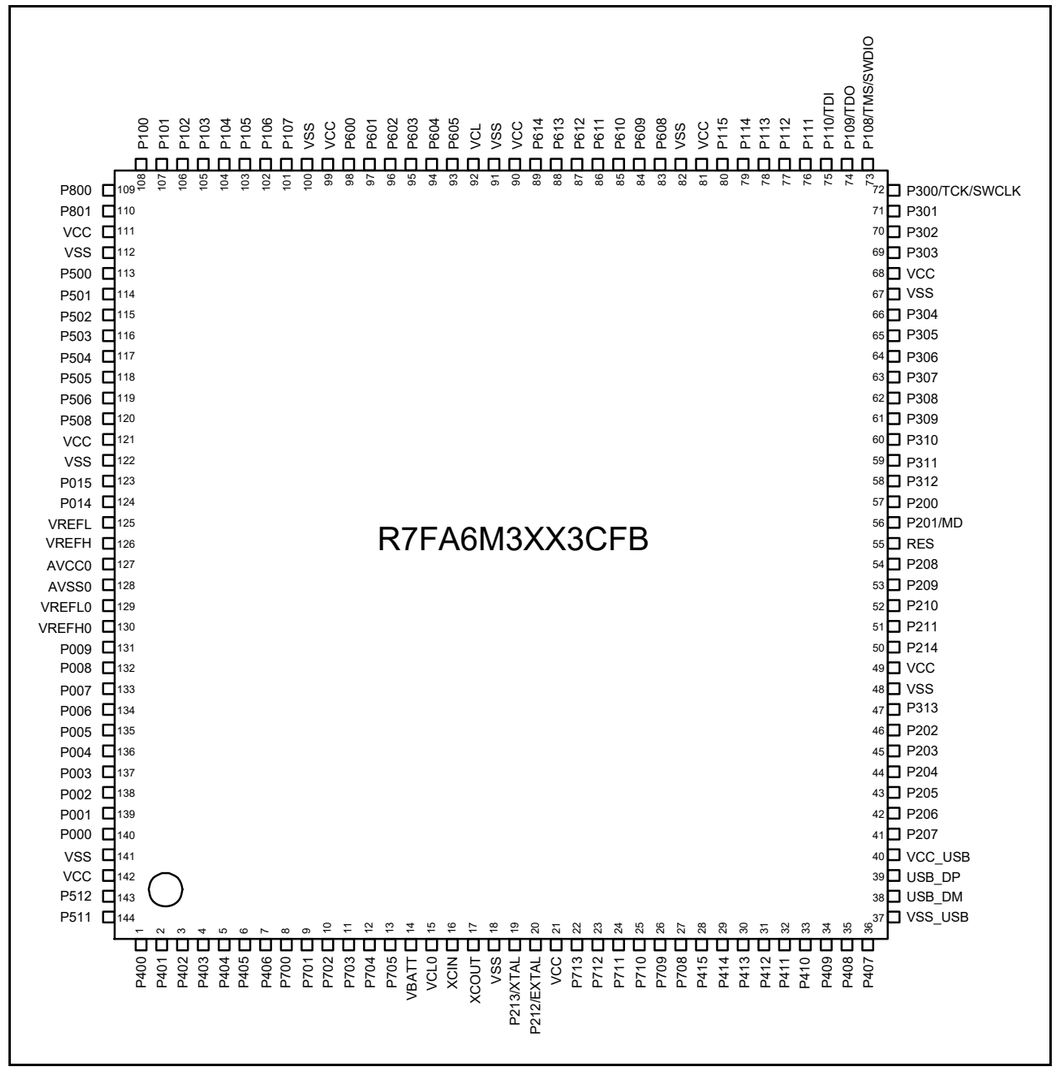


Figure 1.6 144引脚LQFP的引脚分配（俯视图）

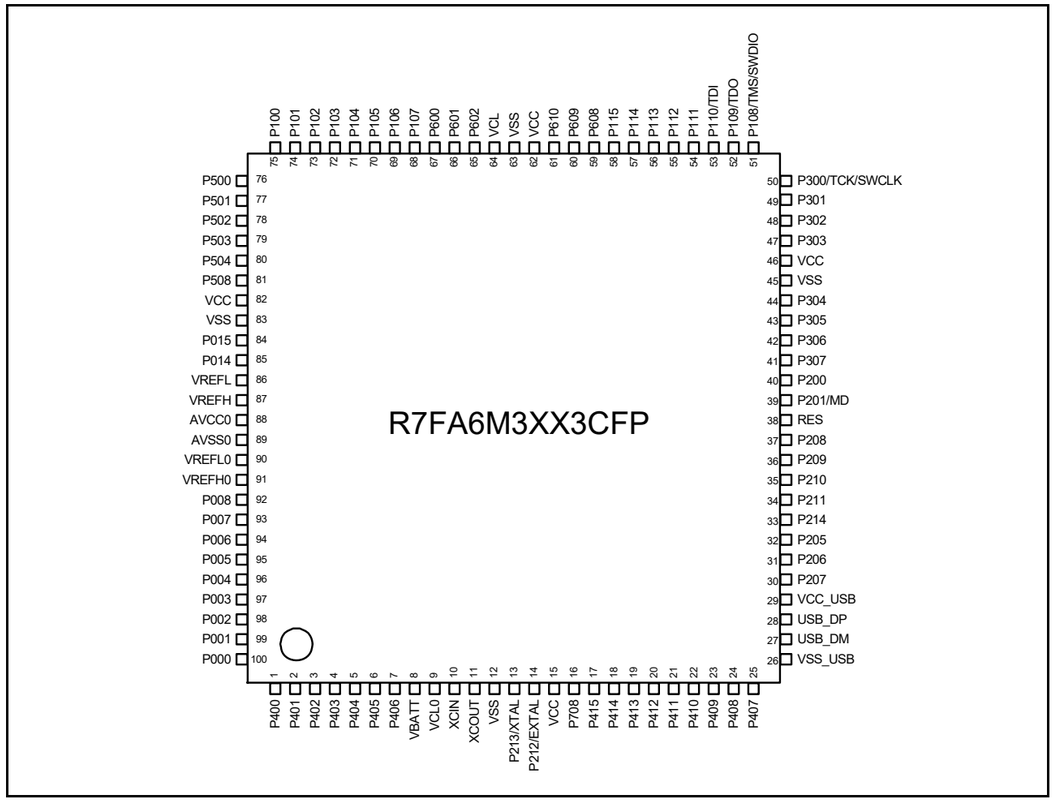


Figure 1.7 Pin assignment for 100-pin LQFP (top view)

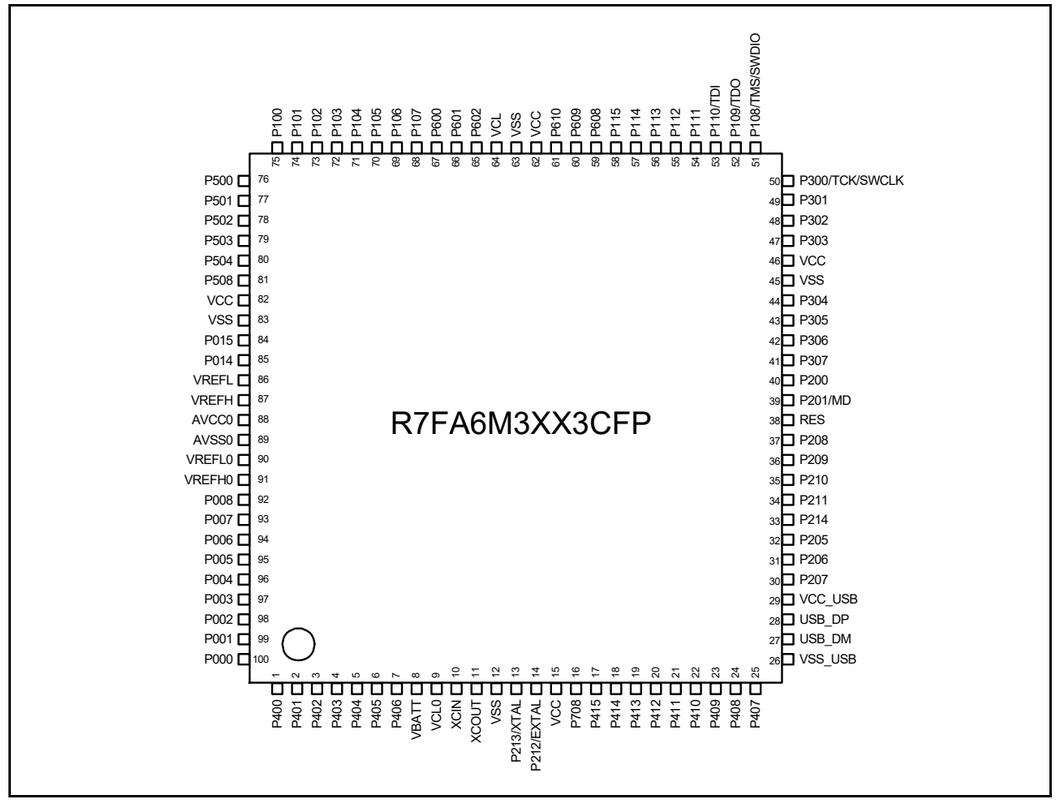


Figure 1.7 100引脚LQFP的引脚分配（顶视图）

1.7 Pin Lists

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces									Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
N13	1	N13	1	1	-	IRQ0	P400	-	-	AGTIO1	-	GTIOC 6A	-	-	SCK4	SCK7	SCL0 _A	-	AUDIO _CLK	ET0_W OL	ET0_ WOL	-	-	ADTRG 1	-	-	-
R15	2	L11	2	2	-	IRQ5-DS	P401	-	-	-	GTETRGA	GTIOC 6B	-	CTX0	CTS4_ RTS4/ SS4	TXD7/ MOSI7 /SDA7	SDA0 _A	-	-	ET0_M DC	ET0_M DC	-	-	-	-	-	-
P14	3	M13	3	3	CACREF	IRQ4-DS	P402	-	-	AGTIO0/ AGTIO1	-	-	RTC IC0	CRX0	-	RXD7/ MISO7 /SCL7	-	-	AUDIO _CLK	ET0_M DIO	ET0_M DIO	-	-	-	-	-	VSYNC
M12	4	K11	4	4	-	-	P403	-	-	AGTIO0/ AGTIO1	-	GTIOC 3A	RTC IC1	-	-	CTS7_ RTS7/ SS7	-	-	SSIBC K0_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD1 DAT7 _B	-	-	-	PIXD7
M13	5	L12	5	5	-	-	P404	-	-	-	-	GTIOC 3B	RTC IC2	-	-	-	-	-	SSILR CK0/S SIFS0_ A	ET0_EX OUT	ET0_E XOUT	-	SD1 DAT6 _B	-	-	-	PIXD6
P15	6	L13	6	6	-	-	P405	-	-	-	-	GTIOC 1A	-	-	-	-	-	-	SSITX D0_A	ET0_TX _EN	RMII0_ TXD_E N_B	-	SD1 DAT5 _B	-	-	-	PIXD5
N14	7	J10	7	7	-	-	P406	-	-	-	-	GTIOC 1B	-	-	-	-	-	SSLB3 _C	SSIRX D0_A	ET0_RX _ER	RMII0_ TXD1_ B	-	SD1 DAT4 _B	-	-	-	PIXD4
N15	8	H10	8	-	-	-	P700	-	-	-	-	GTIOC 5A	-	-	-	-	-	MISOB _C	-	ET0_ET XD1	RMII0_ TXD0_ B	-	SD1 DAT3 _B	-	-	-	PIXD3
M14	9	K12	9	-	-	-	P701	-	-	-	-	GTIOC 5B	-	-	-	-	-	MOSIB _C	-	ET0_ET XD0	REF50 CK0_B	-	SD1 DAT2 _B	-	-	-	PIXD2
L12	10	K13	10	-	-	-	P702	-	-	-	-	GTIOC 6A	-	-	-	-	-	RSPC KB_C	-	ET0_ER XD1	RMII0_ RXD0_ B	-	SD1 DAT1 _B	-	-	-	PIXD1
M15	11	J11	11	-	-	-	P703	-	-	-	-	GTIOC 6B	-	-	-	-	-	SSLB0 _C	-	ET0_ER XD0	RMII0_ RXD1_ B	-	SD1 DAT0 _B	-	VCOUT	-	PIXD0
L13	12	H11	12	-	-	-	P704	-	-	AGTO0	-	-	-	CTX0	-	-	-	-	SSLB1 _C	-	ET0_RX _CLK	RMII0_ RX_E R_B	-	SD1 CLK_ B	-	-	-	HSYNC
K12	13	G11	13	-	-	-	P705	-	-	AGTIO0	-	-	-	CRX0	-	-	-	-	SSLB2 _C	-	ET0_C RS	RMII0_ CRS_ DV_B	-	SD1 CMD _B	-	-	-	PIXCLK
L14	14	-	-	-	-	IRQ7	P706	-	-	-	-	-	-	-	-	RXD3/ MISO3 /SCL3	-	-	-	-	-	-	USB HS_ OVR CUR B	SD1 CD_ B	-	-	-	-
L15	15	-	-	-	-	IRQ8	P707	-	-	-	-	-	-	-	-	TXD3/ MOSI3 /SDA3	-	-	-	-	-	-	USB HS_ OVR CUR A	SD1 WP_ B	-	-	-	-
J12	16	-	-	-	-	-	PB00	-	-	-	-	-	-	-	-	SCK3	-	-	-	-	-	-	USB HS_ VBU SEN	-	-	-	-	-
K13	17	-	-	-	-	-	PB01	-	-	-	-	-	-	-	-	CTS3_ RTS3/ SS3	-	-	-	-	-	-	USB HS_ VBU S	-	-	-	-	-
K14	18	J12	14	8	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K15	19	J13	15	9	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J15	20	H13	16	10	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J14	21	H12	17	11	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J13	22	F12	18	12	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H14	23	G12	19	13	XTAL	IRQ2	P213	-	-	-	GTETRGC	GTIOC 0A	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	-	-	-	-	ADTRG 1	-	-	-	-
H15	24	G13	20	14	EXTAL	IRQ3	P212	-	-	AGTEE1	GTETRGD	GTIOC 0B	-	-	-	RXD1/ MISO1 /SCL1	-	-	-	-	-	-	-	-	-	-	-	-
H12	25	F13	21	15	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H13	26	-	-	-	AVCC_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G13	27	-	-	-	USBHS_ RREF	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G14	28	-	-	-	AVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G15	29	-	-	-	PVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G12	30	-	-	-	VSS2_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F15	31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DM	-	-	-	-	-
F14	32	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DP	-	-	-	-	-
F12	33	-	-	-	VSS1_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F13	34	-	-	-	VCC_US BHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	G10	22	-	-	-	P713	-	-	AGTOA0	-	GTIOC 2A	-	-	-	-	-	-	-	-	-	-	-	-	-	TS17	-	-

1.7 引脚列表

针号					电源系统，时钟，调试，CAC			Extbus		Timers				通讯接口									Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100		Interrupt	I/O port	外部总线	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
N13	1	N13	1	1	-	IRQ0	P400	-	-	AGTIO1	-	GTIOC 6A	-	-	SCK4	SCK7	SCL0 _A	-	AUDIO _CLK	ET0_W OL	ET0_ WOL	-	-	ADTRG 1	-	-	-
R15	2	L11	2	2	-	IRQ5-DS	P401	-	-	-	GTETRGA	GTIOC 6B	-	CTX0	CTS4_ RTS4/ SS4	TXD7/ MOSI7 /SDA7	SDA0 _A	-	-	ET0_M DC	ET0_M DC	-	-	-	-	-	-
P14	3	M13	3	3	CACREF	IRQ4-DS	P402	-	-	AGTIO0/ AGTIO1	-	-	RTC IC0	CRX0	-	RXD7/ MISO7 /SCL7	-	-	AUDIO _CLK	ET0_M DIO	ET0_M DIO	-	-	-	-	-	VSYNC
M12	4	K11	4	4	-	-	P403	-	-	AGTIO0/ AGTIO1	-	GTIOC 3A	RTC IC1	-	-	CTS7_ RTS7/ SS7	-	-	SSIBC K0_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD1 DAT7 _B	-	-	-	PIXD7
M13	5	L12	5	5	-	-	P404	-	-	-	-	GTIOC 3B	RTC IC2	-	-	-	-	-	SSILR CK0/S SIFS0_ A	ET0_EX OUT	ET0_E XOUT	-	SD1 DAT6 _B	-	-	-	PIXD6
P15	6	L13	6	6	-	-	P405	-	-	-	-	GTIOC 1A	-	-	-	-	-	-	SSITX D0_A	ET0_TX _EN	RMII0_ TXD_E N_B	-	SD1 DAT5 _B	-	-	-	PIXD5
N14	7	J10	7	7	-	-	P406	-	-	-	-	GTIOC 1B	-	-	-	-	-	SSLB3 _C	SSIRX D0_A	ET0_RX _ER	RMII0_ TXD1_ B	-	SD1 DAT4 _B	-	-	-	PIXD4
N15	8	H10	8	-	-	-	P700	-	-	-	-	GTIOC 5A	-	-	-	-	-	MISOB _C	-	ET0_ET XD1	RMII0_ TXD0_ B	-	SD1 DAT3 _B	-	-	-	PIXD3
M14	9	K12	9	-	-	-	P701	-	-	-	-	GTIOC 5B	-	-	-	-	-	MOSIB _C	-	ET0_ET XD0	REF50 CK0_B	-	SD1 DAT2 _B	-	-	-	PIXD2
L12	10	K13	10	-	-	-	P702	-	-	-	-	GTIOC 6A	-	-	-	-	-	RSPC KB_C	-	ET0_ER XD1	RMII0_ RXD0_ B	-	SD1 DAT1 _B	-	-	-	PIXD1
M15	11	J11	11	-	-	-	P703	-	-	-	-	GTIOC 6B	-	-	-	-	-	SSLB0 _C	-	ET0_ER XD0	RMII0_ RXD1_ B	-	SD1 DAT0 _B	-	VCOUT	-	PIXD0
L13	12	H11	12	-	-	-	P704	-	-	AGTO0	-	-	-	CTX0	-	-	-	-	SSLB1 _C	-	ET0_RX _CLK	RMII0_ RX_E R_B	-	SD1 CLK_ B	-	-	-	HSYNC
K12	13	G11	13	-	-	-	P705	-	-	AGTIO0	-	-	-	CRX0	-	-	-	-	SSLB2 _C	-	ET0_C RS	RMII0_ CRS_ DV_B	-	SD1 CMD _B	-	-	-	PIXCLK
L14	14	-	-	-	-	IRQ7	P706	-	-	-	-	-	-	-	-	RXD3/ MISO3 /SCL3	-	-	-	-	-	-	USB HS_ OVR CUR B	SD1 CD_ B	-	-	-	-
L15	15	-	-	-	-	IRQ8	P707	-	-	-	-	-	-	-	-	TXD3/ MOSI3 /SDA3	-	-	-	-	-	-	USB HS_ OVR CUR A	SD1 WP_ B	-	-	-	-
J12	16	-	-	-	-	-	PB00	-	-	-	-	-	-	-	-	SCK3	-	-	-	-	-	-	USB HS_ VBU SEN	-	-	-	-	-
K13	17	-	-	-	-	-	PB01	-	-	-	-	-	-	-	-	CTS3_ RTS3/ SS3	-	-	-	-	-	-	USB HS_ VBU S	-	-	-	-	-
K14	18	J12	14	8	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K15	19	J13	15	9	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J15	20	H13	16	10	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J14	21	H12	17	11	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J13	22	F12	18	12	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H14	23	G12	19	13	XTAL	IRQ2	P213	-	-	-	GTETRGC	GTIOC 0A	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	-	-	-	-	ADTRG 1	-	-	-	-
H15	24	G13	20	14	EXTAL	IRQ3	P212	-	-	AGTEE1	GTETRGD	GTIOC 0B	-	-	-	RXD1/ MISO1 /SCL1	-	-	-	-	-	-	-	-	-	-	-	-
H12	25	F13	21	15	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H13	26	-	-	-	AVCC_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G13	27	-	-	-	USBHS_ RREF	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G14	28	-	-	-	AVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G15	29	-	-	-	PVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G12	30	-	-	-	VSS2_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F15	31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DM	-	-	-	-	-
F14	32	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DP	-	-	-	-	-
F12	33	-	-	-	VSS1_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F13	34	-	-	-	VCC_US BHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	G10	22	-	-	-	P713	-	-	AGTOA0	-	GTIOC 2A	-	-	-	-	-	-	-	-	-	-	-	-	-	TS17	-	-

Pin number								Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
-	-	F11	23	-	-	-	P712	-	-	AGTOB0	-	GTIOC 2B	-	-	-	-	-	-	-	-	-	-	-	-	-	TS16	-
-	-	E13	24	-	-	-	P711	-	-	AGTEE0	-	-	-	-	-	CTS1_ RTS1/ SS1	-	-	-	-	ET0_TX _CLK	-	-	-	-	-	TS15	-
-	-	E12	25	-	-	-	P710	-	-	-	-	-	-	-	-	SCK1	-	-	-	-	ET0_TX _ER	-	-	-	-	-	TS14	-
-	-	F10	26	-	-	IRQ10	P709	-	-	-	-	-	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	-	ET0_ET XD2	-	-	-	-	-	TS13	-
E15	35	D13	27	16	CACREF	IRQ11	P708	-	-	-	-	-	-	-	-	RXD1/ MISO1 /SCL1	-	SSLA3 _B	AUDIO _CLK	ET0_ET XD3	-	-	-	-	-	TS12	PCKO
E14	36	E11	28	17	-	IRQ8	P415	-	-	-	-	GTIOC 0A	-	USB_ VBUS EN	-	-	-	SSLA2 _B	-	ET0_TX _EN	RMII0_ TXD_E N_A	-	SD0 CD_ A	-	-	TS11	PIXD5
D15	37	D12	29	18	-	IRQ9	P414	-	-	-	-	GTIOC 0B	-	-	-	-	-	SSLA1 _B	-	ET0_RX _ER	RMII0_ TXD1_ A	-	SD0 WP_ A	-	-	TS10	PIXD4
E13	38	E10	30	19	-	-	P413	-	-	-	GTOUUP	-	-	-	CTS0_ RTS0/ SS0	-	-	SSLA0 _B	-	ET0_ET XD1	RMII0_ TXD0_ A	-	SD0 CLK_ A	-	-	TS09	PIXD3
D14	39	C13	31	20	-	-	P412	-	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPC KA_B	-	ET0_ET XD0	REF50 CK0_A	-	SD0 CMD _A	-	-	TS08	PIX02
C15	40	D11	32	21	-	IRQ4	P411	-	-	AGTOA1	GTOVUP	GTIOC 9A	-	-	TXD0/ MOSI0 /SDA0	CTS3_ RTS3/ SS3	-	MOSIA _B	-	ET0_ER XD1	RMII0_ RXD0_ A	-	SD0 DAT0 _A	-	-	TS07	PIX01
C14	41	C12	33	22	-	IRQ5	P410	-	-	AGTOB1	GTOVLO	GTIOC 9B	-	-	RXD0/ MISO0 /SCL0	SCK3	-	MISOA _B	-	ET0_ER XD0	RMII0_ RXD1_ A	-	SD0 DAT1 _A	-	-	TS06	PIXD0
B15	42	B13	34	23	-	IRQ6	P409	-	-	-	GTOWUP	GTIOC 10A	-	USB_ EXIC EN	-	TXD3/ MOSI3 /SDA3	-	-	-	ET0_RX _CLK	RMII0_ RX_E R_A	USB HS_ EXIC EN	-	-	-	TS05	HSYNC
D13	43	D10	35	24	-	IRQ7	P408	-	-	-	GTOWLO	GTIOC 10B	-	USB_ ID	-	RXD3/ MISO3 /SCL3	SCL0 _B	-	-	ET0_C RS	RMII0_ CRS_ DV_A	USB HS_I D	-	-	-	TS04	PIXCLK
A15	44	A13	36	25	-	-	P407	-	-	AGTIO0	-	-	RTC OUT	USB_ VBUS	CTS4_ RTS4/ SS4	-	SDA0 _B	SSLB3 _A	-	ET0_EX OUT	ET0_E XOUT	-	-	ADTRG 0	-	TS03	-
C13	45	B11	37	26	VSS_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B14	46	A12	38	27	-	-	-	-	-	-	-	-	-	USB_ DM	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	47	B12	39	28	-	-	-	-	-	-	-	-	-	USB_ DP	-	-	-	-	-	-	-	-	-	-	-	-	-
B13	48	A11	40	29	VCC_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C12	49	C11	41	30	-	-	P207	A17	-	-	-	-	-	-	-	-	-	SSLB2 _A/QS SL	-	-	-	-	-	-	-	TS02	LCD_DATA 23_B
D12	50	B10	42	31	-	IRQ0-DS	P206	WAIT	-	-	GTIU	-	-	USB_ VBUS EN	RXD4/ MISO4 /SCL4	-	SDA1 _A	SSLB1 _A	SSIDA TA1_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD0 DAT2 _A	-	-	TS01	-
E12	51	A10	43	32	CLKOUT	IRQ1-DS	P205	A16	-	AGTO1	GTIV	GTIOC 4A	-	USB_ OVR CUR A-DS	TXD4/ MOSI4 /SDA4	CTS9_ RTS9/ SS9	SCL1 _A	SSLB0 _A	SSILR CK1/S SIFS1_ A	ET0_W OL	ET0_ WOL	-	SD0 DAT3 _A	-	-	TSCA P	-
A13	52	C10	44	-	CACREF	-	P204	A18	-	AGTIO1	GTIW	GTIOC 4B	-	USB_ OVR CUR B-DS	SCK4	SCK9	SCL0 _B	RSPC KB_A	SSIBC K1_A	ET0_RX _DV	-	-	SD0 DAT4 _A	-	-	TS00	-
D11	53	A9	45	-	-	IRQ2-DS	P203	A19	-	-	-	GTIOC 5A	-	CTX0	CTS2_ RTS2/ SS2	TXD9/ MOSI9 /SDA9	-	MOSIB _A	-	ET0_C OL	-	-	SD0 DAT5 _A	-	-	TSCA P	-
B12	54	C9	46	-	-	IRQ3-DS	P202	WR1/ BC1	-	-	-	GTIOC 5B	-	CRX0	SCK2	RXD9/ MISO9 /SCL9	-	MISOB _A	-	ET0_ER XD2	-	-	SD0 DAT6 _A	-	-	-	LCD_TCO N3_B
A12	55	B9	47	-	-	-	P313	A20	-	-	-	-	-	-	-	-	-	-	-	ET0_ER XD3	-	-	SD0 DAT7 _A	-	-	-	LCD_TCO N2_B
C11	56	-	-	-	-	-	P314	A21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ADTRG 0	-	-	LCD_TCO N1_B
B11	57	-	-	-	-	-	P315	A22	-	-	-	-	-	-	RXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N0_B
A11	58	-	-	-	-	-	P900	A23	-	-	-	-	-	-	TXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK_ B
C10	59	-	-	-	-	-	P901	-	-	AGTIO1	-	-	-	-	SCK4	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 15_B
D10	60	D9	48	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	61	D8	49	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A10	62	A8	50	33	TRCLK	-	P214	-	-	-	GTIU	-	-	-	-	-	-	QSPC LK	-	ET0_M DC	ET0_M DC	-	SD0 CLK_ B	-	-	-	LCD_DATA 22_B
B10	63	B8	51	34	TRDATA 0	-	P211	-	-	-	GTIV	-	-	-	-	-	-	QIO0	-	ET0_M DIO	ET0_M DIO	-	SD0 CMD _B	-	-	-	LCD_DATA 21_B
A9	64	A7	52	35	TRDATA 1	-	P210	-	-	-	GTIW	-	-	-	-	-	-	QIO1	-	ET0_W OL	ET0_ WOL	-	SD0 CD_ B	-	-	-	LCD_DATA 20_B
B9	65	B7	53	36	TRDATA 2	-	P209	-	-	-	GTOVUP	-	-	-	-	-	-	QIO2	-	ET0_EX OUT	ET0_E XOUT	-	SD0 WP_ B	-	-	-	LCD_DATA 19_B

针号								Extbus		Timers				通讯接口										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	电源系统、时钟、调试、CAC	Interrupt	I/O port	外线总部	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
-	-	F11	23	-	-	-	P712	-	-	AGTOB0	-	GTIOC 2B	-	-	-	-	-	-	-	-	-	-	-	-	-	TS16	-
-	-	E13	24	-	-	-	P711	-	-	AGTEE0	-	-	-	-	-	CTS1_ RTS1/ SS1	-	-	-	ET0_TX _CLK	-	-	-	-	-	TS15	-
-	-	E12	25	-	-	-	P710	-	-	-	-	-	-	-	-	SCK1	-	-	-	ET0_TX _ER	-	-	-	-	-	TS14	-
-	-	F10	26	-	-	IRQ10	P709	-	-	-	-	-	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	ET0_ET XD2	-	-	-	-	-	TS13	-
E15	35	D13	27	16	CACREF	IRQ11	P708	-	-	-	-	-	-	-	-	RXD1/ MISO1 /SCL1	-	SSLA3 _B	AUDIO _CLK	ET0_ET XD3	-	-	-	-	-	TS12	PCKO
E14	36	E11	28	17	-	IRQ8	P415	-	-	-	-	GTIOC 0A	-	USB_ VBUS EN	-	-	-	SSLA2 _B	-	ET0_TX _EN	RMII0_ TXD_E N_A	-	SD0 CD_ A	-	-	TS11	PIXD5
D15	37	D12	29	18	-	IRQ9	P414	-	-	-	-	GTIOC 0B	-	-	-	-	-	SSLA1 _B	-	ET0_RX _ER	RMII0_ TXD1_ A	-	SD0 WP_ A	-	-	TS10	PIXD4
E13	38	E10	30	19	-	-	P413	-	-	-	GTOUUP	-	-	-	CTS0_ RTS0/ SS0	-	-	SSLA0 _B	-	ET0_ET XD1	RMII0_ TXD0_ A	-	SD0 CLK_ A	-	-	TS09	PIXD3
D14	39	C13	31	20	-	-	P412	-	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPC KA_B	-	ET0_ET XD0	REF50 CK0_A	-	SD0 CMD _A	-	-	TS08	PIX02
C15	40	D11	32	21	-	IRQ4	P411	-	-	AGTOA1	GTOVUP	GTIOC 9A	-	-	TXD0/ MOSI0 /SDA0	CTS3_ RTS3/ SS3	-	MOSIA _B	-	ET0_ER XD1	RMII0_ RXD0_ A	-	SD0 DAT0 _A	-	-	TS07	PIX01
C14	41	C12	33	22	-	IRQ5	P410	-	-	AGTOB1	GTOVLO	GTIOC 9B	-	-	RXD0/ MISO0 /SCL0	SCK3	-	MISOA _B	-	ET0_ER XD0	RMII0_ RXD1_ A	-	SD0 DAT1 _A	-	-	TS06	PIXD0
B15	42	B13	34	23	-	IRQ6	P409	-	-	-	GTOWUP	GTIOC 10A	-	USB_ EXIC EN	-	TXD3/ MOSI3 /SDA3	-	-	-	ET0_RX _CLK	RMII0_ RX_E R_A	USB HS_E XICE N	-	-	-	TS05	HSYNC
D13	43	D10	35	24	-	IRQ7	P408	-	-	-	GTOWLO	GTIOC 10B	-	USB_ ID	-	RXD3/ MISO3 /SCL3	SCL0 _B	-	-	ET0_C RS	RMII0_ CRS_ DV_A	USB HS_I D	-	-	-	TS04	PIXCLK
A15	44	A13	36	25	-	-	P407	-	-	AGTIO0	-	-	RTC OUT	USB_ VBUS	CTS4_ RTS4/ SS4	-	SDA0 _B	SSLB3 _A	-	ET0_EX OUT	ET0_E XOUT	-	-	ADTRG 0	-	TS03	-
C13	45	B11	37	26	VSS_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B14	46	A12	38	27	-	-	-	-	-	-	-	-	-	USB_ DM	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	47	B12	39	28	-	-	-	-	-	-	-	-	-	USB_ DP	-	-	-	-	-	-	-	-	-	-	-	-	-
B13	48	A11	40	29	VCC_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C12	49	C11	41	30	-	-	P207	A17	-	-	-	-	-	-	-	-	-	SSLB2 _A/QS SL	-	-	-	-	-	-	-	TS02	LCD_DATA 23_B
D12	50	B10	42	31	-	IRQ0-DS	P206	WAIT	-	-	GTIU	-	-	USB_ VBUS EN	RXD4/ MISO4 /SCL4	-	SDA1 _A	SSLB1 _A	SSIDA TA1_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD0 DAT2 _A	-	-	TS01	-
E12	51	A10	43	32	CLKOUT	IRQ1-DS	P205	A16	-	AGTO1	GTIV	GTIOC 4A	-	USB_ OVR CUR A-DS	TXD4/ MOSI4 /SDA4	CTS9_ RTS9/ SS9	SCL1 _A	SSLB0 _A	SSILR CK1/S SIFS1_ A	ET0_W OL	ET0_ WOL	-	SD0 DAT3 _A	-	-	TSCA P	-
A13	52	C10	44	-	CACREF	-	P204	A18	-	AGTIO1	GTIW	GTIOC 4B	-	USB_ OVR CUR B-DS	SCK4	SCK9	SCL0 _B	RSPC KB_A	SSIBC K1_A	ET0_RX _DV	-	-	SD0 DAT4 _A	-	-	TS00	-
D11	53	A9	45	-	-	IRQ2-DS	P203	A19	-	-	-	GTIOC 5A	-	CTX0	CTS2_ RTS2/ SS2	TXD9/ MOSI9 /SDA9	-	MOSIB _A	-	ET0_C OL	-	-	SD0 DAT5 _A	-	-	TSCA P	-
B12	54	C9	46	-	-	IRQ3-DS	P202	WR1/ BC1	-	-	-	GTIOC 5B	-	CRX0	SCK2	RXD9/ MISO9 /SCL9	-	MISOB _A	-	ET0_ER XD2	-	-	SD0 DAT6 _A	-	-	-	LCD_TCO N3_B
A12	55	B9	47	-	-	-	P313	A20	-	-	-	-	-	-	-	-	-	-	-	ET0_ER XD3	-	-	SD0 DAT7 _A	-	-	-	LCD_TCO N2_B
C11	56	-	-	-	-	-	P314	A21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ADTRG 0	-	-	LCD_TCO N1_B
B11	57	-	-	-	-	-	P315	A22	-	-	-	-	-	-	RXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N0_B
A11	58	-	-	-	-	-	P900	A23	-	-	-	-	-	-	TXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK_ B
C10	59	-	-	-	-	-	P901	-	-	AGTIO1	-	-	-	-	SCK4	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 15_B
D10	60	D9	48	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	61	D8	49	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A10	62	A8	50	33	TRCLK	-	P214	-	-	-	GTIU	-	-	-	-	-	-	QSPC LK	-	ET0_M DC	ET0_M DC	-	SD0 CLK_ B	-	-	-	LCD_DATA 22_B
B10	63	B8	51	34	TRDATA 0	-	P211	-	-	-	GTIV	-	-	-	-	-	-	QIO0	-	ET0_M DIO	ET0_M DIO	-	SD0 CMD _B	-	-	-	LCD_DATA 21_B
A9	64	A7	52	35	TRDATA 1	-	P210	-	-	-	GTIW	-	-	-	-	-	-	QIO1	-	ET0_W OL	ET0_ WOL	-	SD0 CD_ B	-	-	-	LCD_DATA 20_B
B9	65	B7	53	36	TRDATA 2	-	P209	-	-	-	GTOVUP	-	-	-	-	-	-	QIO2	-	ET0_EX OUT	ET0_E XOUT	-	SD0 WP_ B	-	-	-	LCD_DATA 19_B

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (60 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
A8	66	A6	54	37	TRDATA3	-	P208	-	-	-	GTOVLO	-	-	-	-	-	-	QIO3	-	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT0_B	-	-	-	LCD_DATA18_B
C9	67	C7	55	38	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B8	68	B6	56	39	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	69	C8	57	40	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D8	70	-	-	-	-	-	P908	CS7	-	-	-	GTIOC2A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA14_B
D7	71	-	-	-	-	-	P907	CS6	-	-	-	GTIOC2B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA13_B
A7	72	-	-	-	-	-	P906	CS5	-	-	-	GTIOC3A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA12_B
B7	73	-	-	-	-	-	P905	CS4	-	-	-	GTIOC3B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA11_B
C7	74	C6	58	-	-	-	P312	CS3	CAS	AGTOA1	-	-	-	-	-	CTS3_RTS3/SS3	-	-	-	-	-	-	-	-	-	-	-
D6	75	B5	59	-	-	-	P311	CS2	RAS	AGTOB1	-	-	-	-	-	SCK3	-	-	-	-	-	-	-	-	-	-	LCD_DATA23_A
A6	76	D7	60	-	-	-	P310	A15	A15	AGTEE1	-	-	-	-	-	TXD3	-	QIO3	-	-	-	-	-	-	-	-	LCD_DATA22_A
B6	77	A5	61	-	-	-	P309	A14	A14	-	-	-	-	-	-	RXD3	-	QIO2	-	-	-	-	-	-	-	-	LCD_DATA21_A
A5	78	C5	62	-	-	-	P308	A13	A13	-	-	-	-	-	-	-	-	QIO1	-	-	-	-	-	-	-	-	LCD_DATA20_A
C6	79	A4	63	41	-	-	P307	A12	A12	-	GTOUUP	-	-	-	CTS6	-	-	QIO0	-	-	-	-	-	-	-	-	LCD_DATA19_A
A4	80	B4	64	42	-	-	P306	A11	A11	-	GTOULO	-	-	-	SCK6	-	-	QSSL	-	-	-	-	-	-	-	-	LCD_DATA18_A
B5	81	D6	65	43	-	IRQ8	P305	A10	A10	-	GTOWUP	-	-	-	TXD6/MOSI6/SDA6	-	-	QSPCLK	-	-	-	-	-	-	-	-	LCD_DATA17_A
B4	82	C4	66	44	-	IRQ9	P304	A09	A09	-	GTOWLO	GTIOC7A	-	-	RXD6/MISO6/SCL6	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_A
C5	83	A3	67	45	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D5	84	B3	68	46	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A3	85	D5	69	47	-	-	P303	A08	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_A
B3	86	A2	70	48	-	IRQ5	P302	A07	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-	-	-	-	LCD_DATA14_A
A2	87	C3	71	49	-	IRQ6	P301	A06	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-	-	-	-	LCD_DATA13_A
C4	88	B2	72	50	TCK/SWCLK	-	P300	-	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-	-	-	-	-
C3	89	A1	73	51	TMS/SWDIO	-	P108	-	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-	-	-	-	-
A1	90	D4	74	52	CLKOUT/TDO/SWO	-	P109	-	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-	-	-	-	-
D3	91	B1	75	53	TDI	IRQ3	P110	-	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	-	-	-	VCOUT	-	-
D4	92	C2	76	54	-	IRQ4	P111	A05	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-	-	-	-	LCD_DATA12_A
B2	93	D3	77	55	-	-	P112	A04	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-	-	-	-	LCD_DATA11_A
B1	94	C1	78	56	-	-	P113	A03	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-	-	-	-	LCD_DATA10_A
C2	95	E4	79	57	-	-	P114	A02	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-	-	-	-	LCD_DATA09_A
C1	96	E3	80	58	-	-	P115	A01	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-	-	-	-	LCD_DATA08_A
E3	97	D2	81	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E4	98	D1	82	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D2	99	F4	83	59	-	-	P608	A00/BC0	A00/DQM1	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_A
D1	100	E2	84	60	-	-	P609	CS1	CKE	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_A
F3	101	F3	85	61	-	-	P610	CS0	WE	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_A
E2	102	E1	86	-	CLKOUT/CACREF	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_RTS7/SS7	-	-	-	-	-	-	-	-	-	-	-
E1	103	F2	87	-	-	-	P612	D08[A08/D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-	-
F4	104	F1	88	-	-	-	P613	D09[A09/D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-	-
F2	105	G3	89	-	-	-	P614	D10[A10/D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-	-
F1	106	-	-	-	-	-	P615	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA10_B
G1	107	-	-	-	-	-	PA08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA09_B

RA6M3 Group 1. Overview

针号					电源系统，时钟，调试，CAC	Interrupt	I/O port	Extbus		Timers				通讯接口										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				外线总部	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (60 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
A8	66	A6	54	37	TRDATA3	-	P208	-	-	-	GTOVLO	-	-	-	-	-	-	QIO3	-	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT0_B	-	-	-	LCD_DATA18_B
C9	67	C7	55	38	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B8	68	B6	56	39	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	69	C8	57	40	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D8	70	-	-	-	-	-	P908	CS7	-	-	-	GTIOC2A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA14_B
D7	71	-	-	-	-	-	P907	CS6	-	-	-	GTIOC2B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA13_B
A7	72	-	-	-	-	-	P906	CS5	-	-	-	GTIOC3A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA12_B
B7	73	-	-	-	-	-	P905	CS4	-	-	-	GTIOC3B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA11_B
C7	74	C6	58	-	-	-	P312	CS3	CAS	AGTOA1	-	-	-	-	-	CTS3_RTS3/SS3	-	-	-	-	-	-	-	-	-	-	-
D6	75	B5	59	-	-	-	P311	CS2	RAS	AGTOB1	-	-	-	-	-	SCK3	-	-	-	-	-	-	-	-	-	-	LCD_DATA23_A
A6	76	D7	60	-	-	-	P310	A15	A15	AGTEE1	-	-	-	-	-	TXD3	-	QIO3	-	-	-	-	-	-	-	-	LCD_DATA22_A
B6	77	A5	61	-	-	-	P309	A14	A14	-	-	-	-	-	-	RXD3	-	QIO2	-	-	-	-	-	-	-	-	LCD_DATA21_A
A5	78	C5	62	-	-	-	P308	A13	A13	-	-	-	-	-	-	-	-	QIO1	-	-	-	-	-	-	-	-	LCD_DATA20_A
C6	79	A4	63	41	-	-	P307	A12	A12	-	GTOUUP	-	-	-	CTS6	-	-	QIO0	-	-	-	-	-	-	-	-	LCD_DATA19_A
A4	80	B4	64	42	-	-	P306	A11	A11	-	GTOULO	-	-	-	SCK6	-	-	QSSL	-	-	-	-	-	-	-	-	LCD_DATA18_A
B5	81	D6	65	43	-	IRQ8	P305	A10	A10	-	GTOWUP	-	-	-	TXD6/MOSI6/SDA6	-	-	QSPCLK	-	-	-	-	-	-	-	-	LCD_DATA17_A
B4	82	C4	66	44	-	IRQ9	P304	A09	A09	-	GTOWLO	GTIOC7A	-	-	RXD6/MISO6/SCL6	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_A
C5	83	A3	67	45	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D5	84	B3	68	46	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A3	85	D5	69	47	-	-	P303	A08	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_A
B3	86	A2	70	48	-	IRQ5	P302	A07	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-	-	-	-	LCD_DATA14_A
A2	87	C3	71	49	-	IRQ6	P301	A06	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-	-	-	-	LCD_DATA13_A
C4	88	B2	72	50	TCK/SWCLK	-	P300	-	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-	-	-	-	-
C3	89	A1	73	51	TMS/SWDIO	-	P108	-	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-	-	-	-	-
A1	90	D4	74	52	CLKOUT/TDO/SWO	-	P109	-	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-	-	-	-	-
D3	91	B1	75	53	TDI	IRQ3	P110	-	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	-	-	-	VCOUT	-	-
D4	92	C2	76	54	-	IRQ4	P111	A05	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-	-	-	-	LCD_DATA12_A
B2	93	D3	77	55	-	-	P112	A04	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-	-	-	-	LCD_DATA11_A
B1	94	C1	78	56	-	-	P113	A03	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-	-	-	-	LCD_DATA10_A
C2	95	E4	79	57	-	-	P114	A02	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-	-	-	-	LCD_DATA09_A
C1	96	E3	80	58	-	-	P115	A01	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-	-	-	-	LCD_DATA08_A
E3	97	D2	81	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E4	98	D1	82	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D2	99	F4	83	59	-	-	P608	A00/BC0	A00/DQM1	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_A
D1	100	E2	84	60	-	-	P609	CS1	CKE	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_A
F3	101	F3	85	61	-	-	P610	CS0	WE	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_A
E2	102	E1	86	-	CLKOUT/CACREF	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_RTS7/SS7	-	-	-	-	-	-	-	-	-	-	-
E1	103	F2	87	-	-	-	P612	D08[A08/D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-	-
F4	104	F1	88	-	-	-	P613	D09[A09/D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-	-
F2	105	G3	89	-	-	-	P614	D10[A10/D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-	-
F1	106	-	-	-	-	-	P615	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA10_B
G1	107	-	-	-	-	-	PA08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA09_B

Pin number								Extbus		Timers				Communication interfaces										Analog			HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
G4	108	-	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 08_B
G2	109	-	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 07_B
G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	112	H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	113	-	-	-	-	-	PA01	-	-	-	-	-	-	-	SCK8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 06_B
H4	114	-	-	-	-	-	PA00	-	-	-	-	-	-	-	TXD8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 05_B
J4	115	-	-	-	-	-	P607	-	-	-	-	-	-	-	RXD8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_B
J1	116	-	-	-	-	-	P606	-	-	-	-	-	RTC OUT	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_B
J2	117	H2	93	-	-	-	P605	D11[A11/ D11]	DQ11	-	-	GTIOC 8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	118	G4	94	-	-	-	P604	D12[A12/ D12]	DQ12	-	-	GTIOC 8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	119	H3	95	-	-	-	P603	D13[A13/ D13]	DQ13	-	-	GTIOC 7A	-	-	-	CTS9_ RTS9/ SS9	-	-	-	-	-	-	-	-	-	-	-	-
K1	120	J1	96	65	-	-	P602	EBC LK	SDCL K	-	-	GTIOC 7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_A
K2	121	J2	97	66	-	-	P601	WR/ WR0	DQM0	-	-	GTIOC 6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_A
L1	122	H4	98	67	CLKOUT /CACRE F	-	P600	RD	-	-	-	GTIOC 6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 02_A
K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L2	125	J3	101	68	-	KR07	P107	D07[A07/ D07]	DQ07	AGTOA0	-	GTIOC 8A	-	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 01_A
M1	126	K3	102	69	-	KR06	P106	D06[A06/ D06]	DQ06	AGTOB0	-	GTIOC 8B	-	-	SCK8	-	-	SSLA3 _A	-	-	-	-	-	-	-	-	-	LCD_DATA 00_A
L3	127	J4	103	70	-	IRQ0/ KR05	P105	D05[A05/ D05]	DQ05	-	GTETRGA	GTIOC 1A	-	-	TXD8/ MOSI8 /SDA8	-	-	SSLA2 _A	-	-	-	-	-	-	-	-	-	LCD_TCO N3_A
M2	128	L3	104	71	-	IRQ1/ KR04	P104	D04[A04/ D04]	DQ04	-	GTETRGB	GTIOC 1B	-	-	RXD8/ MISO8 /SCL8	-	-	SSLA1 _A	-	-	-	-	-	-	-	-	-	LCD_TCO N2_A
N1	129	L1	105	72	-	KR03	P103	D03[A03/ D03]	DQ03	-	GTOWUP	GTIOC 2A_A	-	CTX0	CTS0_ RTS0/ SS0	-	-	SSLA0 _A	-	-	-	-	-	-	-	-	-	LCD_TCO N1_A
M3	130	M1	106	73	-	KR02	P102	D02[A02/ D02]	DQ02	AGTO0	GTOWLO	GTIOC 2B_A	-	CRX0	SCK0	-	-	RSPC KA_A	-	-	-	-	-	ADTRG 0	-	-	-	LCD_TCO N0_A
N2	131	M2	107	74	-	IRQ1/ KR01	P101	D01[A01/ D01]	DQ01	AGTEE0	GTETRGB	GTIOC 5A	-	-	TXD0/ MOSI0 /SDA0	CTS1_ RTS1/ SS1	SDA1 _B	MOSIA _A	-	-	-	-	-	-	-	-	-	LCD_CLK_ A
P1	132	N1	108	75	-	IRQ2/ KR00	P100	D00[A00/ D00]	DQ00	AGTIO0	GTETRGA	GTIOC 5B	-	-	RXD0/ MISO0 /SCL0	SCK1	SCL1 _B	MISOA _A	-	-	-	-	-	-	-	-	-	LCD_EXT CLK_A
N3	133	L2	109	-	-	-	P800	D14[A14/ D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R1	134	N2	110	-	-	-	P801	D15[A15/ D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT4 _A	-	-	-	-	-
P2	135	-	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT5 _A	-	-	-	-	LCD_DATA 02_B
R2	136	-	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT6 _A	-	-	-	-	LCD_DATA 01_B
P3	137	-	-	-			-	P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT7 _A	-	-	-	-	LCD_DATA 00_B
N4	138	N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M4	139	M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R3	140	K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC 11A	-	USB_ VBUS EN	-	-	-	QSPC LK	-	-	-	-	SD1 CLK_ A	AN016	IVREF0	-	-
P4	141	M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC 11B	-	USB_ OVR_ CUR A	-	TXD5/ MOSI5 /SDA5	-	QSSL	-	-	-	-	SD1 CMD _A	AN116	IVREF1	-	-
R4	142	L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC 12A	-	USB_ OVR_ CUR B	-	RXD5/ MISO5 /SCL5	-	QIO0	-	-	-	-	SD1 DAT0 _A	AN017	IVCMP0	-	-
N5	143	K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC 12B	-	USB_ EXIC EN	CTS6_ RTS6/ SS6	SCK5	-	QIO1	-	-	-	-	SD1 DAT1 _A	AN117	-	-	-
P5	144	L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC 13A	-	USB_ ID	SCK6	CTS5_ RTS5/ SS5	-	QIO2	-	-	-	-	SD1 DAT2 _A	AN018	-	-	-
P6	145	K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC 13B	-	-	RXD6/ MISO6 /SCL6	-	-	QIO3	-	-	-	-	SD1 DAT3 _A	AN118	-	-	-

RA6M3 Group 1. Overview

针号					电源系统、时钟、调试、CAC			Extbus		Timers				通讯接口										Analog			HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100		Interrupt	I/O port	外线总部线	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
G4	108	-	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G2	109	-	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	112	H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	113	-	-	-	-	-	PA01	-	-	-	-	-	-	-	SCK8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 06_B
H4	114	-	-	-	-	-	PA00	-	-	-	-	-	-	-	TXD8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 05_B
J4	115	-	-	-	-	-	P607	-	-	-	-	-	-	-	RXD8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_B
J1	116	-	-	-	-	-	P606	-	-	-	-	-	RTC OUT	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_B
J2	117	H2	93	-	-	-	P605	D11[A11/ D11]	DQ11	-	-	GTIOC 8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	118	G4	94	-	-	-	P604	D12[A12/ D12]	DQ12	-	-	GTIOC 8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	119	H3	95	-	-	-	P603	D13[A13/ D13]	DQ13	-	-	GTIOC 7A	-	-	-	CTS9_ RTS9/ SS9	-	-	-	-	-	-	-	-	-	-	-	-
K1	120	J1	96	65	-	-	P602	EBC LK	SDCL K	-	-	GTIOC 7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_A
K2	121	J2	97	66	-	-	P601	WR/ WR0	DQM0	-	-	GTIOC 6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_A
L1	122	H4	98	67	CLKOUT /CACRE F	-	P600	RD	-	-	-	GTIOC 6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 02_A
K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L2	125	J3	101	68	-	KR07	P107	D07[A07/ D07]	DQ07	AGTOA0	-	GTIOC 8A	-	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 01_A
M1	126	K3	102	69	-	KR06	P106	D06[A06/ D06]	DQ06	AGTOB0	-	GTIOC 8B	-	-	SCK8	-	-	SSLA3 _A	-	-	-	-	-	-	-	-	-	LCD_DATA 00_A
L3	127	J4	103	70	-	IRQ0/ KR05	P105	D05[A05/ D05]	DQ05	-	GTETRGA	GTIOC 1A	-	-	TXD8/ MOSI8 /SDA8	-	-	SSLA2 _A	-	-	-	-	-	-	-	-	-	LCD_TCO N3_A
M2	128	L3	104	71	-	IRQ1/ KR04	P104	D04[A04/ D04]	DQ04	-	GTETRGB	GTIOC 1B	-	-	RXD8/ MISO8 /SCL8	-	-	SSLA1 _A	-	-	-	-	-	-	-	-	-	LCD_TCO N2_A
N1	129	L1	105	72	-	KR03	P103	D03[A03/ D03]	DQ03	-	GTOWUP	GTIOC 2A_A	-	CTX0	CTS0_ RTS0/ SS0	-	-	SSLA0 _A	-	-	-	-	-	-	-	-	-	LCD_TCO N1_A
M3	130	M1	106	73	-	KR02	P102	D02[A02/ D02]	DQ02	AGTO0	GTOWLO	GTIOC 2B_A	-	CRX0	SCK0	-	-	RSPC KA_A	-	-	-	-	-	ADTRG 0	-	-	-	LCD_TCO N0_A
N2	131	M2	107	74	-	IRQ1/ KR01	P101	D01[A01/ D01]	DQ01	AGTEE0	GTETRGB	GTIOC 5A	-	-	TXD0/ MOSI0 /SDA0	CTS1_ RTS1/ SS1	SDA1 _B	MOSIA _A	-	-	-	-	-	-	-	-	-	LCD_CLK_ A
P1	132	N1	108	75	-	IRQ2/ KR00	P100	D00[A00/ D00]	DQ00	AGTIO0	GTETRGA	GTIOC 5B	-	-	RXD0/ MISO0 /SCL0	SCK1	SCL1 _B	MISOA _A	-	-	-	-	-	-	-	-	-	LCD_EXT CLK_A
N3	133	L2	109	-	-	-	P800	D14[A14/ D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R1	134	N2	110	-	-	-	P801	D15[A15/ D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT4 _A	-	-	-	-	-
P2	135	-	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT5 _A	-	-	-	-	LCD_DATA 02_B
R2	136	-	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT6 _A	-	-	-	-	LCD_DATA 01_B
P3	137	-	-	-			-	P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT7 _A	-	-	-	-	LCD_DATA 00_B
N4	138	N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M4	139	M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R3	140	K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC 11A	-	USB_ VBUS EN	-	-	-	QSPC LK	-	-	-	-	SD1 CLK_ A	AN016	IVREF0	-	-
P4	141	M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC 11B	-	USB_ OVR_ CUR A	-	TXD5/ MOSI5 /SDA5	-	QSSL	-	-	-	-	SD1 CMD _A	AN116	IVREF1	-	-
R4	142	L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC 12A	-	USB_ OVR_ CUR B	-	RXD5/ MISO5 /SCL5	-	QIO0	-	-	-	-	SD1 DAT0 _A	AN017	IVCMP0	-	-
N5	143	K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC 12B	-	USB_ EXIC EN	CTS6_ RTS6/ SS6	SCK5	-	QIO1	-	-	-	-	SD1 DAT1 _A	AN117	-	-	-
P5	144	L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC 13A	-	USB_ ID	SCK6	CTS5_ RTS5/ SS5	-	QIO2	-	-	-	-	SD1 DAT2 _A	AN018	-	-	-
P6	145	K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC 13B	-	-	RXD6/ MISO6 /SCL6	-	-	QIO3	-	-	-	-	SD1 DAT3 _A	AN118	-	-	-

Pin number								Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
R5	146	L6	119	-	-	IRQ15	P506	-	-	-	-	-	-	-	TXD6/MOSI6/SDA6	-	-	-	-	-	-	-	SD1CD_A	AN019	-	-	-
N6	147	-	-	-	-	-	P507	-	-	-	-	-	-	-	-	CTS5_RTS5/SS5	-	-	-	-	-	-	SD1WP_A	AN119	-	-	-
R6	148	N4	120	81	-	-	P508	-	-	-	-	-	-	-	SCK6	SCK5	-	-	-	-	-	-	-	AN020	-	-	-
M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	151	M6	123	84	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-	-
R7	152	N6	124	85	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-	-
P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	159	-	-	-	-	IRQ14-DS	P010	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN103	-	-	-
M9	160	M9	131	-	-	IRQ13-DS	P009	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN004	-	-	-
P10	161	N9	132	92	-	IRQ12-DS	P008	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-	-
M6	162	K7	133	93	-	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS100/AN107	-	-	-
N10	163	L9	134	94	-	IRQ11-DS	P006	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-	-
R10	164	K8	135	95	-	IRQ10-DS	P005	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-	-
P11	165	K9	136	96	-	IRQ9-DS	P004	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-	-
M5	166	K10	137	97	-	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS000/AN007	-	-	-
R11	167	M10	138	98	-	IRQ8-DS	P002	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-	-
N11	168	N10	139	99	-	IRQ7-DS	P001	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-	-
R12	169	L10	140	100	-	IRQ6-DS	P000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-	-
M10	170	N11	141	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M11	171	N12	142	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P12	172	-	-	-	-	-	P806	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_EXTCLK_B
R13	173	-	-	-	-	-	P805	-	-	-	-	-	-	-	-	TXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA17_B
N12	174	-	-	-	-	-	P513	-	-	-	-	-	-	-	-	RXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_B
R14	175	M11	143	-	-	IRQ14	P512	-	-	-	-	GTIOC0A	-	CTX1	TXD4/MOSI4/SDA4	-	SCL2	-	-	-	-	-	-	-	-	-	VSYNC
P13	176	M12	144	-	-	IRQ15	P511	-	-	-	-	GTIOC0B	-	CRX1	RXD4/MISO4/SCL4	-	SDA2	-	-	-	-	-	-	-	-	-	PCKO

Note: Some pin names have the added suffix of _A, _B, and _C. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix.

针号								Extbus		Timers				通讯接口										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	电源系统，时钟，调试，CAC	Interrupt	I/O port	外部总线	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
R5	146	L6	119	-	-	IRQ15	P506	-	-	-	-	-	-	-	TXD6/MOSI6/SDA6	-	-	-	-	-	-	-	SD1CD_A	AN019	-	-	-
N6	147	-	-	-	-	-	P507	-	-	-	-	-	-	-	-	CTS5_RTS5/SS5	-	-	-	-	-	-	SD1WP_A	AN119	-	-	-
R6	148	N4	120	81	-	-	P508	-	-	-	-	-	-	-	SCK6	SCK5	-	-	-	-	-	-	-	AN020	-	-	-
M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	151	M6	123	84	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-	-
R7	152	N6	124	85	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-	-
P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	159	-	-	-	-	IRQ14-DS	P010	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN103	-	-	-
M9	160	M9	131	-	-	IRQ13-DS	P009	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN004	-	-	-
P10	161	N9	132	92	-	IRQ12-DS	P008	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-	-
M6	162	K7	133	93	-	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS100/AN107	-	-	-
N10	163	L9	134	94	-	IRQ11-DS	P006	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-	-
R10	164	K8	135	95	-	IRQ10-DS	P005	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-	-
P11	165	K9	136	96	-	IRQ9-DS	P004	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-	-
M5	166	K10	137	97	-	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS000/AN007	-	-	-
R11	167	M10	138	98	-	IRQ8-DS	P002	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-	-
N11	168	N10	139	99	-	IRQ7-DS	P001	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-	-
R12	169	L10	140	100	-	IRQ6-DS	P000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-	-
M10	170	N11	141	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M11	171	N12	142	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P12	172	-	-	-	-	-	P806	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_EXTCLK_B
R13	173	-	-	-	-	-	P805	-	-	-	-	-	-	-	-	TXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA17_B
N12	174	-	-	-	-	-	P513	-	-	-	-	-	-	-	-	RXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_B
R14	175	M11	143	-	-	IRQ14	P512	-	-	-	-	GTIOC0A	-	CTX1	TXD4/MOSI4/SDA4	-	SCL2	-	-	-	-	-	-	-	-	-	VSYNC
P13	176	M12	144	-	-	IRQ15	P511	-	-	-	-	GTIOC0B	-	CRX1	RXD4/MISO4/SCL4	-	SDA2	-	-	-	-	-	-	-	-	-	PCKO

Note: 一些引脚名称添加了_A、_B和_C的后缀。分配GPT、IIC、SPI、SSIE、ETHERC(RMII)、SDHI和GLCDC功能时，选择具有相同后缀的功能管脚。

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr.

Figure 2.1 shows the timing conditions.

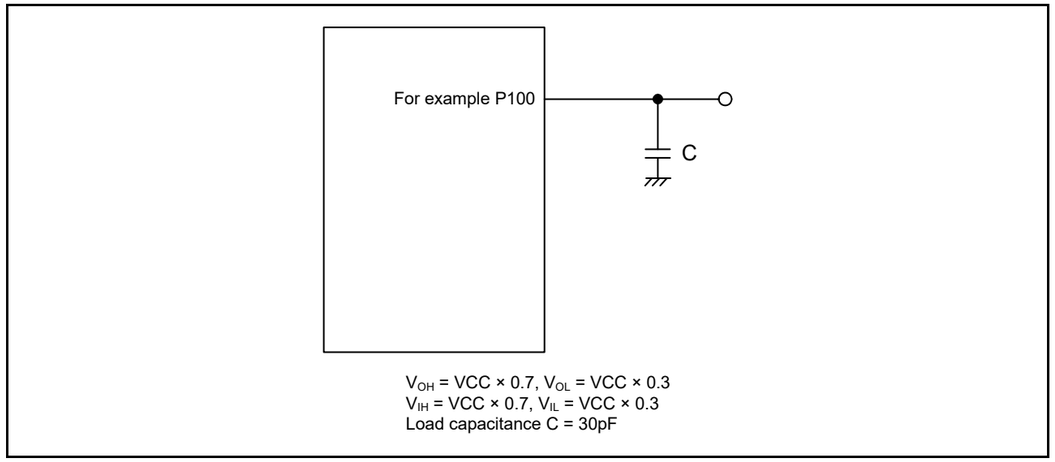


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation, however make sure to adjust driving abilities of each pins to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT power supply voltage	VBATT	-0.3 to +4.0	V
Input voltage (except for 5V-tolerant ports*1)	V_{in}	-0.3 to VCC + 0.3	V
Input voltage (5V-tolerant ports*1)	V_{in}	-0.3 to + VCC + 4.0 (max 5.8)	V
Reference power supply voltage	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
Analog power supply voltage	AVCC0 *2	-0.3 to +4.0	V
USBHS power supply voltage	VCC_USBHS	-0.3 to +4.0	V
USBHS analog power supply voltage	AVCC_USBHS	-0.3 to +4.0	V
Analog input voltage (except for P000 to P007)	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P007) when PGA differential input is disabled	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002, P004 to P006) when PGA differential input is enabled	V_{AN}	-1.3 to AVCC0 + 0.3	V
Analog input voltage (P003, P007) when PGA differential input is enabled	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3,*4,*5	T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

2. 电气特性

除非另有规定，MCU的电气特性在以下条件下定义：

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr.

图2.1显示了时序条件。

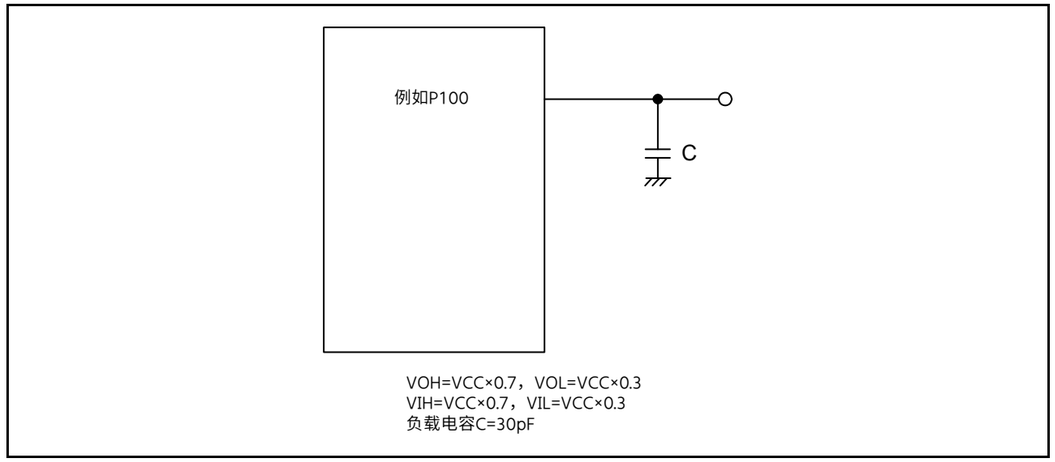


Figure 2.1 输入或输出定时测量条件

每个外设的时序规范的测量条件是推荐的，以获得最佳的外设操作，但请确保调整每个引脚的驱动能力以满足您的条件。

2.1 绝对最大额定值

Table 2.1 绝对最大额定值

Parameter	Symbol	Value	Unit
电源电压	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT电源电压	VBATT	-0.3 to +4.0	V
输入电压（5V耐受端口除外*1）	V_{in}	-0.3 to VCC + 0.3	V
输入电压（5V容限端口*1）	V_{in}	-0.3 to + VCC + 4.0 (max 5.8)	V
参考电源电压	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
模拟电源电压	AVCC0 *2	-0.3 to +4.0	V
USBHS电源电压	VCC_USBHS	-0.3 to +4.0	V
USBHS模拟电源电压	AVCC_USBHS	-0.3 to +4.0	V
模拟输入电压（P000至P007除外）	V_{AN}	-0.3 to AVCC0 + 0.3	V
PGA差分输入禁用时的模拟输入电压（P000至P007）	V_{AN}	-0.3 to AVCC0 + 0.3	V
启用PGA差分输入时的模拟输入电压（P000至P002、P004至P006）	V_{AN}	-1.3 to AVCC0 + 0.3	V
PGA差分输入启用时的模拟输入电压(P003 P007)	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3,*4,*5	T_{opr}	-40 to +85 -40 to +105	°C
贮存温度	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 2.2.1, T_j/T_a Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when T_a = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 5. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/SDRAM is not used	2.7	-	3.6	V
		When USB/SDRAM is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
VBATT power supply voltage	VBATT		1.8	-	3.6	V
Analog power supply voltages	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter nor the comparator is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics
Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.
Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature to 85°C, then Tj max is 105°C, otherwise, 125°C.

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Note 1. 端口P205、P206、P400、P401、P407至P415、P511、P512、P708至P713和PB01可承受5V。
Note 2. 将AVCC0和VCC_USB连接到VCC。
Note 3. 请参阅第2.2.1节，TjTa定义。
Note 4. 有关在Ta=+85°C至+105°C时降额运行的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。
Note 5. 工作温度上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分Numbering.

Table 2.2 推荐工作条件

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC	不使用USBSDRAM时	2.7	-	3.6	V
		使用USBSDRAM时	3.0	-	3.6	V
	VSS		-	0	-	V
USB电源电压	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
VBATT电源电压	VBATT		1.8	-	3.6	V
模拟电源电压	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. 将AVCC0连接到VCC。当AD转换器、DA转换器和比较器均未使用时，请勿将AVCC0、VREFH/VREFH0、AVSS0和VREFL/VREFL0引脚悬空。将AVCC0和VREFH/VREFH0引脚分别连接到VCC，将AVSS0和VREFL/VREFL0引脚分别连接到VSS。

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics
条件：工作温度(Ta)-40至+105°C的产品

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+ICCmax×VCC。
Note 1. 工作温度上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分编号。如果部件号显示工作温度为85°C，则Tjmax为105°C，否则为125°C。

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Parameter				Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI (except RSPCK)		V_{IH}	VCC × 0.8	-	-	V
				V_{IL}	-	-	VCC × 0.2	
		D00 to D15, DQ00 to DQ15		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
		ETHERC		V_{IH}	2.3	-	-	
				V_{IL}	-	-	VCC × 0.2	
		IIC (SMBus)*1		V_{IH}	2.1	-	-	
				V_{IL}	-	-	0.8	
		IIC (SMBus)*2		V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	0.8	
Schmitt trigger input voltage		IIC (except for SMBus)*1		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2		V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		5V-tolerant ports*3, *7		V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.2	
				ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3
					V_{IL}	-	-	V_{BATT} × 0.2
					ΔV_T	V_{BATT} × 0.05	-	-
				When VCC power supply is selected	V_{IH}	VCC × 0.8	-	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	-	VCC + 0.3
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
		Other input pins*4			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
	Ports	5V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)
					V_{IL}	-	-	VCC × 0.2
		Other input pins*6			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 23 pins).

2.2.2 I O V I H

Table 2.4 I O V I H

Parameter				Symbol	Min	Typ	Max	Unit
输入电压（施密特触发器输入引脚除外）	外设功能引脚	EXTAL（外部时钟输入）、WAIT、SPI（除RSPCK)		V_{IH}	VCC × 0.8	-	-	V
				V_{IL}	-	-	VCC × 0.2	
		D00 to D15, DQ00 to DQ15		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
		ETHERC		V_{IH}	2.3	-	-	
				V_{IL}	-	-	VCC × 0.2	
		IIC (SMBus)*1		V_{IH}	2.1	-	-	
				V_{IL}	-	-	0.8	
		IIC (SMBus)*2		V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	0.8	
施密特触发器输入电压		IIC (except for SMBus)*1		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2		V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		5V-tolerant ports*3, *7		V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.2	
				ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	使用备用电池时 Function	选择VBATT电源时	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3
					V_{IL}	-	-	V_{BATT} × 0.2
					ΔV_T	V_{BATT} × 0.05	-	-
				选择VCC电源时	V_{IH}	VCC × 0.8	-	更高的电压VCC+0.3V或VBATT+0.3V
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
			不使用备用电池时 Function		V_{IH}	VCC × 0.8	-	VCC + 0.3
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
		其他输入引脚*4			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
	Ports	5V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)
					V_{IL}	-	-	VCC × 0.2
		其他输入引脚*6			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).
Note 3. RES和与P205、P206、P400、P401、P407至P415、P511、P512、P708至P713、PB01相关的外围功能引脚（共23个引脚）。

Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown might occur because the 5 V-tolerant ports are electrically controlled to not violate the breakdown voltage.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P008 to P010, P201	-	I_{OH}	-	--	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
Permissible output current (max value per pin)	Ports P008 to P010, P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
Permissible output current (max value total pins)	Maximum of all output pins		ΣI_{OH} (max)	-	-	-80	mA
			ΣI_{OL} (max)	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. 除表中已描述的外围功能引脚外的所有输入引脚。
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).
Note 6. 除表中已描述的端口外的所有输入引脚。
Note 7. 当VCC小于2.7V时，5V容限端口的输入电压应小于3.6V，否则可能会发生击穿，因为5V容限端口被电控不超过击穿电压。

2.2.3 我爱我哦

Table 2.5 我爱我哦

Parameter			Symbol	Min	Typ	Max	Unit
允许输出电流（每个引脚的平均值）	端口P008至P010、P201	-	I_{OH}	-	--	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	端口P205、P206、P407至P415、P602、P708至P713、PB01（共19针）	低驱*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		中驱*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		高驱*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	其他输出引脚*4	低驱*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		中驱*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		高驱*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
允许输出电流（每个引脚的最大值）	端口P008至P010、P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	端口P205、P206、P407至P415、P602, P708 to P713, PB01 (total 19 pins)	低驱*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		高驱*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	其他输出引脚*4	低驱*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		高驱*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
允许输出电流（最大总引脚数）	所有输出引脚的最大值		ΣI_{OH} (max)	-	-	-80	mA
			ΣI_{OL} (max)	-	-	80	mA

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流是指在100µs内测得的电流平均值。

Note 1. 这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。
Note 2. 这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。
Note 3. 这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Note 4. Except for P000 to P007, P200, which are input ports.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	IIC*1		V_{OL}	-	-	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	-	0.4	-		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC		V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.4		I_{OL} = 1.0 mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)*2		V_{OH}	VCC - 1.0	-	-		I_{OH} = -20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\|I_{in}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Ports P000 to P002, P004 to P006, P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports		$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for ports P000 to P007, P200)			-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to PB (except for ports P000 to P007)		I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, and ports P003, P007, P014, P015, P400, P401, P511, P512		C_{in}	-	-	16	pF	Vbias = 0V Vamp = 20mV f = 1 MHz T_a = 25°C
	Other input pins			-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register.
The selected driving ability is retained in Deep Software Standby mode.
Note 3. P0nPFS.ASEL (n = 3 or 7) = 1.
Note 4. P0nPFS.ASEL (n = 3 or 7) = 0.

Note 4. 除了P000至P007、P200为输入端口。

2.2.4 IOVOH VOL和其他特性

Table 2.6 IOVOH、VOL和其他特性

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
输出电压	IIC		V_{OL}	-	-	0.4	V	我OL=3.0毫安
			V_{OL}	-	-	0.6		我OL=6.0毫安
	IIC*1		V_{OL}	-	-	0.4		IOL=15.0mA(ICFER.FMPE=1)
			V_{OL}	-	0.4	-		IOL=20.0mA(ICFER.FMPE=1)
	ETHERC		V_{OH}	VCC - 0.5	-	-		IOH=-1.0毫安
			V_{OL}	-	-	0.4		我OL=1.0毫安
	端口P205、P206、P407至P415、P602, P708 to P713, PB01 (total 19 pins)*2		V_{OH}	VCC - 1.0	-	-		我OH=-20毫安VCC=3.3V
			V_{OL}	-	-	1.0		我OL=20毫安VCC=3.3V
	其他输出引脚		V_{OH}	VCC - 0.5	-	-		IOH=-1.0毫安
			V_{OL}	-	-	0.5		我OL=1.0毫安
输入漏电流	RES		$\|I_{in}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	端口P000至P002、P004至P006、P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5V-tolerant ports		$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	其他端口（端口P000至P007、P200除外）			-	-	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉MOS电流	端口P0到PB（端口除外P000 to P007)		I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
输入电容	USB_DP、USB_DM和端口P003, P007, P014, P015, P400, P401, P511, P512		C_{in}	-	-	16	pF	Vbias = 0V Vamp = 20mV f = 1 MHz T_a = 25°C
	其他输入引脚			-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. 这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。
在深度软件待机模式下会保留所选的驾驶能力。
Note 3. P0nPFS.ASEL (n = 3 or 7) = 1.
Note 4. P0nPFS.ASEL (n = 3 or 7) = 0.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	137*2	mA	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	21	-		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		-	34	-		
			All peripheral clocks disabled, while (1) code executing from flash*5, *6		-	14	-		
		Sleep mode*5, *6			-	12	46		
		Increase during BGO operation	Data flash P/E		-	6	-		
			Code flash P/E		-	8	-		
	Low-speed mode*5				-	2.4	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	2	-		ICLK = 32.768 kHz
	Software Standby mode				-	1.8	18		Ta ≤ 85°C
					-	1.8	28		Ta ≤ 105°C
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			-	30	79	μA	Ta ≤ 85°C
					-	30	113	μA	Ta ≤ 105°C
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled		-	13	33	μA	Ta ≤ 85°C
					-	13	40		Ta ≤ 105°C
			Power-on reset circuit low-power function enabled		-	6.3	28		Ta ≤ 85°C
					-	6.3	34		Ta ≤ 105°C
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	5	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	1.5	-		-
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		-	0.9	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.3	-		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		-	1.1	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.8	-		V_{BATT} = 3.3 V, VCC = 0 V
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1unit)				-	100	150	μA	-
	Temperature sensor				-	0.1	0.2	mA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.2	mA	-
			With AMP output		-	0.6	1.1	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)*8				-	2	8	μA	-
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	-	70	120	μA	-
	Waiting for 12-bit A/D conversion (unit 0)				-	0.07	0.5	μA	-
	ADC12 in standby modes (unit 0)				-	0.07	0.5	μA	-
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)			AI_{REFH}	-	70	120	μA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.4	mA	-
			With AMP ouput		-	0.1	0.4	mA	-
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion				-	0.07	0.8	μA	-
	ADC12 unit 1 in standby modes				-	0.07	0.8	μA	-

2.2.5 工作和待机电流

Table 2.7 工作和待机电流(1of2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
供电电流*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	137*2	mA	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	21	-		
		正常模式	启用所有外设时钟，同时(1)代码从闪存执行*4		-	34	-		
			禁用所有外设时钟，同时(1)代码从闪存执行*5、*6		-	14	-		
		睡眠模式*5、*6			-	12	46		
		BGO运行期间增加	数据闪存PE		-	6	-		
			代码闪存PE		-	8	-		
	Low-speed mode*5				-	2.4	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	2	-		ICLK = 32.768 kHz
	软件待机模式				-	1.8	18		Ta ≤ 85°C
					-	1.8	28		Ta ≤ 105°C
	深度软件待机模式	为备用SRAM和USB恢复检测单元供电			-	30	79	μA	Ta ≤ 85°C
					-	30	113	μA	Ta ≤ 105°C
		未向SRAM或USB恢复检测单元供电	上电复位电路低功耗功能禁用		-	13	33	μA	Ta ≤ 85°C
					-	13	40		Ta ≤ 105°C
			上电复位电路低功耗功能启用		-	6.3	28		Ta ≤ 85°C
					-	6.3	34		Ta ≤ 105°C
		RTC和AGT运行时增加	使用低速片上振荡器(LOCO)时		-	5	-		-
			当使用用于低时钟负载的晶体振荡器时		-	1.0	-		-
			当使用标准时钟负载的晶体振荡器时		-	1.5	-		-
		VCC关闭时RTC运行（具有电池备份功能，只有RTC和副时钟振荡器运行）	当使用用于低时钟负载的晶体振荡器时		-	0.9	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.3	-		V_{BATT} = 3.3 V, VCC = 0 V
			当使用标准时钟负载的晶体振荡器时		-	1.1	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.8	-		V_{BATT} = 3.3 V, VCC = 0 V
模拟电源电流	在12位AD转换期间			AI_{CC}	-	0.8	1.1	mA	-
	在使用SHamp进行12位AD转换期间				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1unit)				-	100	150	μA	-
	温度感应器				-	0.1	0.2	mA	-
	DA转换期间（每单位）		无AMP输出		-	0.1	0.2	mA	-
			带AMP输出		-	0.6	1.1	mA	-
	等待AD、DA转换（所有单位）				-	0.9	1.6	mA	-
	ADC12、DAC12处于待机模式（所有单元）*8				-	2	8	μA	-
参考电源电流(VREFH0)	在12位AD转换期间（单元0）			AI_{REFH0}	-	70	120	μA	-
	等待12位AD转换（单元0）				-	0.07	0.5	μA	-
	ADC12处于待机模式（单元0）				-	0.07	0.5	μA	-
参考电源电流(VREFH)	在12位AD转换期间（单元1）			AI_{REFH}	-	70	120	μA	-
	DA转换期间（每单位）		无AMP输出		-	0.1	0.4	mA	-
			带AMP输出		-	0.1	0.4	mA	-
	等待12位AD（单元1）、DA（所有单元）转换				-	0.07	0.8	μA	-
	ADC12单元1处于待机模式				-	0.07	0.8	μA	-

Table 2.7 Operating and standby current (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
USB operating current	Low speed	USB	$I_{CCUSBLS}$	-	3.5	6.5	mA	VCC_USB
		USBHS		-	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	Full speed	USB	$I_{CCUSBFS}$	-	4.0	10.0	mA	VCC_USB
		USBHS		-	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	High speed	USBHS	$I_{CCUSBHS}$	-	50	65	mA	VCC_USBHS = AVCC_USBHS
	Standby mode (direct power down)	USBHS	$I_{CCUSBSBY}$	-	0.5	4.5	µA	VCC_USBHS = AVCC_USBHS

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. ICC depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)
ICC Max. = 0.84 × f + 37 (max. operation in High-speed mode)
ICC Typ. = 0.09 × f + 3.7 (normal operation in High-speed mode)
ICC Typ. = 0.6 × f + 1.8 (Low-speed mode 1)
ICC Max. = 0.08 × f + 37 (Sleep mode).
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. When using ETHERC, GLCDC, DRW, and JPEG, PCLKA frequency is such that PCLKA = ICLK.
Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 Module Stop bit) and MSTPCRD.MSTPD15 (ADC121 Module Stop bit) are in the module-stop state. See section 47.6.8, Available Functions and Register Settings of AN000 to AN002, AN007, AN100 to AN102, and AN107 in User's Manual.

Table 2.7 工作和待机电流(2of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
USB工作电流	低速	USB	$I_{CCUSBLS}$	-	3.5	6.5	mA	VCC_USB
		USBHS		-	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	全速	USB	$I_{CCUSBFS}$	-	4.0	10.0	mA	VCC_USB
		USBHS		-	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	高速	USBHS	$I_{CCUSBHS}$	-	50	65	mA	VCC_USBHS = AVCC_USBHS
	待机模式（直接断电）	USBHS	$I_{CCUSBSBY}$	-	0.5	4.5	µA	VCC_USBHS = AVCC_USBHS

Note 1. 电源电流值是在所有输出引脚空载且所有输入上拉MOS晶体管处于关闭状态的情况下。
Note 2. 使用提供给外围功能的时钟进行测量。这不包括BGO操作。
Note 3. ICC取决于f(ICLK)，如下所示。（ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK=2:2:1:1:2:1:1）
ICC最大值=0.84×f+37（高速模式下的最大操作）
ICC典型值。=0.09×f+3.7（高速模式下的正常操作）
ICC Typ. = 0.6 × f + 1.8 (Low-speed mode 1)
ICC Max. = 0.08 × f + 37 (Sleep mode).
Note 4. 这不包括BGO操作。
Note 5. 在该状态下停止向外围设备提供时钟信号。这不包括BGO操作。
Note 6. FCLK、BCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频(3.75MHz)。
Note 7. 当使用ETHERC、GLCDC、DRW和JPEG时，PCLKA频率使得PCLKA=ICLK。
Note 8. 当MCU处于软件待机模式或MSTPCRD.MSTPD16（ADC120模块停止位）和MSTPCRD.MSTPD15（ADC121模块停止位）处于模块停止状态。请参阅第47.6.8节，可用功能和AN000到AN002、AN007、AN100到AN102和AN107的寄存器设置在用户手册中。

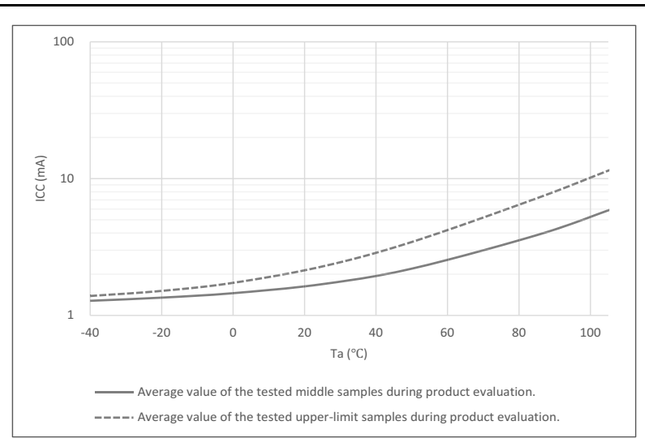


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

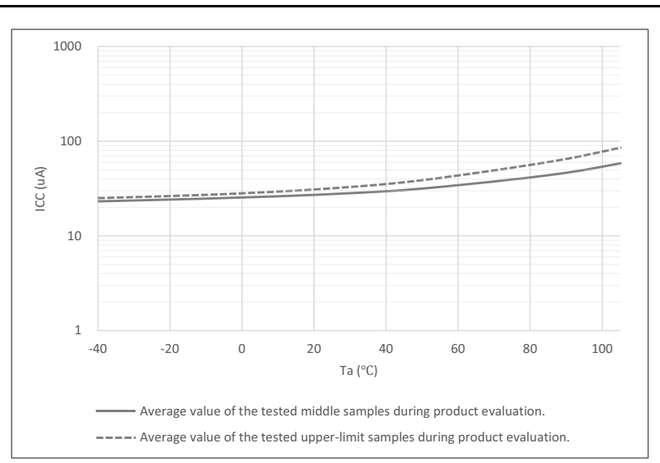


Figure 2.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)

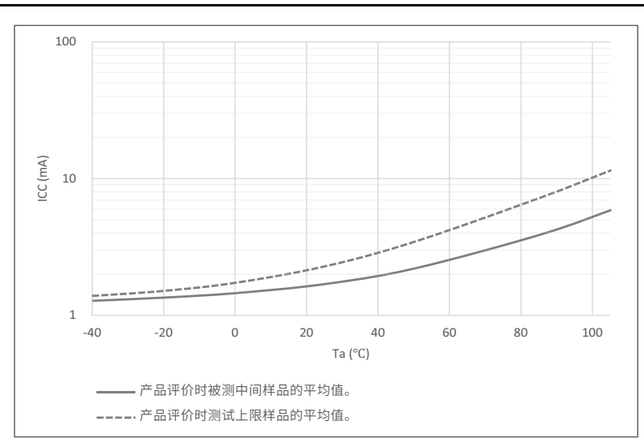


Figure 2.2 软件待机模式下的温度依赖性（参考数据）

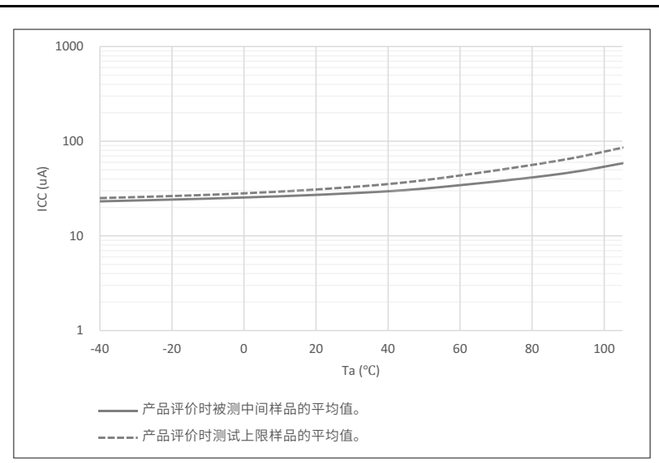


Figure 2.3 深度软件待机模式下的温度依赖性，为待机SRAM供电和USB恢复检测单元（参考数据）

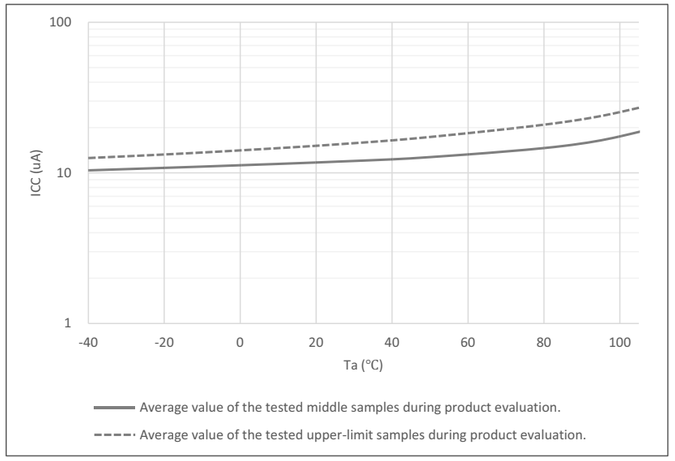


Figure 2.4 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low-power function disabled (reference data)**

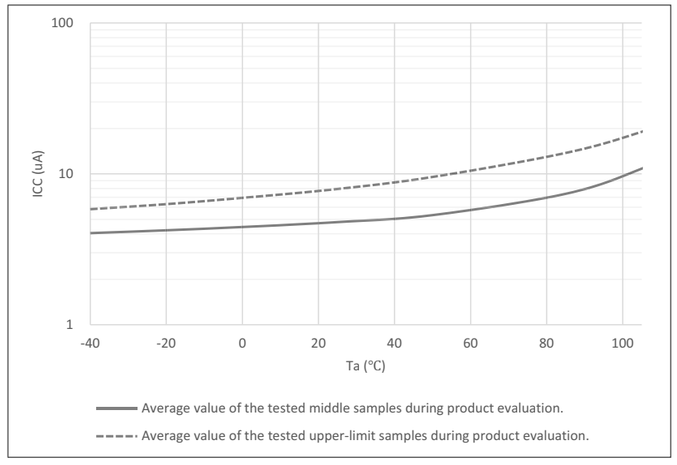


Figure 2.5 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low-power function enabled (reference data)**

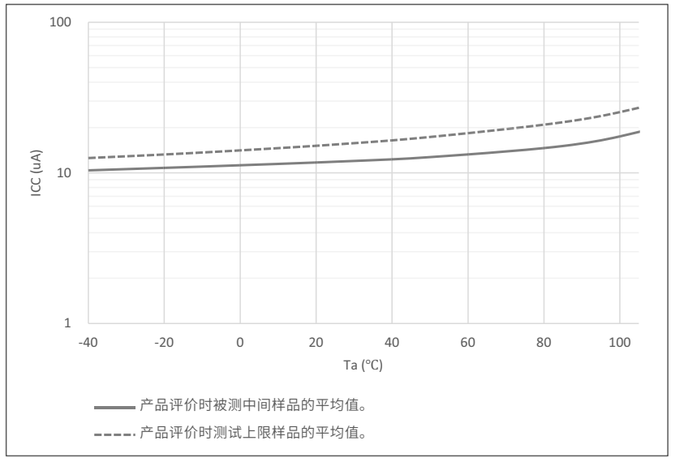


Figure 2.4 **深度软件待机模式下的温度依赖性，未向SRAM或USB恢复检测单元供电，上电复位电路低功耗功能禁用（参考数据）**

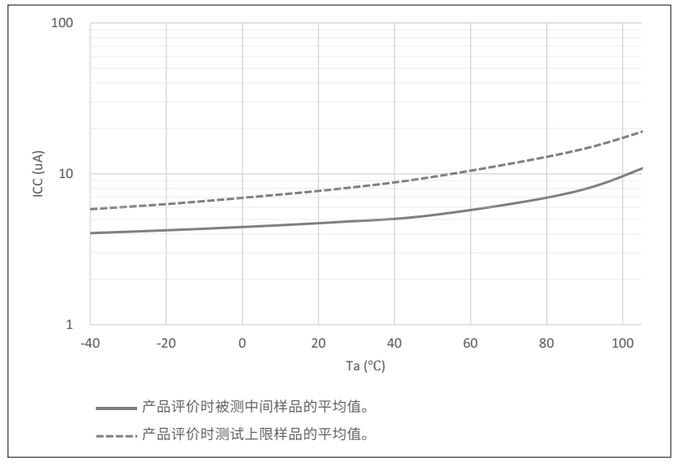


Figure 2.5 **深度软件待机模式下的温度依赖性，不向SRAM或USB恢复检测单元供电，启用上电复位电路低功耗功能禁用（参考数据）**

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.8 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	-	20	ms/V	-
	Voltage monitor 0 reset enabled at startup		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

Table 2.9 Rise and fall gradient and ripple frequency characteristics
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r (VCC)}$	-	-	10	kHz	Figure 2.6 $V_{r (VCC)}$ ≤ VCC × 0.2
		-	-	1	MHz	Figure 2.6 $V_{r (VCC)}$ ≤ VCC × 0.08
		-	-	10	MHz	Figure 2.6 $V_{r (VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

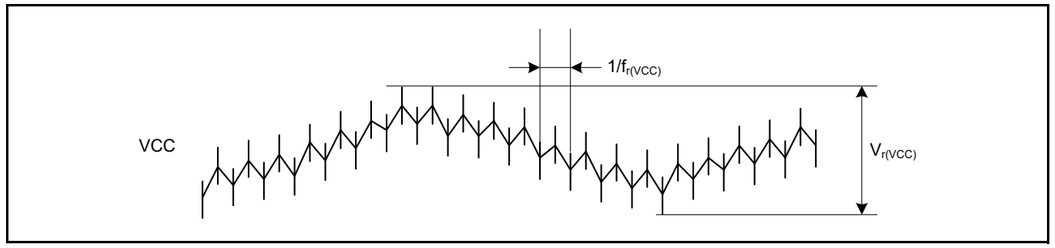


Figure 2.6 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.10 Operation frequency value in high-speed mode

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)		f	-	-	120	MHz
	Peripheral module clock (PCLKA)*2			-	-	120	
	Peripheral module clock (PCLKB)*2			-	-	60	
	Peripheral module clock (PCLKC)*2			-*3	-	60	
	Peripheral module clock (PCLKD)*2			-	-	120	
	Flash interface clock (FCLK)*2			-*1	-	60	
	External bus clock (BCLK)*2			-	-	120	
	EBCLK pin output			-	-	60	
	SDCLK pin output	VCC ≥ 3.0 V		-	-	120	

2.2.6 VCC上升和下降梯度和纹波频率

Table 2.8 上升和下降梯度特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.0084	-	20	ms/V	-
	启动时启用电压监视器0复位		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. 在引导模式下，无论OFS1.LVDAS位的值如何，电压监视器0的复位均被禁用。
Note 2. 这适用于使用VBATT时。

Table 2.9 升降梯度和纹波频率特性
纹波电压必须在VCC上限(3.6V)和下限(2.7V)之间的范围内满足允许的纹波频率fr(VCC)。当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r (VCC)}$	-	-	10	kHz	Figure 2.6 $V_{r (VCC)}$ ≤ VCC × 0.2
		-	-	1	MHz	Figure 2.6 $V_{r (VCC)}$ ≤ VCC × 0.08
		-	-	10	MHz	Figure 2.6 $V_{r (VCC)}$ ≤ VCC × 0.06
允许电压变化上升下降梯度	dt/dVCC	1.0	-	-	ms/V	当VCC变化超过VCC±10%

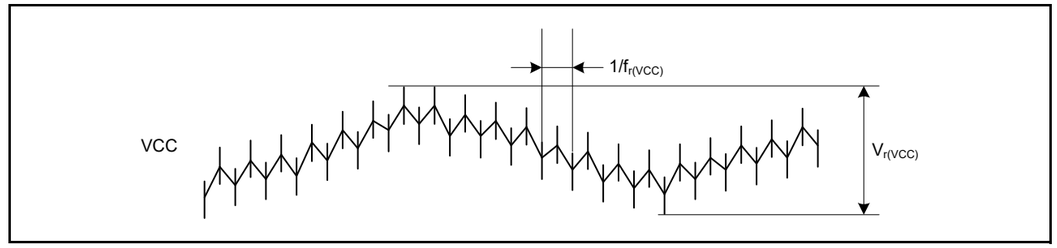


Figure 2.6 纹波波形

2.3 交流特性

2.3.1 Frequency

Table 2.10 高速模式下的运行频率值

Parameter			Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK*2)		f	-	-	120	MHz
	外设模块时钟(PCLKA)*2			-	-	120	
	外设模块时钟(PCLKB)*2			-	-	60	
	外设模块时钟(PCLKC)*2			-*3	-	60	
	外设模块时钟(PCLKD)*2			-	-	120	
	闪存接口时钟(FCLK)*2			-*1	-	60	
	外部总线时钟(BCLK)*2			-	-	120	
	EBCLK引脚输出			-	-	60	
	SDCLK 引脚输出	VCC ≥ 3.0 V		-	-	120	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.11 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2		-	-	1	
	Peripheral module clock (PCLKB)*2		-	-	1	
	Peripheral module clock (PCLKC)*2,*3		-*3	-	1	
	Peripheral module clock (PCLKD)*2		-	-	1	
	Flash interface clock (FCLK)*1, *2		-	-	1	
	External bus clock (BCLK)		-	-	1	
	EBCLK pin output		-	-	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 2.12 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	27.8	-	37.7	kHz
	Peripheral module clock (PCLKA)*2		-	-	37.7	
	Peripheral module clock (PCLKB)*2		-	-	37.7	
	Peripheral module clock (PCLKC)*2,*3		-	-	37.7	
	Peripheral module clock (PCLKD)*2		-	-	37.7	
	Flash interface clock (FCLK)*1, *2		27.8	-	37.7	
	External bus clock (BCLK)*2		-	-	37.7	
	EBCLK pin output		-	-	37.7	

Note 1. Programming or erasing the flash memory is disable in Subosc-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.13 Clock timing except for sub-clock oscillator (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	t_{Bcyc}	16.6	-	-	ns	Figure 2.7
EBCLK pin output high pulse width	t_{CH}	3.3	-	-	ns	
EBCLK pin output low pulse width	t_{CL}	3.3	-	-	ns	
EBCLK pin output rise time	t_{Cr}	-	-	5.0	ns	
EBCLK pin output fall time	t_{Cf}	-	-	5.0	ns	
SDCLK pin output cycle time	t_{SDcyc}	8.33	-	-	ns	
SDCLK pin output high pulse width	t_{CH}	1.0	-	-	ns	
SDCLK pin output low pulse width	t_{CL}	1.0	-	-	ns	
SDCLK pin output rise time	t_{Cr}	-	-	3.0	ns	
SDCLK pin output fall time	t_{Cf}	-	-	3.0	ns	

Note 1. 在对闪存进行编程或擦除时，FCLK必须以至少4MHz的频率运行。
Note 2. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率。
Note 3. 使用ADC12时，PCLKC频率必须至少为1MHz。

Table 2.11 低速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	-	-	1	MHz
	外设模块时钟(PCLKA)*2		-	-	1	
	外设模块时钟(PCLKB)*2		-	-	1	
	外设模块时钟(PCLKC)*2 *3		-*3	-	1	
	外设模块时钟(PCLKD)*2		-	-	1	
	Flash接口时钟(FCLK)*1 *2		-	-	1	
	外部总线时钟(BCLK)		-	-	1	
	EBCLK引脚输出		-	-	1	

Note 1. 在低速模式下禁止对闪存进行编程或擦除。
Note 2. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率。
Note 3. 使用ADC12时，PCLKC频率必须设置为至少1MHz。

Table 2.12 Subosc-speed模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	27.8	-	37.7	kHz
	外设模块时钟(PCLKA)*2		-	-	37.7	
	外设模块时钟(PCLKB)*2		-	-	37.7	
	外设模块时钟(PCLKC)*2 *3		-	-	37.7	
	外设模块时钟(PCLKD)*2		-	-	37.7	
	Flash接口时钟(FCLK)*1 *2		27.8	-	37.7	
	外部总线时钟(BCLK)*2		-	-	37.7	
	EBCLK引脚输出		-	-	37.7	

Note 1. 在Subosc速度模式下，禁止对闪存进行编程或擦除。
Note 2. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率。
Note 3. ADC12不能使用。

2.3.2 时钟时序

Table 2.13 除副时钟振荡器外的时钟时序（2个中的1个）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
EBCLK引脚输出周期时间	t_{Bcyc}	16.6	-	-	ns	Figure 2.7
EBCLK引脚输出高脉冲宽度	t_{CH}	3.3	-	-	ns	
EBCLK引脚输出低脉冲宽度	t_{CL}	3.3	-	-	ns	
EBCLK引脚输出上升时间	t_{Cr}	-	-	5.0	ns	
EBCLK引脚输出下降时间	t_{Cf}	-	-	5.0	ns	
SDCLK 引脚输出周期时间	t_{SDcyc}	8.33	-	-	ns	
SDCLK 引脚输出高脉冲宽度	t_{CH}	1.0	-	-	ns	
SDCLK 引脚输出低脉冲宽度	t_{CL}	1.0	-	-	ns	
SDCLK 引脚输出上升时间	t_{Cr}	-	-	3.0	ns	
SDCLK 引脚输出下降时间	t_{Cf}	-	-	3.0	ns	

Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	41.66	-	-	ns	Figure 2.8
EXTAL external clock input high pulse width		t_{EXH}	15.83	-	-	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	-	-	ns	
EXTAL external clock rise time		t_{EXr}	-	-	5.0	ns	
EXTAL external clock fall time		t_{EXf}	-	-	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	-	24	MHz	-
Main clock oscillation stabilization wait time (crystal) *1		$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 2.9
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	-	-	60.4	µs	Figure 2.10
ILOCO clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	-	-	15.0	µs	-
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		-40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	-	-	64.7	µs	-
FLL stabilization wait time		t_{FLLWT}	-	-	1.8	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	µs	Figure 2.11

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	*1	s	Figure 2.12

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. Two times the value shown is recommended.

Table 2.13 除副时钟振荡器外的时钟时序(2of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间		t_{EXcyc}	41.66	-	-	ns	Figure 2.8
EXTAL外部时钟输入高脉冲宽度		t_{EXH}	15.83	-	-	ns	
EXTAL外部时钟输入低脉冲宽度		t_{EXL}	15.83	-	-	ns	
EXTAL外部时钟上升时间		t_{EXr}	-	-	5.0	ns	
EXTAL外部时钟下降时间		t_{EXf}	-	-	5.0	ns	
主时钟振荡器频率		f_{MAIN}	8	-	24	MHz	-
主时钟振荡稳定等待时间（晶振）*1		$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 2.9
LOCO时钟振荡频率		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO时钟振荡稳定等待时间		t_{LOCOWT}	-	-	60.4	µs	Figure 2.10
ILOCO时钟振荡频率		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	-
MOCO时钟振荡稳定等待时间		t_{MOCOWT}	-	-	15.0	µs	-
HOCO时钟振荡器振荡频率	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		−40≤Ta≤105°C副时钟频率精度为±50ppm。
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO时钟振荡稳定等待时间*2		t_{HOCOWT}	-	-	64.7	µs	-
FLL稳定等待时间		t_{FLLWT}	-	-	1.8	ms	-
锁相环时钟频率		f_{PLL}	120	-	240	MHz	-
PLL时钟振荡稳定等待时间		t_{PLLWT}	-	-	174.9	µs	Figure 2.11

Note 1. 设置主时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟振荡器。

Note 2. 这是从复位状态释放到HOCO振荡频率(fHOCO)达到保证工作范围的时间。

Table 2.14 副时钟振荡器的时钟时序

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
副时钟振荡稳定等待时间	$t_{SUBOSCWT}$	-	-	*1	s	Figure 2.12

Note 1. 设置副时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。更改SOSCCR.SOSTP位的设置以启动副时钟操作后，只有在副时钟振荡稳定时间过去并留有足够余量后才开始使用副时钟振荡器。建议使用显示值的两倍。

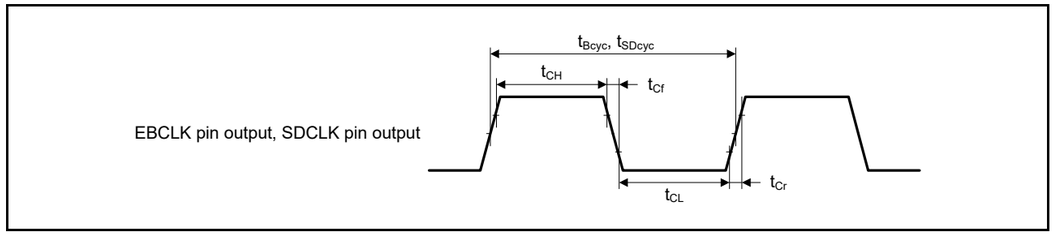


Figure 2.7 EBCLK and SDCLK output timing

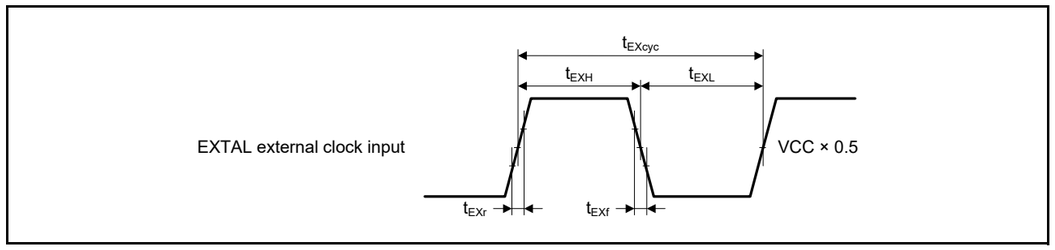


Figure 2.8 EXTAL external clock input timing

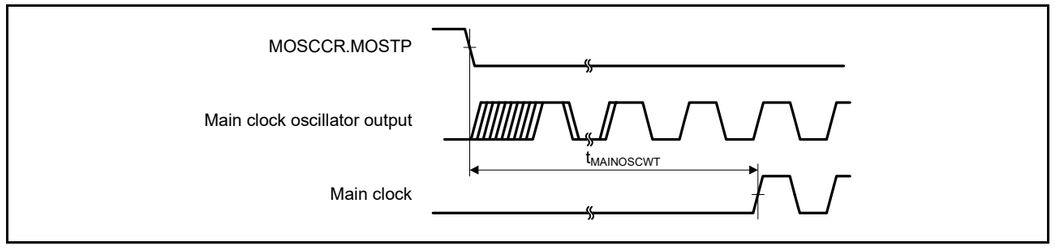


Figure 2.9 Main clock oscillation start timing

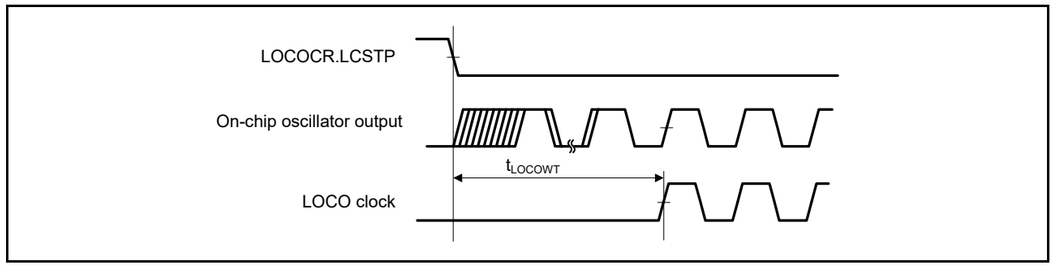


Figure 2.10 LOCO clock oscillation start timing

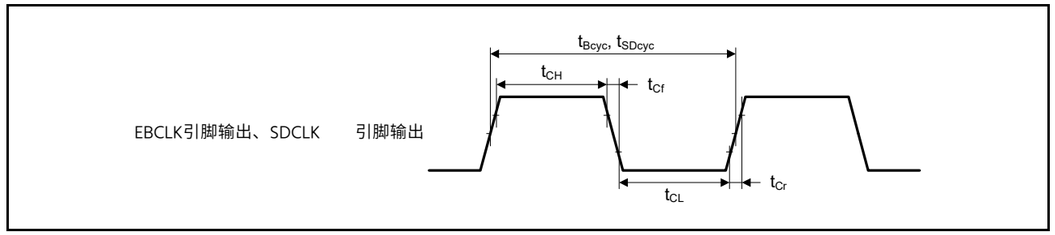


Figure 2.7 EBCLK和SDCLK 输出时序

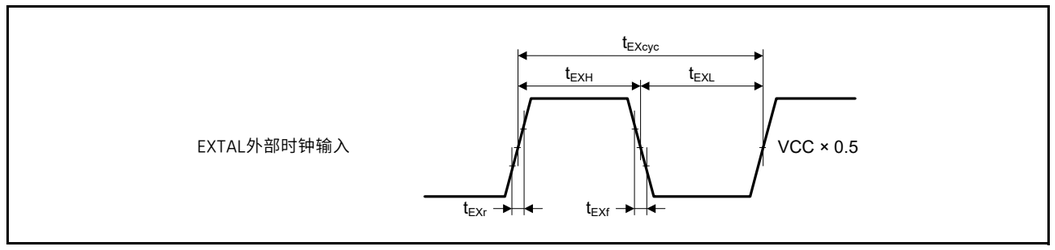


Figure 2.8 EXTAL外部时钟输入时序

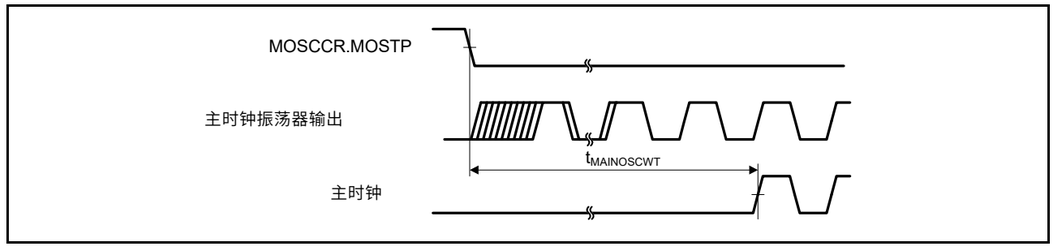


Figure 2.9 主时钟振荡开始时序

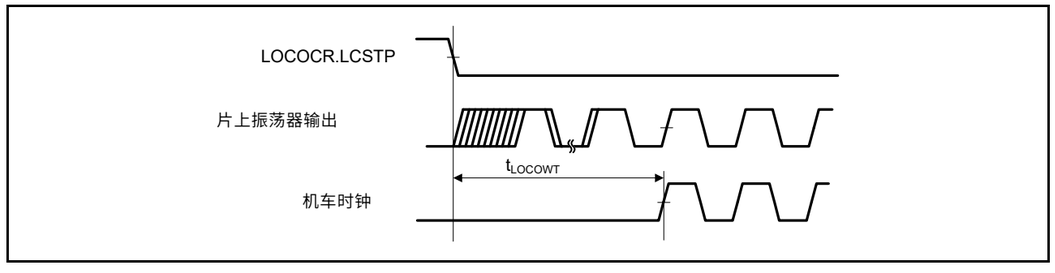


Figure 2.10 LOCO时钟振荡开始时序

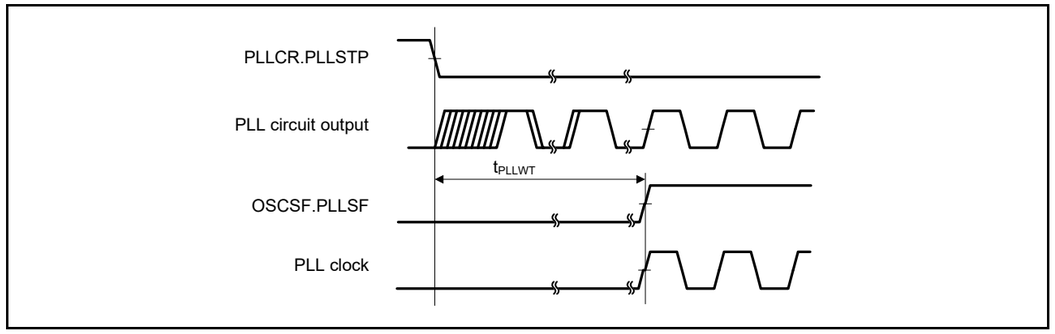


Figure 2.11 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

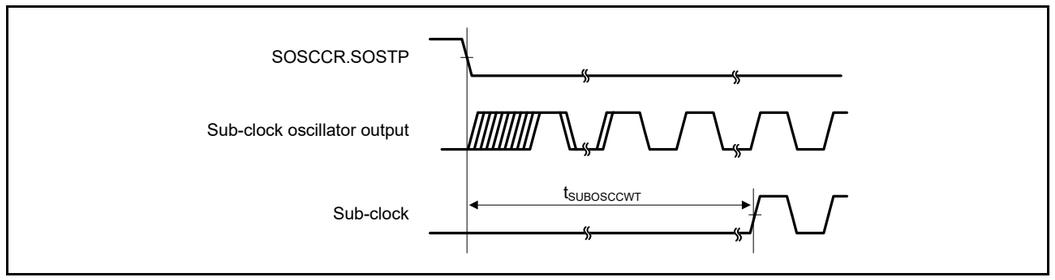


Figure 2.12 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.13
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 2.14
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	µs	
Wait time after RES cancellation		t_{RESWT}	-	29	33	µs	Figure 2.13
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		t_{RESW2}	-	320	408	µs	-

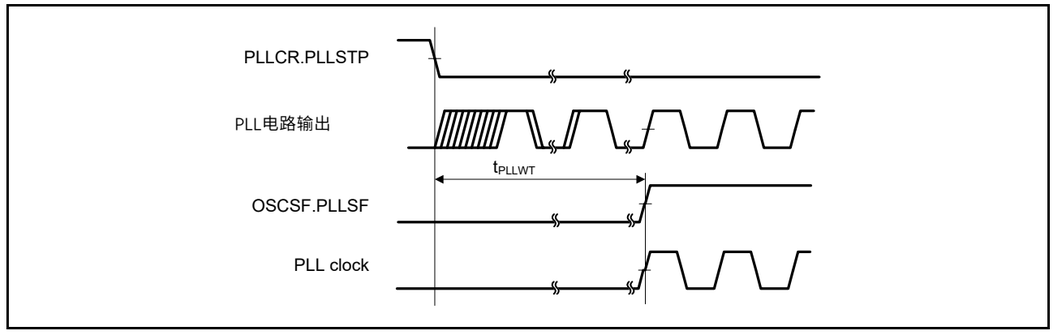


Figure 2.11 PLL时钟振荡开始时序

Note: 仅在主时钟振荡稳定后操作PLL。

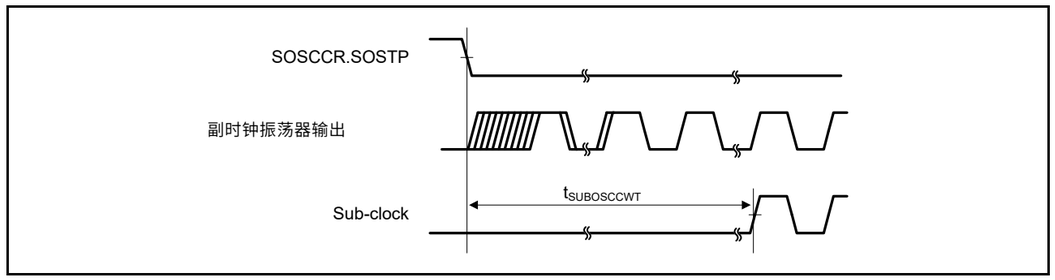


Figure 2.12 副时钟振荡开始时序

2.3.3 重置时间

Table 2.15 重置时间

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.13
	深度软件待机模式	t_{RESWD}	0.6	-	-	ms	Figure 2.14
	软件待机模式，Subosc速度模式	t_{RESWS}	0.3	-	-	ms	
	所有其他	t_{RESW}	200	-	-	µs	
RES取消后的等待时间		t_{RESWT}	-	29	33	µs	Figure 2.13
内部复位取消后的等待时间（IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、SRAMECC错误复位、总线主MPU错误复位、总线从MPU错误复位、堆栈指针错误复位）		t_{RESW2}	-	320	408	µs	-

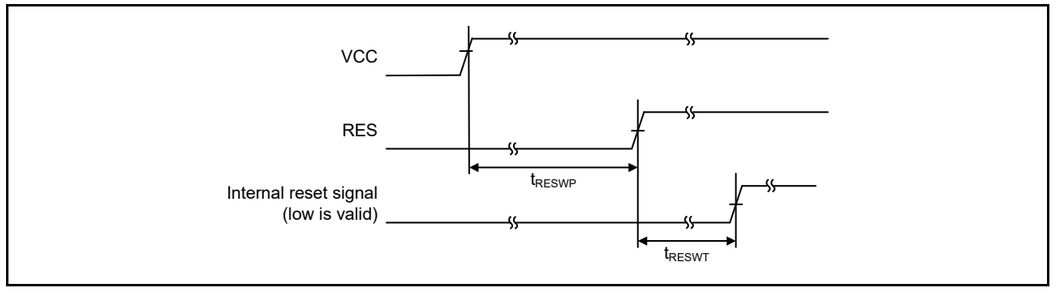


Figure 2.13 Power-on reset timing

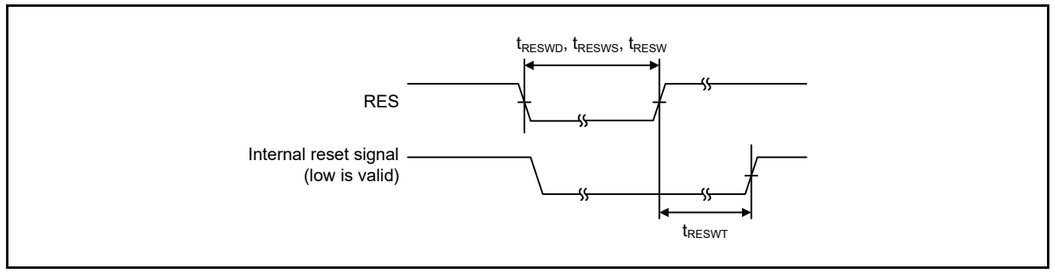


Figure 2.14 Reset input timing

2.3.4 Wakeup Timing

Table 2.16 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	Figure 2.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}	-	230*9	280*9	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}	-	570*9	700*9	µs	
	System clock source is sub-clock oscillator*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	System clock source is LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	System clock source is HOCO clock oscillator*6		t_{SBYHO}	-	240*9, *10	310 *9, *10	µs	
	System clock source is MOCO clock oscillator*7		t_{SBYMO}	-	220*9	300*9	µs	
Recovery time from Deep Software Standby mode			t_{DSBY}	-	0.65	1.0	ms	Figure 2.16
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	34	-	35	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	-	35*9, *10	71 *9, *10	µs	Figure 2.17
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	-	11*9	14*9	µs	

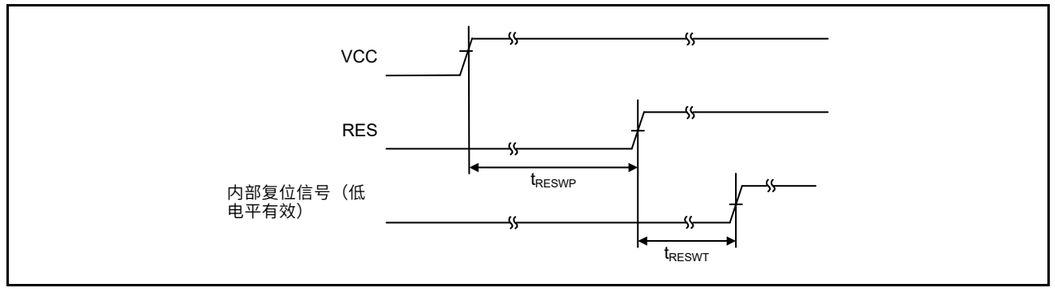


Figure 2.13 上电复位时序

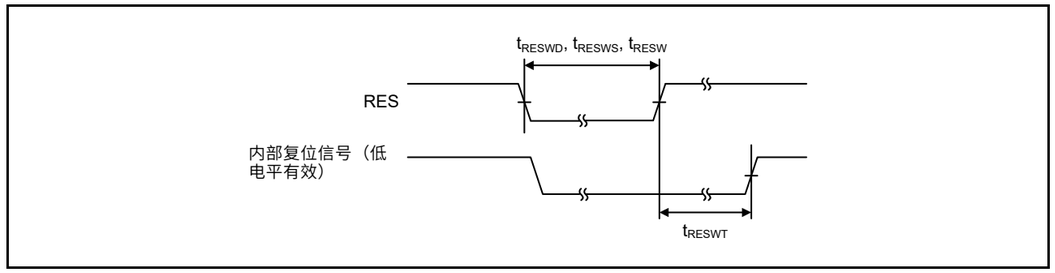


Figure 2.14 复位输入时序

2.3.4 唤醒时间

Table 2.16 从低功耗模式恢复的时间

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	图2.15所有振荡器的分频比为1。
		系统时钟源是带有主时钟振荡器的PLL*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器*4	t_{SBYEX}	-	230*9	280*9	µs	
		系统时钟源是带有主时钟振荡器*5的PLL	t_{SBYPE}	-	570*9	700*9	µs	
	系统时钟源为副时钟振荡器*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	系统时钟源为LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	系统时钟源为HOCO时钟振荡器*6		t_{SBYHO}	-	240*9, *10	310 *9, *10	µs	
	系统时钟源为MOCO时钟振荡器*7		t_{SBYMO}	-	220*9	300*9	µs	
从深度软件待机模式恢复时间			t_{DSBY}	-	0.65	1.0	ms	Figure 2.16
取消深度软件待机模式后的等待时间			t_{DSBYWT}	34	-	35	t_{cyc}	
从软件待机模式恢复到	系统时钟源为HOCO(20MHz)时的高速模式		t_{SNZ}	-	35*9, *10	71 *9, *10	µs	Figure 2.17
贪睡模式	系统时钟源为MOCO(8MHz)时的高速模式		t_{SNZ}	-	11*9	14*9	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 01h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 01h))

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 01h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 01h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 µs (typical), 34 µs (maximum)
STCONR.STCON[1:0] = 11b:16 µs (typical), 104 µs (maximum).

Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 µs (typical) or 18 µs (maximum) is added as the HOCO wait time.

Note 1. 恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=振荡器作为系统时钟源的恢复时间+任何需要比系统时钟源更长稳定时间的振荡器的最长振荡稳定时间+2个LOCO周期（当LOCO运行时）+3个SOSC周期（当Subosc正在振荡且MSTPC0=0（CAC模块停止）时）。

Note 2. 当晶振频率为24MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为05h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=05h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=05h))

Note 3. 当PLL的频率为240MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为05h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=05h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=05h))

Note 4. 当外部时钟频率为24MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为01h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=01h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=01h))

Note 5. 当PLL的频率为240MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为01h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=01h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=01h))

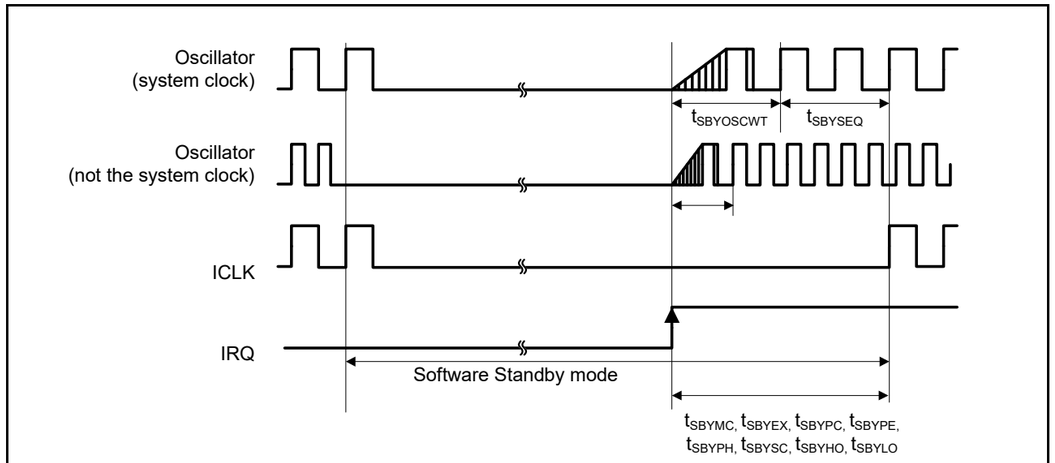
Note 6. HOCO频率为20MHz。

Note 7. MOCO频率为8MHz。

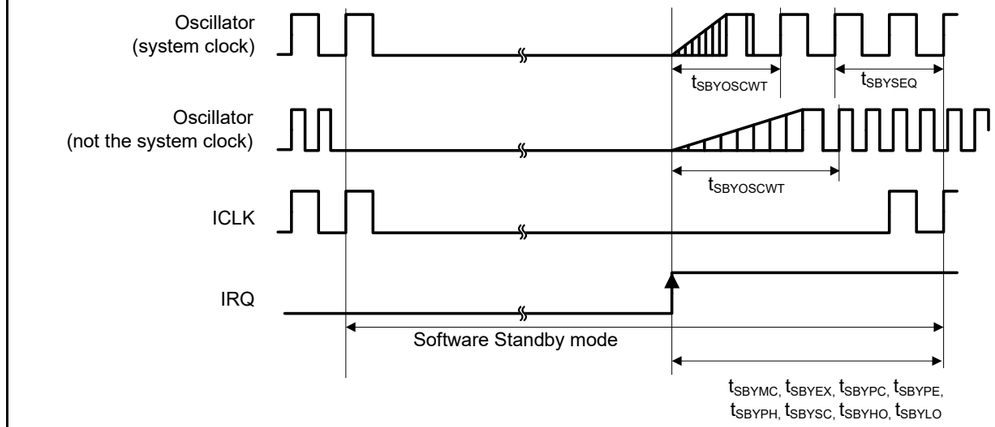
Note 8. 在Subosc速度模式下，副时钟振荡器或LOCO在软件待机模式下继续振荡。

Note 9. 当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：
STCONR.STCON[1:0] = 00b:16 µs (typical), 34 µs (maximum)
STCONR.STCON[1:0] = 11b:16 µs (typical), 104 µs (maximum).

注10.当SNZCR.RXDREQEN位设置为0时，添加16µs（典型值）或18µs（最大值）作为HOCO等待时间。

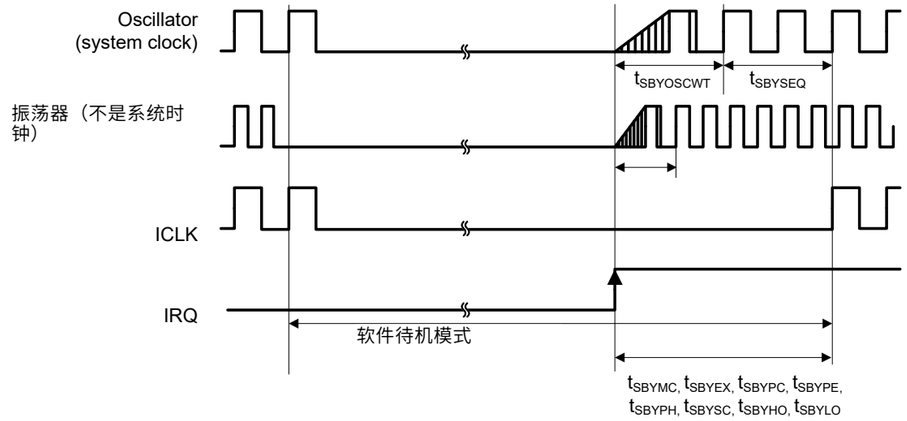


When stabilization of the system clock oscillator is slower

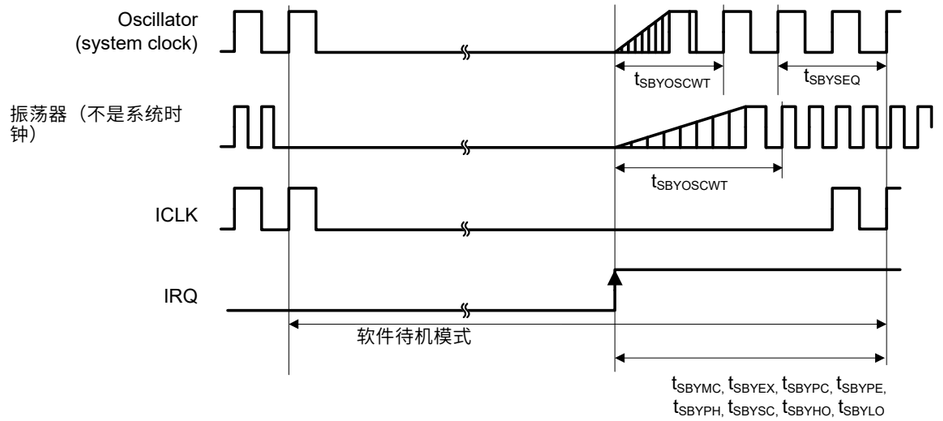


When stabilization of an oscillator other than the system clock is slower

Figure 2.15 Software Standby mode cancellation timing



当系统时钟振荡器的稳定速度较慢时



当系统时钟以外的振荡器稳定较慢时

Figure 2.15 软件待机模式取消时序

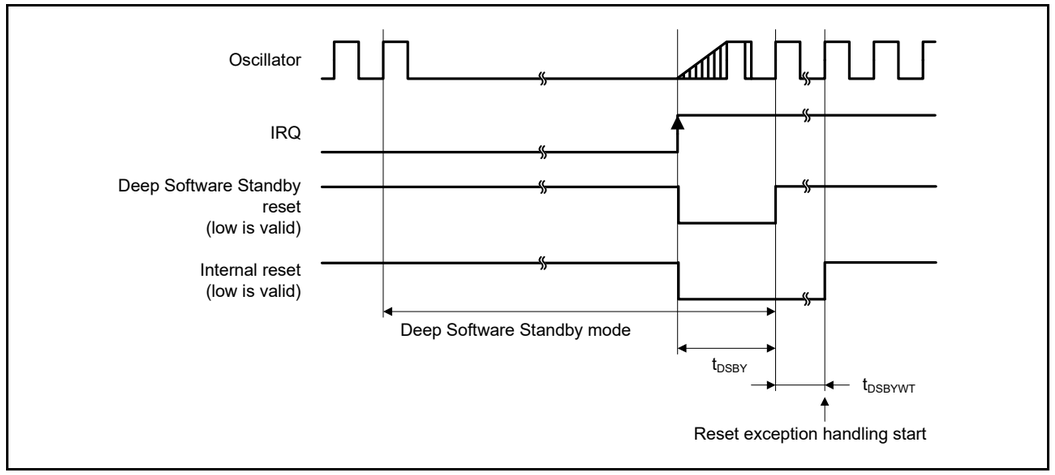
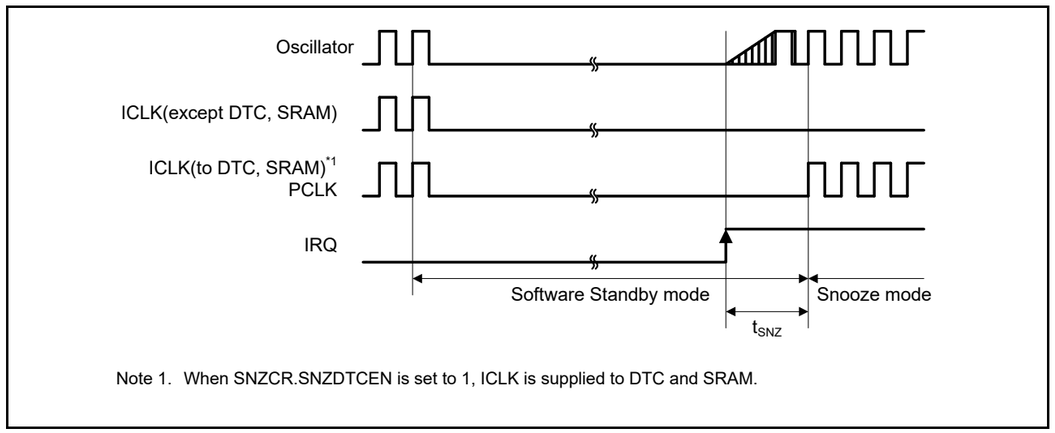


Figure 2.16 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.17 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.

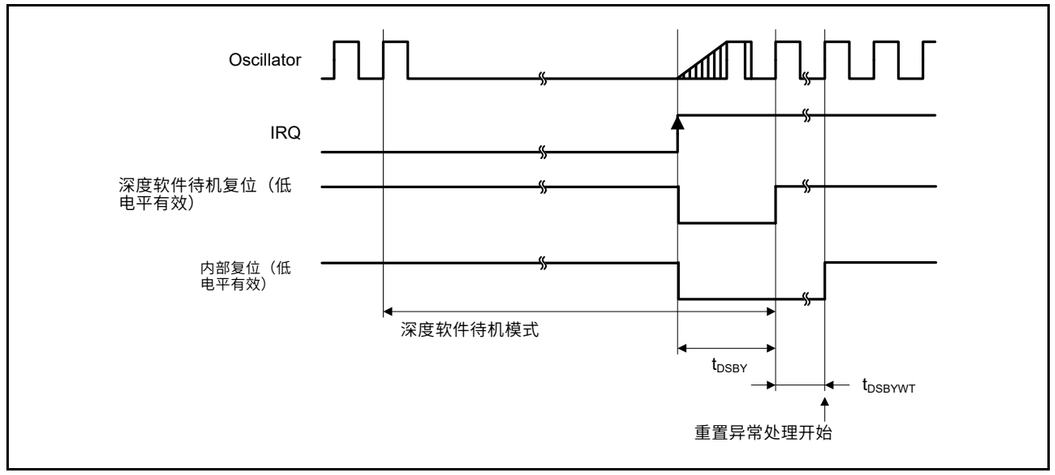
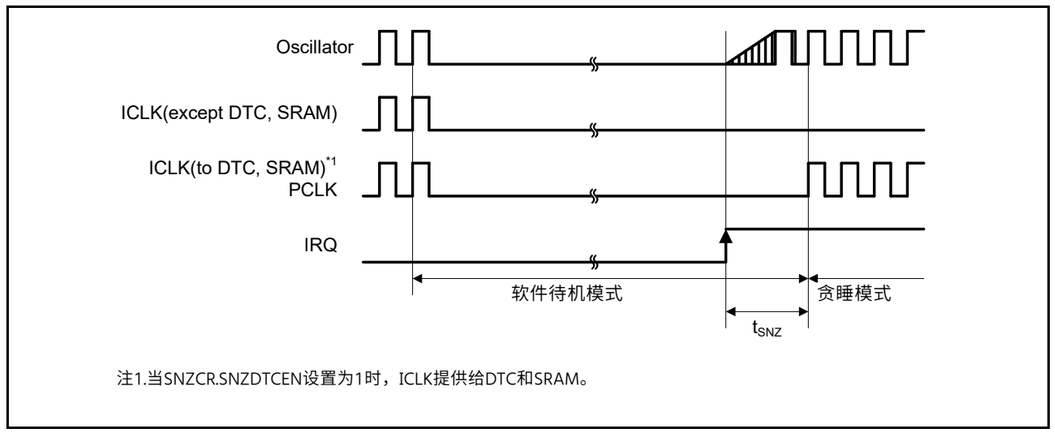


Figure 2.16 深度软件待机模式取消时序



注1.当SNZCR.SNZDTCEN设置为1时，ICLK提供给DTC和SRAM。

Figure 2.17 从软件待机模式到贪睡模式的恢复时间

2.3.5 NMI和IRQ噪声滤波器

Table 2.17 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	-	-	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	-	-	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。
Note: 如果时钟源切换，则增加切换源的4个时钟周期。

Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

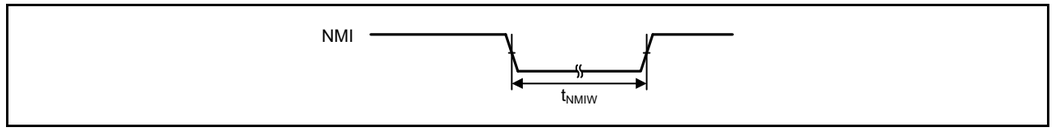


Figure 2.18 NMI interrupt input timing

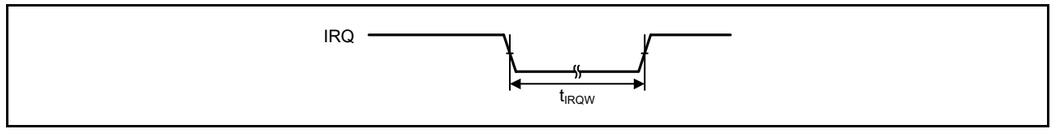


Figure 2.19 IRQ interrupt input timing

2.3.6 Bus Timing

Table 2.18 Bus timing (1 of 2)
Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	12.5	ns	Figure 2.20 to Figure 2.25
Byte control delay	t_{BCD}	-	12.5	ns	
CS delay	t_{CSD}	-	12.5	ns	
ALE delay time	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
Read data setup time	t_{RDS}	12.5	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR/WRn delay	t_{WRD}	-	12.5	ns	
Write data delay	t_{WDD}	-	12.5	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	12.5	-	ns	Figure 2.26
WAIT hold time	t_{WTH}	0	-	ns	

Note 1. tPcyc表示PCLKB周期。
Note 2. tNMICK表示NMI数字滤波器采样时钟的周期。
Note 3. tIRQCK表示IRQi数字滤波器采样时钟的周期。

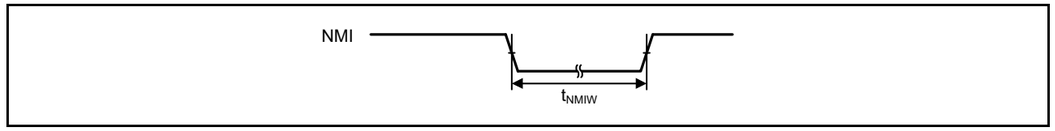


Figure 2.18 NMI中断输入时序

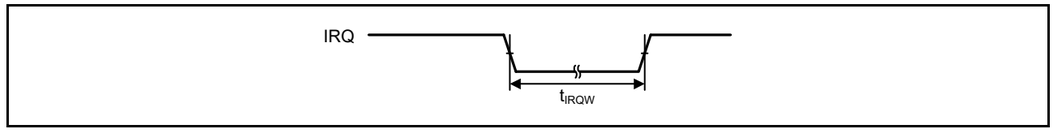


Figure 2.19 IRQ中断输入时序

2.3.6 巴士时间

Table 2.18 巴士计时（1of2）
条件1：使用CS区域控制器(CSC)时。
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF
EBCLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。其他：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

条件2：使用SDRAM区域控制器(SDRAMC)时。
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

条件3：同时使用SDRAM区域控制器(SDRAMC)和CS区域控制器(CSC)时。
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Max	Unit	测试条件
地址延迟	t_{AD}	-	12.5	ns	图2.20至 Figure 2.25
字节控制延迟	t_{BCD}	-	12.5	ns	
CS delay	t_{CSD}	-	12.5	ns	
ALE延迟时间	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
读取数据建立时间	t_{RDS}	12.5	-	ns	
读取数据保持时间	t_{RDH}	0	-	ns	
WR/WRn delay	t_{WRD}	-	12.5	ns	
写数据延迟	t_{WDD}	-	12.5	ns	
写数据保持时间	t_{WDH}	0	-	ns	
等待设置时间	t_{WTS}	12.5	-	ns	Figure 2.26
WAIT保持时间	t_{WTH}	0	-	ns	

Table 2.18 Bus timing (2 of 2)

Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	t_{AD2}	0.8	6.8	ns	Figure 2.27 to Figure 2.33
CS delay 2 (SDRAM)	t_{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t_{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t_{CKED}	0.8	6.8	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	2.9	-	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	1.5	-	ns	
Write data delay 2 (SDRAM)	t_{WDD2}	-	6.8	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	-	ns	
WE delay (SDRAM)	t_{WED}	0.8	6.8	ns	
RAS delay (SDRAM)	t_{RASD}	0.8	6.8	ns	
CAS delay (SDRAM)	t_{CASD}	0.8	6.8	ns	

Table 2.18 巴士计时（2之2）

条件1：使用CS区域控制器(CSC)时。
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF
EBCLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。其他：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

条件2：使用SDRAM区域控制器(SDRAMC)时。
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

条件3：同时使用SDRAM区域控制器(SDRAMC)和CS区域控制器(CSC)时。
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Max	Unit	测试条件
地址延迟2(SDRAM)	t_{AD2}	0.8	6.8	ns	图2.27至 Figure 2.33
CS delay 2 (SDRAM)	t_{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t_{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t_{CKED}	0.8	6.8	ns	
读取数据建立时间2(SDRAM)	t_{RDS2}	2.9	-	ns	
读取数据保持时间2(SDRAM)	t_{RDH2}	1.5	-	ns	
写入数据延迟2(SDRAM)	t_{WDD2}	-	6.8	ns	
写数据保持时间2(SDRAM)	t_{WDH2}	0.8	-	ns	
WE延迟(SDRAM)	t_{WED}	0.8	6.8	ns	
RAS延迟(SDRAM)	t_{RASD}	0.8	6.8	ns	
CAS延迟(SDRAM)	t_{CASD}	0.8	6.8	ns	

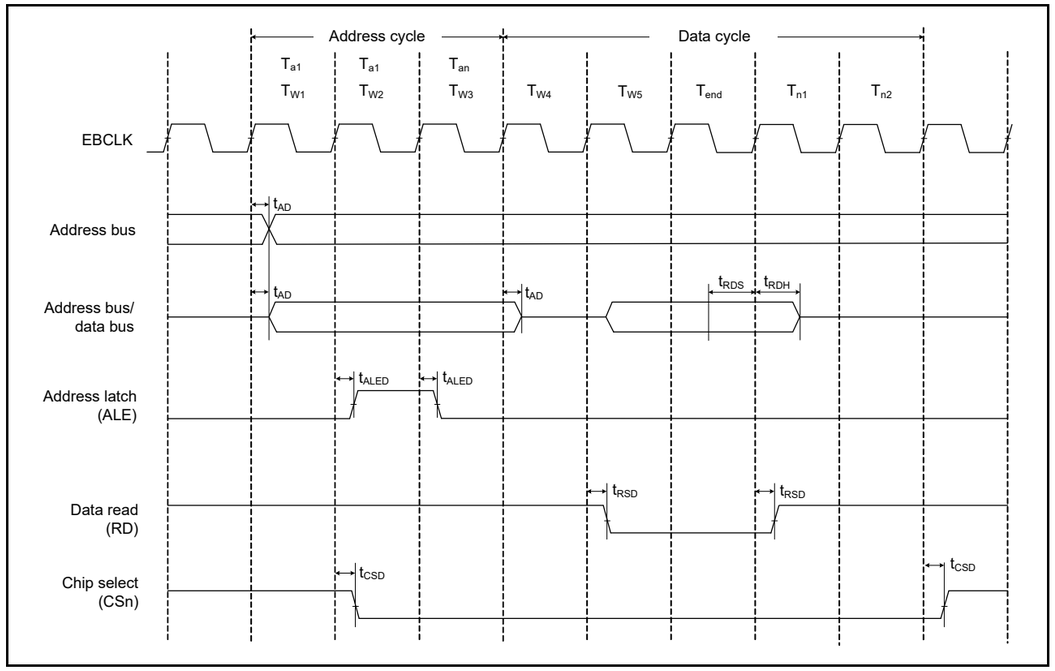


Figure 2.20 Address/data multiplexed bus read access timing

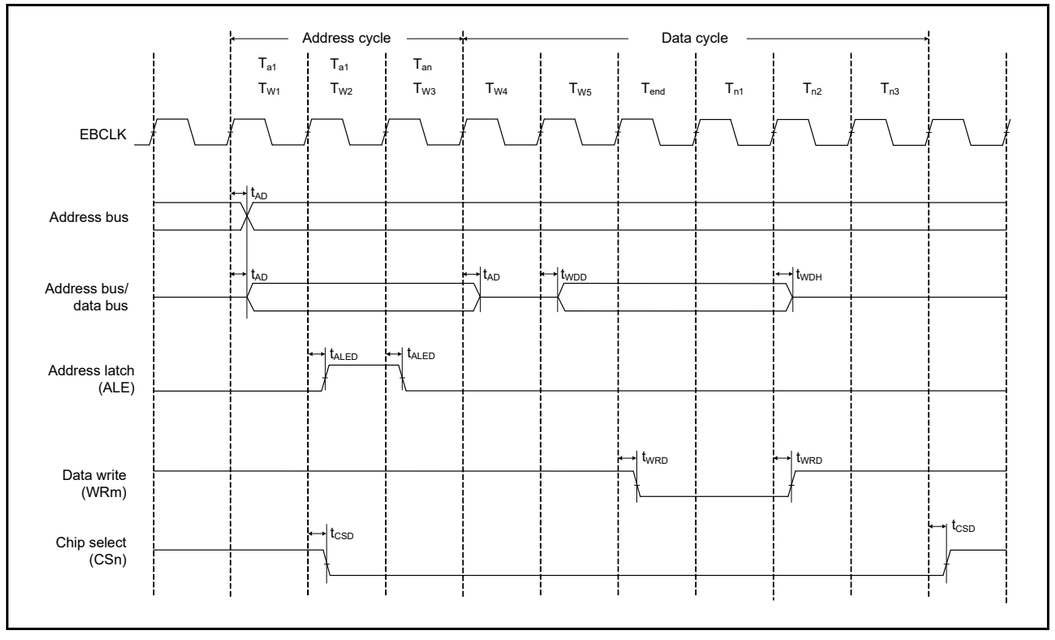


Figure 2.21 Address/data multiplexed bus write access timing

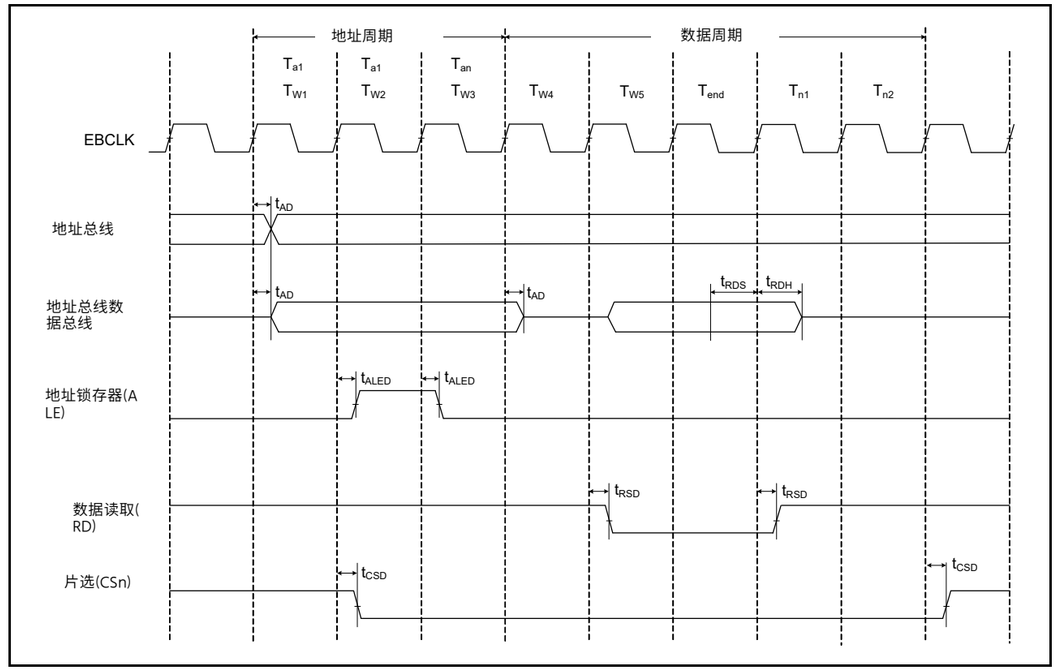


Figure 2.20 地址数据复用总线读访问时序

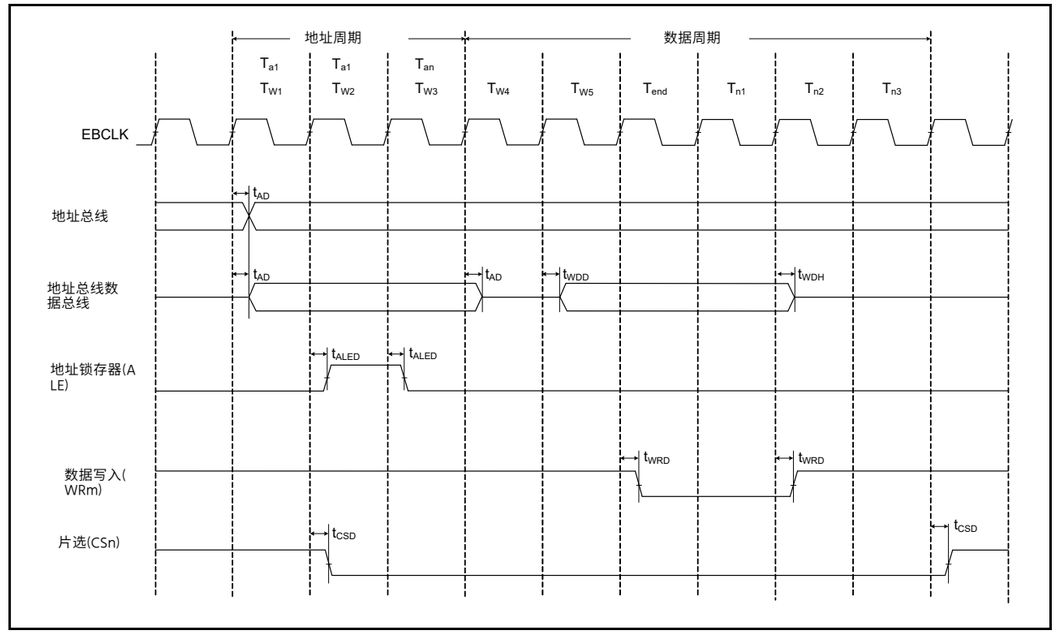


Figure 2.21 地址数据复用总线写访问时序

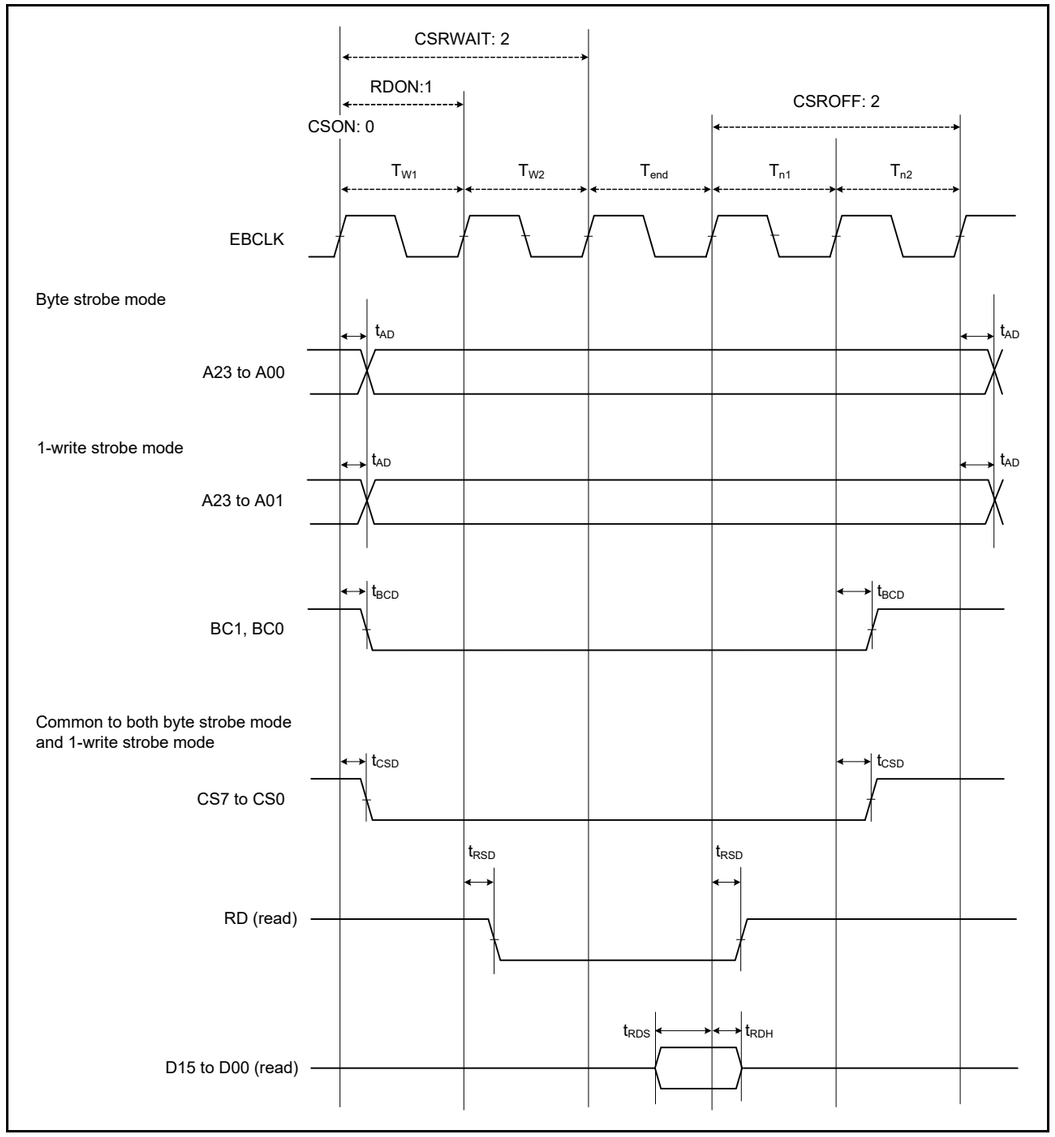


Figure 2.22 External bus timing for normal read cycle with bus clock synchronized

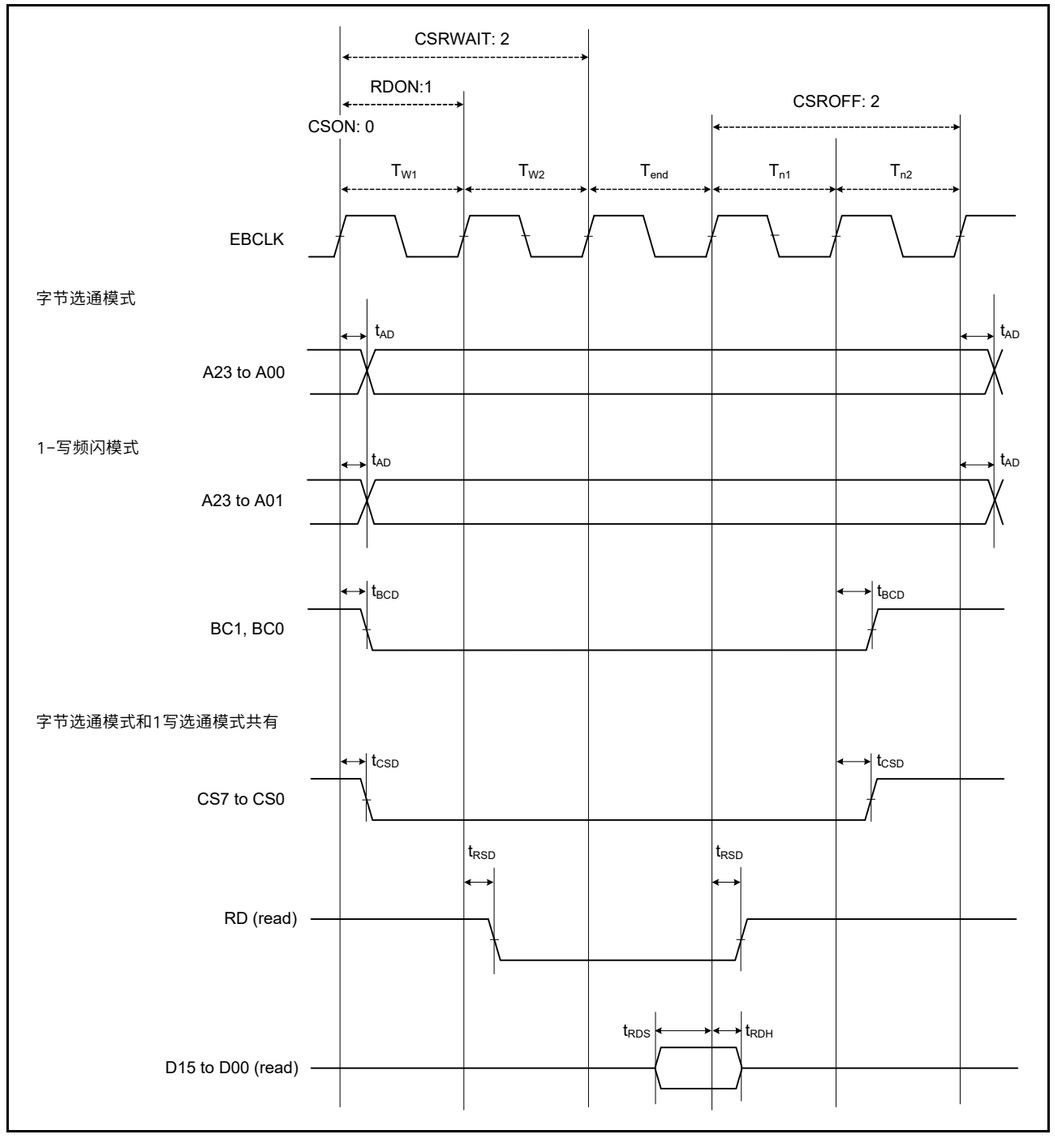
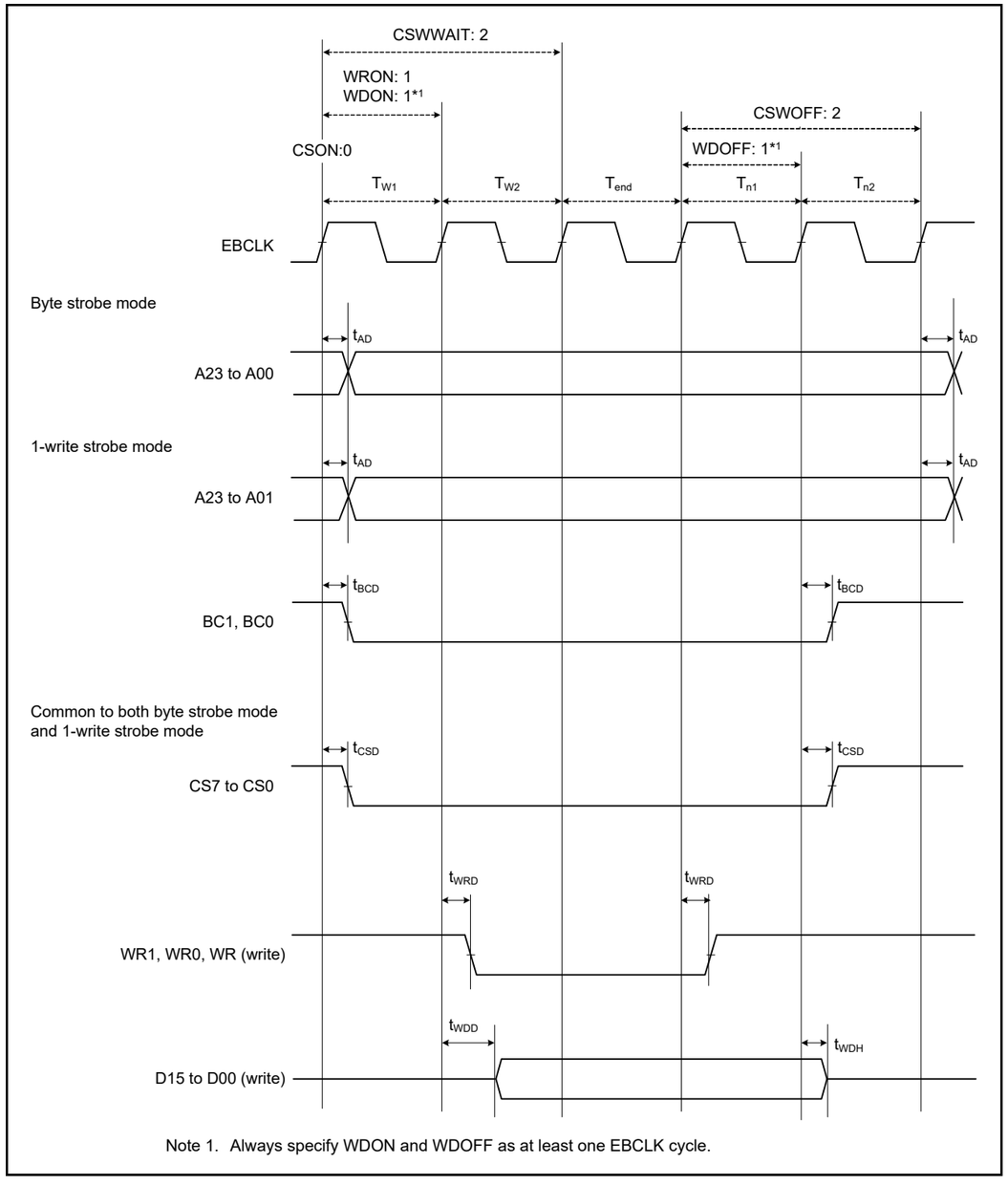
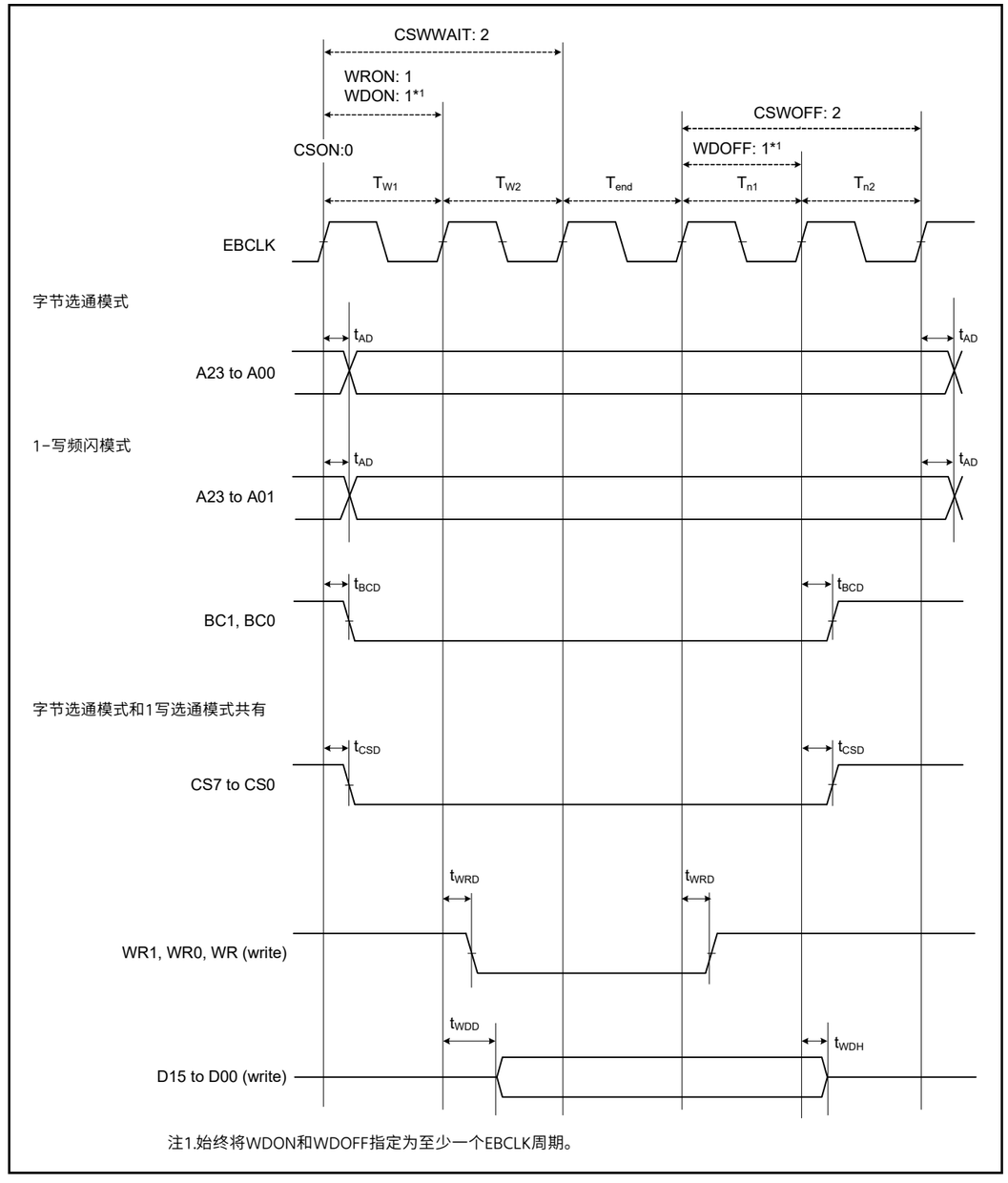


Figure 2.22 正常读取周期的外部总线时序与总线时钟同步



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.23 External bus timing for normal write cycle with bus clock synchronized



注1.始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 2.23 与总线时钟同步的正常写周期的外部总线时序

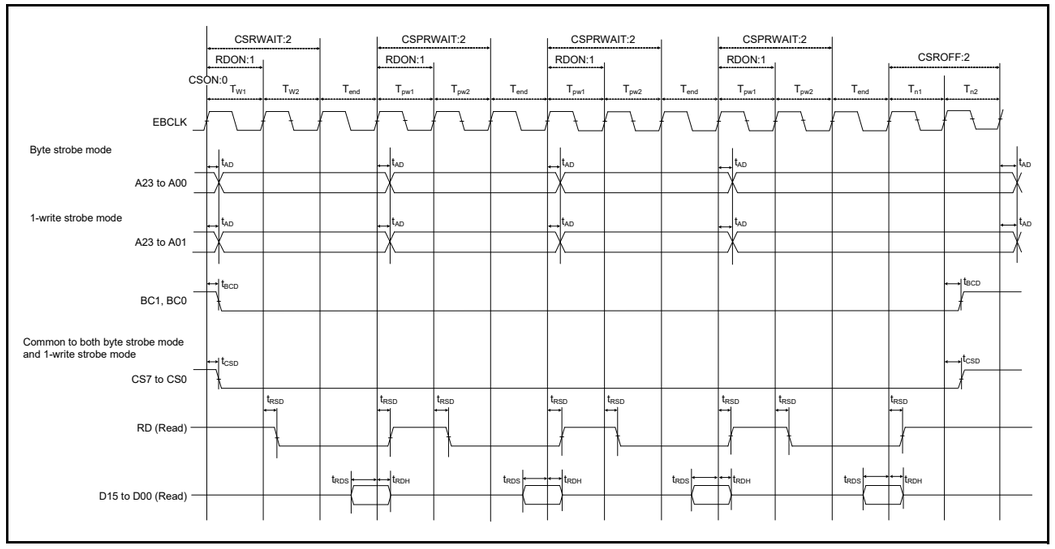
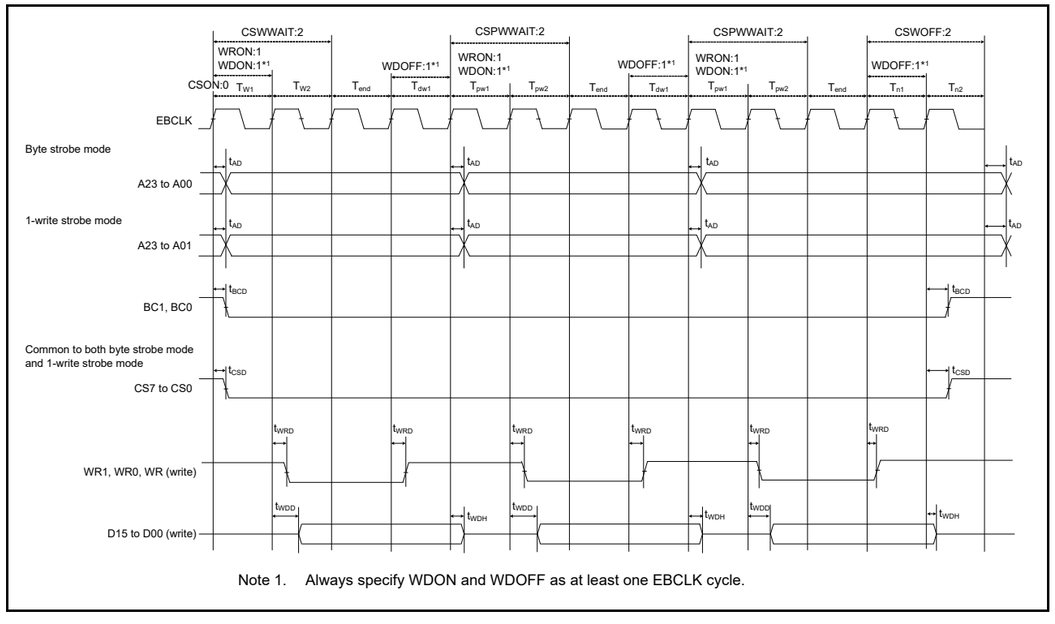


Figure 2.24 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.25 External bus timing for page write cycle with bus clock synchronized

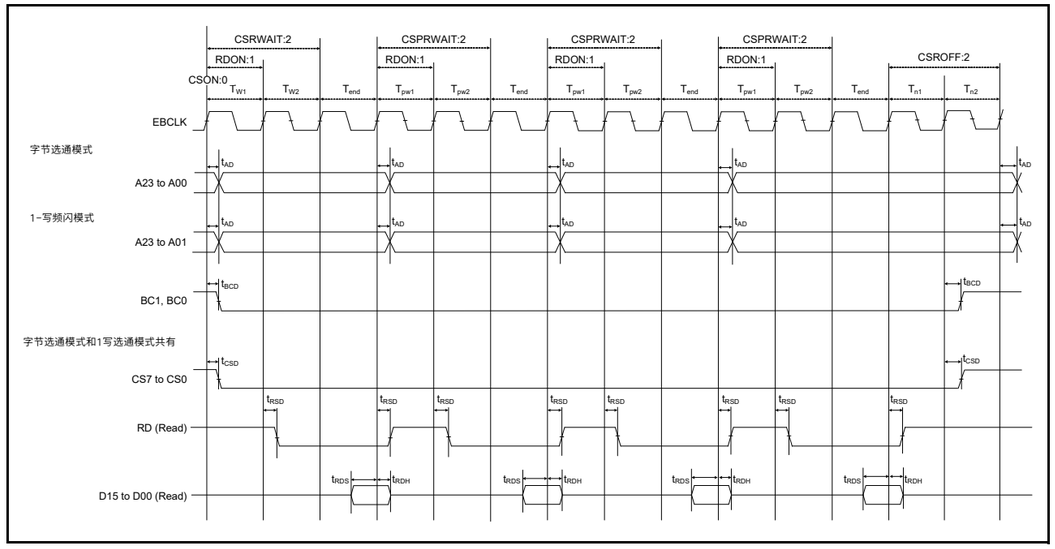
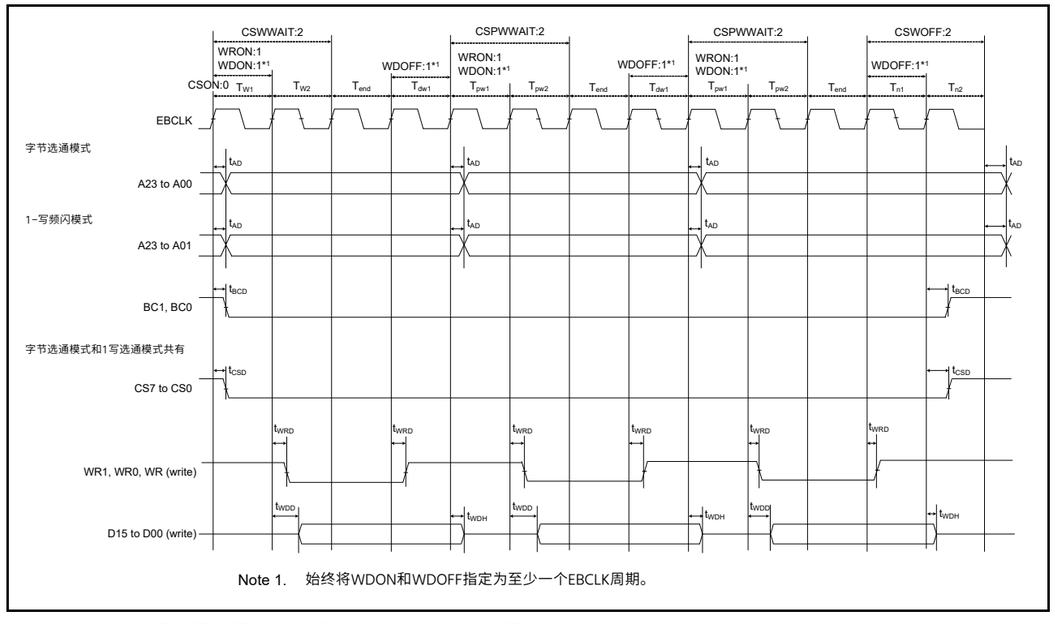


Figure 2.24 页面读取周期的外部总线时序与总线时钟同步



Note 1. 始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 2.25 页面写入周期的外部总线时序与总线时钟同步

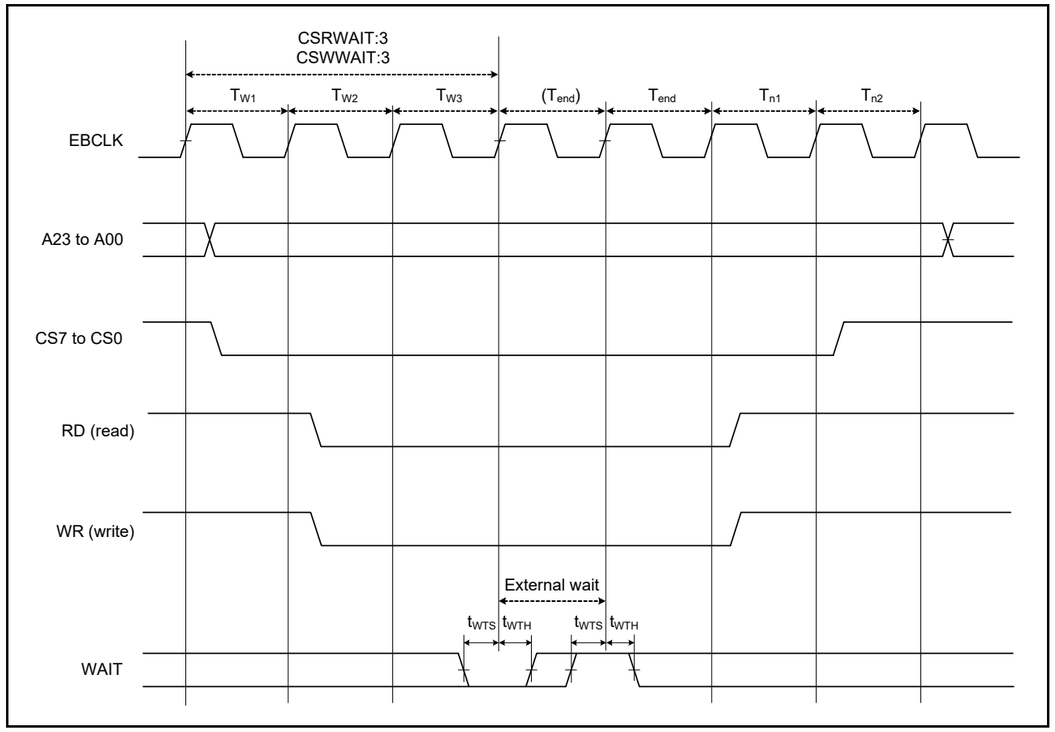


Figure 2.26 External bus timing for external wait control

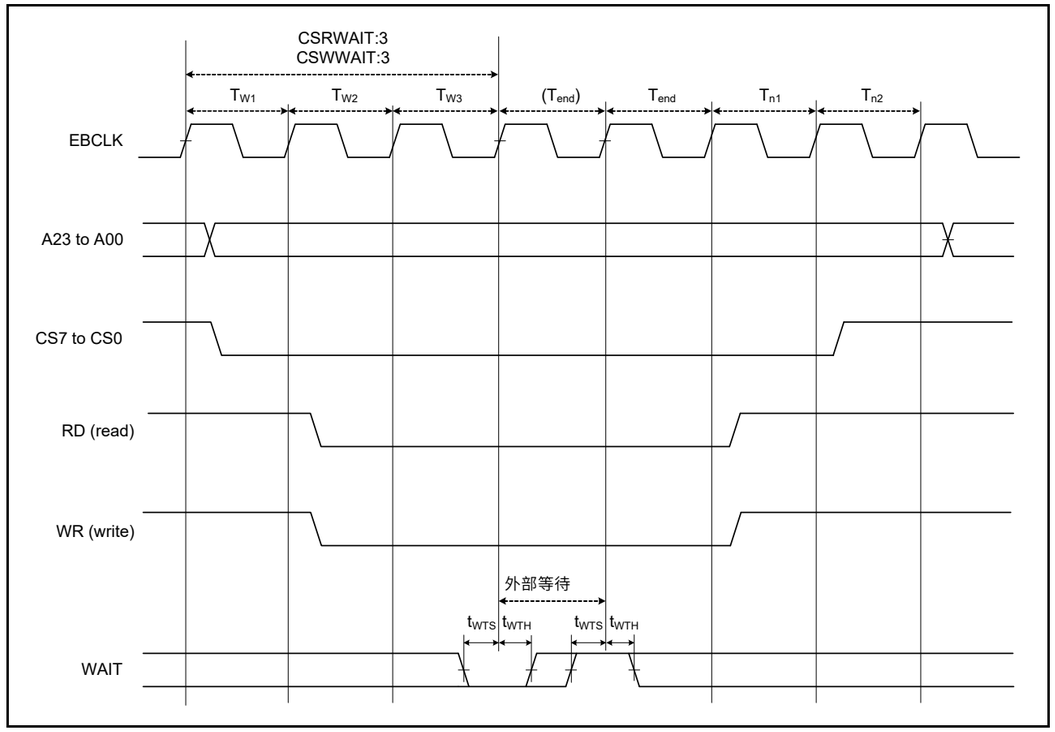
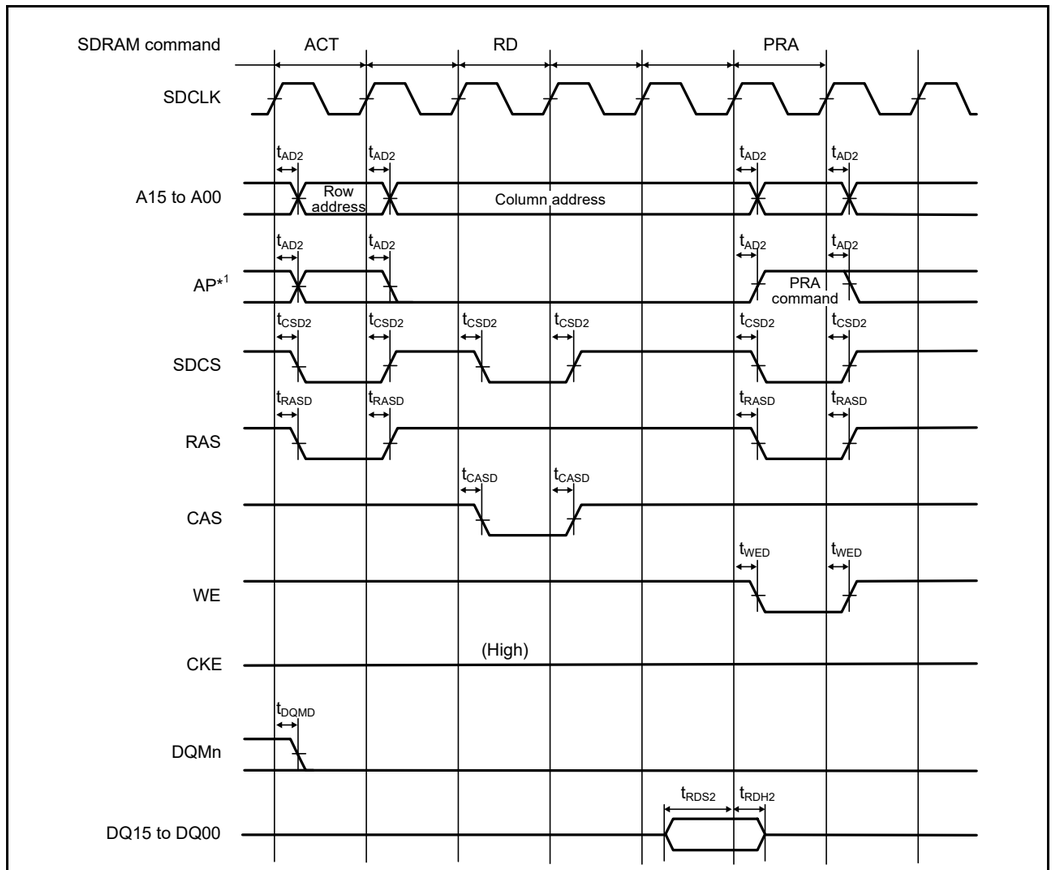
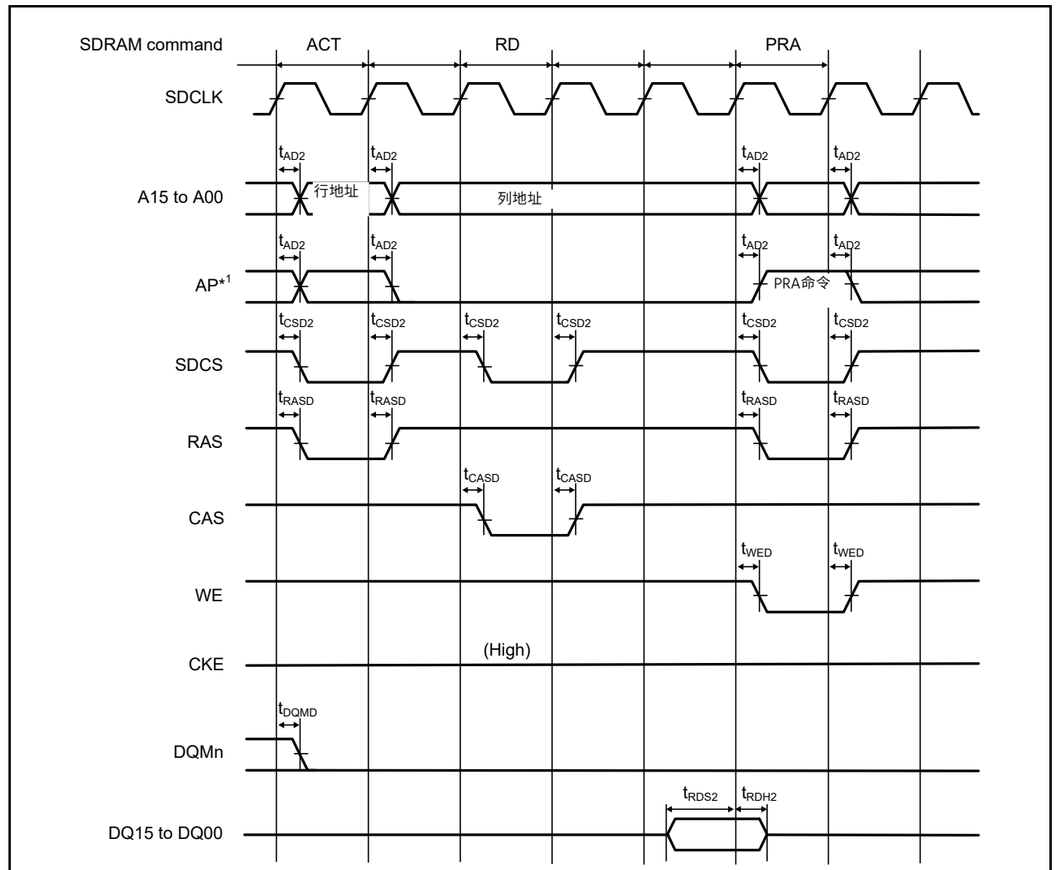


Figure 2.26 外部等待控制的外部总线时序



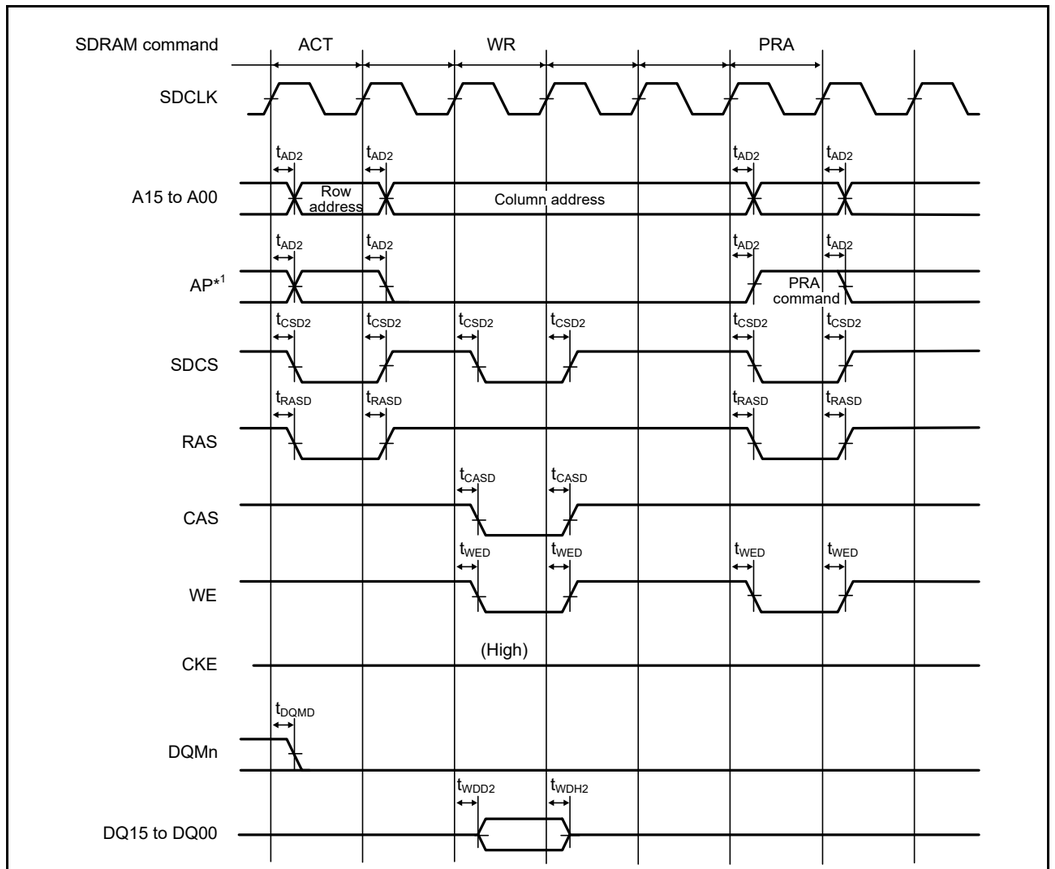
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.27 SDRAM single read timing



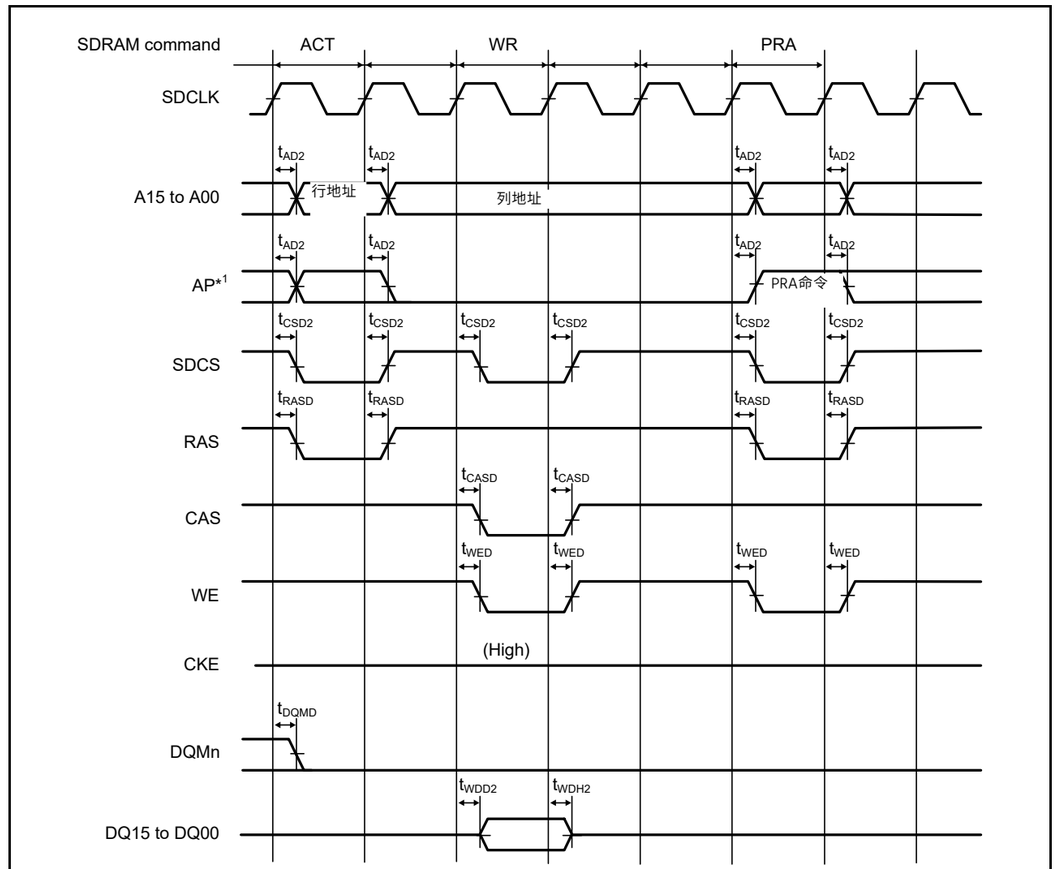
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.27 SDRAM单次读取时序



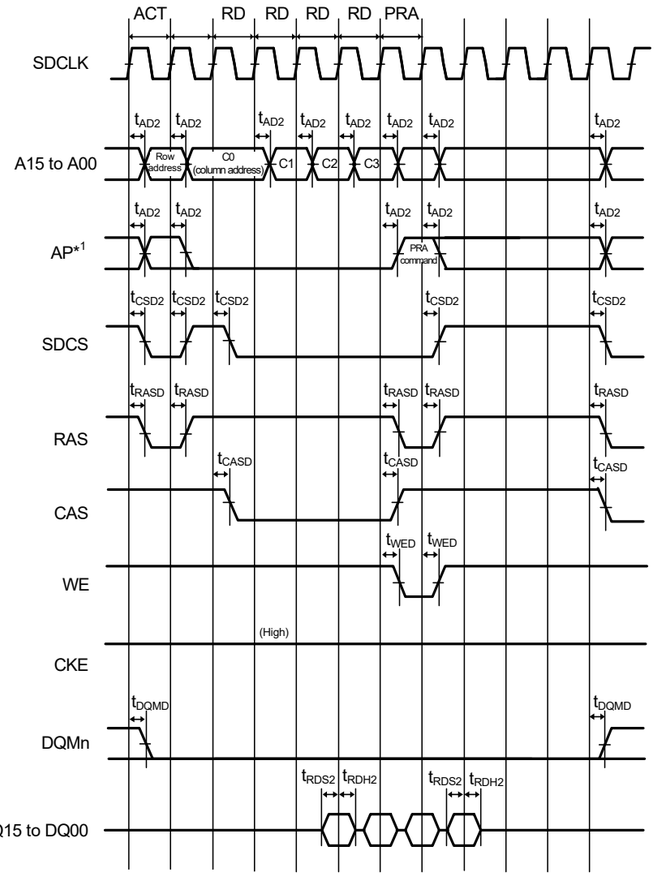
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.28 SDRAM single write timing



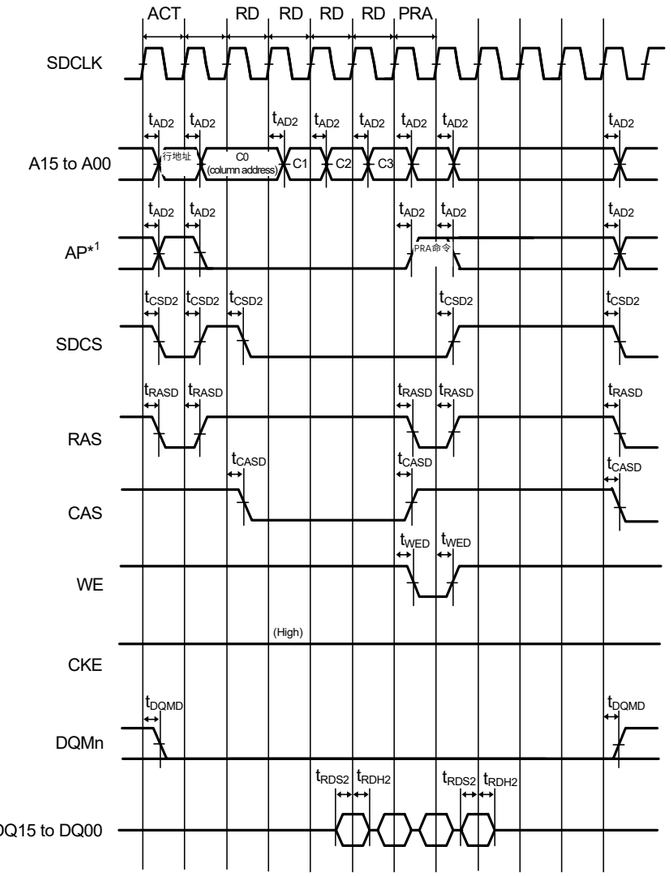
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.28 SDRAM单次写入时序



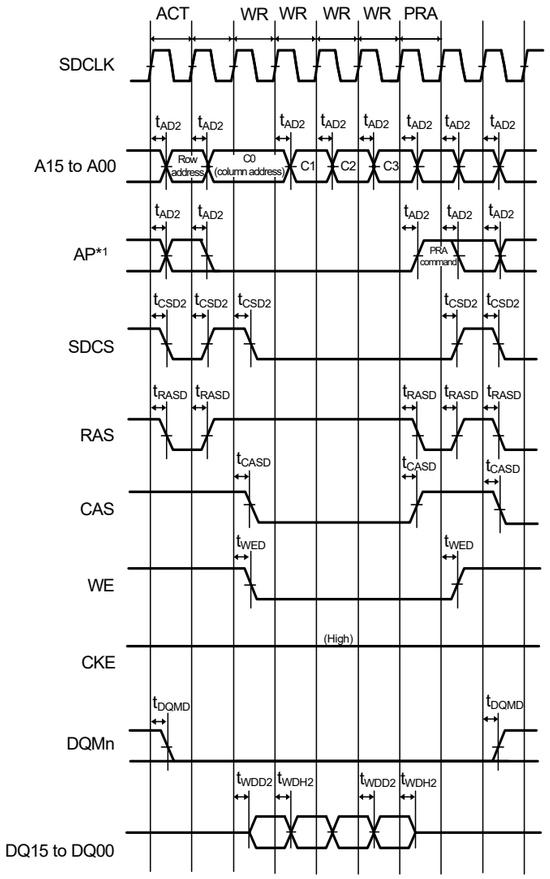
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.29 SDRAM multiple read timing



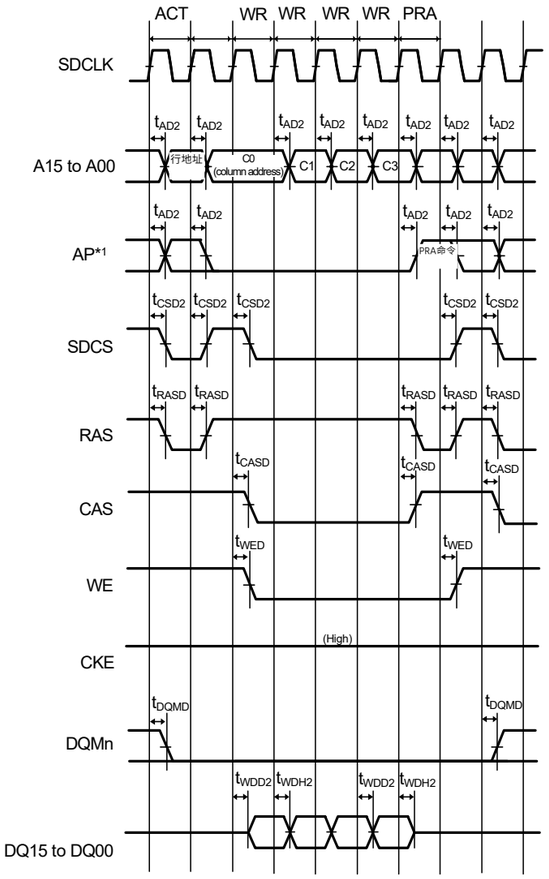
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.29 SDRAM多读时序



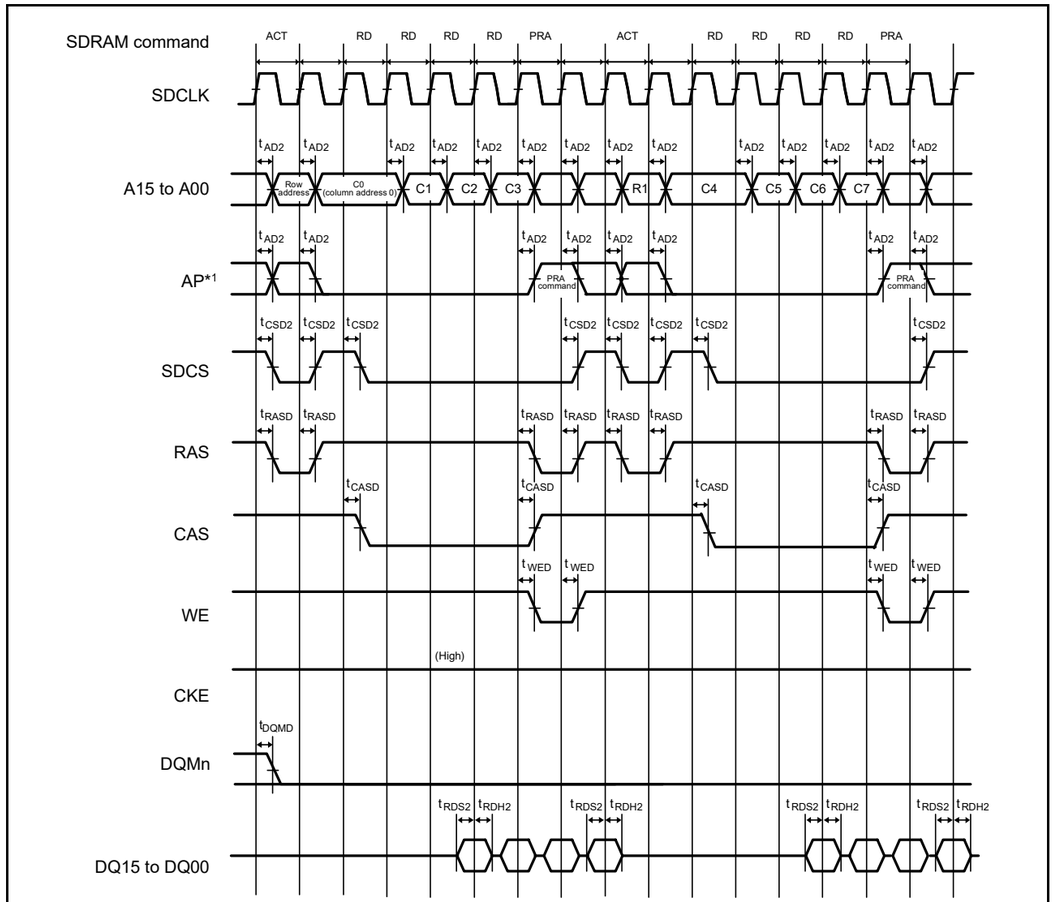
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.30 SDRAM multiple write timing



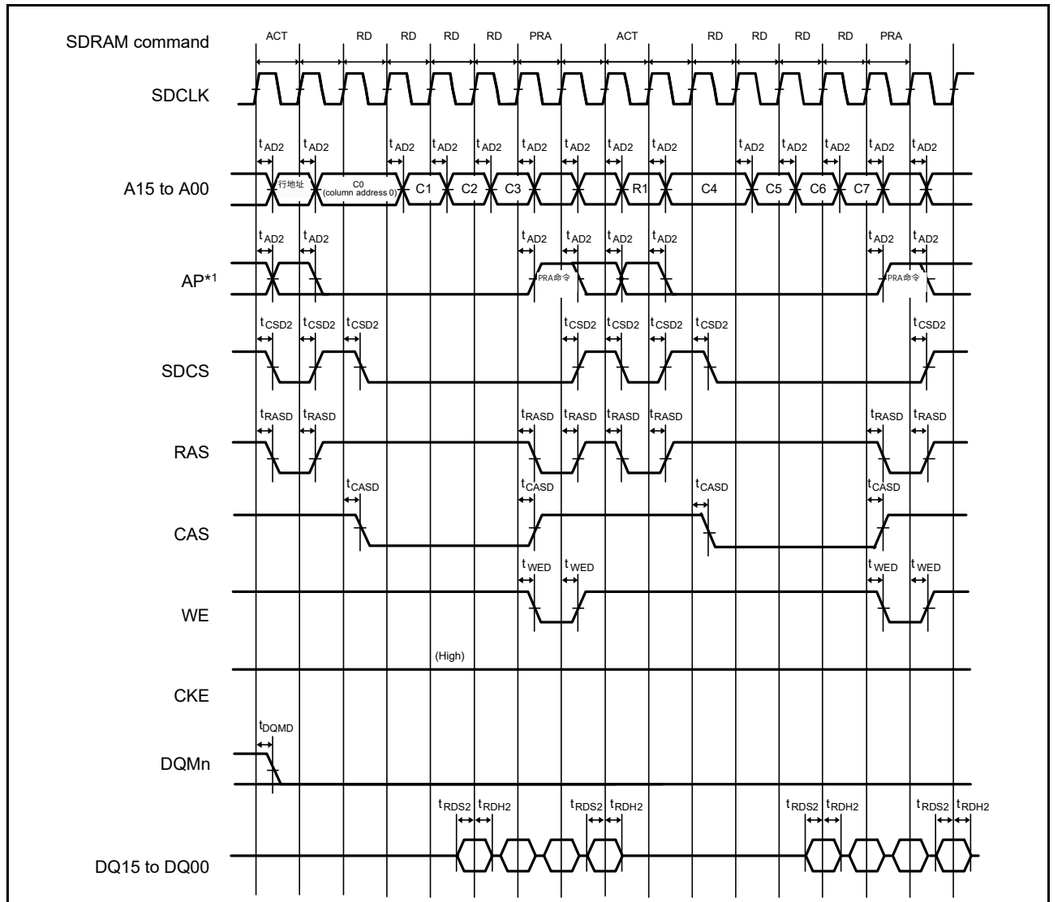
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.30 SDRAM多次写入时序



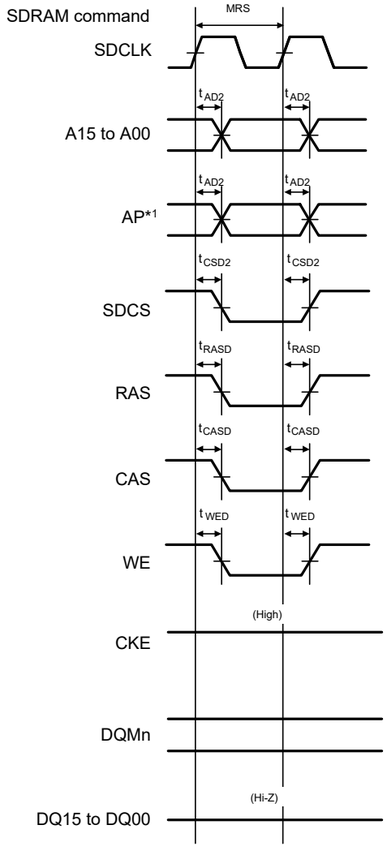
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.31 SDRAM multiple read line stride timing



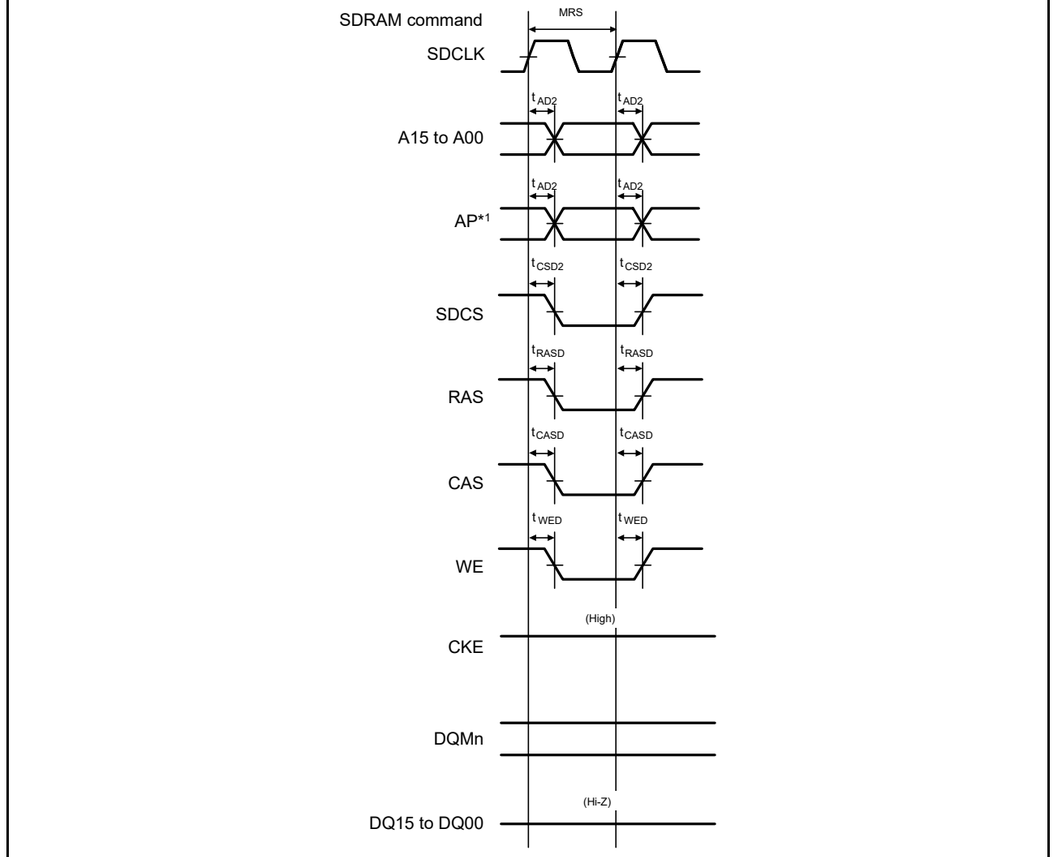
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.31 SDRAM多条读取线步幅时序



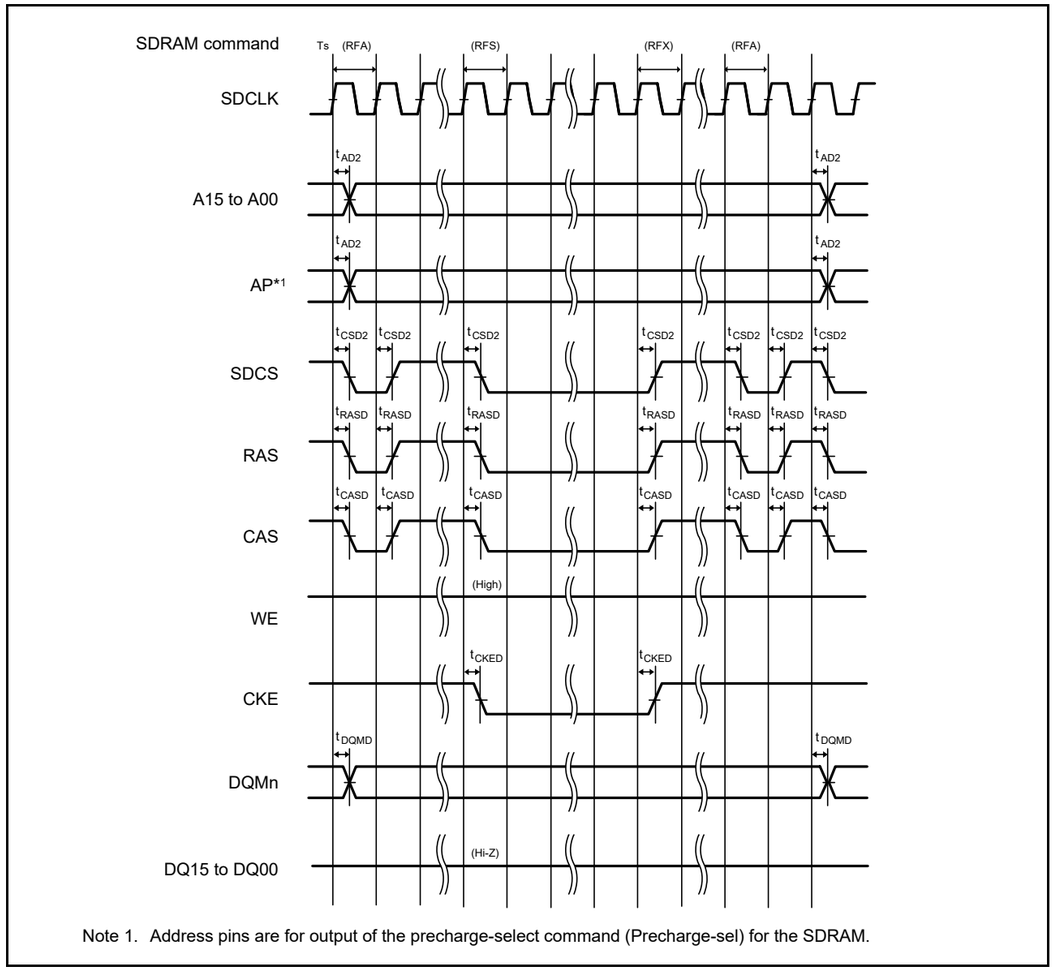
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.32 SDRAM mode register set timing



注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.32 SDRAM模式寄存器设置时序



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

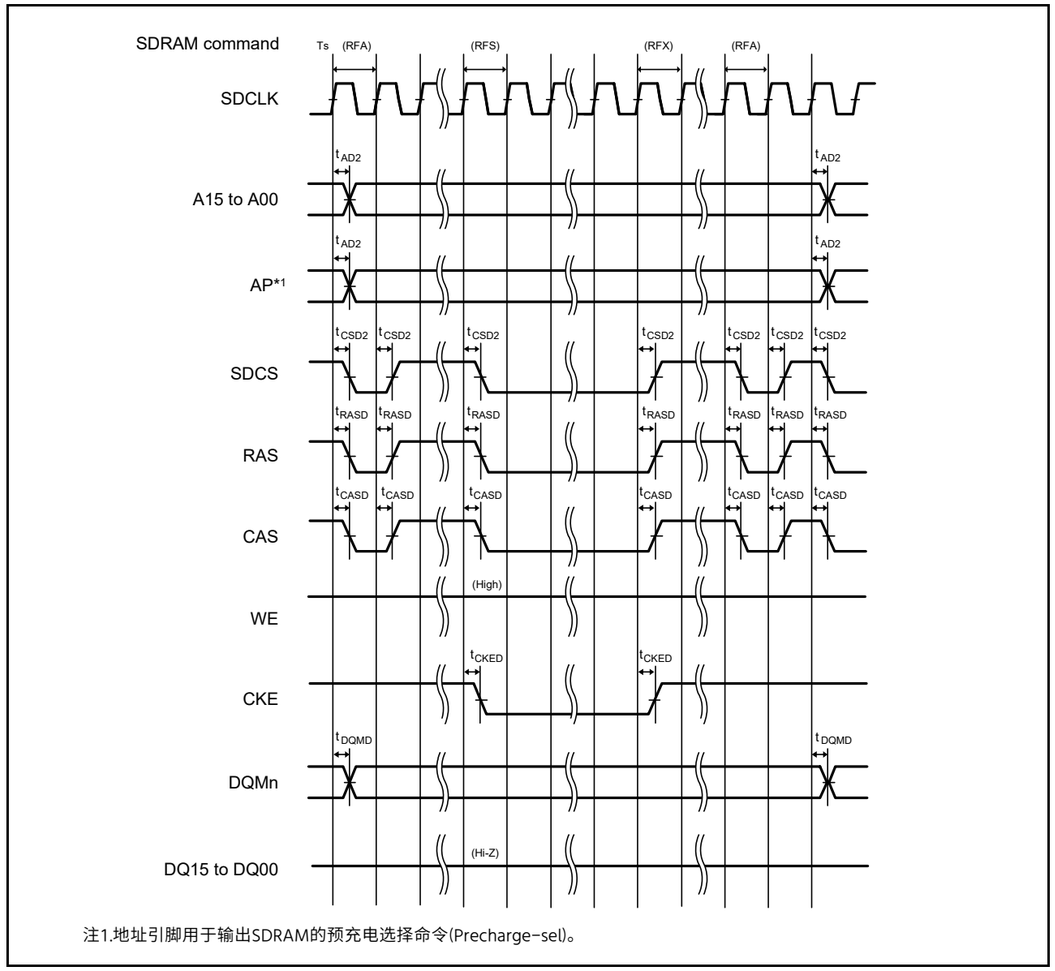
Figure 2.33 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)
GPT32 Conditions:
High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.34
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.35



注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 2.33 SDRAM self-refresh timing

2.3.7 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序

Table 2.19 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序（1of2）
GPT32 Conditions:
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter		Symbol	Min	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.34
POEG	POEG输入触发脉冲宽度	t_{POEW}	3	-	t_{Pcyc}	Figure 2.35

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)
GPT32 Conditions:
High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.36
		Dual edge		2.5	-		
	GTIOCxY output skew (x = 0 to 7, Y= A or B)	Middle drive buffer	t_{GTISK}*1	-	4	ns	Figure 2.37
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.38
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*2	-	2.0	ns	Figure 2.39
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*3	100	-	ns	Figure 2.40
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.41
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 2.42

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. The load is 30 pF.
Note 3. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

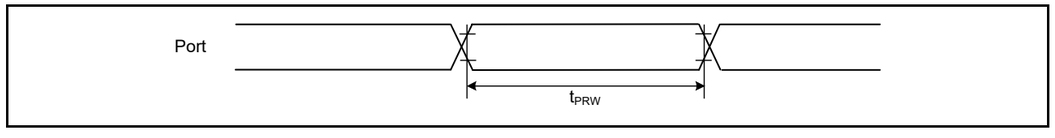


Figure 2.34 I/O ports input timing

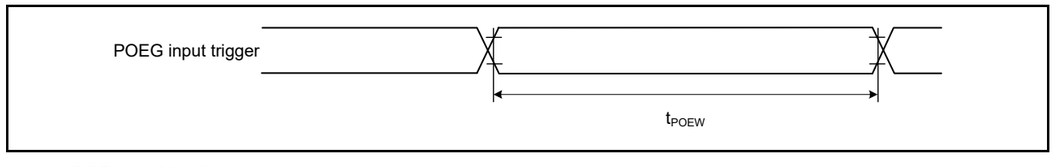


Figure 2.35 POEG input trigger timing

Table 2.19 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序(2of2)
GPT32 Conditions:
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter			Symbol	Min	Max	Unit	测试条件
GPT32	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.36
		双刃		2.5	-		
	GTIOCxY输出偏移（x=0到7，Y=A或B）	中间驱动缓冲器	t_{GTISK}*1	-	4	ns	Figure 2.37
		高驱动缓冲器		-	4		
	GTIOCxY输出偏差（x=8到13，Y=A或B）	中间驱动缓冲器		-	4		
		高驱动缓冲器		-	4		
	GTIOCxY输出偏差（x=0到13，Y=A或B）	中间驱动缓冲器		-	6		
		高驱动缓冲器		-	6		
	OPS输出偏差 GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.38
GPT(PWM 延迟产生 Circuit)	GTIOCxY_Z输出偏移（x=0到3，Y=A或B，Z=A）		t_{HRSK}*2	-	2.0	ns	Figure 2.39
AGT	AGTIO、AGTEE输入周期		t_{ACYC}*3	100	-	ns	Figure 2.40
	AGTIO、AGTEE输入高宽、低宽		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO、AGTO、AGTOA、AGTOB输出周期		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12触发输入脉冲宽度		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.41
KINT	KRn(n=00to07)脉冲宽度		t_{KR}	250	-	ns	Figure 2.42

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. 当使用相同的驱动程序IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。

Note 2. 负载为30pF。
Note 3. 输入周期的约束：
不切换源时钟时：tPcyc×2<tACYC应满足。
切换源时钟时：tPcyc×6<tACYC应满足。

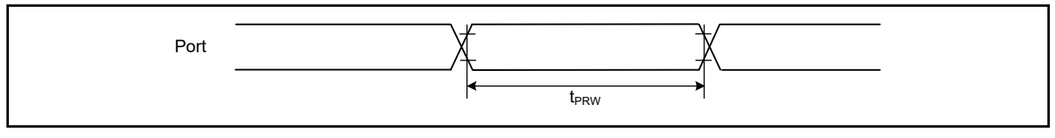


Figure 2.34 IO端口输入时序

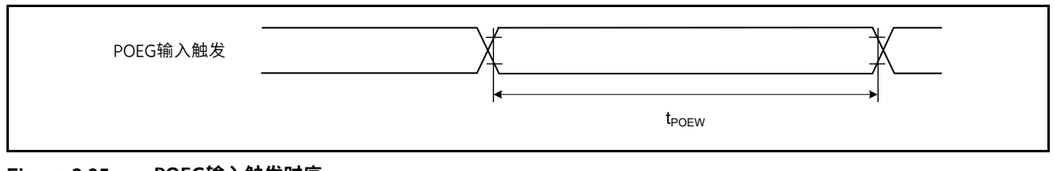


Figure 2.35 POEG输入触发时序

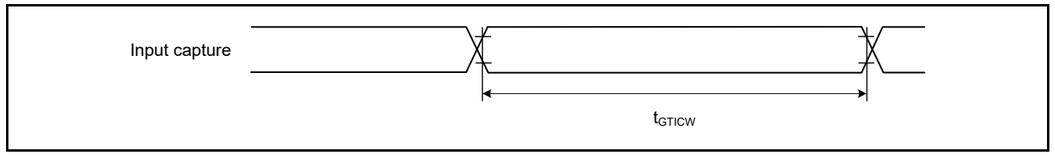


Figure 2.36 GPT32 input capture timing

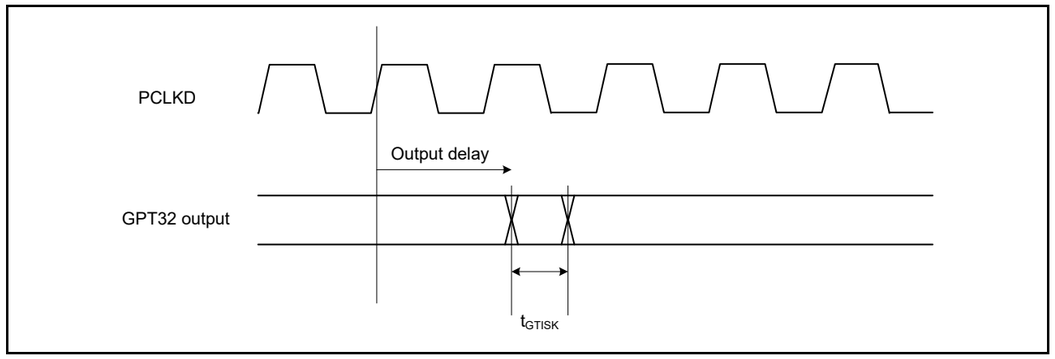


Figure 2.37 GPT32 output delay skew

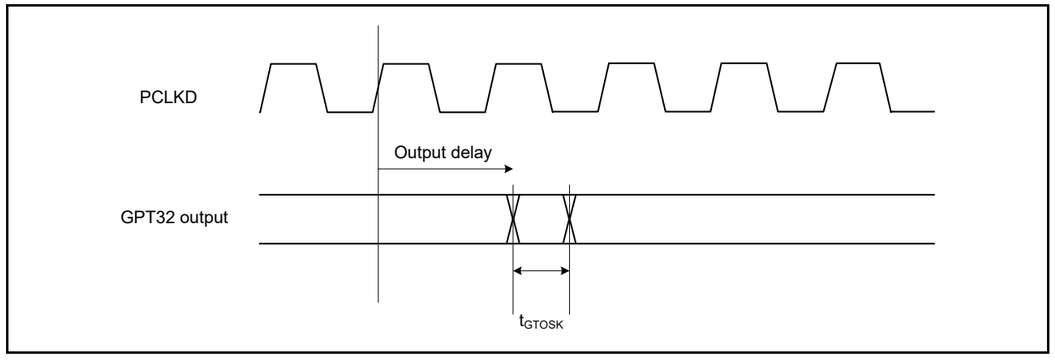


Figure 2.38 GPT32 output delay skew for OPS

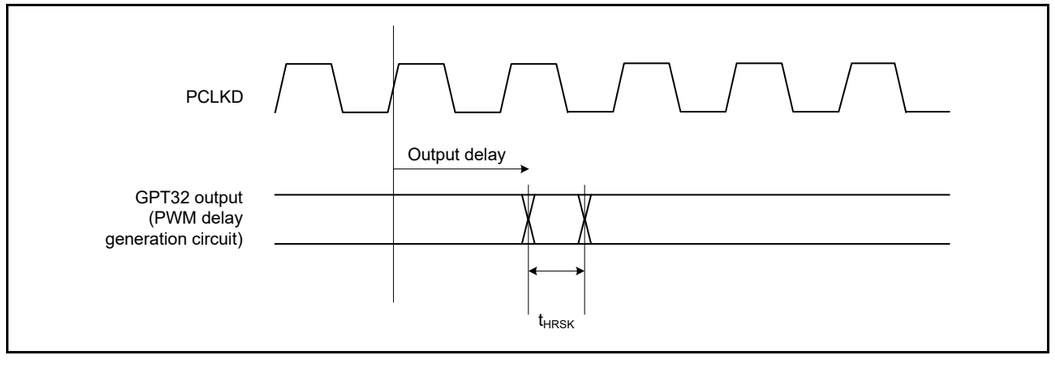


Figure 2.39 GPT32 (PWM Delay Generation Circuit) output delay skew

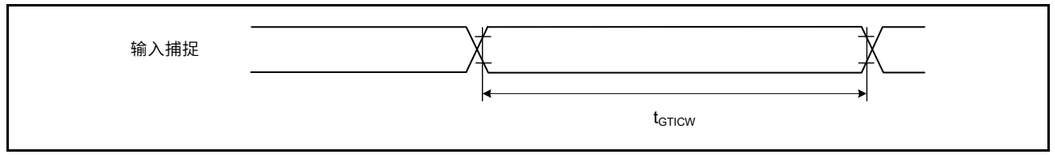


Figure 2.36 GPT32输入捕捉时序

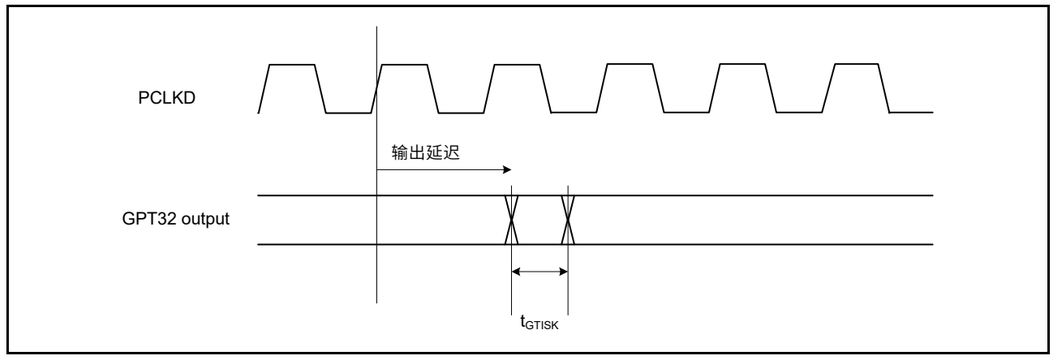


Figure 2.37 GPT32输出延迟偏移

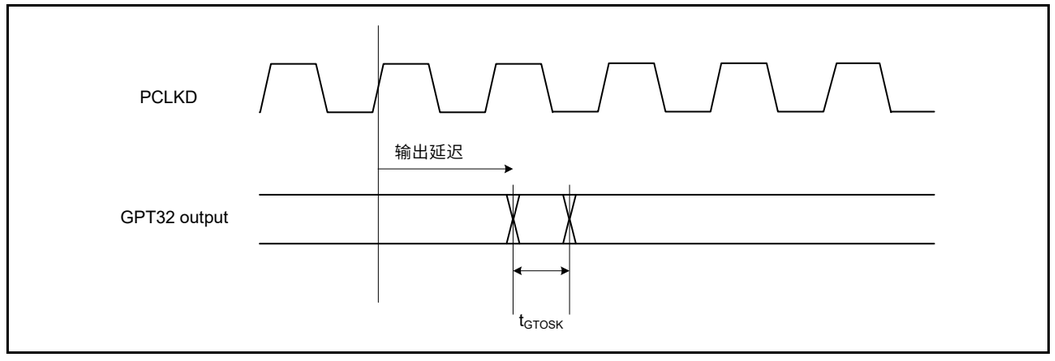


Figure 2.38 用于OPS的GPT32输出延迟偏移

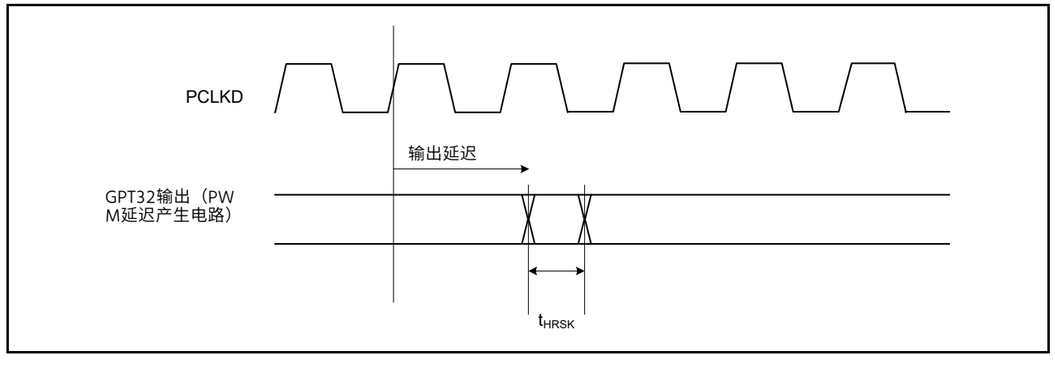


Figure 2.39 GPT32（PWM延迟生成电路）输出延迟偏移

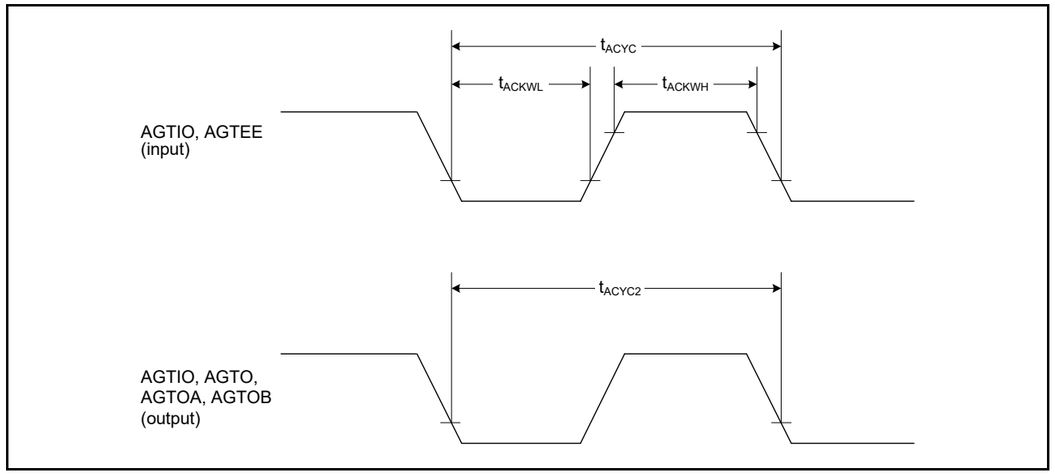


Figure 2.40 AGT input/output timing

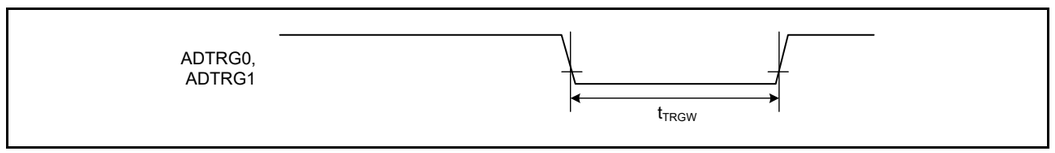


Figure 2.41 ADC12 trigger input timing

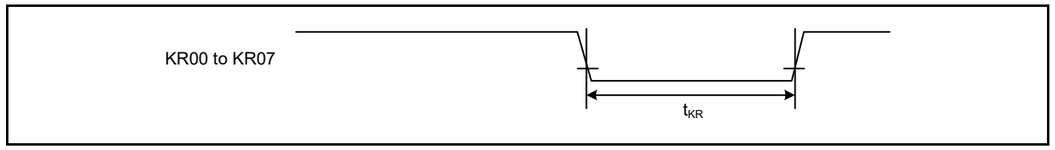


Figure 2.42 Key interrupt input timing

2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.9 CAC Timing

Table 2.21 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

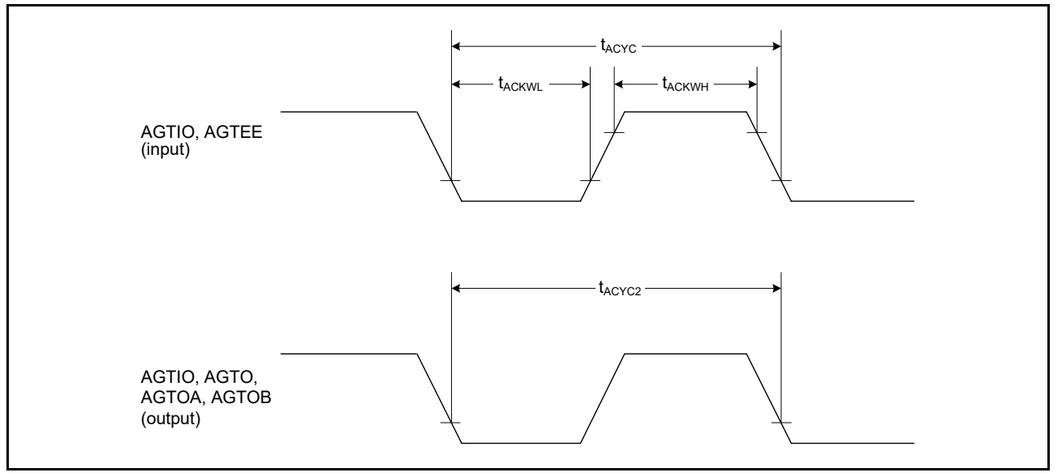


Figure 2.40 AGT input/output timing

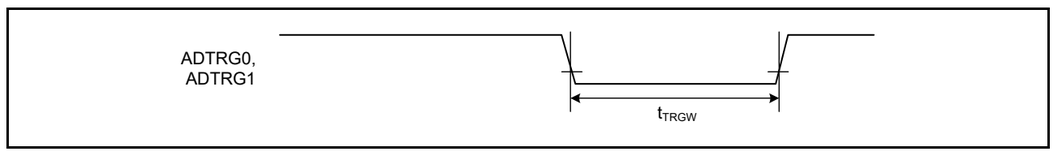


Figure 2.41 ADC12触发输入时序

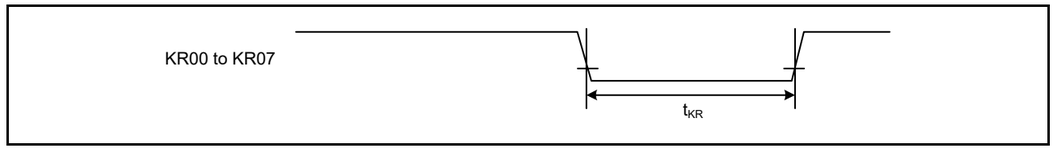


Figure 2.42 按键中断输入时序

2.3.8 PWM延迟产生电路时序

Table 2.20 PWM延迟产生电路时序

Parameter	Min	Typ	Max	Unit	测试条件
运行频率	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. 此值标准化1-LSB分辨率中的行之间的差异。

2.3.9 CAC时序

Table 2.21 CAC计时

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	$t_{PBcyc} \le tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

2.3.10 SCI Timing

Table 2.22 SCI timing (1)
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.43
		Clock synchronous		6	-		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	-	5	ns	
	Input clock fall time		t_{SCKf}	-	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous		4	-		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	-	5	ns	
	Output clock fall time		t_{SCKf}	-	5	ns	
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns	Figure 2.44
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

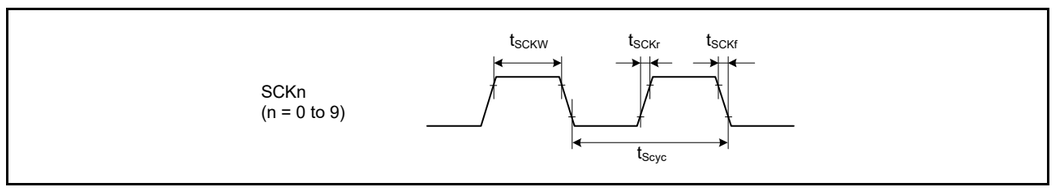


Figure 2.43 SCK clock input/output timing

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. tcac:CAC计数时钟源周期。

2.3.10 SCI时序

Table 2.22 SCI时序（1）
条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高驱动输出：SCK0至SCK9。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit*1	测试条件
SCI	输入时钟周期	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.43
		时钟同步		6	-		
	输入时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间		t_{SCKr}	-	5	ns	
	输入时钟下降时间		t_{SCKf}	-	5	ns	
	输出时钟周期	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		时钟同步		4	-		
	输出时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		t_{SCKr}	-	5	ns	
	输出时钟下降时间		t_{SCKf}	-	5	ns	
	传输数据延迟	时钟同步	t_{TXD}	-	25	ns	Figure 2.44
	接收数据建立时间	时钟同步	t_{RXS}	15	-	ns	
	接收数据保持时间	时钟同步	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

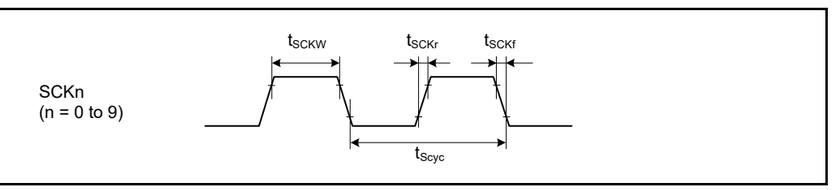


Figure 2.43 SCK时钟输入输出时序

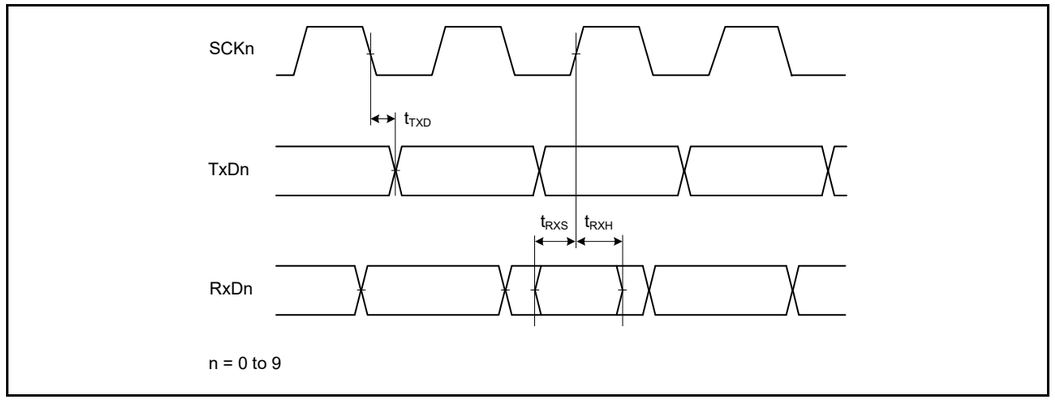


Figure 2.44 SCI input/output timing in clock synchronous mode

Table 2.23 SCI timing (2)
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 2.45
	SCK clock cycle input (slave)	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	Data input setup time	t_{SU}	33.3	-	ns	Figure 2.46 to Figure 2.49
	Data input hold time	t_H	33.3	-	ns	
	SS input setup time	t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	t_{OD}	-	33.3	ns	
	Data output hold time	t_{OH}	-10	-	ns	
	Data rise and fall time	t_{Dr}, t_{Df}	-	16.6	ns	
	SS input rise and fall time	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	Slave access time	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 2.49
	Slave output release time	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

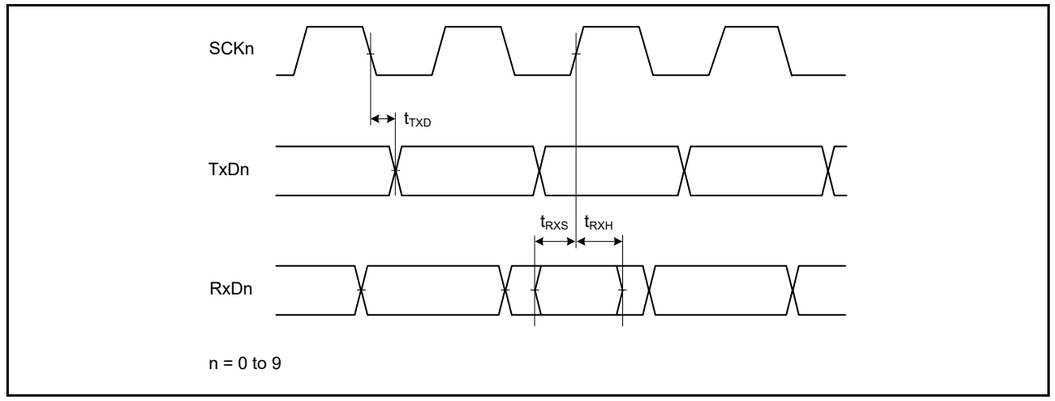


Figure 2.44 时钟同步模式下的SCI输入输出时序

Table 2.23 SCI时序（2）
条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高驱动输出：SCK0至SCK9。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple SPI	SCK时钟周期输出（主机）	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 2.45
	SCK时钟周期输入（从机）	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK时钟高脉冲宽度	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	数据输入建立时间	t_{SU}	33.3	-	ns	图2.46至Figure 2.49
	数据输入保持时间	t_H	33.3	-	ns	
	SS输入建立时间	t_{LEAD}	1	-	t_{SPcyc}	
	SS输入保持时间	t_{LAG}	1	-	t_{SPcyc}	
	数据输出延迟	t_{OD}	-	33.3	ns	
	数据输出保持时间	t_{OH}	-10	-	ns	
	数据上升和下降时间	t_{Dr}, t_{Df}	-	16.6	ns	
	SS输入上升和下降时间	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	从站访问时间	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 2.49
	从机输出释放时间	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

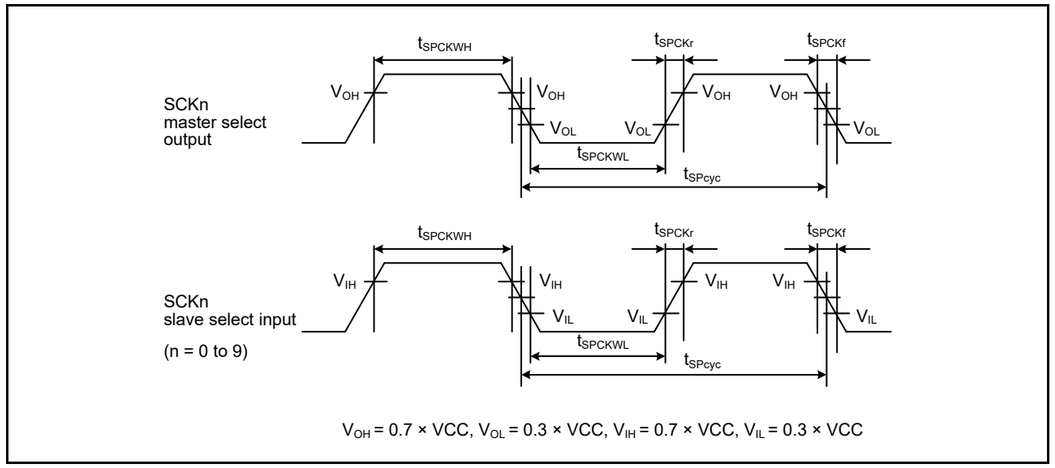


Figure 2.45 SCI simple SPI mode clock timing

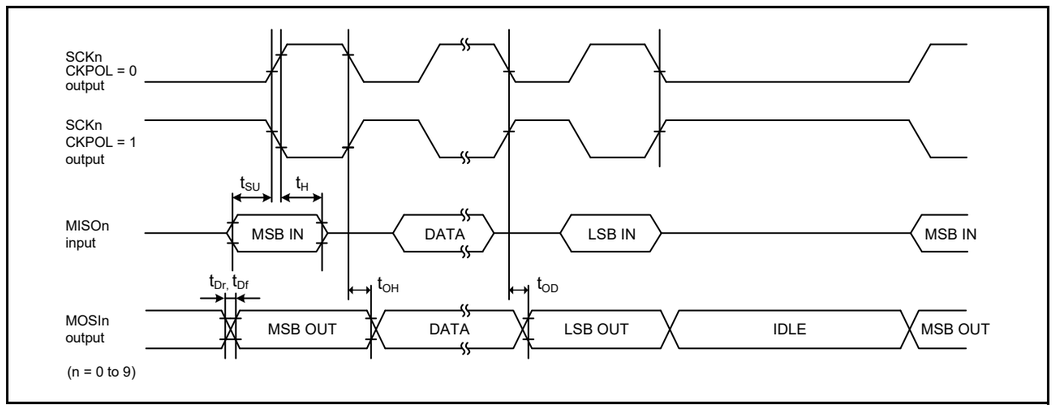


Figure 2.46 SCI simple SPI mode timing for master when CKPH = 1

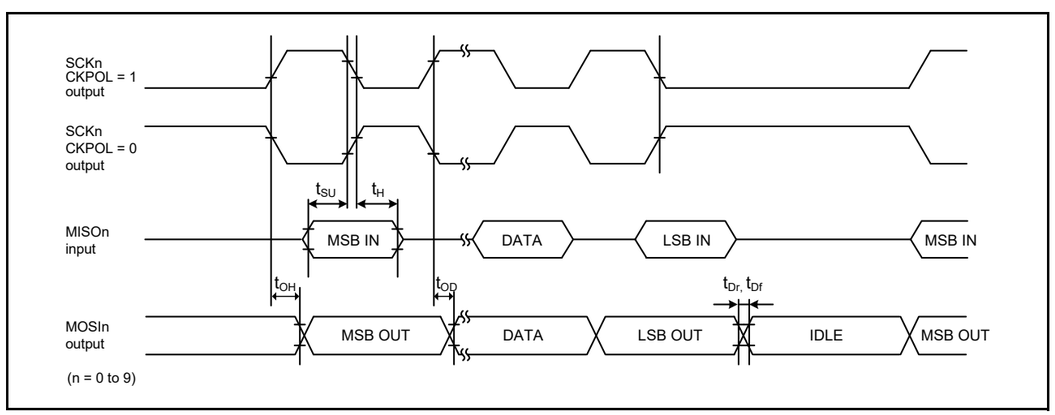


Figure 2.47 SCI simple SPI mode timing for master when CKPH = 0

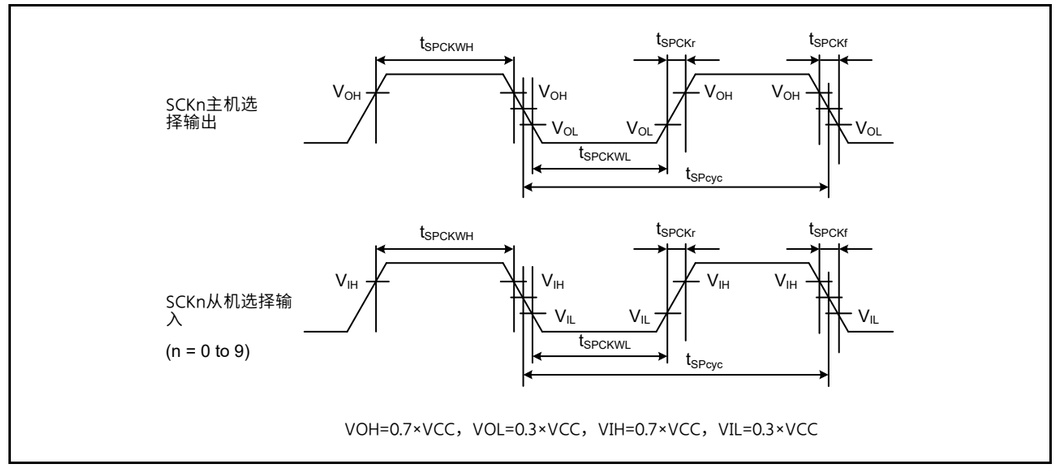


Figure 2.45 SCI简单SPI模式时钟时序

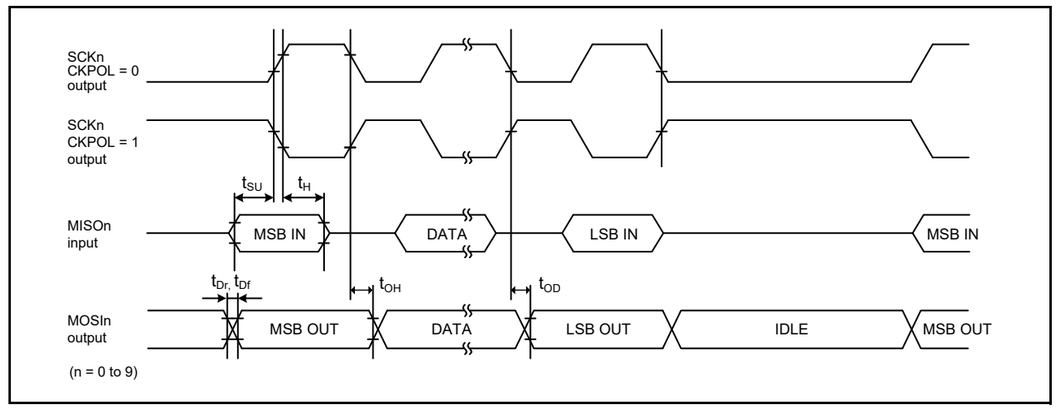


Figure 2.46 CKPH=1时主机的SCI简单SPI模式时序

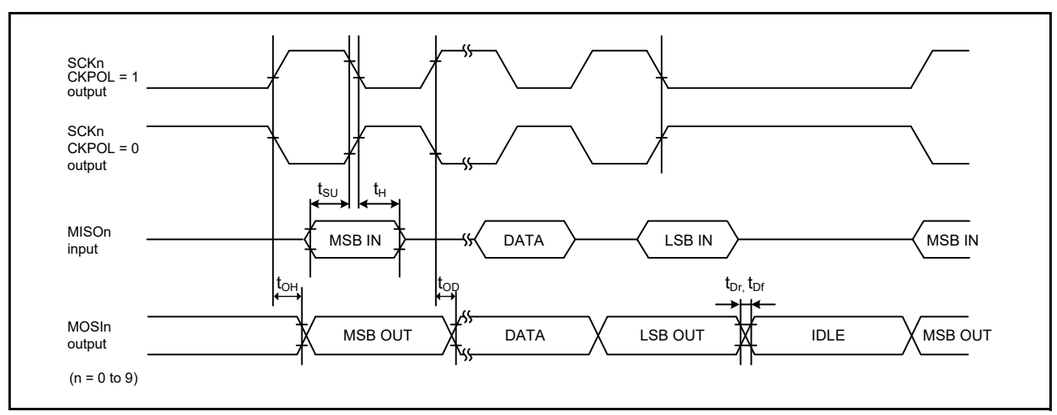


Figure 2.47 CKPH=0时主机的SCI简单SPI模式时序

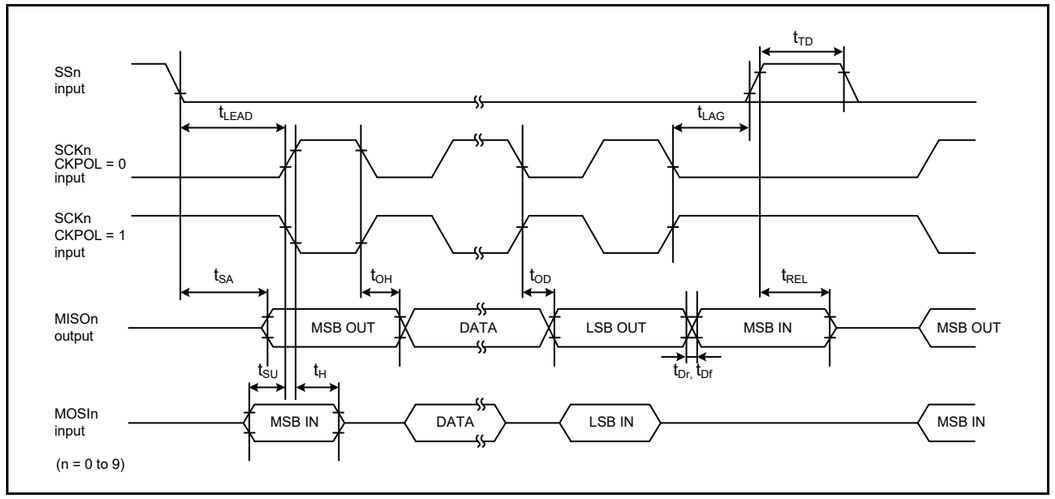


Figure 2.48 SCI simple SPI mode timing for slave when CKPH = 1

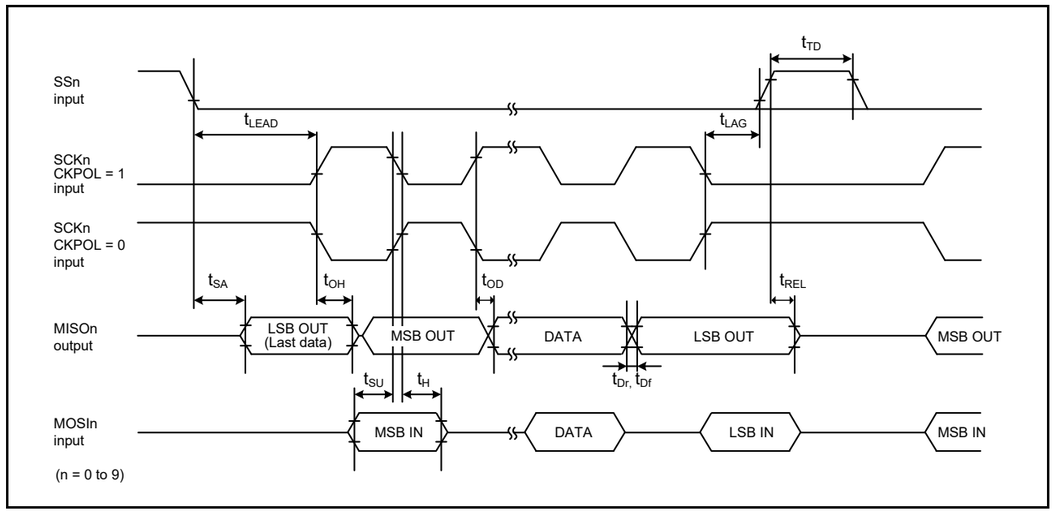


Figure 2.49 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1 of 2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.50
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

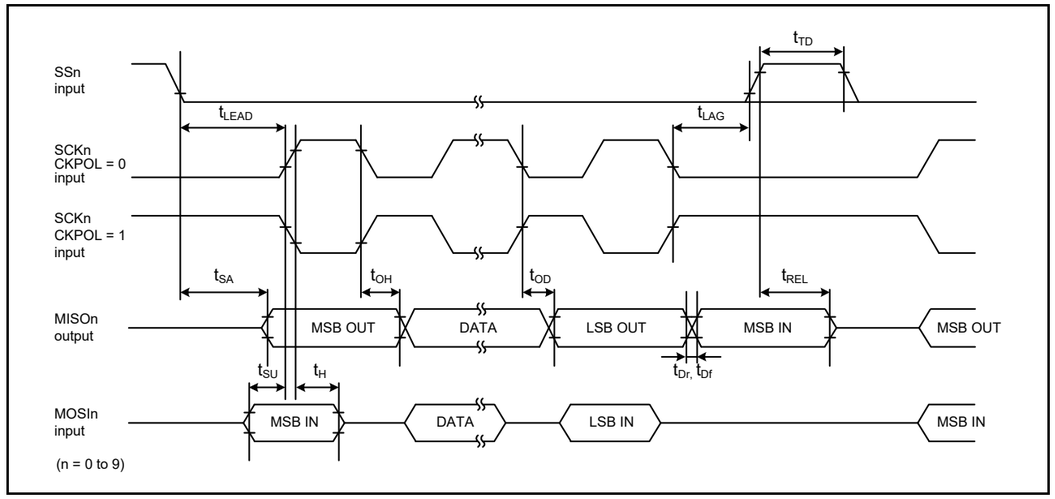


Figure 2.48 CKPH=1时从机的SCI简单SPI模式时序

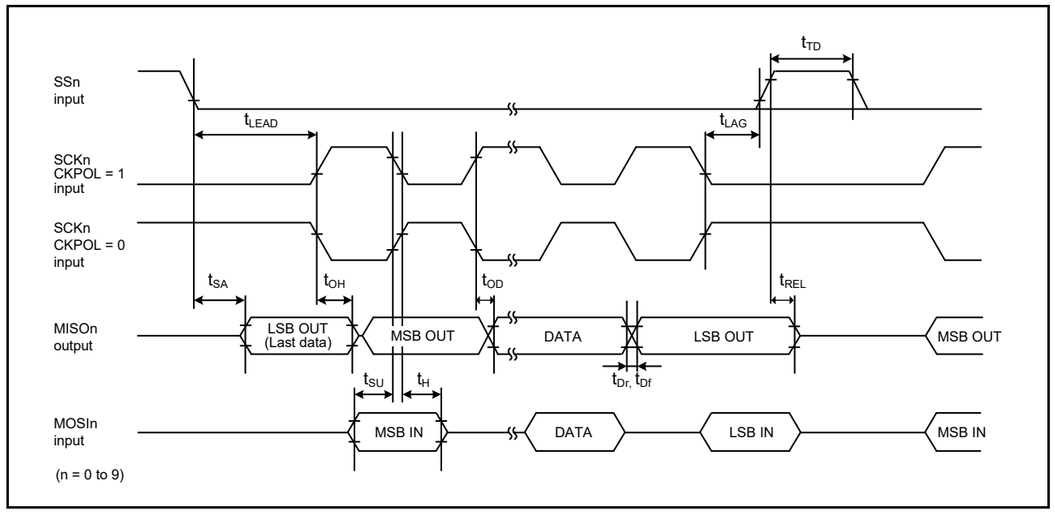


Figure 2.49 CKPH=0时从机的SCI简单SPI模式时序

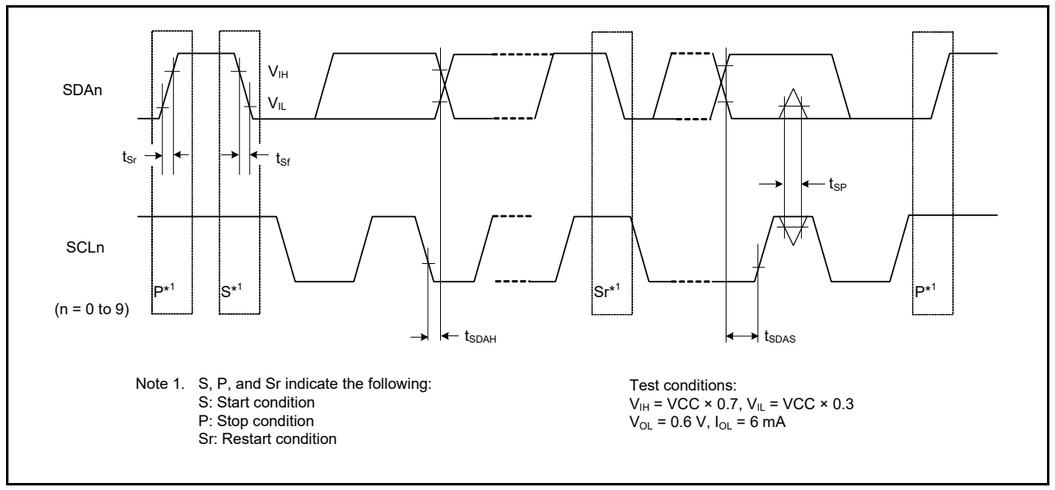
Table 2.24 SCI计时(3)(1of2)
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	-	1000	ns	Figure 2.50
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	250	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Table 2.24 SCI timing (3) (2 of 2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.50
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. Cb indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

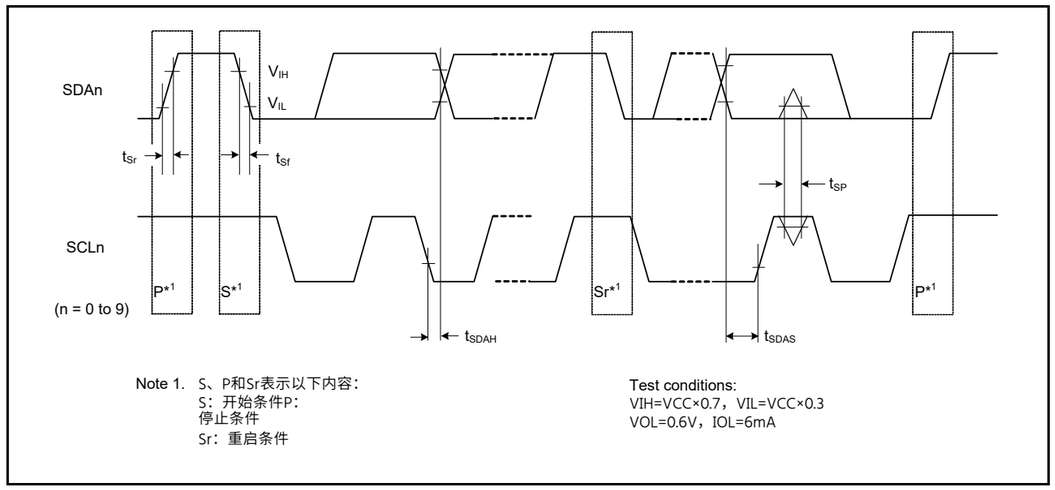
Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 2.50 SCI simple IIC mode timing

Table 2.24 SCI计时(3)(2of2)
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	-	300	ns	Figure 2.50
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	100	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note 1. Cb表示公交线路的总容量。



Note 1. S、P和Sr表示以下内容：
S：开始条件P：
停止条件
Sr：重启条件

Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA

Figure 2.50 SCI简单IIC模式时序

2.3.11 SPI Timing

Table 2.25 SPI timing
Conditions:
For RSPCKA and RSPCKB pins, high drive output is selected with the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.51 C = 30 pF
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 2.52 to Figure 2.57 C = 30 pF
		Slave		5	-		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	-	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} - 10*3	N × t_{SPcyc} + 100*3	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	SSL hold time	Master	t_{LAG}	N × t_{SPcyc} - 10 *4	N × t_{SPcyc} + 100*4	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	Data output delay	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		6 × t_{Pcyc}			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	2 x t_{Pcyc} + 28	ns	Figure 2.56 and Figure 2.57 C = 30pF
	Slave output release time		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.

2.3.11 SPI时序

Table 2.25 SPI时序
Conditions:
对于RSPCKA和RSPCKB引脚，通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK时钟周期	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.51 C = 30 pF
		Slave		4	4096		
	RSPCK时钟高脉冲宽度	Master	t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK时钟低脉冲宽度	Master	t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK时钟上升和下降时间	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	数据输入建立时间	Master	t_{SU}	4	-	ns	图2.52至 Figure 2.57 C = 30 pF
		Slave		5	-		
	数据输入保持时间	主控（PCLKA分频比设置为12）	t_{HF}	0	-	ns	
		主控（PCLKA分频比设置为12以外的值）	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL设置时间	Master	t_{LEAD}	N × t_{SPcyc} - 10*3	N × t_{SPcyc} + 100*3	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	SSL保持时间	Master	t_{LAG}	N × t_{SPcyc} - 10 *4	N × t_{SPcyc} + 100*4	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	数据输出延迟	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	数据输出保持时间	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	连续传输延迟	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		6 × t_{Pcyc}			
	MOSI和MISO上升和下降时间	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL上升和下降时间	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	从站访问时间		t_{SA}	-	2 x t_{Pcyc} + 28	ns	图2.56和 Figure 2.57 C = 30pF
	从机输出释放时间		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
Note 4. N is set to an integer from 1 to 8 by the SSLND register.

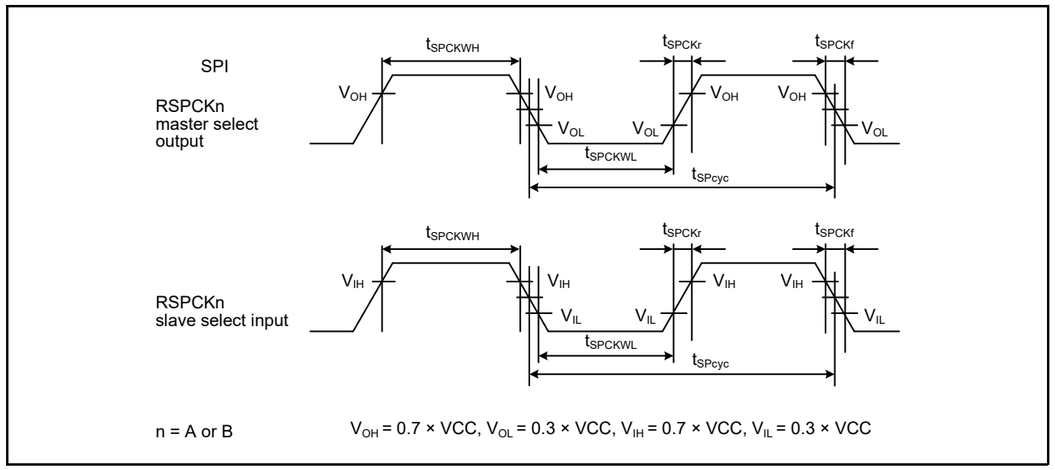


Figure 2.51 SPI clock timing

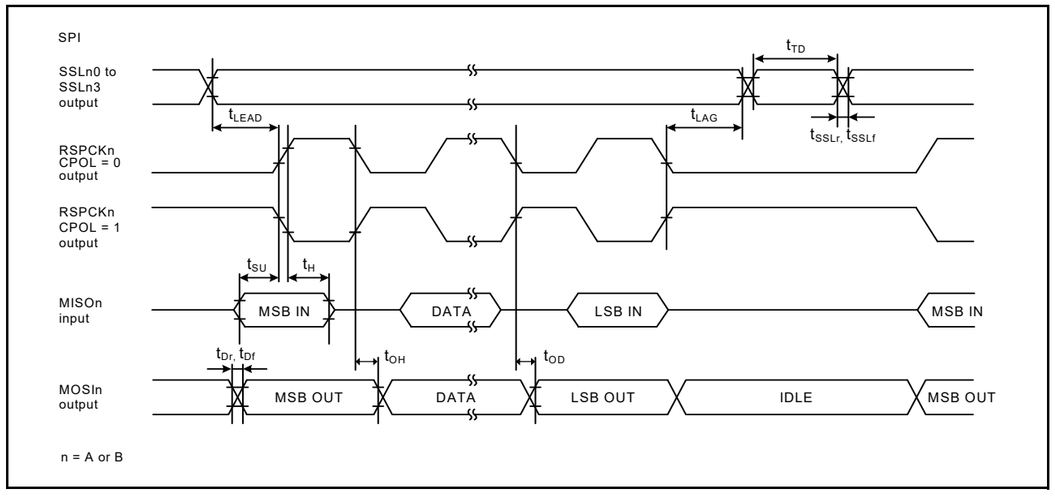


Figure 2.52 SPI timing for master when CPHA = 0

Note 2. 必须使用带有字母（“_A”、“_B”）的引脚来表示作为组附加到其名称的组成员身份。对于SPI接口，测量每组的电气特性的交流部分。
Note 3. N由SPCKD寄存器设置为从1到8的整数。
Note 4. N由SSLND寄存器设置为从1到8的整数。

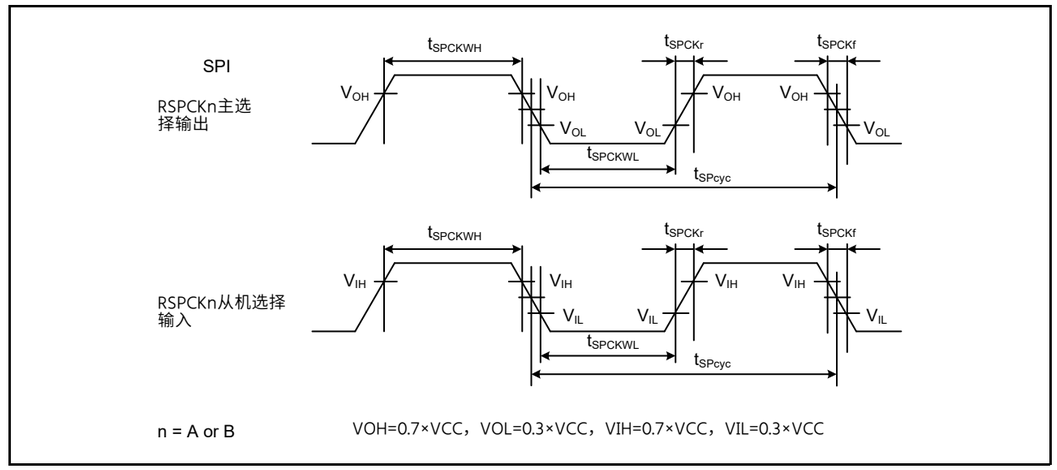


Figure 2.51 SPI时钟时序

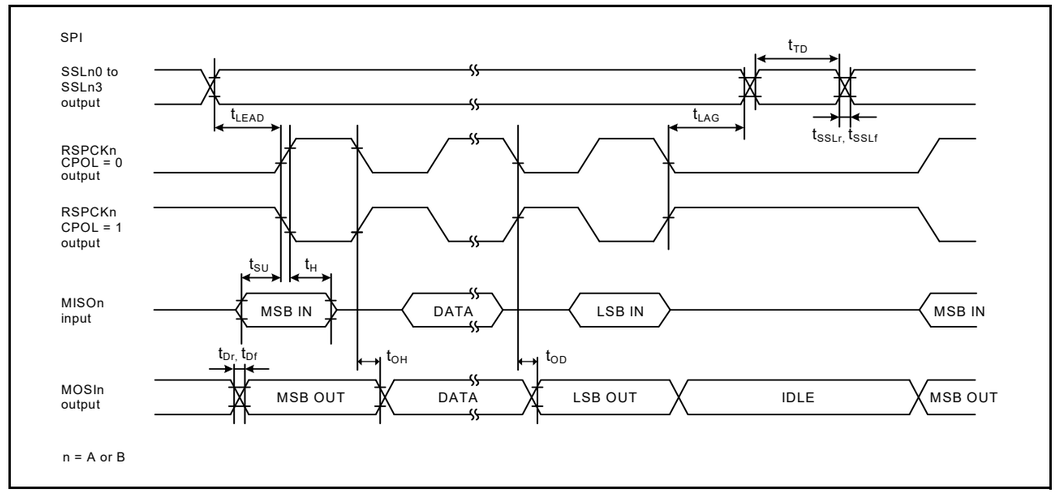


Figure 2.52 CPHA=0时主机的SPI时序

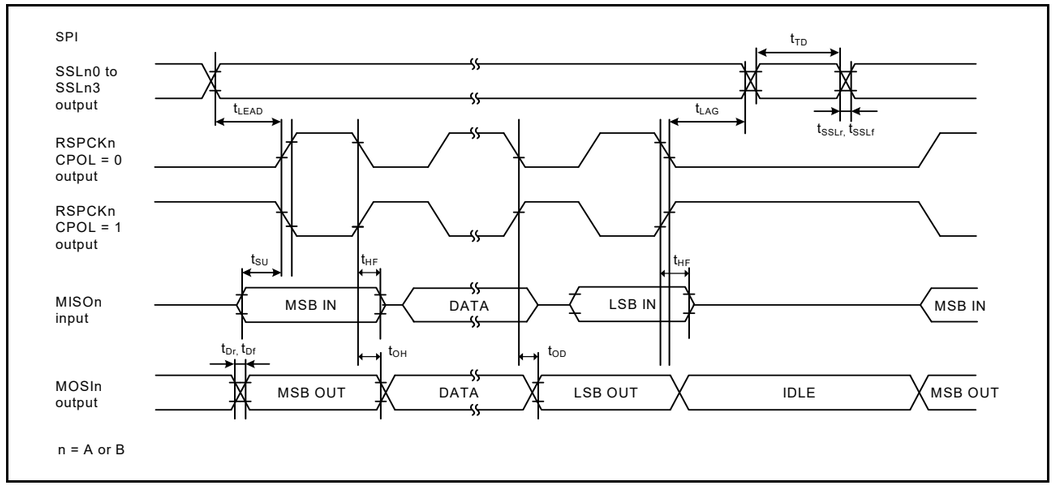


Figure 2.53 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

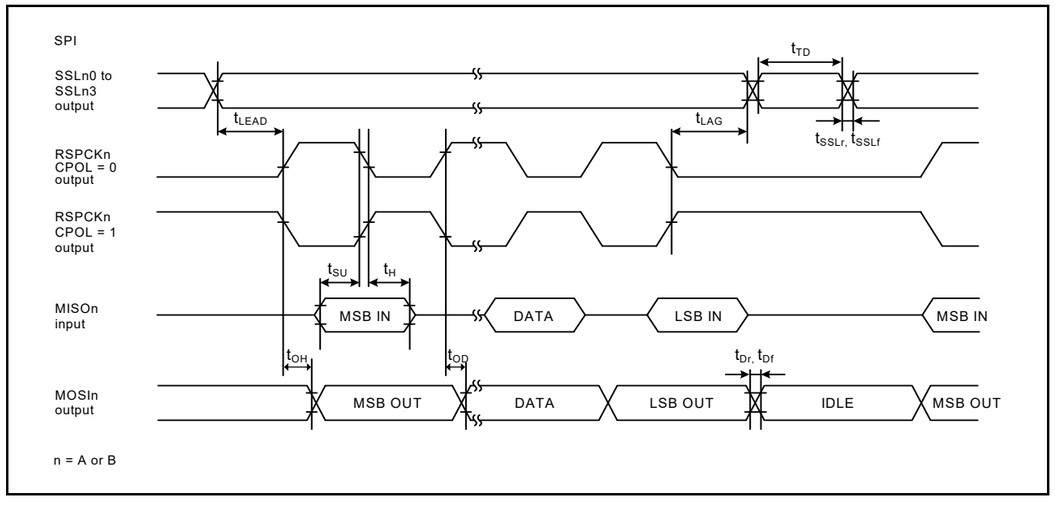


Figure 2.54 SPI timing for master when CPHA = 1

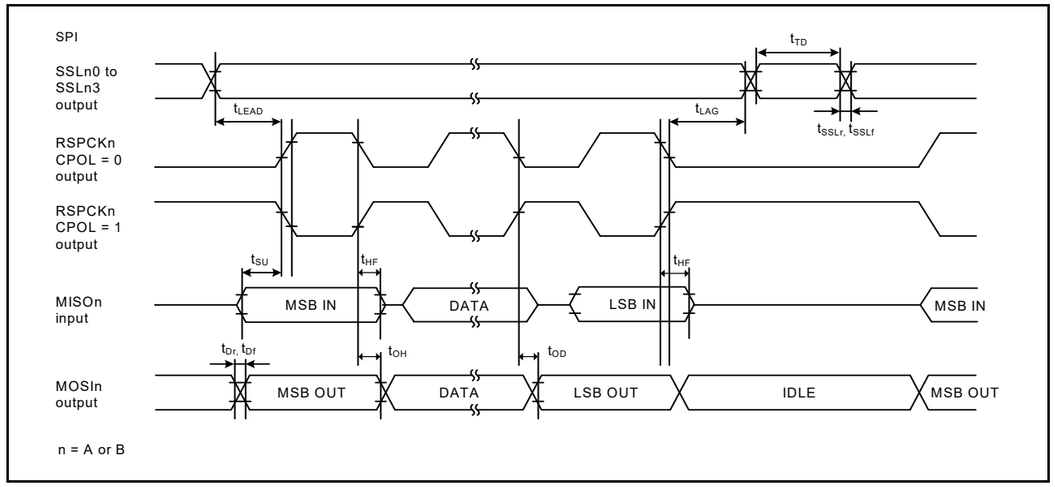


Figure 2.53 当CPHA=0且比特率设置为PCLKA2时主设备的SPI时序

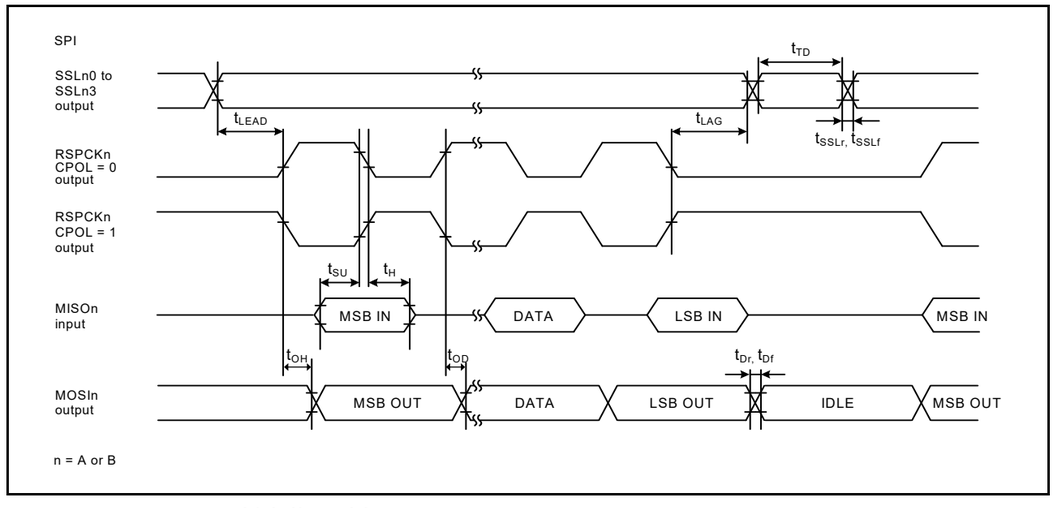


Figure 2.54 CPHA=1时主机的SPI时序

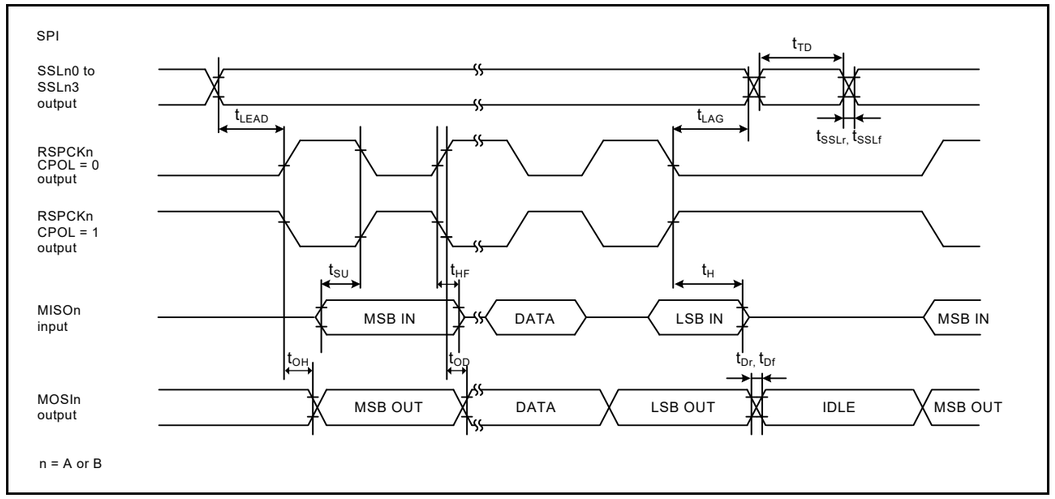


Figure 2.55 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

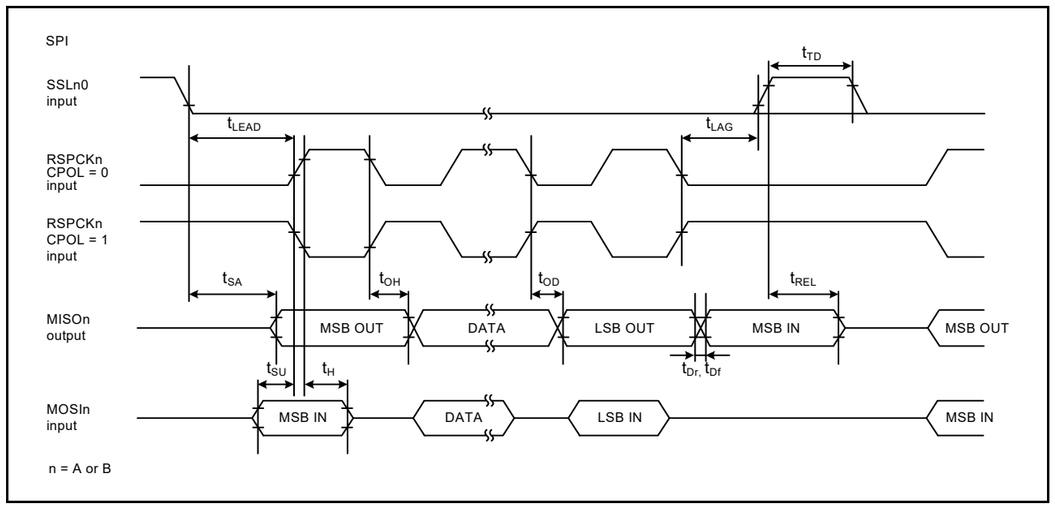


Figure 2.56 SPI timing for slave when CPHA = 0

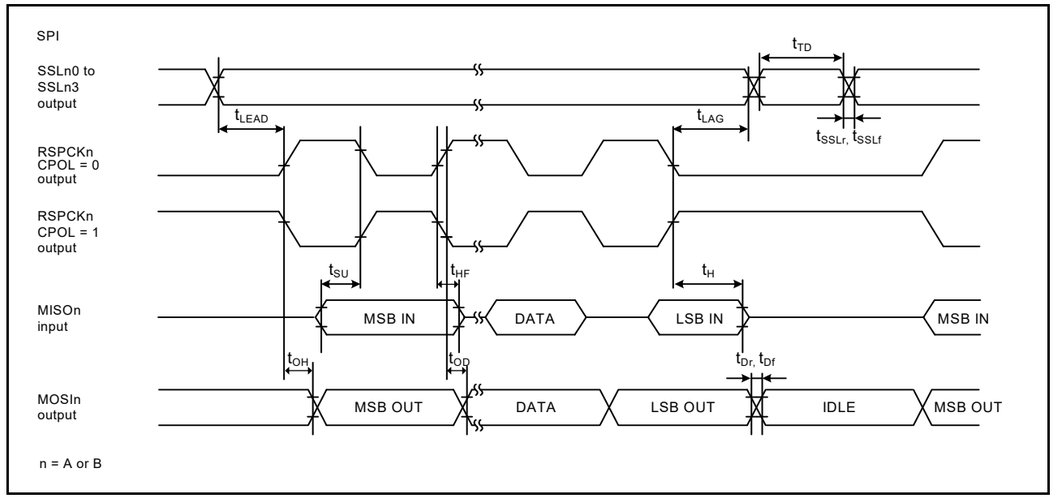


Figure 2.55 当CPHA=1且比特率设置为PCLKA2时，主机的RSPI时序

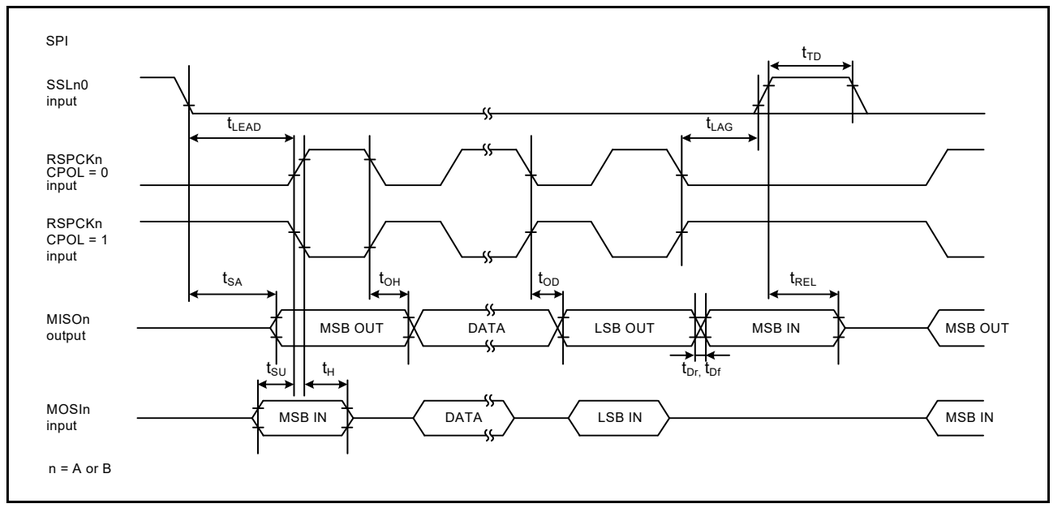


Figure 2.56 CPHA=0时从机的SPI时序

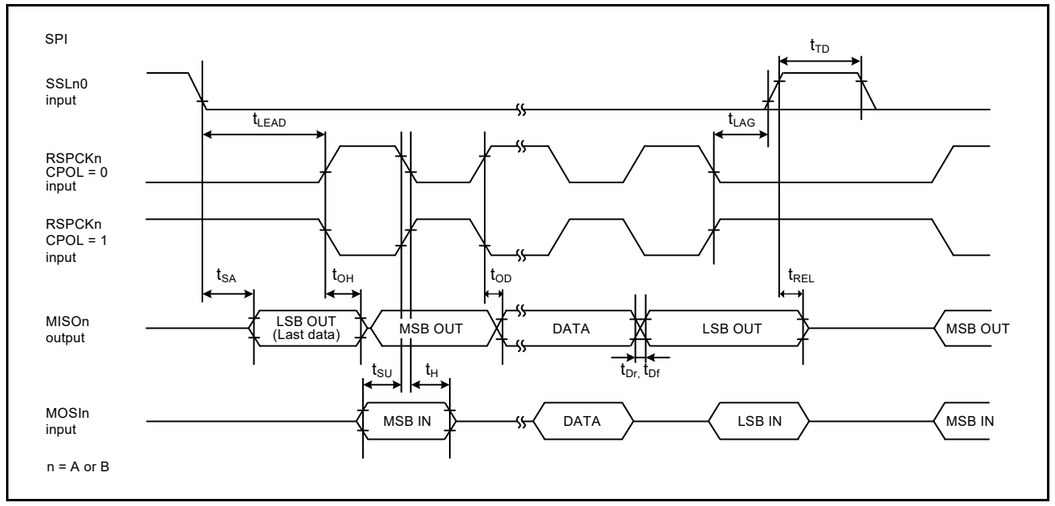


Figure 2.57 SPI timing for slave when CPHA = 1

2.3.12 QSPI Timing

Table 2.26 QSPI timing
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit*1	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.58
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	Data input setup time	t_{Su}	8	-	ns	Figure 2.59
	Data input hold time	t_{IH}	0	-	ns	
	QSSL setup time	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 *2	(N+0.5) x t_{Qscyc} +100 *2	ns	
	QSSL hold time	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 *3	(N+0.5) x t_{Qscyc} +100 *3	ns	
	Data output delay	t_{OD}	-	4	ns	
	Data output hold time	t_{OH}	-3.3	-	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set to 0 or 1 in SFMSLD.
Note 3. N is set to 0 or 1 in SFMSHD.

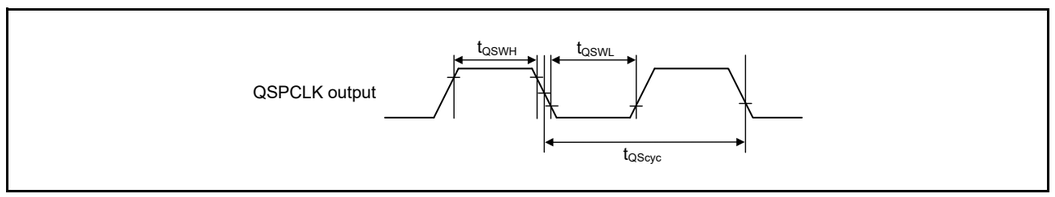


Figure 2.58 QSPI clock timing

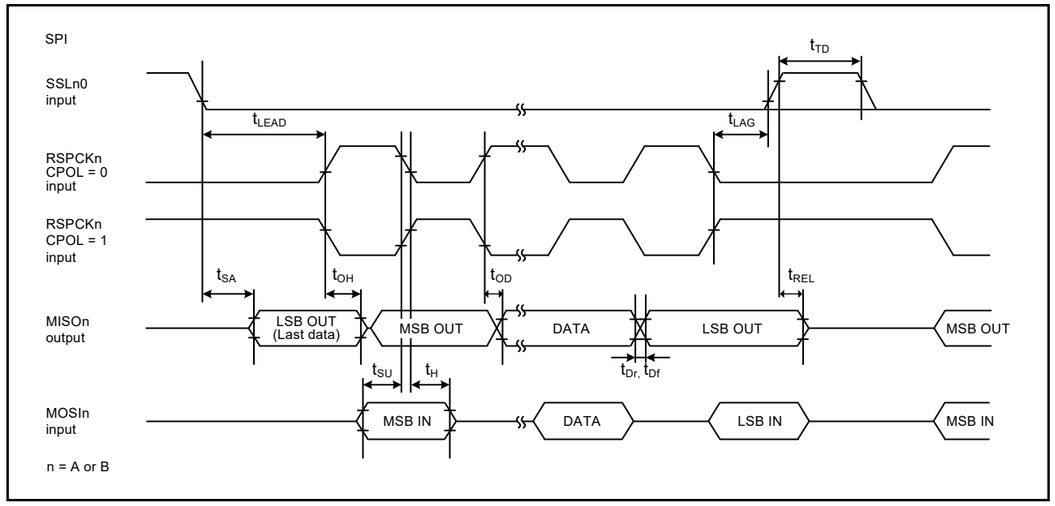


Figure 2.57 CPHA=1时从机的SPI时序

2.3.12 QSPI Timing

Table 2.26 QSPI timing
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		Symbol	Min	Max	Unit*1	测试条件
QSPI	QSPCK时钟周期	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.58
	QSPCK时钟高脉冲宽度	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK时钟低脉冲宽度	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	数据输入建立时间	t_{Su}	8	-	ns	Figure 2.59
	数据输入保持时间	t_{IH}	0	-	ns	
	QSSL设置时间	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 *2	(N+0.5) x t_{Qscyc} +100 *2	ns	
	QSSL保持时间	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 *3	(N+0.5) x t_{Qscyc} +100 *3	ns	
	数据输出延迟	t_{OD}	-	4	ns	
	数据输出保持时间	t_{OH}	-3.3	-	ns	
	连续传输延迟	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N在SFMSLD中设置为0或1。
Note 3. N在SFMSHD中设置为0或1。

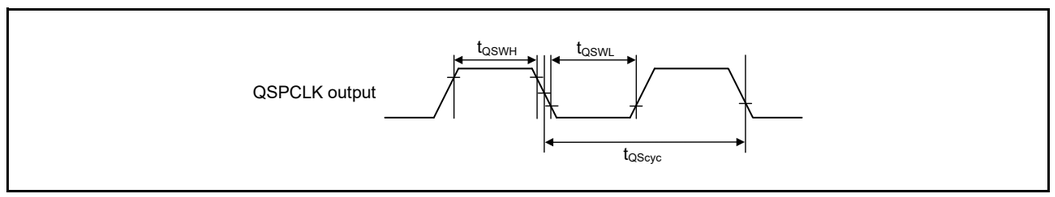


Figure 2.58 QSPI时钟时序

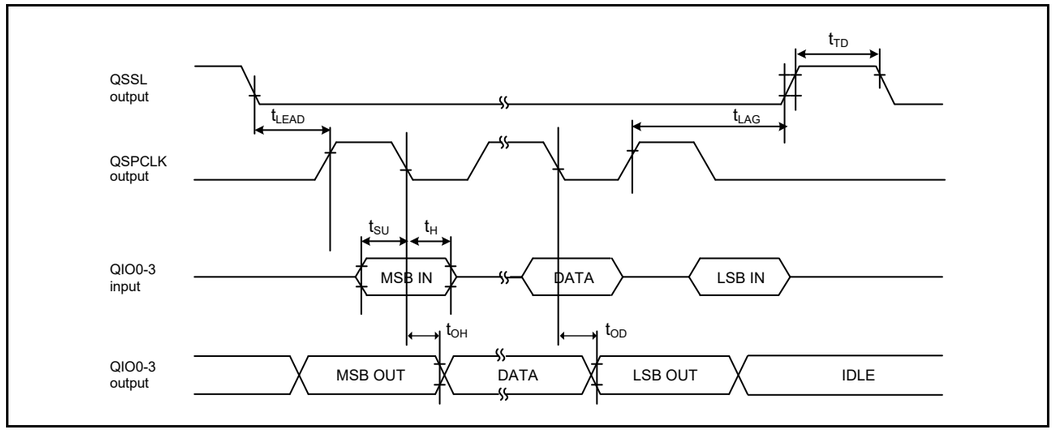


Figure 2.59 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.60
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

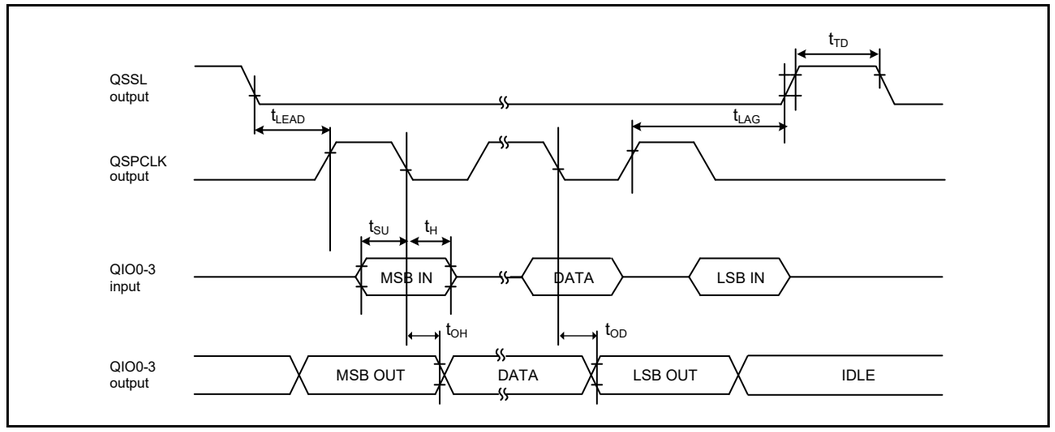


Figure 2.59 发送和接收时序

2.3.13 IIC Timing

表2.27IIC时序(1)(1of2)(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_A、SCL1_A、SDA1_B、SCL1_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL2、SDA2。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.60
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	1000	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	-	ns	
	STOP条件输入建立时间	t_{STOS}	1000	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Table 2.27 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.60
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.
Note 3. Must use pins that have a letter ("_A", "_B") to indicate group membership appended to their name as groups. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

表2.27IIC时序(1)(2of2)(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_A、SCL1_A、SDA1_B、SCL1_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL2、SDA2。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.60
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL、SDA输入下降时间	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	300	-	ns	
	STOP条件输入建立时间	t_{STOS}	300	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。
Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。
Note 2. 仅支持SCL0_A、SDA0_A、SCL2和SDA2。
Note 3. 必须使用带有字母（"_A"、"_B"）的引脚来表示作为组附加到其名称的组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Table 2.28 IIC timing (2)
Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min*1,*2	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.60
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.

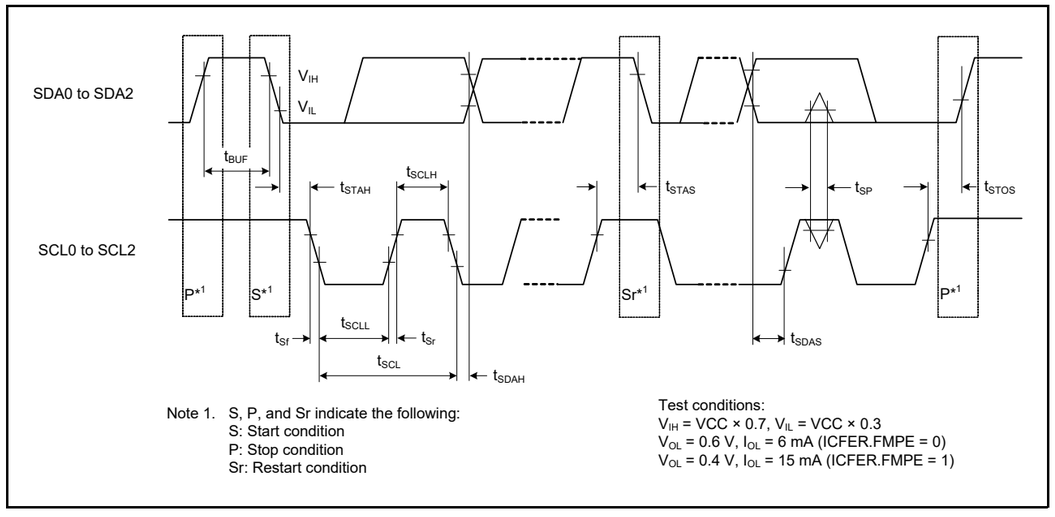


Figure 2.60 I²C bus interface input/output timing

Table 2.28 IIC timing (2)
PmnPFS寄存器中的端口驱动能力位不需要设置SCL0_A、SDA0_A引脚。

Parameter		Symbol	Min*1,*2	Max	Unit	测试条件
IIC (Fast-mode+) ICFER.FMPE = 1	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.60
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	120	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	120	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	禁用唤醒功能时的启动条件输入保持时间	t_{STAH}	t_{IICcyc} + 120	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	重启条件输入建立时间	t_{STAS}	120	-	ns	
	停止条件输入建立时间	t_{STOS}	120	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。
Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。
Note 2. Cb表示公交线路的总容量。

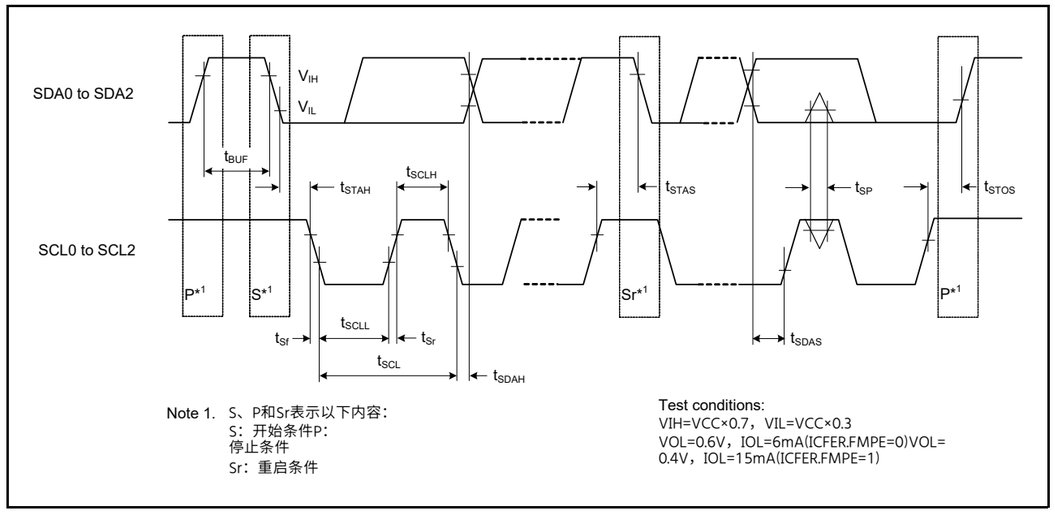


Figure 2.60 I2C总线接口输入输出时序

2.3.14 SSIE Timing

Table 2.29 SSIE timing

(1) High drive output is selected with the port drive capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK	Cycle	Master	t_O	80	-	ns	Figure 2.61
		Slave	t_I	80	-	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	Rising time/falling time	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK/SSIFS, SSITXD0, SSIRXD0, SSIDATA1	Input set up time	Master	t_{SR}	12	-	ns	Figure 2.63, Figure 2.64
		Slave		12	-	ns	
	Input hold time	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.63, Figure 2.64
	Output delay time from SSILRCK/SSIFS change	Slave	t_{DTRW}	-	20	ns	Figure 2.65*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 2.62
	High level/ low level		t_{EXL}/ t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK/SSIFS pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA1 pin.

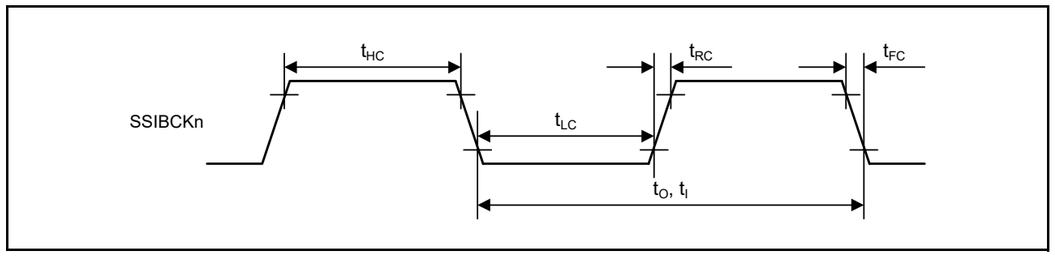


Figure 2.61 SSIE clock input/output timing

2.3.14 SSIE Timing

表2.29SSIE时序(1)通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。(2)使用名称后附有字母的引脚，例如"_A"或"_B"来表示组成员身份。对于SSIE接口，测量每组的电气特性的交流部分。

Parameter			Symbol	目标规格		Unit	Comments
				Min.	Max.		
SSIBCK	Cycle	Master	t_O	80	-	ns	Figure 2.61
		Slave	t_I	80	-	ns	
	高电平低电平	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	上升时间下降时间	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK/SSIFS, SSITXD0, SSIRXD0, SSIDATA1	输入建立时间	Master	t_{SR}	12	-	ns	Figure 2.63, Figure 2.64
		Slave		12	-	ns	
	输入保持时间	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	输出延迟时间	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.63, Figure 2.64
	从输出延迟时间 SSILRCK/SSIFS change	Slave	t_{DTRW}	-	20	ns	Figure 2.65*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 2.62
	高电平低电平		t_{EXL}/ t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. 对于从模式传输，SSIE有一个路径，通过该路径，从SSILRCKSSIFS引脚输入的信号用于生成传输数据，传输数据逻辑输出到SSITXD0或SSIDATA1引脚。

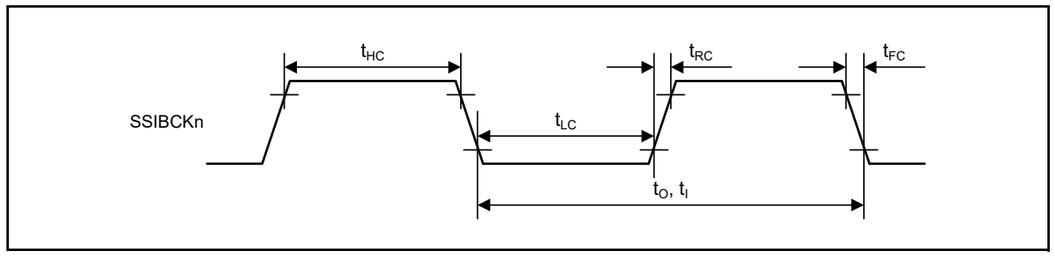


Figure 2.61 SSIE时钟输入输出时序

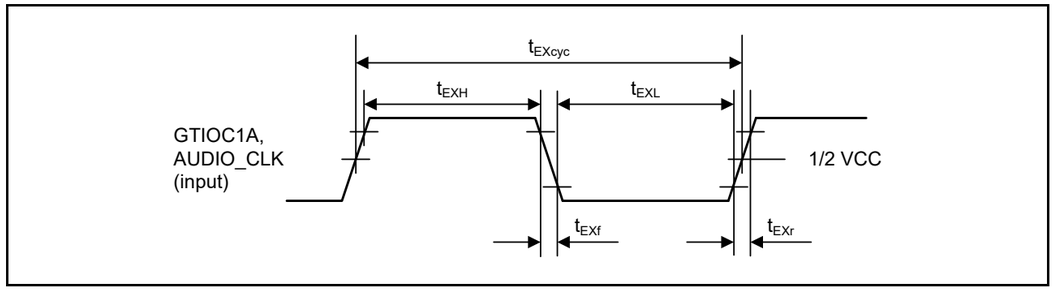


Figure 2.62 Clock input timing

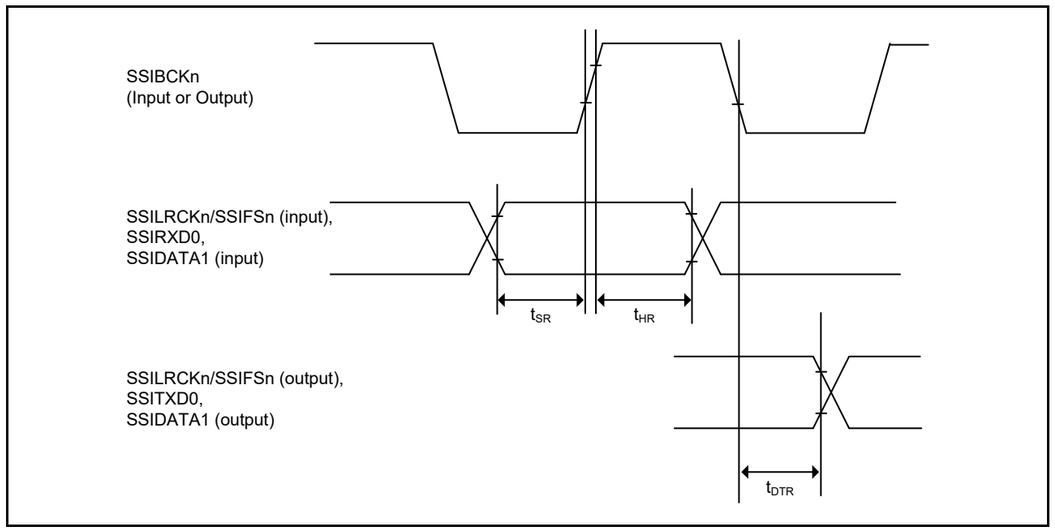


Figure 2.63 SSIE data transmit and receive timing when SSICR.BCKP = 0

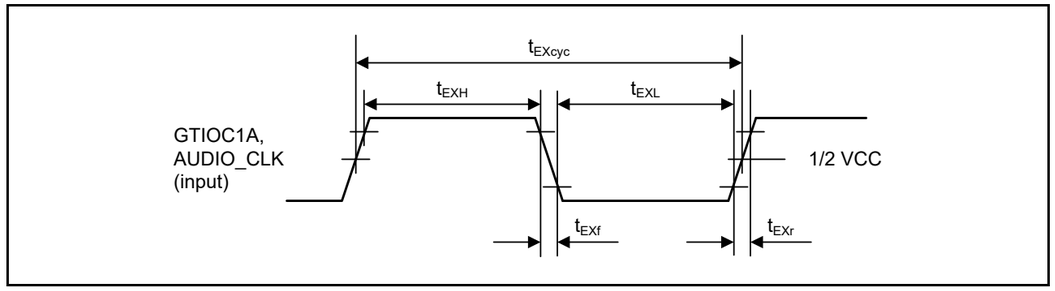


Figure 2.62 时钟输入时序

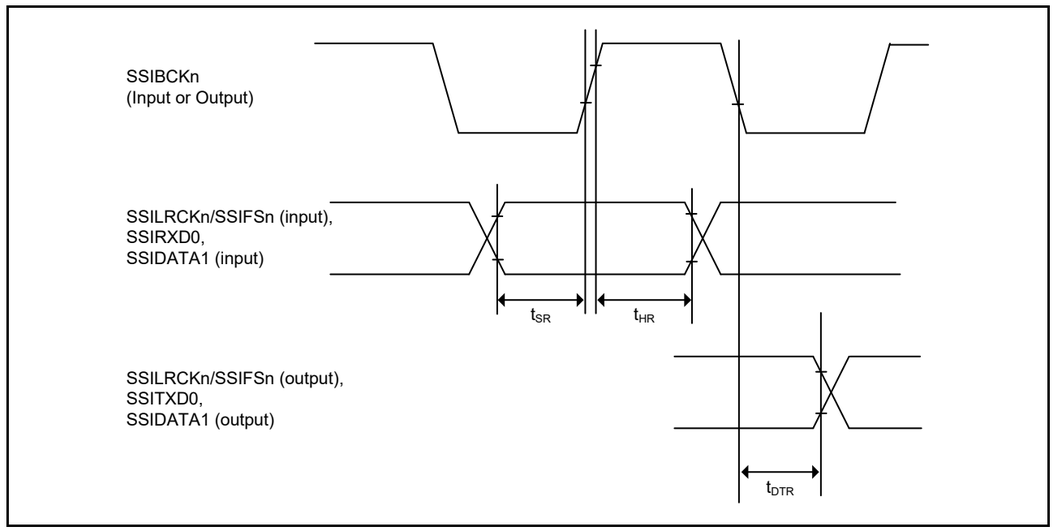


Figure 2.63 SSICR.BCKP=0时的SSIE数据发送和接收时序

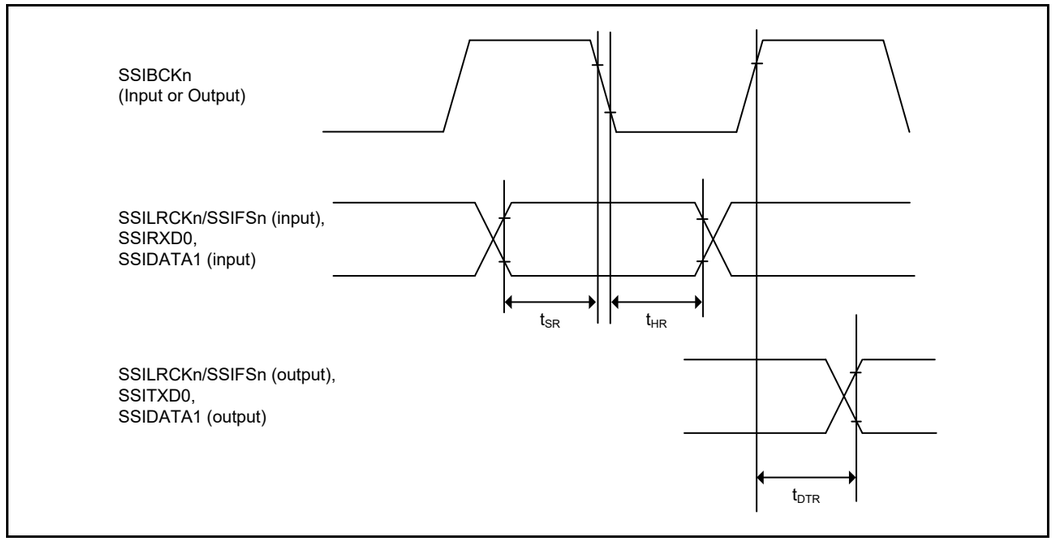


Figure 2.64 SSIE data transmit and receive timing when SSICR.BCKP = 1

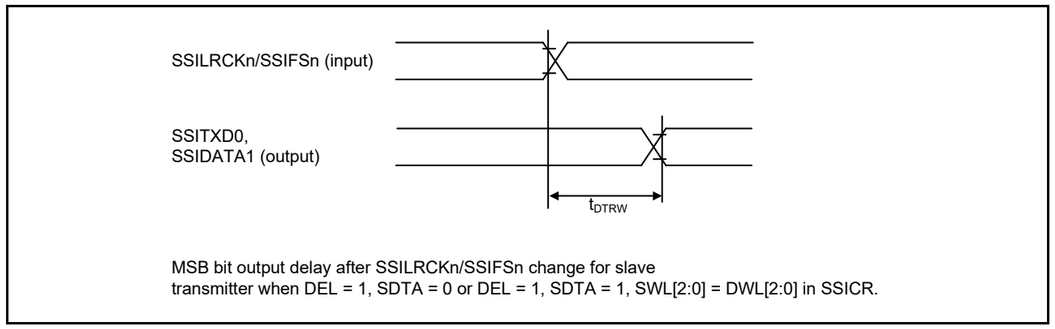


Figure 2.65 SSIE data output delay after SSILRCKn/SSIFSn change

2.3.15 SD/MMC Host Interface Timing

Table 2.30 SD/MMC Host Interface signal timing
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Parameter	Symbol	Min	Max	Unit	Test conditions*1
SDCLK clock cycle	T_{SDCYC}	20	-	ns	Figure 2.66
SDCLK clock high pulse width	T_{SDWH}	6.5	-	ns	
SDCLK clock low pulse width	T_{SDWL}	6.5	-	ns	
SDCLK clock rise time	T_{SDLH}	-	3	ns	
SDCLK clock fall time	T_{SDHL}	-	3	ns	
SDCMD/SDDAT output data delay	T_{SDODLY}	-6	5	ns	
SDCMD/SDDAT input data setup	T_{SDIS}	4	-	ns	
SDCMD/SDDAT input data hold	T_{SDIH}	2	-	ns	

Note 1. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For

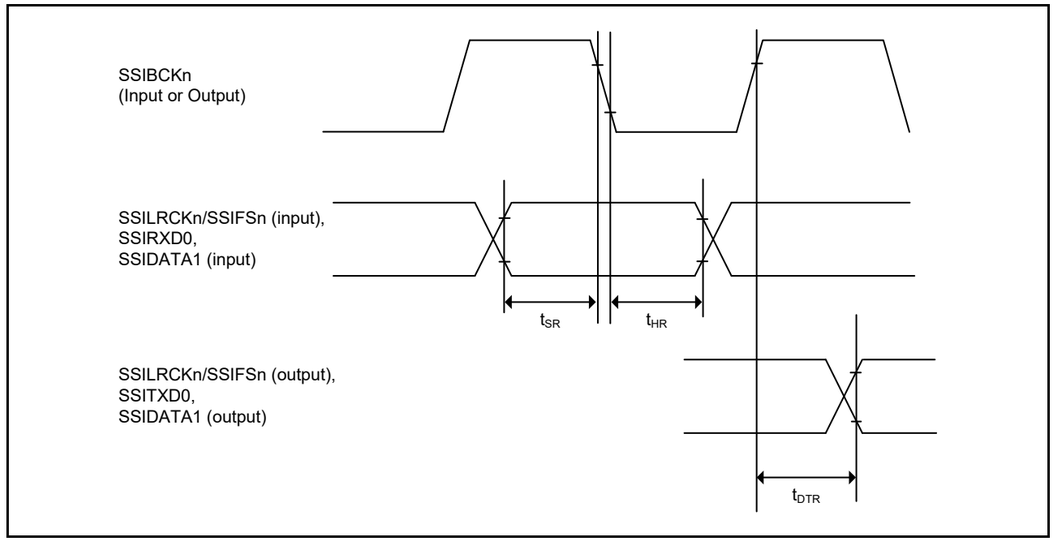


Figure 2.64 SSICR.BCKP=1时的SSIE数据发送和接收时序

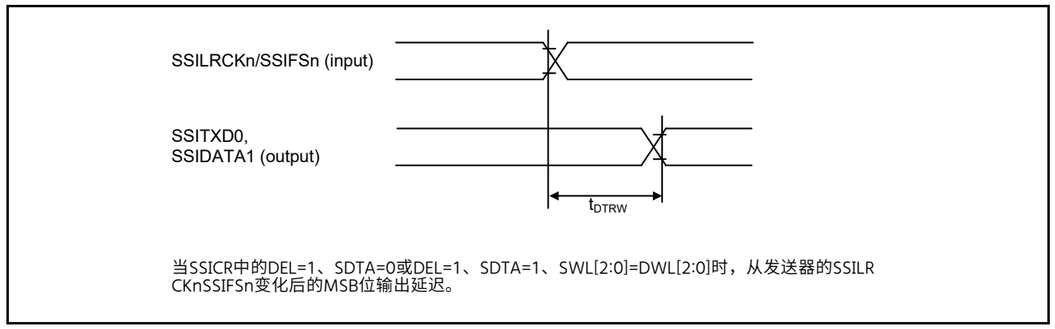


Figure 2.65 SSILRCKnSSIFSn改变后的SSIE数据输出延迟

2.3.15 SDMMC主机接口时序

Table 2.30 SDMMC主机接口信号时序
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
时钟占空比为50%。

Parameter		Symbol	Min	Max	Unit	Test conditions*1
SDCLK	时钟周期	T_{SDCYC}	20	-	ns	Figure 2.66
SDCLK	时钟高脉冲宽度	T_{SDWH}	6.5	-	ns	
SDCLK	时钟低脉冲宽度	T_{SDWL}	6.5	-	ns	
SDCLK	时钟上升时间	T_{SDLH}	-	3	ns	
SDCLK	时钟下降时间	T_{SDHL}	-	3	ns	
SDCMDSDDAT输出数据延迟		T_{SDODLY}	-6	5	ns	
SDCMDSDDAT输入数据设置		T_{SDIS}	4	-	ns	
SDCMDSDDAT输入数据保持		T_{SDIH}	2	-	ns	

注1.必须使用带有字母（“_A”、“_B”）的引脚来表示作为组附加在其名称后的组成员身份。为了

the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

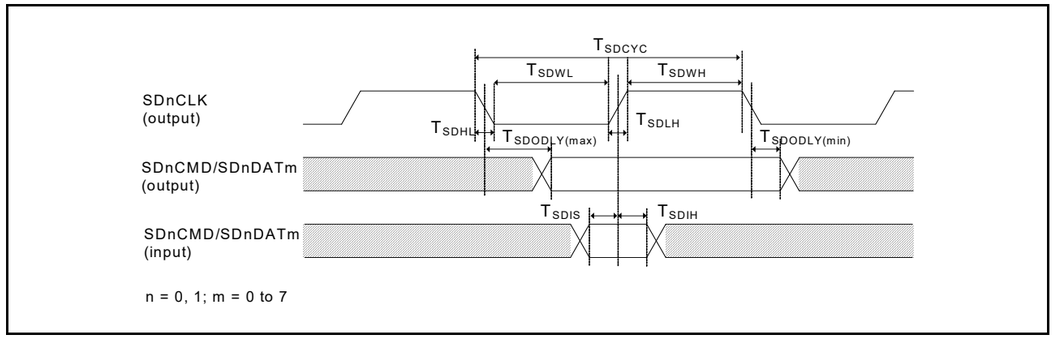


Figure 2.66 SD/MMC Host Interface signal timing

2.3.16 ETHERC Timing

Table 2.31 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the port drive capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions*3
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	-	ns	Figure 2.67 to Figure 2.70
	REF50CK frequency, typical 50 MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxxx*1 output delay	T_{co}	2.5	12.0	ns	
	RMII0_xxxx*2 setup time	T_{su}	3	-	ns	
	RMII0_xxxx*2 hold time	T_{hd}	1	-	ns	
	RMII0_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET0_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 2.71
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	-	ns	-
	ET0_TX_EN output delay	t_{TENd}	1	20	ns	Figure 2.72
	ET0_ETXD0 to ET0_ETXD3 output delay	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	-	ns	
	ET0_CRS hold time	t_{CRSh}	10	-	ns	
	ET0_COL setup time	t_{COLs}	10	-	ns	Figure 2.73
	ET0_COL hold time	t_{COLh}	10	-	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	-	ns	-
	ET0_RX_DV setup time	t_{RDVs}	10	-	ns	Figure 2.74
	ET0_RX_DV hold time	t_{RDVh}	10	-	ns	
	ET0_ERXD0 to ET0_ERXD3 setup time	t_{MRDs}	10	-	ns	
	ET0_ERXD0 to ET0_ERXD3 hold time	t_{MRDh}	10	-	ns	
	ET0_RX_ER setup time	t_{RERs}	10	-	ns	Figure 2.75
	ET0_RX_ER hold time	t_{RESh}	10	-	ns	
	ET0_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 2.76

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0.
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER.

SDMMC主机接口，测量每组电气特性的交流部分。

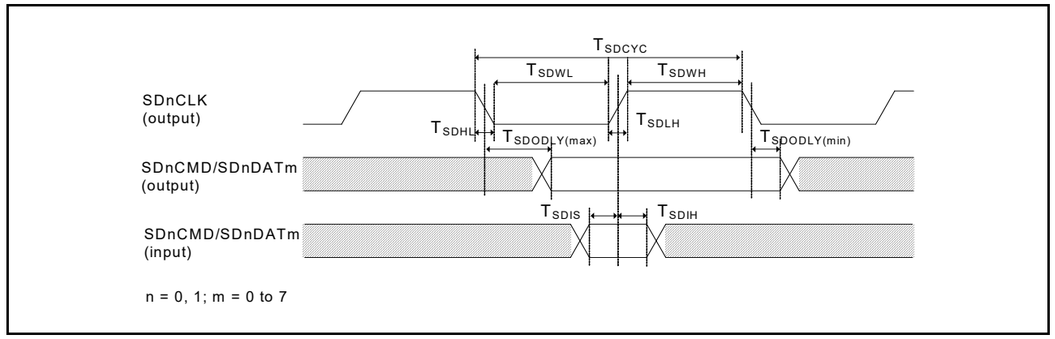


Figure 2.66 SDMMC主机接口信号时序

2.3.16 ETHERC Timing

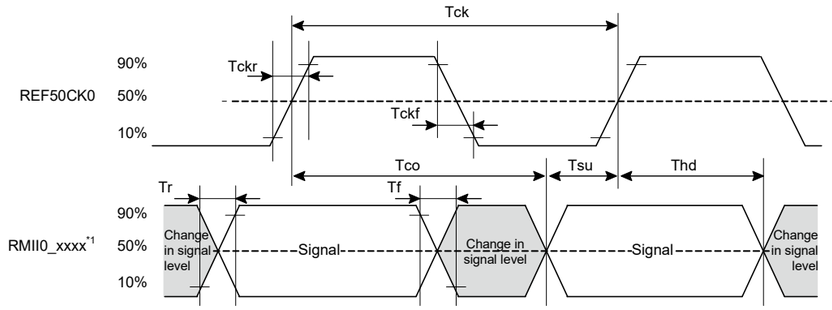
Table 2.31 ETHERC timing

条件：ETHERC(RMII)：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：
ET0_MDC, ET0_MDIO.
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
ETHERC(MII)：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	Test conditions*3
ETHERC (RMII)	REF50CK循环时间	T_{ck}	20	-	ns	图2.67至 Figure 2.70
	REF50CK频率，典型值50MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxxx*1输出延迟	T_{co}	2.5	12.0	ns	
	RMII0_xxxx*2建立时间	T_{su}	3	-	ns	
	RMII0_xxxx*2保持时间	T_{hd}	1	-	ns	
	RMII0_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET0_WOL输出延迟	t_{WOLd}	1	23.5	ns	Figure 2.71
ETHERC (MII)	ET0_TX_CLK周期时间	t_{Tcyc}	40	-	ns	-
	ET0_TX_EN输出延迟	t_{TENd}	1	20	ns	Figure 2.72
	ET0_ETXD0到ET0_ETXD3输出延迟	t_{MTDd}	1	20	ns	
	ET0_CRS建立时间	t_{CRSs}	10	-	ns	
	ET0_CRS保持时间	t_{CRSh}	10	-	ns	
	ET0_COL建立时间	t_{COLs}	10	-	ns	Figure 2.73
	ET0_COL保持时间	t_{COLh}	10	-	ns	
	ET0_RX_CLK周期时间	t_{TRcyc}	40	-	ns	-
	ET0_RX_DV建立时间	t_{RDVs}	10	-	ns	Figure 2.74
	ET0_RX_DV保持时间	t_{RDVh}	10	-	ns	
	ET0_ERXD0到ET0_ERXD3建立时间	t_{MRDs}	10	-	ns	
	ET0_ERXD0到ET0_ERXD3保持时间	t_{MRDh}	10	-	ns	
	ET0_RX_ER建立时间	t_{RERs}	10	-	ns	Figure 2.75
	ET0_RX_ER保持时间	t_{RESh}	10	-	ns	
	ET0_WOL输出延迟	t_{WOLd}	1	23.5	ns	Figure 2.76

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0.
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER.

Note 3. The following pins, must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group. REF50CK0_A, REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B



Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Figure 2.67 REF50CK0 and RMII signal timing

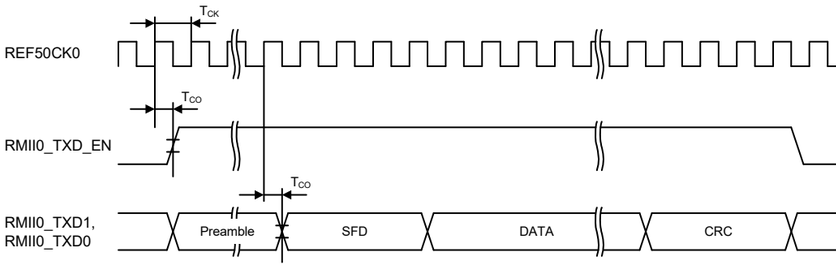


Figure 2.68 RMII transmission timing

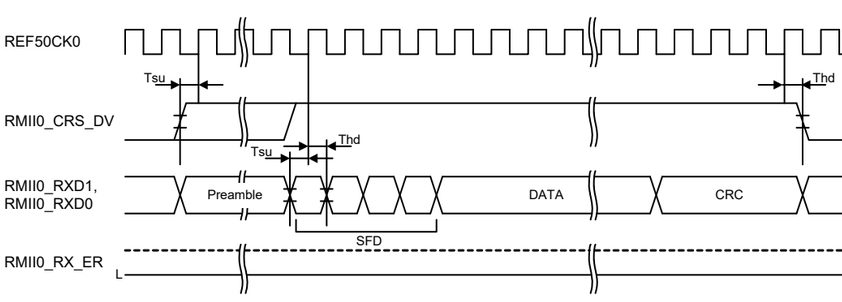
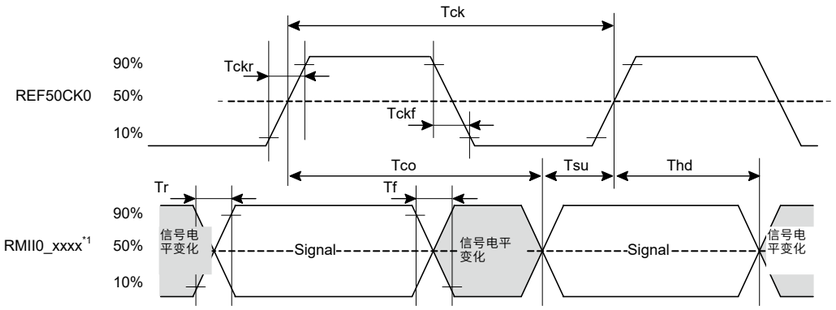


Figure 2.69 RMII reception timing in normal operation

Note 3. 以下管脚必须使用带有字母（“_A”、“_B”）的管脚来表示作为组附加到其名称的组成员身份。对于ETHERC(RMII)主机接口，测量每组的电气特性的交流部分。REF50CK0_A、REF50CK0_B、RMII0_xxxx_A、RMII0_xxxx_B



Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Figure 2.67 REF50CK0和RMII信号时序

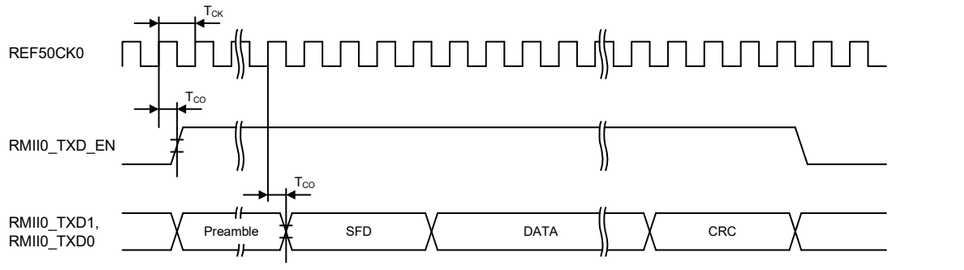


Figure 2.68 RMII传输时序

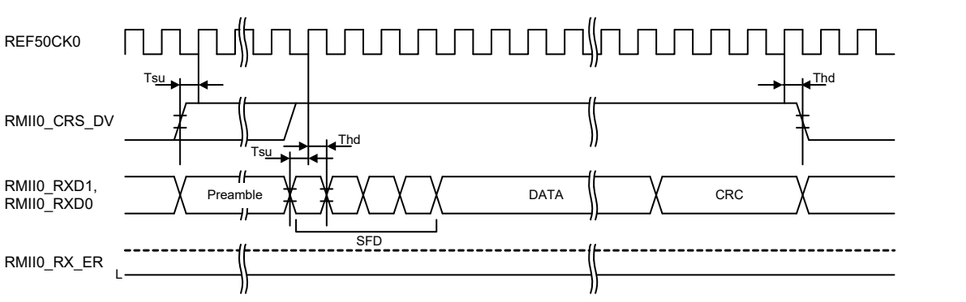


Figure 2.69 正常操作中的RMII接收时序

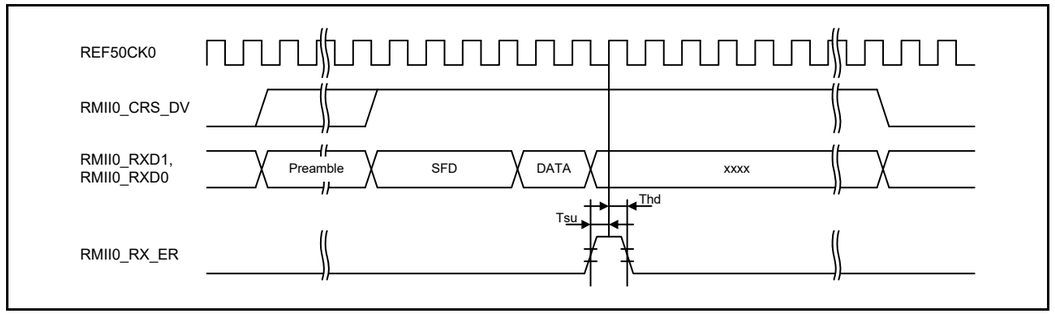


Figure 2.70 RMII reception timing when an error occurs

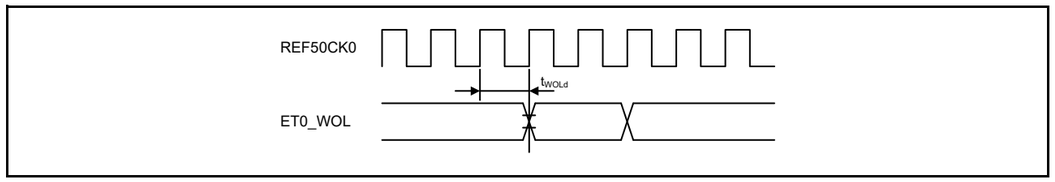


Figure 2.71 WOL output timing for RMII

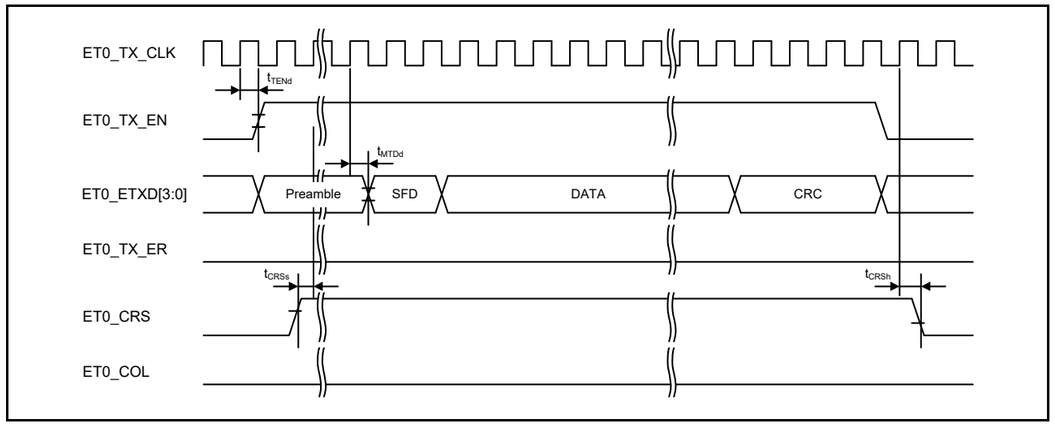


Figure 2.72 MII transmission timing in normal operation

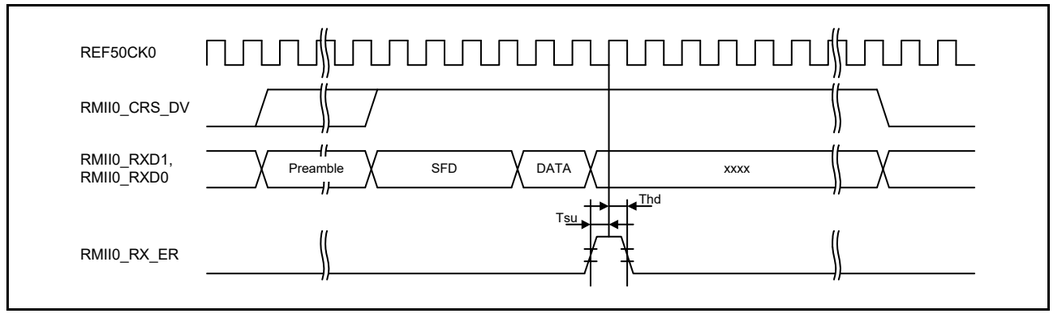


Figure 2.70 发生错误时的RMII接收时序

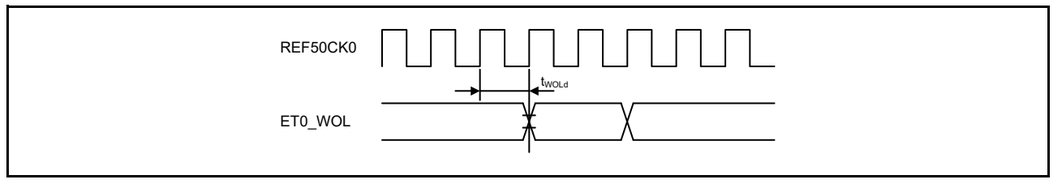


Figure 2.71 RMII的WOL输出时序

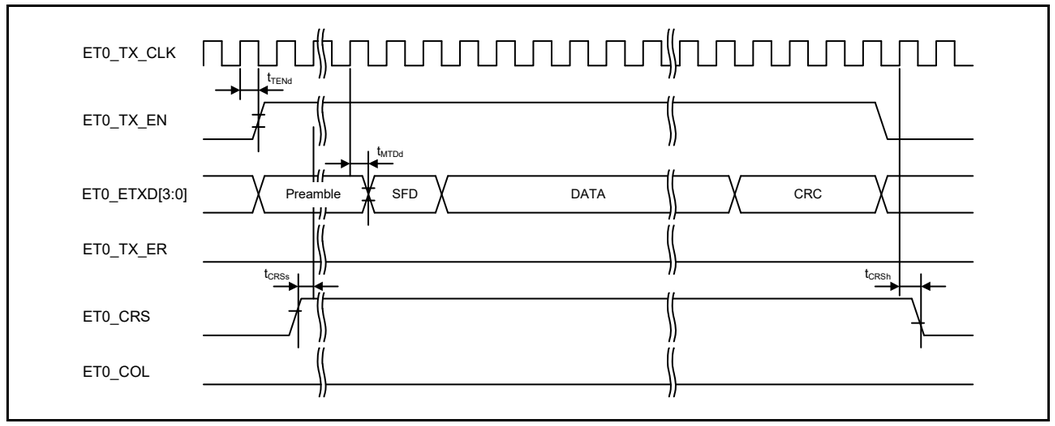


Figure 2.72 正常操作中的MII传输时序

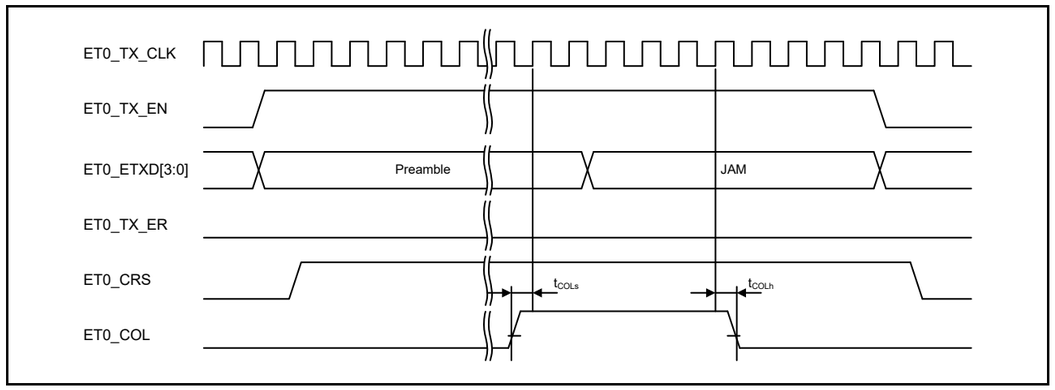


Figure 2.73 MII transmission timing when a conflict occurs

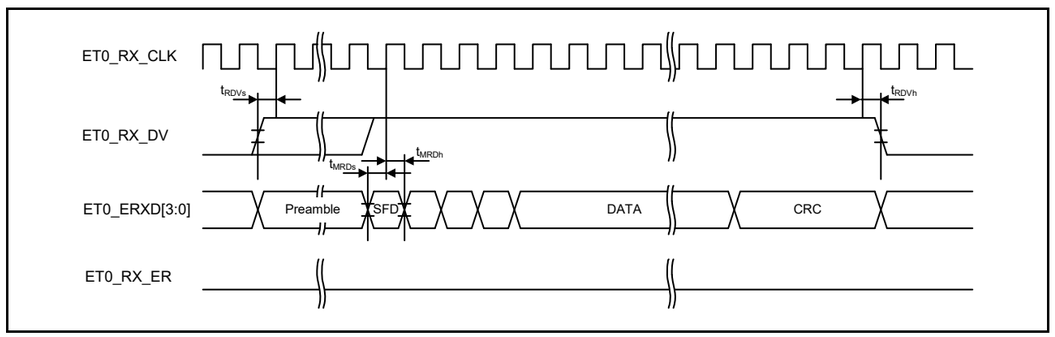


Figure 2.74 MII reception timing in normal operation

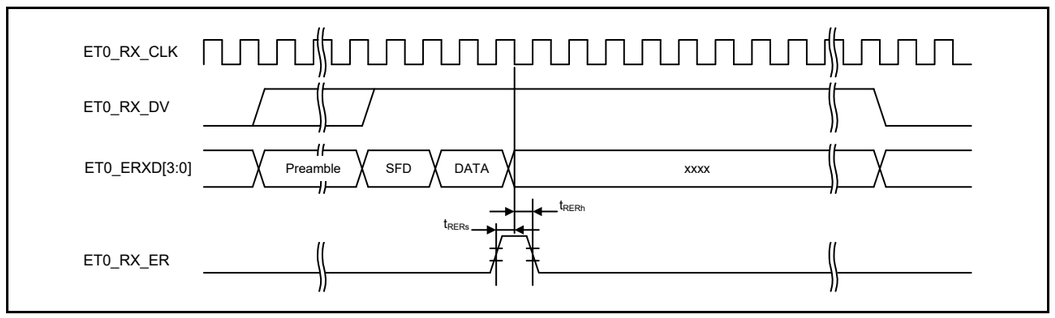


Figure 2.75 MII reception timing when an error occurs

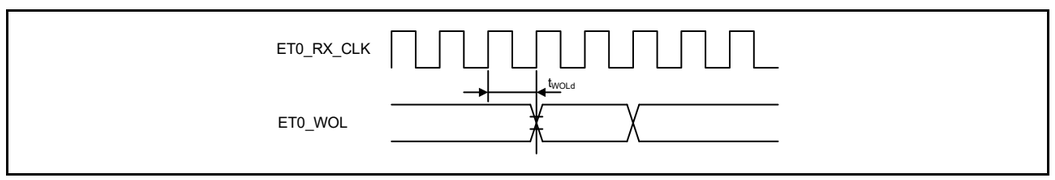


Figure 2.76 WOL output timing for MII

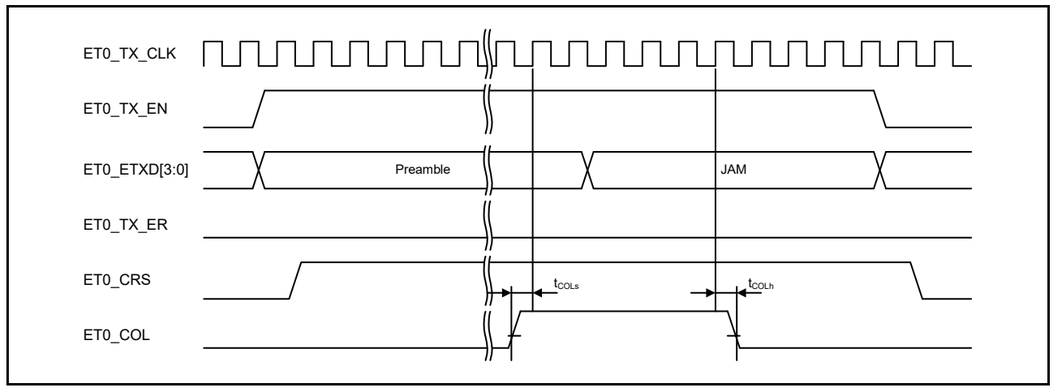


Figure 2.73 发生冲突时的MII传输时序

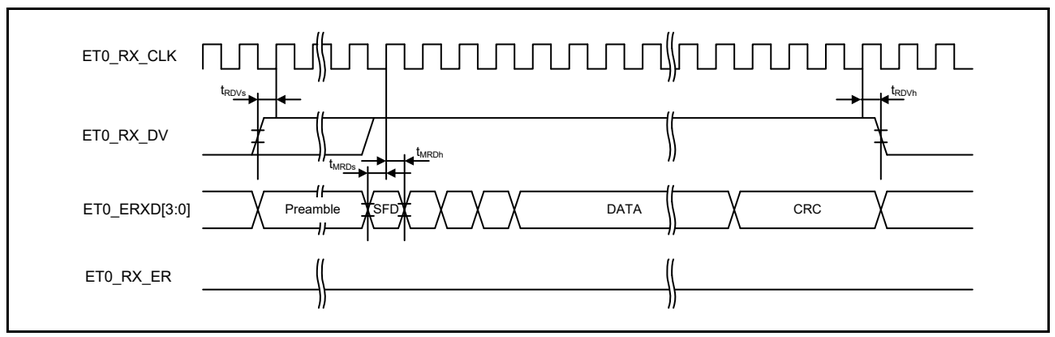


Figure 2.74 正常操作中的MII接收时序

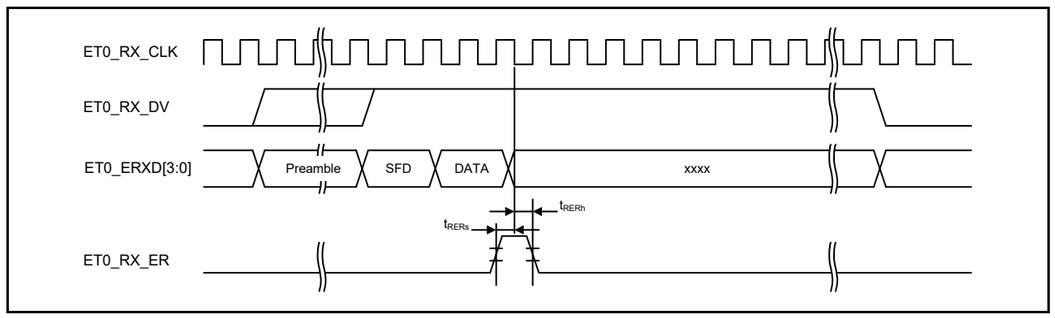


Figure 2.75 发生错误时的MII接收时序

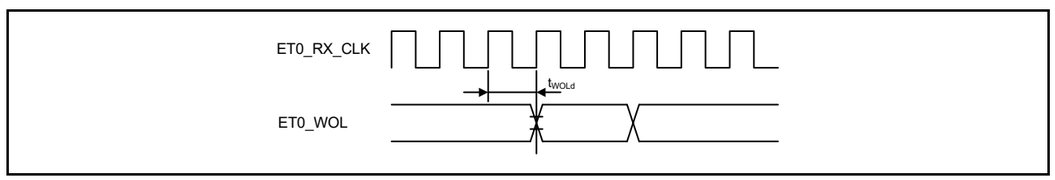


Figure 2.76 MII的WOL输出时序

2.3.17 PDC Timing

Table 2.32 PDC timing
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Parameter		Symbol	Min	Max	Unit	Test conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	-	ns	Figure 2.77
	PIXCLK input high pulse width	t_{PIXH}	10	-	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	-	ns	
	PIXCLK rise time	t_{PIXr}	-	5	ns	
	PIXCLK fall time	t_{PIXf}	-	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 2.78
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO rise time	t_{PCKr}	-	5	ns	
	PCKO fall time	t_{PCKf}	-	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	-	ns	Figure 2.79
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	-	ns	
	PIXD input setup time	t_{PIXDS}	10	-	ns	
	PIXD input hold time	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

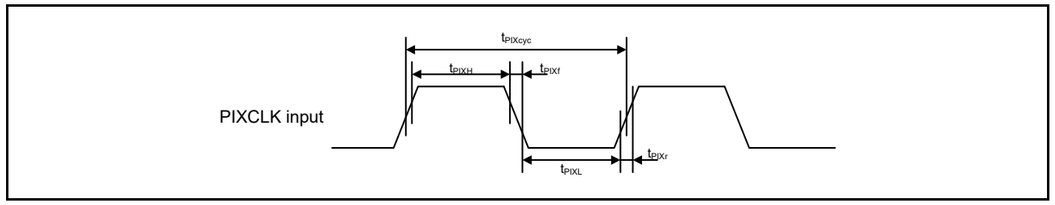


Figure 2.77 PDC input clock timing

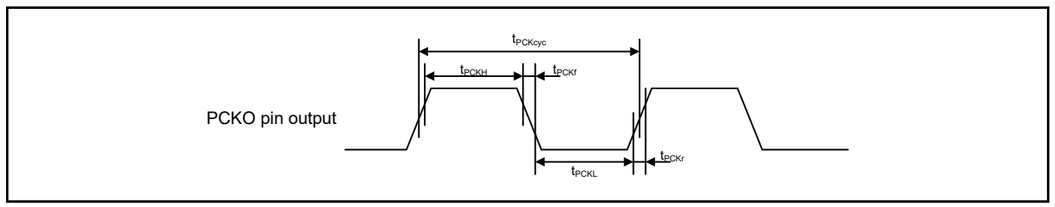


Figure 2.78 PDC output clock timing

2.3.17 PDC Timing

Table 2.32 PDC timing
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF

Parameter		Symbol	Min	Max	Unit	测试条件
PDC	PIXCLK输入周期时间	t_{PIXcyc}	37	-	ns	Figure 2.77
	PIXCLK输入高脉冲宽度	t_{PIXH}	10	-	ns	
	PIXCLK输入低脉冲宽度	t_{PIXL}	10	-	ns	
	PIXCLK上升时间	t_{PIXr}	-	5	ns	
	PIXCLK下降时间	t_{PIXf}	-	5	ns	
	PCKO输出循环时间	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 2.78
	PCKO输出高脉冲宽度	t_{PCKH}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO输出低脉冲宽度	t_{PCKL}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO上升时间	t_{PCKr}	-	5	ns	
	PCKO下降时间	t_{PCKf}	-	5	ns	
	VSYNVHSYNC输入建立时间	t_{SYNCS}	10	-	ns	Figure 2.79
	VSYNVHSYNC输入保持时间	t_{SYNCH}	5	-	ns	
	PIXD输入建立时间	t_{PIXDS}	10	-	ns	
	PIXD输入保持时间	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

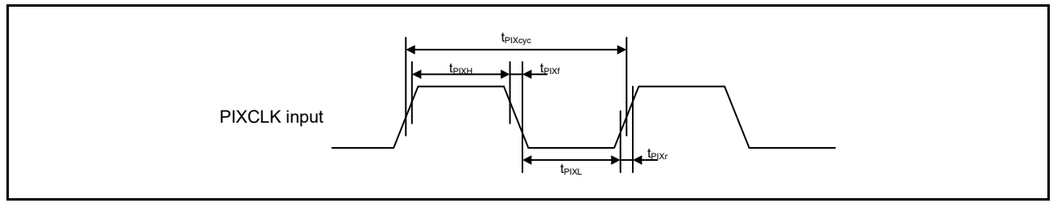


Figure 2.77 PDC输入时钟时序

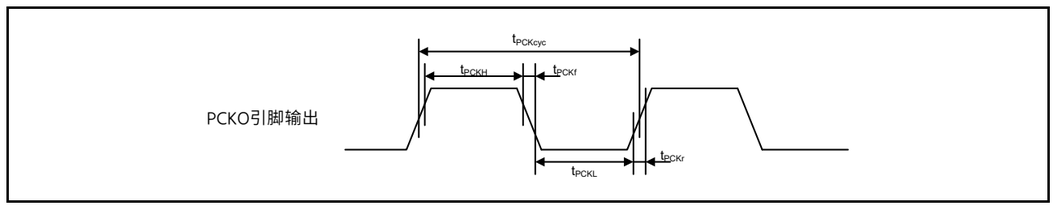


Figure 2.78 PDC输出时钟时序

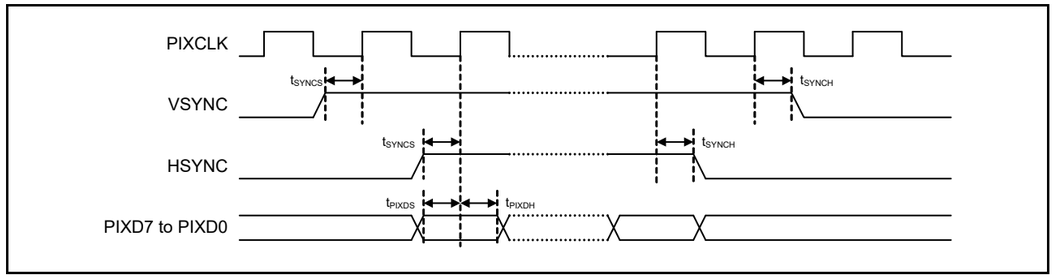


Figure 2.79 PDC AC timing

2.3.18 GLCDC Timing

Table 2.33 GLCDC timing
Conditions:
LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
LCD_EXTCLK input clock frequency		t_{Ecyc}	-	-	60*1	MHz	Figure 2.80
LCD_EXTCLK input clock low pulse width		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK input clock high pulse width		t_{WH}	0.45	-	0.55		
LCD_CLK output clock frequency		t_{Lcyc}	-	-	60*1	MHz	Figure 2.81
LCD_CLK output clock low pulse width		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 2.81
LCD_CLK output clock high pulse width		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 2.81
LCD data output delay timing	_A or _B combinations*2	t_{DD}	-3.5	-	4	ns	Figure 2.82
	_A and _B combinations*3		-5.0	-	5.5		

Note 1. Parallel RGB888, 666,565: Maximum 54 MHz
Serial RGB888: Maximum 60 MHz (4x speed)
Note 2. Use pins that have a letter appended to their names, for instance, “_A” or “_B”, to indicate
Note 3. Pins of group “_A” and “_B” combinations are used.

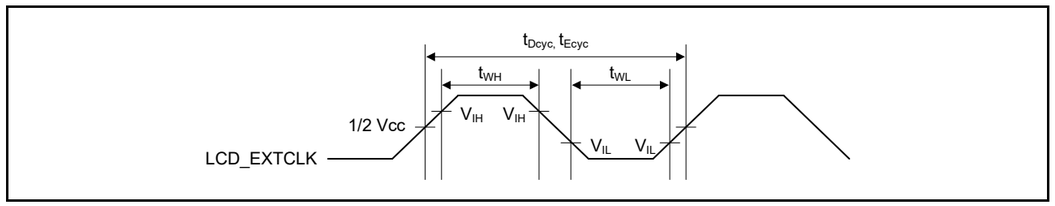


Figure 2.80 LCD_EXTCLK clock input timing

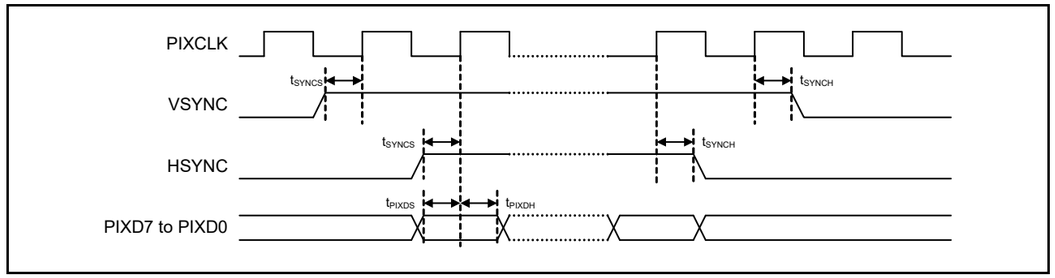


Figure 2.79 PDC交流正时

2.3.18 GLCDC Timing

Table 2.33 GLCDC timing
Conditions:
LCD_CLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
LCD_DATA：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
LCD_EXTCLK输入时钟频率		t_{Ecyc}	-	-	60*1	MHz	Figure 2.80
LCD_EXTCLK输入时钟低脉冲宽度		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK输入时钟高脉冲宽度		t_{WH}	0.45	-	0.55		
LCD_CLK输出时钟频率		t_{Lcyc}	-	-	60*1	MHz	Figure 2.81
LCD_CLK输出时钟低脉冲宽度		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 2.81
LCD_CLK输出时钟高脉冲宽度		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 2.81
LCD数据输出延迟时序	_A or _B combinations*2	t_{DD}	-3.5	-	4	ns	Figure 2.82
	_A and _B combinations*3		-5.0	-	5.5		

Note 1. 并行RGB888、666 565：最大54MHz串行RG
B888：最大60MHz（4倍速）
Note 2. 使用名称后附有字母（例如“_A”或“_B”）的引脚来表示
Note 3. 使用组“_A”和“_B”组合的引脚。

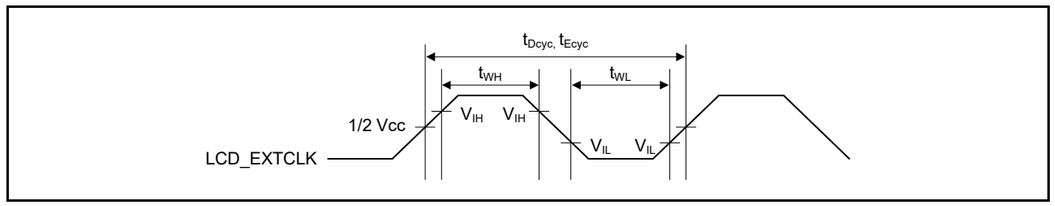


Figure 2.80 LCD_EXTCLK时钟输入时序

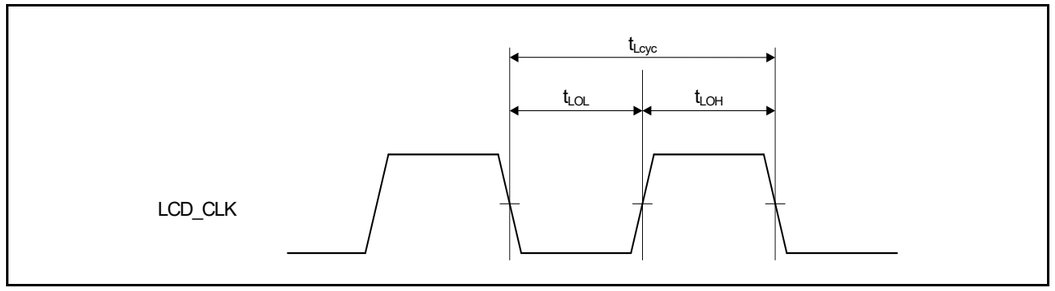


Figure 2.81 LCD_CLK clock output timing

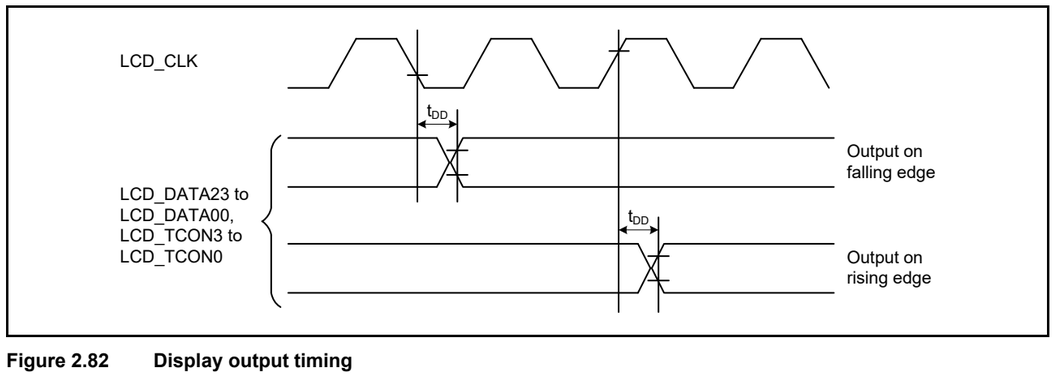


Figure 2.82 Display output timing

2.4 USB Characteristics

2.4.1 USBHS Timing

Table 2.34 USBHS low-speed characteristics for host only (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-	-
	Input low voltage	V_{IL}	-	-	0.8	V	-	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 2.83, Figure 2.84
	Rise time	t_{LR}	75	-	300	ns	-	
	Fall time	t_{LF}	75	-	300	ns	-	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR} / t_{LF}	-
Pull-up, Pull-down characteristics	USBHS_DP and USBHS_DM pull-down resistors (Host)	R_{pd}	14.25	-	24.80	kΩ	-	

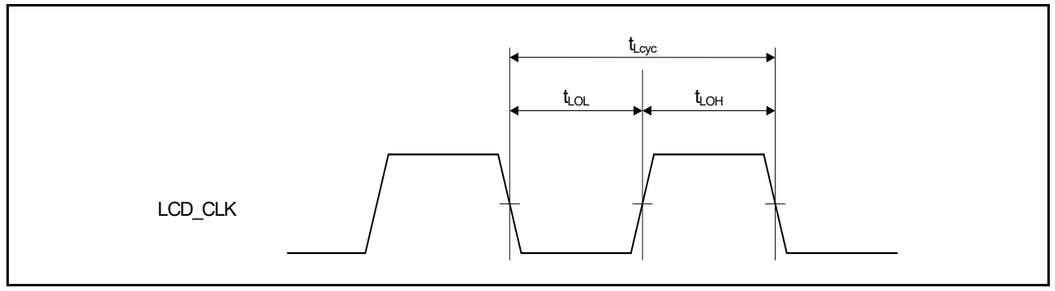


Figure 2.81 LCD_CLK时钟输出时序

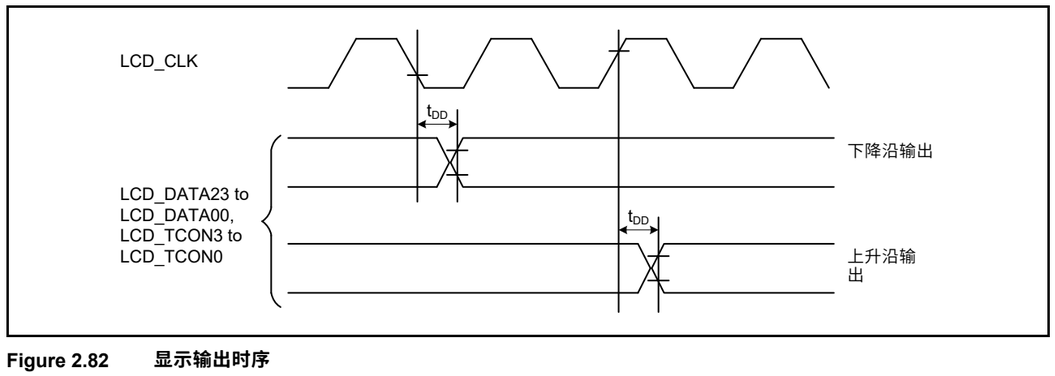


Figure 2.82 显示输出时序

2.4 USB特性

2.4.1 USBHS Timing

Table 2.34 仅主机的USBHS低速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件	
输入特性	输入高压	V_{IH}	2.0	-	-	V	-	-
	输入低电压	V_{IL}	-	-	0.8	V	-	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	差分共模范围	V_{CM}	0.8	-	2.5	V	-	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 2.83, Figure 2.84
	上升时间	t_{LR}	75	-	300	ns	-	
	秋季时间	t_{LF}	75	-	300	ns	-	
	上升下降时间比	t_{LR} / t_{LF}	80	-	125	%	t_{LR} / t_{LF}	-
Pull-up, Pull-down characteristics	USBHS_DP和USBHS_DM下拉电阻（主机）	R_{pd}	14.25	-	24.80	kΩ	-	

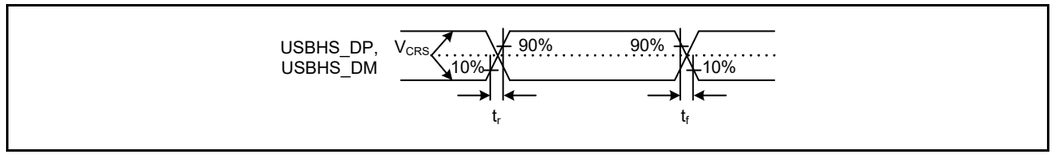


Figure 2.83 USBHS_DP and USBHS_DM output timing in low-speed mode

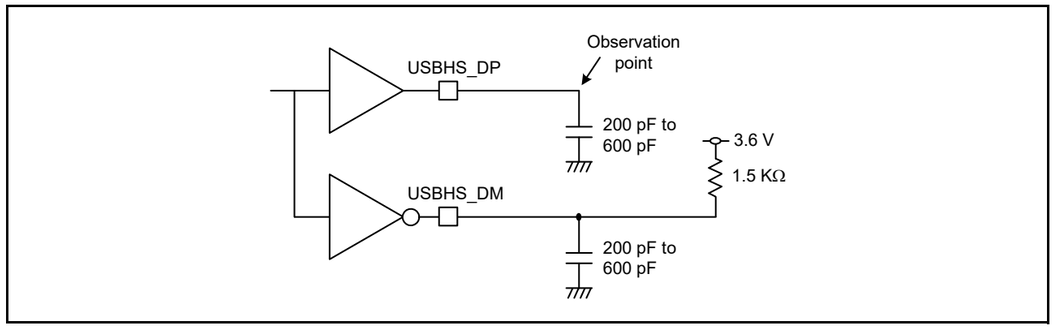


Figure 2.84 Test circuit in low-speed mode

Table 2.35 USBHS full-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-	-
	Input low voltage	V_{IL}	-	-	0.8	V	-	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 2.85, Figure 2.86
	Rise time	t_{LR}	4	-	20	ns	-	
	Fall time	t_{LF}	4	-	20	ns	-	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR} / t_{FF}	-
	Output resistance	Z_{DRV}	40.5	-	49.5	Ω	Rs Not used (PHYSET.REPSEL[1:0] = 01b and PHYSET. HSEB = 0)	
DC characteristics	USBHS_DM pull-up resistor (device)	R_{pu}	0.900	-	1.575	kΩ	During idle state	
			1.425	-	3.090	kΩ	During transmission and reception	
	USBHS_DP/USBHS_DM pull-down resistor (host)	R_{pd}	14.25	-	24.80	kΩ	-	

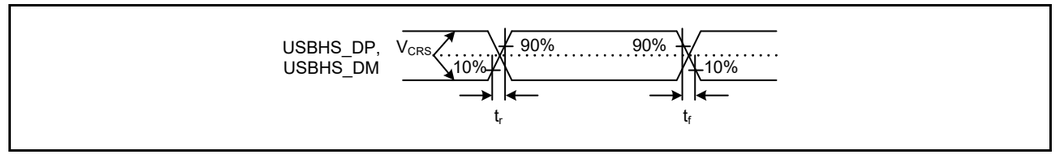


Figure 2.83 低速模式下的USBHS_DP和USBHS_DM输出时序

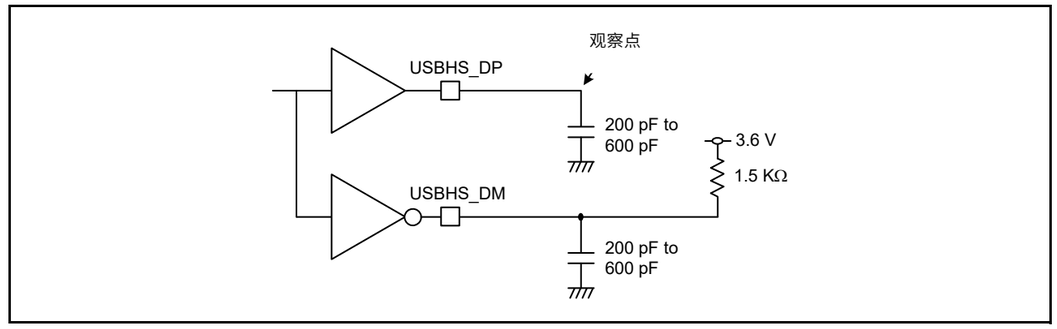


Figure 2.84 低速模式下的测试电路

Table 2.35 USBHS全速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件	
输入特性	输入高压	V_{IH}	2.0	-	-	V	-	-
	输入低电压	V_{IL}	-	-	0.8	V	-	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	差分共模范围	V_{CM}	0.8	-	2.5	V	-	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 2.85, Figure 2.86
	上升时间	t_{LR}	4	-	20	ns	-	
	秋季时间	t_{LF}	4	-	20	ns	-	
	上升下降时间比	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR} / t_{FF}	-
	输出电阻	Z_{DRV}	40.5	-	49.5	Ω	Rs未使用（PHYSET.REPSEL[1:0]=01b和PHYSET.HSEB=0）	
DC characteristics	USBHS_DM pull-up resistor (device)	R_{pu}	0.900	-	1.575	kΩ	空闲状态期间	
			1.425	-	3.090	kΩ	在发送和接收期间	
	USBHS_DP/USBHS_DM pull-down resistor (host)	R_{pd}	14.25	-	24.80	kΩ	-	

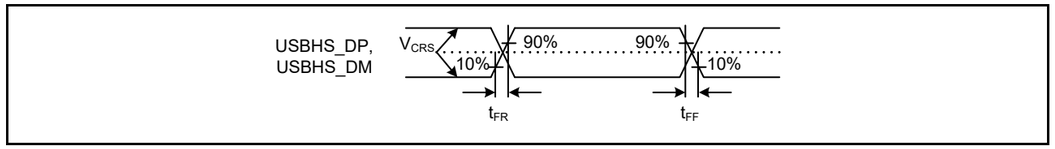


Figure 2.85 USBHS_DP and USBHS_DM output timing in full-speed mode

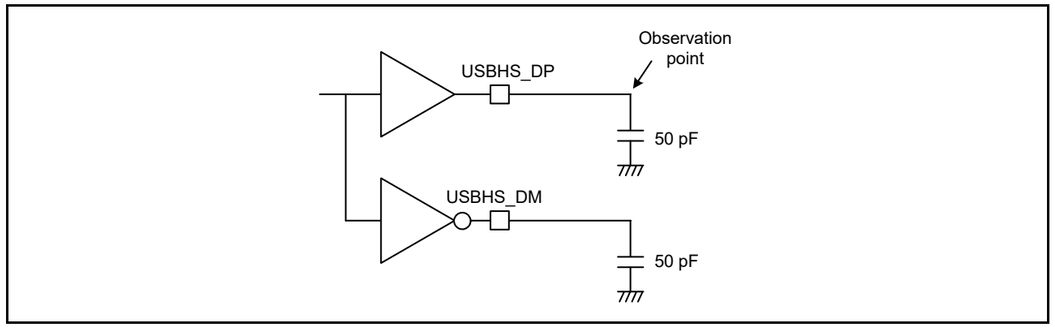


Figure 2.86 Test circuit in full-speed mode

Table 2.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Squelch detect sensitivity	V_{HSSQ}	100	-	150	mV	Figure 2.87
	Disconnect detect sensitivity	V_{HSDSC}	525	-	625	mV	Figure 2.88
	Common-mode voltage	V_{HSCM}	-50	-	500	mV	-
Output characteristics	Idle state	V_{HSOI}	-10.0	-	10	mV	-
	Output high voltage	V_{HSOH}	360	-	440	mV	
	Output low voltage	V_{HSOL}	-10.0	-	10	mV	
	Chirp J output voltage (difference)	V_{CHIRPJ}	700	-	1100	mV	
	Chirp K output voltage (difference)	V_{CHIRPK}	-900	-	-500	mV	
AC characteristics	Rise time	t_{HSR}	500	-	-	ps	Figure 2.89
	Fall time	t_{HSF}	500	-	-	ps	
	Output resistance	Z_{HSDRV}	40.5	-	49.5	Ω	-

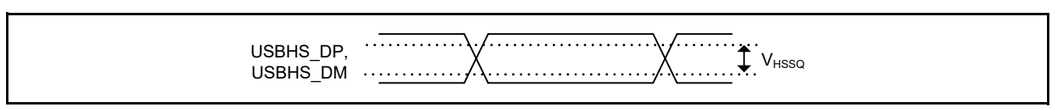


Figure 2.87 USBHS_DP and USBHS_DM squelch detect sensitivity in high-speed mode

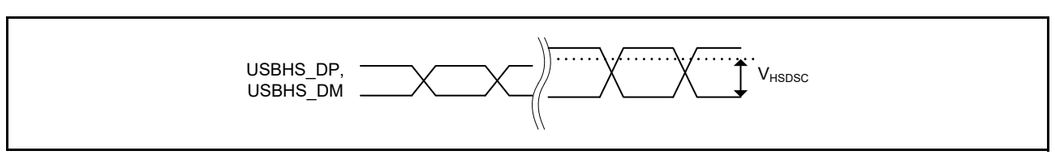


Figure 2.88 USBHS_DP and USBHS_DM disconnect detect sensitivity in high-speed mode

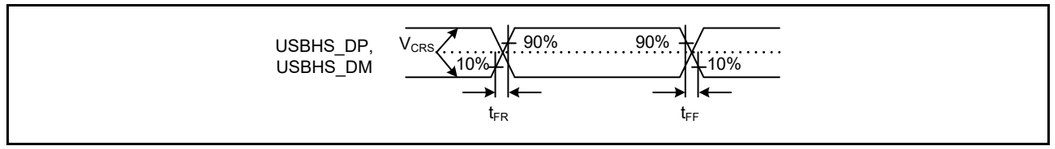


Figure 2.85 全速模式下的USBHS_DP和USBHS_DM输出时序

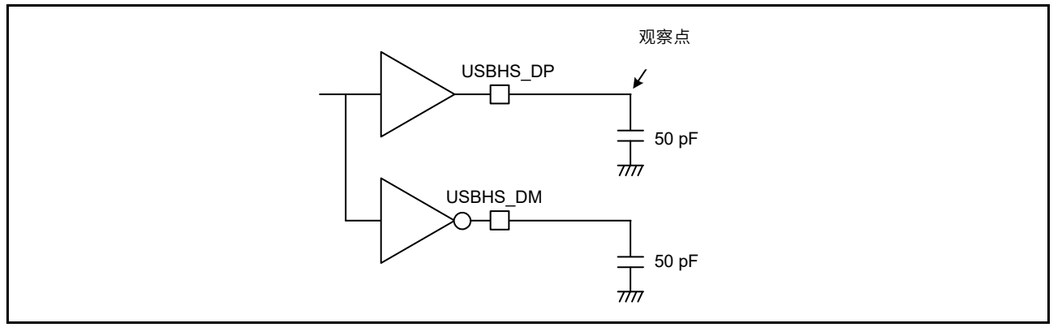


Figure 2.86 全速模式下的测试电路

Table 2.36 USBHS高速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	静噪检测灵敏度	V_{HSSQ}	100	-	150	mV	Figure 2.87
	断开检测灵敏度	V_{HSDSC}	525	-	625	mV	Figure 2.88
	Common-mode voltage	V_{HSCM}	-50	-	500	mV	-
输出特性	空闲状态	V_{HSOI}	-10.0	-	10	mV	-
	输出高压	V_{HSOH}	360	-	440	mV	
	输出低电压	V_{HSOL}	-10.0	-	10	mV	
	啁啾J输出电压（差值）	V_{CHIRPJ}	700	-	1100	mV	
	啁啾K输出电压（差）	V_{CHIRPK}	-900	-	-500	mV	
交流特性	上升时间	t_{HSR}	500	-	-	ps	Figure 2.89
	秋季时间	t_{HSF}	500	-	-	ps	
	输出电阻	Z_{HSDRV}	40.5	-	49.5	Ω	-

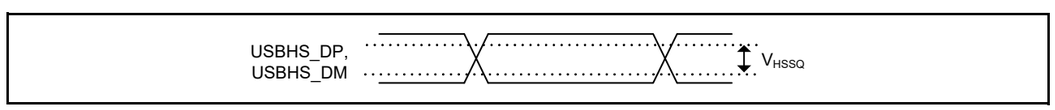


Figure 2.87 USBHS_DP和USBHS_DM静噪检测高速模式下的灵敏度

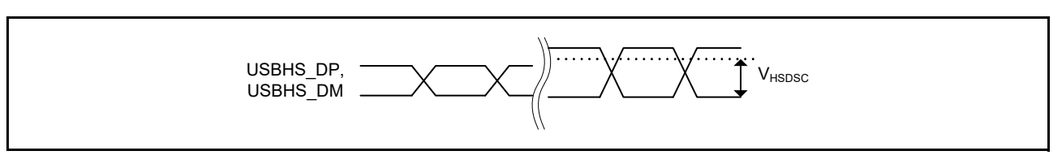


Figure 2.88 USBHS_DP和USBHS_DM断开检测高速模式下的灵敏度

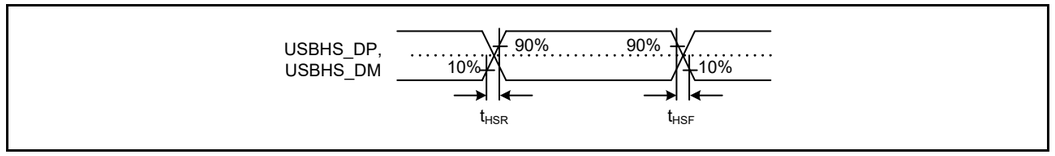


Figure 2.89 USBHS_DP and USBHS_DM output timing in high-speed mode

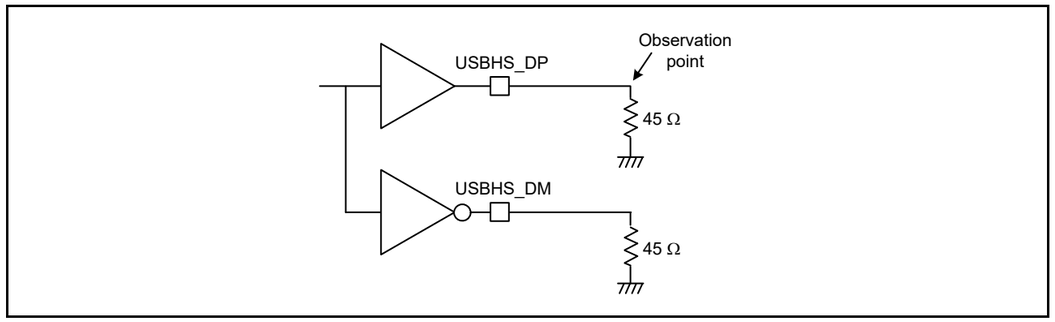


Figure 2.90 Test circuit in high-speed mode

Table 2.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	175	μA	-
	D- sink current	I_{DM_SINK}	25	175	μA	-
	DCD source current	I_{DP_SRC}	7	13	μA	-
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-
	D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.91
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}

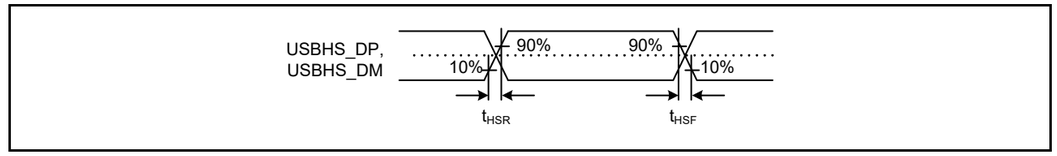


Figure 2.89 高速模式下的USBHS_DP和USBHS_DM输出时序

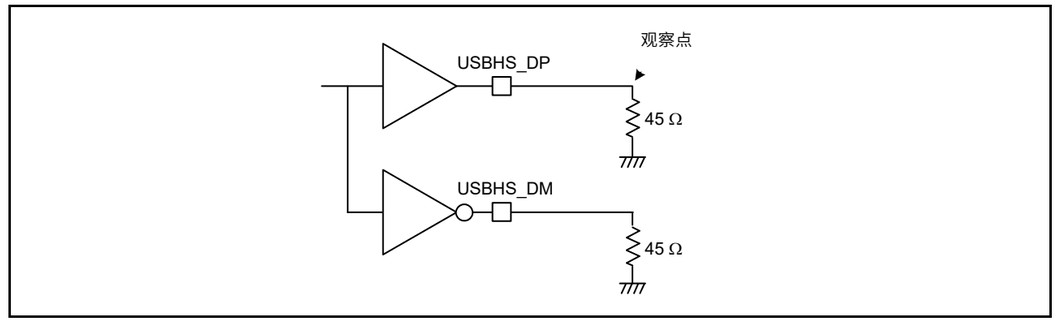


Figure 2.90 高速模式下的测试电路

Table 2.37 USBHS高速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Max	Unit	测试条件
电池充电 Specification	D+灌电流	I_{DP_SINK}	25	175	μA	-
	D- sink current	I_{DM_SINK}	25	175	μA	-
	DCD源电流	I_{DP_SRC}	7	13	μA	-
	数据检测电压	V_{DAT_REF}	0.25	0.4	V	-
	D+源电压	V_{DP_SRC}	0.5	0.7	V	输出电流=250μA
	D- source voltage	V_{DM_SRC}	0.5	0.7	V	输出电流=250μA

2.4.2 USBFS Timing

Table 2.38 仅主机的USBFS低速特性（USB_DP和USB_DM引脚特性）（1of2）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	-	-	V	-
	输入低电压	V_{IL}	-	-	0.8	V	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	-	2.5	V	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.91
	上升时间	t_{LR}	75	-	300	ns	
	秋季时间	t_{LF}	75	-	300	ns	
	上升下降时间比	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (2 of 2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

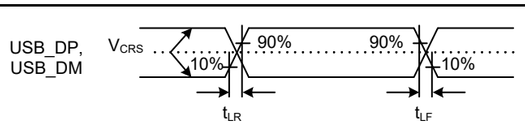


Figure 2.91 USB_DP and USB_DM output timing in low-speed mode

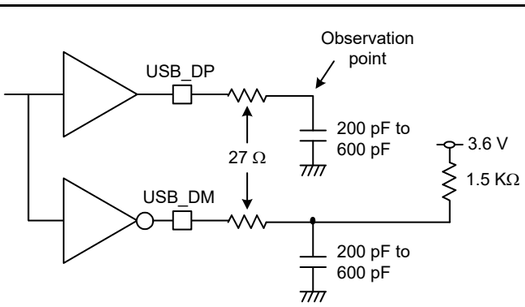


Figure 2.92 Test circuit in low-speed mode

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.93
	Rise time	t_{LR}	4	-	20	ns	
	Fall time	t_{LF}	4	-	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	-	1.575	kΩ	During idle state
			1.425	-	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

Table 2.38 仅主机的USBFS低速特性（USB_DP和USB_DM引脚特性）（2之2）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上拉和下拉特性	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	-	24.80	kΩ	-

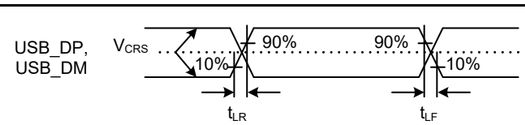


Figure 2.91 低速模式下的USB_DP和USB_DM输出时序

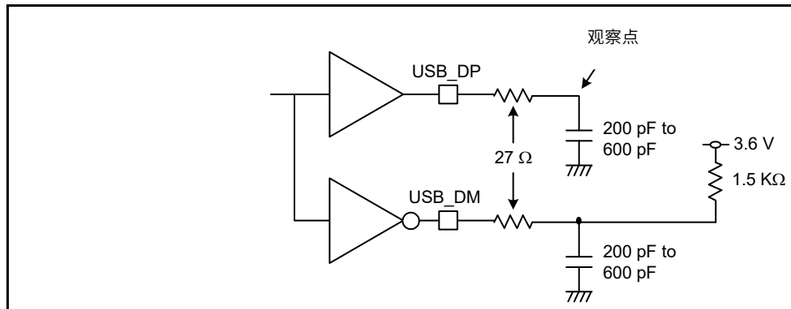


Figure 2.92 低速模式下的测试电路

Table 2.39 USBFS全速特性（USB_DP和USB_DM引脚特性）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	-	-	V	-
	输入低电压	V_{IL}	-	-	0.8	V	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	-	2.5	V	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.93
	上升时间	t_{LR}	4	-	20	ns	
	秋季时间	t_{LF}	4	-	20	ns	
	上升下降时间比	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	输出电阻	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
上拉和下拉特性	设备控制器模式下的DM上拉电阻	R_{pu}	0.900	-	1.575	kΩ	空闲状态期间
			1.425	-	3.090	kΩ	在发送和接收期间
	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	-	24.80	kΩ	-

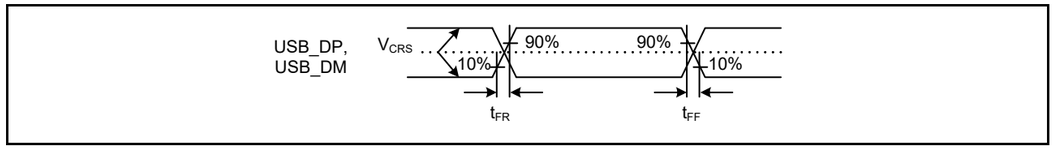


Figure 2.93 USB_DP and USB_DM output timing in full-speed mode

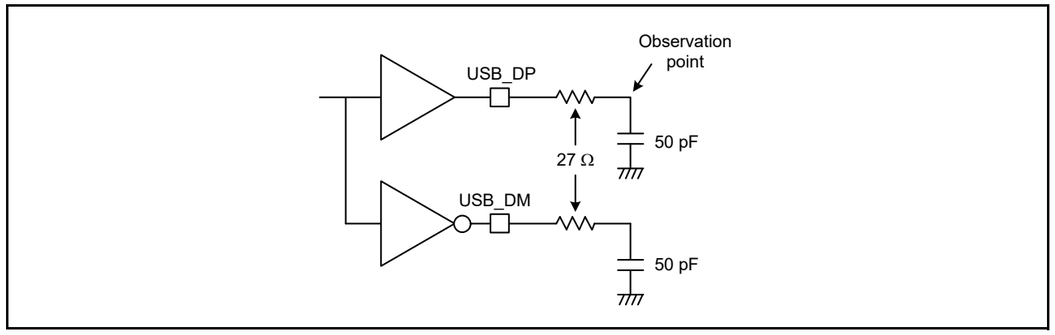


Figure 2.94 Test circuit in full-speed mode

2.5 ADC12 Characteristics

Table 2.40 A/D conversion characteristics for unit 0 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	μs	-
	Dynamic range		0.25	-	VREFH 0 - 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-

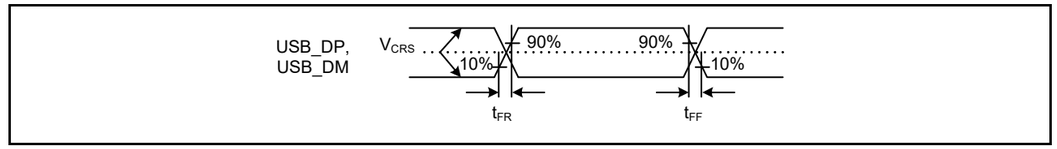


Figure 2.93 全速模式下的USB_DP和USB_DM输出时序

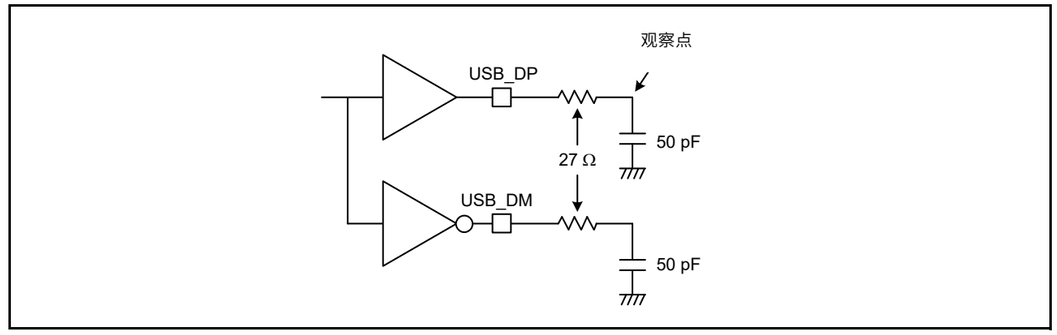


Figure 2.94 全速模式下的测试电路

2.5 ADC12 Characteristics

Table 2.40 单元0(1of2)的AD转换特性
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
Frequency			1	-	60	MHz	-
模拟输入电容			-	-	30	pF	-
量化误差			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
使用中的通道专用采样保持电路（AN000至AN002）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	通道采样 24种状态的专用采样保持电路 15种状态的采样
	偏移误差		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	绝对精度		-	±2.5	±5.5	LSB	-
	DNL微分非线性误差		-	±1.0	±2.0	LSB	-
	INL积分非线性误差		-	±1.5	±3.0	LSB	-
	采样保持电路的保持特性		-	-	20	μs	-
	动态范围		0.25	-	VREFH 0 - 0.25	V	-
未使用通道专用采样保持电路（AN000至AN002）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	μs	在16个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-

Table 2.40 A/D conversion characteristics for unit 0 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN003 to AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 2.41 A/D conversion characteristics for unit 1 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH - 0.25	V	-

Table 2.40 单元0(2of2)的AD转换特性
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
高精度通道（AN003至AN007）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	在11个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
普通精度通道（AN016至AN020）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.88 (0.667)*2	-	-	µs	在40个州进行抽样
	偏移误差		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	绝对精度		-	±2.0	±7.5	LSB	-
	DNL微分非线性误差		-	±0.5	±4.5	LSB	-
	INL积分非线性误差		-	±1.0	±5.5	LSB	-

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果访问发生在D转换，值可能不在指定范围内。
使用12位AD转换器时，不允许将端口0用作数字输出。
这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note 1. 转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。
Note 2. 括号中的值表示采样时间。

Table 2.41 单元1的AD转换特性（2个中的1个）
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
Frequency			1	-	60	MHz	-
模拟输入电容			-	-	30	pF	-
量化误差			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
使用中的通道专用采样保持电路（AN100至AN102）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	通道采样 24种状态的专用采样保持电路 15种状态的采样
	偏移误差		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	绝对精度		-	±2.5	±5.5	LSB	-
	DNL微分非线性误差		-	±1.0	±2.0	LSB	-
	INL积分非线性误差		-	±1.5	±3.0	LSB	-
	采样保持电路的保持特性		-	-	20	µs	-
	动态范围		0.25	-	VREFH - 0.25	V	-

Table 2.41 A/D conversion characteristics for unit 1 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN103, AN105 to AN107)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116 to AN119)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 2.42 A/D conversion characteristics for simultaneous using of channel-dedicated sample-and-hold circuits in unit0 and unit1
Conditions: PCLKC = 30/60 MHz

Parameter		Min	Typ	Max	Test conditions
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0	• PCLKC = 60 MHz • Sampling in 15 states
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5	• PCLKC = 30 MHz • Sampling in 7 states
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	

Table 2.41 单元1的AD转换特性（2个中的2个）
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
未使用通道专用采样保持电路（AN100至AN102）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗 Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
高精度通道（AN103、AN105至AN107）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗 Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	在11个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
普通精度通道（AN116至AN119）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗 Max.=1kΩ	0.88 (0.667)*2	-	-	µs	在40个州进行抽样
	偏移误差		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	绝对精度		-	±2.0	±7.5	LSB	-
	DNL微分非线性误差		-	±0.5	±4.5	LSB	-
	INL积分非线性误差		-	±1.0	±5.5	LSB	-

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果访问发生在D转换，值可能不在指定范围内。
使用12位AD转换器时，不允许将端口0用作数字输出。
这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note 1. 转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

Note 2. 括号中的值表示采样时间。

表2.42在unit0和unit1中同时使用通道专用采样保持电路的AD转换特性条件：PCLKC=3060MHz

Parameter		Min	Typ	Max	测试条件
启用连续采样功能的通道专用采样保持电路（AN000至AN002）	偏移误差	-	±1.5	±5.0	PCLKC=60MHz 15种状态采样
	Full-scale error	-	±2.5	±5.0	
	绝对精度	-	±4.0	±8.0	
启用连续采样功能的通道专用采样保持电路（AN100至AN102）	偏移误差	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	绝对精度	-	±4.0	±8.0	
启用连续采样功能的通道专用采样保持电路（AN000至AN002）	偏移误差	-	±1.5	±3.5	PCLKC=30MHz 7种状态采样
	Full-scale error	-	±1.5	±3.5	
	绝对精度	-	±3.0	±5.5	
启用连续采样功能的通道专用采样保持电路（AN100至AN102）	偏移误差	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	绝对精度	-	±3.0	±5.5	

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit0 and unit1, setting the ADSHMSR.SHMD bit to 1 is recommended.

Table 2.43 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	μs	-

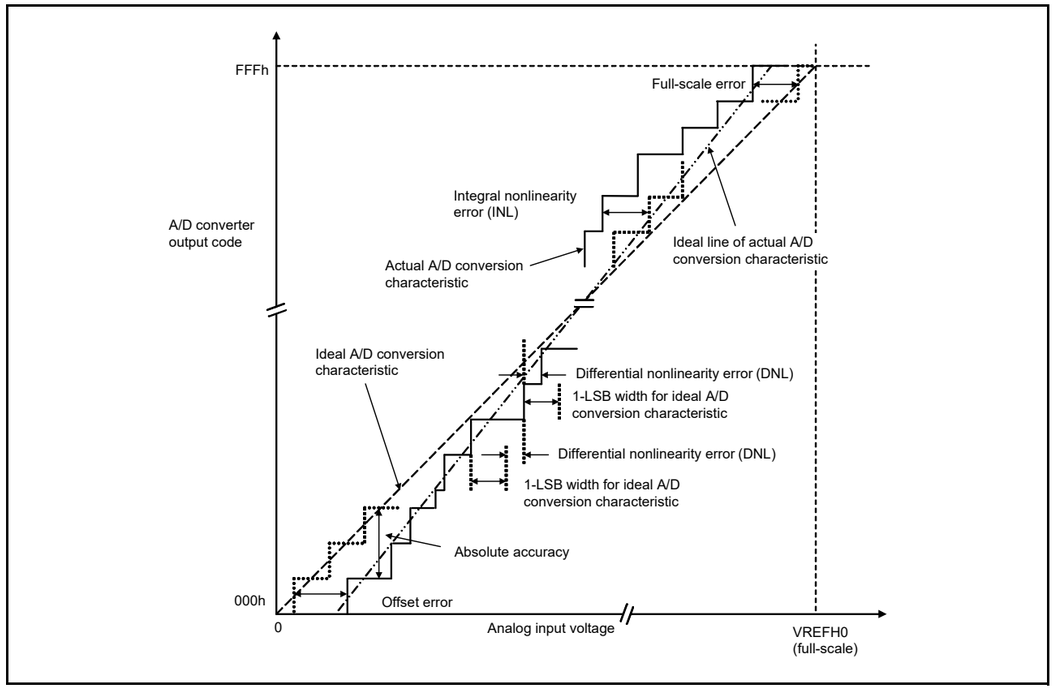


Figure 2.95 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Note: 在unit0和unit1中同时使用通道专用采样保持电路时，建议将ADSHMSR.SHMD位设置为1。

Table 2.43 AD内部参考电压特性

Parameter	Min	Typ	Max	Unit	测试条件
AD内部参考电压	1.13	1.18	1.23	V	-
采样时间	4.15	-	-	μs	-

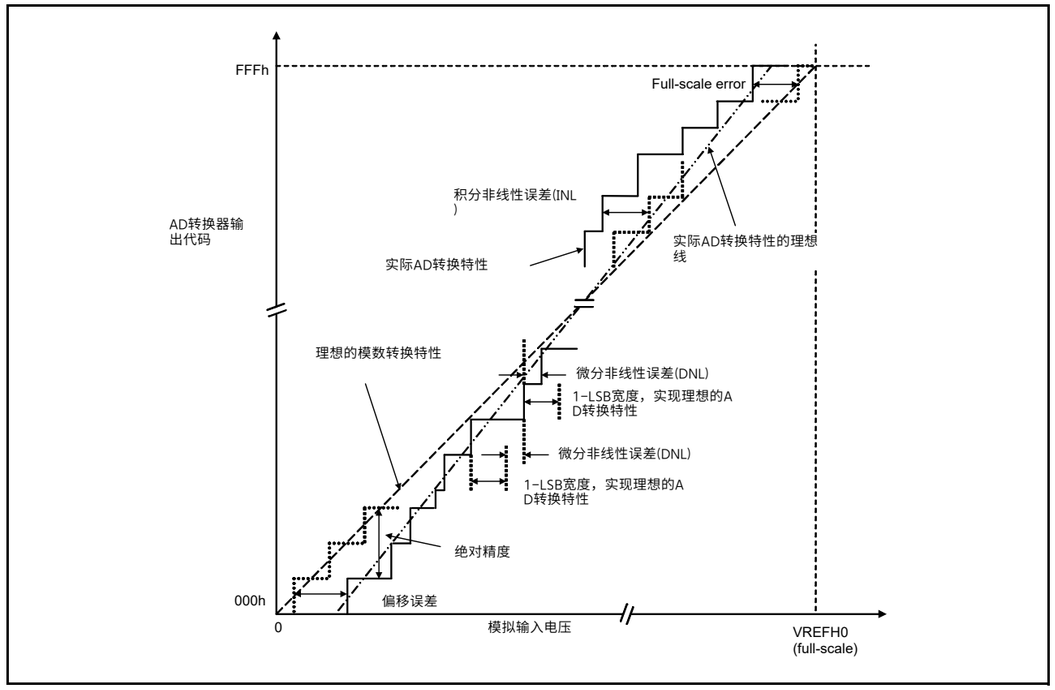


Figure 2.95 ADC12特征项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压可以满足基于理论模数转换特性输出等码的预期.例如，如果使用12位分辨率且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在003h到00Dh的范围内，尽管从理论上的AD转换特性可以预期输出码为008h。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.44 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
INL	-	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	-	±1.0	±2.0	LSB	-
Output impedance	-	8.5	-	kΩ	-
Conversion time	-	-	3.0	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	-	VREFH	V	-
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	µs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH - 0.2	V	-

2.7 TSN Characteristics

Table 2.45 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.46 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.96

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

2.6 DAC12 Characteristics

Table 2.44 DA转换特性

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	-	-	12	Bits	-
无输出放大器					
绝对精度	-	-	±24	LSB	阻性负载2MΩ
INL	-	±2.0	±8.0	LSB	阻性负载2MΩ
DNL	-	±1.0	±2.0	LSB	-
输出阻抗	-	8.5	-	kΩ	-
转换时间	-	-	3.0	µs	电阻负载2MΩ，电容负载20pF
输出电压范围	0	-	VREFH	V	-
带输出放大器					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
转换时间	-	-	4.0	µs	-
阻性负载	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
输出电压范围	0.2	-	VREFH - 0.2	V	-

2.7 TSN Characteristics

Table 2.45 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	-	-	±1.0	-	°C	-
温度斜率	-	-	4.0	-	mV/°C	-
输出电压（25°C时）	-	-	1.24	-	V	-
温度传感器启动时间	t_{START}	-	-	30	µs	-
采样时间	-	4.15	-	-	µs	-

2.8 OSC停止检测特性

Table 2.46 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	-	-	1	ms	Figure 2.96

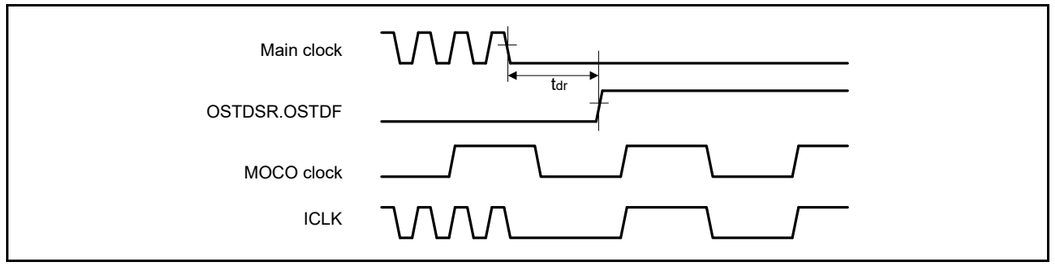


Figure 2.96 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.47 Power-on reset circuit and voltage detection circuit characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 2.97
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.98
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.99
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.100
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	-	4.5	-	ms	Figure 2.97
	LVD0 reset time		t_{LVD0}	-	0.51	-		Figure 2.98
	LVD1 reset time		t_{LVD1}	-	0.38	-		Figure 2.99
	LVD2 reset time		t_{LVD2}	-	0.38	-		Figure 2.100
Minimum VCC down time*1			t_{VOFF}	200	-	-	µs	Figure 2.97, Figure 2.98
Response delay			t_{det}	-	-	200	µs	Figure 2.97 to Figure 2.100
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	-	-	10	µs	Figure 2.99, Figure 2.100
Hysteresis width (LVD1 and LVD2)			V_{LVH}	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.

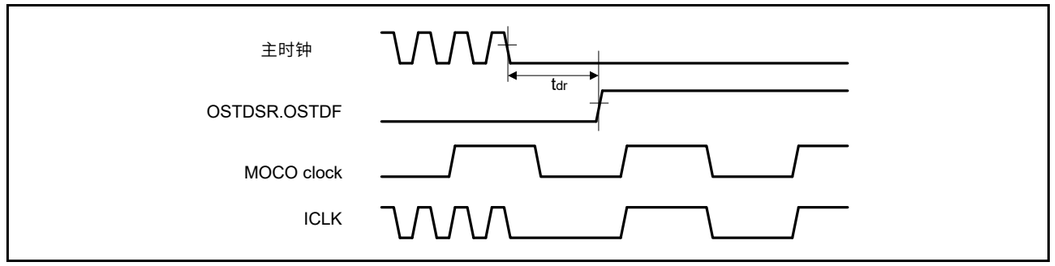


Figure 2.96 振荡停止检测时机

2.9 POR和LVD特性

Table 2.47 上电复位电路及电压检测电路特性

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 2.97
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	电压检测电路（LVD0）		V_{det0_1}	2.84	2.94	3.04		Figure 2.98
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	电压检测电路（LVD1）		V_{det1_1}	2.89	2.99	3.09		Figure 2.99
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	电压检测电路（LVD2）		V_{det2_1}	2.89	2.99	3.09		Figure 2.100
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
内部复位时间	上电复位时间		t_{POR}	-	4.5	-	ms	Figure 2.97
	LVD0复位时间		t_{LVD0}	-	0.51	-		Figure 2.98
	LVD1复位时间		t_{LVD1}	-	0.38	-		Figure 2.99
	LVD2复位时间		t_{LVD2}	-	0.38	-		Figure 2.100
最短VCC停机时间*1			t_{VOFF}	200	-	-	µs	Figure 2.97, Figure 2.98
响应延迟			t_{det}	-	-	200	µs	图2.97至 Figure 2.100
LVD操作稳定时间（启用LVD后）			$t_{d(E-A)}$	-	-	10	µs	Figure 2.99, Figure 2.100
迟滞宽度（LVD1和LVD2）			V_{LVH}	-	70	-	mV	

Note 1. 最小VCC停机时间表示VCC低于电压检测电平VPOR的最小值的时间，Vdet1和Vdet2用于POR和LVD。

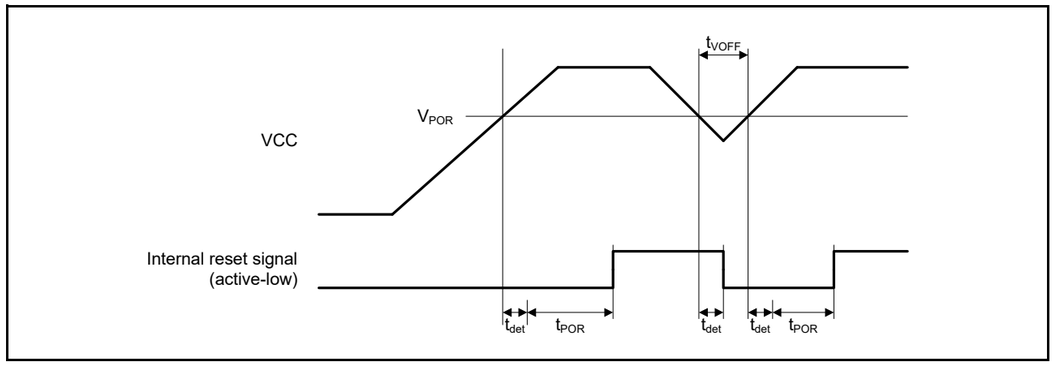


Figure 2.97 Power-on reset timing

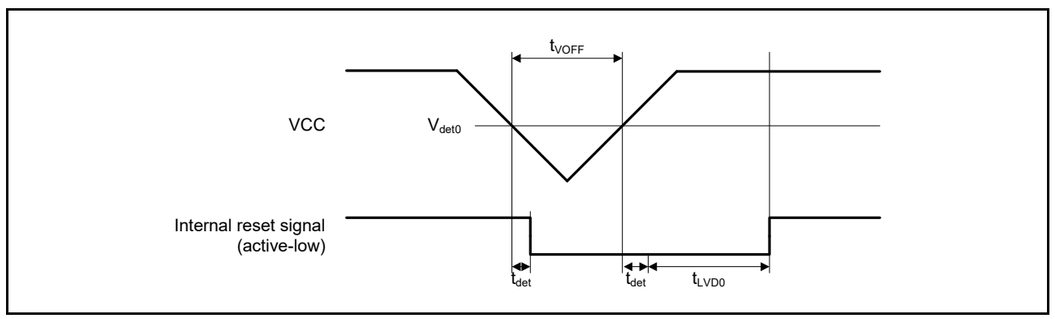


Figure 2.98 Voltage detection circuit timing (V_{det0})

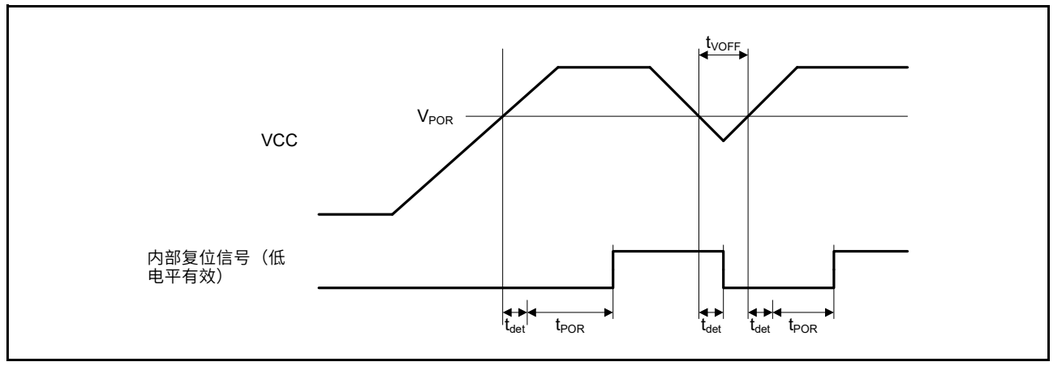


Figure 2.97 上电复位时序

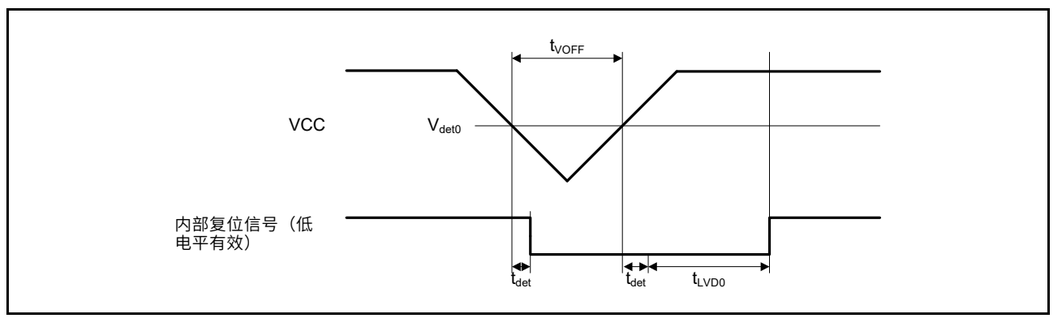


Figure 2.98 电压检测电路时序（Vdet0）

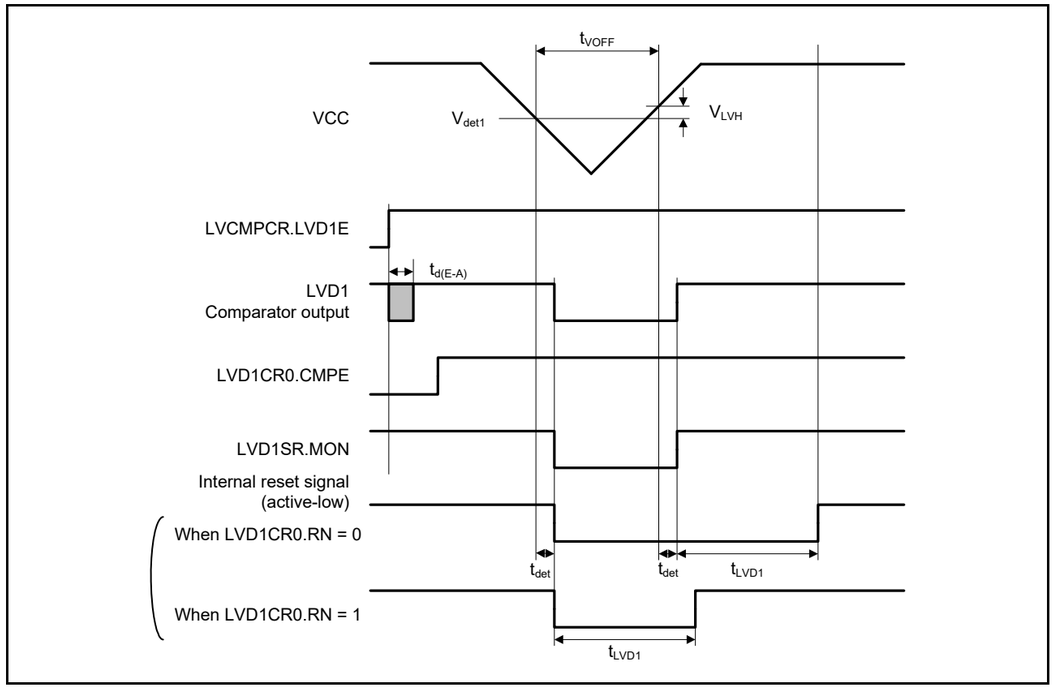


Figure 2.99 Voltage detection circuit timing (V_{det1})

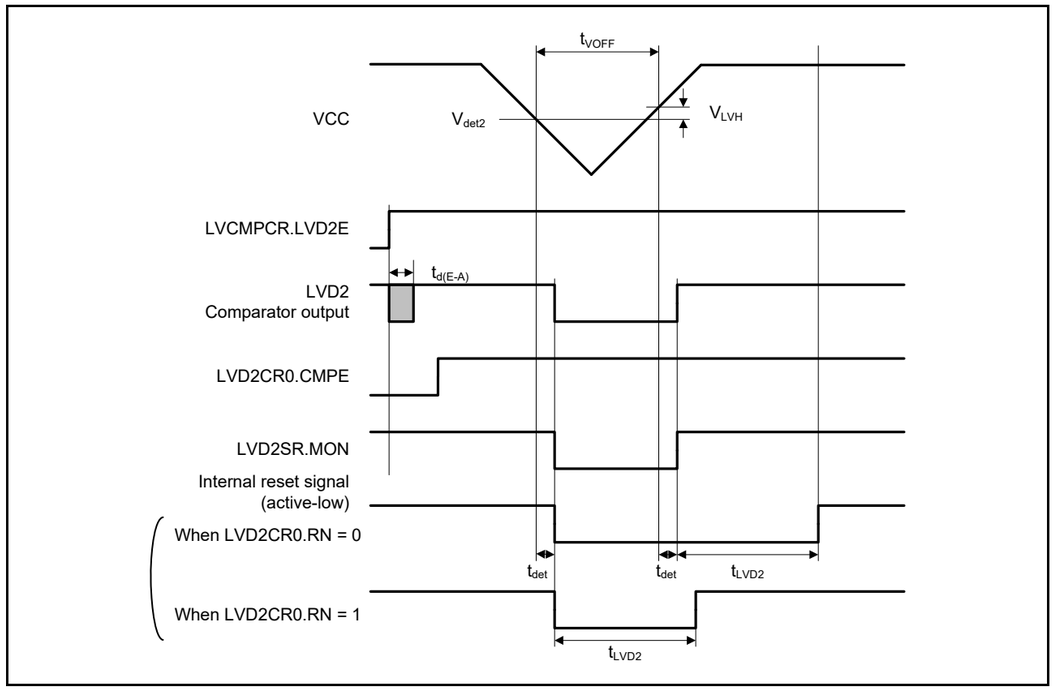


Figure 2.100 Voltage detection circuit timing (V_{det2})

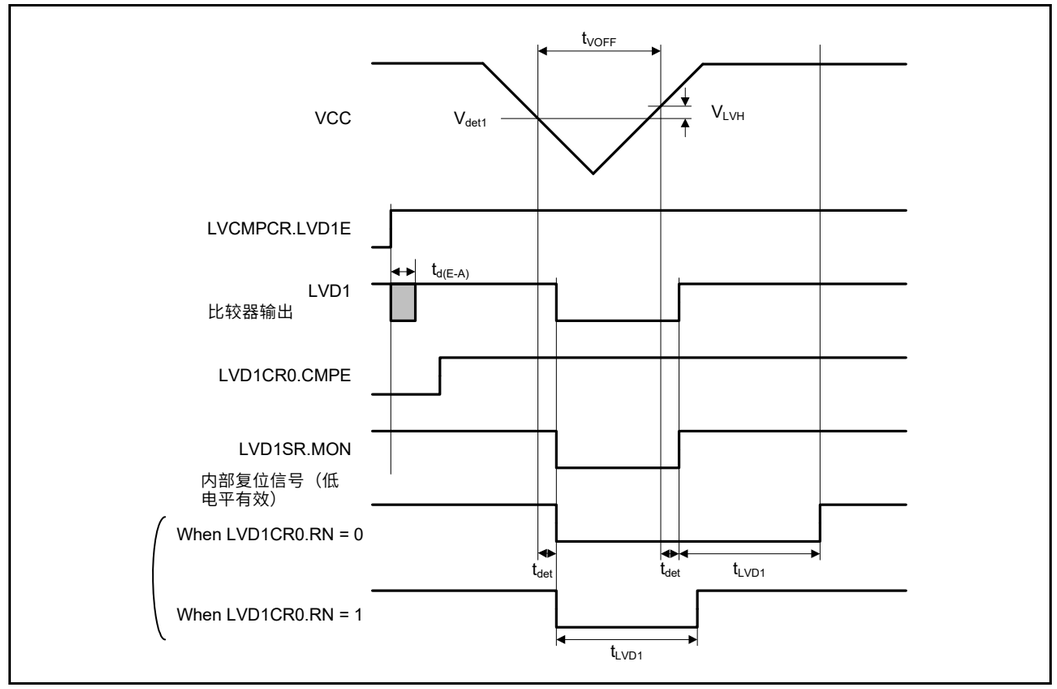


Figure 2.99 电压检测电路时序（Vdet1）

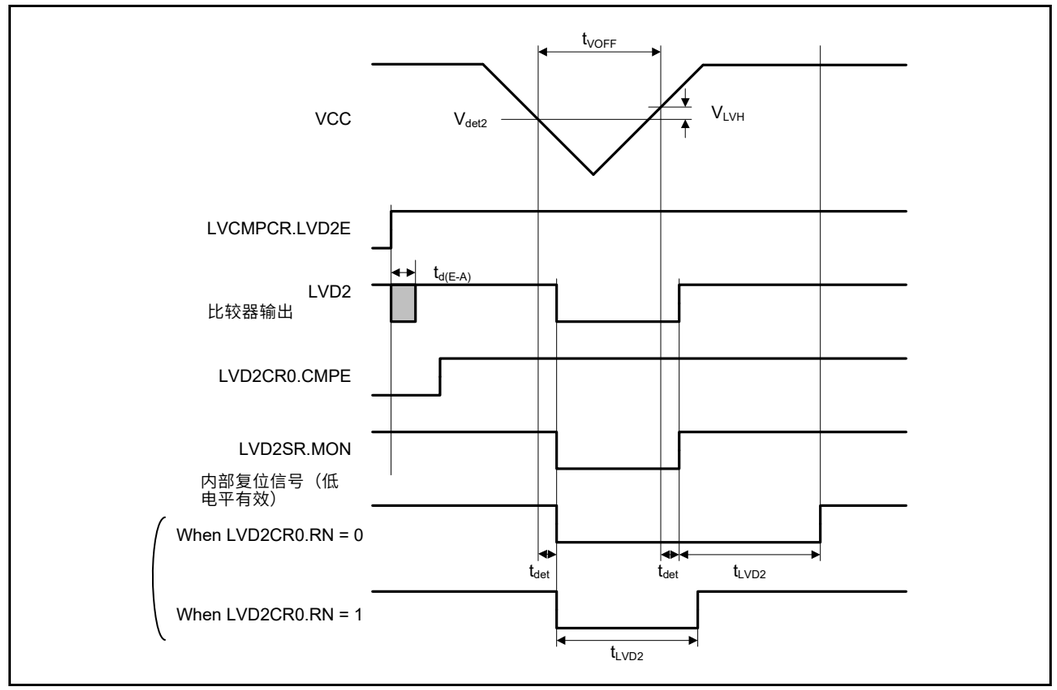


Figure 2.100 电压检测电路时序（Vdet2）

2.10 VBATT Characteristics

Table 2.48 Battery backup function characteristics
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.101
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	-	-	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	-	-	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

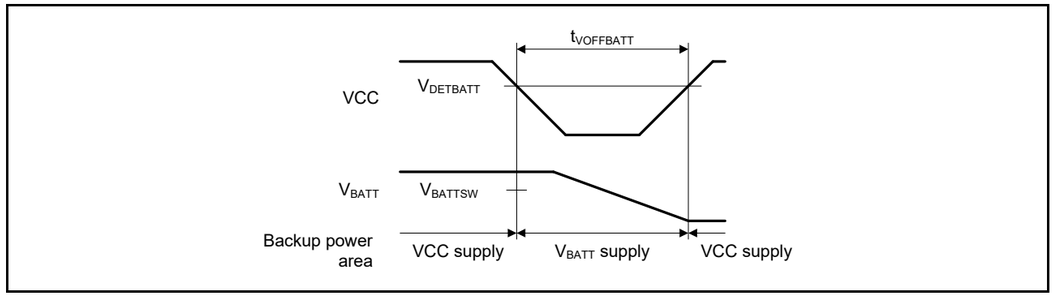


Figure 2.101 Battery backup function characteristics

2.11 CTSU Characteristics

Table 2.49 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{oH}	-	-	-40	mA	When the mutual capacitance method is applied

2.12 ACMPHS Characteristics

Table 2.50 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
Internal reference voltage	Vref	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

2.10 VBATT Characteristics

Table 2.48 电池备份功能特点
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
切换到备用电池的电压电平	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.101
VCC压降引起的电源切换下限VBATT电压	V_{BATTSW}	2.70	-	-	V	
启动电源切换的VCC-off周期	$t_{VOFFBATT}$	200	-	-	µs	

Note: 开始电源切换的VCC-off周期表示VCC低于切换到备用电池的电压电平最小值(VDETBATT)的周期。

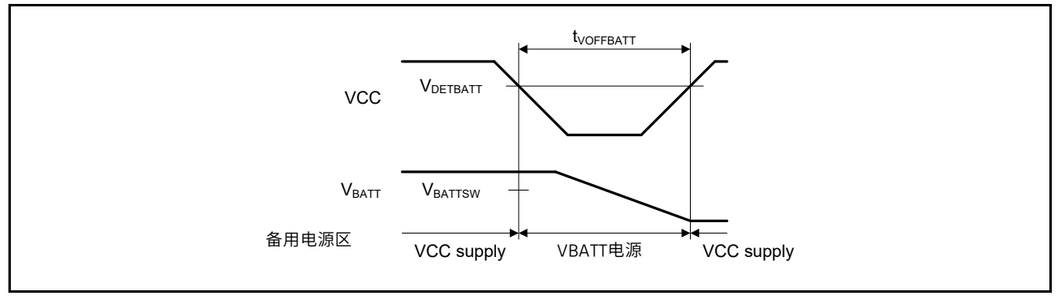


Figure 2.101 电池备份功能特点

2.11 CTSU Characteristics

Table 2.49 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C_{tscap}	9	10	11	nF	-
TS引脚容性负载	C_{base}	-	-	50	pF	-
允许输出大电流	ΣI_{oH}	-	-	-40	mA	应用互电容法时

2.12 ACMPHS Characteristics

Table 2.50 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
参考电压范围	VREF	0	-	AVCC0	V	-
输入电压范围	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
内部参考电压	Vref	1.13	1.18	1.23	V	-

Note 1. 该值是内部传播延迟。

2.13 PGA Characteristics

Table 2.51 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
Gain error	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
Offset error	Voff	-8	-	8	mV

Table 2.52 PGA characteristics in differential mode (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	-	0.3	V
Differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

2.13 PGA特性

Table 2.51 单模PGA特性

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS输入电压范围	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
增益误差	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
偏移误差	Voff	-8	-	8	mV

Table 2.52 差模下的PGA特性(1of2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS输入电压范围		PGAVSS	-0.5	-	0.3	V
差分输入电压范围	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

Table 2.52 PGA characteristics in differential mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.53 Code flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time $N_{PEC} \leq 100$ times	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
Programming time $N_{PEC} > 100$ times	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
Erasure time $N_{PEC} \leq 100$ times	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
Erasure time $N_{PEC} > 100$ times	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*Note:		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		t_{SPD}	-	-	264	-	-	120	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	-	-	216	-	-	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	-	-	1.7	-	-	1.7	ms	
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note: The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)
Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

Table 2.52 差模下的PGA特性(2of2)

Parameter		Symbol	Min	Typ	Max	Unit
增益误差	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

2.14 闪存特性

2.14.1 代码闪存特性

Table 2.53 代码闪存特性
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程时间NPEC 100次	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
编程时间NPEC>100次	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
擦除时间 NPEC 100次	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
擦除时间 NPEC>100次	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*Note:		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
编程期间暂停延迟		t_{SPD}	-	-	264	-	-	120	µs	
挂起优先模式下擦除期间的第一个挂起延迟		t_{SESD1}	-	-	216	-	-	120	µs	
挂起优先模式下擦除期间的第二挂起延迟		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
擦除优先模式下擦除期间的挂起延迟		t_{SEED}	-	-	1.7	-	-	1.7	ms	
强制停止命令		t_{FD}	-	-	32	-	-	20	µs	
数据保持时间*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note: 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=10 000）时，可以对每个块执行n次擦除。例如，当对8KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止覆盖。）

Note 1. 这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

Note 2. 这表示在指定范围内执行重新编程时特性的最小值。
Note 3. 这个结果是从可靠性测试中获得的。

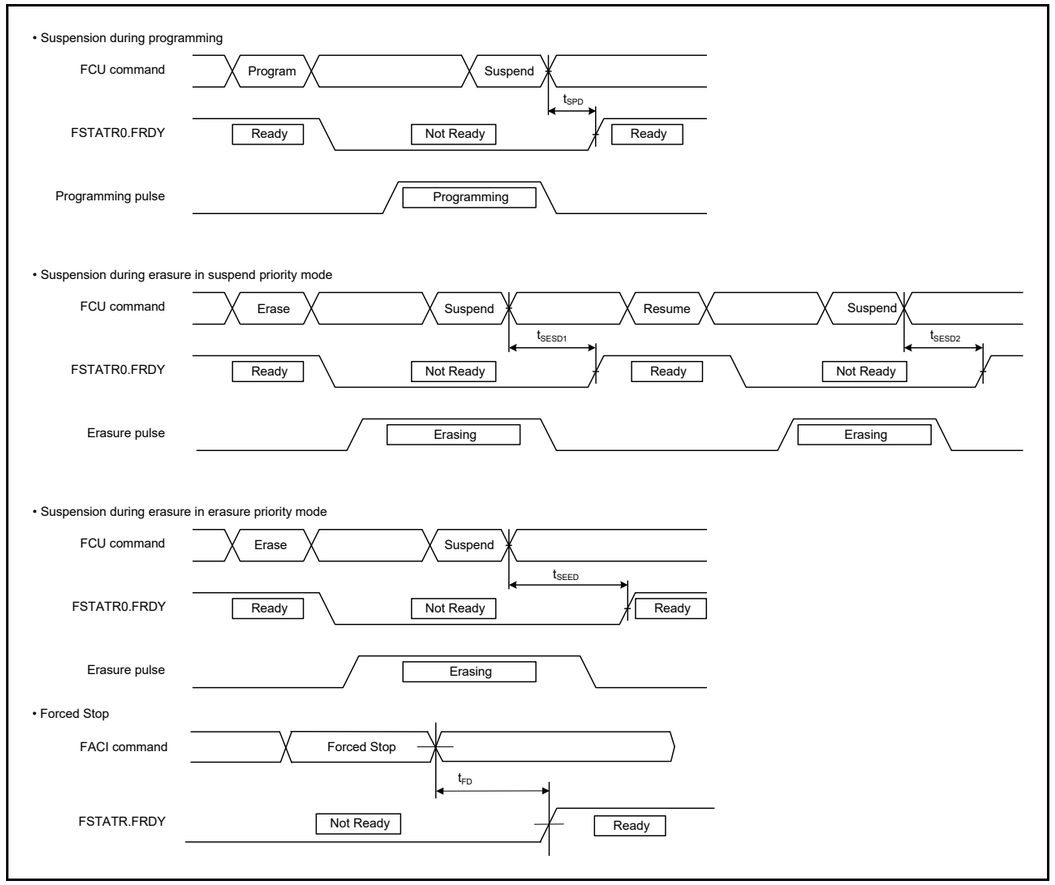


Figure 2.102 Suspension and forced stop timing for flash memory programming and erasure

2.14.2 Data Flash Memory Characteristics

Table 2.54 Data flash memory characteristics (1 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
Erasure time	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000 *2	-	-	125000 *2	-	-	-	

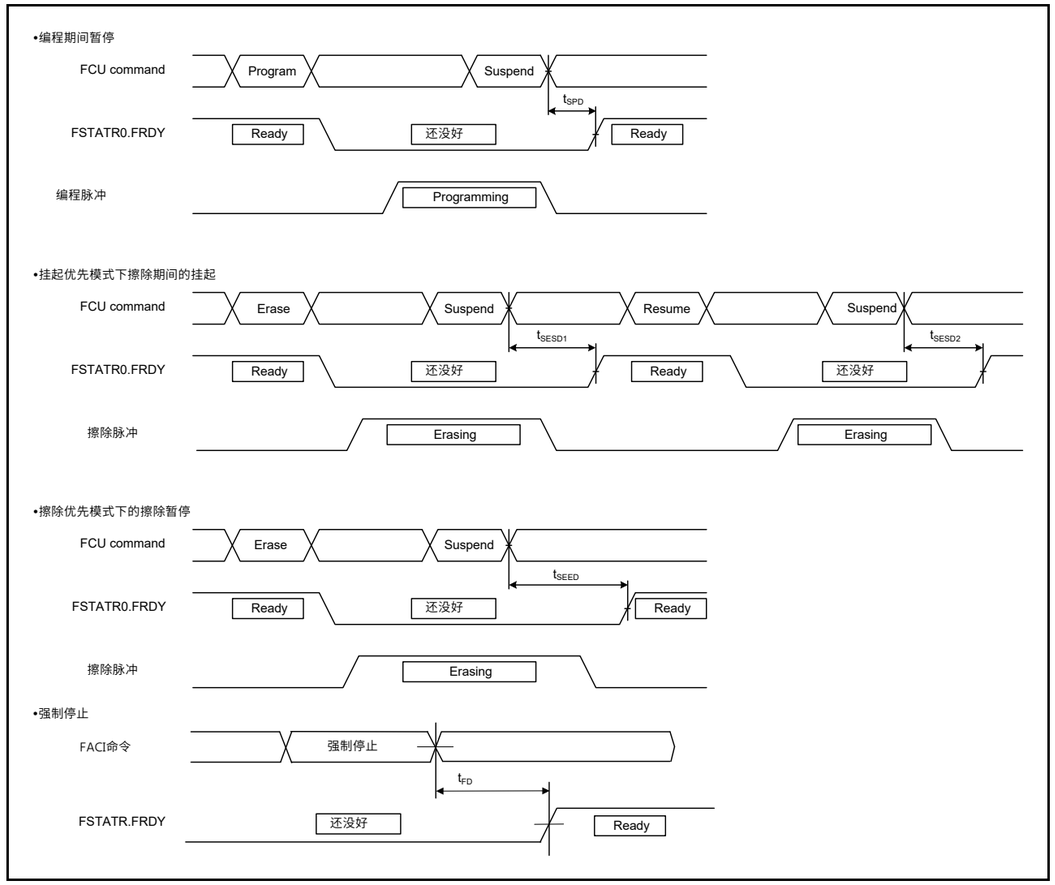


Figure 2.102 闪存编程和擦除的暂停和强制停止时序

2.14.2 数据闪存特性

Table 2.54 数据闪存特性(1of2)
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程时间	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
擦除时间	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
空白检查时间	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000 *2	-	-	125000 *2	-	-	-	

Table 2.54 Data flash memory characteristics (2 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Suspend delay during programming	4-byte	t_{DSPD}	-	-	264	-	-	120	µs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	-	-	216	-	-	120	µs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.

2.15 Boundary Scan

Table 2.55 Boundary scan characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 2.103
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 2.104
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.105

Note 1. Boundary scan does not function until the power-on reset becomes negative.

Table 2.54 数据闪存特性(2of2)
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程期间暂停延迟	4-byte	t_{DSPD}	-	-	264	-	-	120	µs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
挂起优先模式下擦除期间的第一个挂起延迟	64-byte	t_{DSESD1}	-	-	216	-	-	120	µs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
挂起优先模式下擦除期间的第二挂起延迟	64-byte	t_{DSESD2}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
在擦除优先模式下擦除期间暂停延迟	64-byte	t_{DSEED}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
强制停止命令		t_{FD}	-	-	32	-	-	20	µs	
数据保持时间*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=125 000）时，可以对每个块执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止覆盖。）
Note 2. 这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
Note 3. 这表示在指定范围内执行重新编程时特性的最小值。
Note 4. 这个结果是从可靠性测试中获得的。

2.15 边界扫描

Table 2.55 边界扫描特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	100	-	-	ns	Figure 2.103
TCK时钟高脉冲宽度	t_{TCKH}	45	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	45	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	
TMS设置时间	t_{TMSS}	20	-	-	ns	Figure 2.104
TMS保持时间	t_{TMSH}	20	-	-	ns	
TDI建立时间	t_{TDIS}	20	-	-	ns	
TDI保持时间	t_{TDIH}	20	-	-	ns	
TDO数据延迟	t_{TDOD}	-	-	40	ns	
边界扫描电路启动时间*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.105

Note 1. 在上电复位变为负值之前，边界扫描不起作用。

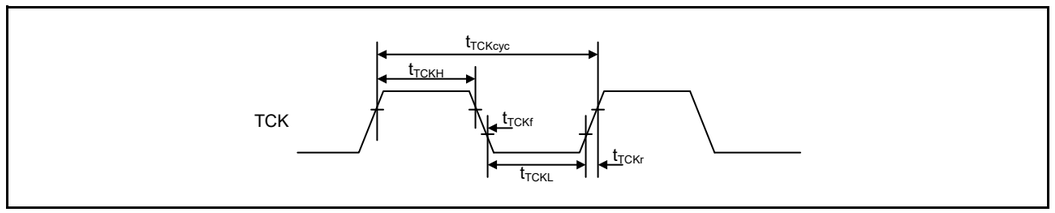


Figure 2.103 Boundary scan TCK timing

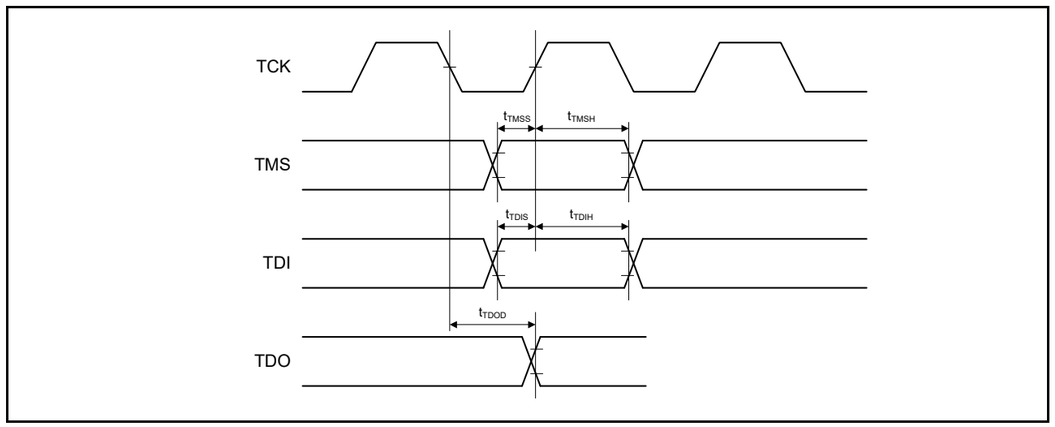


Figure 2.104 Boundary scan input/output timing

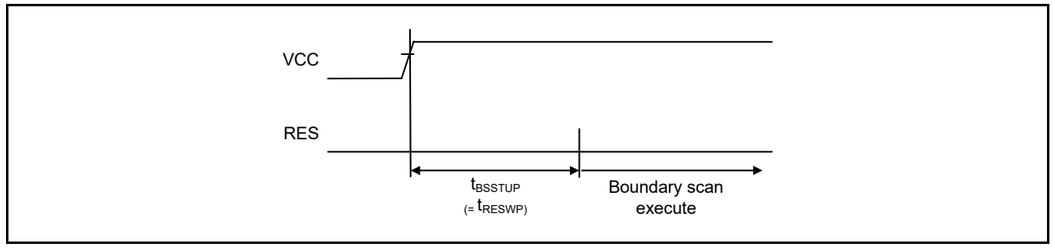


Figure 2.105 Boundary scan circuit startup timing

2.16 Joint Test Action Group (JTAG)

Table 2.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	-	-	ns	Figure 2.103
TCK clock high pulse width	t_{TCKH}	15	-	-	ns	
TCK clock low pulse width	t_{TCKL}	15	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	

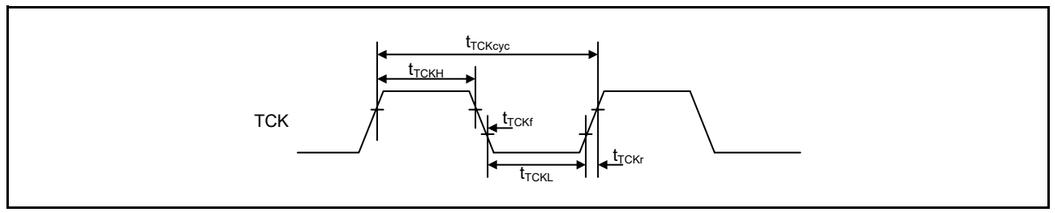


Figure 2.103 边界扫描TCK时序

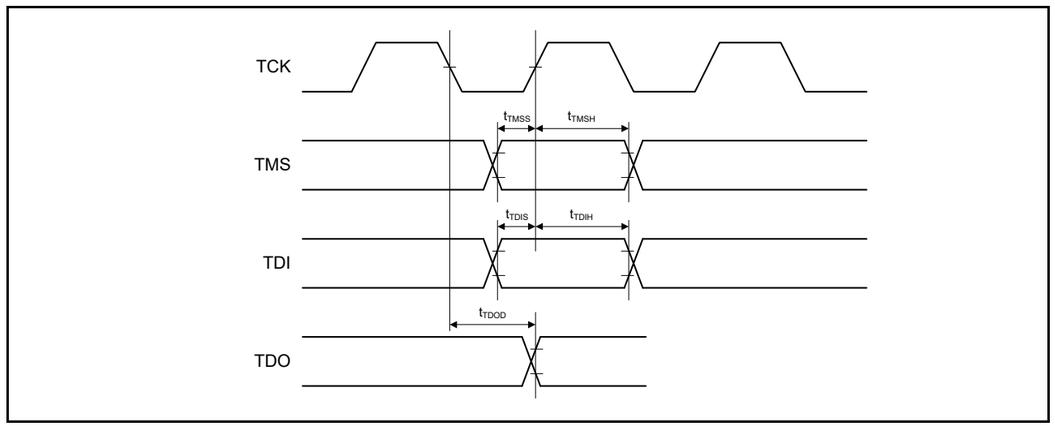


Figure 2.104 边界扫描输入输出时序

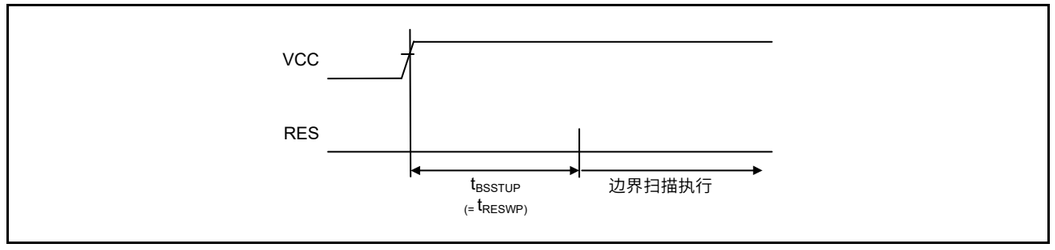


Figure 2.105 边界扫描电路启动时序

2.16 联合测试行动组(JTAG)

Table 2.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	40	-	-	ns	Figure 2.103
TCK时钟高脉冲宽度	t_{TCKH}	15	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	15	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	

Table 2.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	t_{TMSS}	8	-	-	ns	Figure 2.104
TMS hold time	t_{TMSH}	8	-	-	ns	
TDI setup time	t_{TDIS}	8	-	-	ns	
TDI hold time	t_{TDIH}	8	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	20	ns	

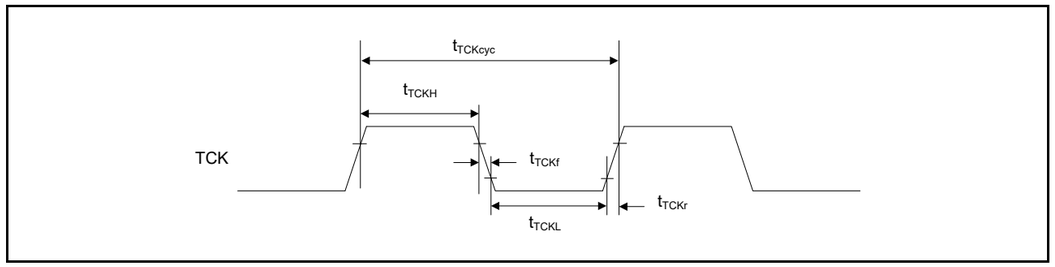


Figure 2.106 JTAG TCK timing

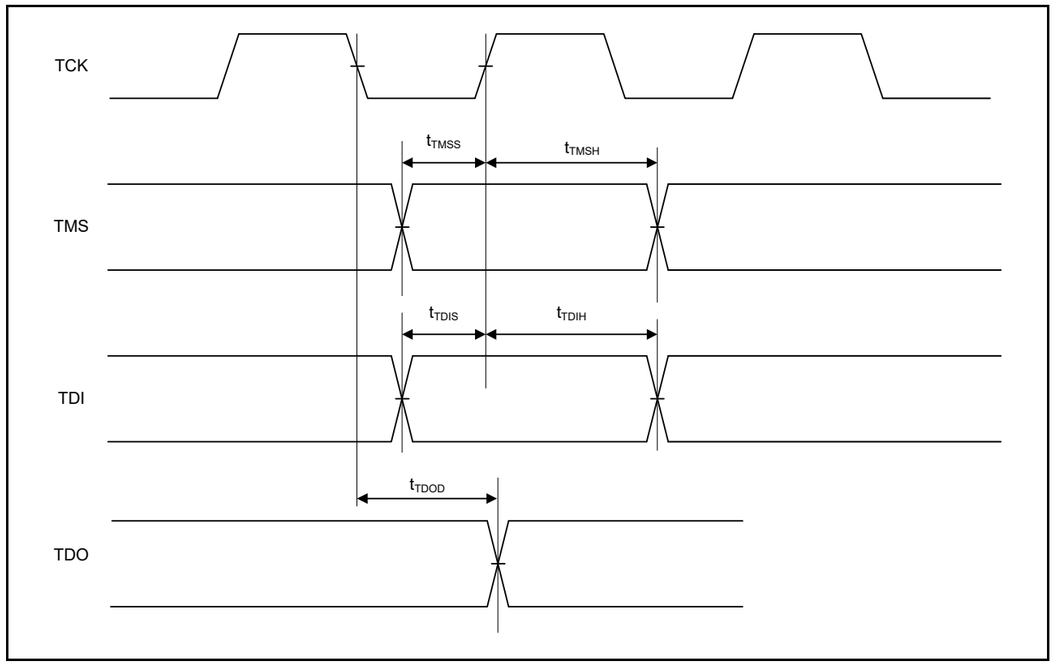


Figure 2.107 JTAG input/output timing

Table 2.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TMS设置时间	t_{TMSS}	8	-	-	ns	Figure 2.104
TMS保持时间	t_{TMSH}	8	-	-	ns	
TDI建立时间	t_{TDIS}	8	-	-	ns	
TDI保持时间	t_{TDIH}	8	-	-	ns	
TDO数据延迟时间	t_{TDOD}	-	-	20	ns	

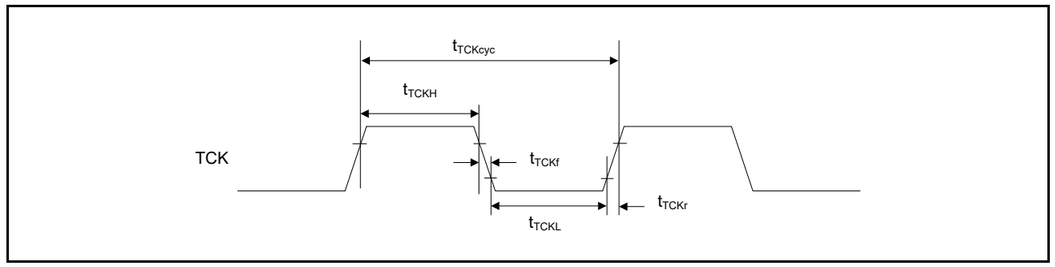


Figure 2.106 JTAG TCK timing

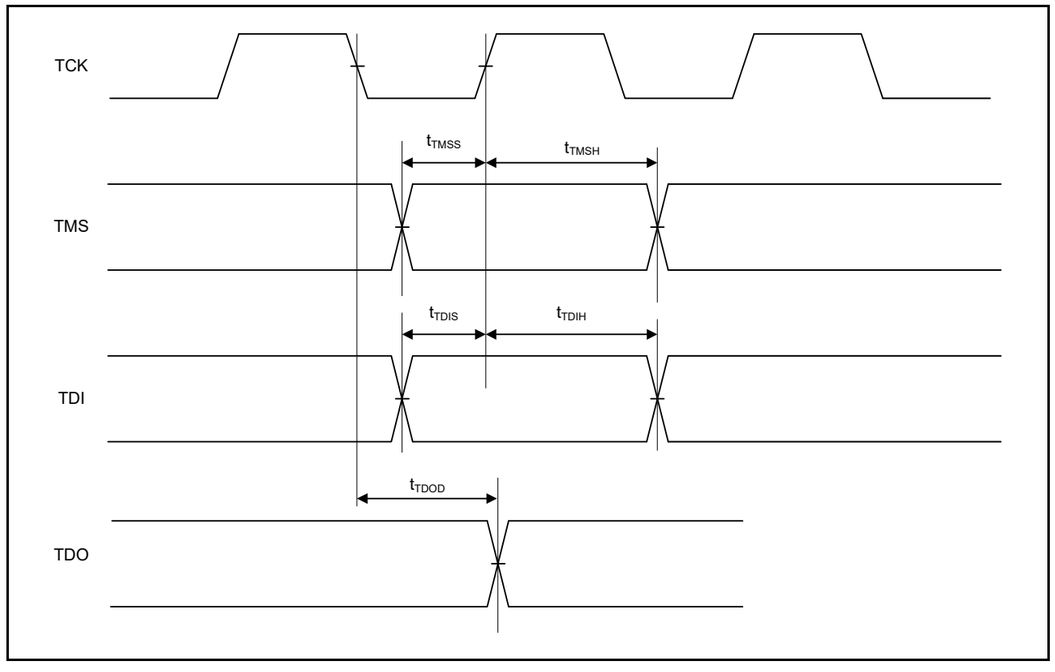


Figure 2.107 JTAG input/output timing

2.17 Serial Wire Debug (SWD)

Table 2.57 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.108
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 2.109
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

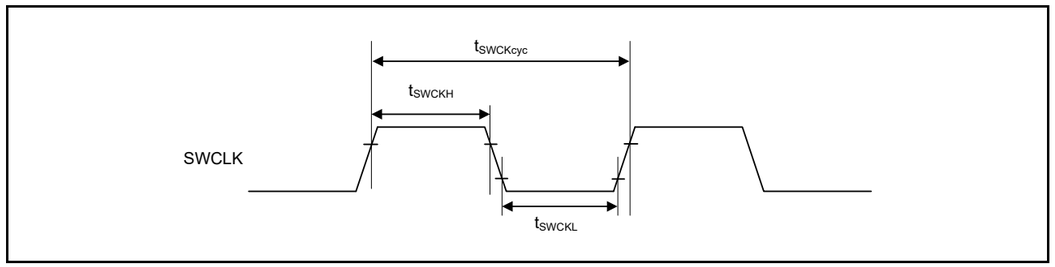


Figure 2.108 SWD SWCLK timing

2.17 串行线调试(SWD)

Table 2.57 SWD

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.108
SWCLK时钟高脉冲宽度	t_{SWCKH}	15	-	-	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	15	-	-	ns	
SWCLK时钟上升时间	t_{SWCKr}	-	-	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	-	-	5	ns	
SWDIO设置时间	t_{SWDS}	8	-	-	ns	Figure 2.109
SWDIO保持时间	t_{SWDH}	8	-	-	ns	
SWDIO数据延迟时间	t_{SWDD}	2	-	28	ns	

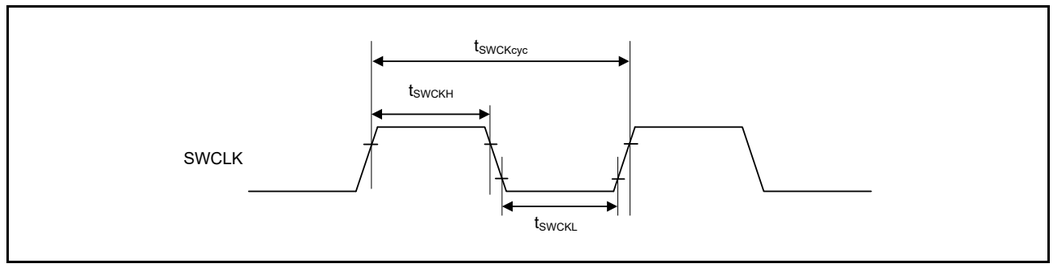


Figure 2.108 SWD SWCLK timing

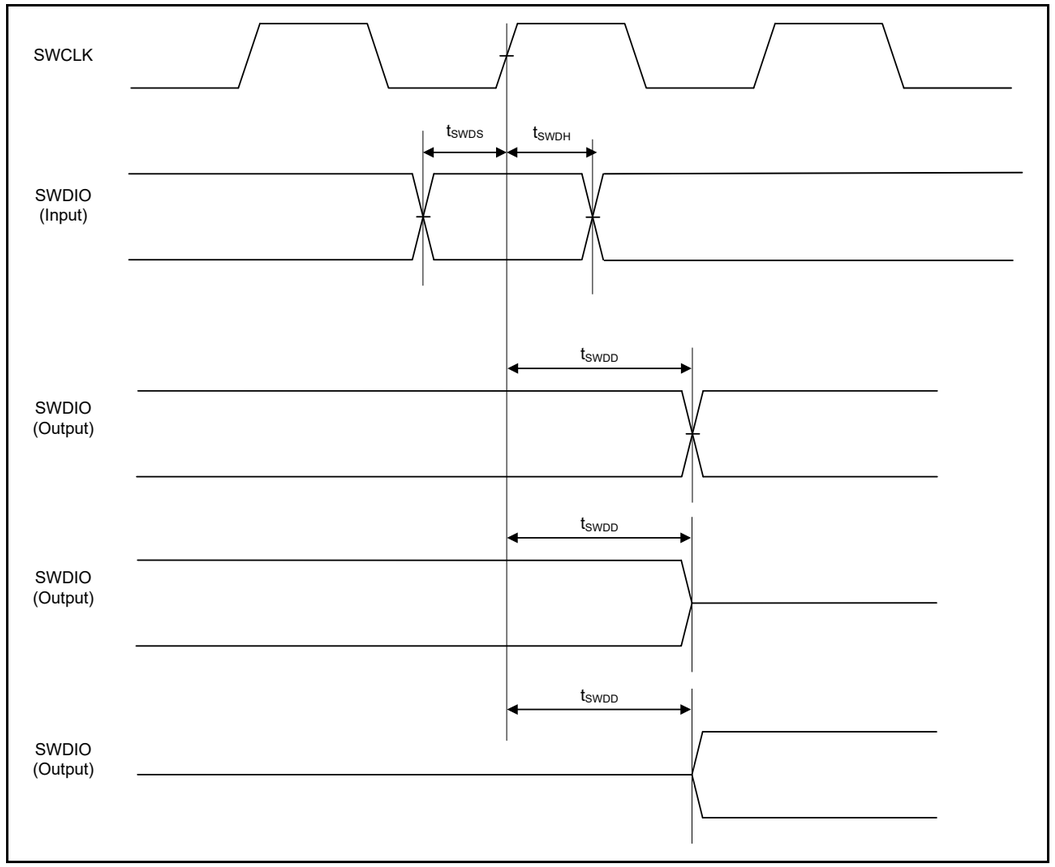


Figure 2.109 SWD input/output timing

2.18 Embedded Trace Macro Interface (ETM)

Table 2.58 ETM
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 2.110
TCLK clock high pulse width	t_{TCLKH}	13.6	-	-	ns	
TCLK clock low pulse width	t_{TCLKL}	13.6	-	-	ns	
TCLK clock rise time	t_{TCLKr}	-	-	3	ns	
TCLK clock fall time	t_{TCLKf}	-	-	3	ns	
TDATA[3:0] output setup time	t_{TRDS}	3.5	-	-	ns	Figure 2.111
TDATA[3:0] output hold time	t_{TRDH}	2.5	-	-	ns	

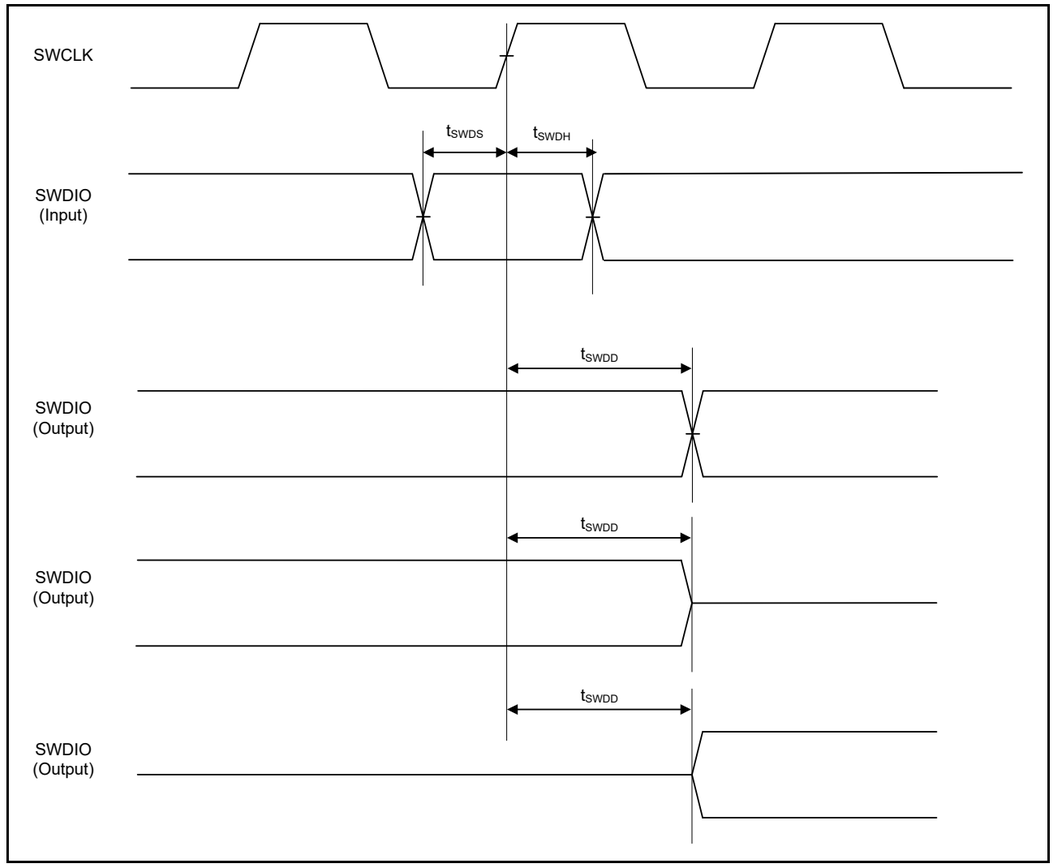


Figure 2.109 SWD input/output timing

2.18 嵌入式跟踪宏接口(ETM)

Table 2.58 ETM
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCLK时钟周期时间	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 2.110
TCLK时钟高脉冲宽度	t_{TCLKH}	13.6	-	-	ns	
TCLK时钟低脉冲宽度	t_{TCLKL}	13.6	-	-	ns	
TCLK时钟上升时间	t_{TCLKr}	-	-	3	ns	
TCLK时钟下降时间	t_{TCLKf}	-	-	3	ns	
TDATA[3:0]输出建立时间	t_{TRDS}	3.5	-	-	ns	Figure 2.111
TDATA[3:0]输出保持时间	t_{TRDH}	2.5	-	-	ns	

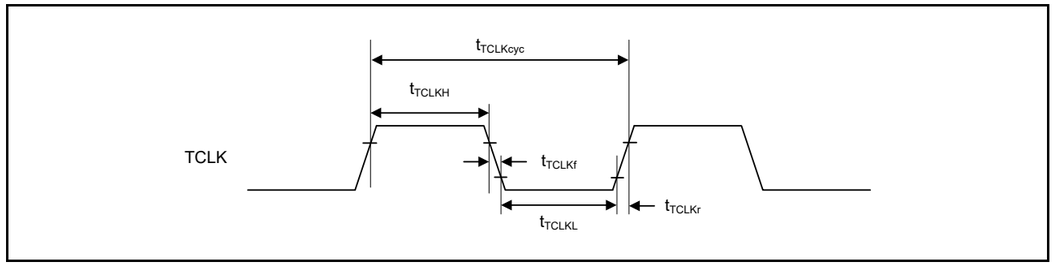


Figure 2.110 ETM TCLK timing

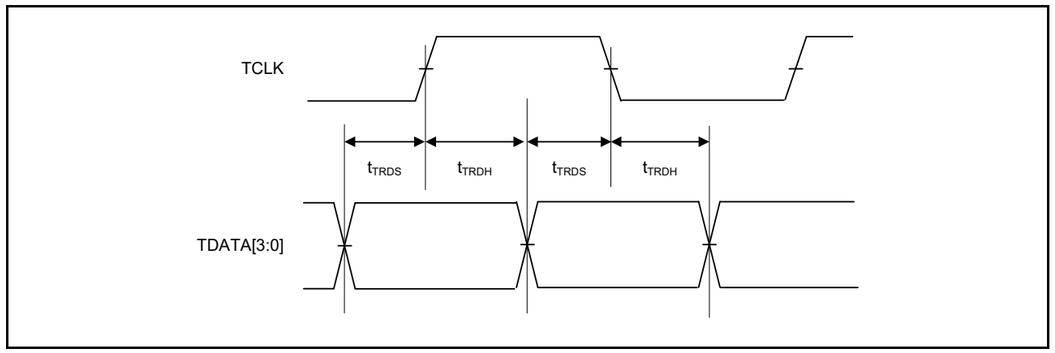


Figure 2.111 ETM output timing

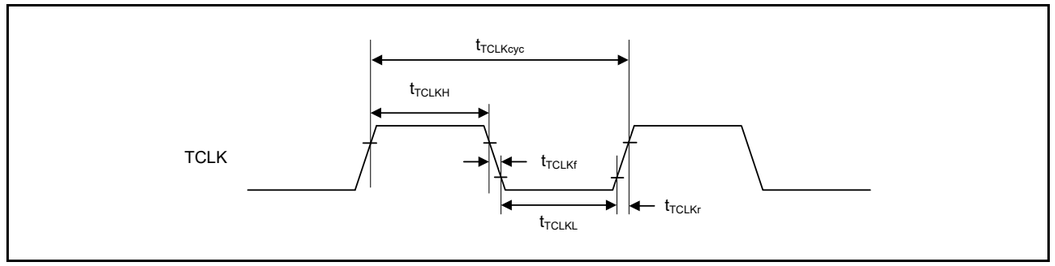


Figure 2.110 ETM TCLK timing

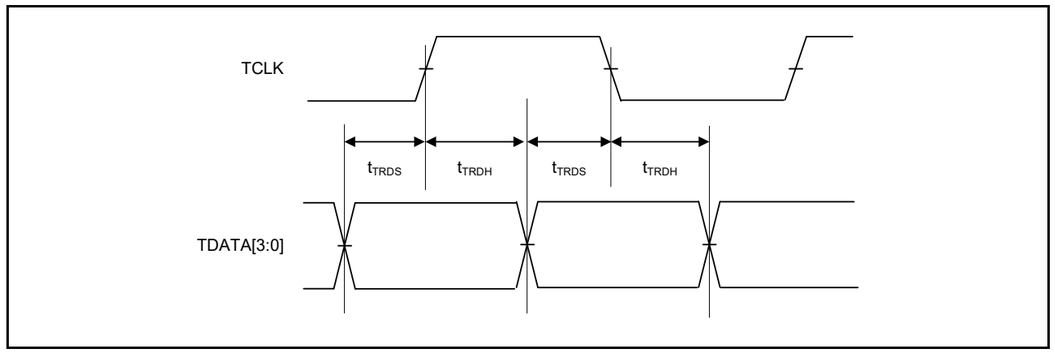
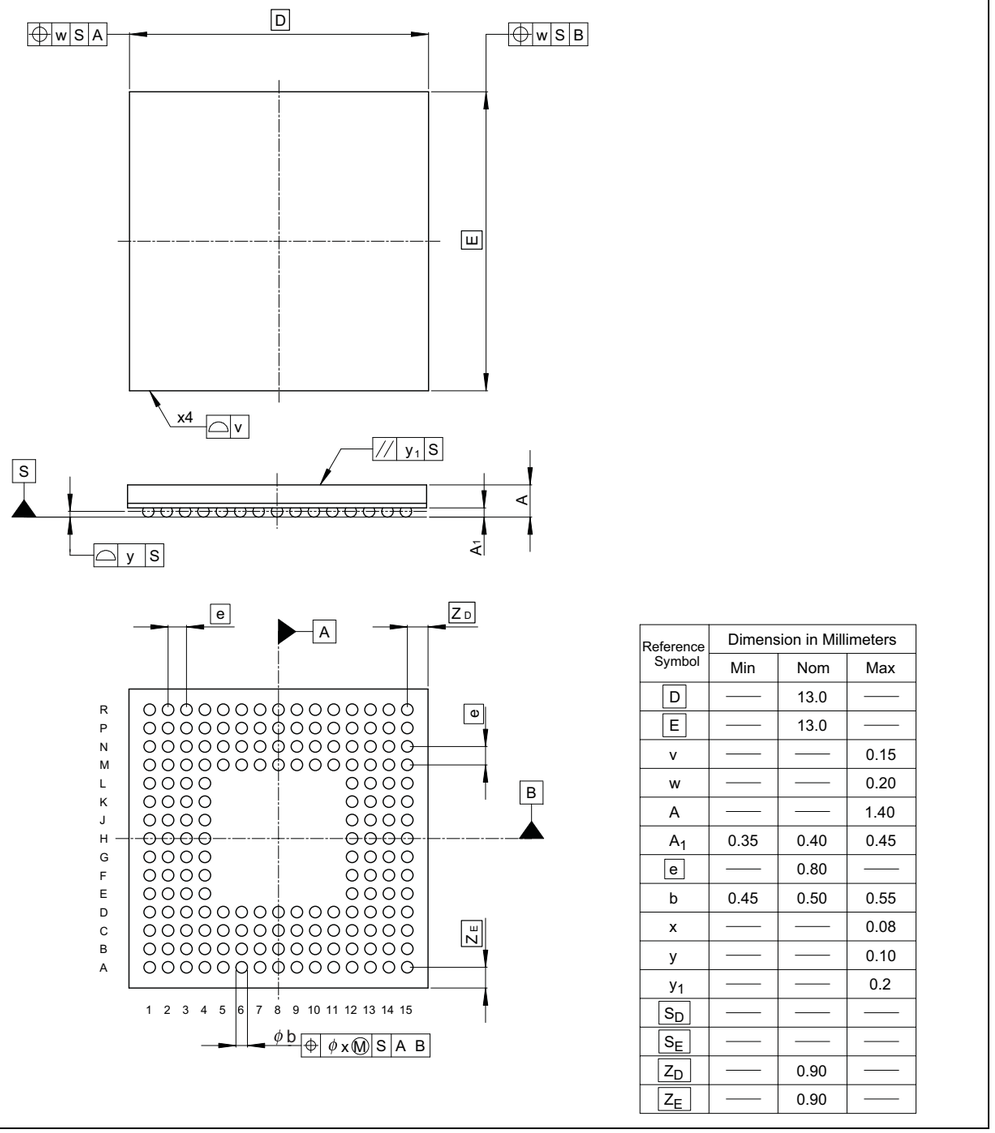


Figure 2.111 ETM输出时序

Appendix 1.Package Dimensions

For information on the latest version of the package dimensions or mountings, go to “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g



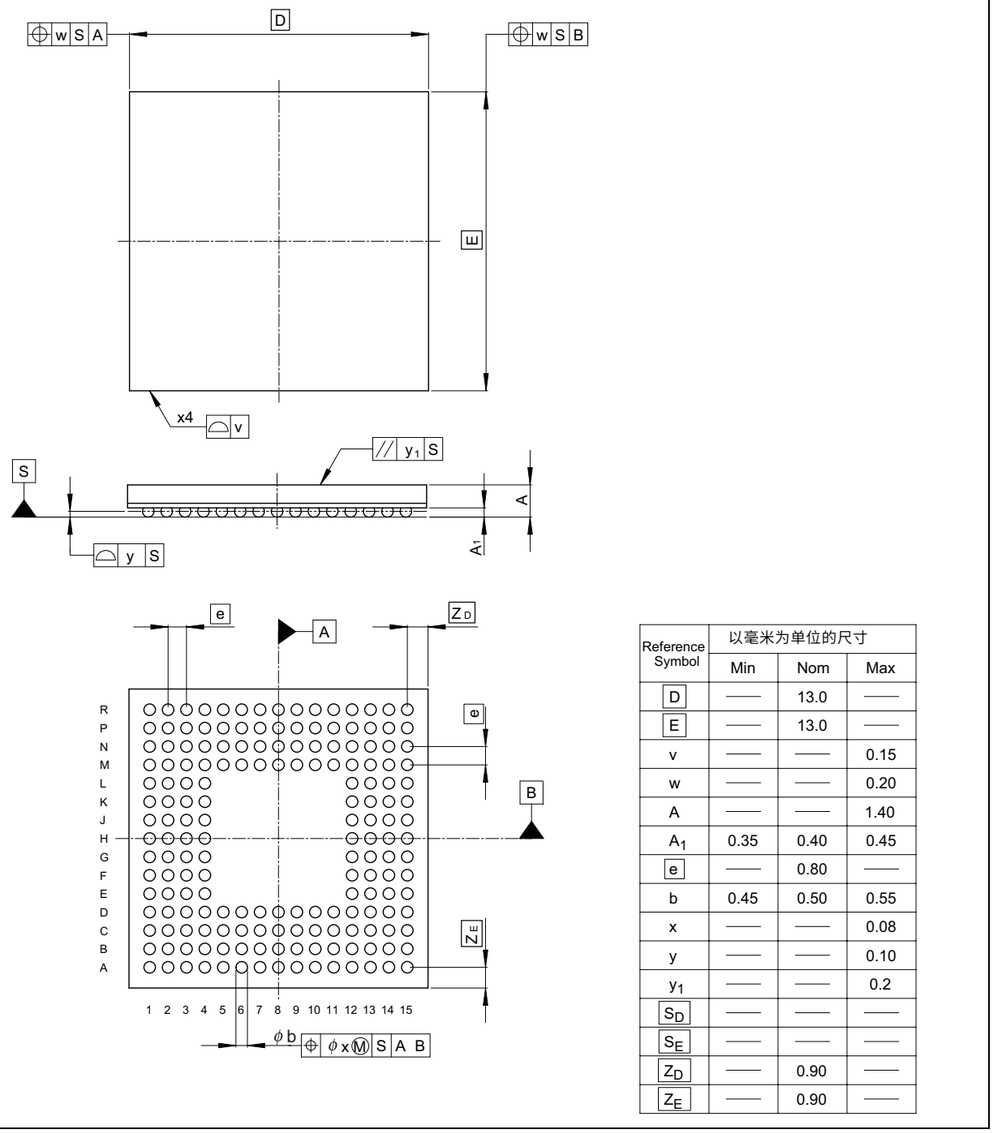
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	13.0	——
E	——	13.0	——
v	——	——	0.15
w	——	——	0.20
A	——	——	1.40
A_1	0.35	0.40	0.45
e	——	0.80	——
b	0.45	0.50	0.55
x	——	——	0.08
y	——	——	0.10
y_1	——	——	0.2
S_D	——	——	——
S_E	——	——	——
Z_D	——	0.90	——
Z_E	——	0.90	——

Figure 1.1 176-pin BGA

附录1.包装尺寸

有关最新版本的封装尺寸或安装信息，请访问Renesas上的“封装”电子公司网站。

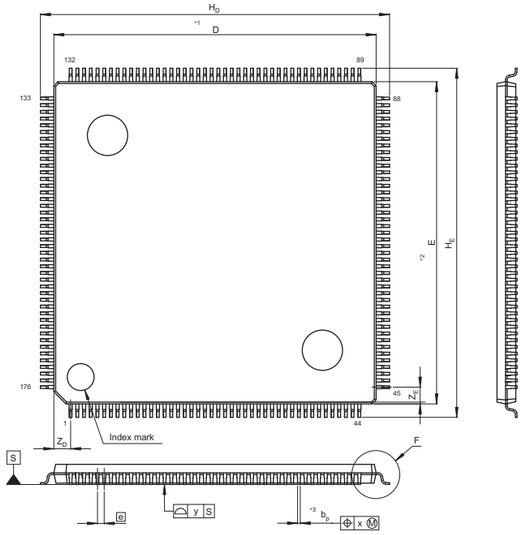
JEITA包装代码	RENESAS Code	以前的代码	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g



Reference Symbol	以毫米为单位的尺寸		
	Min	Nom	Max
D	——	13.0	——
E	——	13.0	——
v	——	——	0.15
w	——	——	0.20
A	——	——	1.40
A_1	0.35	0.40	0.45
e	——	0.80	——
b	0.45	0.50	0.55
x	——	——	0.08
y	——	——	0.10
y_1	——	——	0.2
S_D	——	——	——
S_E	——	——	——
Z_D	——	0.90	——
Z_E	——	0.90	——

Figure 1.1 176-pin BGA

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g

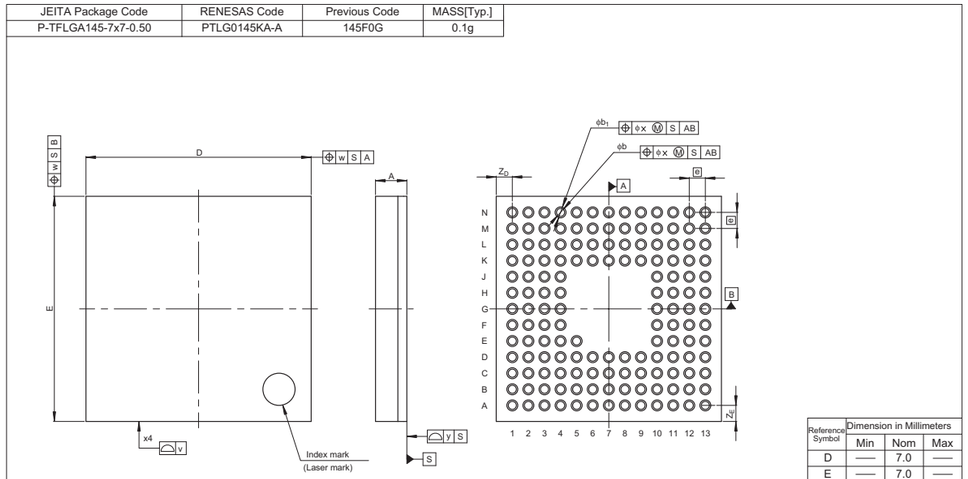


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 1.2 176-pin LQFP

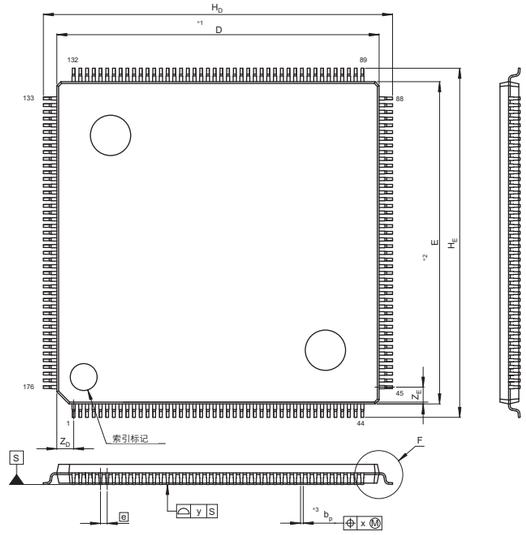
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 1.3 145-pin LGA

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g

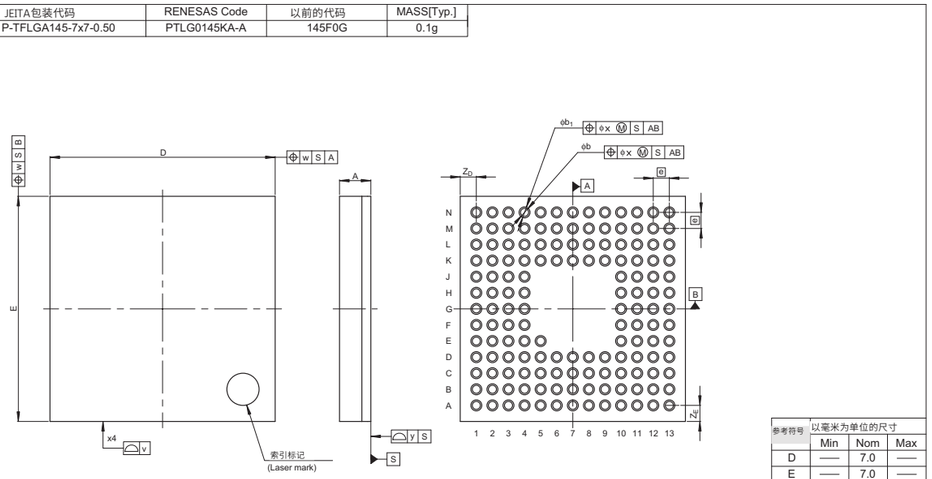


NOTE)
1.尺寸"*1"和"*2"
不包括模具溢料。
2.尺寸"*3"不
包括修剪偏移。

参考符号	以毫米为单位的尺寸		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 1.2 176-pin LQFP

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g

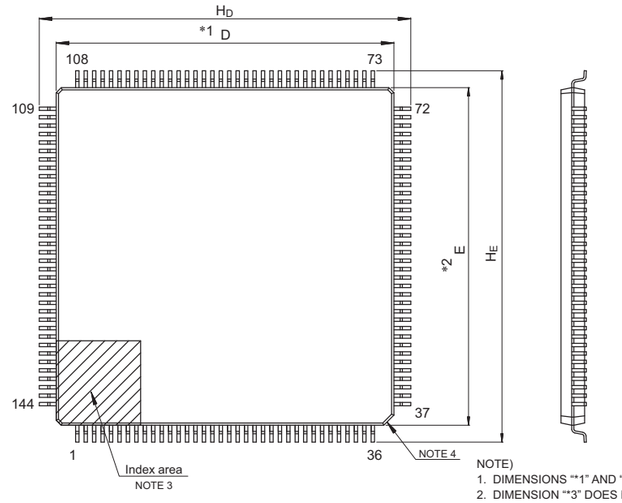


参考符号	以毫米为单位的尺寸		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 1.3 145-pin LGA

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



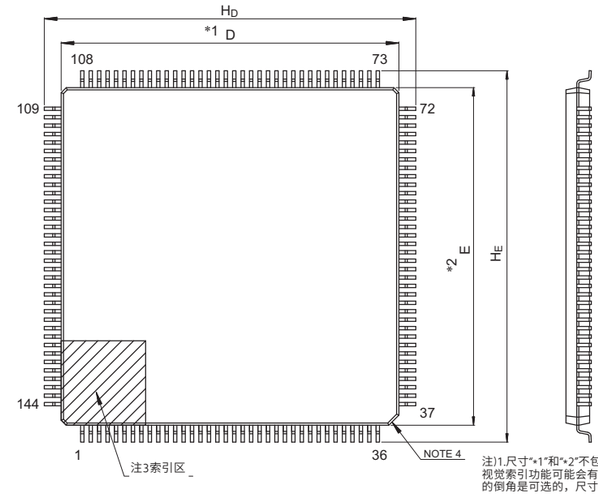
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.4 144-pin LQFP

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



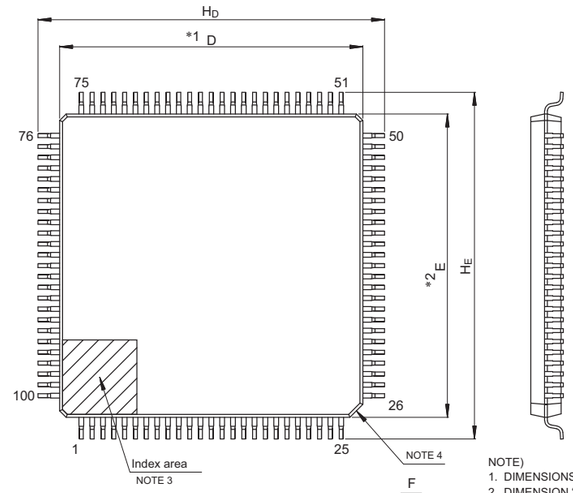
注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.4 144-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



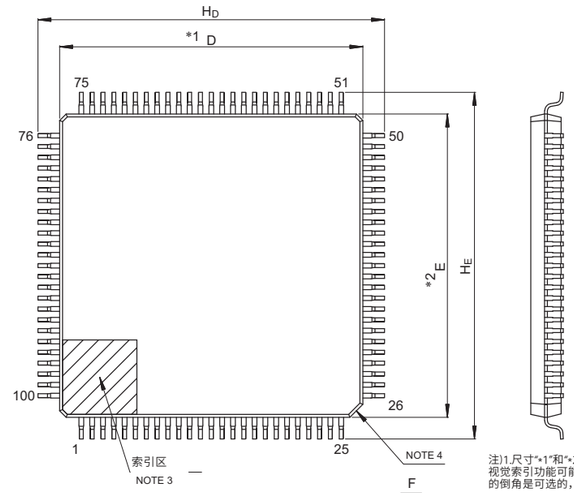
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.5 100-pin LQFP

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.5 100-pin LQFP

Revision History	RA6M3 Group Datasheet

Rev.	Date	Summary
1.00	Oct 8, 2019	First Edition issued
1.10	Dec 25, 2020	Second Edition issued

Proprietary Notice

修订记录	RA6M3 Group Datasheet

Rev.	Date	Summary
1.00	Oct 8, 2019	第一版发行
1.10	Dec 25, 2020	第二版发行

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RA6M3 Group Datasheet

Publication Date: Rev.1.10 Dec 25, 2020

Published by: Renesas Electronics Corporation

RA6M3 Group Datasheet

Publication Date: Rev.1.10 Dec 25, 2020

Published by: 瑞萨电子公司

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

处理微处理单元和微控制器的一般注意事项单位产品

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   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量包括工作台和地板在内的工具必须接地。操作员还必须使用腕带接地。半导体器件不得赤手触摸。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。
2. 上电处理
   通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态在通过片内上电复位功能复位的产品中，从供电时间到供电达到指定重置的级别。
3. 断电状态下的信号输入
   请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部元件劣化。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。
4. 处理未使用的引脚
   按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。
5. 时钟信号
   应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到产生的时钟信号在程序执行过程中使用外部谐振器或外部振荡器，等待目标时钟信号稳定。
6. 输入引脚的电压施加波形
   由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在VIL(Max.)之间的区域和VIH(Min.)，例如，设备可能会发生故障。输入电平时注意防止抖动噪声进入设备是固定的，并且在输入电平通过VIL(Max.)和VIH(Min.)之间的区域时也是如此。
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6. 瑞萨电子产品根据以下两个质量等级进行分类：“标准”和“高质量”。每个瑞萨电子产品的预期应用取决于产品的质量等级，如下所示。“标准”：

   电脑;办公用品;通讯设备；测试和测量设备；视听设备；家用电器；机械工具;个人电子设备；工业机器人；等等

   “高品质”：运输设备（汽车、火车、轮船等）；交通管制（红绿灯）；大型通讯设备；关键金融终端系统；安全控制设备；除非在瑞萨电子数据表或其他瑞萨电子文档中明确指定为高可靠性产品或适用于恶劣环境的产品，否则瑞萨电子产品不得用于或授权用于可能对人类构成直接威胁的产品或系统生命或身体伤害（人工生命支持设备或系统；外科植入物等），或可能造成严重财产损失（空间系统；海底中继器；核电控制系统；飞机控制系统；关键工厂系统；军事装备等）。）。对于您或任何第三方因使用与任何瑞萨电子数据表、用户手册或其他瑞萨电子文档不一致的任何瑞萨电子产品而导致的任何损害或损失，瑞萨电子不承担任何责任。
7. 没有半导体产品是绝对安全的。尽管瑞萨电子硬件或软件产品中可能实施任何安全措施或功能，但瑞萨电子绝对不承担因任何漏洞或安全漏洞引起的任何责任，包括但不限于任何未经授权访问或使用瑞萨电子产品或使用瑞萨电子产品的系统。瑞萨电子不保证或保证瑞萨电子产品或使用瑞萨电子产品创建的任何系统不会受到损坏、攻击、病毒、干扰、

   黑客攻击、数据丢失或盗窃或其他安全入侵（“漏洞问题”）。瑞萨电子不承担任何和
   由任何漏洞问题引起或与之相关的所有责任或义务。此外，在某种程度上
   在适用法律允许的情况下，瑞萨电子不提供任何明示或暗示的保证，包括
   关于本文档和任何相关或随附的软件或硬件，包括但不限于
   对适销性或特定用途适用性的默示保证。
8. 使用瑞萨电子产品时，请参阅最新的产品信息（数据表、用户手册、应用说明、“通用说明
   处理和使用半导体器件”在可靠性手册等），并确保使用条件在规定的范围内
   瑞萨电子关于最大额定值、工作电源电压范围、散热特性、安装等方面的信息。瑞萨电子不对因在上述规定范围之外使用瑞萨电子产品而引起的任何故障、故障或事故承担任何责任.

9.尽管瑞萨电子努力提高瑞萨电子产品的质量和可靠性，但半导体产品具有特定的特性，例如以一定的速率发生故障以及在特定的使用条件下发生故障。除非在瑞萨电子数据表或其他瑞萨电子文档中指定为高可靠性产品或适用于恶劣环境的产品，否则瑞萨电子产品不受抗辐射设计的约束。您有责任实施安全措施，以防止在瑞萨电子产品出现故障或故障时可能造成人身伤害、火灾造成的伤害或损害以及/或对公众造成危险，例如硬件和软件的安全设计，包括但不限于冗余、火灾控制和故障预防、老化退化的适当处理或任何其他适当的措施。因为单单评估微机软件是非常困难和不切实际的，您有责任评估您制造的最终产品或系统的安全性。10.请联系瑞萨电子销售办事处了解有关环境问题的详细信息，例如每个瑞萨电子产品的环境兼容性。您有责任仔细、充分地调查适用于管制物质的包含或使用的法律和法规，包括但不限于欧盟RoHS指令，并按照所有这些适用的法律和法规使用瑞萨电子产品。瑞萨电子对因您不遵守适用法律和法规而造成的损害或损失不承担任何责任。11.瑞萨电子的产品和技术不得用于或整合到任何适用的国内或国外法律或法规禁止制造、使用或销售的产品或系统中。您应遵守对各方或交易主张管辖权的任何国家/地区的政府颁布和管理的任何适用的出口管制法律和法规。12.瑞萨电子产品的购买者或分销商，或将产品分销、处置或以其他方式出售或转让给第三方的任何其他方，有责任提前通知该第三方有关内容和条件本文件中规定。13.未经瑞萨电子事先书面同意，不得以任何形式全部或部分翻印、复制或复制本文档。14.如果您对本文档中包含的信息或瑞萨电子产品有任何疑问，请联系瑞萨电子销售办事处。

(Note1) 本文档中使用的“瑞萨电子”是指瑞萨电子公司，还包括其直接或间接控制的子公司。
(Note2) “瑞萨电子产品”是指由瑞萨电子开发或制造或为瑞萨电子开发或制造的任何产品。

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